

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.



08/03/04

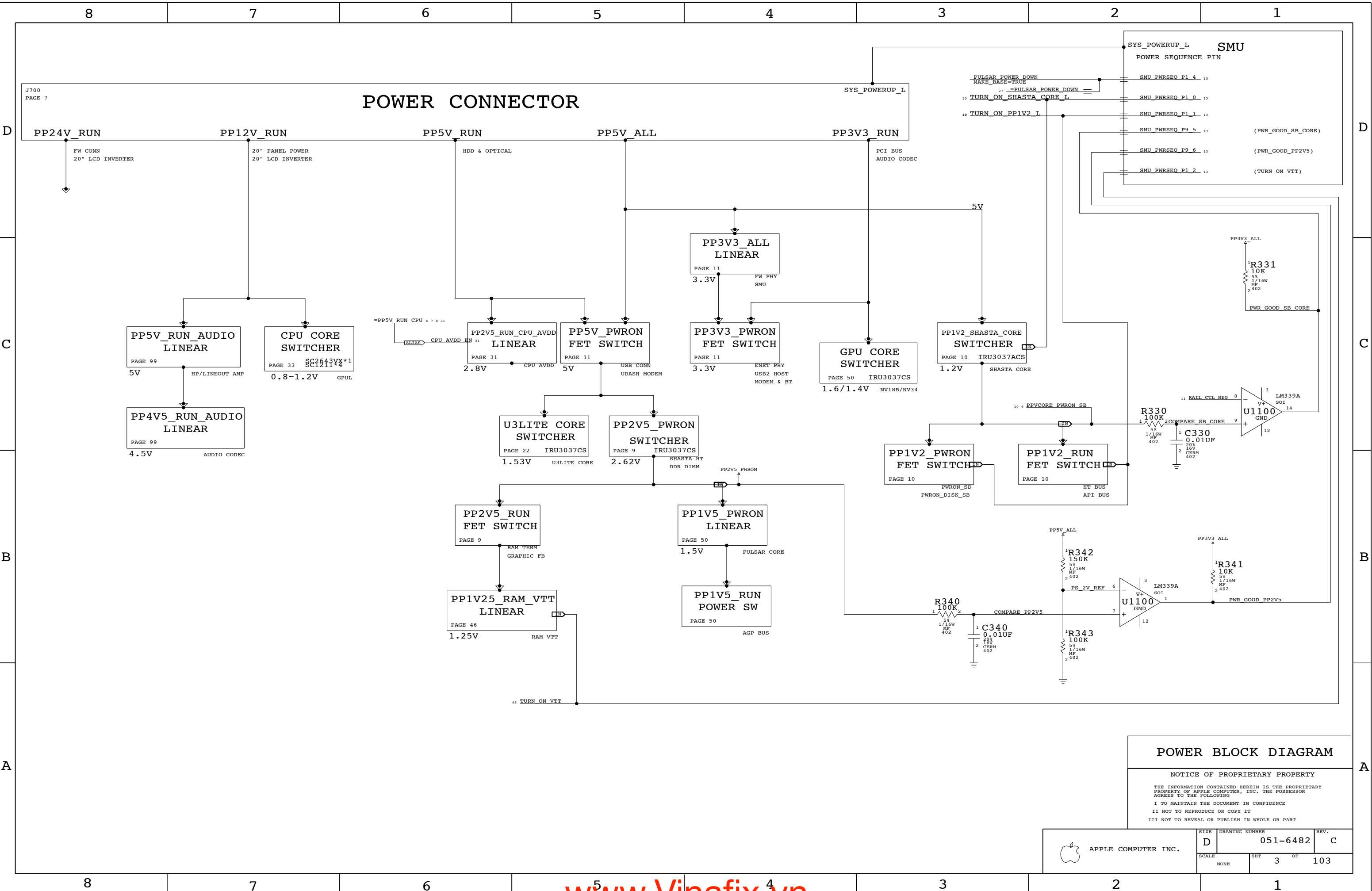
REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
C		338723	PRODUCTION RELEASED	DATE	DATE
				08/04/04	?

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<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <p style="text-align: center;">  <small>THIRD ANGLE PROJECTION</small> </p>	<p>METRIC</p>	 <p>Apple Computer Inc.</p>	<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>														
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAWER</td> <td style="width: 25%;">DESIGN CK</td> <td style="width: 25%;">MFG APPD</td> <td style="width: 25%;">TITLE</td> </tr> <tr> <td style="width: 25%;">ENG APPD</td> <td style="width: 25%;">DESIGNER</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">DRAWING NUMBER</td> </tr> <tr> <td style="width: 25%;">QA APPD</td> <td style="width: 25%;">NONE</td> <td style="width: 25%;">SIZE</td> <td style="width: 25%;">REV. C</td> </tr> <tr> <td style="width: 25%;">RELEASE</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">NONE</td> <td style="width: 25%;">D</td> </tr> </table>	DRAWER	DESIGN CK	MFG APPD	TITLE	ENG APPD	DESIGNER	SCALE	DRAWING NUMBER	QA APPD	NONE	SIZE	REV. C	RELEASE	SCALE	NONE	D	<p>SCH, MLB, IMG5</p> <p style="font-size: small;">DRAWING NUMBER 051-6482 REV. C</p> <p style="font-size: x-small; text-align: right;">SHT 1 OF 103</p>
DRAWER	DESIGN CK	MFG APPD	TITLE														
ENG APPD	DESIGNER	SCALE	DRAWING NUMBER														
QA APPD	NONE	SIZE	REV. C														
RELEASE	SCALE	NONE	D														



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PROCESSORS

QUALIFIED

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2968	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.6G,85C,ARA	1.6GHZ	1.25V	45W	?	U2900	CPU_DD30_1_6GHZ
337S2969	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.8G,85C,BPA	1.8GHZ	1.20V	45W	?	U2900	CPU_DD30_1_8GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S2970	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BRA	1.25V

NOT QUALIFIED

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S2957	337S2786	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BNA	1.20V

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2865	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD2.11,1.8GHZ,85C	1.8GHZ	1.45V	45W	?	U2900	CPU_DD211_1_8GHZ
337S2866	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD2.11,2.0GHZ,85C	2.0GHZ	1.45V	45W	?	U2900	CPU_DD211_2_0GHZ
337S2787	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,REV3,2.0G,85C,CJA	2.0GHZ	1.25V	45W	?	U2900	CPU_DD30_2_0GHZ

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
820-1540	1	PCB,FAB,MLB	MLB1	
825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
051-6482	1	PCB,SCHEM,MLB	SCH1	
341T1366	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
341T1395	1	PURCH ASSY, SMU BIG	U1300	
CRITICAL 603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL 603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114	LED700	LED702	LED5900 KINGBRIGHT LED

TABLE ITEMS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	C
SCALE	SHT	OF
NONE	5	103


	8	7	6	5	4	3	2	1	
D	<pre> 1430 NO_TEST=YES TP_BUF_RST 57 1431 NO_TEST=YES TP_DFPCLK 57 1432 NO_TEST=YES TP_DFPCLK_L 58 1433 NO_TEST=YES TP_DFPD0 58 1434 NO_TEST=YES TP_DFPD1 58 1435 NO_TEST=YES TP_DFPD2 58 1436 NO_TEST=YES TP_DFPD3 58 1437 NO_TEST=YES TP_DFPD5 58 1438 NO_TEST=YES TP_DFPD6 58 1439 NO_TEST=YES TP_EXT_TMDS_CKM 58 1440 NO_TEST=YES TP_EXT_TMDS_CKP 58 1441 NO_TEST=YES TP_EXT_TMDS_D0M 58 1442 NO_TEST=YES TP_EXT_TMDS_D0P 58 1443 NO_TEST=YES TP_EXT_TMDS_D1M 58 1444 NO_TEST=YES TP_EXT_TMDS_D1P 58 1445 NO_TEST=YES TP_EXT_TMDS_D2M 58 1446 NO_TEST=YES TP_EXT_TMDS_D2P 58 1447 NO_TEST=YES TP_FBBCS1_L 52 1448 NO_TEST=YES TP_GPU_INTB_L 49 1449 NO_TEST=YES TP_GPU_THERMA 58 1450 NO_TEST=YES TP_GPU_THERMC 58 1451 NO_TEST=YES TP_IPF1VREF 58 1452 NO_TEST=YES TP_NVAGP_TDO 49 </pre>	<pre> 1430 NO_TEST=YES TP_RAM_CKE_R<3> 8 1431 NO_TEST=YES TP_RAM_CKE_R<6> 8 1432 NO_TEST=YES TP_RAM_CKE_R<7> 8 1433 NO_TEST=YES TP_RAM_CS_L_R<10> 8 1434 NO_TEST=YES TP_RAM_CS_L_R<11> 8 1435 NO_TEST=YES TP_RAM_CS_L_R<2> 8 1436 NO_TEST=YES TP_RAM_CS_L_R<3> 8 1437 NO_TEST=YES TP_RAM_MUXEN0 8 1438 NO_TEST=YES TP_RAM_MUXEN4 8 1439 NO_TEST=YES TP_NB_FM_SLEEP0 24 1440 NO_TEST=YES TP_J4000_SJRESET_L 40 1441 NO_TEST=YES TP_J4001_SJRESET_L 40 1442 NO_TEST=YES TP_CMP_SPARE 8 1443 NO_TEST=YES TP_ENET_TXD<6> 87 1444 NO_TEST=YES U2100_UNUSED 21 1445 NO_TEST=YES PLS_CLK_66M_0_R 27 1446 NO_TEST=YES PLS_CLK_66M_1_R 27 </pre>	<pre> 90 FW_VP_PORT1 FUNC_TEST=YES 91 FW_TPO1P FUNC_TEST=YES 92 FW_TPO1N FUNC_TEST=YES 93 FW_TPI1P FUNC_TEST=YES 94 FW_TPI1N FUNC_TEST=YES 95 FW_VP_PORT2 FUNC_TEST=YES 96 FW_TPO2P FUNC_TEST=YES 97 FW_TPO2N FUNC_TEST=YES 98 FW_TPI2P FUNC_TEST=YES 99 FW_TPI2N FUNC_TEST=YES 100 FW_VGND FUNC_TEST=YES 77 76 75 74 73 PCI_AD<31..0> FUNC_TEST=TRUE 77 76 74 73 PCI_CBE_L<3..0> FUNC_TEST=TRUE 77 76 74 73 PCI_CLK33M_AIRPORT FUNC_TEST=YES 76 74 PCI_SLOTA_REQ_L FUNC_TEST=YES 76 74 PCI_SLOTA_GNT_L FUNC_TEST=YES 76 25 PCI_SLOTA_INT_L FUNC_TEST=YES 74 58 51 8 PCI_RESET_L FUNC_TEST=YES 77 76 74 73 PCI_FRAME_L FUNC_TEST=YES 77 76 74 73 PCI_TRDY_L FUNC_TEST=YES 77 76 74 73 PCI_IRDY_L FUNC_TEST=YES 77 76 74 73 PCI_STOP_L FUNC_TEST=YES 77 76 74 73 PCI_DEVSEL_L FUNC_TEST=YES 77 76 74 73 PCI_PAR FUNC_TEST=YES 76 PCI_SLOTA_DSESEL FUNC_TEST=YES 76 75 74 ROM_CS_L FUNC_TEST=YES 76 75 74 ROM_OE_L FUNC_TEST=YES 76 75 74 ROM_WE_L FUNC_TEST=YES 76 75 ROM_ONBOARD_CS_L FUNC_TEST=YES 76 AIRPORT_CLKRUN_L_PD FUNC_TEST=YES 92 USB_BT_N FUNC_TEST=YES 92 USB_BT_P FUNC_TEST=YES 92 USB2_PORT1_N_F FUNC_TEST=YES 92 USB2_PORT1_P_F FUNC_TEST=YES 92 USB2_PORT2_N_F FUNC_TEST=YES 92 USB2_PORT2_P_F FUNC_TEST=YES 92 USB2_PORT3_N_F FUNC_TEST=YES 92 USB2_PORT3_P_F FUNC_TEST=YES 92 PP5V_USB2_PORT1_F FUNC_TEST=YES 92 PP5V_USB2_PORT2_F FUNC_TEST=YES 92 PP5V_USB2_PORT3_F FUNC_TEST=YES 94 76 25 I2S1_DEV_TO_SB_DTI 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_SYNC 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_BITCLK 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_MCLK 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_SB_TO_DEV_DTO 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_RESET_L 2 TEST POINTS FUNC_TEST=YES 94 25 MODEM_RING2SYS_L 2 TEST POINTS FUNC_TEST=YES 94 18 I2C_UDASH_SDA FUNC_TEST=YES 94 18 I2C_UDASH_SCL FUNC_TEST=YES 94 USB_UDASH_N FUNC_TEST=YES 94 USB_UDASH_P FUNC_TEST=YES 94 UDASH_SDOWN FUNC_TEST=YES 94 UDASH_RESET_L FUNC_TEST=YES 94 UDASH_I2C_AI_PU FUNC_TEST=YES 59 PPVCC_TMDS FUNC_TEST=YES 59 PP3V3_DDC FUNC_TEST=YES 59 TD0M FUNC_TEST=YES 59 TD0P FUNC_TEST=YES 59 TD1M FUNC_TEST=YES 59 TD1P FUNC_TEST=YES 59 TD2M FUNC_TEST=YES 59 TD2P FUNC_TEST=YES 59 TCKM FUNC_TEST=YES 59 TCKP FUNC_TEST=YES 59 TMDS_DDC_DAT FUNC_TEST=YES 59 TMDS_DDC_CLK FUNC_TEST=YES 59 7 GND_CHASSIS_TMDS FUNC_TEST=YES 59 FILT_ANALOG_RED FUNC_TEST=YES 59 FILT_ANALOG_GRN FUNC_TEST=YES 59 FILT_ANALOG_BLU FUNC_TEST=YES 59 56 ANALOG_HSYNC_L FUNC_TEST=YES 59 56 ANALOG_VSYNC_L FUNC_TEST=YES 59 VGA_IIC_CLK FUNC_TEST=YES 59 VGA_IIC_DAT FUNC_TEST=YES 59 58 MON_DETECT FUNC_TEST=YES 59 DDC_VCC_5 FUNC_TEST=YES 59 PP24V_INV FUNC_TEST=YES 59 GND_20_INV FUNC_TEST=YES 59 INV_20_LCD_PWM FUNC_TEST=YES 59 INV_20_CUR_HI_F FUNC_TEST=YES 59 PP12V_INV FUNC_TEST=YES 59 GND_17_INV FUNC_TEST=YES 59 PP5V_AGP_RL FUNC_TEST=YES 59 INV_17_LCD_PWM_F FUNC_TEST=YES 59 LAMP_STS_F FUNC_TEST=YES 59 INV_17_CUR_HI_F FUNC_TEST=YES 33 8 CPU_VID_R<5..0> FUNC_TEST=TRUE 36 KPVDD2_FMAX FUNC_TEST=YES 36 KPGND2_FMAX FUNC_TEST=YES 36 TDIODE_POS_FMAX FUNC_TEST=YES 36 TDIODE_NEG_FMAX FUNC_TEST=YES 36 CORE_ISNS_M FUNC_TEST=YES 36 33 CORE_ISNS_P FUNC_TEST=YES </pre>	<pre> 11 7 PP12V_RUN 10 TEST POINTS FUNC_TEST=YES 11 7 PP5V_ALL 5 TEST POINTS FUNC_TEST=YES 18 11 PP5V_RUN 5 TEST POINTS FUNC_TEST=YES 18 11 PP3V3_RUN 5 TEST POINTS FUNC_TEST=YES 18 11 PP24V_RUN 5 TEST POINTS FUNC_TEST=YES 83 7 =PP5V_DISK 5 TEST POINTS FUNC_TEST=YES 83 7 =PP12V_DISK 5 TEST POINTS FUNC_TEST=YES 12 GND 12 TEST POINTS FUNC_TEST=YES PP12V_RUN PP5V_RUN PP24V_RUN PP5V_ALL PP3V3_RUN PP2V5_RUN PP5V_PWRON PP1V2_PWRON PP1V5_RUN PP3V3_PWRON 18 11 PP2V5_RUN FUNC_TEST=YES 18 11 PP1V5_RUN FUNC_TEST=YES 18 11 PP5V_PWRON FUNC_TEST=YES 27 18 11 PP3V3_PWRON FUNC_TEST=YES 18 11 PP1V2_PWRON FUNC_TEST=YES 10 PPVCORE_PWRON_SB FUNC_TEST=YES 13 8 =PP3V3_ALL_SMU FUNC_TEST=TRUE 31 8 7 =PP5V_RUN_CPU FUNC_TEST=YES 22 PPVCORE_NB FUNC_TEST=YES 35 34 33 PPVCORE_CPU FUNC_TEST=YES 33 PP12V_CPU FUNC_TEST=YES 33 VCORE_SENSE_GND FUNC_TEST=YES 33 VCORE_SENSE_VOUT FUNC_TEST=YES 8 7 SMU_MANUAL_RESET_L 2 TEST POINTS FUNC_TEST=YES 13 7 SYS_POWER_BUTTON_L 2 TEST POINTS FUNC_TEST=YES 7 POWER_BUTTON_L FUNC_TEST=YES 7 RESET_BUTTON_L FUNC_TEST=YES 13 SMU_RESET_L FUNC_TEST=YES 33 13 7 SYS_POWERUP_L FUNC_TEST=YES 33 13 10 9 4 SYS_SLEEP FUNC_TEST=YES 13 8 SYS_POWERFAIL_L FUNC_TEST=YES 13 8 EXT_POWER_BUTTON_L FUNC_TEST=TRUE 9 U900_FEEDBACK FUNC_TEST=YES 22 U2200_FEEDBACK FUNC_TEST=YES 59 57 ANALOG_RED FUNC_TEST=YES 59 57 ANALOG_GRN FUNC_TEST=YES 59 57 ANALOG_BLU FUNC_TEST=YES 101 7 AUDIO_LI_DETECT_L FUNC_TEST=TRUE 77 AUDIO_IO_DET_L FUNC_TEST=YES 77 ROM_WP_L FUNC_TEST=YES 83 80 UATA_DD<15..0> FUNC_TEST=TRUE 83 80 UATA_DA<2..0> FUNC_TEST=TRUE 83 80 UATA_CS0_L FUNC_TEST=YES 83 80 UATA_CS1_L FUNC_TEST=YES 83 80 UATA_RESET_L FUNC_TEST=YES 83 80 UATA_DSTROBE_R FUNC_TEST=YES 83 80 UATA_HSTROBE FUNC_TEST=YES 83 80 UATA_STOP FUNC_TEST=YES 83 80 UATA_DMARQ_R FUNC_TEST=YES 83 80 UATA_DMACQ_L FUNC_TEST=YES 83 80 UATA_INTRO_R FUNC_TEST=YES 83 80 UATA_IOCS16_PU FUNC_TEST=YES 83 80 UATA_CSEL_PD FUNC_TEST=YES 34 33 TDIODE_NEG FUNC_TEST=YES 74 TP_AIRPORT_PME_L FUNC_TEST=YES 74 TP_AIRPORT_RF_DISABLE FUNC_TEST=YES </pre>	D				
C	<pre> 1453 NO_TEST=YES TP_TMDS_TXD3M 58 1454 NO_TEST=YES TP_TMDS_TXD3P 58 1455 NO_TEST=YES TP_TMDS_TXD7M 58 1456 NO_TEST=YES TP_TMDS_TXD7P 58 1457 NO_TEST=YES TP_VIPCLK 57 1458 NO_TEST=YES TP_FRWLPS 57 1459 NO_TEST=YES TP_AGP_MB_AGP8X_DET_L 48 1460 NO_TEST=YES TP_ATTENTION 29 1461 NO_TEST=YES TP_ENET_CLK125M_GTX 87 1462 NO_TEST=YES TP_ENET_TXD<7> 87 1463 NO_TEST=YES TP_ENET_TXD<4> 87 1464 NO_TEST=YES TP_ENET_TXD<5> 87 1465 NO_TEST=YES TP_FN_CLK98M_LCLK 90 1466 NO_TEST=YES TP_AFN 29 1467 NO_TEST=YES TP_PSR01 29 1468 NO_TEST=YES TP_PSR02 29 1469 NO_TEST=YES TP_PSYNCOOT 29 1470 NO_TEST=YES TP_USB2_PWREN<2> 92 1471 NO_TEST=YES TP_USB2_PWREN<3> 92 1472 NO_TEST=YES TP_USB2_PWREN<4> 92 1473 NO_TEST=YES TP_NEC_AMC 77 1474 NO_TEST=YES TP_NEC_NANDTEST 77 1475 NO_TEST=YES TP_NEC_NTST1 77 1476 NO_TEST=YES TP_NEC_SMC 77 1477 NO_TEST=YES TP_NEC_SMI_L 77 1478 NO_TEST=YES TP_NEC_SRCCLK 77 1479 NO_TEST=YES TP_NEC_SRDATA 77 1480 NO_TEST=YES TP_NEC_SRMOD 77 1481 NO_TEST=YES TP_NEC_TEB 77 1482 NO_TEST=YES TP_NEC_TEST 77 1483 NO_TEST=YES TP_PLS_CLK_66M_0 27 1484 NO_TEST=YES TP_PLS_CLK_66M_1 27 1485 NO_TEST=YES TP_PLS_REF_CML 27 1486 NO_TEST=YES TP_PLS_TEST1 27 1487 NO_TEST=YES TP_PLS_TEST2 27 1488 NO_TEST=YES TP_PLS_TEST3 27 1489 NO_TEST=YES TP_SB_FSTEST 25 1490 NO_TEST=YES TP_SB_PLTEST 25 1491 NO_TEST=YES TP_VREF_CG 48 1492 NO_TEST=YES TP_SB_NC_P7 91 1493 NO_TEST=YES TP_SB_NC_P8 91 1494 NO_TEST=YES TP_SB_NC_R3 91 1495 NO_TEST=YES TP_SB_NC_R4 91 1496 NO_TEST=YES TP_SB_NC_R5 91 1497 NO_TEST=YES TP_SB_NC_R6 91 1498 NO_TEST=YES TP_SB_NC_R7 91 1499 NO_TEST=YES TP_SB_NC_R8 91 1500 NO_TEST=YES TP_SB_NC_T1 91 1501 NO_TEST=YES TP_SB_NC_T2 91 1502 NO_TEST=YES TP_SB_NC_T3 91 1503 NO_TEST=YES TP_SB_NC_T4 91 1504 NO_TEST=YES TP_SB_NC_T5 91 1505 NO_TEST=YES TP_SB_NC_T6 91 1506 NO_TEST=YES TP_SB_NC_T7 91 1507 NO_TEST=YES TP_SB_NC_T8 91 1508 NO_TEST=YES TP_SB_NC_U1 91 1509 NO_TEST=YES TP_SB_NC_U2 91 1510 NO_TEST=YES TP_SB_NC_U3 91 1511 NO_TEST=YES TP_SB_NC_U4 91 1512 NO_TEST=YES TP_SB_NC_U5 91 1513 NO_TEST=YES TP_SB_NC_U6 91 1514 NO_TEST=YES TP_SB_NC_V1 91 1515 NO_TEST=YES TP_SB_NC_V2 91 1516 NO_TEST=YES TP_SB_NC_V3 91 1517 NO_TEST=YES TP_SB_NC_V4 91 1518 NO_TEST=YES TP_SB_NC_W1 91 1519 NO_TEST=YES TP_SB_NC_W3 91 1520 NO_TEST=YES TP_SB_NC_Y1 91 1521 NO_TEST=YES TP_SB_NC_Y3 91 1522 NO_TEST=YES TP_SATA_CLK25M 27 1523 NO_TEST=YES TP_ENET_TCK 87 1524 NO_TEST=YES TP_USB2_PWREN<0> 92 1525 NO_TEST=YES TP_USB2_PWREN<1> 92 1526 NO_TEST=YES TP_DUMMY_A 24 1527 NO_TEST=YES TP_DUMMY_B 24 1528 NO_TEST=YES TP_RAM_CKE_R<2> 8 </pre>	<pre> GENZ SHOULD USE J1400 FOR THE FOLLOWING NETS: 1428 29 EI_CPU_TO_NB_AD<0..43> 1428 29 EI_CPU_TO_NB_CLK_N 1428 29 EI_CPU_TO_NB_CLK_P 1428 29 EI_CPU_TO_NB_SR_N<0..1> 1428 29 EI_CPU_TO_NB_SR_P<0..1> 1428 29 EI_NB_TO_CPU_AD<0..43> 1428 29 EI_NB_TO_CPU_CLK_N 1428 29 EI_NB_TO_CPU_CLK_P 1428 29 EI_NB_TO_CPU_SR_N<0..1> 1428 29 EI_NB_TO_CPU_SR_P<0..1> 8 14 29 CHKSTOP_L 14 29 30 CPU_HRESET_L 14 29 30 CPU_INT_L 14 29 30 CPU1_HTBEN 14 27 EI_CPU1_CLK_N 14 27 EI_CPU1_CLK_P 14 28 29 EI_QACK_L 14 28 29 30 EI_QREQ_L 14 28 29 30 EI_SE 13 14 18 I2C_SMU_A_SCL_OUT_L 13 14 18 I2C_SMU_A_SDA_OUT_L 14 29 MCP_L 14 29 30 RI_L 14 29 30 SYNCENABLE 14 29 TP_PROC_TRIGGER_OUT 14 27 EI_CPU1_SYNC </pre>	<pre> 92 USB BT N FUNC_TEST=YES 92 USB BT P FUNC_TEST=YES 92 USB2_PORT1_N_F FUNC_TEST=YES 92 USB2_PORT1_P_F FUNC_TEST=YES 92 USB2_PORT2_N_F FUNC_TEST=YES 92 USB2_PORT2_P_F FUNC_TEST=YES 92 USB2_PORT3_N_F FUNC_TEST=YES 92 USB2_PORT3_P_F FUNC_TEST=YES 92 PP5V_USB2_PORT1_F FUNC_TEST=YES 92 PP5V_USB2_PORT2_F FUNC_TEST=YES 92 PP5V_USB2_PORT3_F FUNC_TEST=YES 94 76 25 I2S1_DEV_TO_SB_DTI 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_SYNC 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_BITCLK 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_MCLK 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_SB_TO_DEV_DTO 2 TEST POINTS FUNC_TEST=YES 94 25 I2S1_RESET_L 2 TEST POINTS FUNC_TEST=YES 94 25 MODEM_RING2SYS_L 2 TEST POINTS FUNC_TEST=YES 94 18 I2C_UDASH_SDA FUNC_TEST=YES 94 18 I2C_UDASH_SCL FUNC_TEST=YES 94 USB_UDASH_N FUNC_TEST=YES 94 USB_UDASH_P FUNC_TEST=YES 94 UDASH_SDOWN FUNC_TEST=YES 94 UDASH_RESET_L FUNC_TEST=YES 94 UDASH_I2C_AI_PU FUNC_TEST=YES 59 PPVCC_TMDS FUNC_TEST=YES 59 PP3V3_DDC FUNC_TEST=YES 59 TD0M FUNC_TEST=YES 59 TD0P FUNC_TEST=YES 59 TD1M FUNC_TEST=YES 59 TD1P FUNC_TEST=YES 59 TD2M FUNC_TEST=YES 59 TD2P FUNC_TEST=YES 59 TCKM FUNC_TEST=YES 59 TCKP FUNC_TEST=YES 59 TMDS_DDC_DAT FUNC_TEST=YES 59 TMDS_DDC_CLK FUNC_TEST=YES 59 7 GND_CHASSIS_TMDS FUNC_TEST=YES 59 FILT_ANALOG_RED FUNC_TEST=YES 59 FILT_ANALOG_GRN FUNC_TEST=YES 59 FILT_ANALOG_BLU FUNC_TEST=YES 59 56 ANALOG_HSYNC_L FUNC_TEST=YES 59 56 ANALOG_VSYNC_L FUNC_TEST=YES 59 VGA_IIC_CLK FUNC_TEST=YES 59 VGA_IIC_DAT FUNC_TEST=YES 59 58 MON_DETECT FUNC_TEST=YES 59 DDC_VCC_5 FUNC_TEST=YES 59 PP24V_INV FUNC_TEST=YES 59 GND_20_INV FUNC_TEST=YES 59 INV_20_LCD_PWM FUNC_TEST=YES 59 INV_20_CUR_HI_F FUNC_TEST=YES 59 PP12V_INV FUNC_TEST=YES 59 GND_17_INV FUNC_TEST=YES 59 PP5V_AGP_RL FUNC_TEST=YES 59 INV_17_LCD_PWM_F FUNC_TEST=YES 59 LAMP_STS_F FUNC_TEST=YES 59 INV_17_CUR_HI_F FUNC_TEST=YES 33 8 CPU_VID_R<5..0> FUNC_TEST=TRUE 36 KPVDD2_FMAX FUNC_TEST=YES 36 KPGND2_FMAX FUNC_TEST=YES 36 TDIODE_POS_FMAX FUNC_TEST=YES 36 TDIODE_NEG_FMAX FUNC_TEST=YES 36 CORE_ISNS_M FUNC_TEST=YES 36 33 CORE_ISNS_P FUNC_TEST=YES </pre>	C					
B									B
A									A

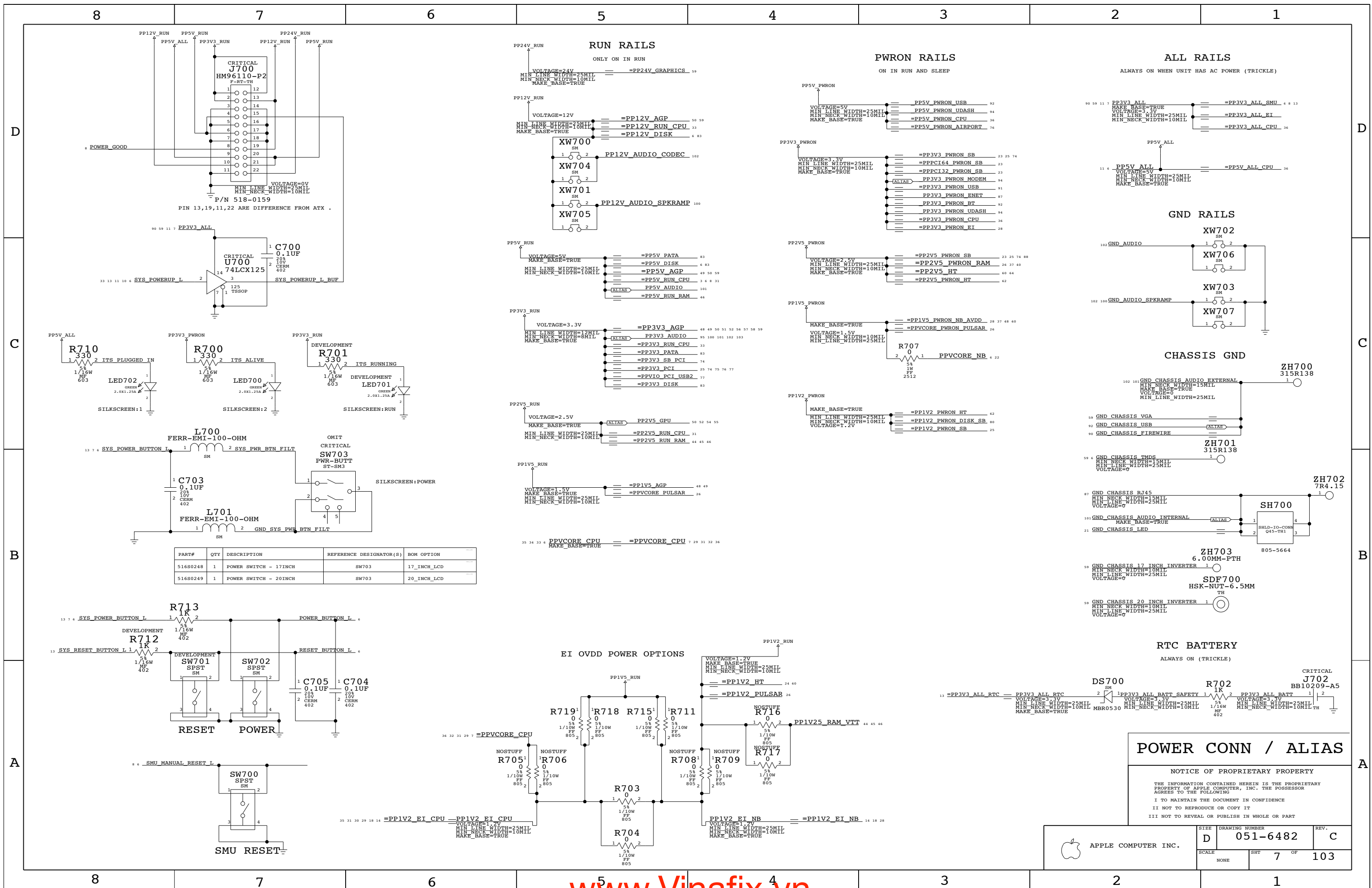
FUNC TEST

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	NONE	D 051-6482	C
	SHT	6	OF 103



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
51680248	1	POWER SWITCH - 17INCH	SW703	17_INCH_LCD
51680249	1	POWER SWITCH - 20INCH	SW703	20_INCH_LCD

POWER CONN / ALIAS

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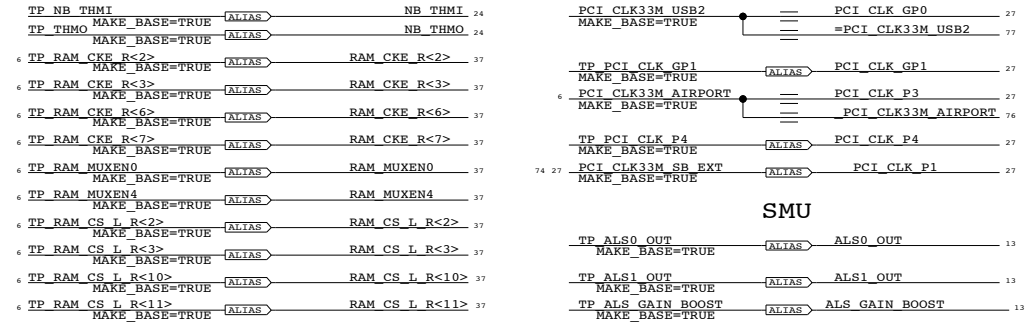
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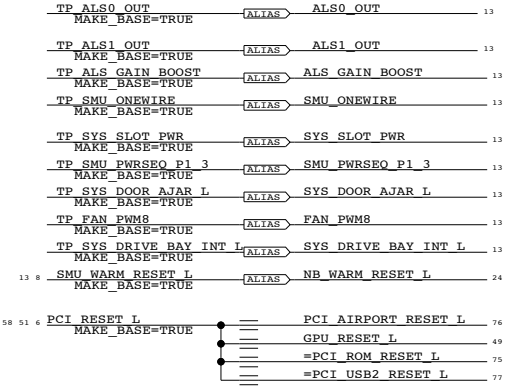
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHEET 7 OF 103	

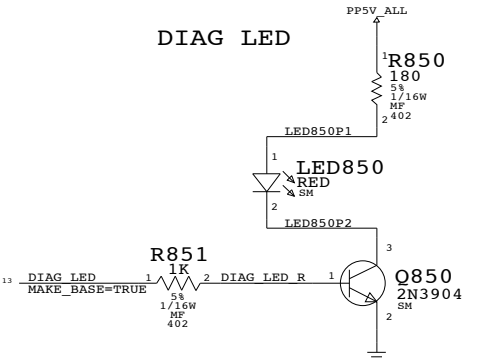
PCI CLOCKS



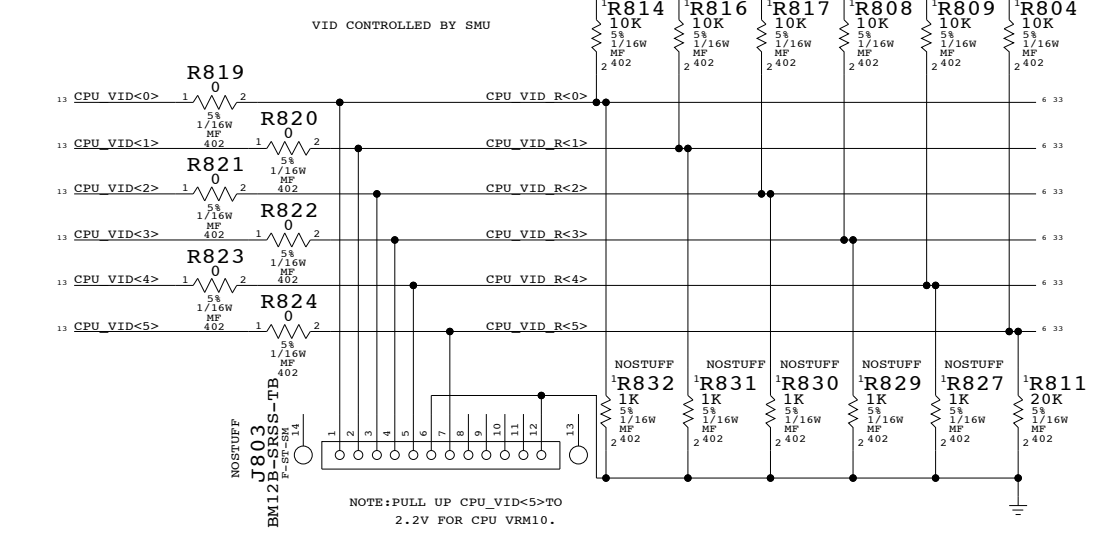
SMU



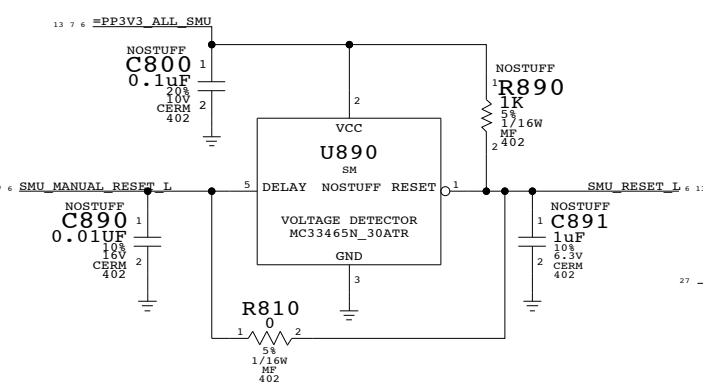
DIAG LED



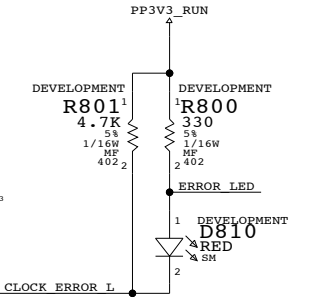
CPU VID<0:5>



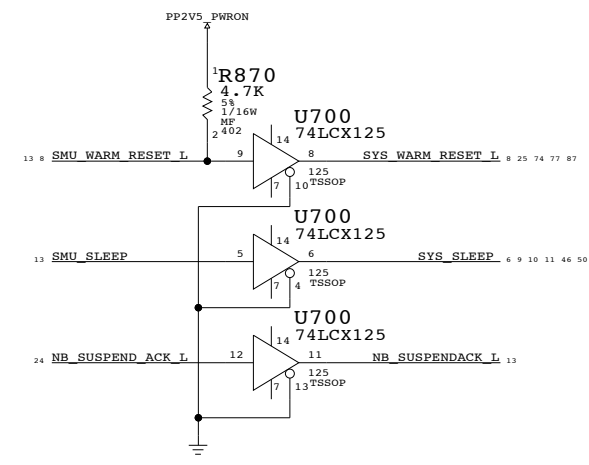
BACKUP SMU RESET CIRCUIT



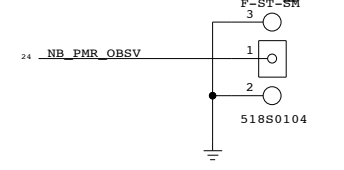
PULSAR ERROR_L LED



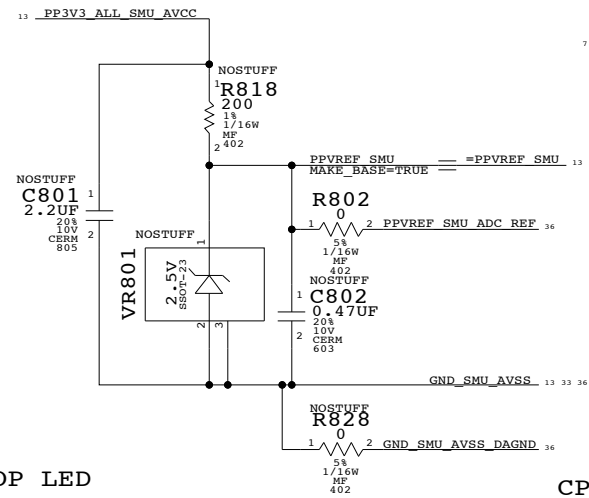
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
R840	SMU_RESET	10 MIL SPACING
R841	SMU_RESET	10 MIL SPACING



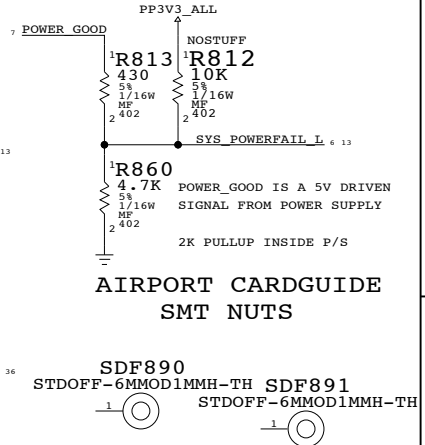
DEVELOPMENT J800



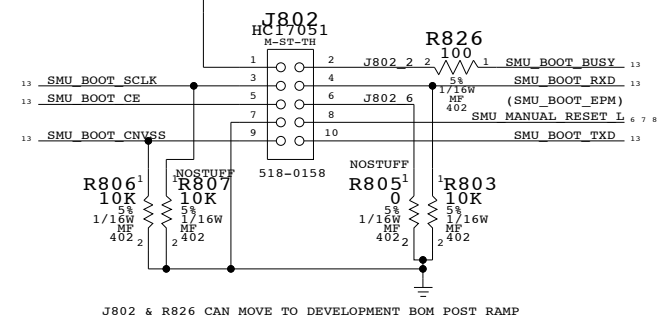
SMU ANALOG VREF



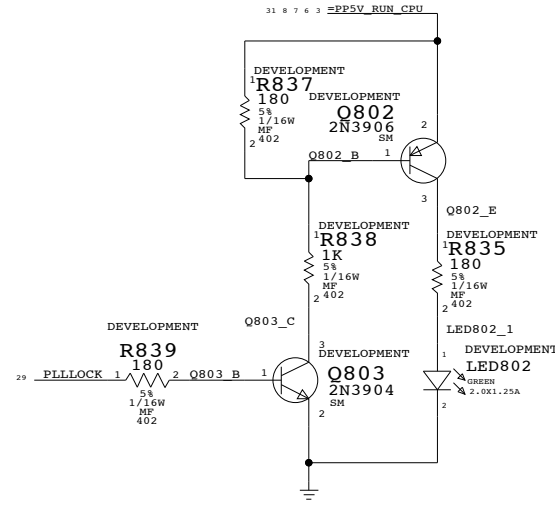
POWER FAIL_L CONNECTION



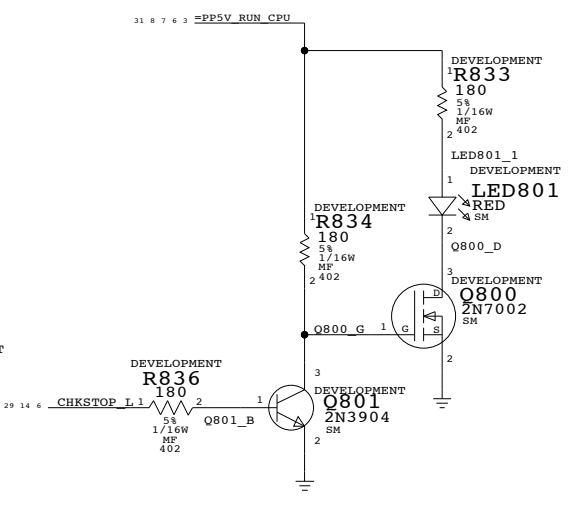
DOWNLOAD CONNECTOR



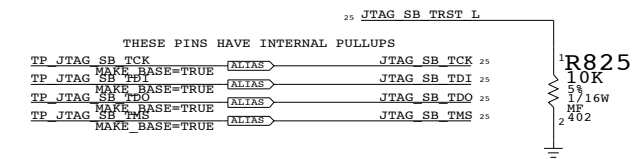
PLL LOCK LED



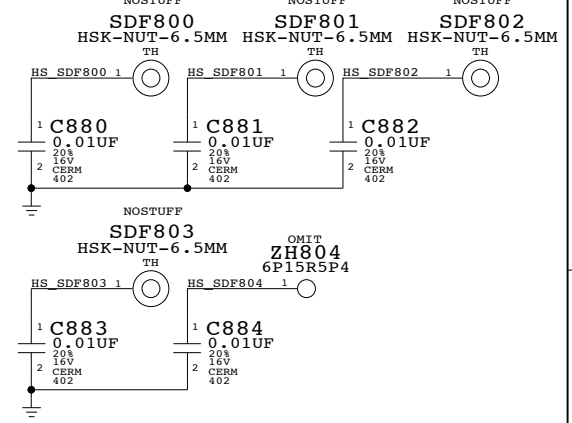
CHKSTOP LED



SHASTA JTAG PULL DOWN



CPU HEATSINK SMT NUTS

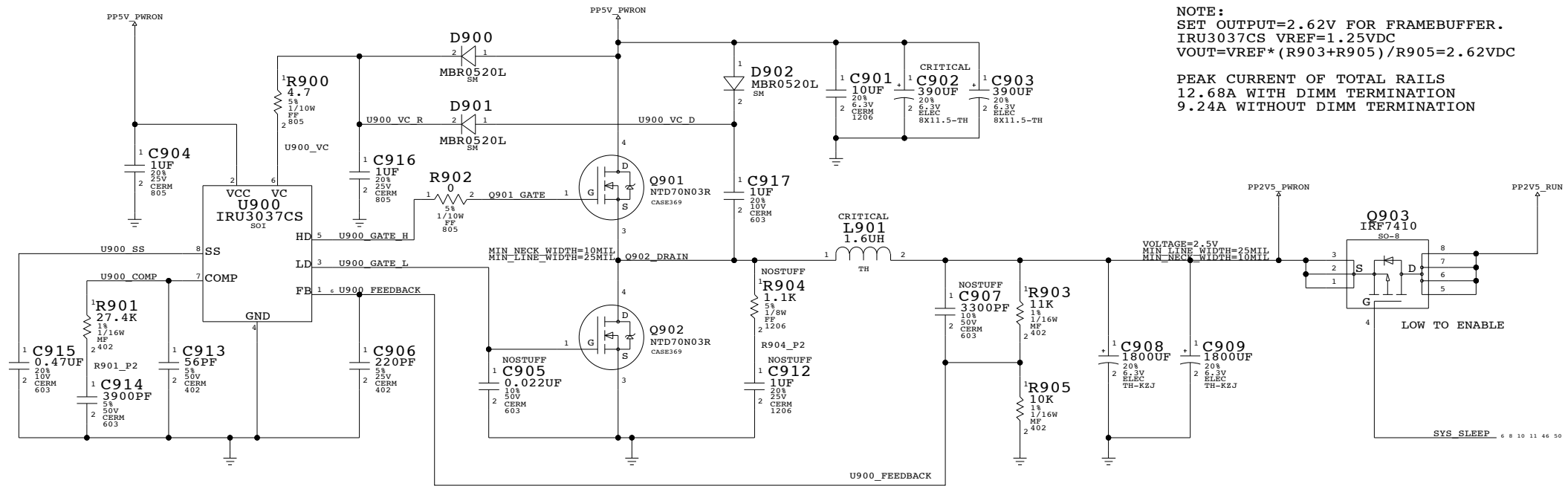


SIGNAL ALIAS

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	D	051-6482	C
SCALE	SHT	8 OF	103
NONE			

2.5V VOLTAGE REGULATOR



NOTE:
 SET OUTPUT=2.62V FOR FRAMEBUFFER.
 IRU3037CS VREF=1.25VDC
 $V_{OUT} = V_{REF} * (R_{903} + R_{905}) / R_{905} = 2.62VDC$

PEAK CURRENT OF TOTAL RAILS
 12.68A WITH DIMM TERMINATION
 9.24A WITHOUT DIMM TERMINATION

2.5V VREG

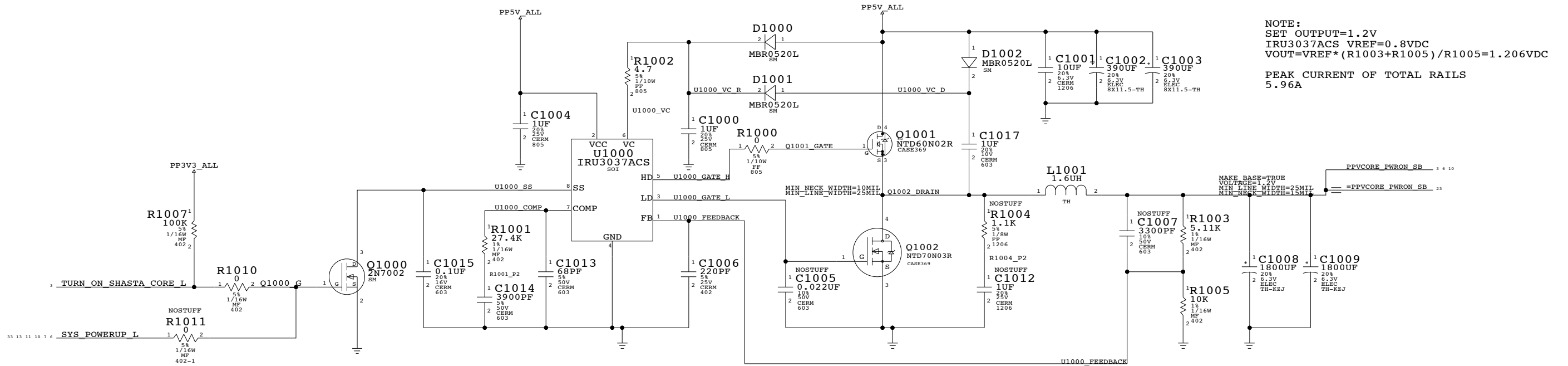
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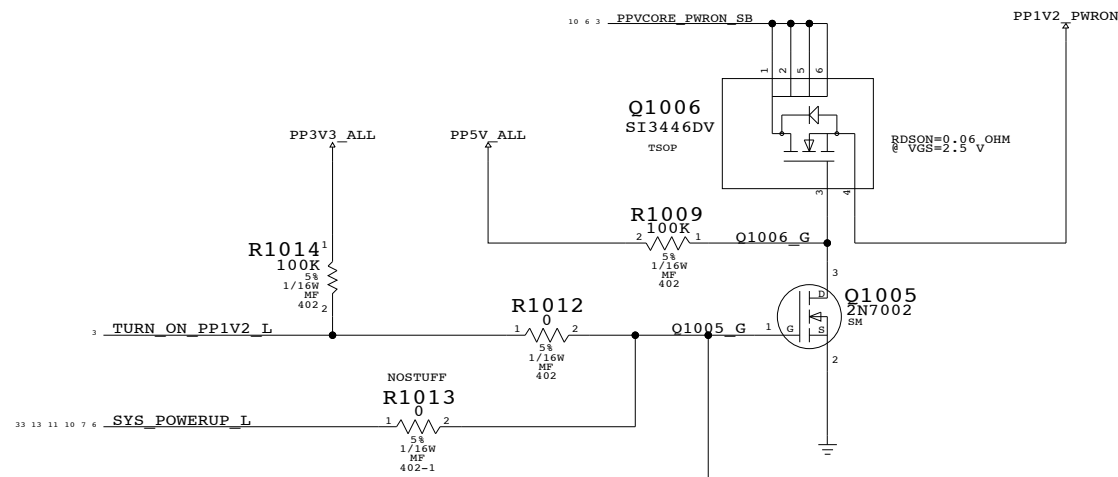
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHT 9	OF 103

SHASTA CORE VOLTAGE REGULATOR

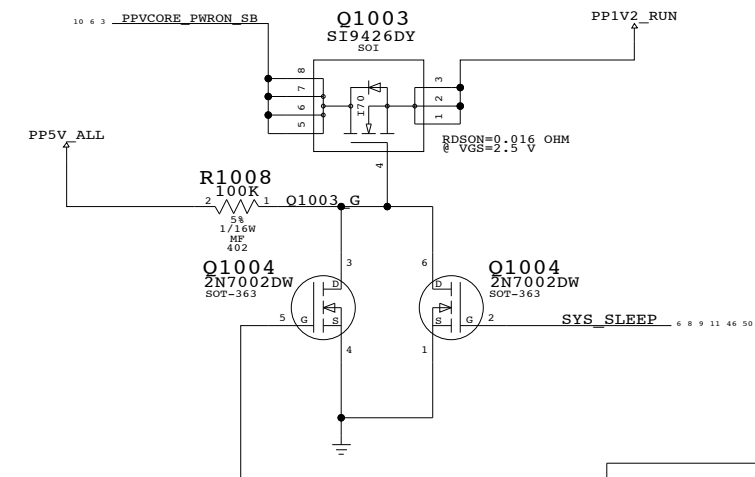


NOTE:
 SET OUTPUT=1.2V
 IRU3037ACS VREF=0.8VDC
 $V_{OUT} = V_{REF} * (R1003 + R1005) / R1005 = 1.206VDC$
 PEAK CURRENT OF TOTAL RAILS
 5.96A

PP1V2_PWRON FET SWITCH PEAK CURRENT 0.6A



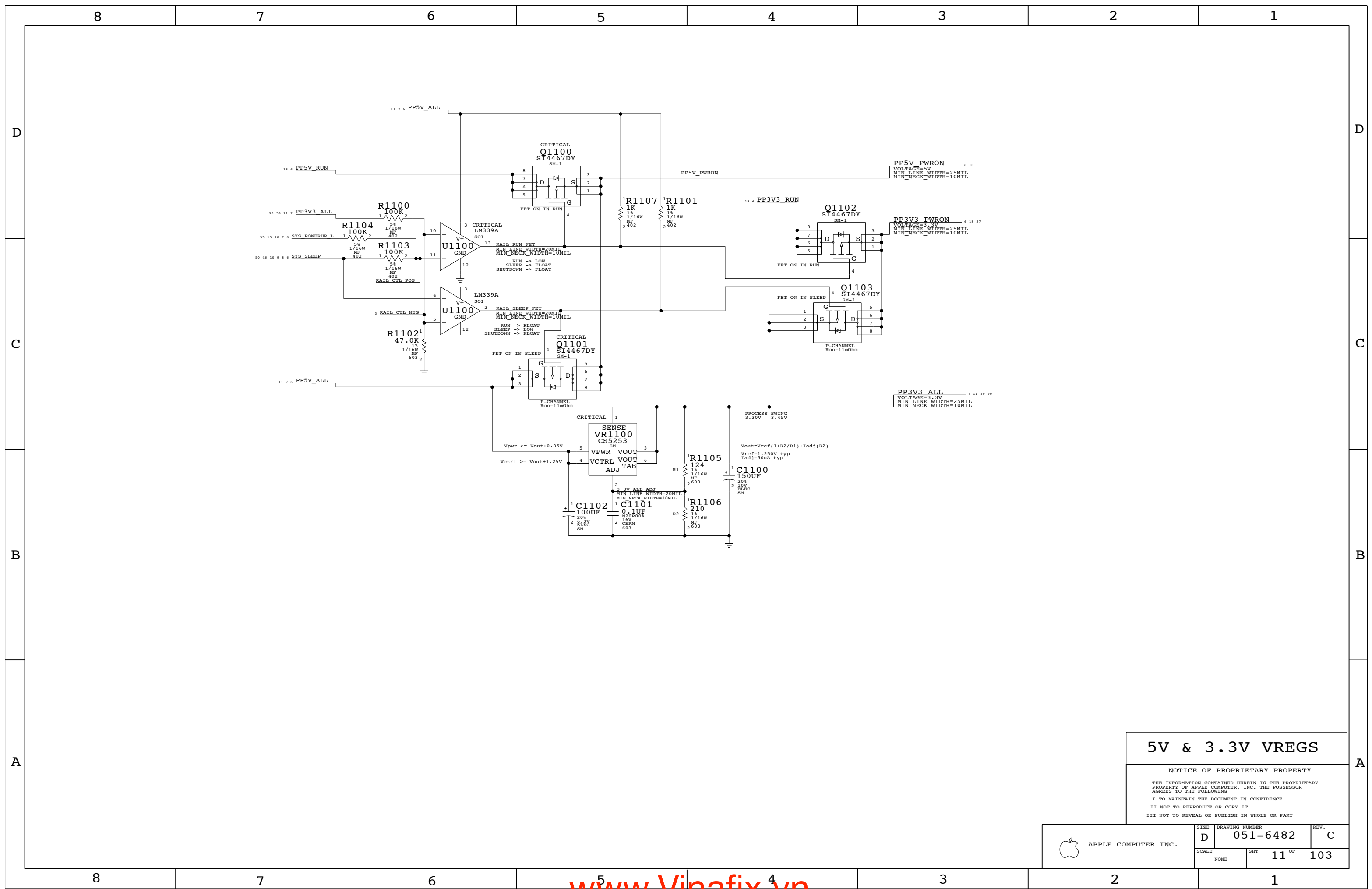
PP1V2_RUN FET SWITCH PEAK CURRENT 4.43A



1.2V VREG

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	D	051-6482	C
SCALE	SHT	10 OF	103
NONE			



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	15 MIL SPACING	SMU_CLK10M_XIN
	15 MIL SPACING	SMU_CLK10M_XOUT
	15 MIL SPACING	SMU_CLK10M_XOUT_R
RTC_CLK32K_XTAL	15 MIL SPACING	RTC_CLK32K_X1
	15 MIL SPACING	RTC_CLK32K_X2

Page Notes

Power aliases required by this page:
 - PP3V3_ALL_SMU
 - PP3V3_ALL_RTC
 - PP3V3_PWRON_SMU
 - PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

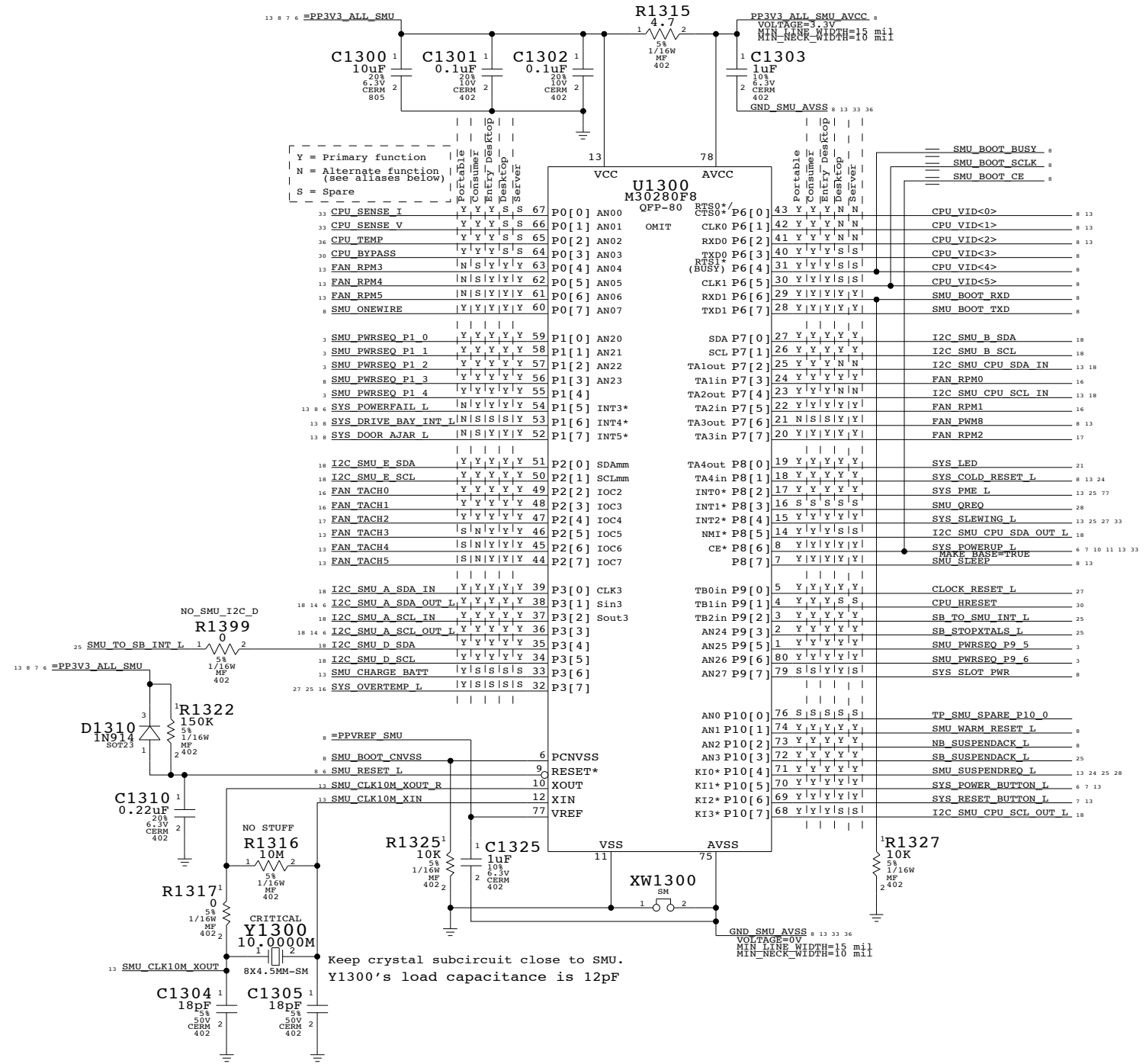
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND SMU AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND SMU AVSS). None of those capacitors are provided on this page.

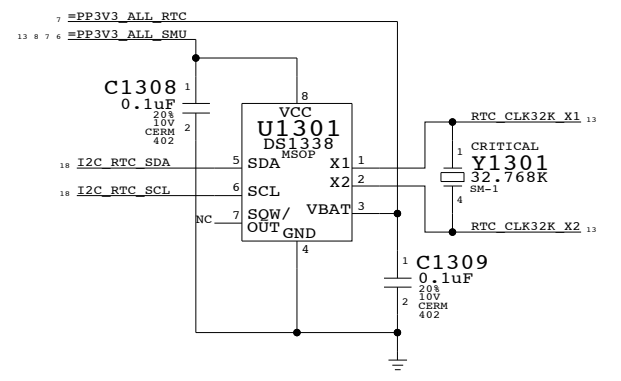
NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

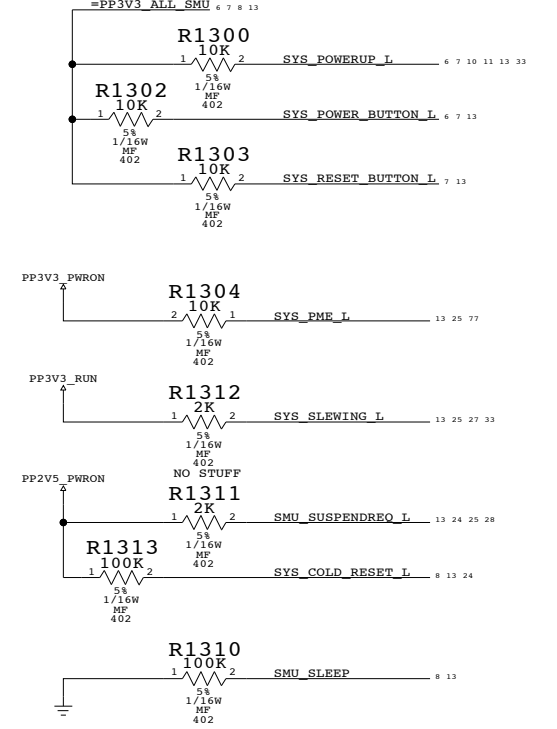
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



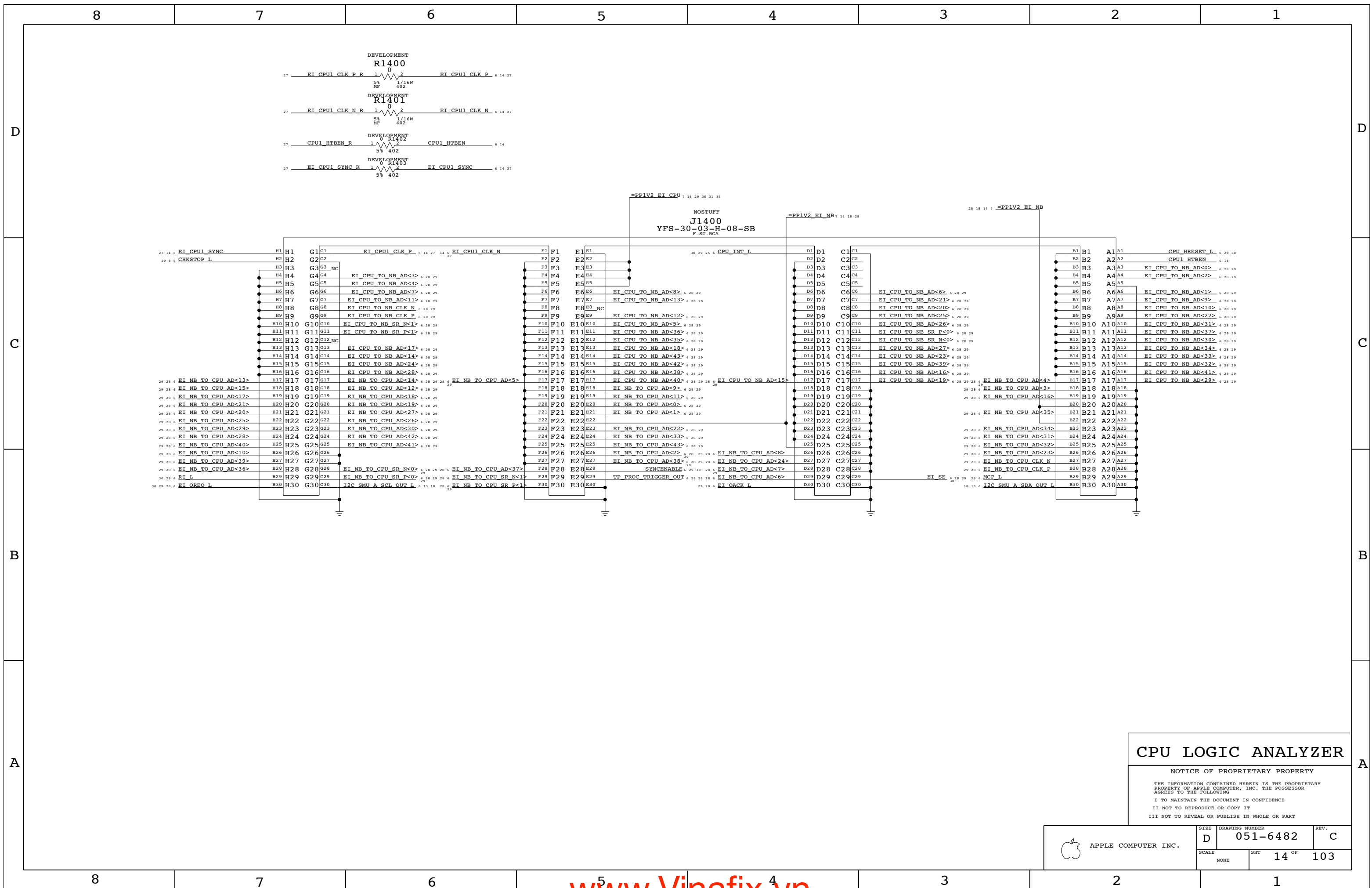
Alternate Functions

Portable			Consumer			Tower & Server		
Port			Port			Port		
13	FAN_RPM3	0.4	ALSO OUT	13	FAN_TACH3	2.5	SYS_LED_RED	21
13	FAN_RPM4	0.5	ALS1 OUT	13	FAN_TACH4	2.6	SYS_LED_GREEN	21
13	FAN_RPM5	0.6	ALS_GAIN_BOOST	13	FAN_TACH5	2.7	SYS_LED_BLUE	21
13	SYS_POWERFAIL_L	1.5	SMU_ACIN	13	SMU_CHARGE_BATT	3.6	DIAG_LED	8
13	SYS_DRIVE_BAY_INT_L	1.6	SMU_BATT_DET_L					
13	SYS_DOOR_AJAR_L	1.7	SYS_LID_OPEN					
13	FAN_PWM8	7.6	SYS_KBDLED					
13	CPU_VID<0>	6.0	FAN_TACH6					
13	CPU_VID<1>	6.1	FAN_TACH7					
13	CPU_VID<2>	6.2	FAN_TACH8					
10	I2C_SMU_CPU_SDA_IN	7.2	FAN_PWM6					
10	I2C_SMU_CPU_SCL_IN	7.4	FAN_PWM7					

System Management Unit

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		SHEET	13 OF 103

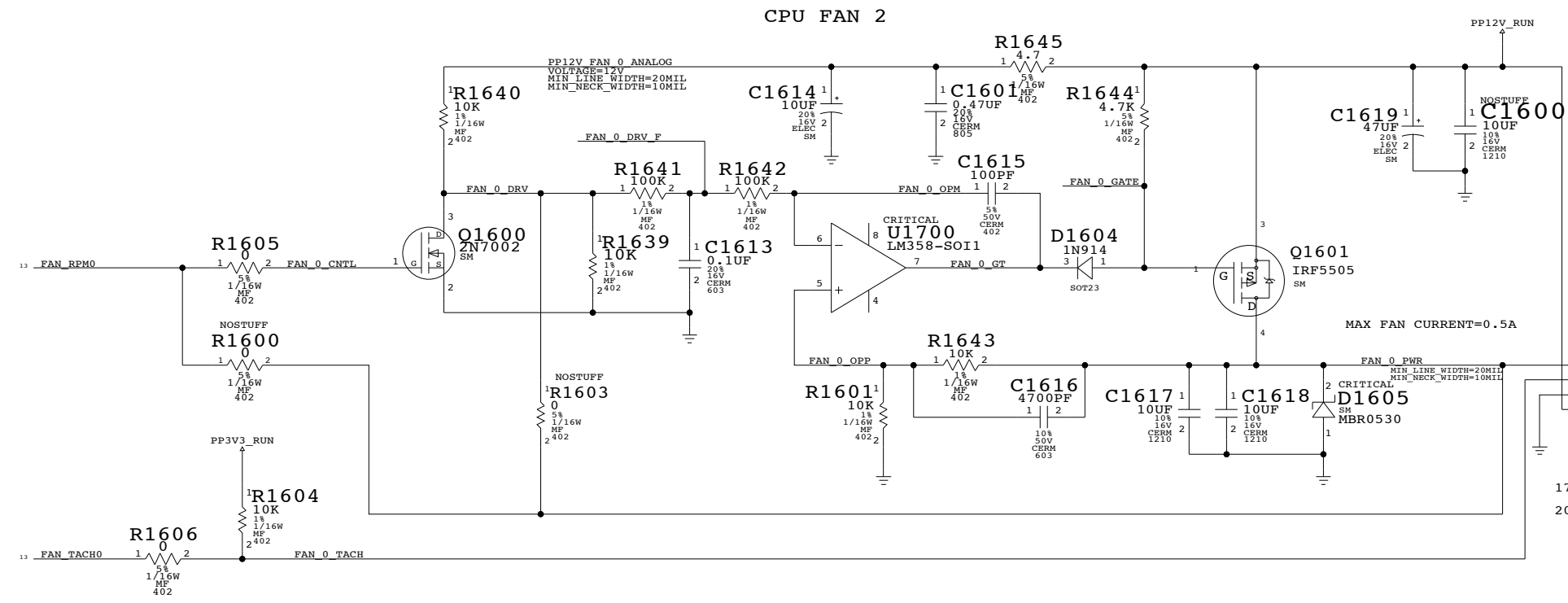


CPU LOGIC ANALYZER

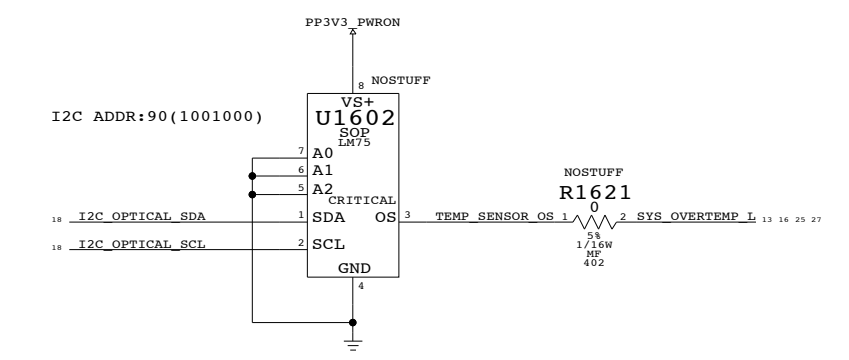
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	SCALE NONE	SHT 14 OF 103	

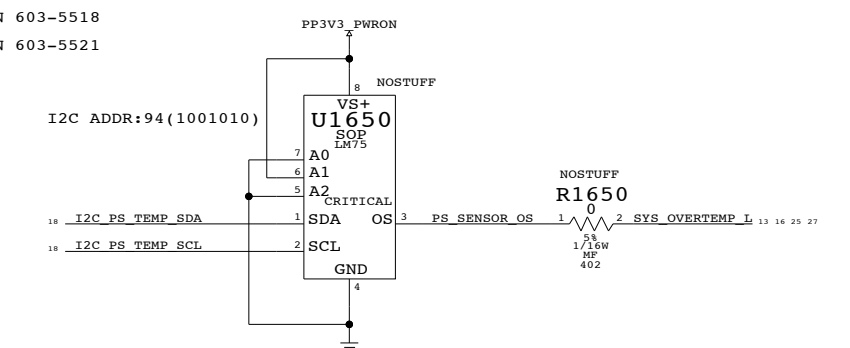
FAN 1 - Q37 STYLE CPU FAN CONTROL CIRCUIT



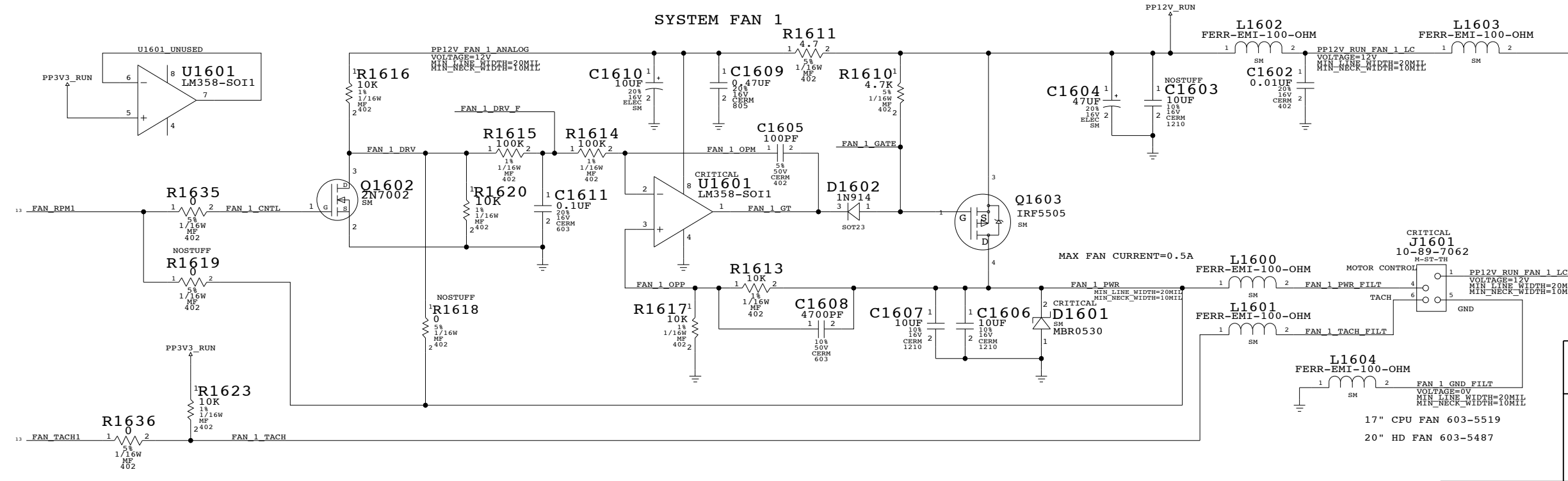
OPTICAL TEMP SENSOR



POWER SUPPLY TEMP SENSOR



FAN 2 - Q37 STYLE CPU FAN CONTROL CIRCUIT

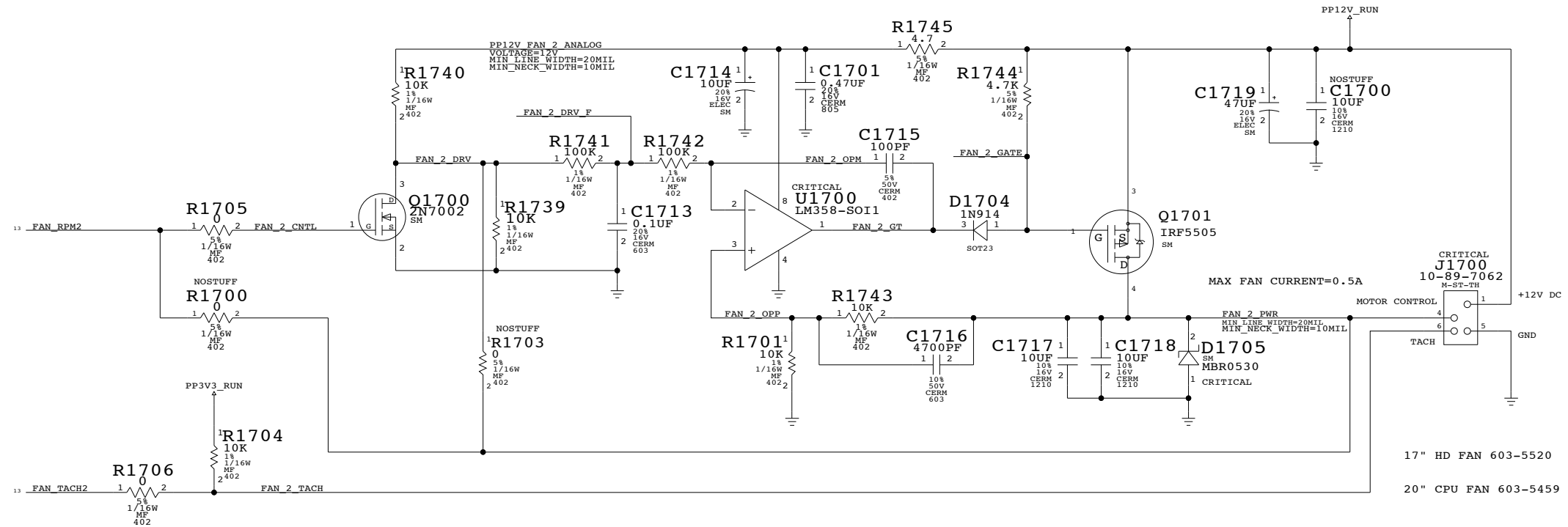


FAN 1, 2 & SYSTEM TEMP

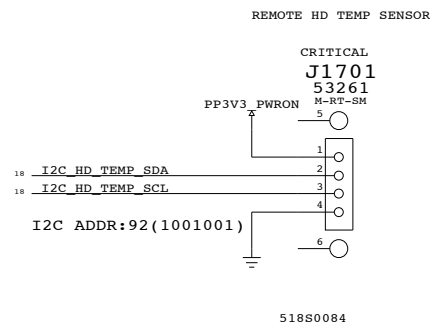
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SCALE	SHT	OF	REV.
NONE	16	103	

FAN 3 - Q37 STYLE SYSTEM FAN CONTROL CIRCUIT



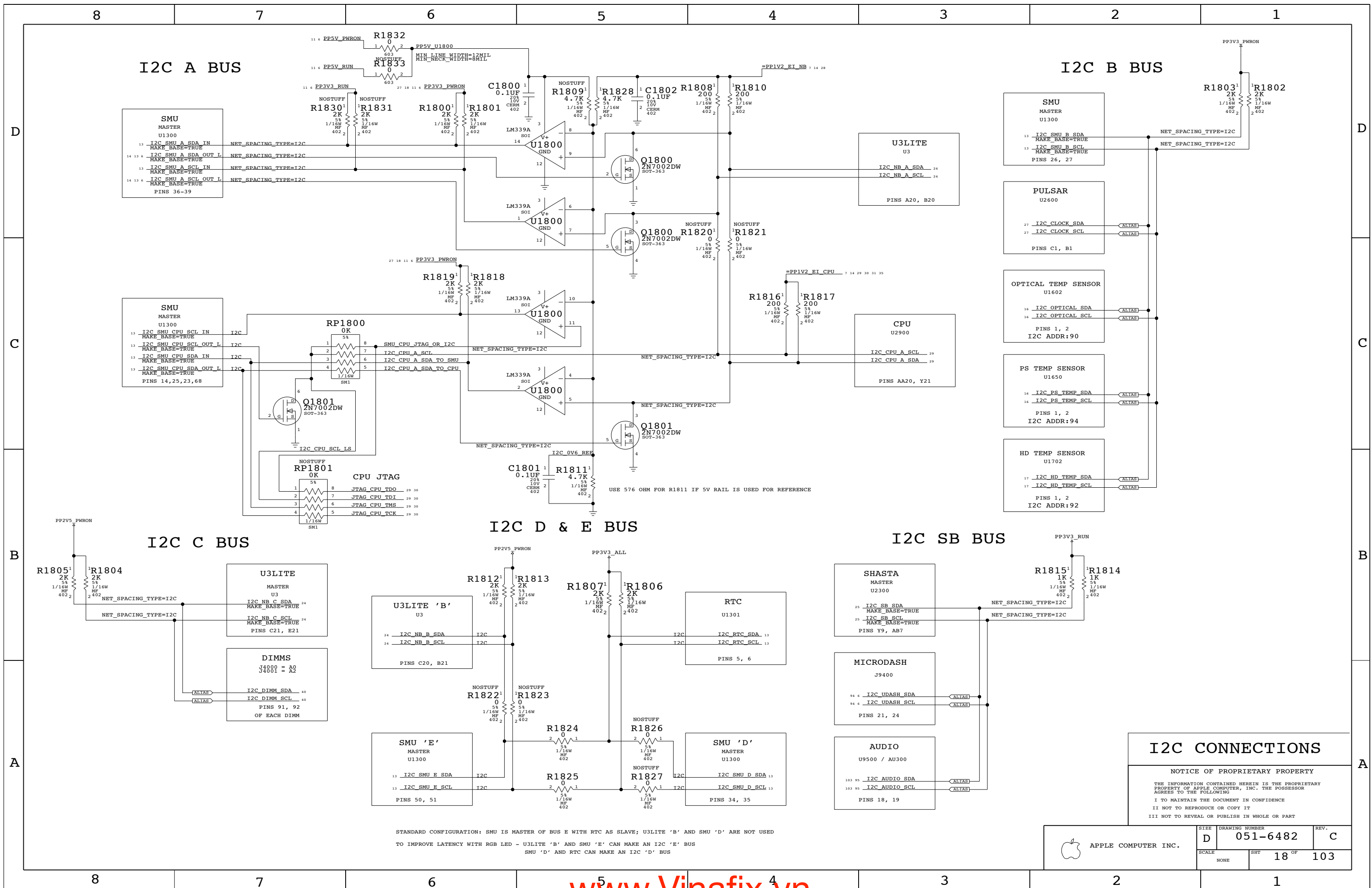
REMOTE HARD DRIVE TEMP SENSOR



FAN 3 & HD TEMP

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SCALE	SHT	17 OF	103
NONE			



I2C A BUS

I2C B BUS

I2C C BUS

I2C D & E BUS

I2C SB BUS

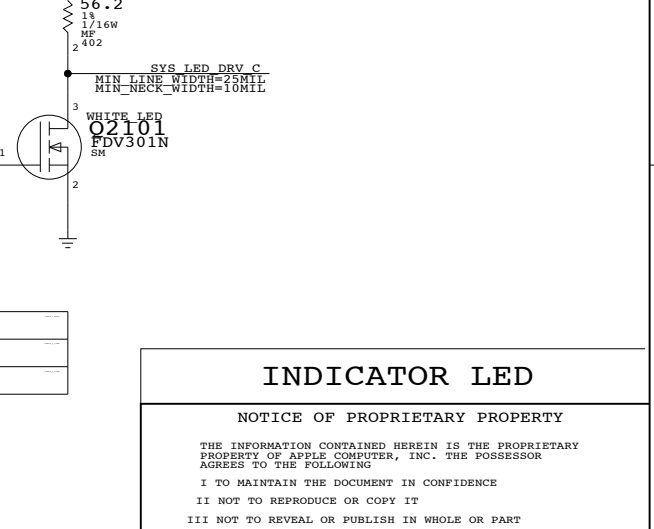
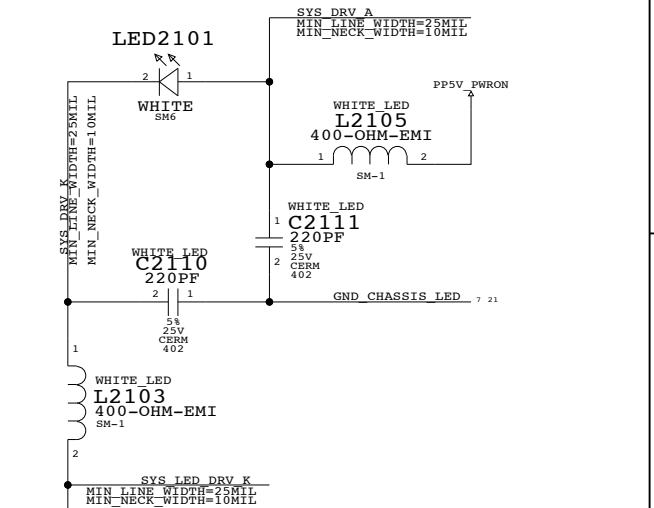
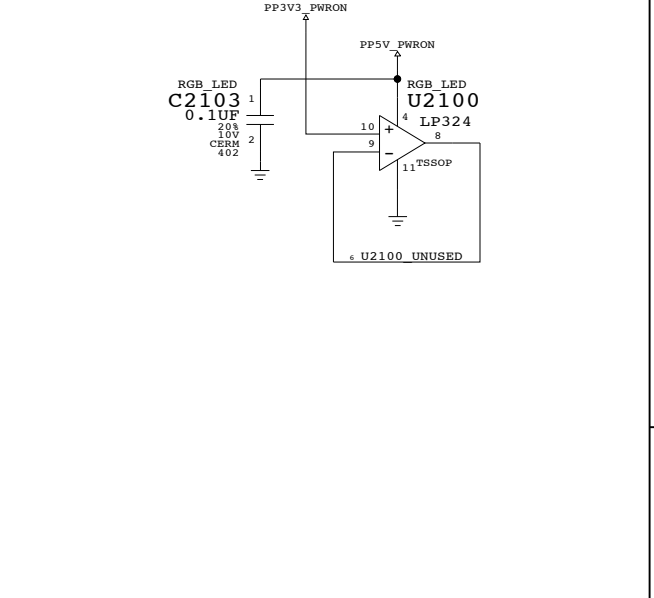
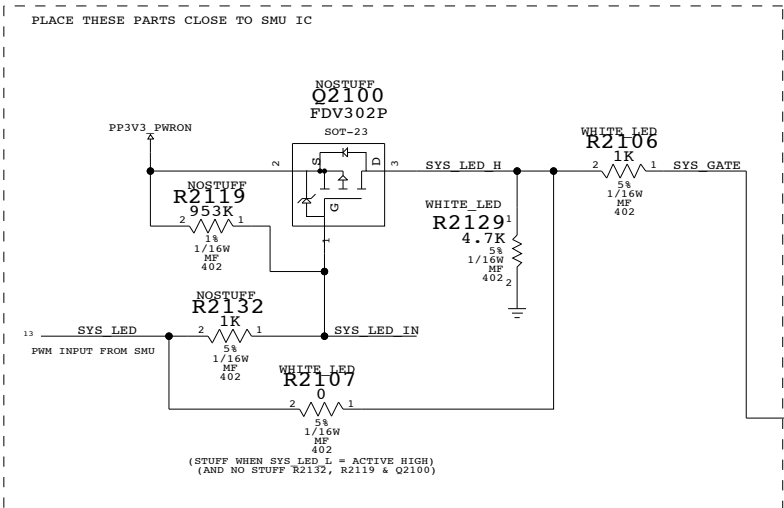
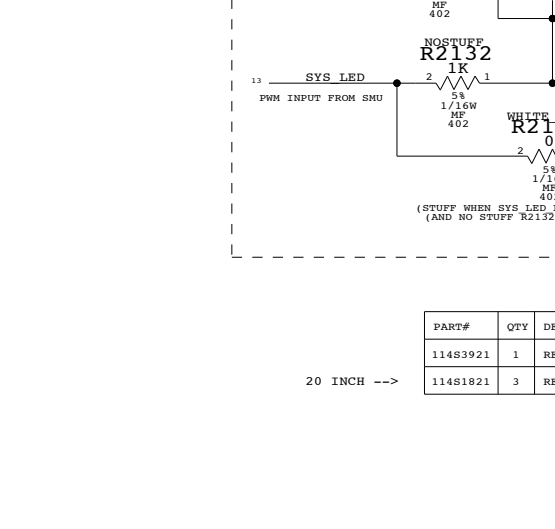
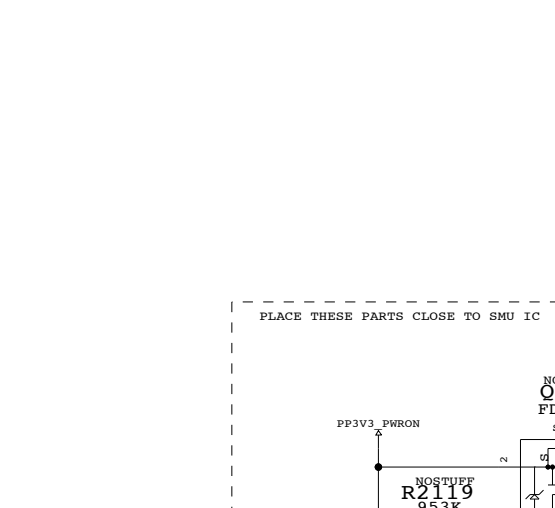
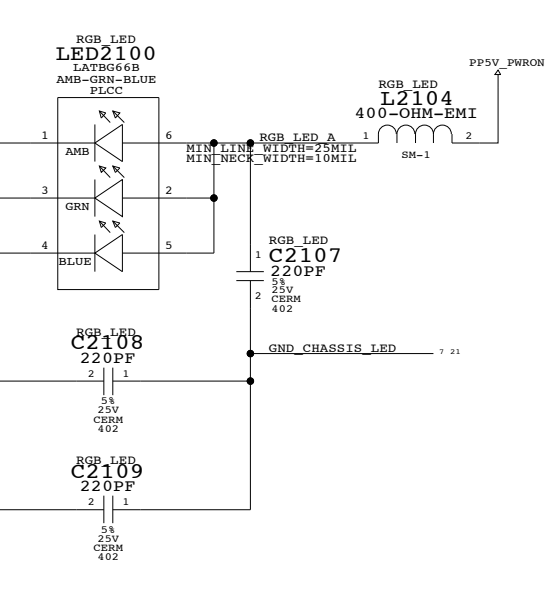
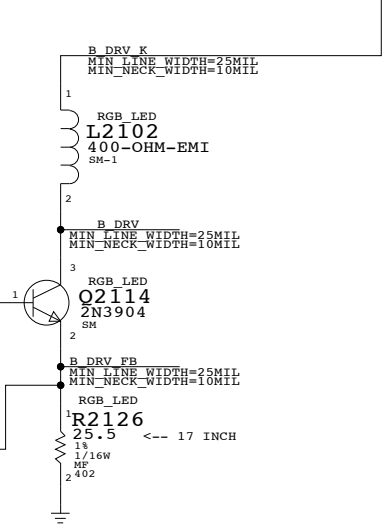
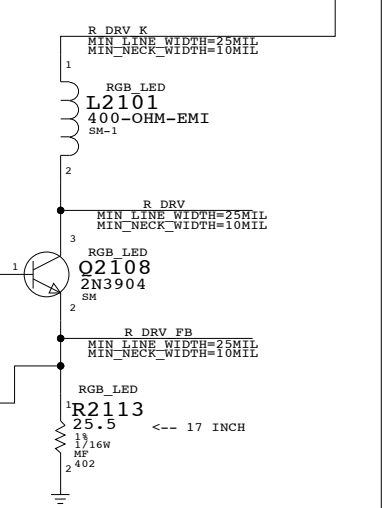
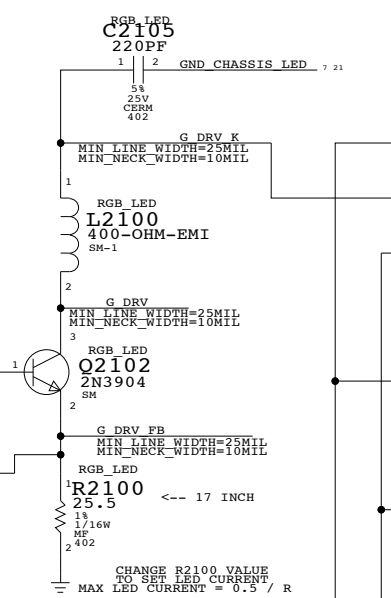
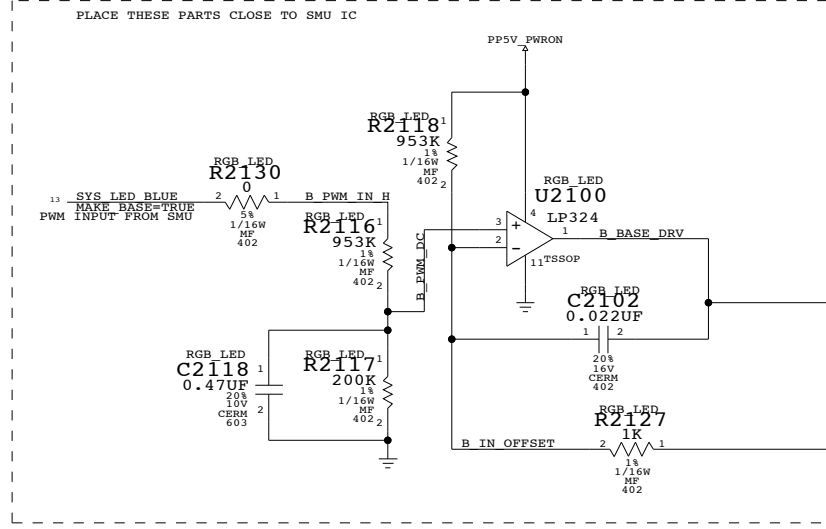
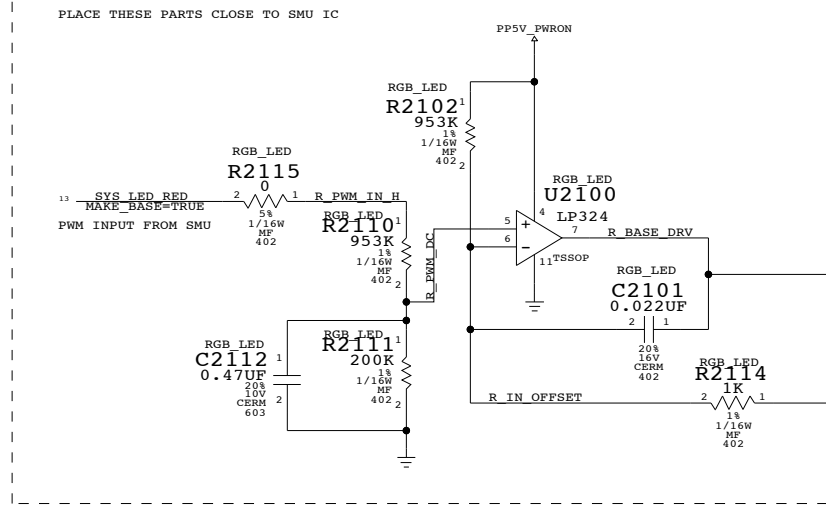
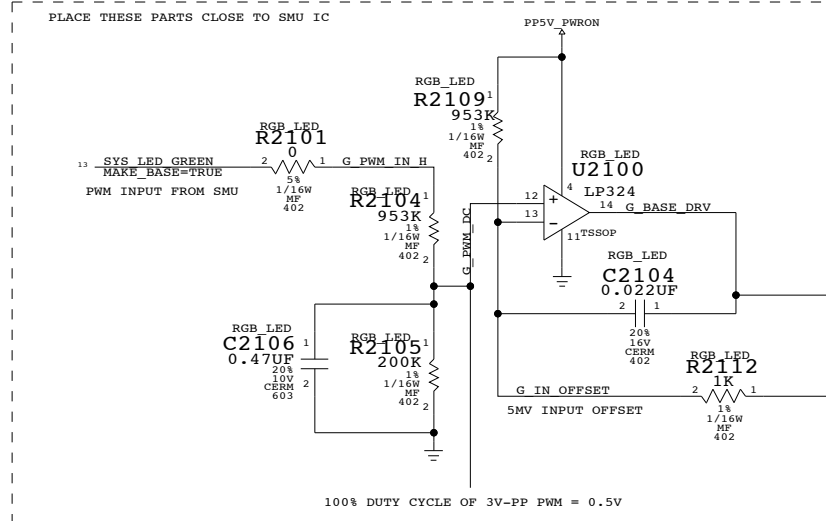
I2C CONNECTIONS

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STANDARD CONFIGURATION: SMU IS MASTER OF BUS E WITH RTC AS SLAVE; U3LITE 'B' AND SMU 'D' ARE NOT USED
 TO IMPROVE LATENCY WITH RGB LED - U3LITE 'B' AND SMU 'E' CAN MAKE AN I2C 'E' BUS
 SMU 'D' AND RTC CAN MAKE AN I2C 'D' BUS

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	18 OF 103	
NONE			

TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
11481821	3	RES, 18.2 OHM, 1%, 402	R2100,R2113,R2126	NOSTUFF

INDICATOR LED

NOTICE OF PROPRIETARY PROPERTY

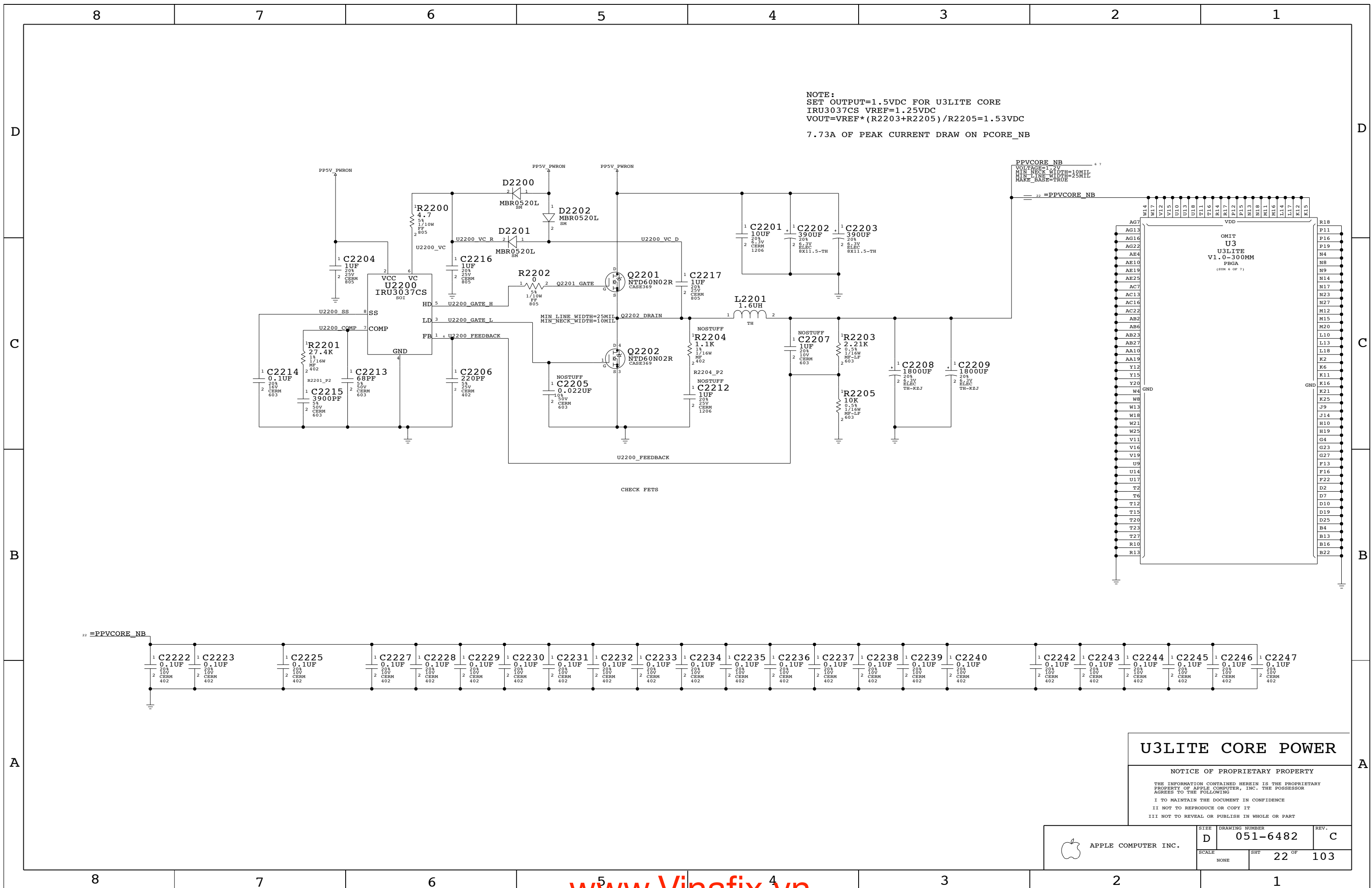
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	21	103	C



NOTE:
 SET OUTPUT=1.5VDC FOR U3LITE CORE
 IRU3037CS VREF=1.25VDC
 $V_{OUT} = V_{REF} * (R_{2203} + R_{2205}) / R_{2205} = 1.53VDC$
 7.73A OF PEAK CURRENT DRAW ON PCORE_NB

PPVCORE_NB
 VOLTAGE=1.2V
 MIN_TRACK_WIDTH=10MIL
 MIN_LINE_WIDTH=25MIL
 MAKE_BASE=TRUE

CHECK FETS

U3LITE CORE POWER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	NONE	SHT	22 OF 103

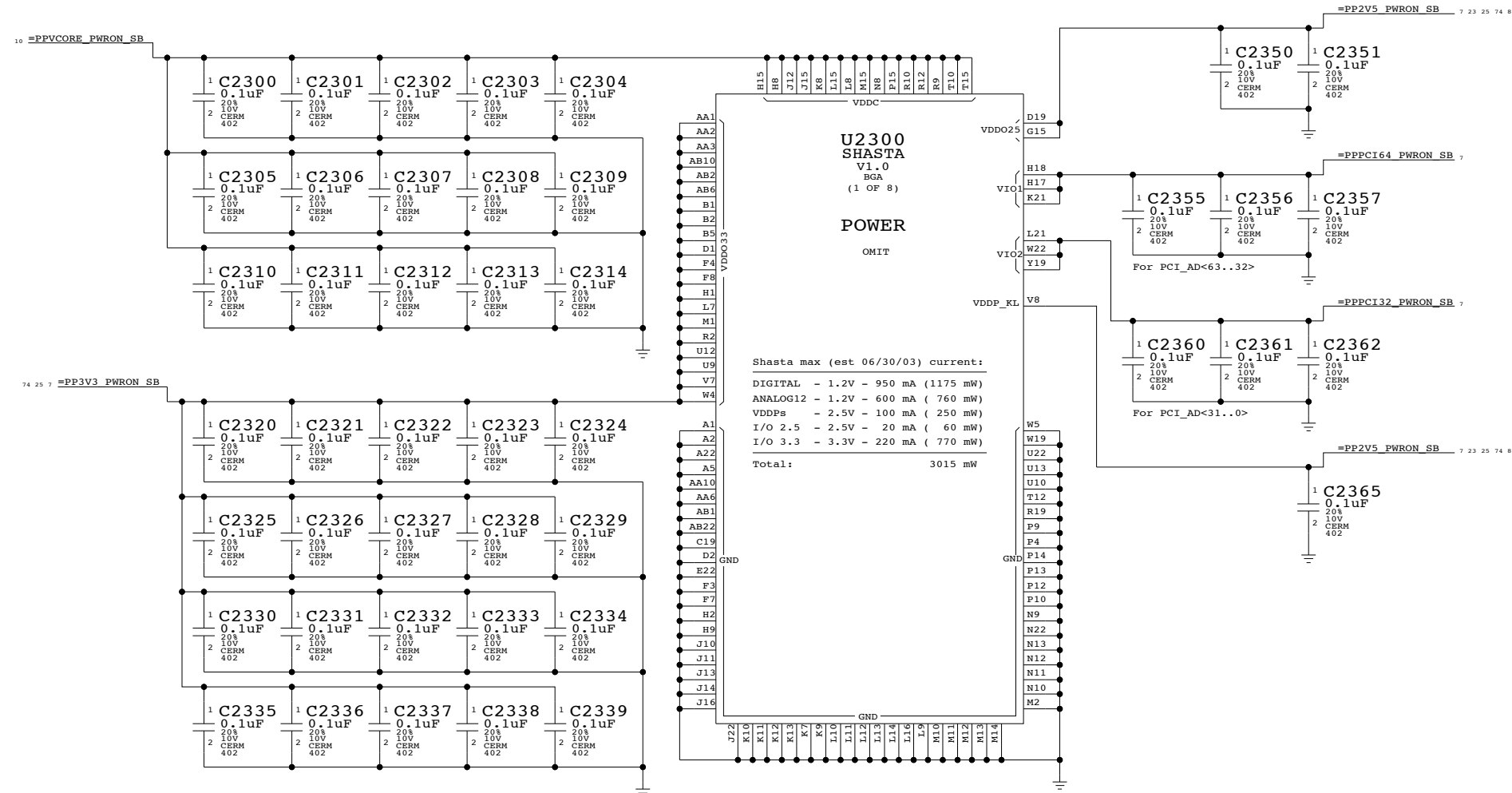
Page Notes

Power aliases required by this page:
 - _PPPCI164_PWRON_SB (to 5V or 3.3V)
 - _PPPCI32_PWRON_SB (to 5V or 3.3V)
 - _PP3V3_PWRON_SB
 - _PP2V5_PWRON_SB
 - _PPVCORE_PWRON_SB (1.2V)
 NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI164_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Power Sequencing:
 Must power Shasta VCore rail before any other Shasta supplies.



Master: Link

Shasta Core Power

NOTICE OF PROPRIETARY PROPERTY

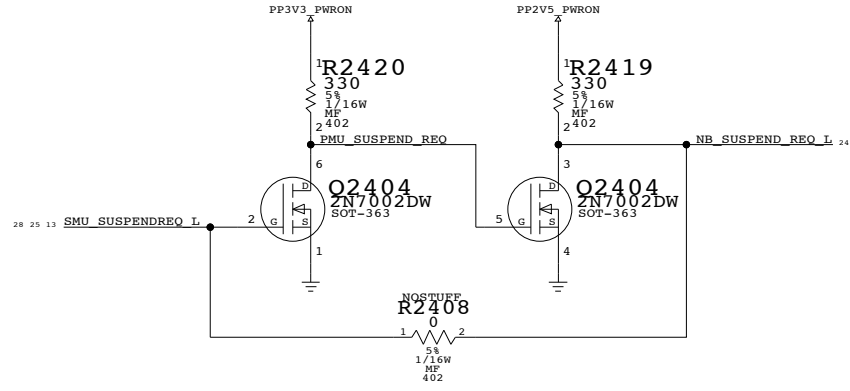
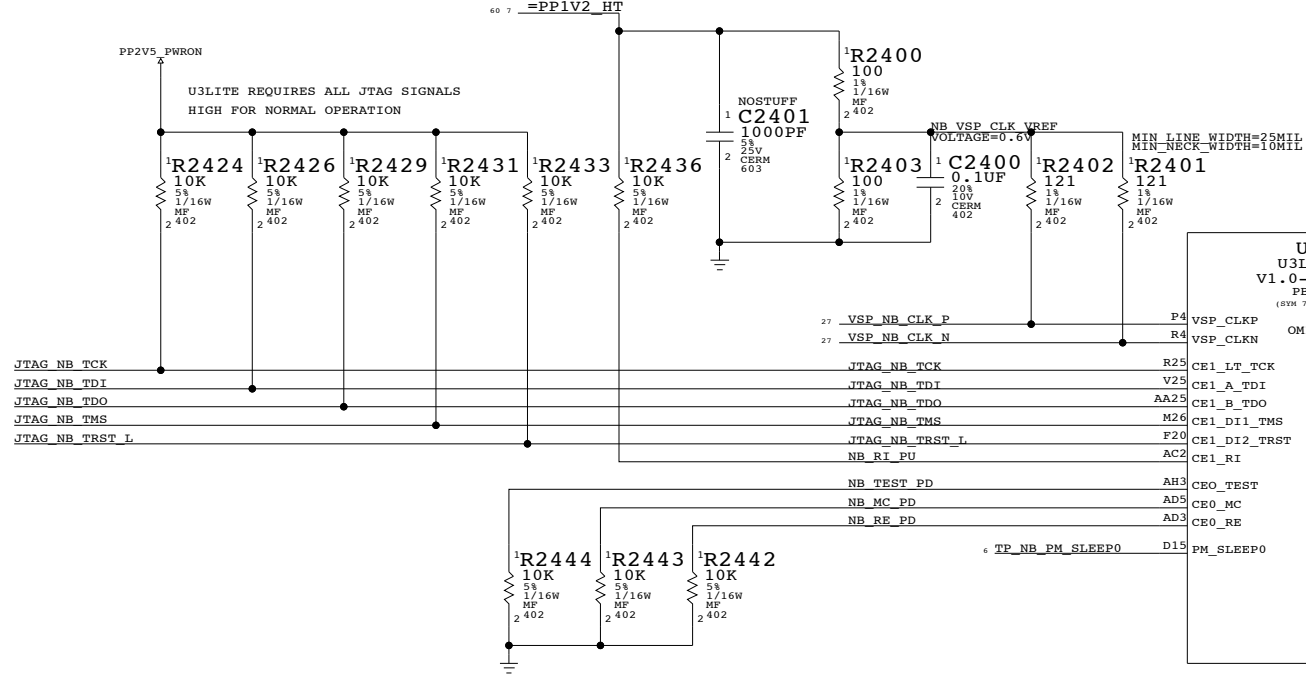
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_DRAWING
 TITLE=PIZZY
 ABBREV=DRAWING
 LAST_MODIFIED=Wed Aug 4 17:57:46 2004

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT		OF
NONE	23		103

D

D

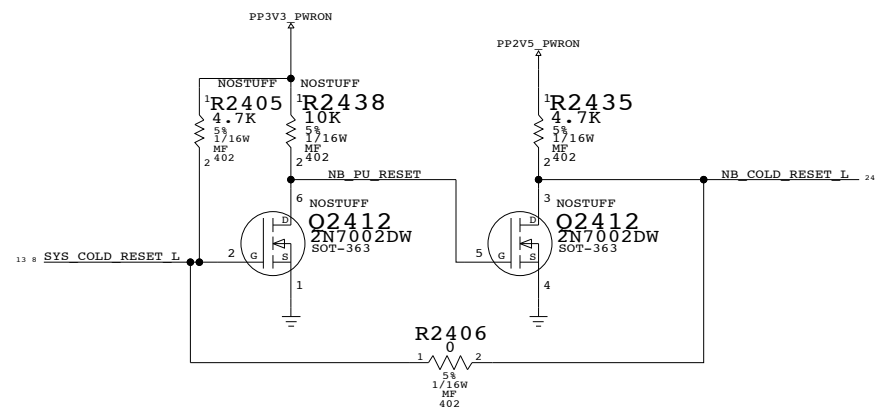


C

C

B

B



A

A

MASTER: GILA
LAST MODIFIED: JUNE 10, 04

U3LITE MISC

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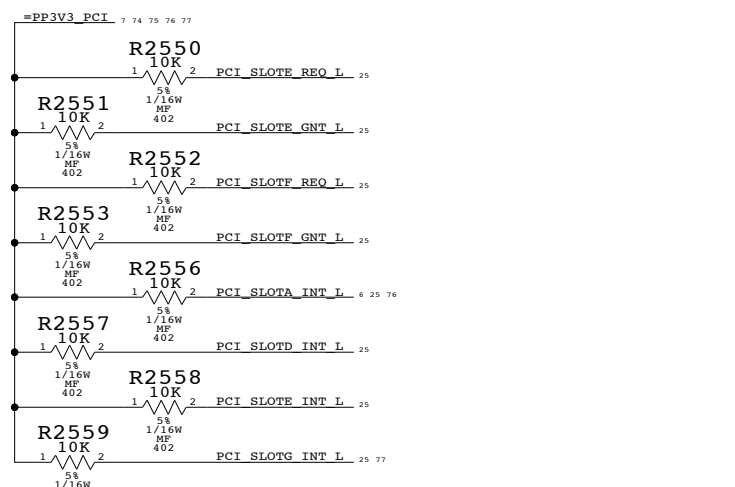
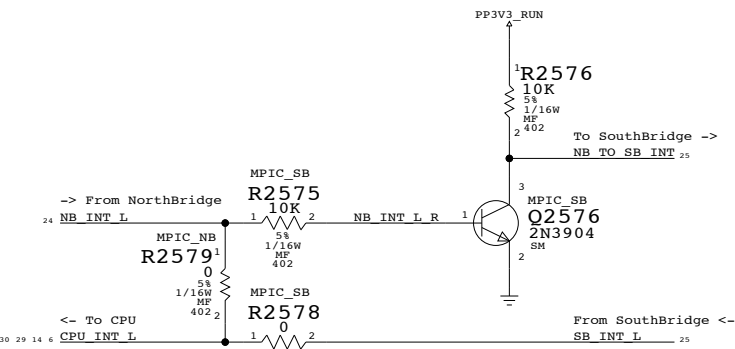
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	24 OF 103	
NONE			

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		I2S0_DEV_TO_SB DTI
I2S0_TO_DEV		I2S0_SB_TO_DEV DTO
I2S0_TO_DEV	AUDIO	I2S0_MCLK
I2S0_BIDIR		I2S0_BITCLK
I2S0_BIDIR		I2S0_SYNC
I2S1_TO_SB		I2S1_DEV_TO_SB DTI
I2S1_TO_DEV		I2S1_SB_TO_DEV DTO
I2S1_TO_DEV	10 MIL SPACING	I2S1_MCLK
I2S1_BIDIR		I2S1_BITCLK
I2S1_BIDIR		I2S1_SYNC
I2S2_TO_SB		I2S2_DEV_TO_SB DTI
I2S2_TO_DEV		I2S2_SB_TO_DEV DTO
I2S2_TO_DEV	10 MIL SPACING	I2S2_MCLK
I2S2_BIDIR		I2S2_BITCLK
I2S2_BIDIR		I2S2_SYNC
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALI
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALO
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALO_R
SB_CLK25M_ATA	15 MIL SPACING	SB_CLK25M_ATA

Page Notes

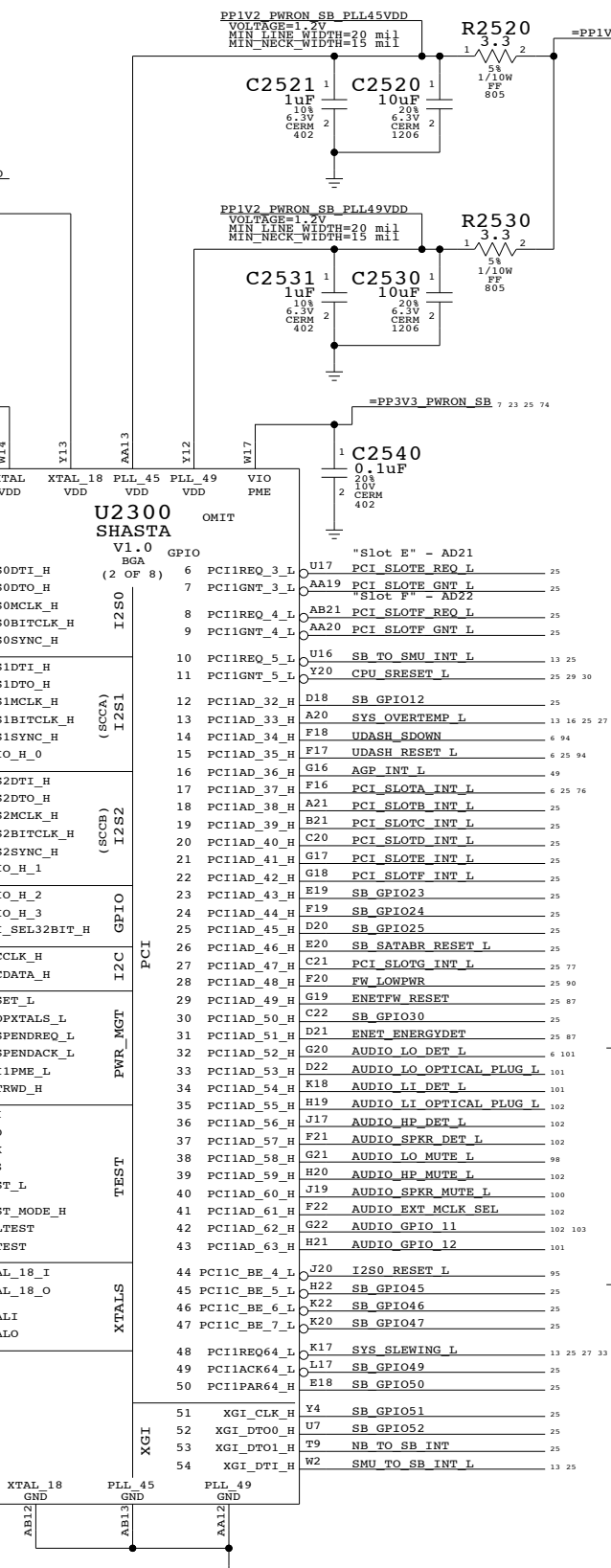
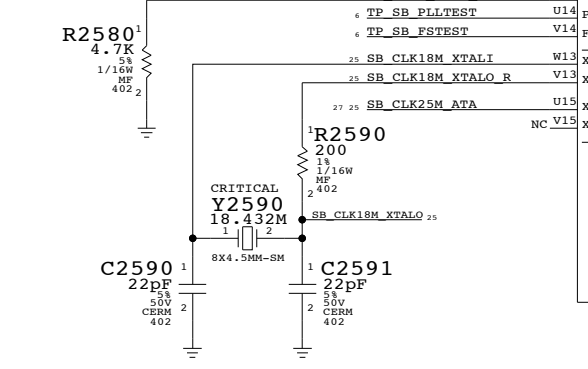
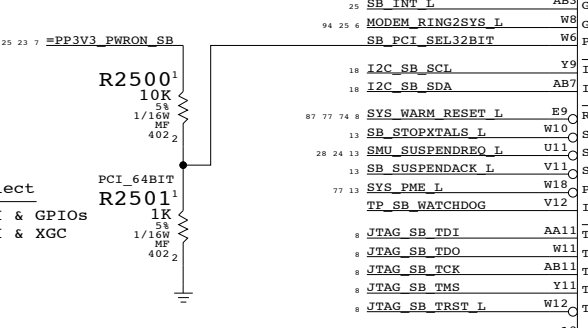
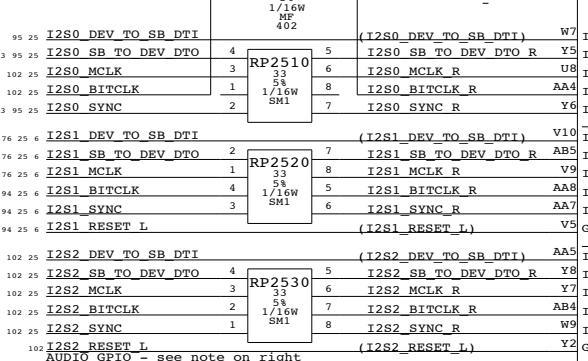
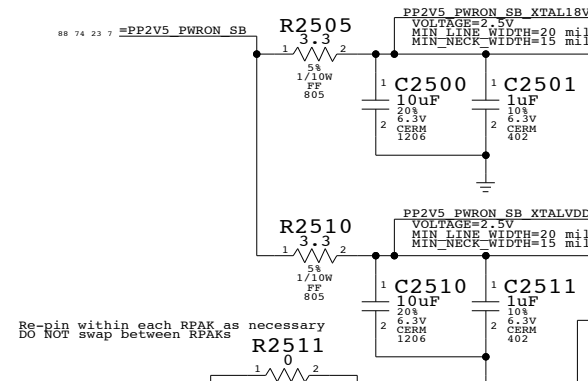
- Power aliases required by this page:
- PP3V3_PCI
 - PP3V3_PWRON_SB
 - PP2V5_PWRON_SB
 - PP1V2_PWRON_SB
- Signal aliases required by this page: (NONE)
- BOM options provided by this page:
- PCI_64BIT
 - Configures Shasta for 64-bit PCI
 - NOTE: XGC required for Shasta GPIOs
 - MPIC_NB/MPIC_SB
 - Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing

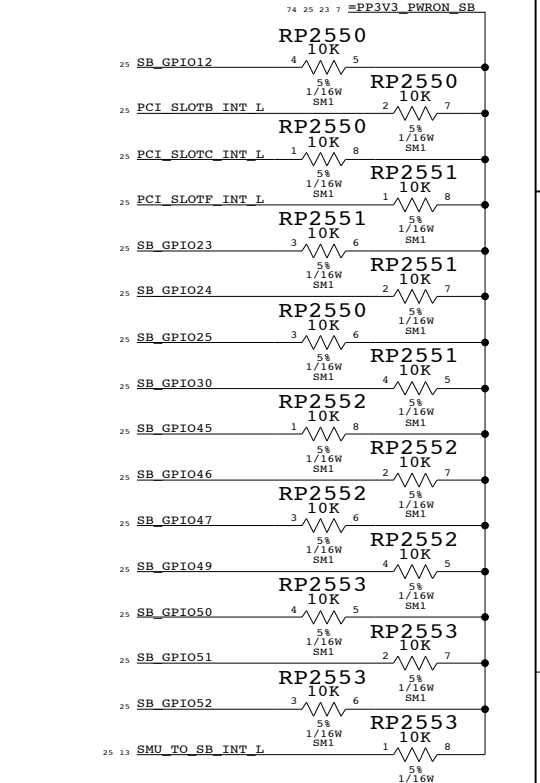
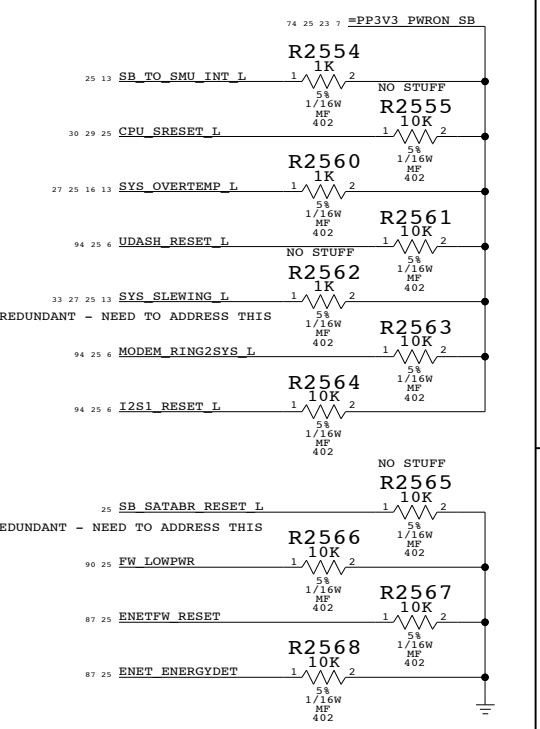


PCI 32-bit select
 1 = 32-bit PCI & GPIOs
 0 = 64-bit PCI & XGC

I2S1: Soft Modem
 I2S2: S/P-DIF



AUDIO GPIOs
 NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.



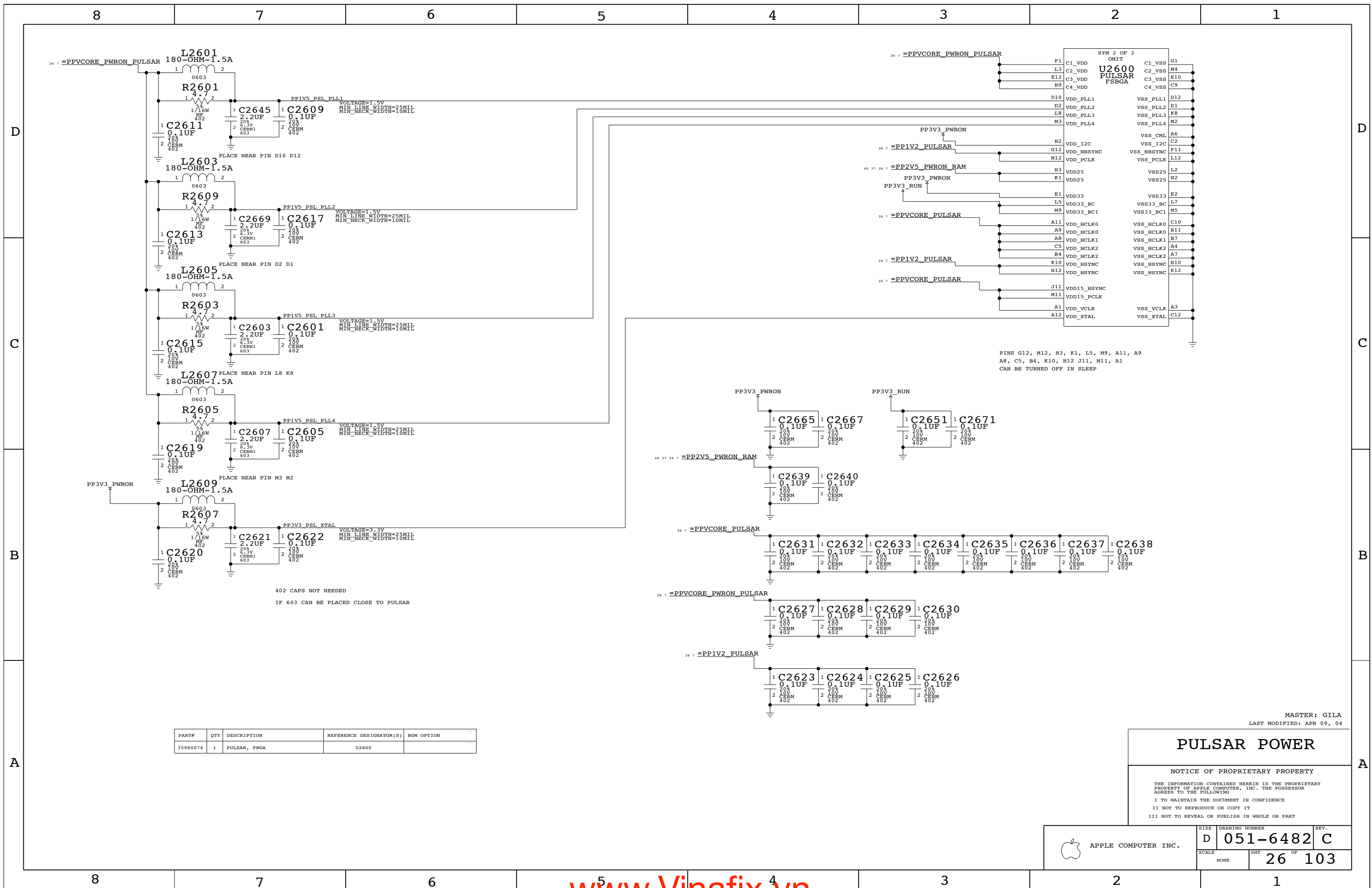
Master: Link

Shasta Serial / Misc

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402 CAPS NOT NEEDED
IF 603 CAN BE PLACED CLOSE TO PULSAR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, FBGA	U2600	

MASTER: GILA
LAST MODIFIED: APR 09, 04

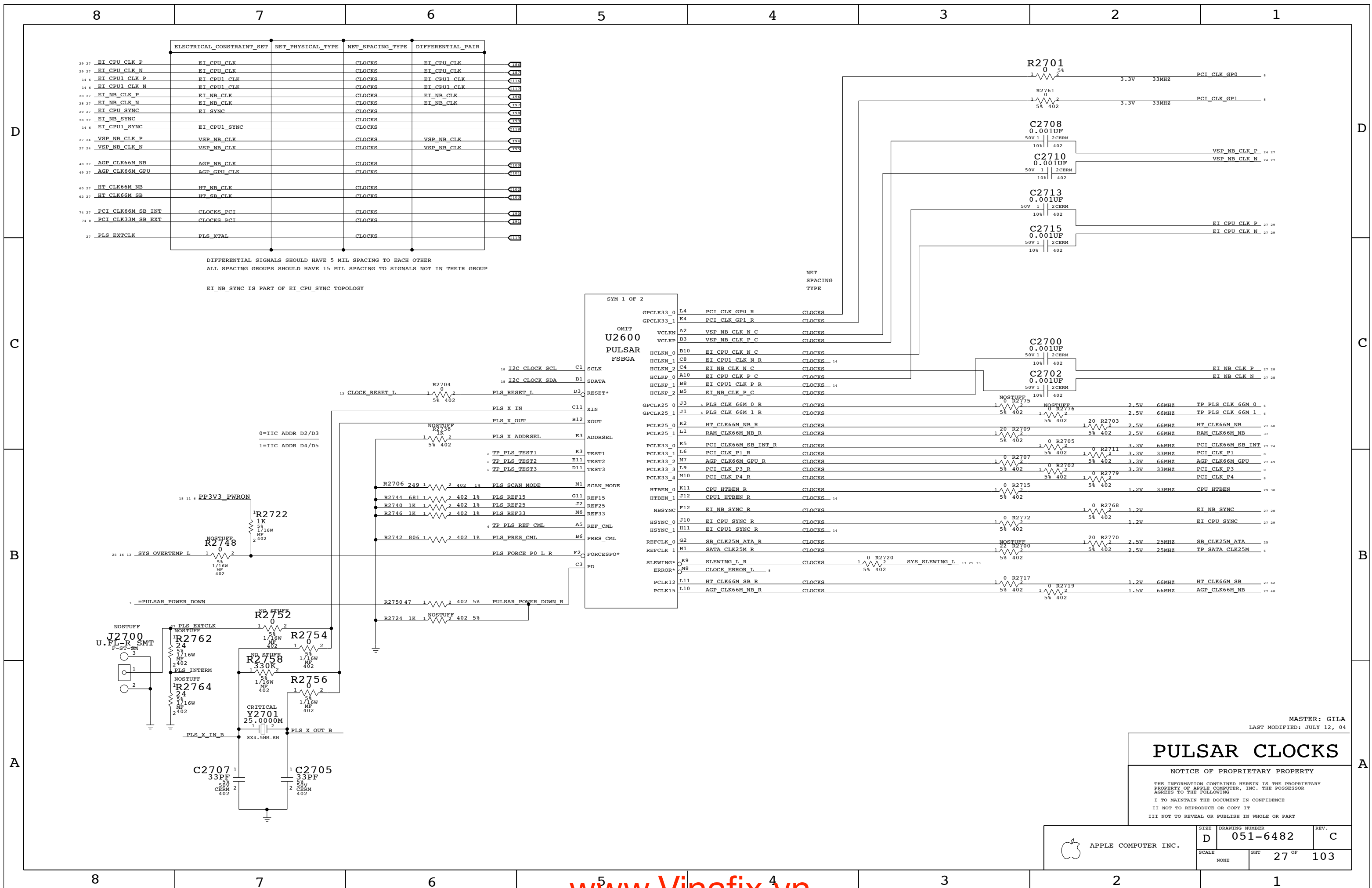
PULSAR POWER

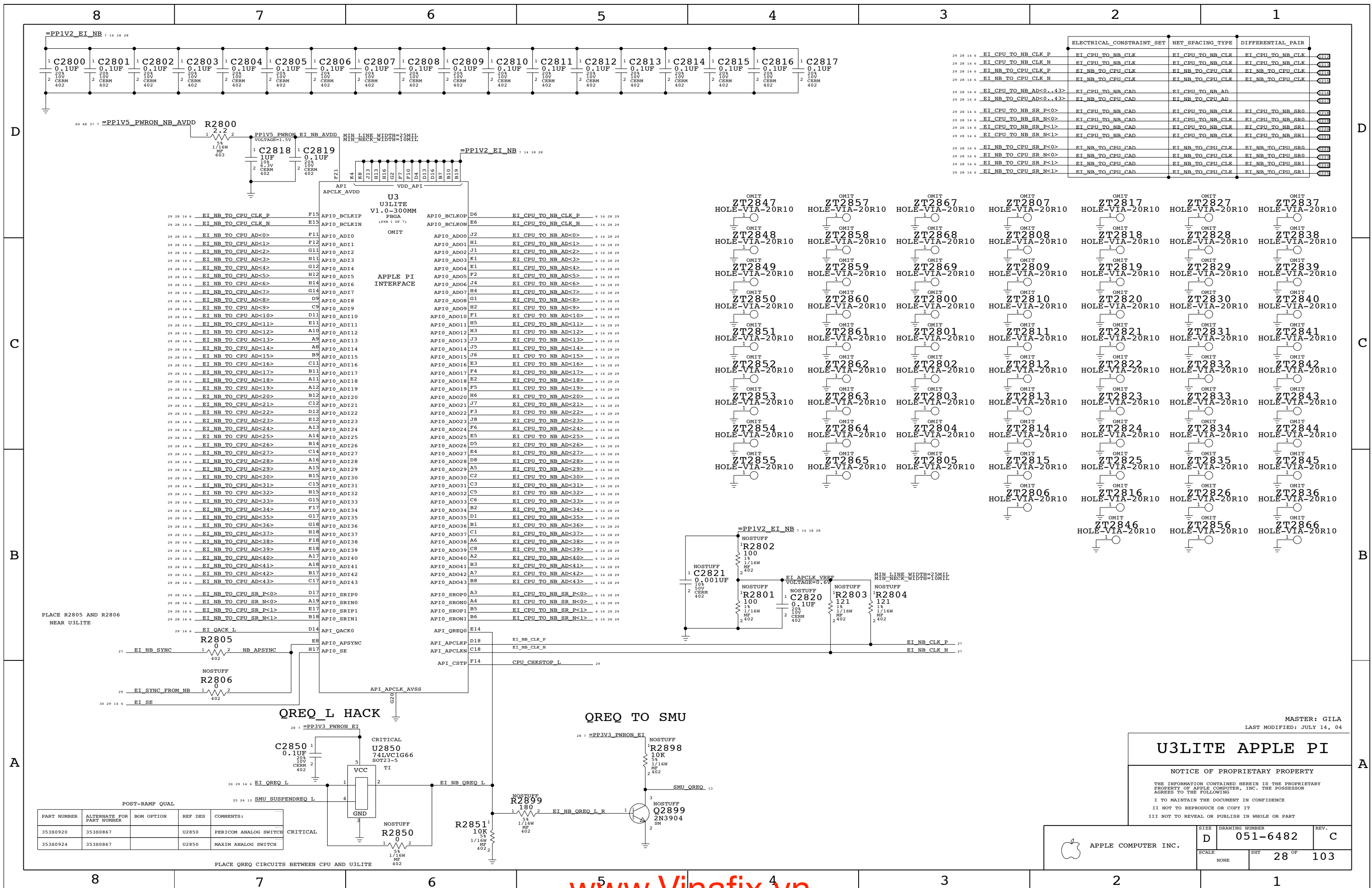
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	D	051-6482	C
SCALE	NONE	SHT	26 OF 103





ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR1
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR1

PLACE R2805 AND R2806 NEAR U3LITE

QREQ_L HACK

QREQ TO SMU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35380920	35380867		U2850	PERICOM ANALOG SWITCH
35380924	35380867		U2850	MAXIM ANALOG SWITCH

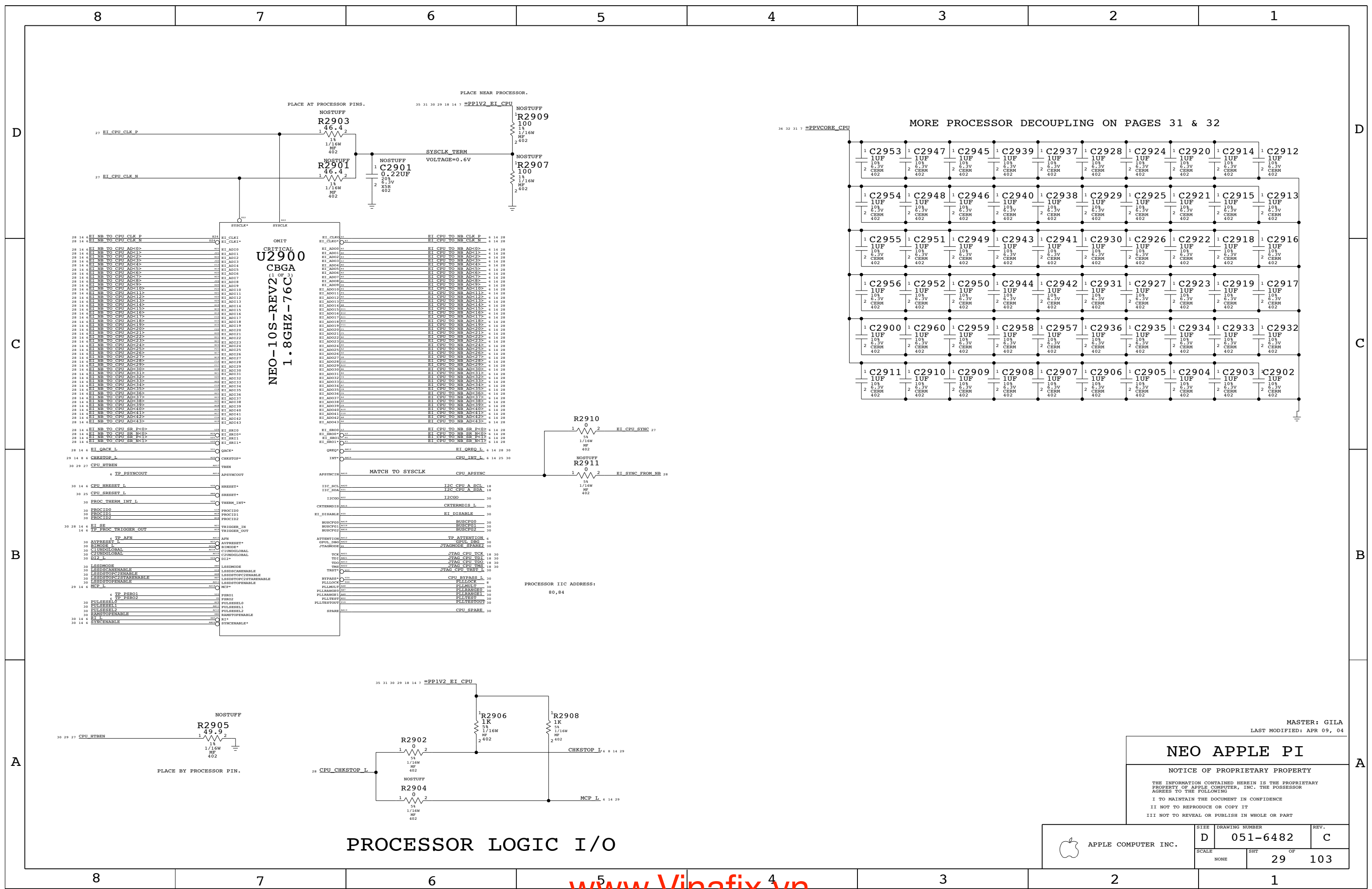
PLACE QREQ CIRCUITS BETWEEN CPU AND U3LITE

MASTER: GILA
LAST MODIFIED: JULY 14, 04

U3LITE APPLE PI

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	D	051-6482	C
SCALE	SHT	28 OF 103	
NONE			



CRITICAL
U2900
 NEO-10S-REV2
 CBGA
 (1 OF 1)
 1.8GHZ-76C

MORE PROCESSOR DECOUPLING ON PAGES 31 & 32

PROCESSOR IIC ADDRESS:
 80,84

MASTER: GILA
 LAST MODIFIED: APR 09, 04

NEO APPLE PI

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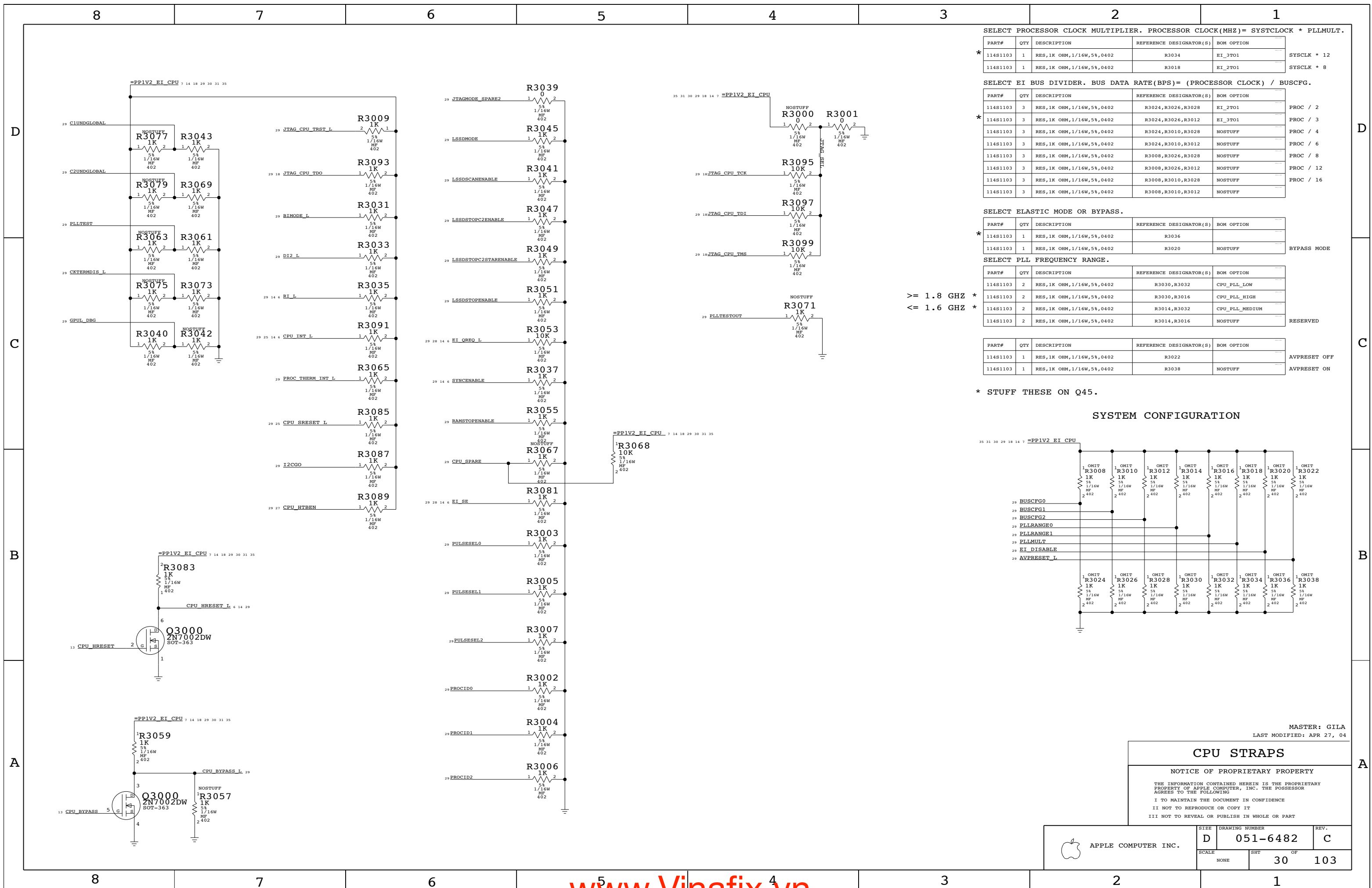
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PROCESSOR LOGIC I/O

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	NONE	SHT	OF
		29	103



SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3T01
11481103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2T01

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2T01
11481103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3T01
11481103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF
11481103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF
11481103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF
11481103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF
11481103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481103	1	RES,1K OHM,1/16W,5%,0402	R3036	
11481103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF

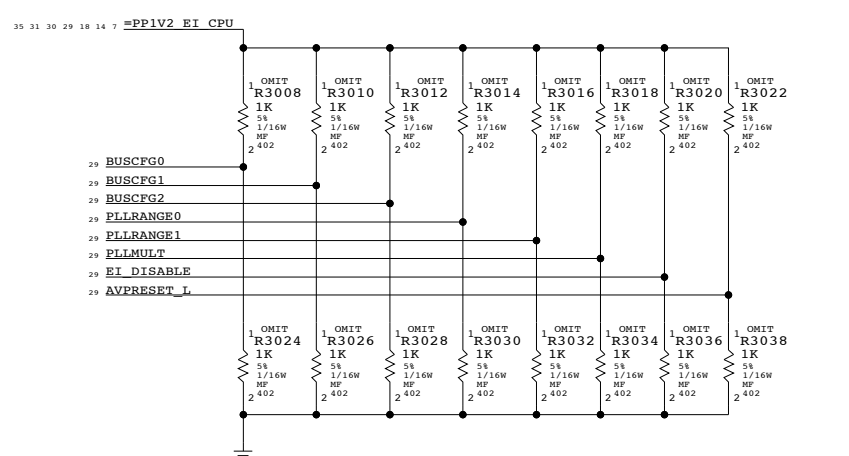
SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW
11481103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH
11481103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM
11481103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481103	1	RES,1K OHM,1/16W,5%,0402	R3022	AVPRESET OFF
11481103	1	RES,1K OHM,1/16W,5%,0402	R3038	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



MASTER: GILA
LAST MODIFIED: APR 27, 04

CPU STRAPS

NOTICE OF PROPRIETARY PROPERTY

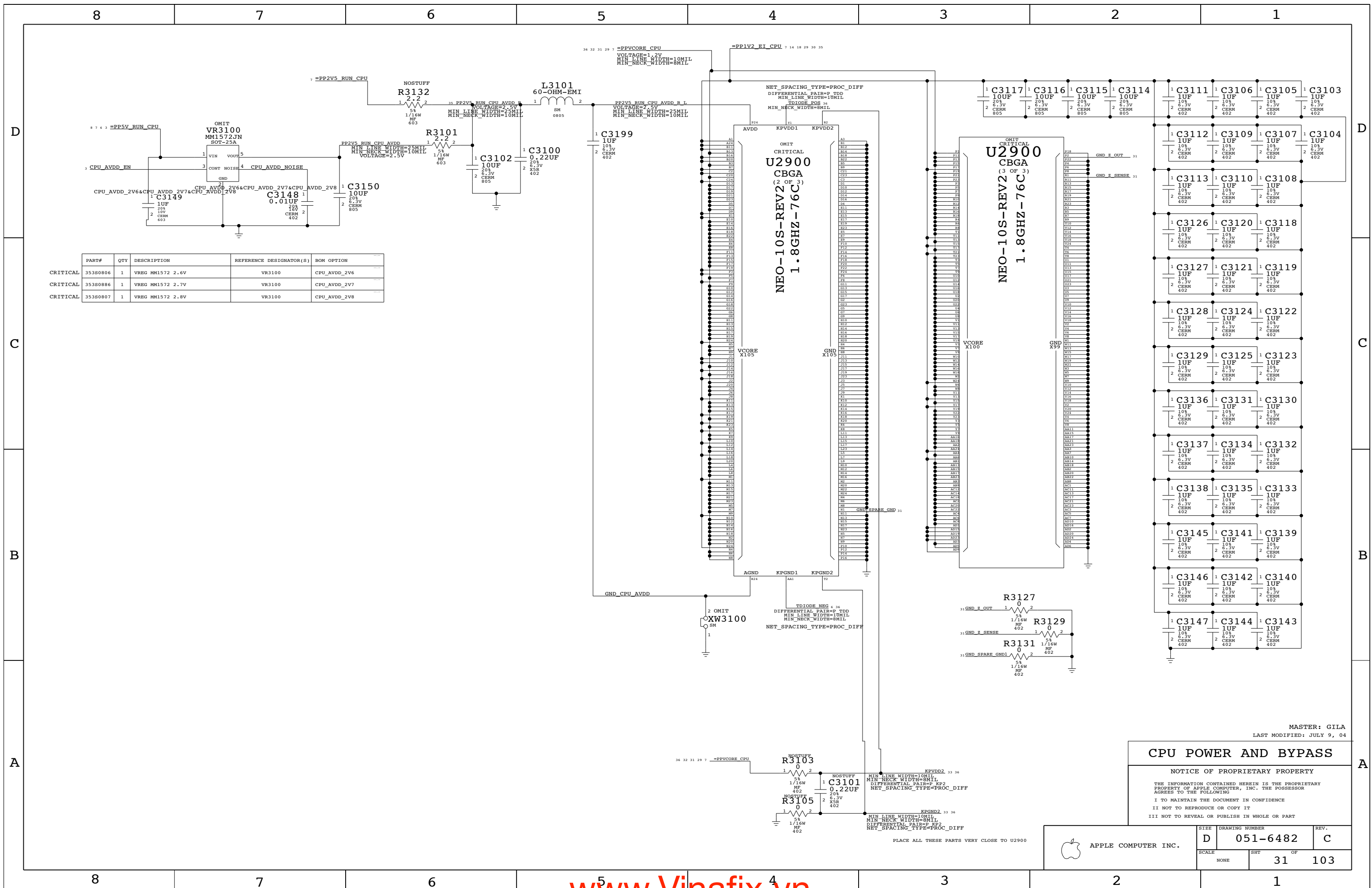
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	D	051-6482	C
SCALE	SHT OF		
NONE	30		103



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL 3538086	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL 3538086	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL 3538087	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

MASTER: GILA
LAST MODIFIED: JULY 9, 04

CPU POWER AND BYPASS

NOTICE OF PROPRIETARY PROPERTY

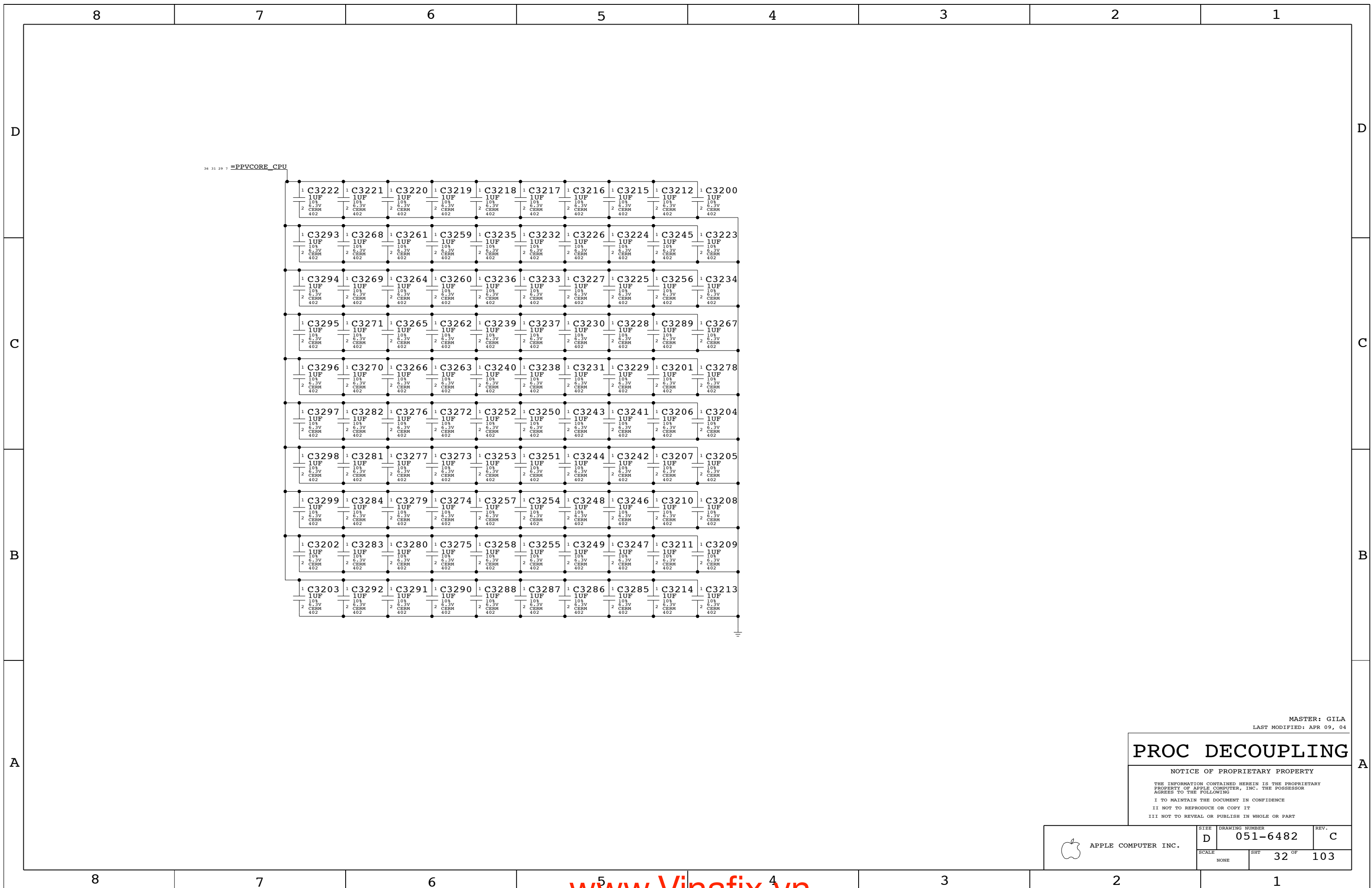
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	D	051-6482	C
SCALE	SHT OF		
NONE	31		103

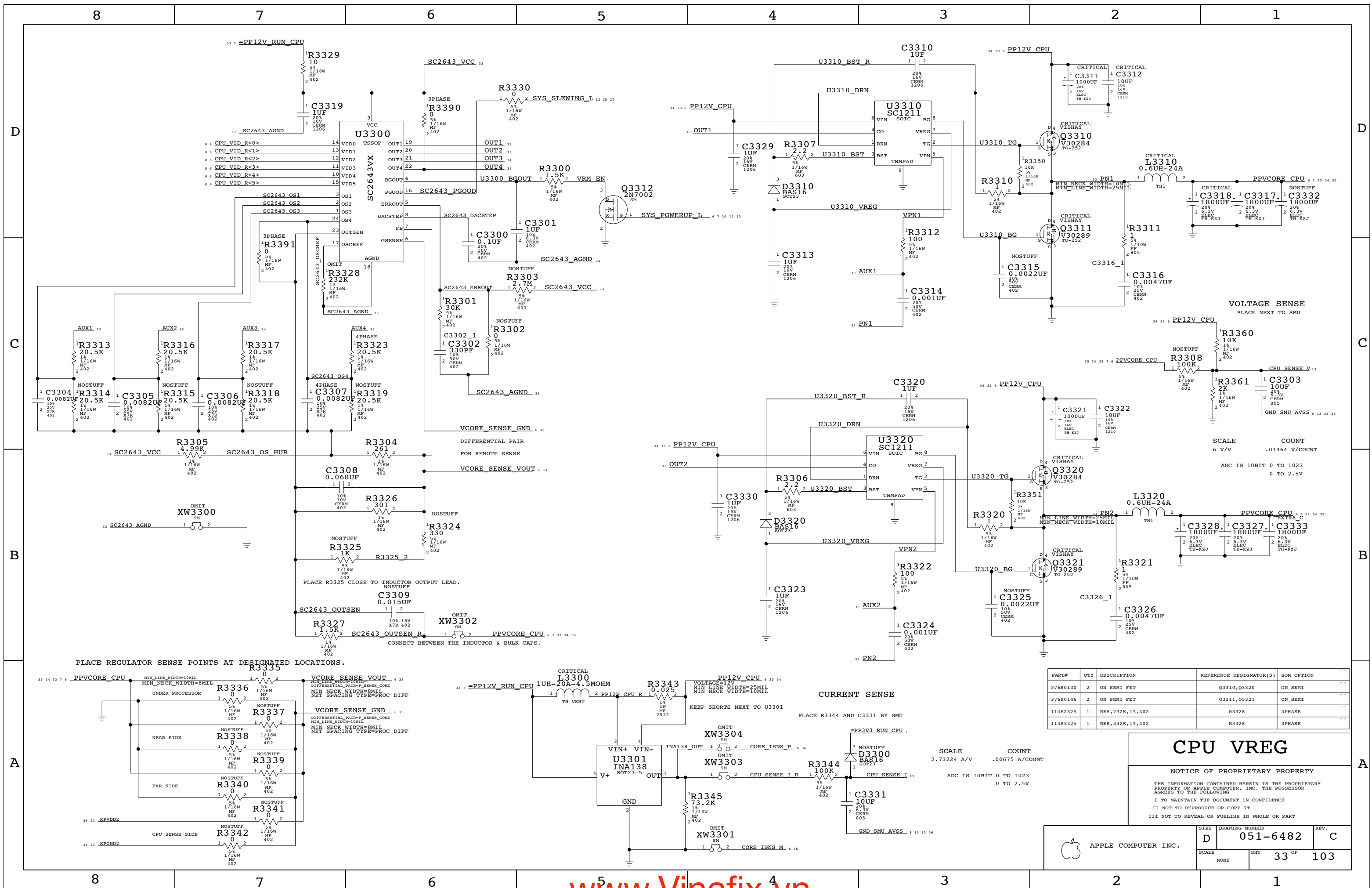


MASTER: GILA
 LAST MODIFIED: APR 09, 04

PROC DECOUPLING

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	OF	
NONE	32	103	

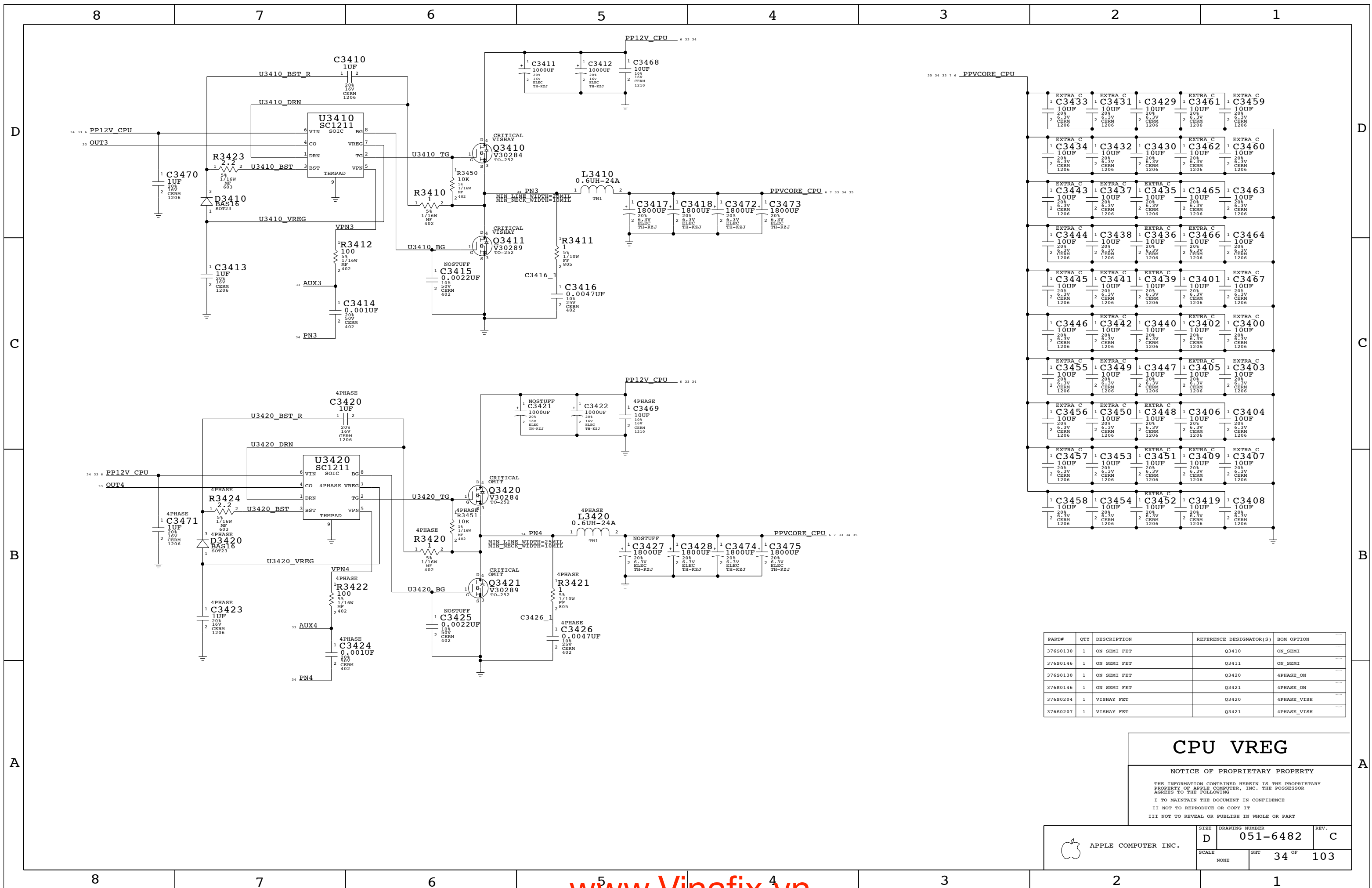


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
37650130	2	ON SEMI FET	Q3310, Q3320	ON_SEMI
37680146	2	ON SEMI FET	Q3311, Q3321	ON_SEMI
11482325	1	RES, 232K, 1%, 402	R3328	4PHASE
11483325	1	RES, 332K, 1%, 402	R3328	3PHASE

CPU VREG

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	33 OF	103
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
37680130	1	ON SEMI FET	Q3410	ON_SEMI
37680146	1	ON SEMI FET	Q3411	ON_SEMI
37680130	1	ON SEMI FET	Q3420	4PHASE_ON
37680146	1	ON SEMI FET	Q3421	4PHASE_ON
37680204	1	VISHAY FET	Q3420	4PHASE_VISH
37680207	1	VISHAY FET	Q3421	4PHASE_VISH

CPU VREG

NOTICE OF PROPRIETARY PROPERTY

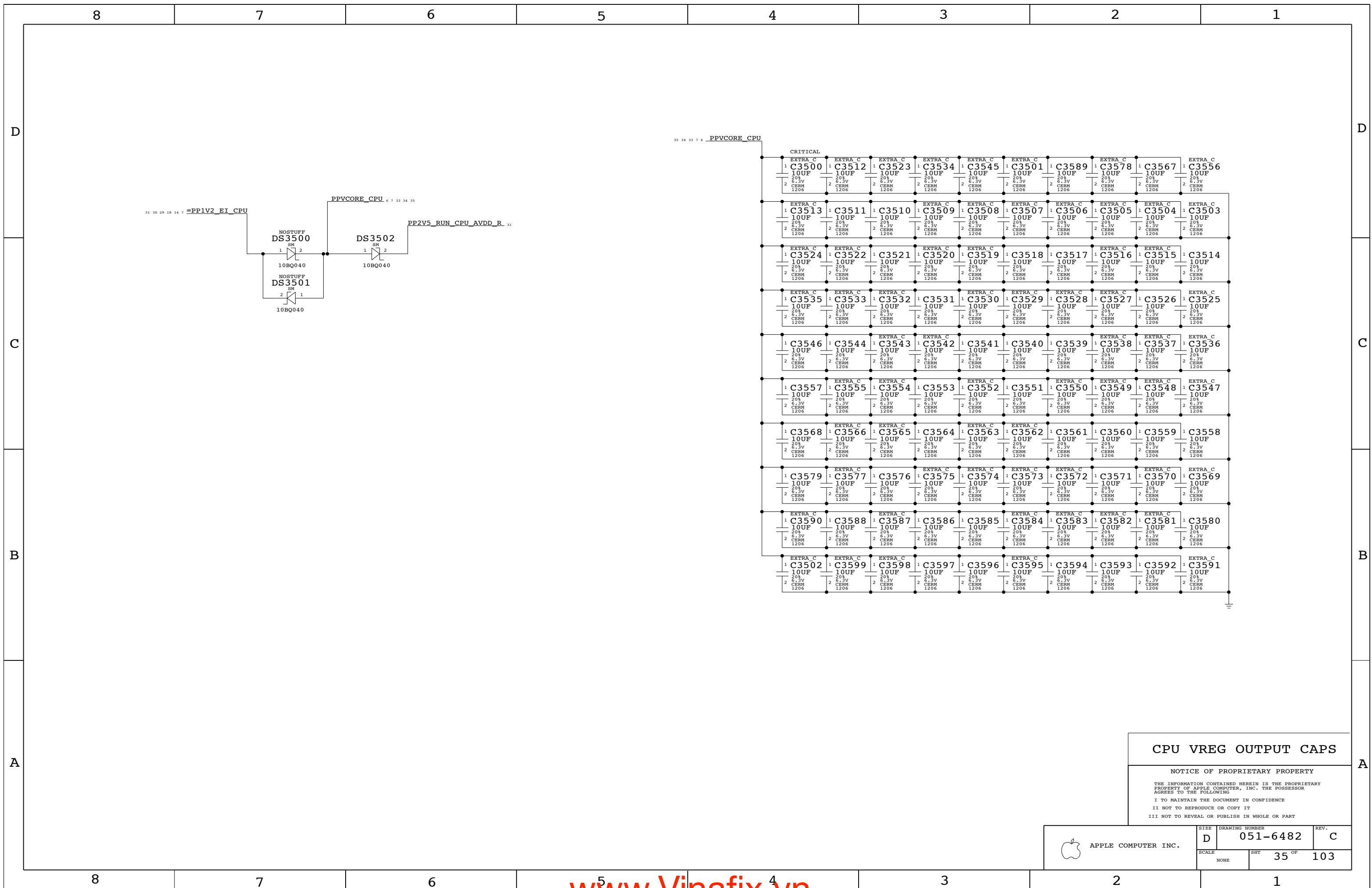
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	D	051-6482	C
SCALE	NONE	SHT	34 OF 103



CPU VREG OUTPUT CAPS

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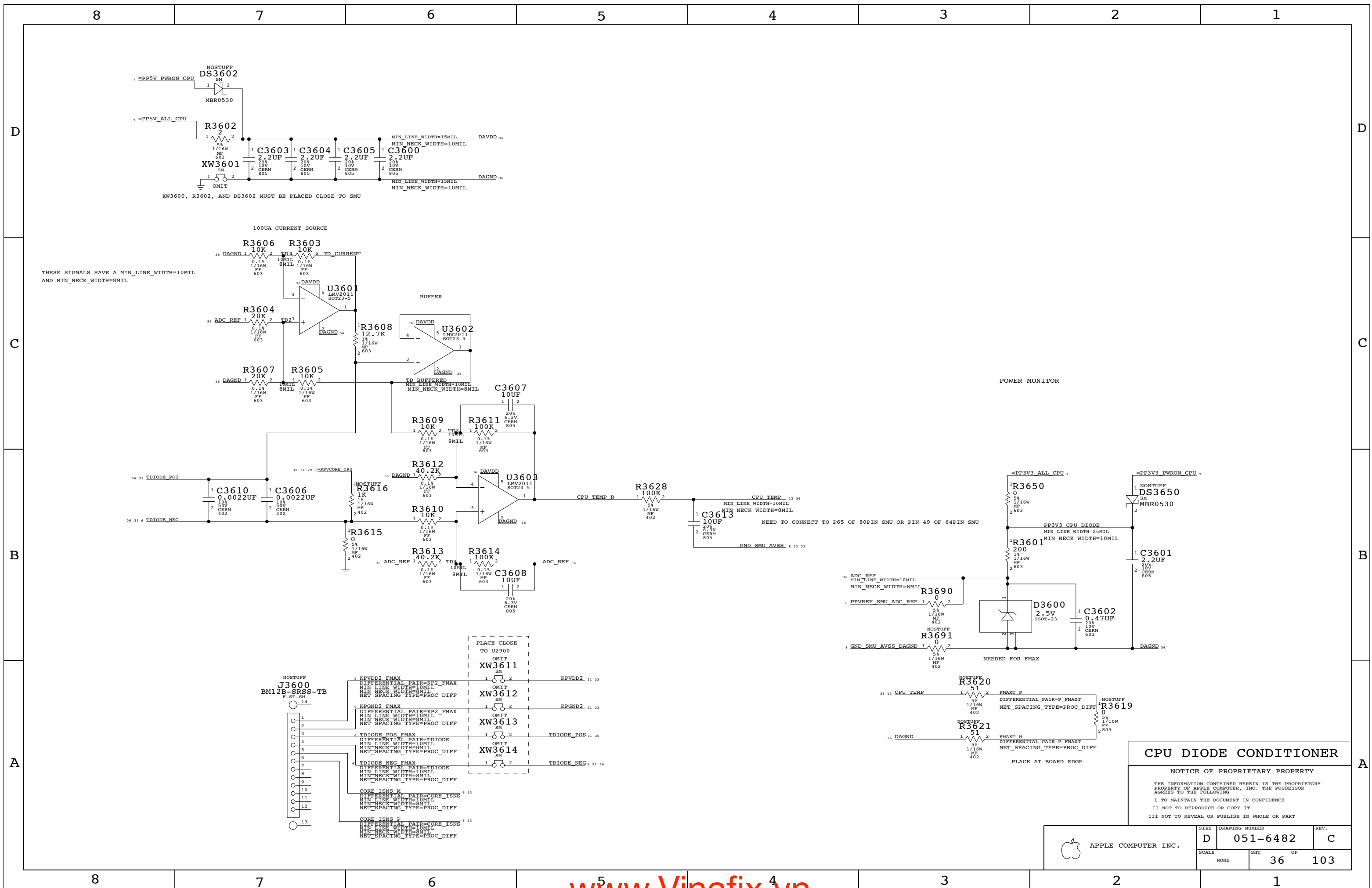
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SCALE	SHT		REV.
NONE	35 OF		103

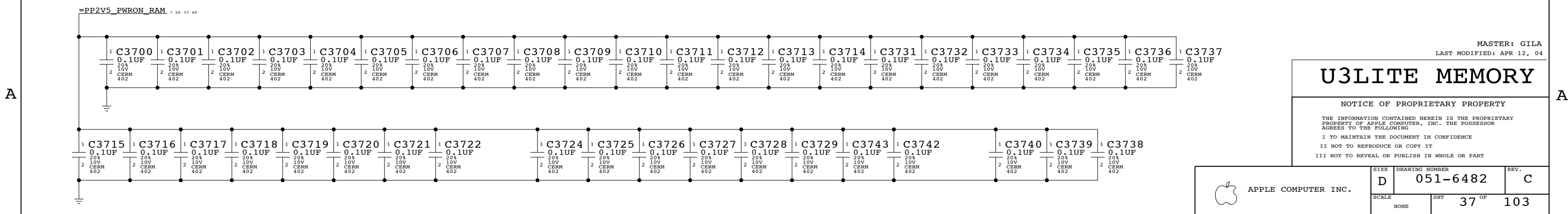
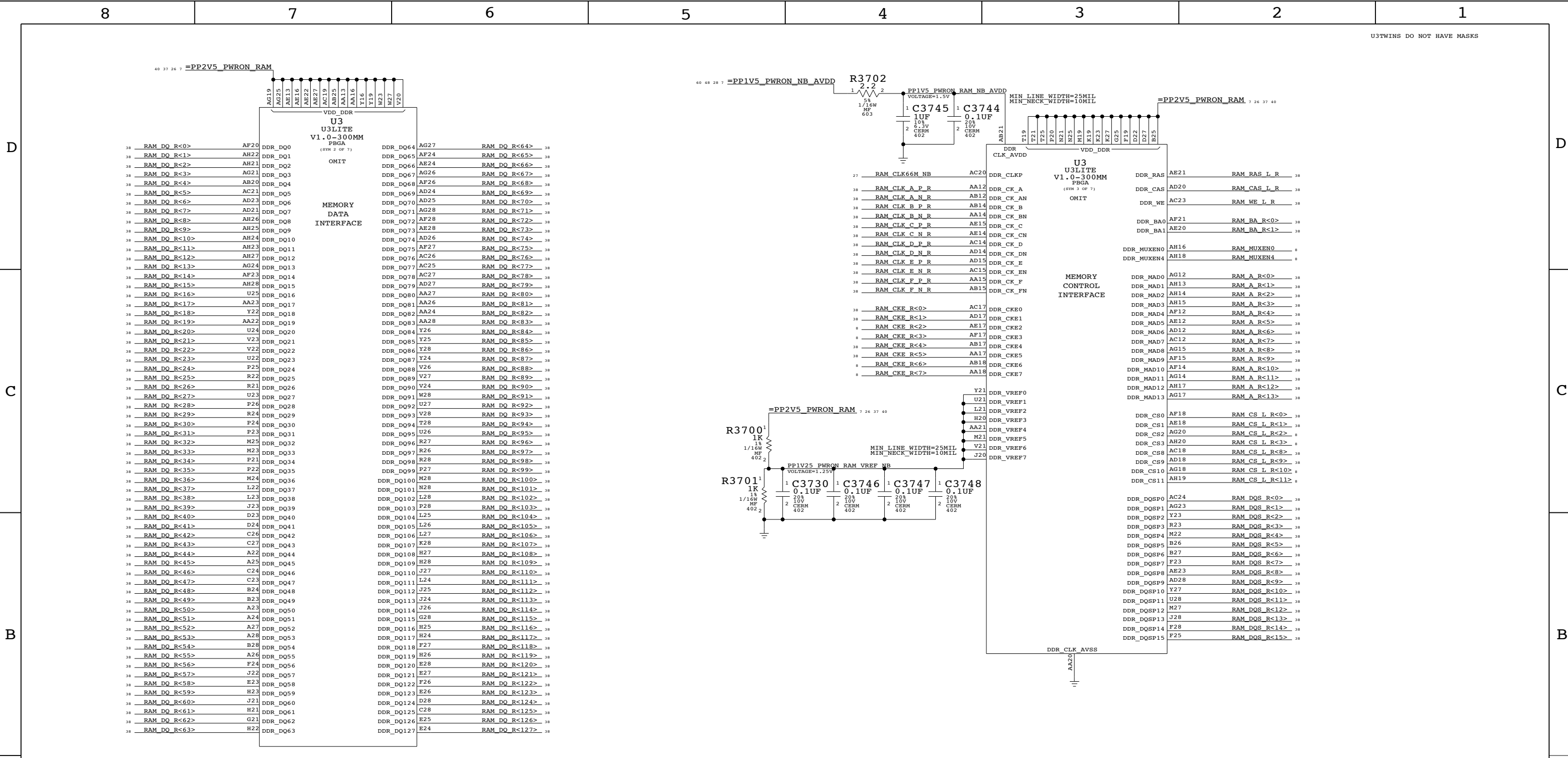


CPU DIODE CONDITIONER

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SCALE	SHT	OF	
NONE	36	103	



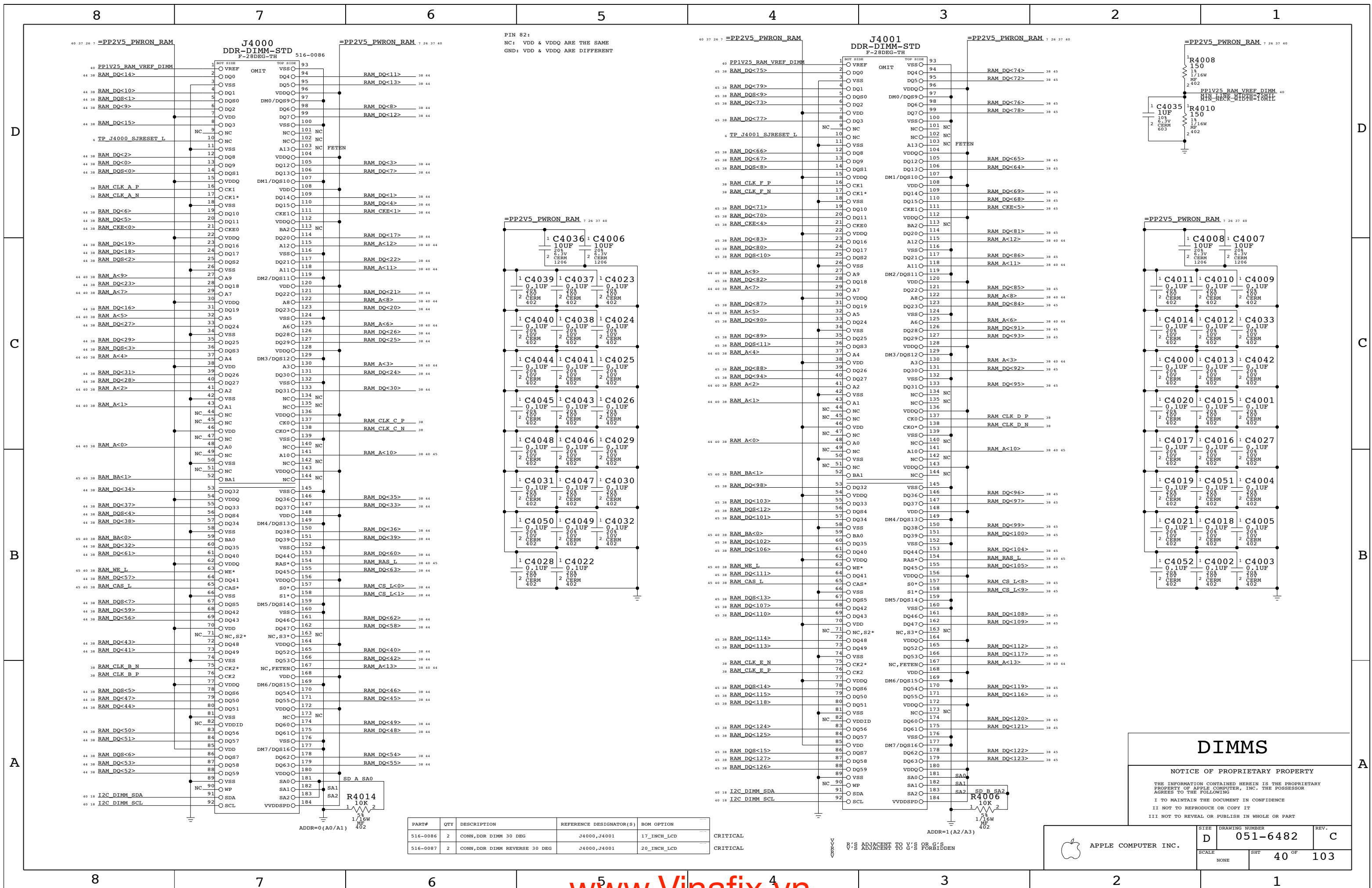
MASTER: GILA
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SCALE	SHT	37 OF 103	
NONE			

8		7		6		5		4		3		2		1			
ALL R PACKS ARE 1/16W 5%																	
ELECTRICAL_CONSTRAINT_SET																	
NET_PHYSICAL_TYPE																	
NET_SPACING_TYPE																	
DIFFERENTIAL_PAIR																	
38 37	RAM_DQ_R<7>	RP3836	4	5	22	RAM_DQ<7>	38 40	44	38 37	RAM_CLK_A_P_R		RAM_CLK	RAM_CLK_A_R		0405		
38 37	RAM_DQ_R<2>	RP3836	1	8	22	RAM_DQ<2>	38 40	44	38 37	RAM_CLK_A_N_R		RAM_CLK	RAM_CLK_A_R		0405		
38 37	RAM_DQ_R<0>	RP3836	3	6	22	RAM_DQ<0>	38 40	44	38 37	RAM_CLK_B_P_R		RAM_CLK	RAM_CLK_B_R		0405		
38 37	RAM_DQ_R<3>	RP3836	2	7	22	RAM_DQ<3>	38 40	44	38 37	RAM_CLK_B_N_R		RAM_CLK	RAM_CLK_B_R		0405		
38 37	RAM_DQ_R<1>	RP3816	1	8	22	RAM_DQ<1>	38 40	44	38 37	RAM_CLK_C_P_R		RAM_CLK	RAM_CLK_C_R		0405		
38 37	RAM_DQ_R<4>	RP3816	2	7	22	RAM_DQ<4>	38 40	44	38 37	RAM_CLK_C_N_R		RAM_CLK	RAM_CLK_C_R		0405		
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38 37	RAM_DQ_R<9>	RP3835	4	5	22	RAM_DQ<9>	38 40	44	38 37	RAM_CLK_E_P_R		RAM_CLK	RAM_CLK_E_R		0405		
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38 37	RAM_DQ_R<12>	RP3835	2	7	22	RAM_DQ<12>	38 40	44	40 38	RAM_CLK_A_P	RAM_CLK0	RAM_CLK	RAM_CLK_A		0405		
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38 37	RAM_DQ_R<32>	RP3826	4	5	22	RAM_DQ<32>	38 40	44	44 40 38	RAM_CS_L<0>	RAM_CKECS0	RAM_CAD			0405		
38 37	RAM_DQ_R<35>	RP3807	2	7	22	RAM_DQ<35>	38 40	44	44 40 38	RAM_CS_L<1>	RAM_CKECS0	RAM_CAD			0405		
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THE FOLLOWING IS A SWAPPABLE GROUP																	
38 37	RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>	38 40	45	38 37	RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P	38 40	45
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38 37	RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>	38 40	44	38 37	RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P	38 40	45
38 37	RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>	38 40	44	38 37	RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N	38 40	45
38 37	RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>	38 40	45	38 37	RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P	38 40	45
38 37	RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>	38 40	45	38 37	RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N	38 40	45
38 37	RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>	38 40	44	38 37	RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P	38 40	45
38 37	RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>	38 40	44	38 37	RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N	38 40	45
38 37	RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>	38 40	44	38 37	RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P	38 40	45
38 37	RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>	38 40	44	38 37	RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N	38 40	45
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38 37	RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L	38 40	45	38 37	RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N	38 40	45
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38 37	RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>	38 40	44	38 37	RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>	38 40	44
38 37	RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>	38 40	44	38 37	RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>	38 40</	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
516-0086	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD
516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD

DIMMS

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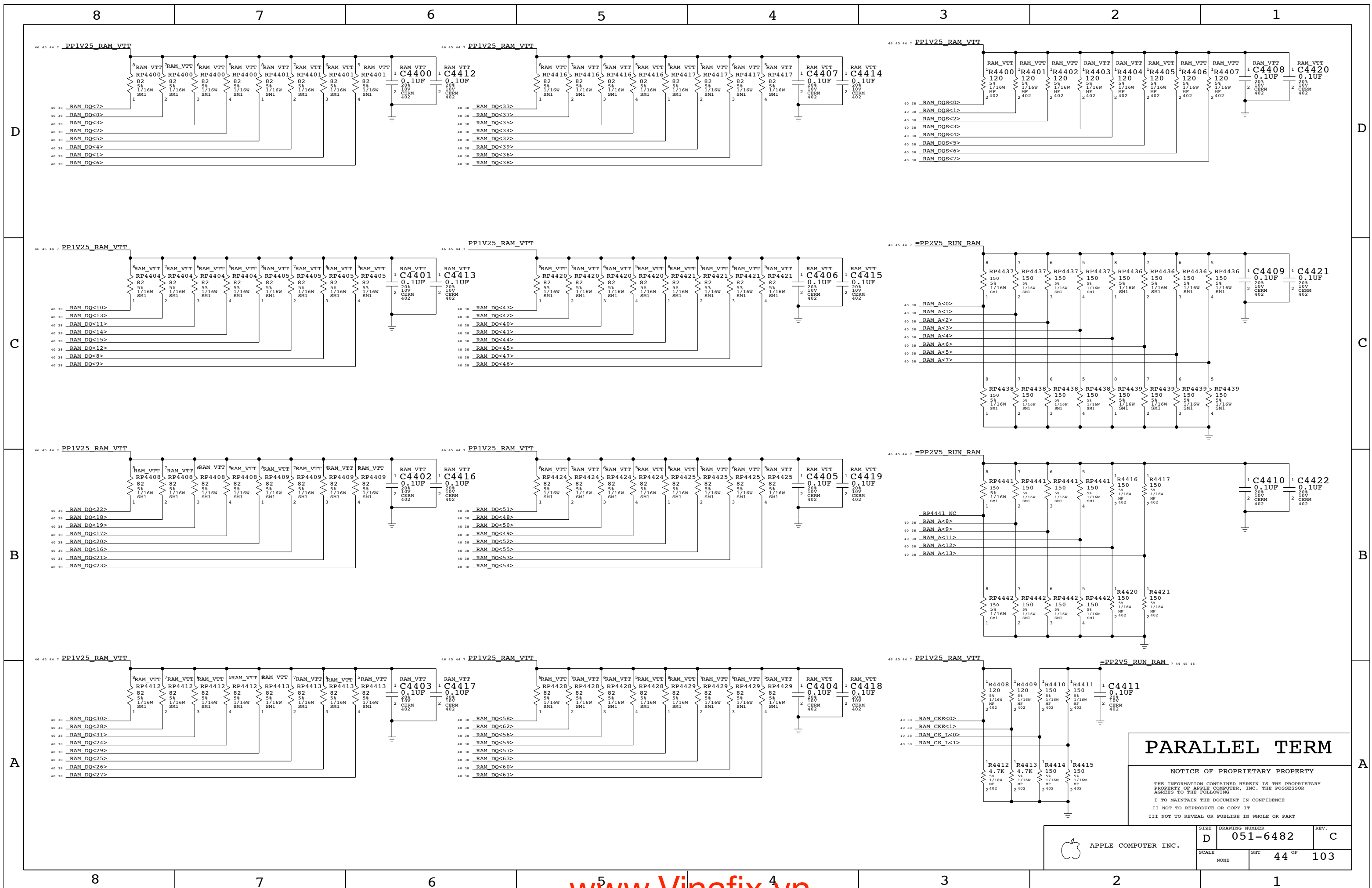
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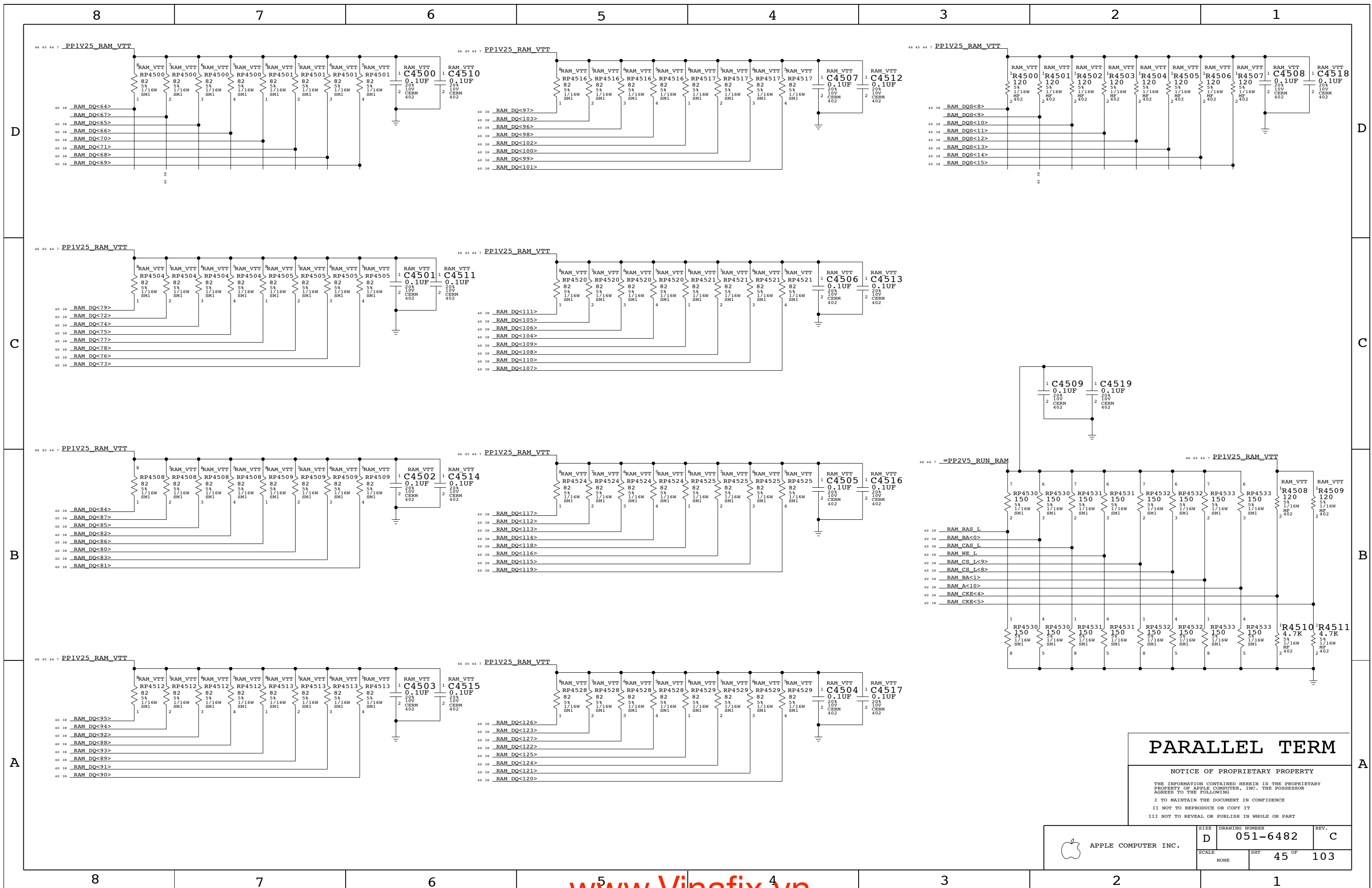
	SCALE	SHEET	REV.
	NONE	40 OF 103	C



PARALLEL TERM

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SCALE	SHT	44 OF 103	
NONE			

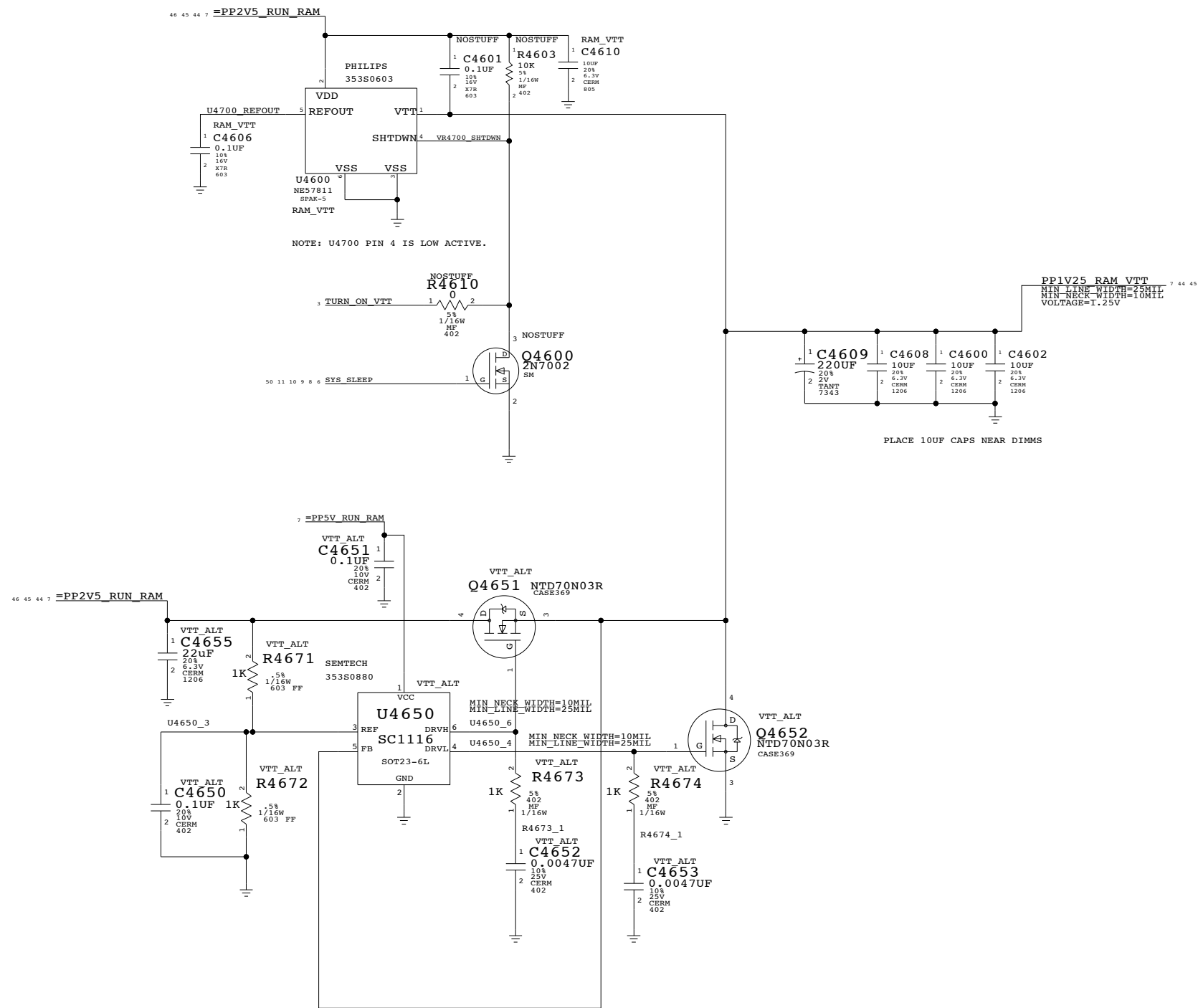


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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHEET 45 OF 103	

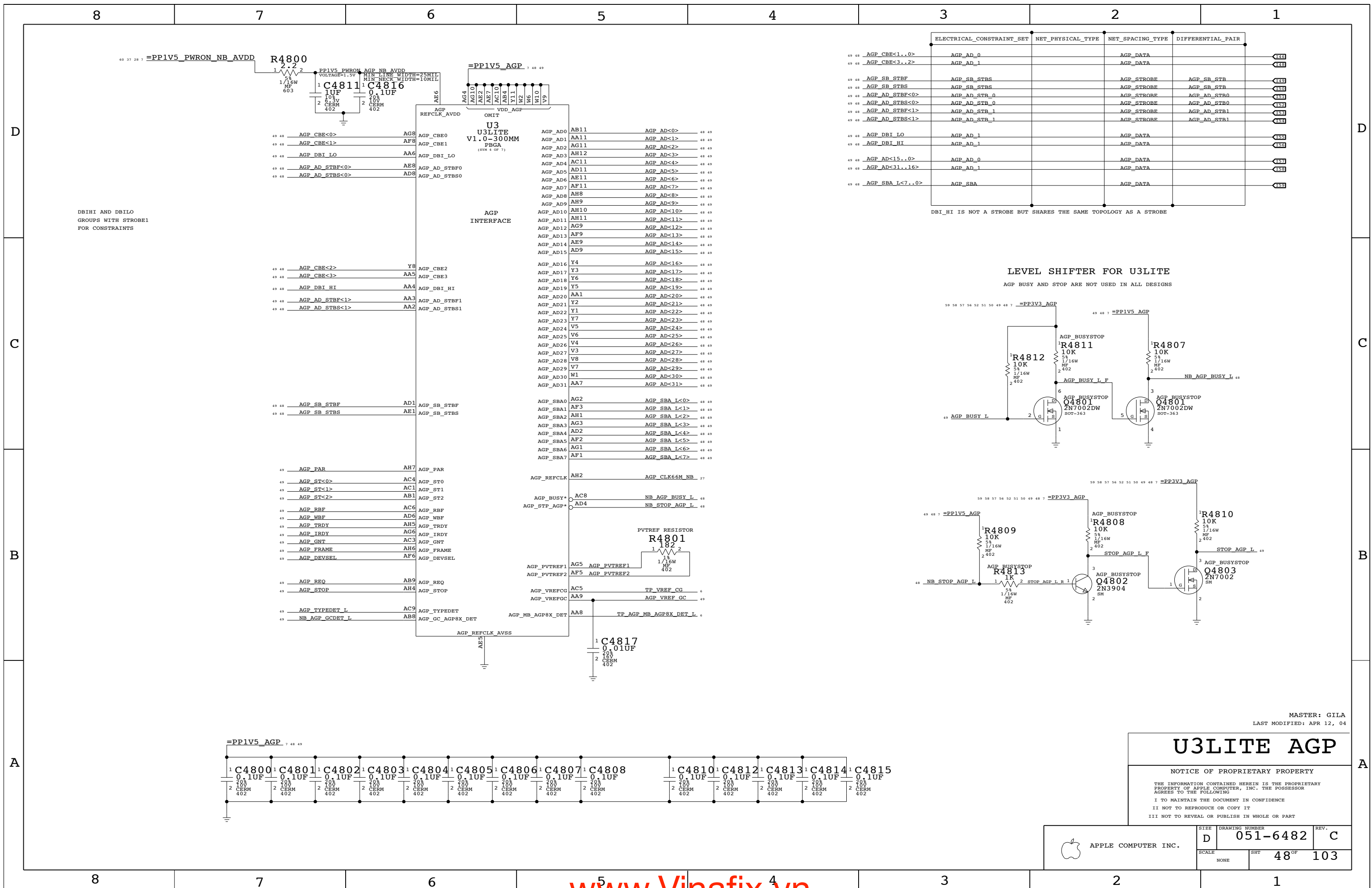
ONLY STUFF ONE VTT VREG



MEM TERM VREGS

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SCALE	SHT	46 OF	103
NONE			

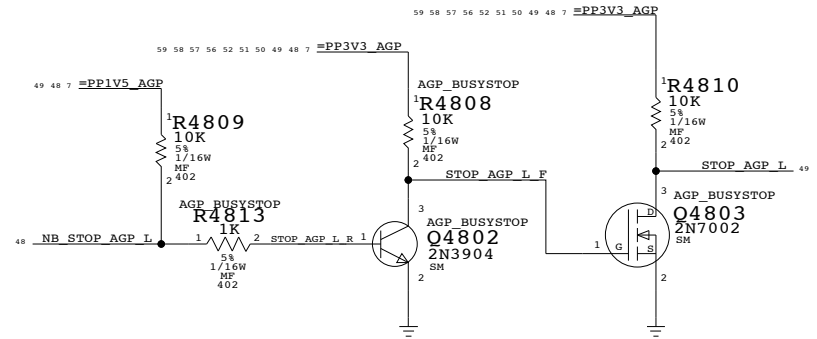
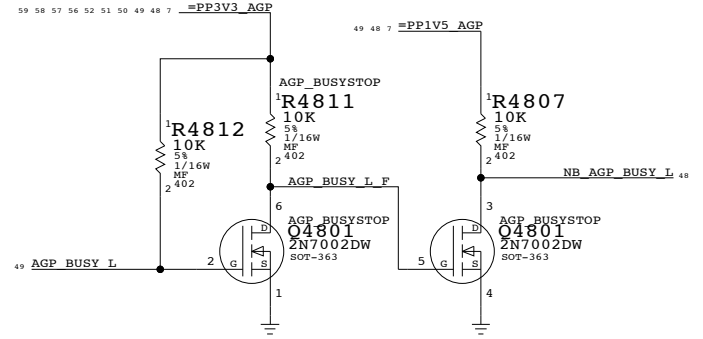


DBIHI AND DBILO GROUPS WITH STROBE1 FOR CONSTRAINTS

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
AGP_CBE<1..0>	AGP_AD_0	AGP_DATA	
AGP_CBE<3..2>	AGP_AD_1	AGP_DATA	
AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	AGP_SB_STR
AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	AGP_SB_STR
AGP_AD_STBF<0>	AGP_AD_STR_0	AGP_STROBE	AGP_AD_STR0
AGP_AD_STBS<0>	AGP_AD_STR_0	AGP_STROBE	AGP_AD_STR0
AGP_AD_STBF<1>	AGP_AD_STR_1	AGP_STROBE	AGP_AD_STR1
AGP_AD_STBS<1>	AGP_AD_STR_1	AGP_STROBE	AGP_AD_STR1
AGP_DBI_LO	AGP_AD_1	AGP_DATA	
AGP_DBI_HI	AGP_AD_1	AGP_DATA	
AGP_AD<15..0>	AGP_AD_0	AGP_DATA	
AGP_AD<31..16>	AGP_AD_1	AGP_DATA	
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA	

DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

LEVEL SHIFTER FOR U3LITE
AGP BUSY AND STOP ARE NOT USED IN ALL DESIGNS



AGP REFCLK_AVDD	AGP_CBE0	AGP_CBE1	AGP_DBI_LO	AGP_AD_STBF0	AGP_AD_STBS0	AGP_CBE2	AGP_CBE3	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE4	AGP_CBE5	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE6	AGP_CBE7	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE8	AGP_CBE9	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE10	AGP_CBE11	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE12	AGP_CBE13	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE14	AGP_CBE15	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE16	AGP_CBE17	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE18	AGP_CBE19	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE20	AGP_CBE21	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE22	AGP_CBE23	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE24	AGP_CBE25	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE26	AGP_CBE27	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE28	AGP_CBE29	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE30	AGP_CBE31	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE32	AGP_CBE33	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE34	AGP_CBE35	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE36	AGP_CBE37	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE38	AGP_CBE39	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE40	AGP_CBE41	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE42	AGP_CBE43	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE44	AGP_CBE45	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE46	AGP_CBE47	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE48	AGP_CBE49	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE50	AGP_CBE51	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE52	AGP_CBE53	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE54	AGP_CBE55	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE56	AGP_CBE57	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE58	AGP_CBE59	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE60	AGP_CBE61	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE62	AGP_CBE63	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE64	AGP_CBE65	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE66	AGP_CBE67	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE68	AGP_CBE69	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE70	AGP_CBE71	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE72	AGP_CBE73	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE74	AGP_CBE75	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE76	AGP_CBE77	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE78	AGP_CBE79	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE80	AGP_CBE81	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE82	AGP_CBE83	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE84	AGP_CBE85	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE86	AGP_CBE87	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE88	AGP_CBE89	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE90	AGP_CBE91	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE92	AGP_CBE93	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE94	AGP_CBE95	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE96	AGP_CBE97	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1	AGP_CBE98	AGP_CBE99	AGP_DBI_HI	AGP_AD_STBF1	AGP_AD_STBS1
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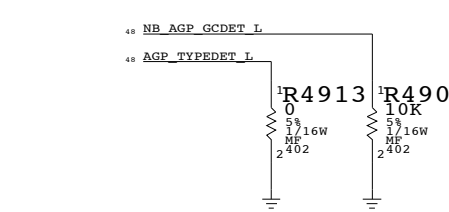
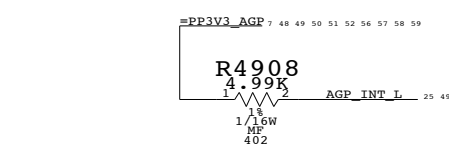
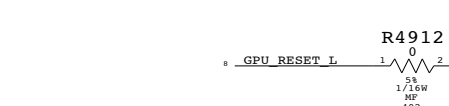
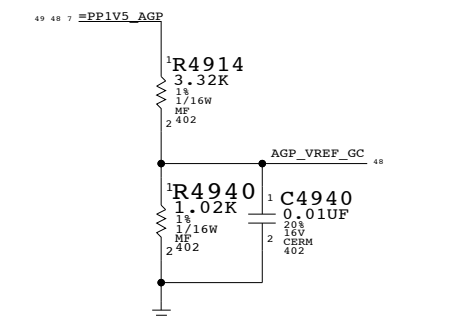
U3LITE AGP

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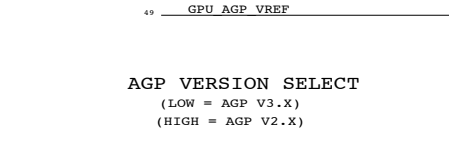
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	48 OF 103	
NONE			

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0176	1	IC,NV18B,GRAPHIC CTRL,C1	U4900	NV18B
338S0175	1	IC,NV34,GRAPHIC CTRL,B1	U4900	NV34

U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)



DOES HOOP UP AGP_BUSY_L & STOP_AGP_L TO 3.3V OR 1.5V?



Pin	Signal	Reference Designator	Function
48	AGP_AD<0>	AJ28	PCIAD0
48	AGP_AD<1>	AK28	PCIAD1
48	AGP_AD<2>	AH27	PCIAD2
48	AGP_AD<3>	AK27	PCIAD3
48	AGP_AD<4>	AJ27	PCIAD4
48	AGP_AD<5>	AH26	PCIAD5
48	AGP_AD<6>	AJ26	PCIAD6
48	AGP_AD<7>	AH25	PCIAD7
48	AGP_AD<8>	AH23	PCIAD8
48	AGP_AD<9>	AJ23	PCIAD9
48	AGP_AD<10>	AH22	PCIAD10
48	AGP_AD<11>	AJ22	PCIAD11
48	AGP_AD<12>	AJ21	PCIAD12
48	AGP_AD<13>	AK21	PCIAD13
48	AGP_AD<14>	AH20	PCIAD14
48	AGP_AD<15>	AJ20	PCIAD15
48	AGP_AD<16>	AG26	PCIAD16
48	AGP_AD<17>	AE24	PCIAD17
48	AGP_AD<18>	AG25	PCIAD18
48	AGP_AD<19>	AG24	PCIAD19
48	AGP_AD<20>	AF24	PCIAD20
48	AGP_AD<21>	AG23	PCIAD21
48	AGP_AD<22>	AE22	PCIAD22
48	AGP_AD<23>	AF22	PCIAD23
48	AGP_AD<24>	AE21	PCIAD24
48	AGP_AD<25>	AG20	PCIAD25
48	AGP_AD<26>	AG19	PCIAD26
48	AGP_AD<27>	AF19	PCIAD27
48	AGP_AD<28>	AE19	PCIAD28
48	AGP_AD<29>	AF18	PCIAD29
48	AGP_AD<30>	AG18	PCIAD30
48	AGP_AD<31>	AE18	PCIAD31

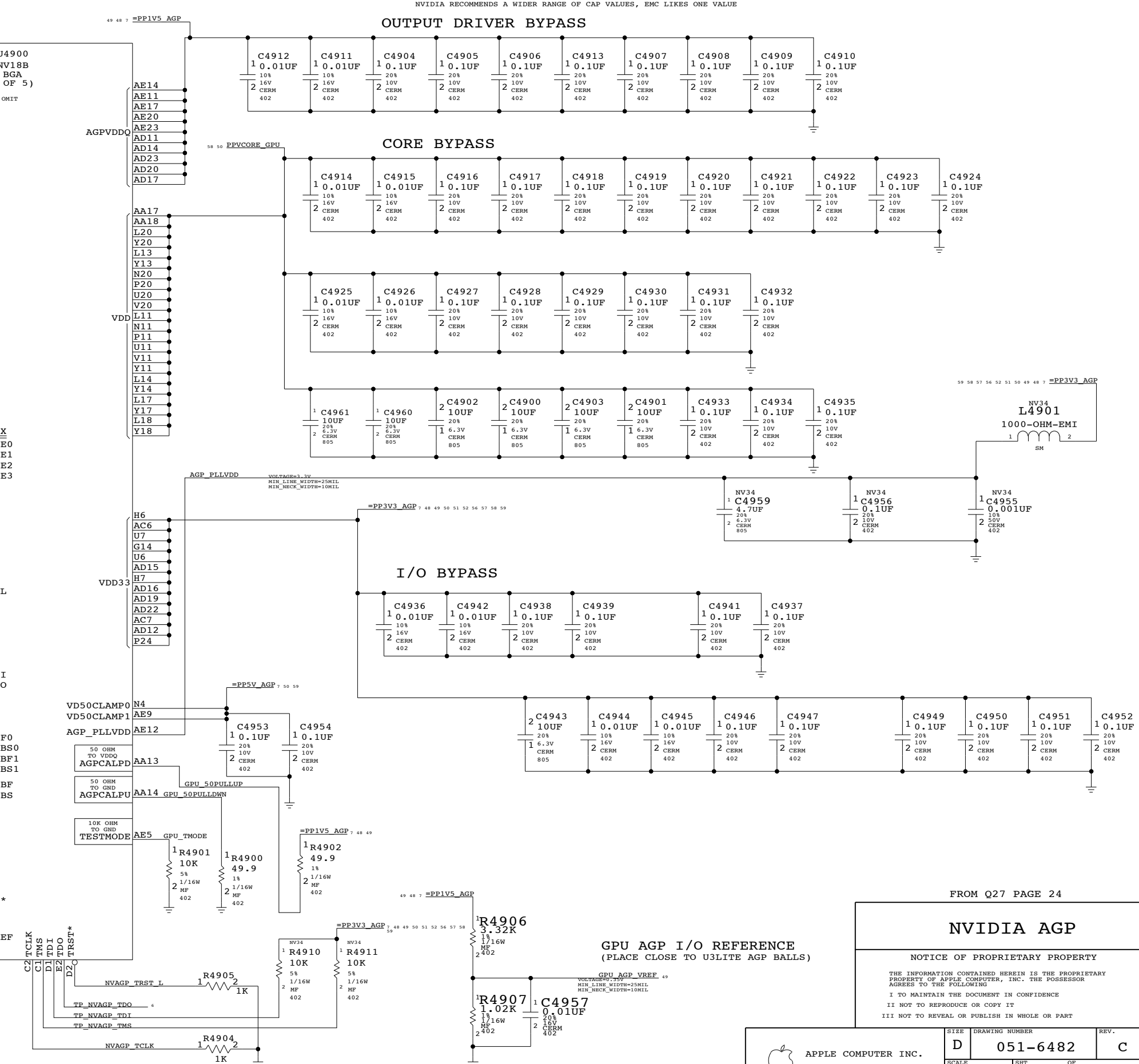
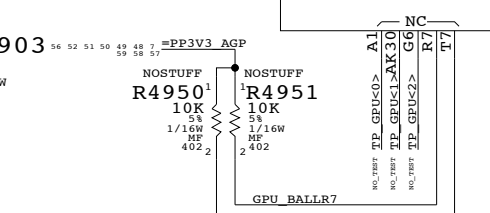
Pin	Signal	Reference Designator	Function
48	AGP_CBE<0>	AJ24	PCIC0/BE0*
48	AGP_CBE<1>	AH19	PCIC1/BE1*
48	AGP_CBE<2>	AF25	PCIC2/BE2*
48	AGP_CBE<3>	AG22	PCIC3/BE3*

Pin	Signal	Reference Designator	Function
27	AGP_CLK66M GPU	AG12	PCICLK : CLK
48	AGP_REQ	AF15	PCIRST* : RST*
48	AGP_GNT	AE15	PCIGNT* : GNT
48	AGP_REQ	AF13	PCIREQ* : REQ
48	AGP_FRAME	AK16	PCIFRAME* : FRAME
48	AGP_IRDY	AG16	PCIIRDY* : IRDY
48	AGP_TRDY	AJ17	PCITRDY* : TRDY
48	AGP_DEVSEL	AJ16	PCIDEVSEL* : DEVSEL
48	AGP_STOP	AH17	PCISTOP* : STOP
48	AGP_PAR	AK18	PCIPAR : PAR

Pin	Signal	Reference Designator	Function
25	AGP_INT_L	AG15	PCIINTA* : INTA
6	TP_GPU_INTB_L	AE10	NC_PCIINTB* : INTB
48	AGP_RBF	AG14	AGPRBF* : RBF
48	AGP_WBF	AG17	AGPWBF* : WBF
48	AGP_DBI_HI	AJ18	AGPDBI* : DBI_HI
48	AGP_DBI_LO	AJ19	<RESRVD> : DBI_LO
48	AGP_ST<0>	AG13	AGPST0 : ST0
48	AGP_ST<1>	AE16	AGPST1 : ST1
48	AGP_ST<2>	AE13	AGPST2 : ST2

Pin	Signal	Reference Designator	Function
48	AGP_AD_STBF<0>	AK24	AGPADSTBF0 : ADSTBF0
48	AGP_AD_STBS<0>	AJ25	AGPADSTBS0* : ADSTBS0
48	AGP_AD_STBF<1>	AG21	AGPADSTBF1 : ADSTBF1
48	AGP_AD_STBS<1>	AF21	AGPADSTBS1* : ADSTBS1
48	AGP_SB_STBF	AK13	AGPSBSTBF : SBSTBF
48	AGP_SB_STBS	AJ13	AGPSBSTBS* : SBSTBS
48	AGP_SBA_L<0>	AJ11	AGPSBA0 : SBA0*
48	AGP_SBA_L<1>	AH11	AGPSBA1 : SBA1*
48	AGP_SBA_L<2>	AJ12	AGPSBA2 : SBA2*
48	AGP_SBA_L<3>	AH12	AGPSBA3 : SBA3*
48	AGP_SBA_L<4>	AJ14	AGPSBA4 : SBA4*
48	AGP_SBA_L<5>	AH14	AGPSBA5 : SBA5*
48	AGP_SBA_L<6>	AJ15	AGPSBA6 : SBA6*
48	AGP_SBA_L<7>	AH15	AGPSBA7 : SBA7*

Pin	Signal	Reference Designator	Function
48	GPU_MBDT_L	AF16	<RESRVD> : MBDT*
48	AGP_BUSY_L	AF12	AGPBUSY* : BUSY*
48	STOP_AGP_L	AG11	AGPSTOP* : STOP*
48	GPU_VREF	AK29	AGPVREF : AGPVREF



AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

GPU AGP I/O REFERENCE
(PLACE CLOSE TO U3LITE AGP BALLS)

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NVIDIA AGP

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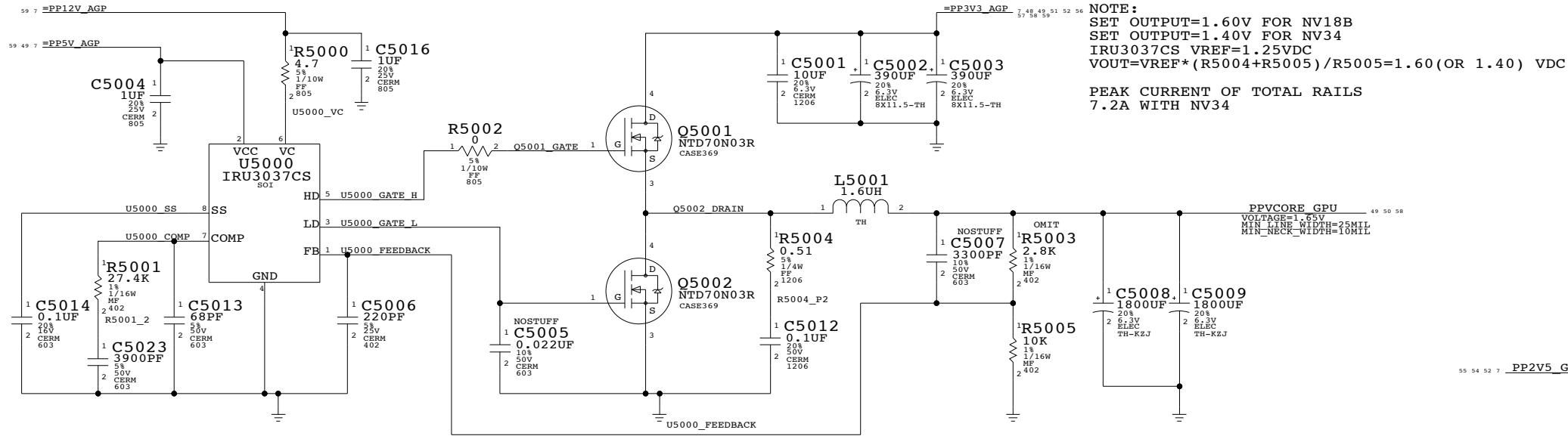
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NONE	49	103

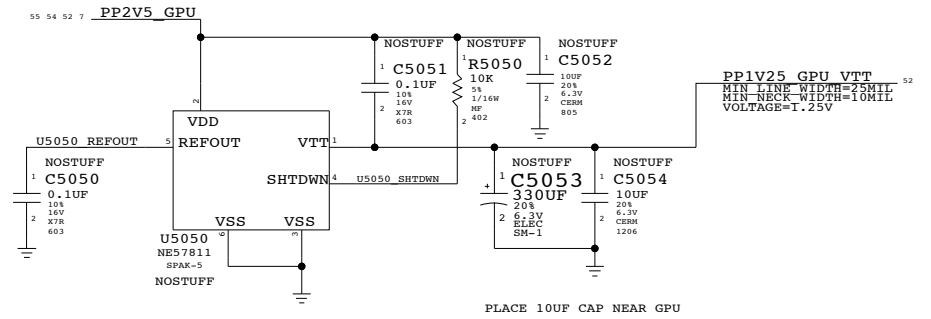
GPU VCORE VREG

PPVCORE_GPU	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1.60VDC	11482803	1	RES,2.8K OHM,1/16W,1%,0402	R5003	NV18B
1.40VDC	11481213	1	RES,1.21K OHM,1/16W,1%,0402	R5003	NV34



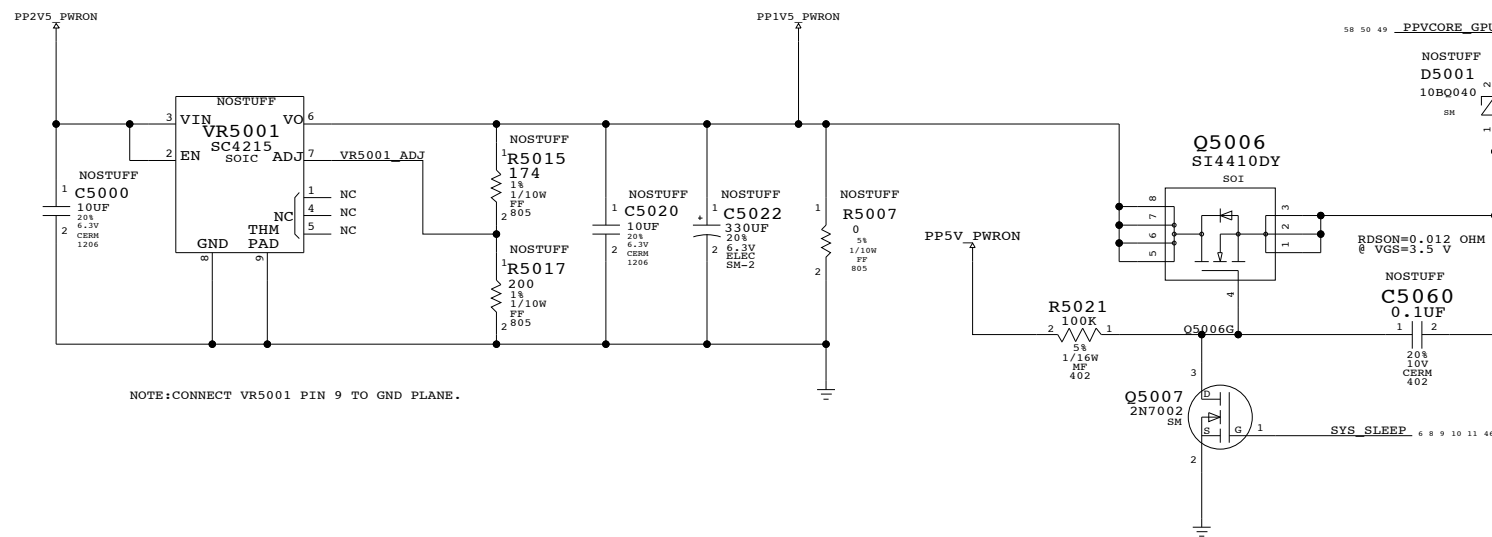
NOTE:
 SET OUTPUT=1.60V FOR NV18B
 SET OUTPUT=1.40V FOR NV34
 IRU3037CS VREF=1.25VDC
 $VOUT=VREF*(R5004+R5005)/R5005=1.60(OR\ 1.40)\ VDC$
 PEAK CURRENT OF TOTAL RAILS
 7.2A WITH NV34

GPU VTT VREG



PLACE 10UF CAP NEAR GPU

AGP 1.5V VREG



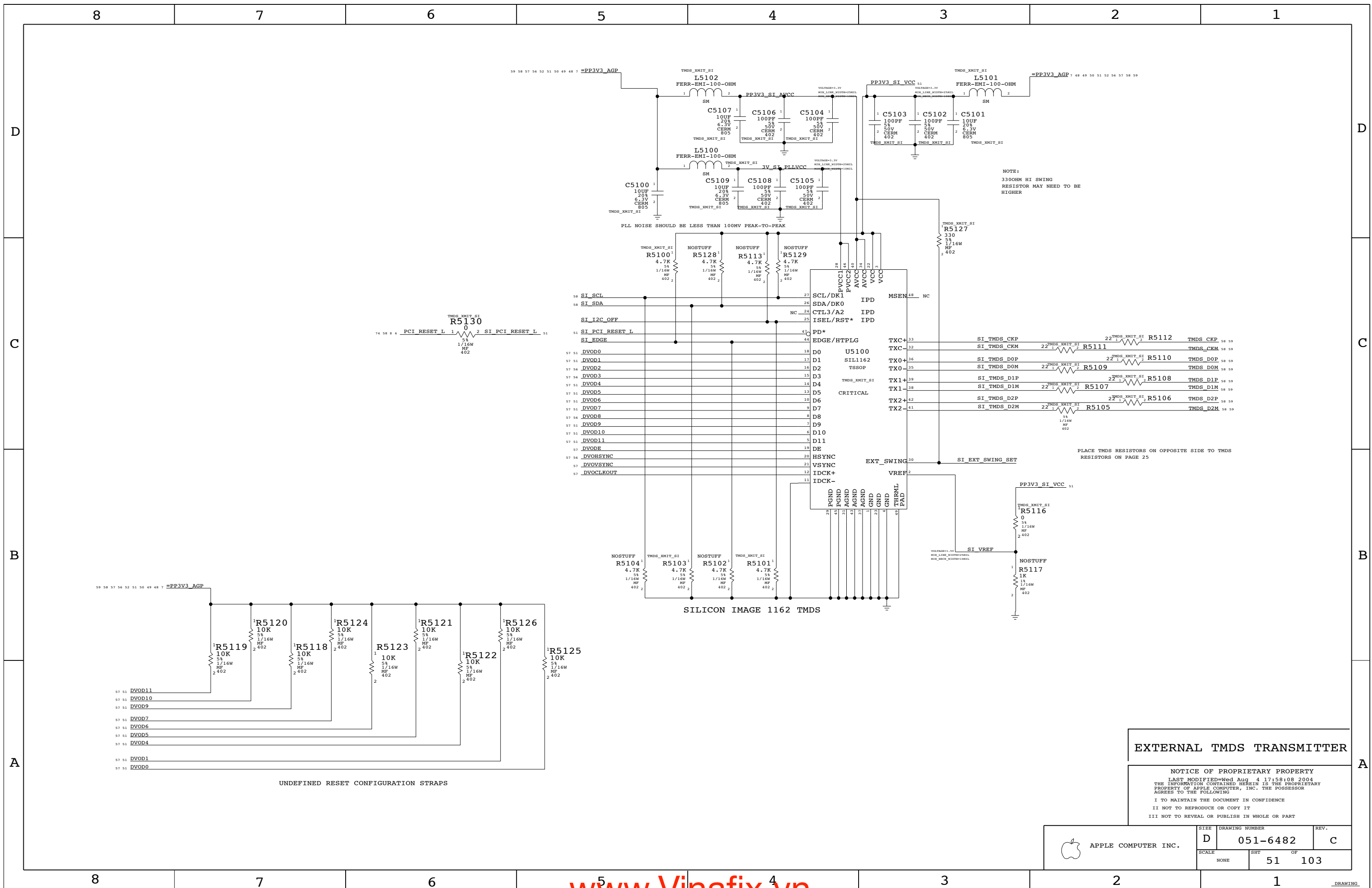
NOTE:CONNECT VR5001 PIN 9 TO GND PLANE.

NOTE:
 SET OUTPUT=1.5V
 SC4215 VREF=0.8VDC
 $VOUT=VREF*(R5015+R5017)/R5017=1.5\ VDC$
 PEAK CURRENT OF TOTAL RAILS
 0.95A

GRAPHICS VREGS

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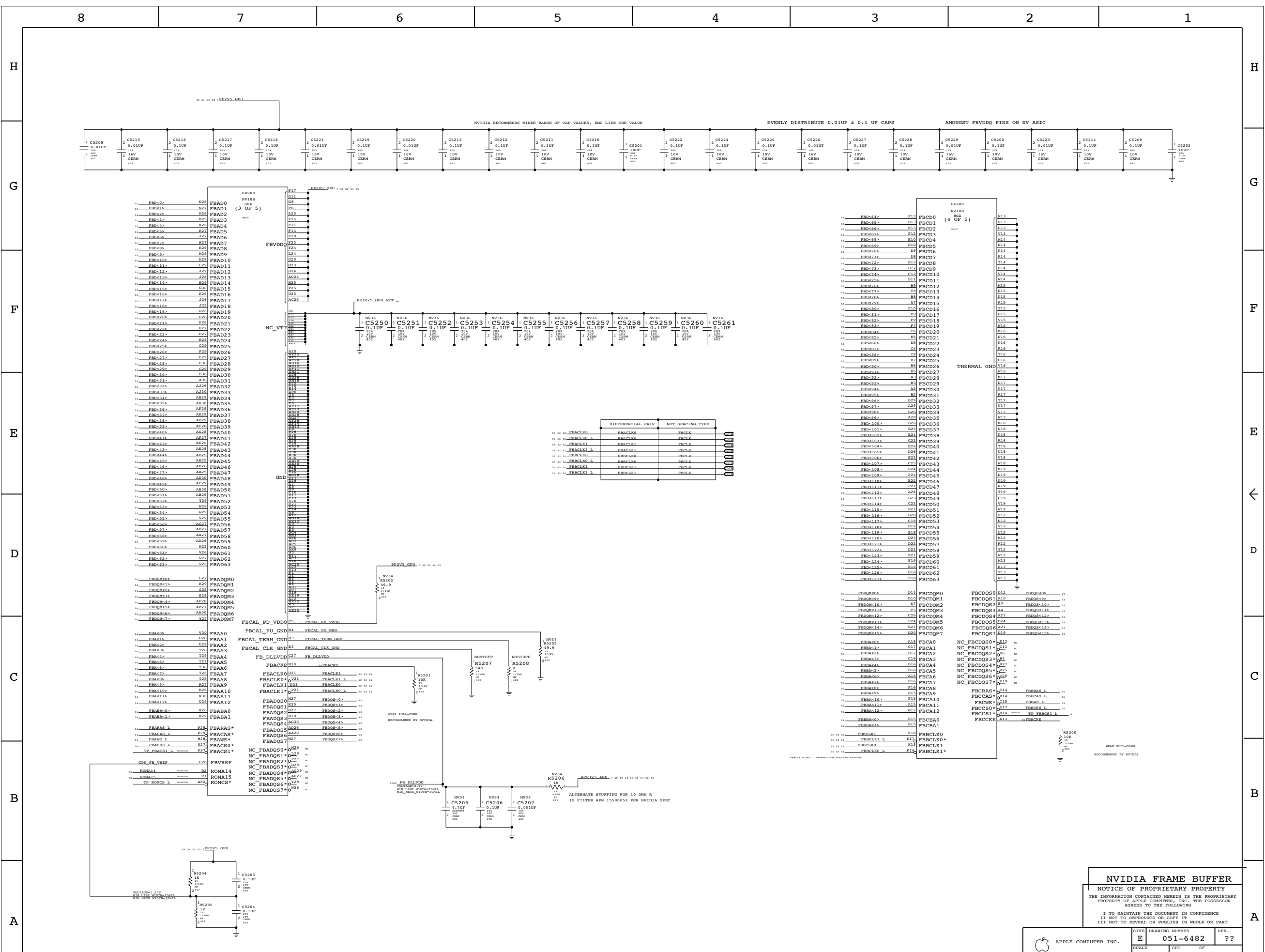
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SCALE	NONE	SHT	OF
		50	103



EXTERNAL TMSD TRANSMITTER

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		51	103



NVIDIA FRAME BUFFER

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SCALE	SHT	OF	
NONE	52	103	

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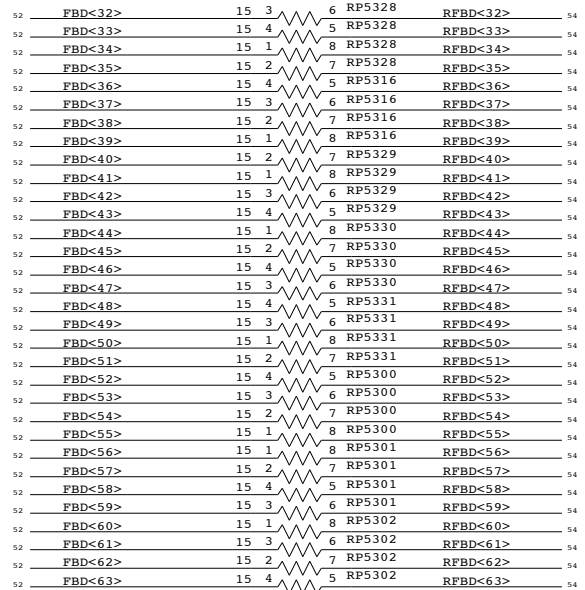
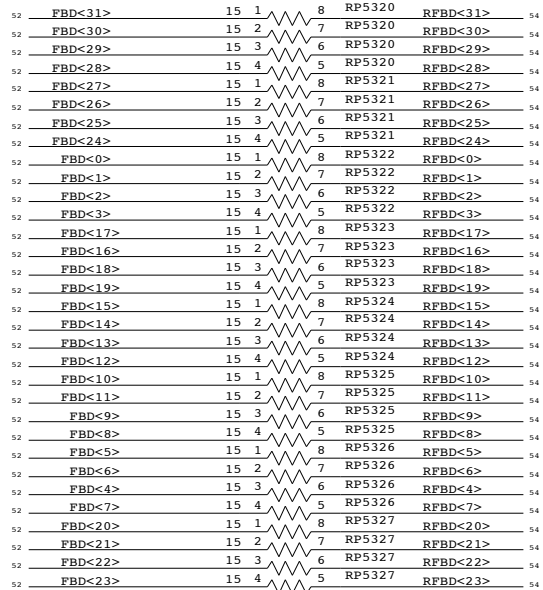
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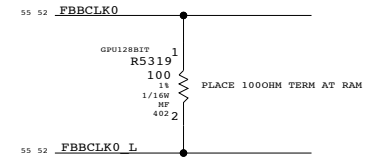
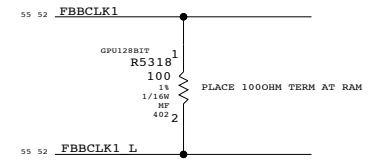
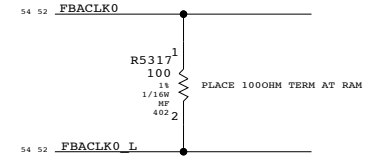
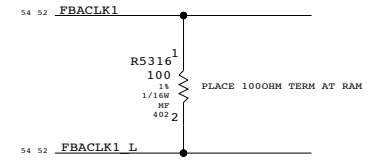
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PLACE R'S CLOSE TO MEMORY



PLACE R'S CLOSE TO GPU



D

D

C

C

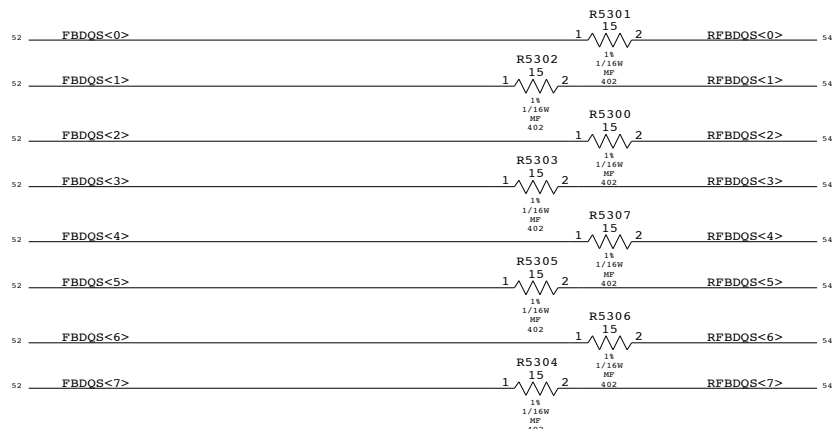
B

B

A

A

PLACE THESE R CLOSE TO SGRAM



PLACE THESE R CLOSE TO SGRAM



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FB TERMINATION

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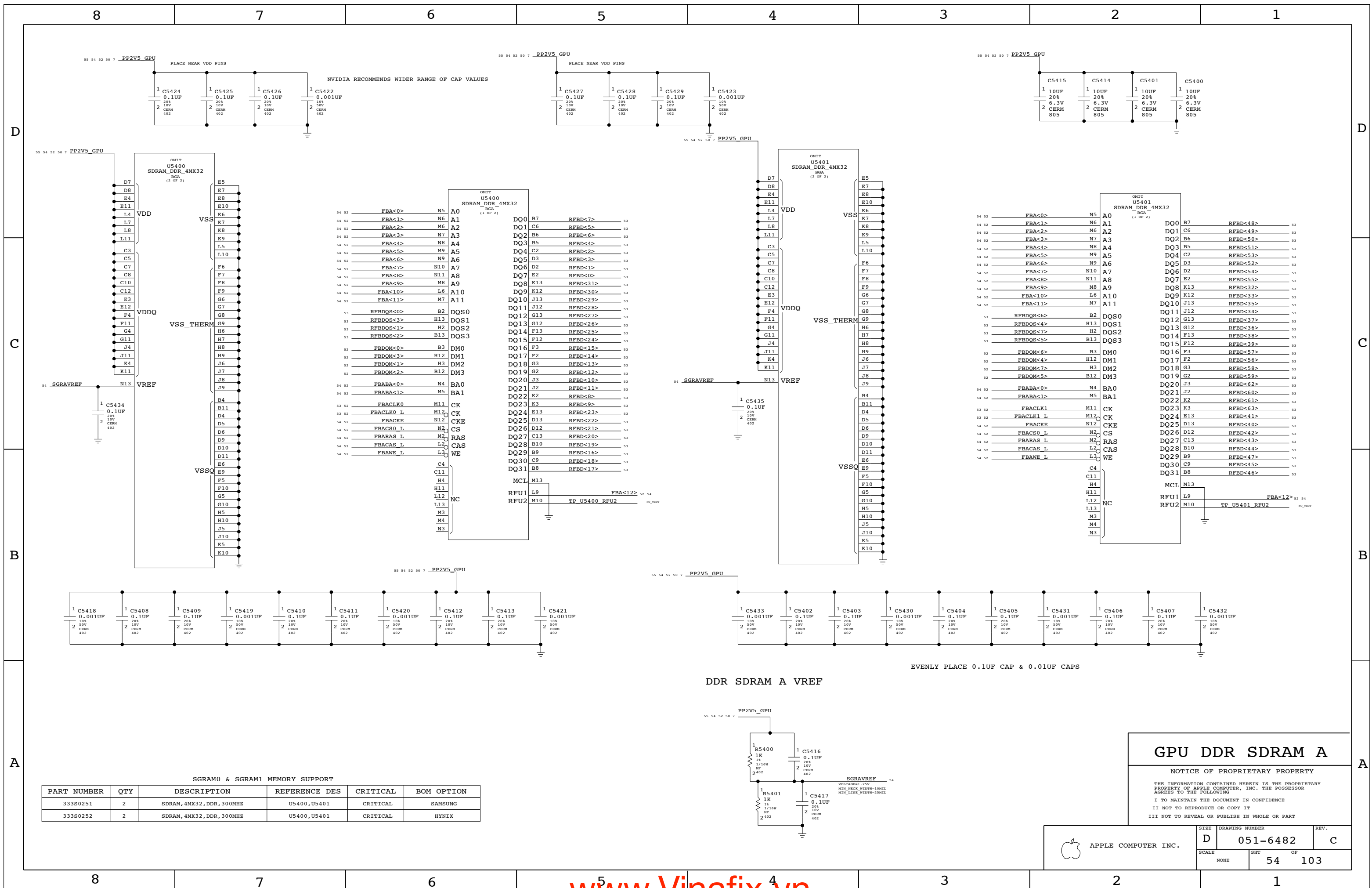
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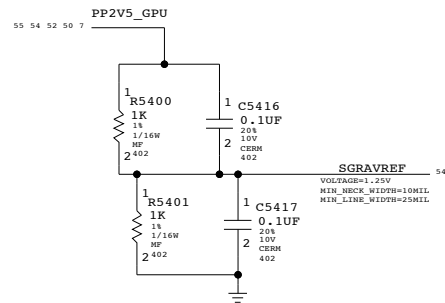
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	D	051-6482	C
SCALE	NONE	SHT OF	53 OF 103



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U5400, U5401	CRITICAL	SAMSUNG
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U5400, U5401	CRITICAL	HYNIX

DDR SDRAM A VREF



EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

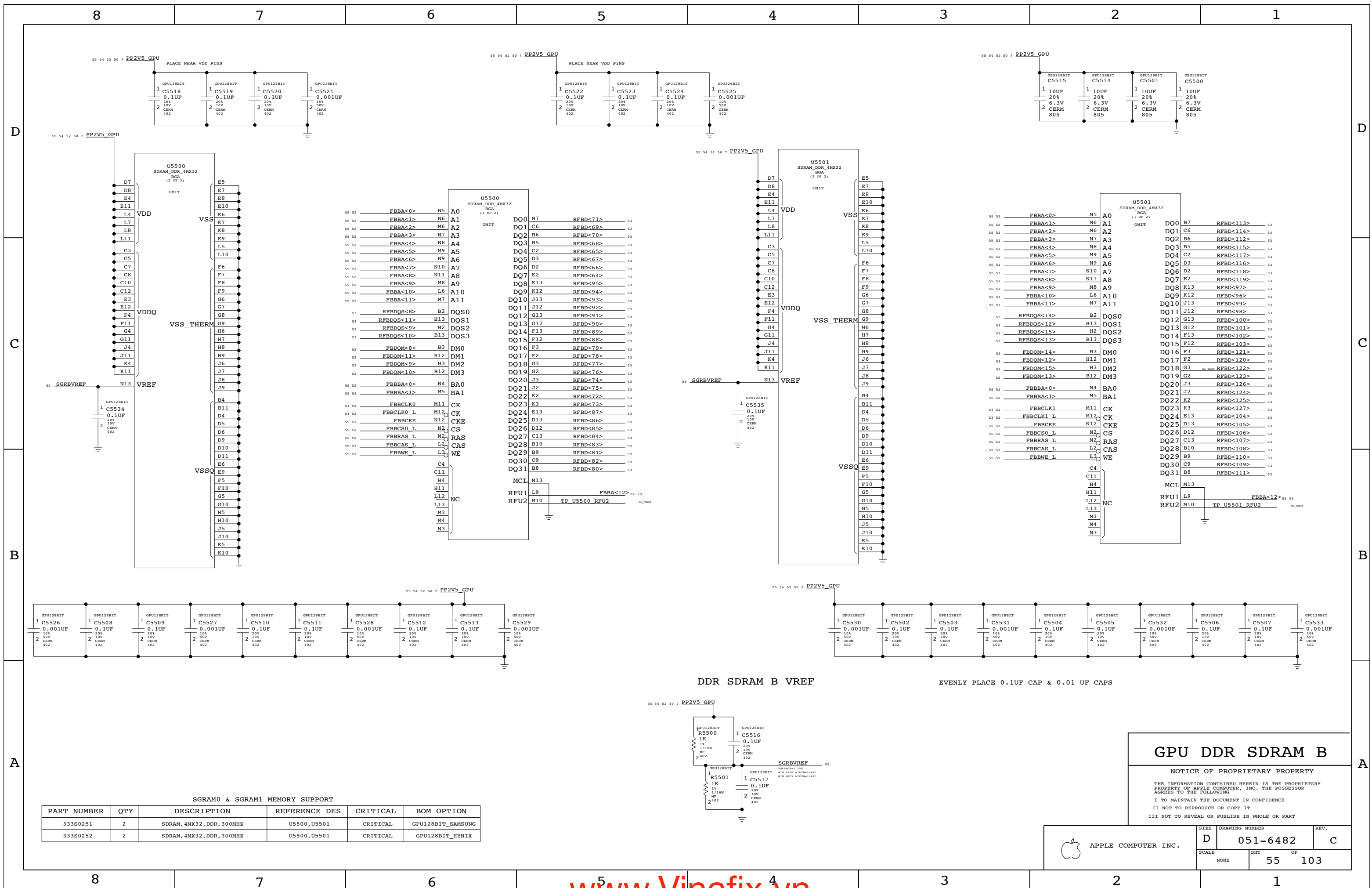
GPU DDR SDRAM A

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SCALE	SHT	OF	
NONE	54	103	



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33380251	2	SDRAM, 4MX32, DDR, 300MHZ	U5500, U5501	CRITICAL	GPU128BIT_SAMSUNG
33380252	2	SDRAM, 4MX32, DDR, 300MHZ	U5500, U5501	CRITICAL	GPU128BIT_HYNIX

GPU DDR SDRAM B

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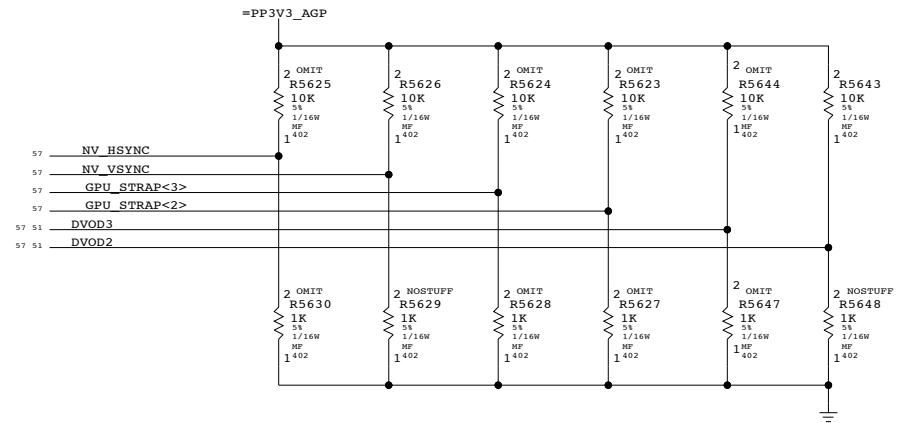
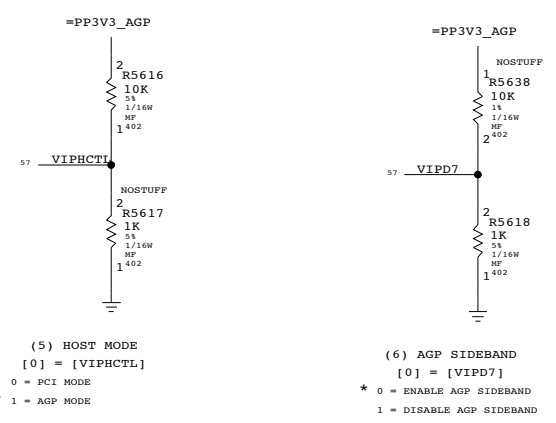
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHEET OF		
NONE	55		103

D

D

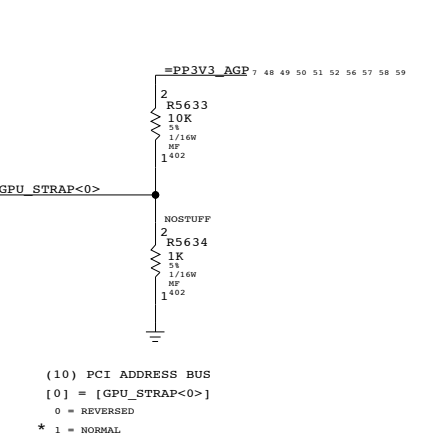
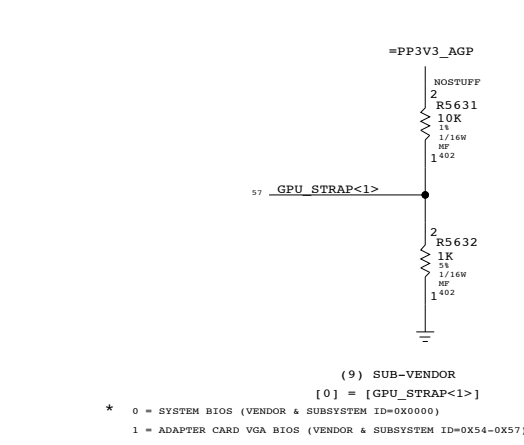
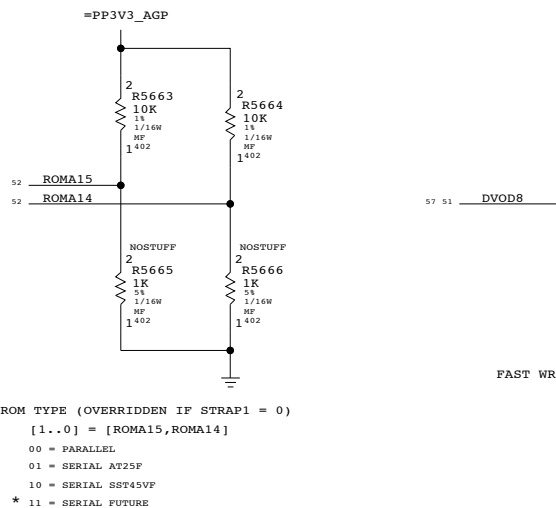


(8) FRAME BUFFER MEMORY SPEED
[5..0] = [NV11_HSYNC, NV11_VSYNC, GPU_STRAP<3>, GPU_STRAP<2>, DVOD3, DVOD2]

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
110111 = 270MHZ SAMSUNG (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5623		270MHZ_SAM_18
116S1104	1	RES,10K-OHM,1/16W,5%	R5644		270MHZ_SAM_18
116S1103	1	RES,1K-OHM,1/16W,5%	R5628		270MHZ_SAM_18
110011 = 270MHZ HYNIX (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5644		270MHZ_HYN_18
116S1103	2	RES,1K-OHM,1/16W,5%	R5628,R5627		270MHZ_HYN_18
111101 = 270MHZ SAMSUNG (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5624		270MHZ_SAM_34
116S1104	1	RES,10K-OHM,1/16W,5%	R5623		270MHZ_SAM_34
116S1103	1	RES,1K-OHM,1/16W,5%	R5647		270MHZ_SAM_34
111100 = 270MHZ HYNIX (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5624,R5623		270MHZ_HYN_34
116S1103	2	RES,1K-OHM,1/16W,5%	R5630,R5647		270MHZ_HYN_34

C

C



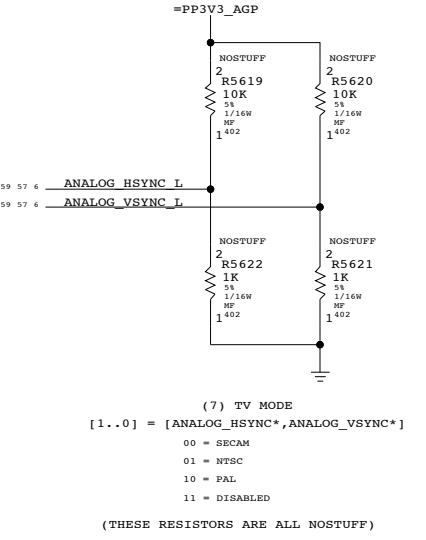
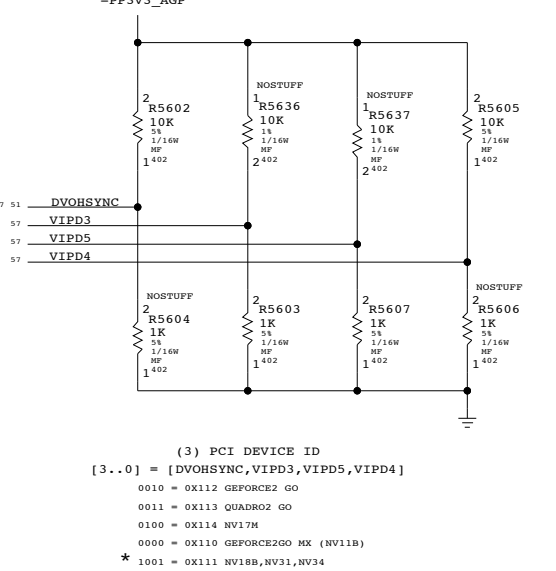
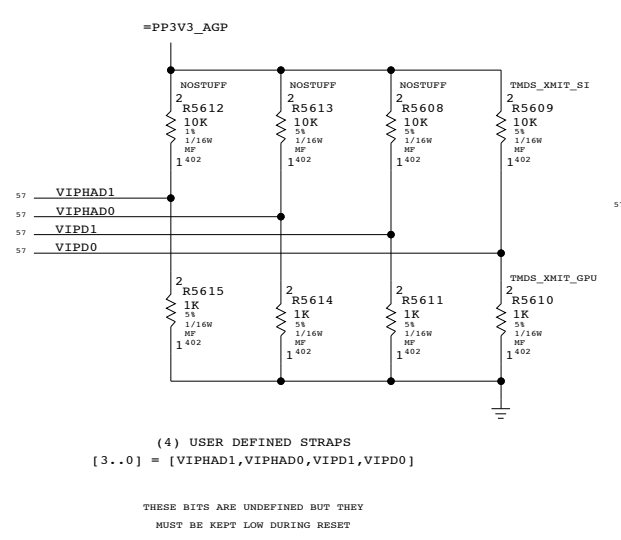
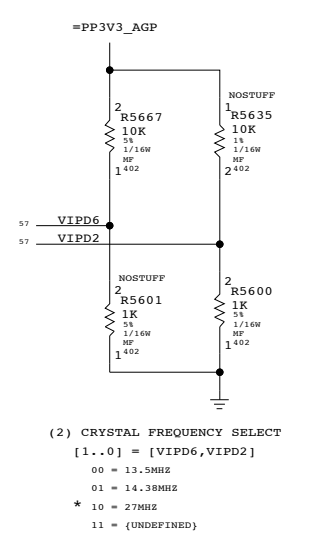
(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
[1..0] = [ROMA15,ROMA14]
00 = PARALLEL
01 = SERIAL AT25F
10 = SERIAL SST45VF
* 11 = SERIAL FUTURE

(9) SUB-VENDOR
[0] = [GPU_STRAP<1>]
* 0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)

(10) PCI ADDRESS BUS
[0] = [GPU_STRAP<0>]
0 = REVERSED
* 1 = NORMAL

B

B



(2) CRYSTAL FREQUENCY SELECT
[1..0] = [VIPD6,VIPD2]
00 = 13.5MHZ
01 = 14.3MHZ
* 10 = 27MHZ
11 = (UNDEFINED)

(4) USER DEFINED STRAPS
[3..0] = [VIPHAD1,VIPHAD0,VIPD1,VIPD0]
THESE BITS ARE UNDEFINED BUT THEY MUST BE KEPT LOW DURING RESET

(3) PCI DEVICE ID
[3..0] = [DVODHSYNC, VIPD3, VIPD5, VIPD4]
0010 = 0X112 GEFORCE2 GO
0011 = 0X113 QUADRO2 GO
0100 = 0X114 NV17M
0000 = 0X110 GEFORCE2GO MX (NV11B)
* 1001 = 0X111 NV18B,NV31,NV34

(7) TV MODE
[1..0] = [ANALOG_HSYNC*,ANALOG_VSYNC*]
00 = SECAM
01 = NTSC
10 = PAL
11 = DISABLED
(THESE RESISTORS ARE ALL NOSTUFF)

A

A

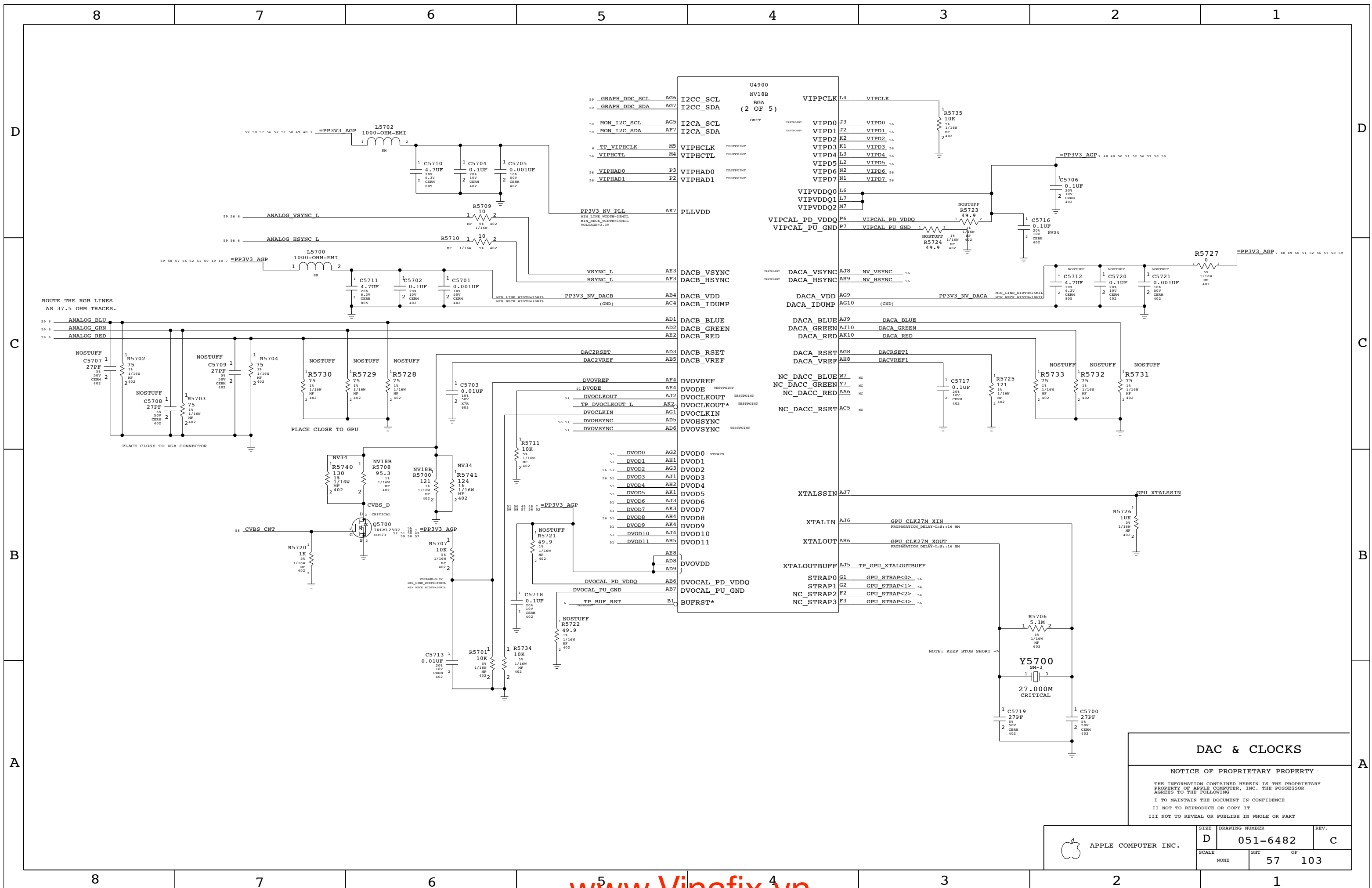
NVIDIA STRAPS

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SCALE	SHT	OF	
NONE	56	103	



DAC & CLOCKS

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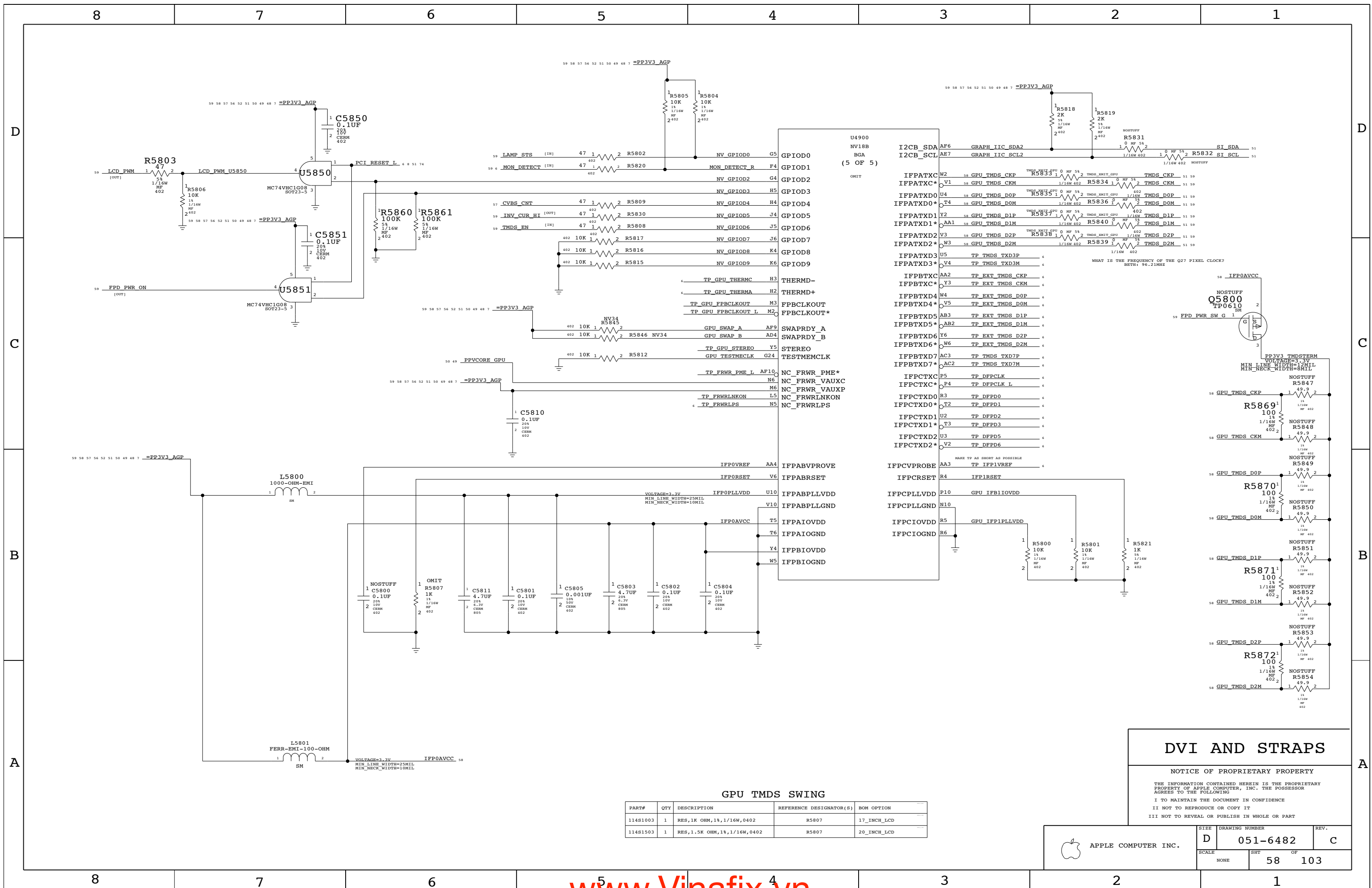
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	SCALE NONE	SHEET 57	OF 103



DVI AND STRAPS

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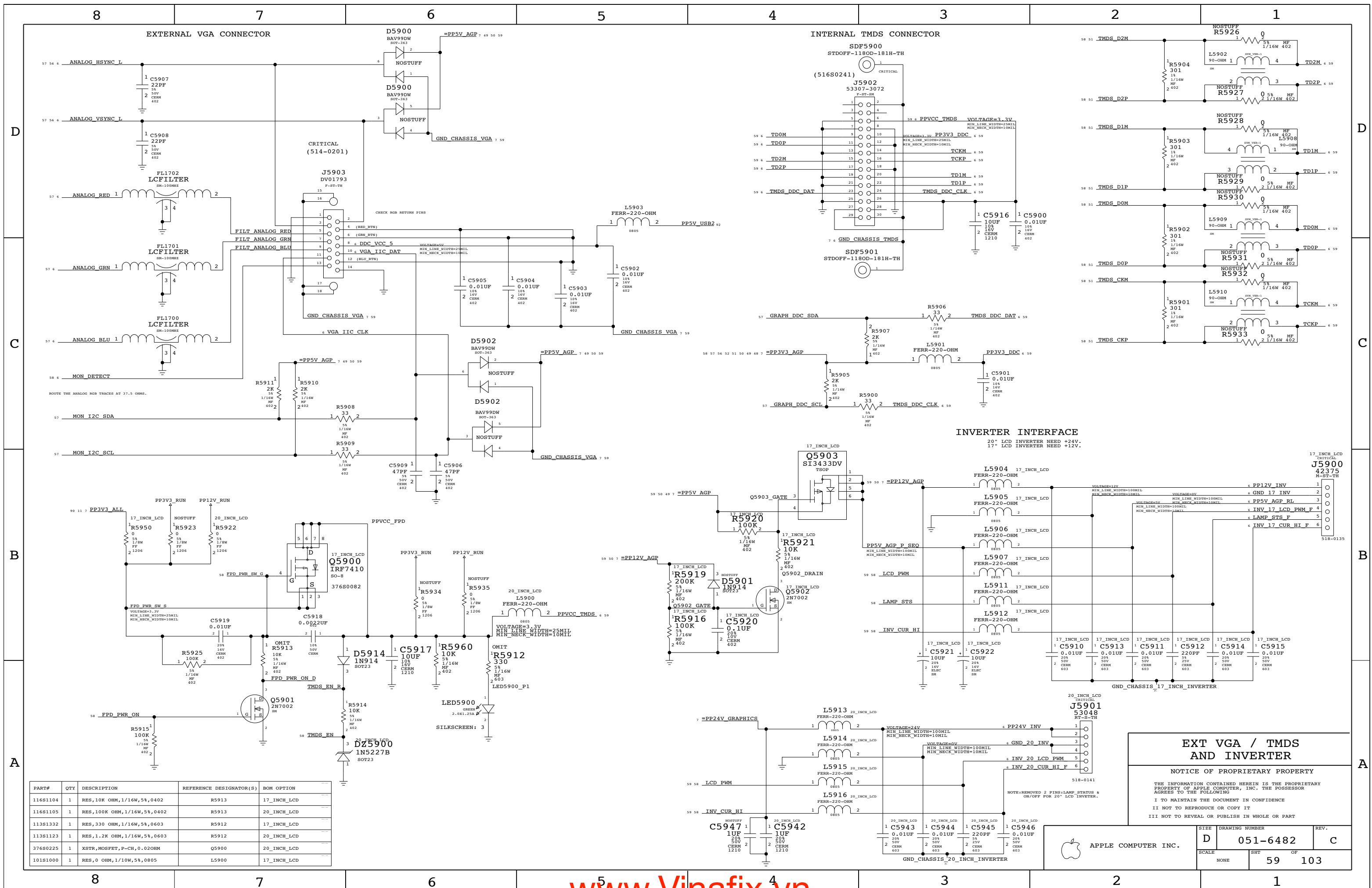
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	SCALE NONE	SHT 58	OF 103



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOH OPTION
116S1104	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S1105	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
113S1332	1	RES,330 OHM,1/16W,5%,0603	R5912	17_INCH_LCD
113S1123	1	RES,1.2K OHM,1/16W,5%,0603	R5912	20_INCH_LCD
376S0225	1	XSTR,MOSFET,P-CH,0.020OHM	Q5900	20_INCH_LCD
101S1000	1	RES,0 OHM,1/10W,5%,0805	L5900	17_INCH_LCD

EXT VGA / TMD5 AND INVERTER

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APPLE COMPUTER INC.

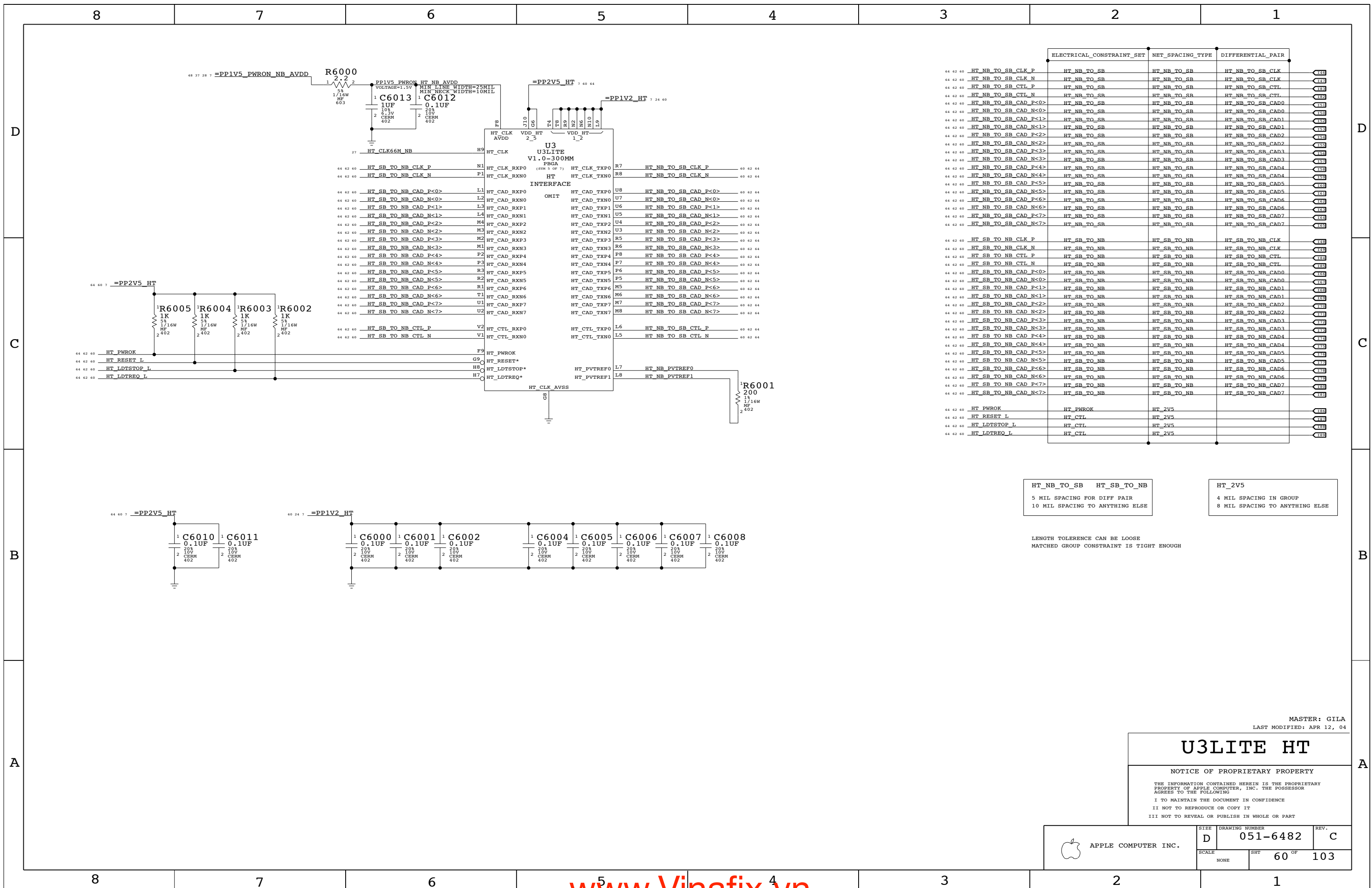
SIZE: D

DRAWING NUMBER: 051-6482

REV. C

SCALE: NONE

SHEET: 59 OF 103



	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
64 62 60	HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK
64 62 60	HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK
64 62 60	HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL
64 62 60	HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL
64 62 60	HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0
64 62 60	HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0
64 62 60	HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1
64 62 60	HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1
64 62 60	HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2
64 62 60	HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2
64 62 60	HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3
64 62 60	HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3
64 62 60	HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4
64 62 60	HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4
64 62 60	HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5
64 62 60	HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5
64 62 60	HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6
64 62 60	HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6
64 62 60	HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7
64 62 60	HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7
64 62 60	HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK
64 62 60	HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK
64 62 60	HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL
64 62 60	HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL
64 62 60	HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0
64 62 60	HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0
64 62 60	HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1
64 62 60	HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1
64 62 60	HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2
64 62 60	HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2
64 62 60	HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3
64 62 60	HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3
64 62 60	HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4
64 62 60	HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4
64 62 60	HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5
64 62 60	HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5
64 62 60	HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6
64 62 60	HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6
64 62 60	HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7
64 62 60	HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7
64 62 60	HT_PWROK	HT_PWROK	HT_2V5	
64 62 60	HT_RESET_L	HT_CTL	HT_2V5	
64 62 60	HT_LDTSTOP_L	HT_CTL	HT_2V5	
64 62 60	HT_LDTREQ_L	HT_CTL	HT_2V5	

HT_NB_TO_SB HT_SB_TO_NB
 5 MIL SPACING FOR DIFF PAIR
 10 MIL SPACING TO ANYTHING ELSE

HT_2V5
 4 MIL SPACING IN GROUP
 8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERANCE CAN BE LOOSE
 MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: GILA
 LAST MODIFIED: APR 12, 04

U3LITE HT

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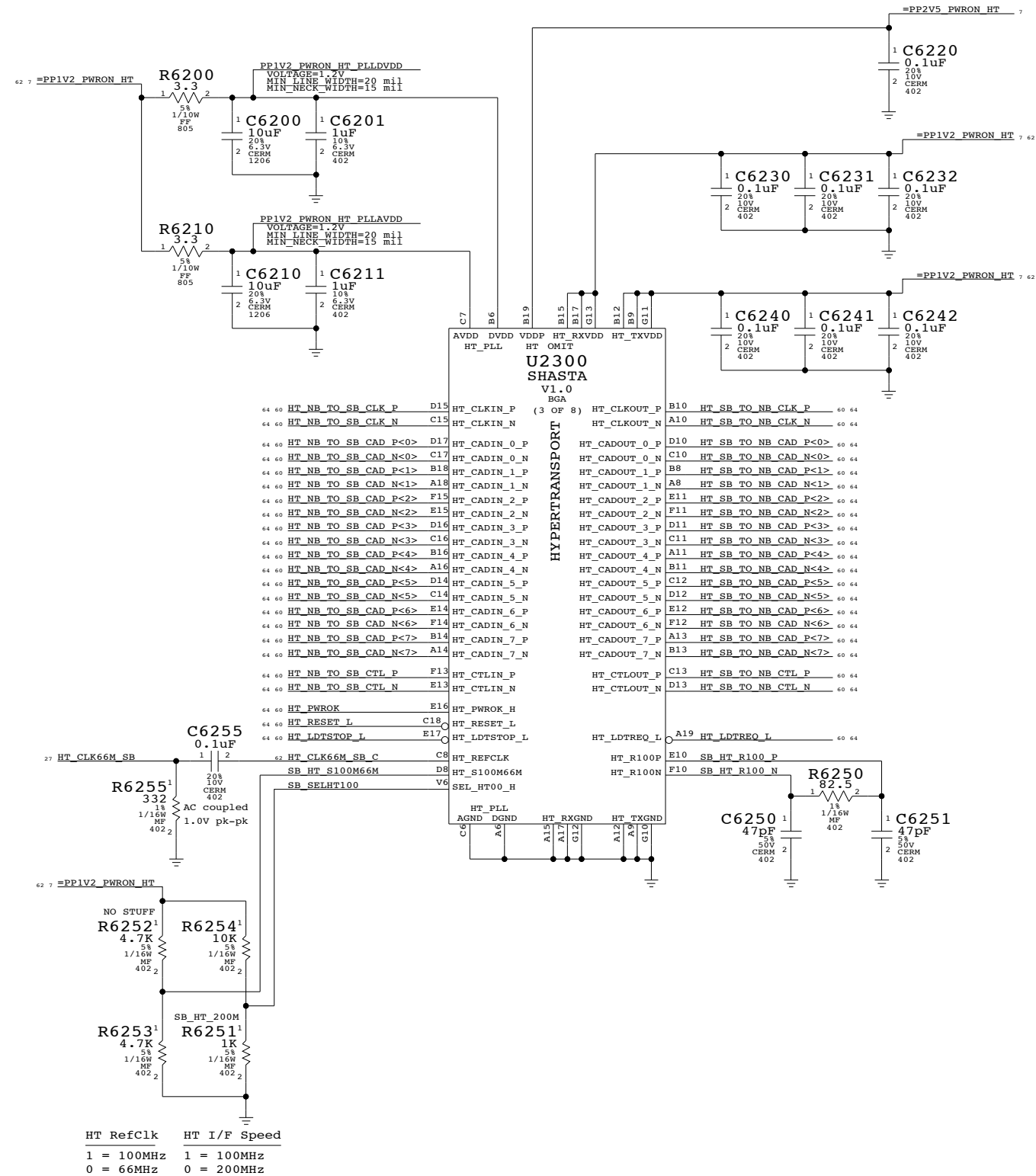
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	60 OF	103
NONE			

Page Notes

Power aliases required by this page:
 - _PP2V5_PWRON_HT
 - _PP1V2_PWRON_HT

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - SB_HT_200M
 Stuffs resistor to select 200MHz HT I/F.



Master: Link

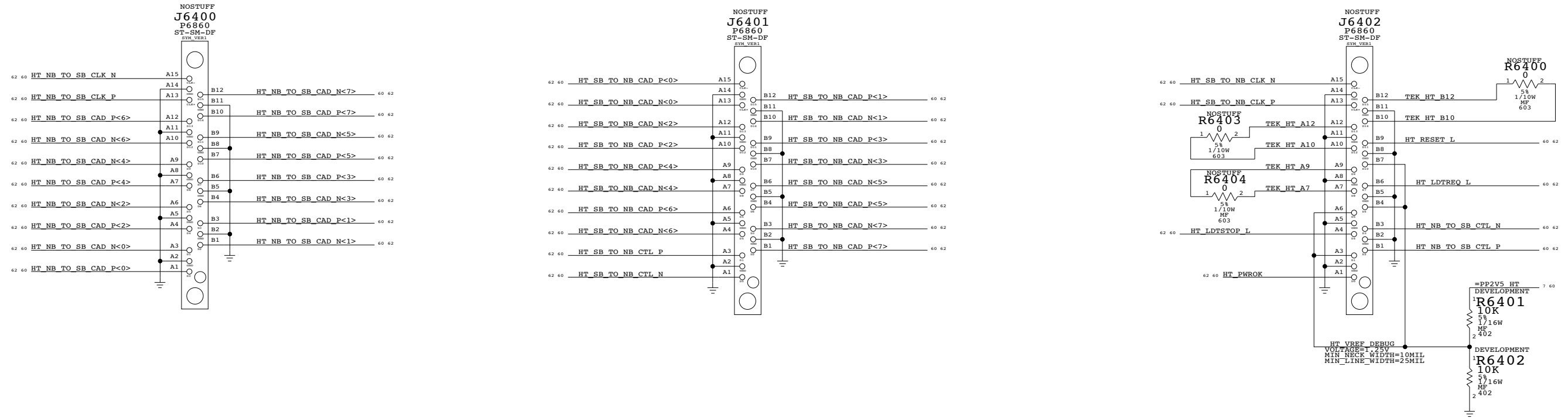
Shasta HyperTransport

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	D	051-6482	C
SCALE	SHT	OF	
NONE	62	103	

SAME CONNECTORS & PINOUT AS
Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2



MASTER: GILA
LAST MODIFIED: APR 12, 04

HT DEBUG CONN

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHT 64 OF 103	

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C

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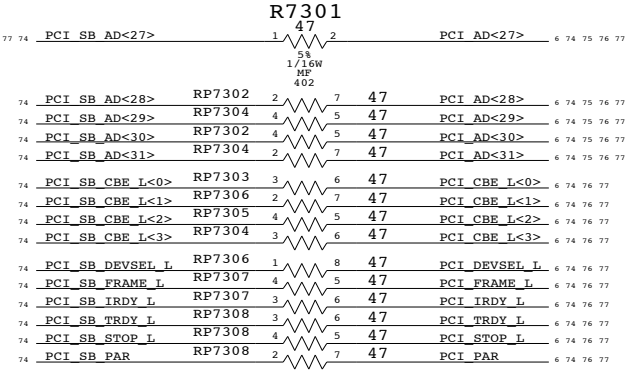
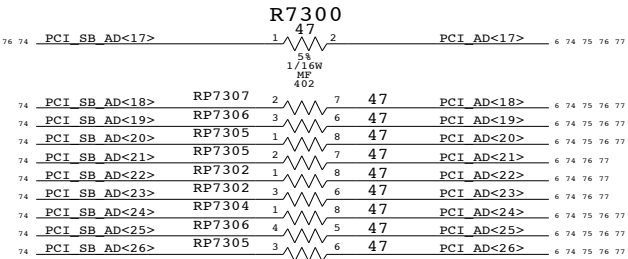
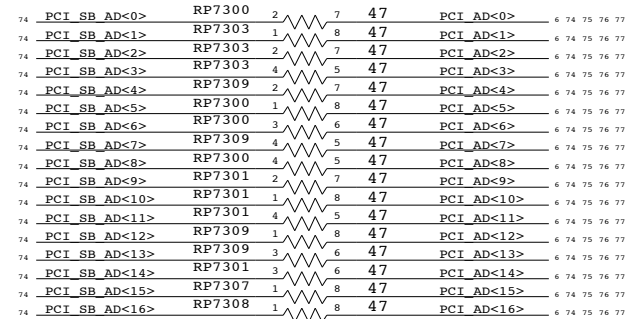
B

A

A

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)



PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	73 OF 103	
NONE			

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7

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1

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
PCI_AD			PCI_AD<31..28>	6 73 75 76 77
PCI_AD27			PCI_AD<27>	6 73 75 76 77
PCI_AD			PCI_AD<26..24>	6 73 75 76 77
PCI_AD23			PCI_AD<23>	6 73 76 77
PCI_AD22			PCI_AD<22>	6 73 76 77
PCI_AD21			PCI_AD<21>	6 73 76 77
PCI_AD20			PCI_AD<20>	6 73 75 76 77
PCI_AD			PCI_AD<19..18>	6 73 75 76 77
PCI_AD17			PCI_AD<17>	6 73 75 76 77
PCI_AD			PCI_AD<16..0>	6 73 75 76 77
PCI			PCI_CBE_L<3..0>	6 73 76 77
PCI			PCI_PAR	6 73 76 77
PCI_CTL			PCI_DEVSEL_L	6 73 74 76 77
PCI_CTL			PCI_FRAME_L	6 73 74 76 77
PCI_CTL			PCI_IRDY_L	6 73 74 76 77
PCI_CTL			PCI_TRDY_L	6 73 74 76 77
PCI_CTL			PCI_STOP_L	6 73 74 76 77

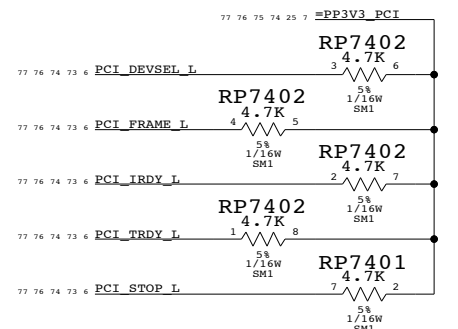
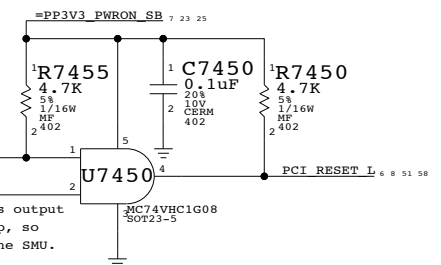
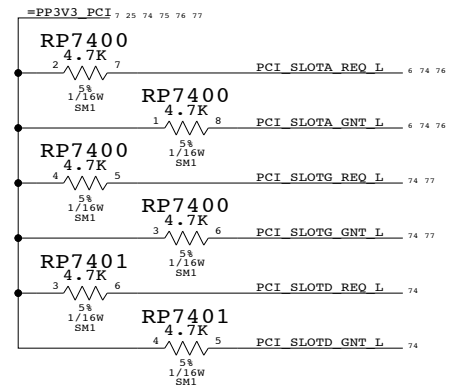
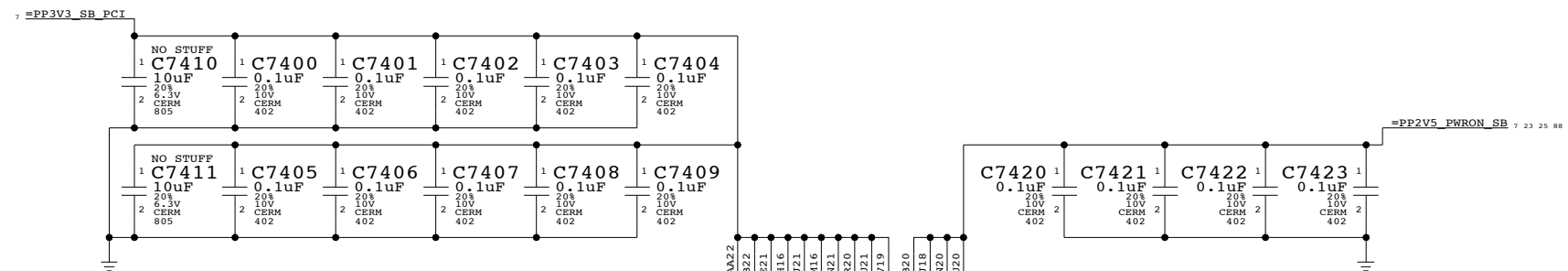
Page Notes

Power aliases required by this page:
 - _PP3V3_PCI
 - _PP3V3_SB_PCI (can be _PP3V3_PCI)
 - _PP3V3_PWRON_SB
 - _PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD11 - PCI0 (0x106B/0x0053)
 AD11 - PCI1 (0x106B/0x0054)
 AD11 - PCI2 (0x106B/0x0055)
 AD23 - KeyLargo (0x106B/0x004F, PCI1)
 AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
 AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
 AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
 AD31 - Ethernet (0x106B/0x0051, PCI0)



Shasta PCI Interface

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SIZE	DRAWING NUMBER	REV.
D	051-6482	C
SCALE	SHT	74 OF 103
NONE		

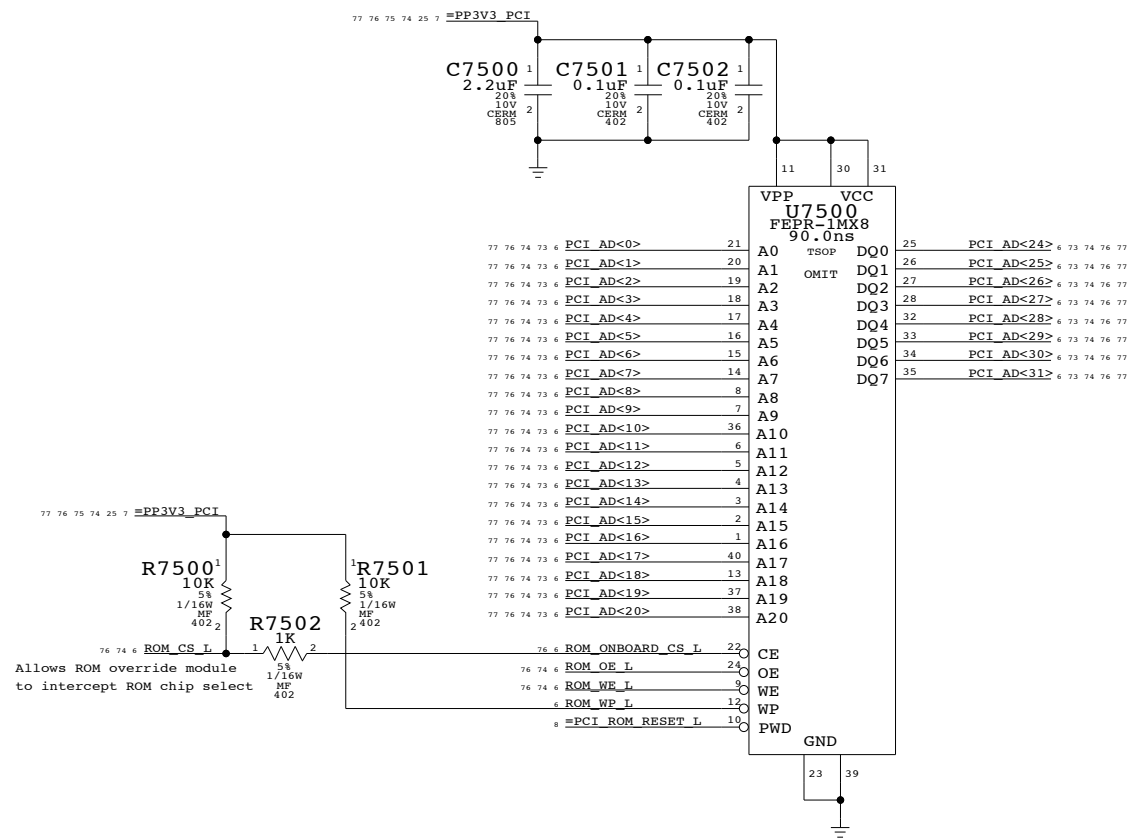
Page Notes

Power aliases required by this page:
 - _PP3V3_PCI

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



Master: Link

BootROM

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_DRAWING
 TITLE=FIZZY
 ABBREV=DRAWING
 LAST_MODIFIED=Wed Aug 4 17:58:24 2004

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHEET OF 75 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 8 76

Page Notes

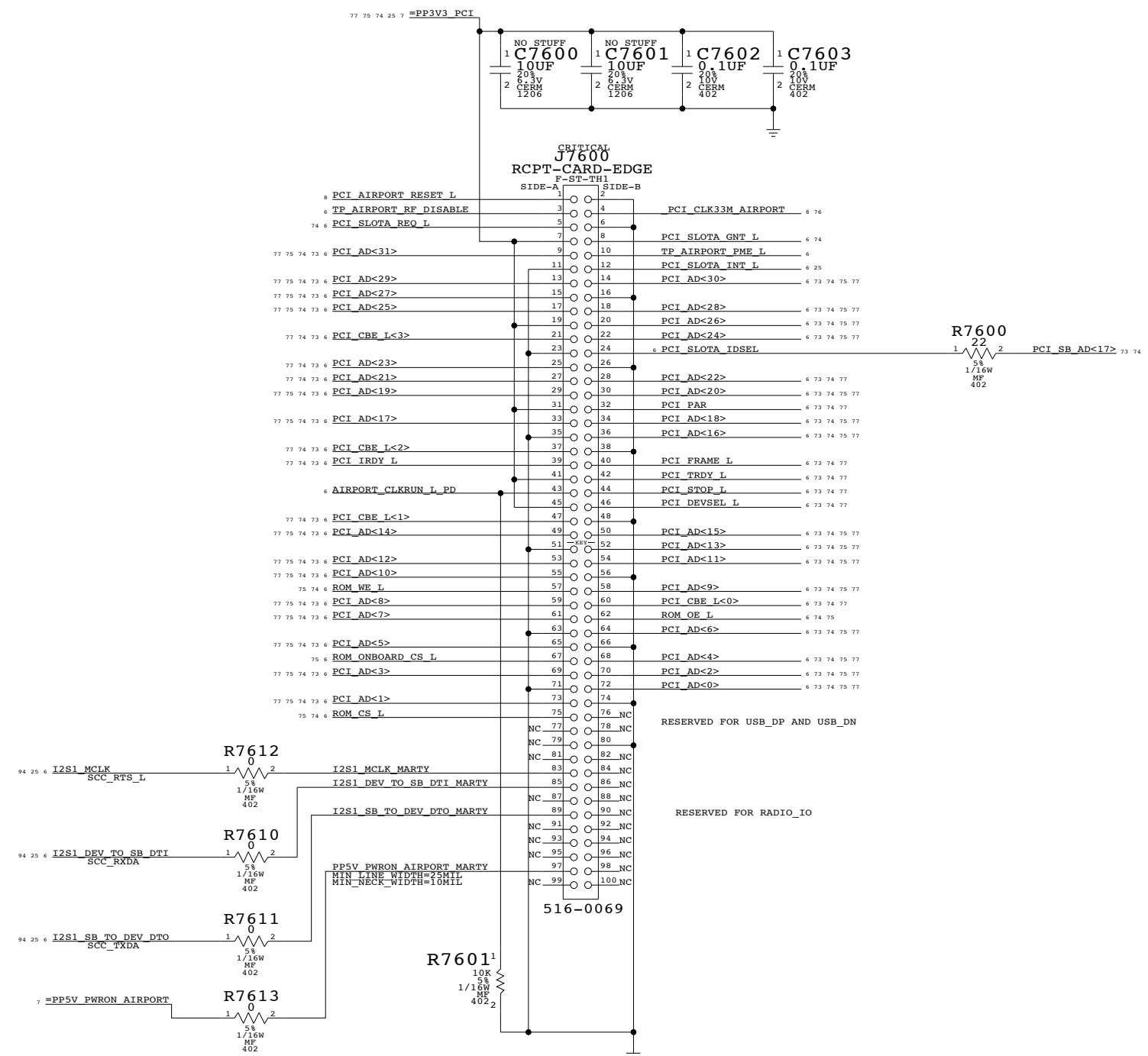
Power aliases required by this page:
 - _PP3V3_PCI

Signal aliases required by this page:
 - _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



AirPort Extreme

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT OF		
NONE	76 OF		103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	=PCI_CLK33M_USB2

Page Notes

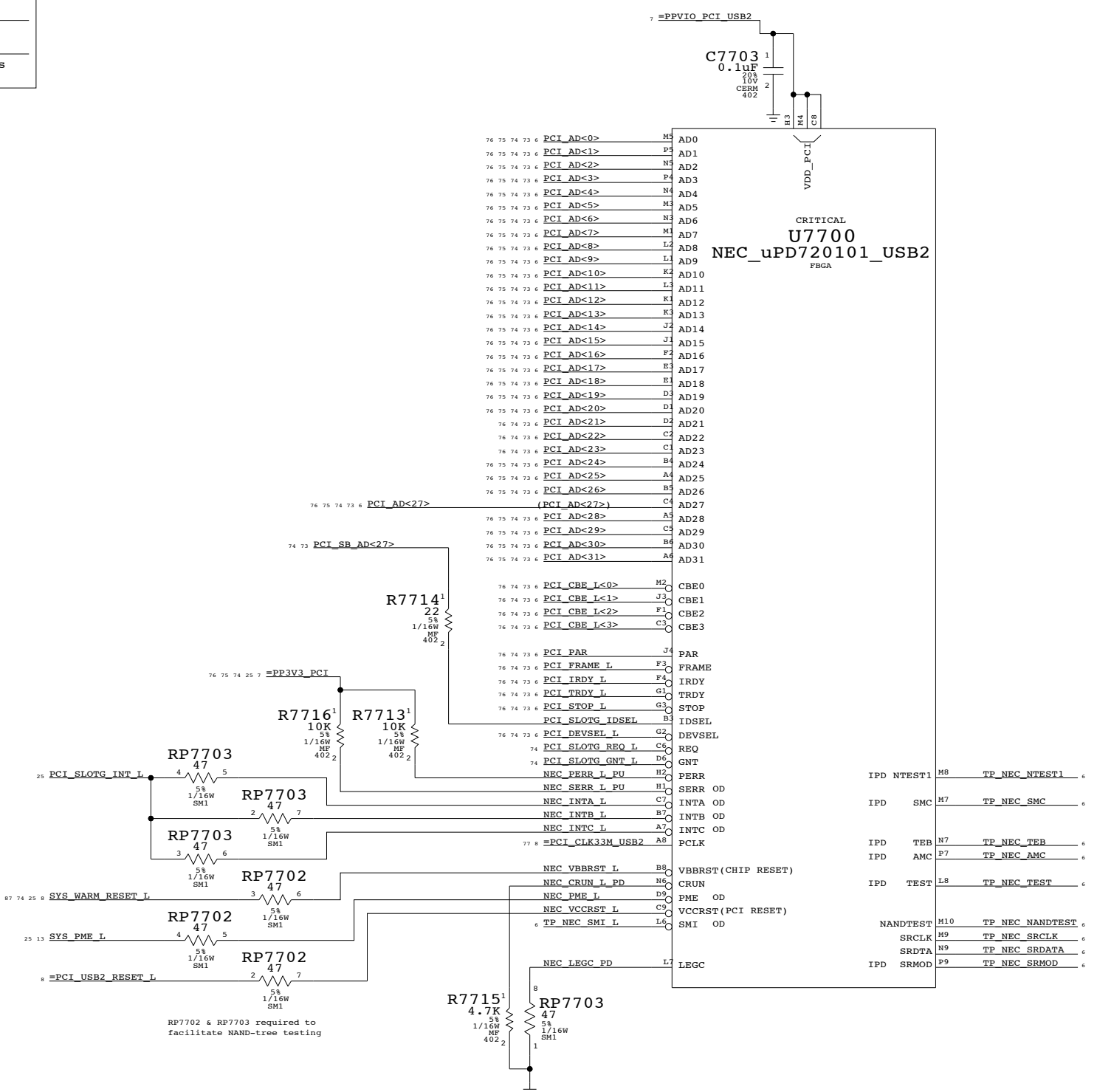
Power aliases required by this page:
 - _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
 - _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



Master: Link

USB 2.0 PCI Interface

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	D	051-6482	C
SCALE	SHT	OF	
NONE	77	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD		UATA_DD<15..8>	
UATA_DD7		UATA_DD<7>	
UATA_DD		UATA_DD<6..0>	
UATA_HOST		UATA_DA<2..0>	
UATA_HOST		UATA_CS0_L	
UATA_HOST		UATA_CS1_L	
UATA_HOST		UATA_HSTROBE	
UATA_HOST		UATA_STOP	
UATA_HOST_R		UATA_DMACK_L	
UATA_HOST_R		UATA_RESET_L	
UATA_DEV_R_C		UATA_DSTROBE	
UATA_DEV_R		UATA_DMARQ	
UATA_DEV_R		UATA_INTRQ	

Page Notes

Power aliases required by this page:
 - _PP1V2_PWRON_DISK

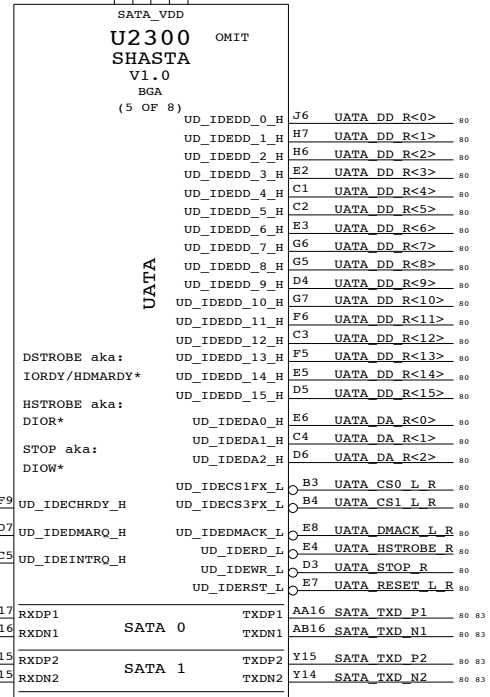
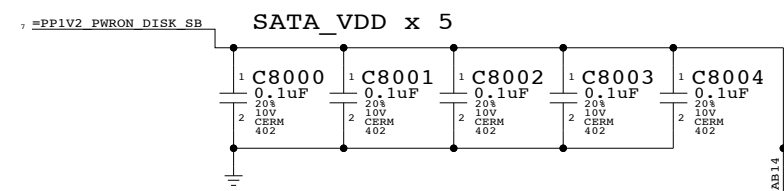
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Net Spacing Type: SATA

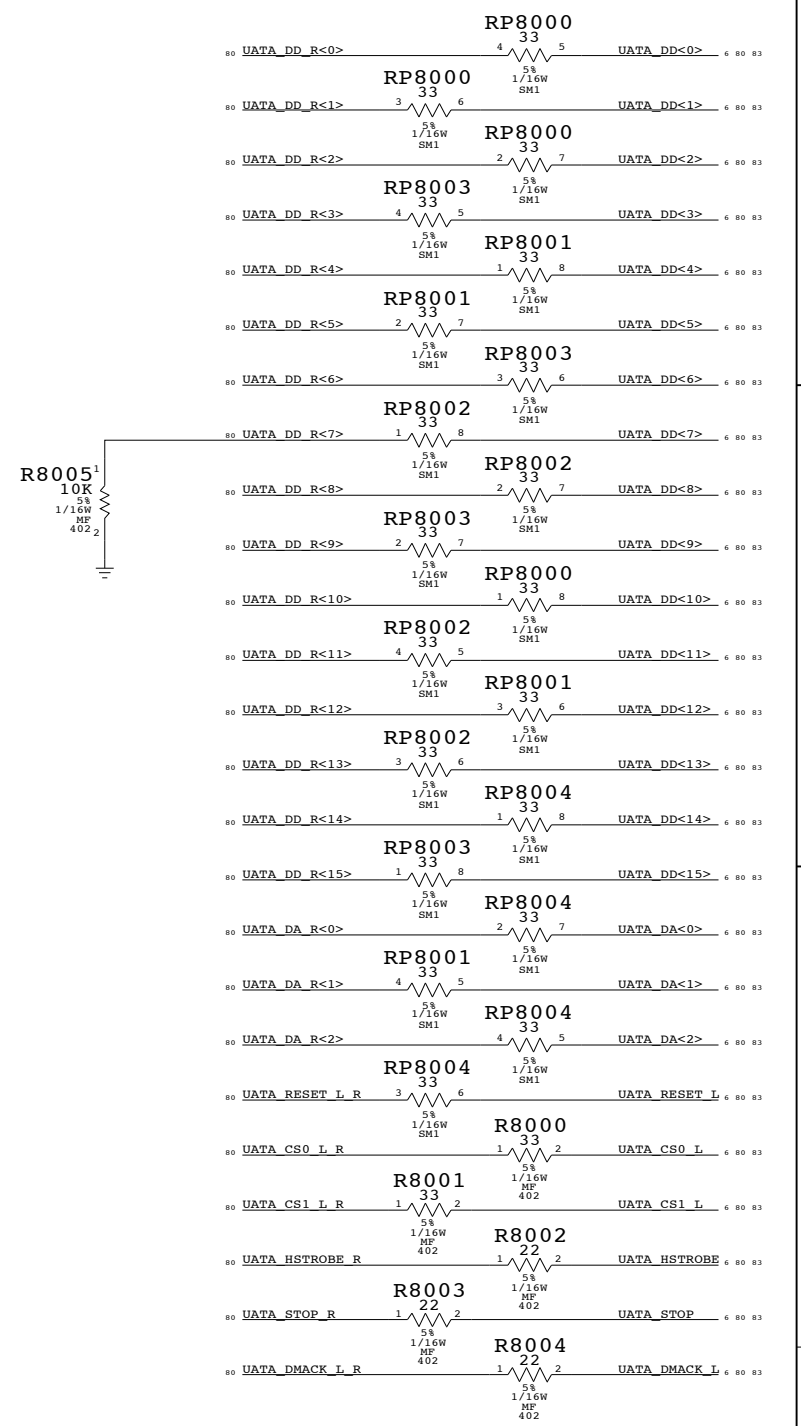
Line To Line: 15 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 10 mils outer
 Primary Max Sep: 9 mils inner
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.



AC coupling required for any SATA pair used.
 Recommend 0.1uF cap placed close to Shasta.
 (Caps provided by device page)

UATA Termination



Master: Link

Shasta Disk

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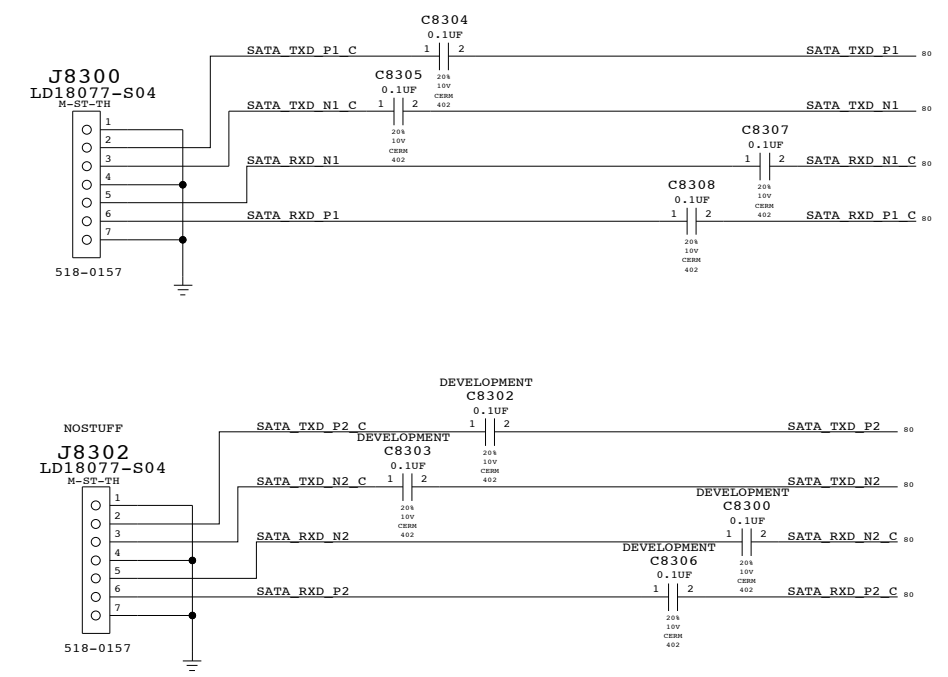
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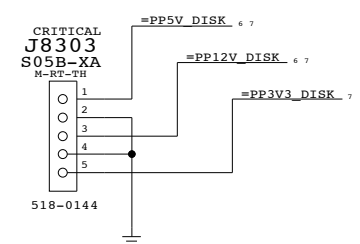
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
83 80 6 UATA_DD<15..8>	UATA_DD			
83 80 6 UATA_DD<7>	UATA_DD7			
83 80 6 UATA_DD<6..0>	UATA_DD			
83 80 6 UATA_DA<2..0>	UATA_HOST			
83 80 6 UATA_CS0_L	UATA_HOST			
83 80 6 UATA_CS1_L	UATA_HOST			
83 80 6 UATA_HSTROBE	UATA_HOST			
83 80 6 UATA_STOP	UATA_HOST			
83 80 6 UATA_DMACK_L	UATA_HOST_R			
83 80 6 UATA_RESET_L	UATA_HOST_R			
83 80 6 UATA_DSTROBE	UATA_DEV_R_C			
83 80 6 UATA_DMARQ	UATA_DEV_R			
83 80 6 UATA_INTRO	UATA_DEV_R			

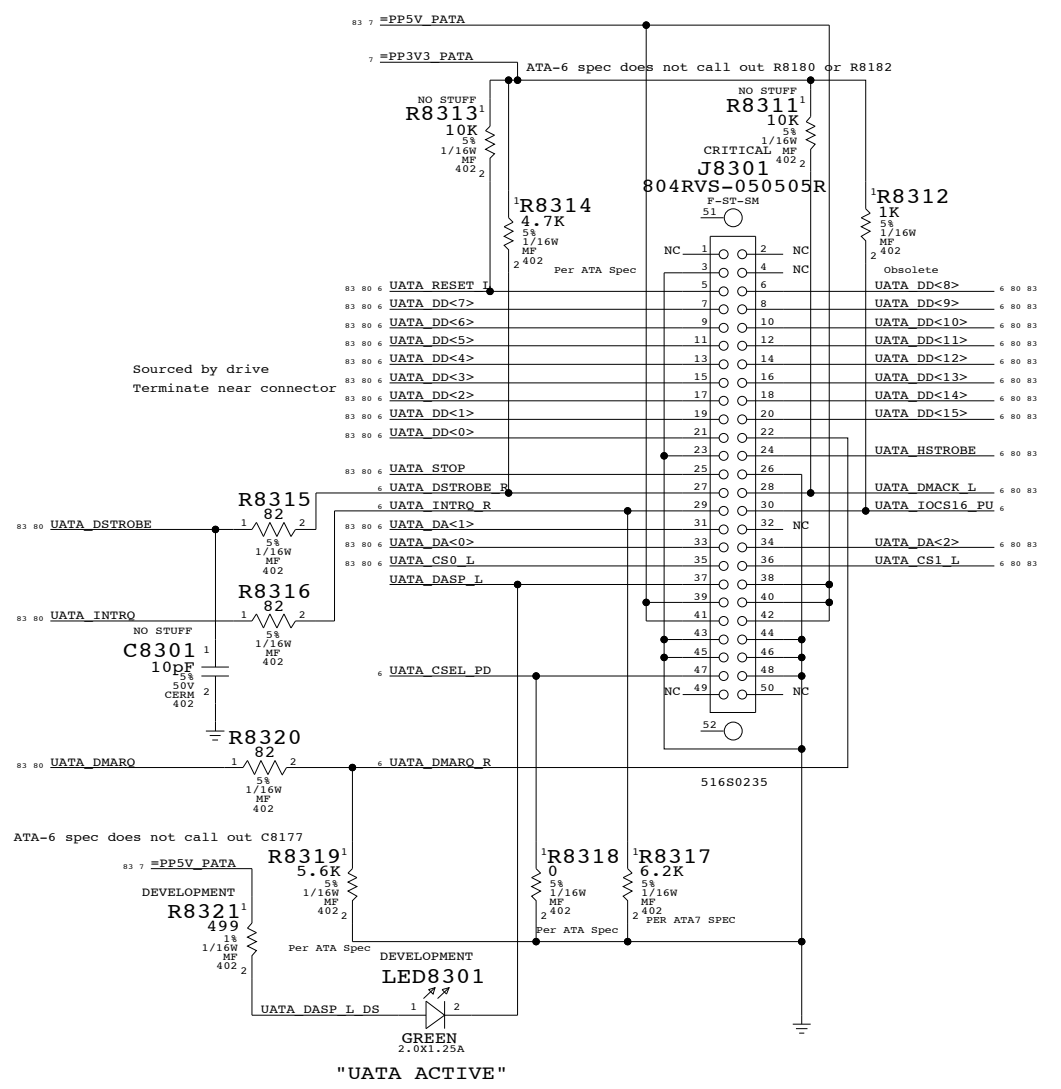
SATA CONNECTORS



HD POWER



PATA CONNECTOR



DISK CONNECTORS

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SCALE	NONE	SHT OF	83 OF 103

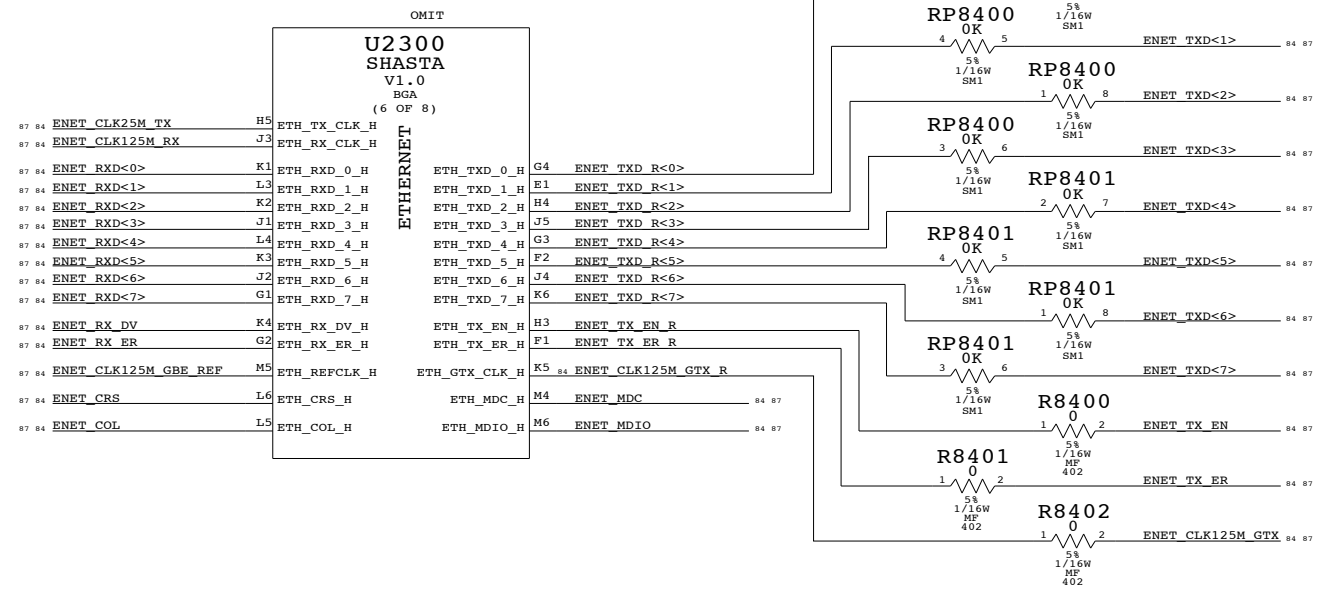
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK	ENET	10 MIL	ENET_CLK25M_TX
ENET_RX_CLK	ENET	10 MIL	ENET_CLK125M_RX
ENET_GBE_REF	ENET	15 MIL SPACING	ENET_CLK125M_GBE_REF
ENET_TX_CLK	ENET	15 MIL SPACING	ENET_CLK125M_GTX
	ENET	15 MIL SPACING	ENET_CLK125M_GTX_R
ENET_RX	ENET		ENET_RXD<7..0>
ENET_RX_CTL	ENET		ENET_RX_DV
ENET_RX_CTL	ENET		ENET_RX_ER
ENET_TX	ENET		ENET_TXD<7..0>
ENET_TX_CTL	ENET		ENET_TX_EN
ENET_TX_CTL	ENET		ENET_TX_ER
ENET_RX_CTL	ENET		ENET_CR_S
ENET_RX_CTL	ENET		ENET_COL
ENET_MDC	ENET		ENET_MDC
ENET_MDIO	ENET		ENET_MDIO

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

Shasta Ethernet

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	D	051-6482	C
SCALE	SHT		OF
NONE	84		103

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ABBREV=DRAWING
LAST_MODIFIED=Tue Aug 3 15:55:45 2004

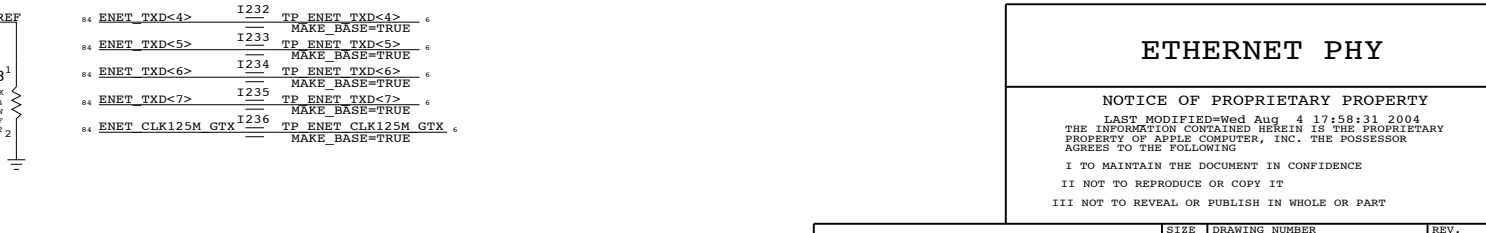
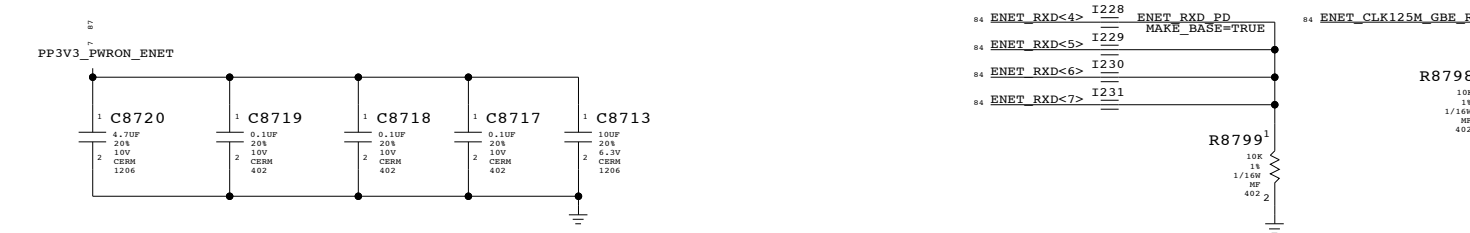
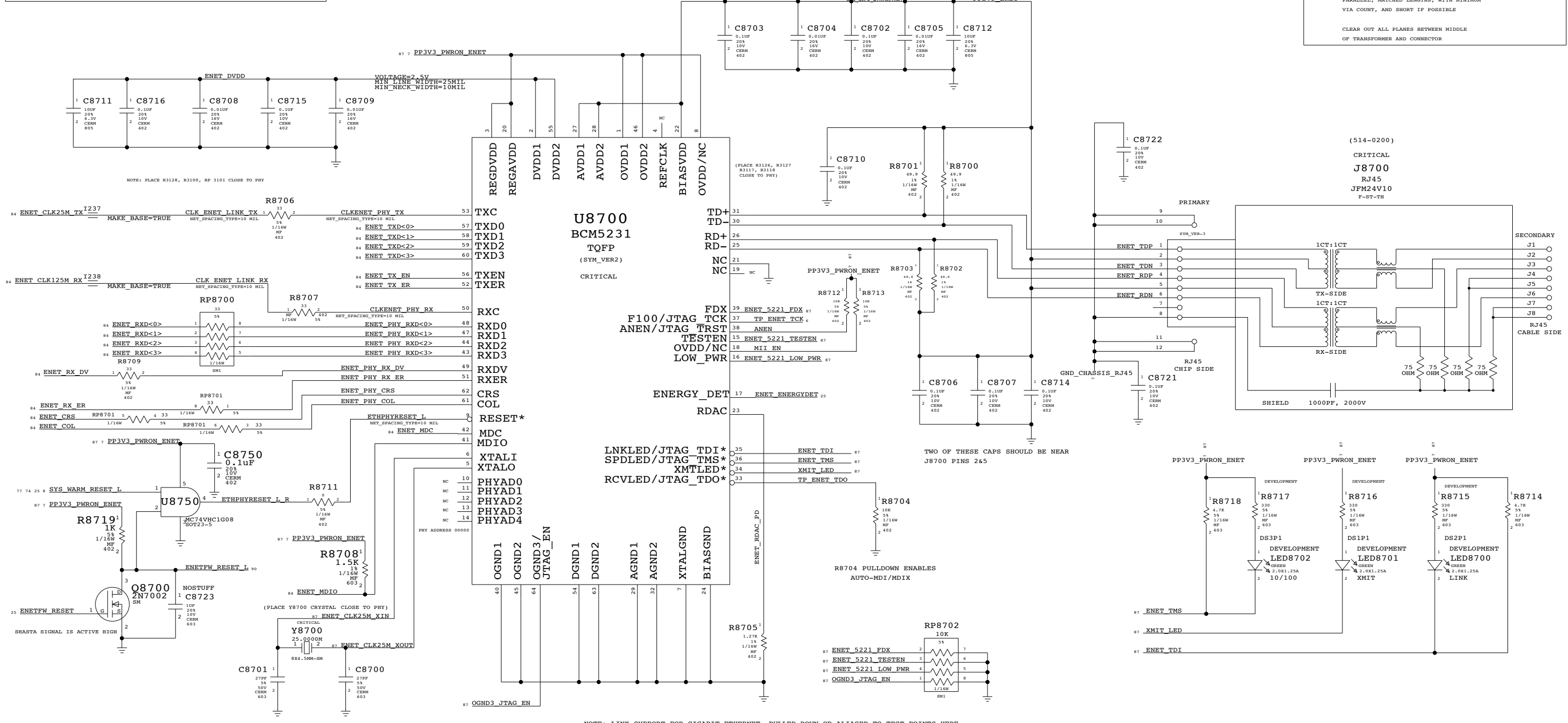
ETHERNET ROUTING PRIORITY:
 1. DECOUPLING CAPS
 2. TX TERMINATION - LOCATE NEAR PHY
 3. RX TERMINATION - LOCATE NEAR PHY

ROUTE TO OVER 2.5V PLANE (BOTTOM LAYER) ONLY
 ROUTE RD OVER GROUND PLANE (TOP LAYER) ONLY

ALL DIFFERENTIAL SIGNALS SHOULD BE CLOSE,
 PARALLEL, MATCHED LENGTHS, WITH MINIMUM
 VIA COUNT, AND SHORT IF POSSIBLE

CLEAR OUT ALL PLANES BETWEEN MIDDLE
 OF TRANSFORMER AND CONNECTOR

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_MDI_TX	ENET	ENET_MDI_TD
ENET_MDI_RX	ENET	ENET_MDI_RD
ENET_XTAL	15 MIL SPACING	ENET_CLK25M_XIN
	15 MIL SPACING	ENET_CLK25M_XOUT



ETHERNET PHY

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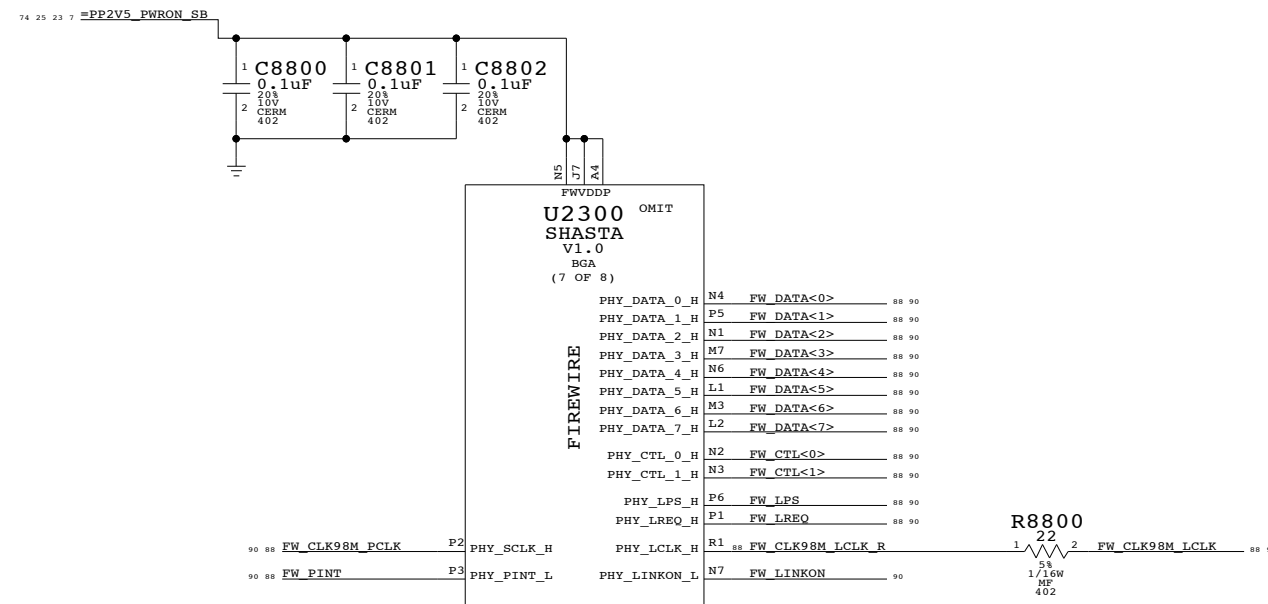
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW	FW		FW DATA<7..0>
FW	FW		FW CTL<1..0>
FW_LPS	FW		FW LPS
FW_LREQ	FW		FW LREQ
FW_PINT	FW		FW PINT
FW_LCLK	FW	15 MIL SPACING	FW CLK98M_LCLK
FW_PCLK	FW	15 MIL SPACING	FW CLK98M_PCLK
		15 MIL SPACING	FW CLK98M_LCLK_R

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

Shasta FireWire

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TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 4 17:58:31 2004



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	C
SCALE	SHT	OF
NONE	88	103

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2 P<0>
USB2_0	USB2	USB2	USB2_0	USB2 N<0>
USB2_1	USB2	USB2	USB2_1	USB2 P<1>
USB2_1	USB2	USB2	USB2_1	USB2 N<1>
USB2_2	USB2	USB2	USB2_2	USB2 P<2>
USB2_2	USB2	USB2	USB2_2	USB2 N<2>
USB2_3	USB2	USB2	USB2_3	USB2 P<3>
USB2_3	USB2	USB2	USB2_3	USB2 N<3>
USB2_4	USB2	USB2	USB2_4	USB2 P<4>
USB2_4	USB2	USB2	USB2_4	USB2 N<4>
USB2_NEC_XTAL	15 MIL SPACING		NEC_CLK30M_XT1	
	15 MIL SPACING		NEC_CLK30M_XT2	
	15 MIL SPACING		NEC_CLK30M_XT2_R	

Page Notes

Power aliases required by this page:
 - _PP3V3_PWRON_USB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

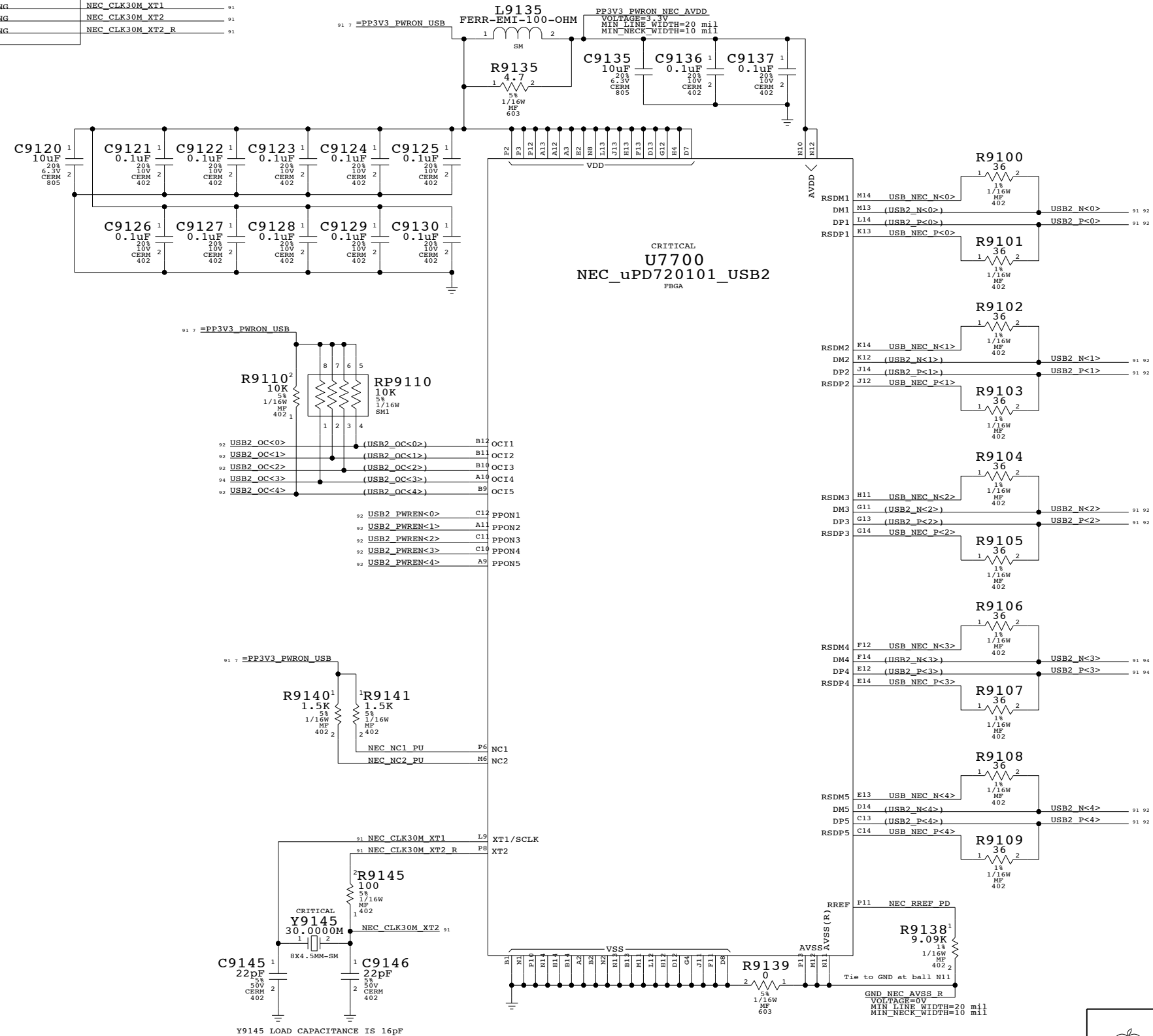
Net Spacing Type: USB2

Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA
 V1.0
 BGA
 (8 OF 8)
 OMIT

NC0	P7	TP_SB_NC_P7
NC1	P8	TP_SB_NC_P8
NC2	R3	TP_SB_NC_R3
NC3	R4	TP_SB_NC_R4
NC4	R5	TP_SB_NC_R5
NC5	R6	TP_SB_NC_R6
NC6	R7	TP_SB_NC_R7
NC7	R8	TP_SB_NC_R8
NC8	T1	TP_SB_NC_T1
NC9	T2	TP_SB_NC_T2
NC10	T3	TP_SB_NC_T3
NC11	T4	TP_SB_NC_T4
NC12	T5	TP_SB_NC_T5
NC13	T6	TP_SB_NC_T6
NC14	T7	TP_SB_NC_T7
NC15	T8	TP_SB_NC_T8
NC16	U1	TP_SB_NC_U1
NC17	U2	TP_SB_NC_U2
NC18	U3	TP_SB_NC_U3
NC19	U4	TP_SB_NC_U4
NC20	U5	TP_SB_NC_U5
NC21	U6	TP_SB_NC_U6
NC22	V1	TP_SB_NC_V1
NC23	V2	TP_SB_NC_V2
NC24	V3	TP_SB_NC_V3
NC25	V4	TP_SB_NC_V4
NC26	W1	TP_SB_NC_W1
NC27	W3	TP_SB_NC_W3
NC28	Y1	TP_SB_NC_Y1
NC29	Y3	TP_SB_NC_Y3



Master: Fizzy

USB Host Interfaces

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 ABBREV=DRAWING
 LAST_MODIFIED=Wed Aug 4 17:58:34 2004

SIZE	DRAWING NUMBER	REV.
D	051-6482	C
SCALE	SHT	OF
NONE	91	103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PROVIDED	USB2	USB2_PORT1_F
BY	USB2	USB2_PORT1_N_F
USB	USB2	USB2_PORT2_F
CONTROLLER	USB2	USB2_PORT2_N_F
	USB2	USB2_PORT3_F
	USB2	USB2_PORT3_N_F

Page Notes

Power aliases required by this page:
 - PP5V_PWRON_USB
 - PP5V_PWRON_UDASH
 - PP3V3_PWRON_UDASH
 - PP3V3_PWRON_BT

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

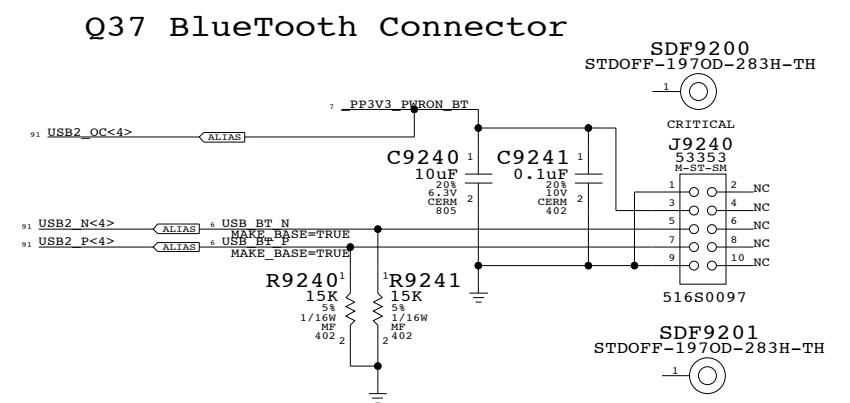
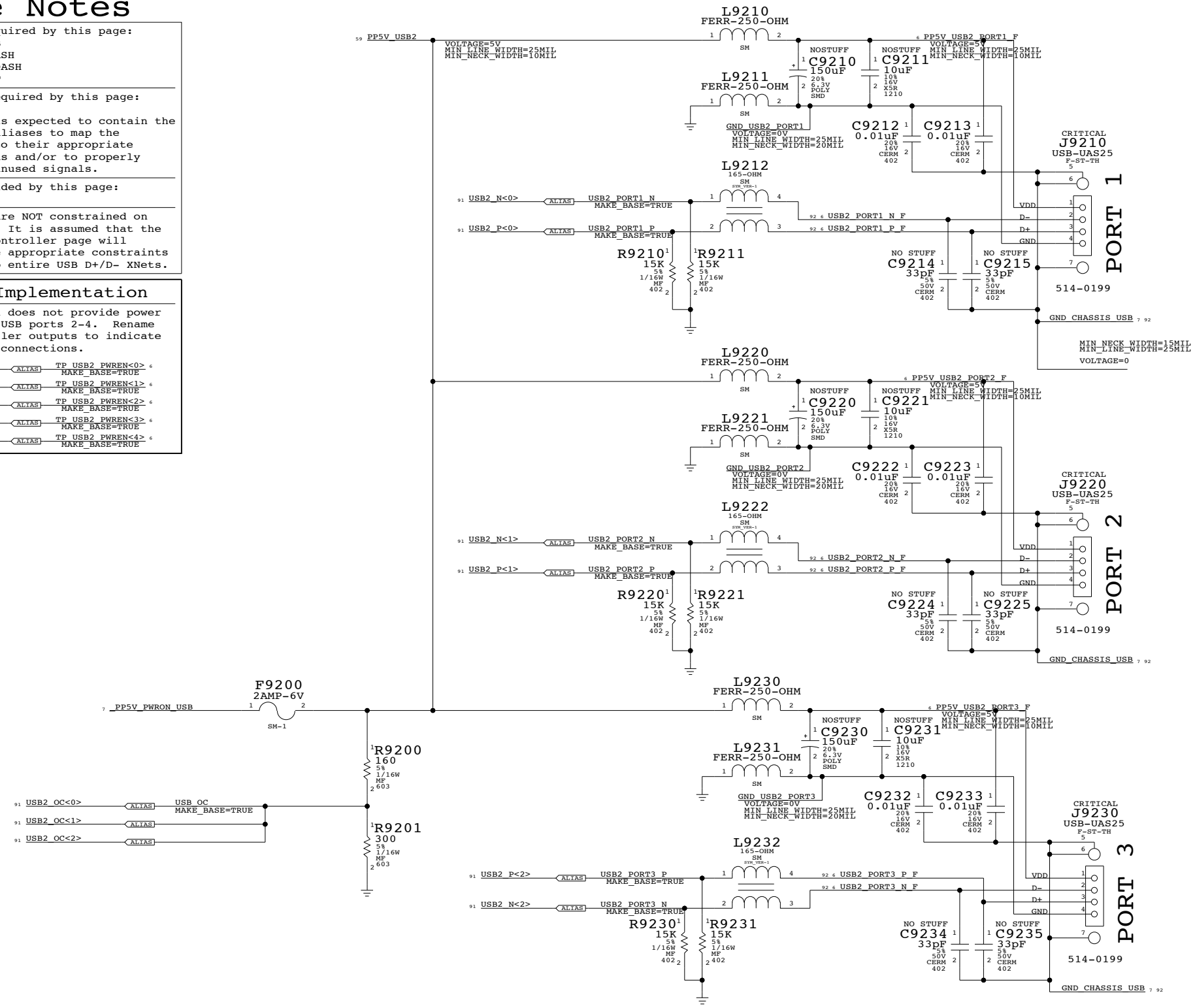
NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

91 USB2_PWREN<0> <ALIAS> TP USB2_PWREN<0> MAKE_BASE=TRUE
 91 USB2_PWREN<1> <ALIAS> TP USB2_PWREN<1> MAKE_BASE=TRUE
 91 USB2_PWREN<2> <ALIAS> TP USB2_PWREN<2> MAKE_BASE=TRUE
 91 USB2_PWREN<3> <ALIAS> TP USB2_PWREN<3> MAKE_BASE=TRUE
 91 USB2_PWREN<4> <ALIAS> TP USB2_PWREN<4> MAKE_BASE=TRUE

External USB Ports



USB Device Interfaces

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SCALE	SHT	OF	
NONE	92	103	

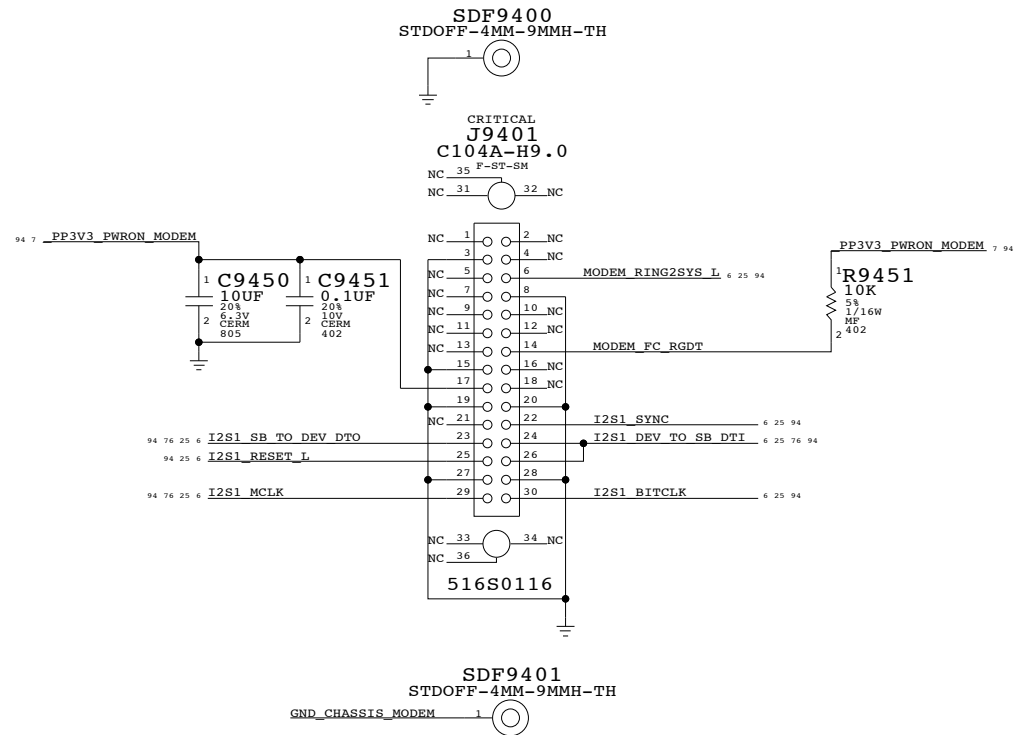
Page Notes

Power aliases required by this page:
 - _PP3V3_PWRON_MODEM
 Spec Load: 0.5 A active, 3 mA auxiliary

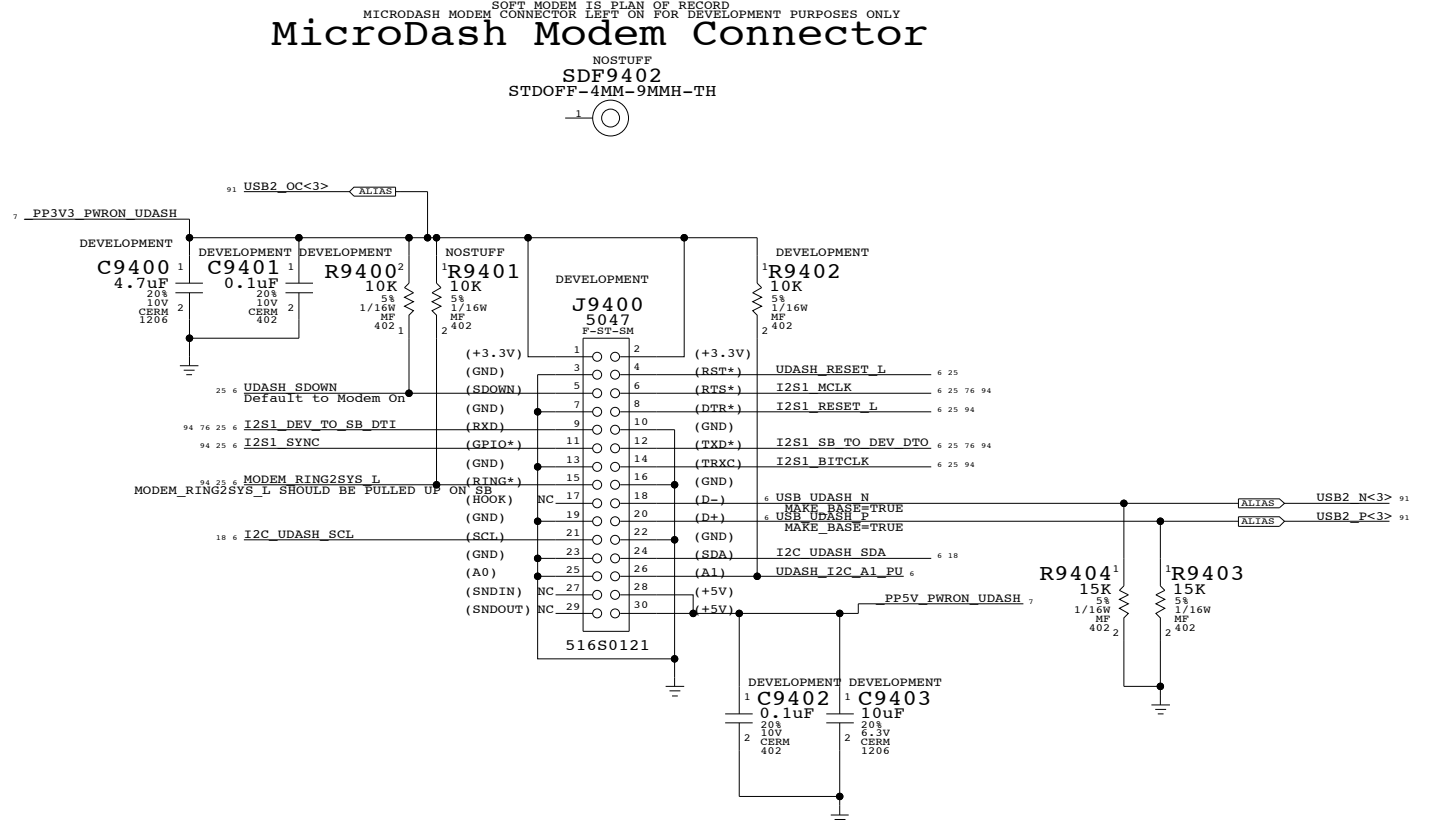
Signal aliases required by this page:
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BOM options provided by this page:
 (NONE)

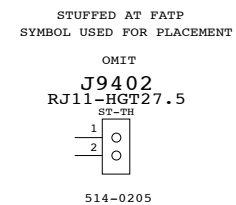
Q52 Modem Connector



MicroDash Modem Connector



RJ11 CONNECTOR



From Intel Mobile Audio/Modem
 Daughter Card Specification
 Rev 1.0, February 22, 1999

- | | |
|----------------------|---------------------|
| 1 - MONO_OUT/PC_BEEP | 2 - AUDIO_PWRON |
| 3 - GND | 4 - MONO_PHONE |
| 5 - AUX_RIGHT | 6 - RESERVED |
| 7 - AUX_LEFT | 8 - GND |
| 9 - CD_GND | 10 - 5Vmain |
| 11 - CD_RIGHT | 12 - RESERVED |
| 13 - CD_LEFT | 14 - RESERVED |
| 15 - GND | 16 - PRIMARY_DN |
| 17 - 3.3Vaux | 18 - 5Vd |
| 19 - GND | 20 - GND |
| 21 - 3.3Vmain | 22 - AC97_SYNC |
| 23 - AC97_SDATA_OUT | 24 - AC97_SDATA_INB |
| 25 - AC97_RESET# | 26 - AC97_SDATA_INA |
| 27 - GND | 28 - GND |
| 29 - AC97_MSTRCLK | 30 - AC97_BITCLK |

Modem Interface

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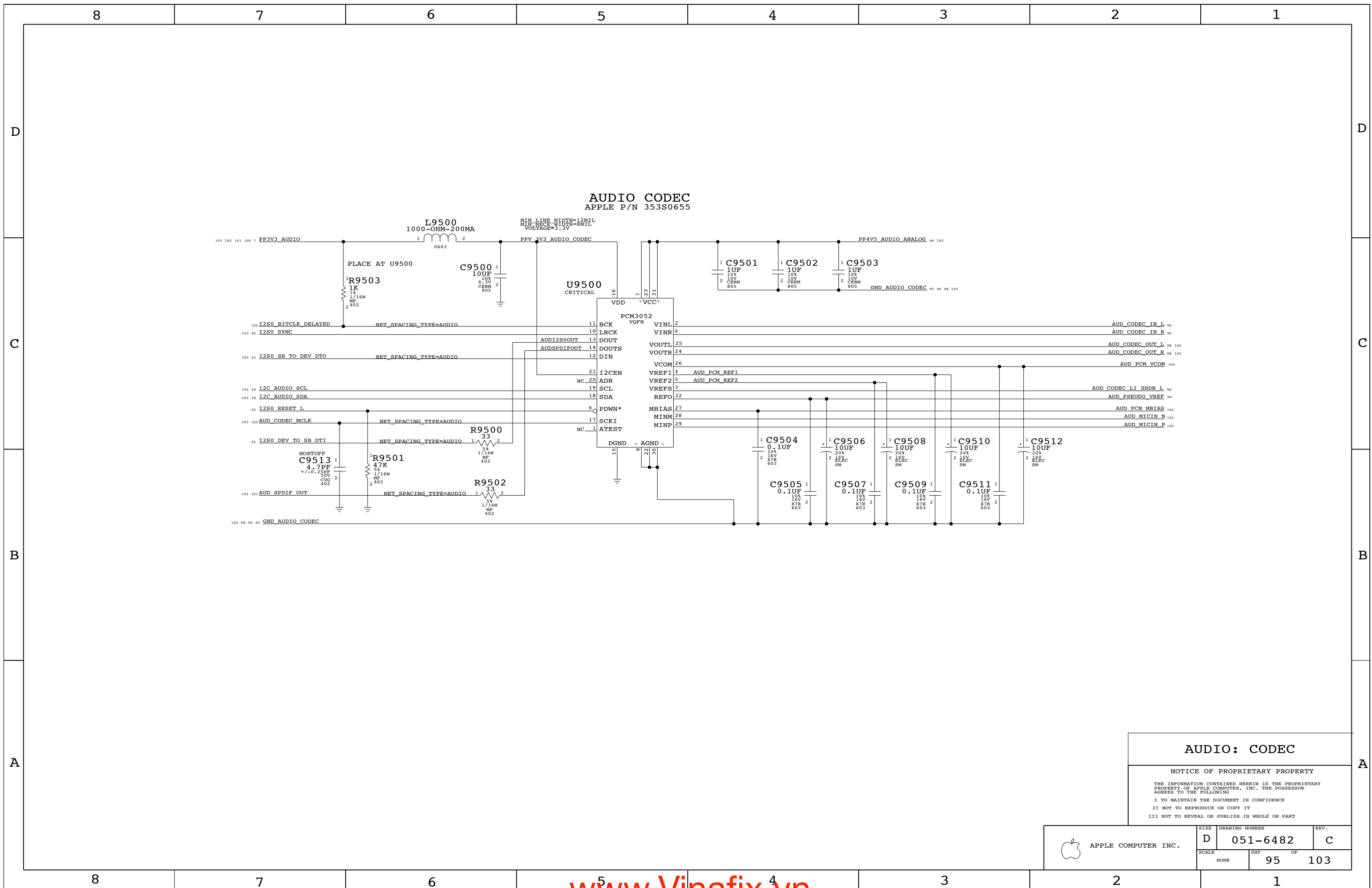
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SCALE	SHT OF		
NONE	94		103



AUDIO: CODEC

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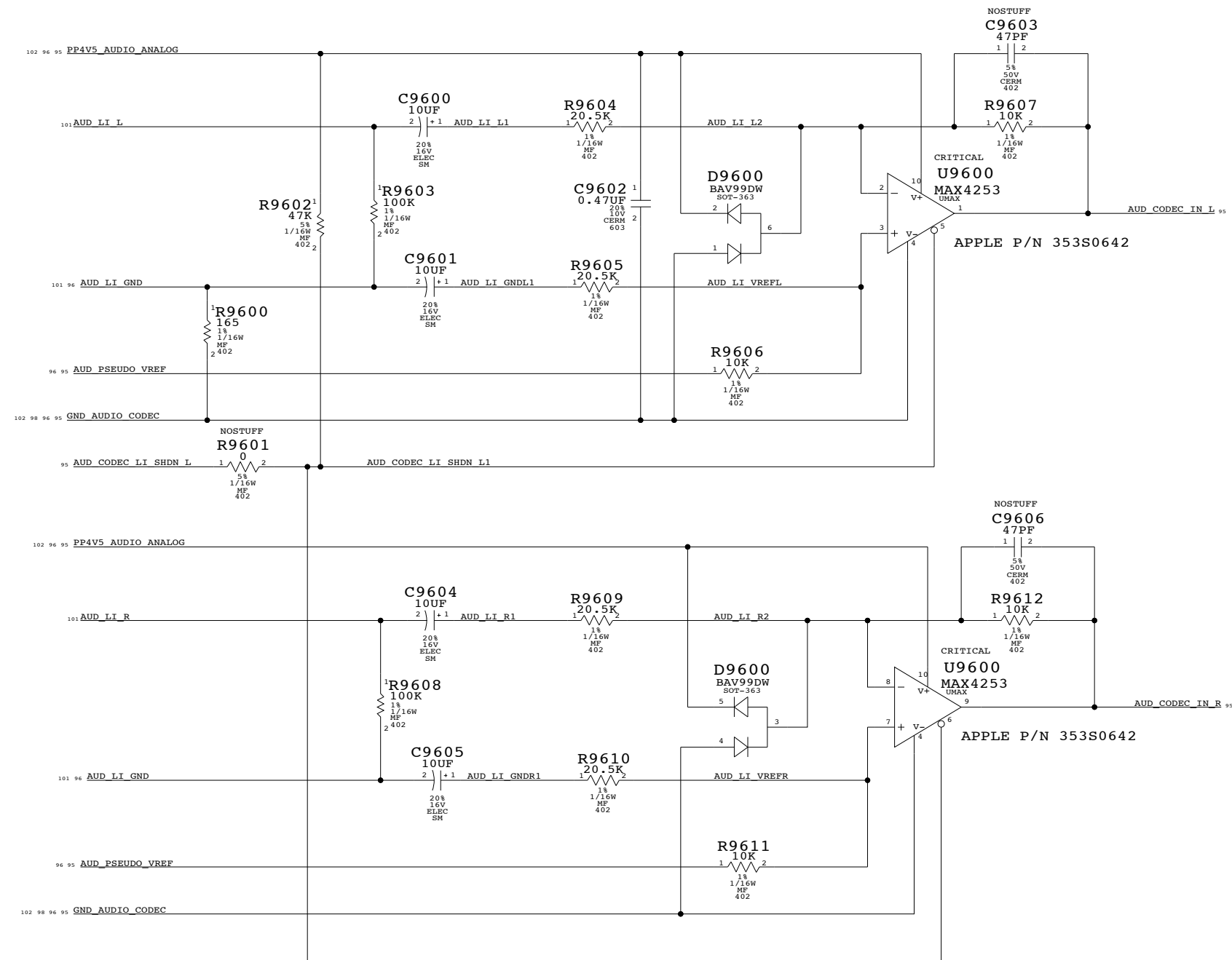
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHT 95	OF 103

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

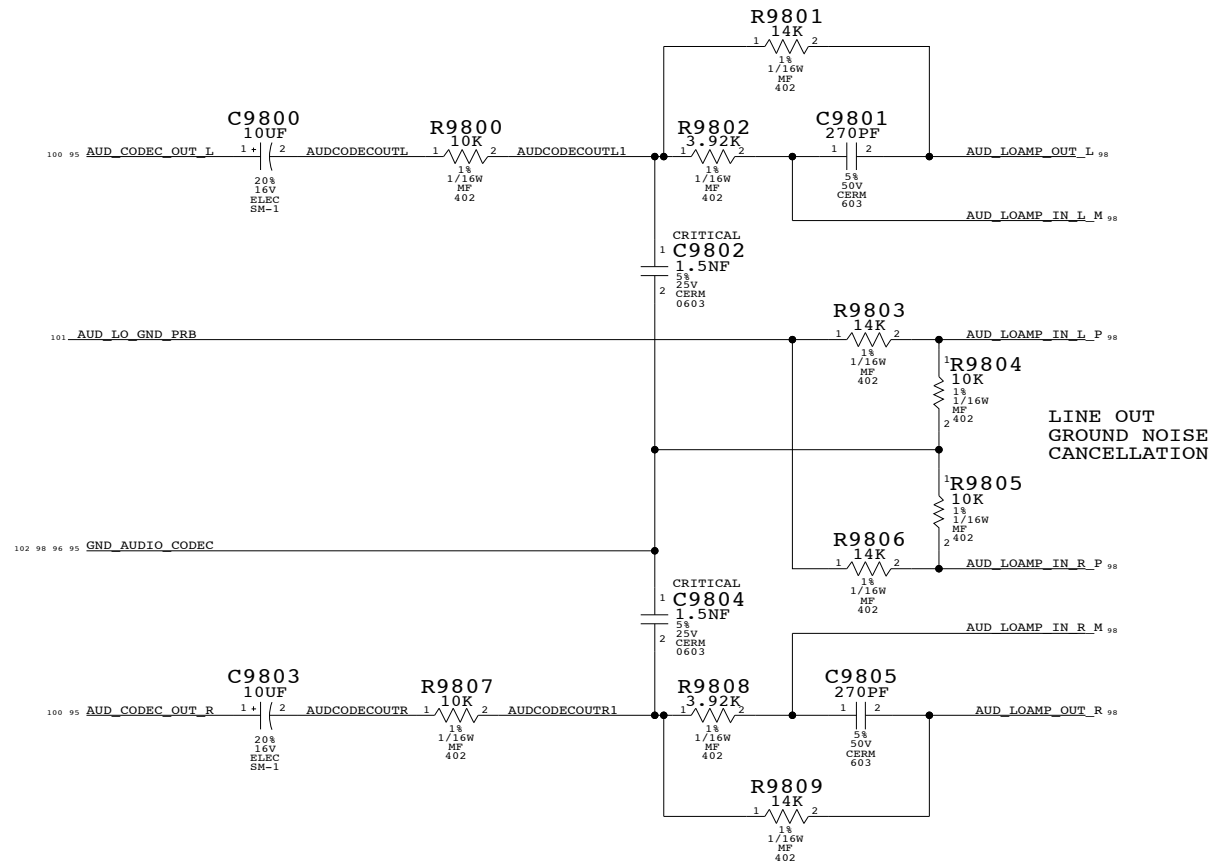
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	D	051-6482	C
SCALE	NONE	SHT OF	96 OF 103

LINE OUT LOW-PASS FILTER

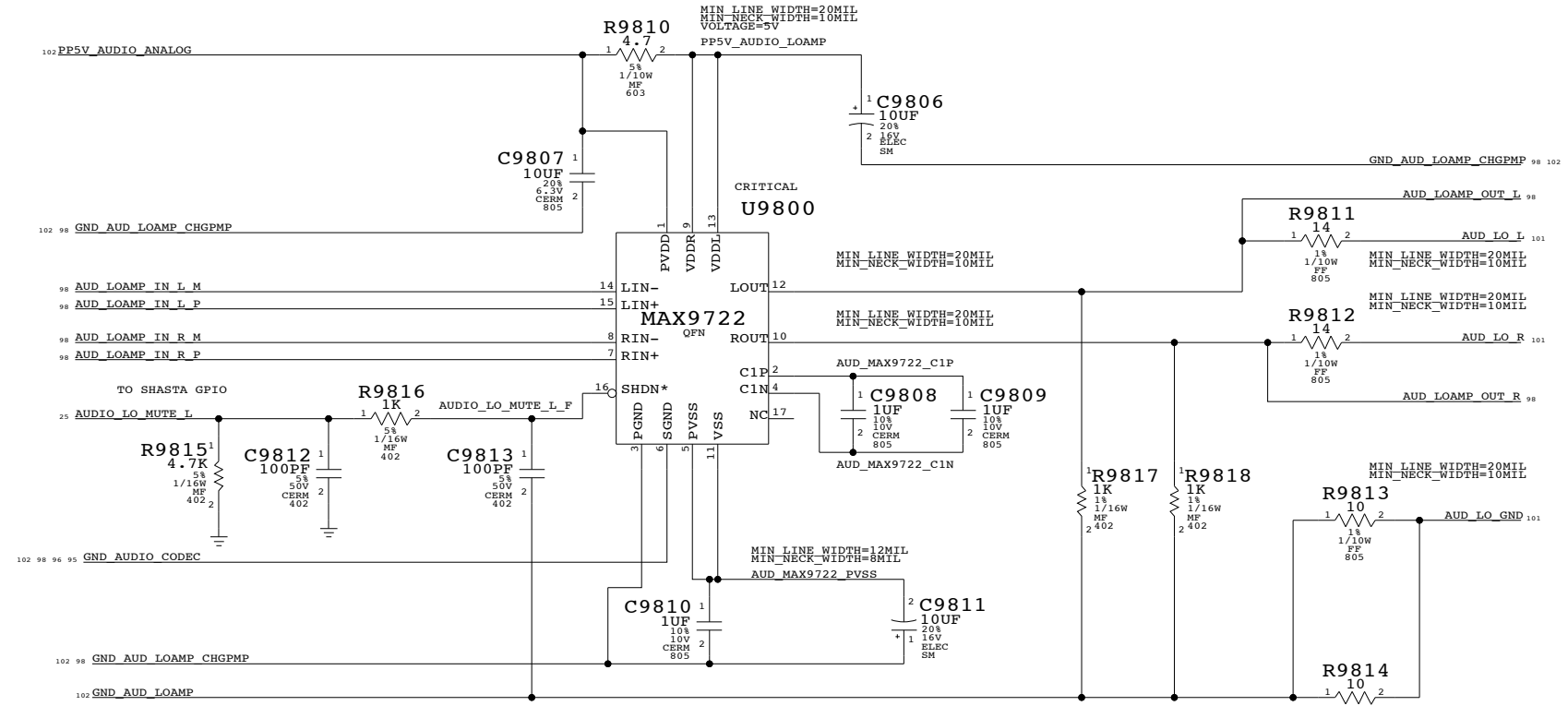
FC = 37 KHZ, HO = -1.4



LINE OUT
GROUND NOISE
CANCELLATION

LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

NOTICE OF PROPRIETARY PROPERTY

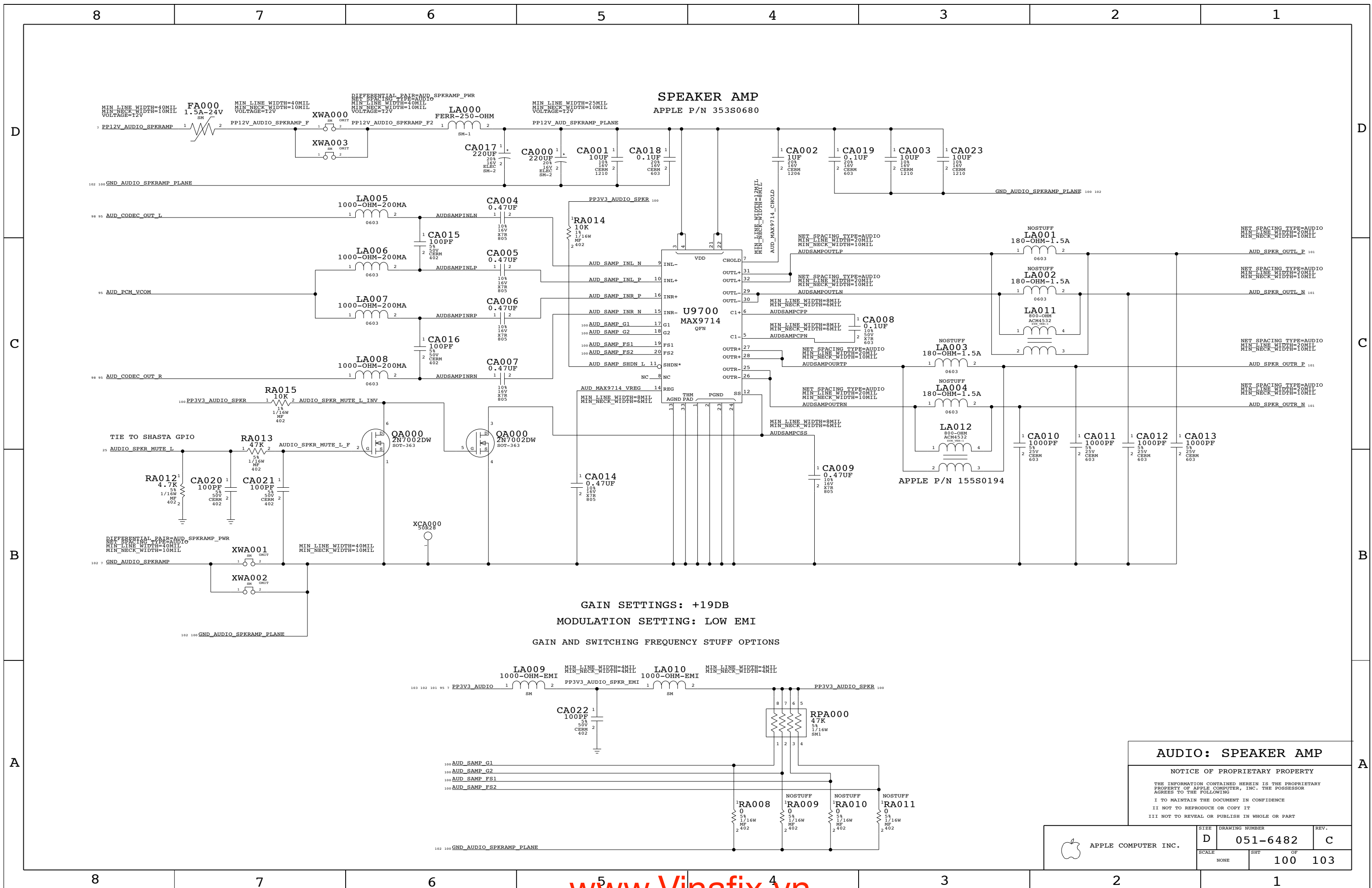
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SCALE	SHT	OF	REV.
NONE	98	103	



GAIN SETTINGS: +19DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP

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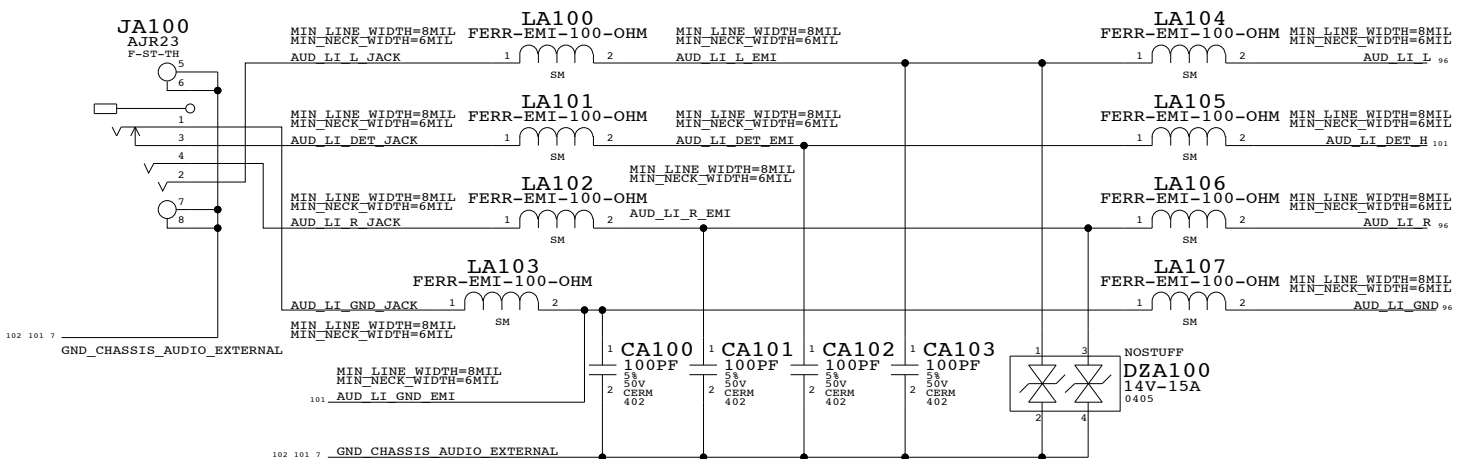
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SCALE	SHEET OF		
NONE	100		103

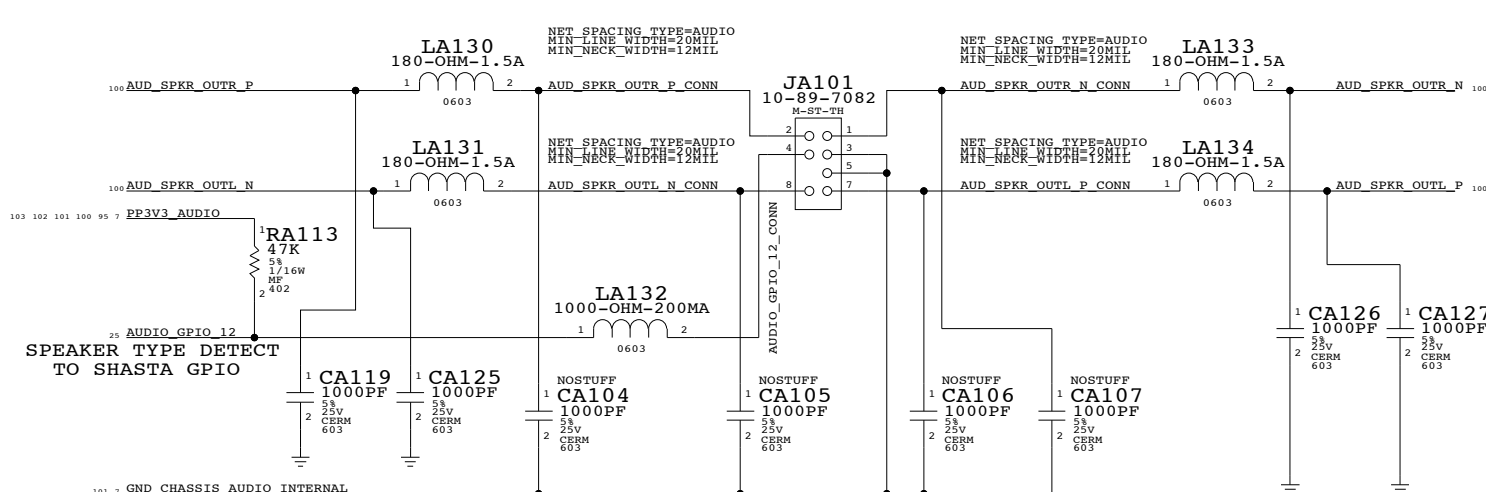
LINE IN JACK

APPLE P/N 514-0203



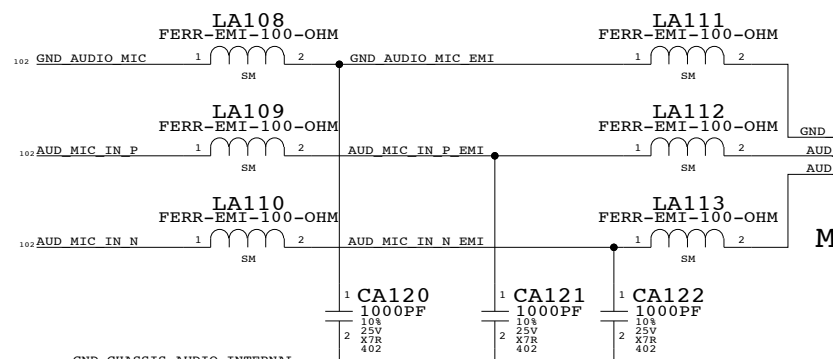
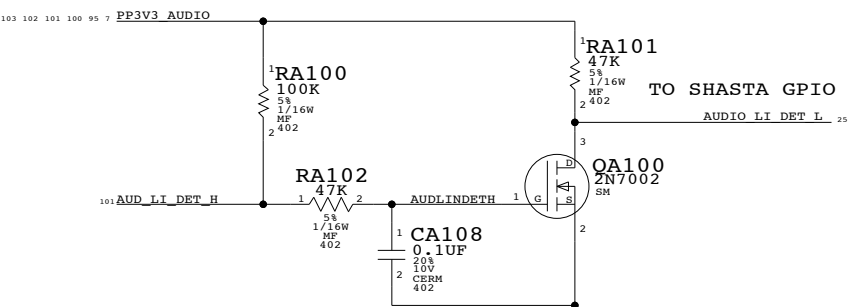
SPEAKER CABLE CONNECTOR

APPLE P/N 518-0138



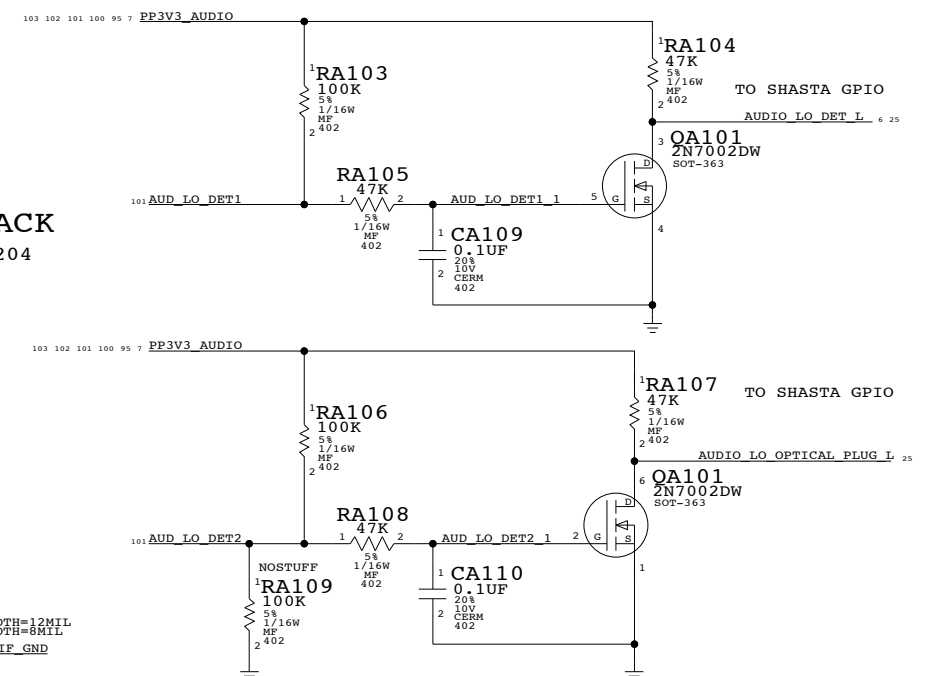
LINE IN PLUG DETECT

AUDIO_IN_DET_O_L = LOW: PLUG INSERTED
AUDIO_IN_DET_O_L = HIGH: PLUG NOT INSERTED



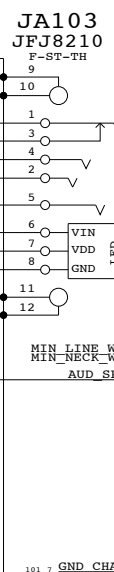
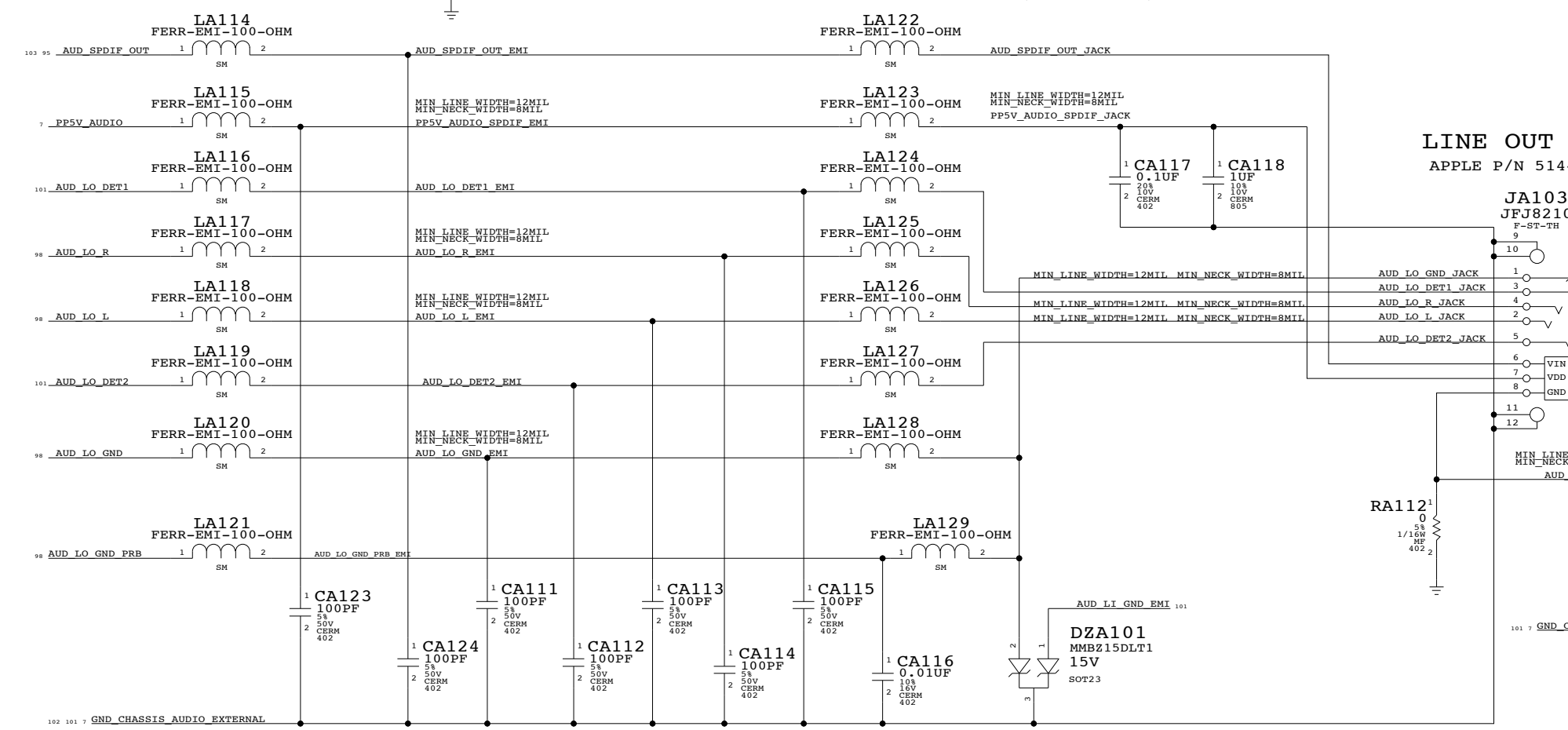
LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED
AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK

APPLE P/N 514-0204



AUDIO: Q45 CONNECTORS

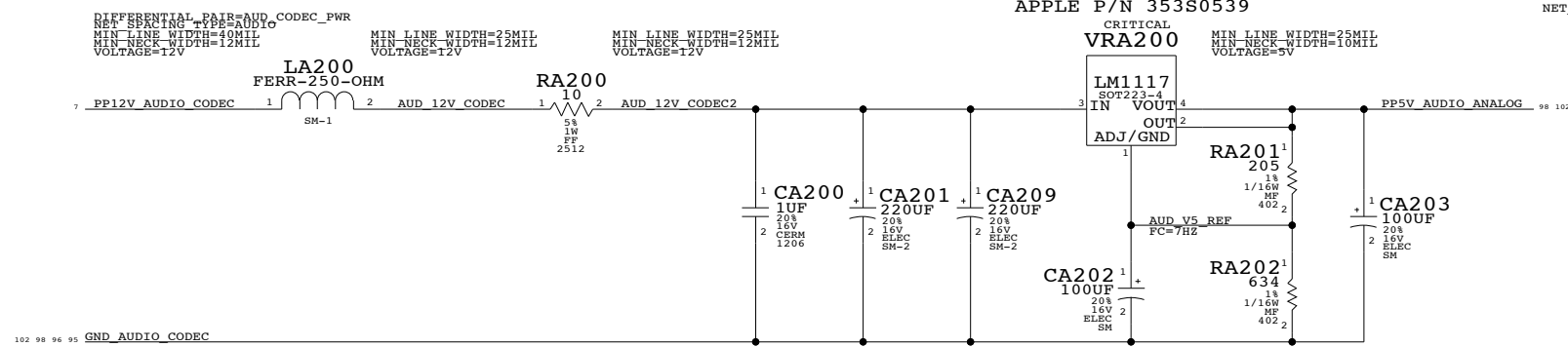
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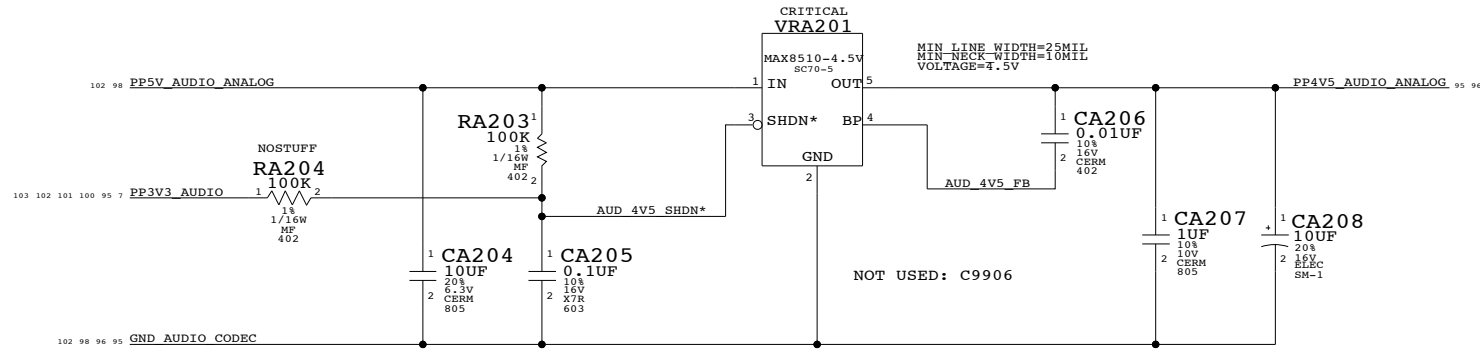
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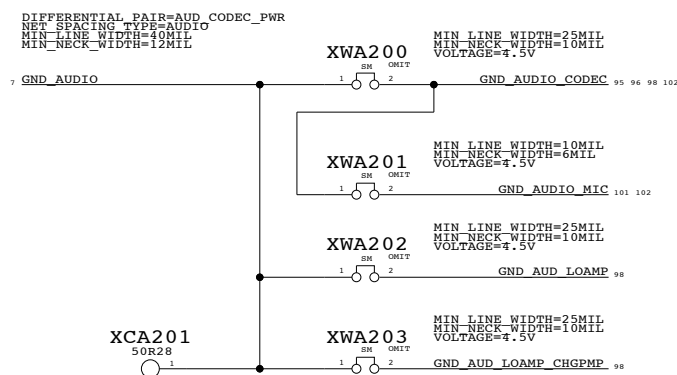
5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP



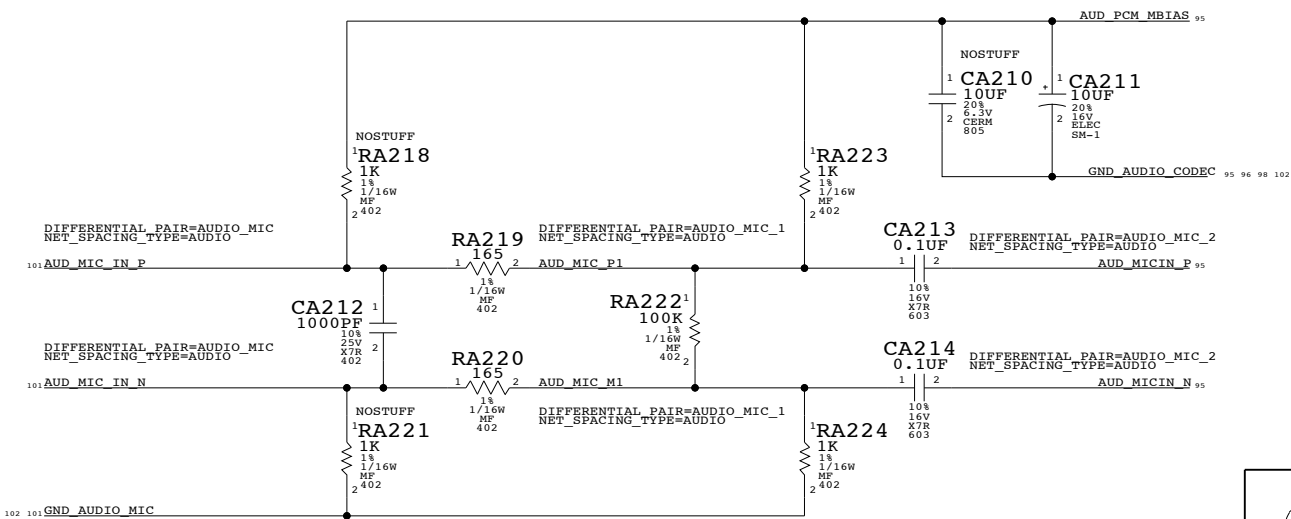
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



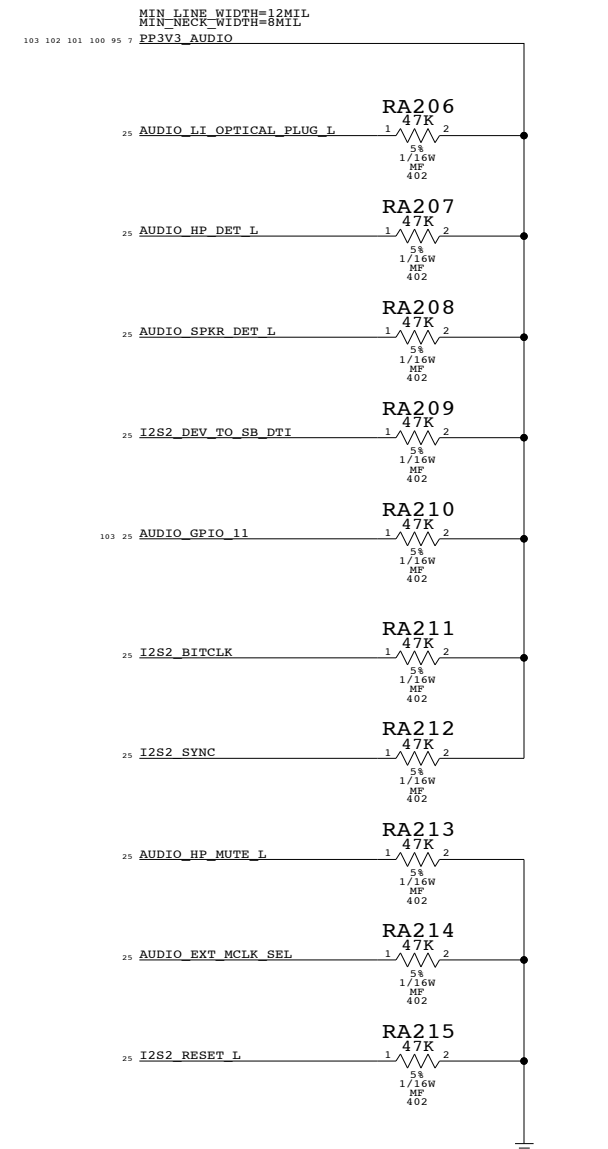
AUDIO GROUND RETURNS



MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: Q45 POWER SUPPLIES

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	D	051-6482	C
SCALE	NONE	SHT OF	102 OF 103

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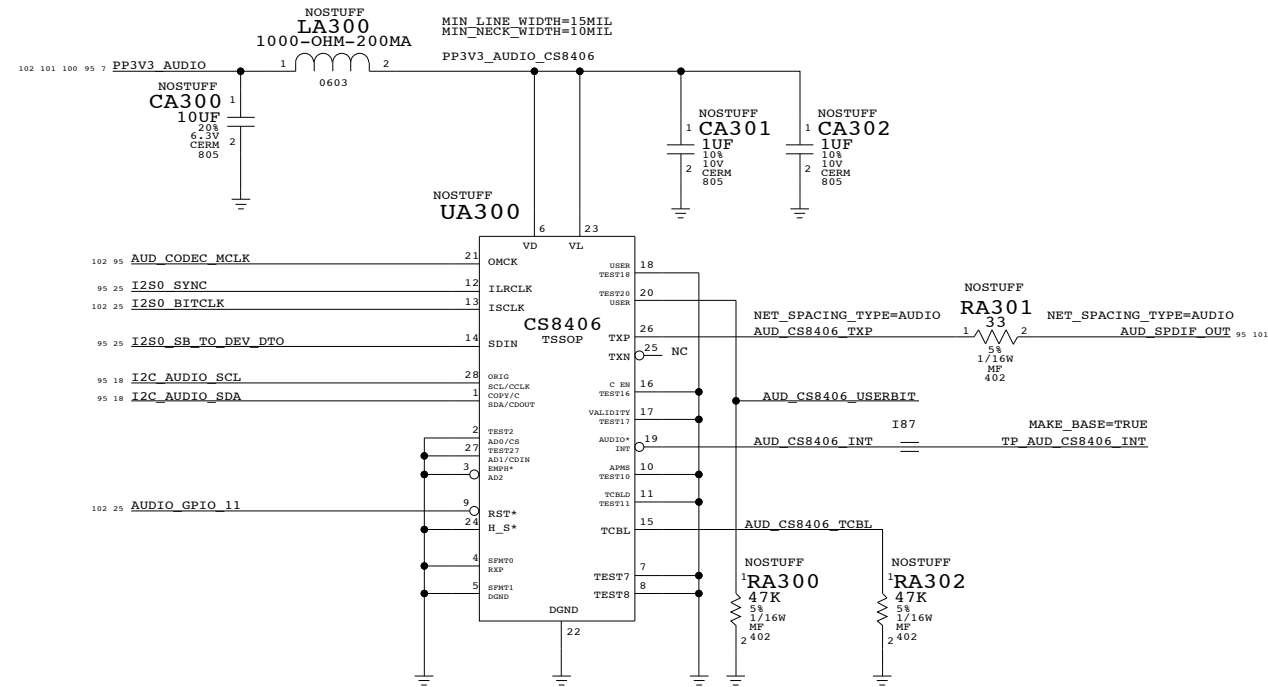
B

B

A

A

S/PDIF TRANSMITTER
I2C ADDRESS = 0010 000X
 APPLE P/N 353S0597



AUDIO: S/PDIF XMITTER

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SCALE	NONE	SHT OF	103 OF 103