1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

FINO M23
PROTO2

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
08		381734	ENGINEERING RELEASED	05/19/05	?

5/19/05

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram		FINO-DD	MASTER
3	4	Power Block Diagram		FINO-PC	05/18/2005
4	5	Table Items		FINO-DD	MASTER
5	6	FUNC TEST 1 OF 2		FINO-ME	05/18/2005
6	7	Power Conn / Alias		M23-PC	05/18/2005
7	8	Signal Alias		FINO-DD	MASTER
8	9	FUNC TEST 2 OF 2		FINO-ME	05/18/2005
9	11	1.8V Vreg		M23-PC	05/18/2005
10	12	1.5V Vreg		FINO-PC	05/18/2005
11	13	1.2V Vreg		FINO-PC	05/18/2005
12	15	2.5V Vreg		FINO-PC	05/18/2005
13	16	5V & 3.3V Fets		FINO-PC	05/18/2005
14	17	Vesta Core / Misc		FINO-HC	05/18/2005
15	19	KODIAK CORE & BYPASS		Q63	05/18/2005
16	20	KODIAK & SHASTA MISC		FINO-ME	05/18/2005
17	23	Shasta Core Power		Q63	05/18/2005
18	24	Shasta Serial / Misc		FINO-ME	05/18/2005
19	25	PULSAR2 POWER		Q63	05/18/2005
20	26	PULSAR2 CLOCKS		FINO-ME	05/18/2005
21	27	Pulsar Aliases		FINO-ME	05/18/2005
22	28	System Management Unit		Q63	05/18/2005
23	29	SMU SUPPLEMENTAL (2)		FINO-MS	05/18/2005
24	30	SMU SUPPLEMENTAL (3)		FINO-MS	05/18/2005
25	31	SMU SUPPLEMENTAL (4)		FINO-MS	05/18/2005
26	32	Fan 0, 1 & System Temp		FINO-PC	05/18/2005
27	33	Fan 2 & HD Temp		FINO-PC	05/18/2005
28	39	I2C Connections		FINO-ME	05/18/2005
29	41	KODIAK EI PWR & CAPS		Q63	05/18/2005
30	42	KODIAK EI A		Q63	05/18/2005
31	43	CPU EI AND IO		FINO-MS	05/18/2005
32	44	KODIAK EI B		Q63	05/18/2005
33	47	CPU STRAPS		FINO-MS	05/18/2005
34	48	CPU POWER AND BYPASS		FINO-MS	05/18/2005
35	49	PROC DECOUPLING		FINO-MS	05/18/2005
36	50	CPU VCORE VREG		M23-MS	05/18/2005
37	52	CPU VCORE MORE BYPASS		FINO-MS	05/18/2005
38	54	CPU AVDD VREG		FINO-MS	05/18/2005
39	55	T,V,I SENSORS		FINO-MS	05/18/2005
40	56	CPU ALIASES & MISC		FINO-MS	05/18/2005
41	58	KODIAC NBMEM PWR & CAPS		Q63	05/18/2005
42	59	Kodiak Memory Dq/Ctl		FINO-RT	05/18/2005
43	61	Parallel Term		FINO-RT	05/18/2005
44	62	Main Memory Clock Buffer		FINO-RT	05/18/2005
45	63	MEMORY ADDR BRANCHING		FINO-EG	05/18/2005
46	67	Memory Dimm A		FINO-RT	05/18/2005
47	68	MLB Mem Series Term		FINO-RT	05/18/2005
48	69	On-Board DDR SDRAM		FINO-RT	05/18/2005
49	70	On-Board DDR SDRAM		FINO-RT	05/18/2005
50	82	KODIAK PCI-E X16		Q63	05/18/2005
51	84	GPU PCIe		FINO-DD	MASTER
52	85	Graphics Vregs		M23-DD	MASTER
53	86	GPU Core Power		FINO-DD	MASTER
54	87	GPU Frame Buffer		FINO-DD	MASTER
55	88	FB Series Termination		FINO-DD	MASTER
56	89	GPU GDDR SDRAM A		FINO-DD	MASTER
57	90	GPU GDDR SDRAM B		FINO-DD	MASTER
58	92	GPU Straps		FINO-DD	MASTER
59	93	GPU DVI & DACs		FINO-DD	MASTER
60	96	TMDS/Inverter/ExtVGA		M23-DD	MASTER
61	97	KODIAK PCI-E CONST		FINO-DD	MASTER
62	98	KODIAK HT16		Q63	05/18/2005
63	101	HT ALIASES		FINO-EG	05/18/2005
64	103	Shasta HyperTransport		Q63	05/18/2005
65	119	Shasta PCI Interface		Q63	05/18/2005
66	120	PCI SERIES TERMINATION		FINO-EG	05/18/2005
67	121	AIRPORT & BLUETOOTH		FINO-EG	05/18/2005
68	122	USB 2.0 PCI Interface		Q63	05/18/2005
69	125	BootROM		Q63	05/18/2005
70	127	Shasta Disk		M23-MB	05/18/2005
71	129	Disk Connectors		M23-MB	05/18/2005
72	130	ENET SERIES TERM		FINO-HC	05/18/2005
73	131	Shasta Ethernet		Q63	05/18/2005
74	132	Vesta Ethernet PHY		Q63	05/18/2005
75	136	ETHERNET CONNECTOR		FINO-HC	05/18/2005
76	138	Shasta FireWire		Q63	05/18/2005
77	139	Vesta FireWire PHY		Q63	05/18/2005
78	140	FIREWIRE CONNECTORS		FINO-HC	05/18/2005
79	142	USB Host Interfaces		Q63	05/18/2005
80	143	USB Device Interfaces		FINO-MB	05/18/2005
81	144	Flash Media Ctrl		FINO-PC	05/18/2005
82	145	Flash Connector		FINO-PC	05/18/2005
83	147	AUDIO: CODEC		FINO-SO	05/18/2005
84	148	AUDIO: LINE INPUT AMP		FINO-SO	05/18/2005
85	150	AUDIO: LINE OUT AMP		FINO-SO	05/18/2005
86	152	AUDIO: SPEAKER AMP		FINO-SO	05/18/2005
87	153	AUDIO: CONNECTORS		FINO-SO	05/18/2005
88	154	AUDIO: POWER SUPPLIES		FINO-SO	05/18/2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK
ENG APPD / MFG APPD
QA APPD / DESIGNER
RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

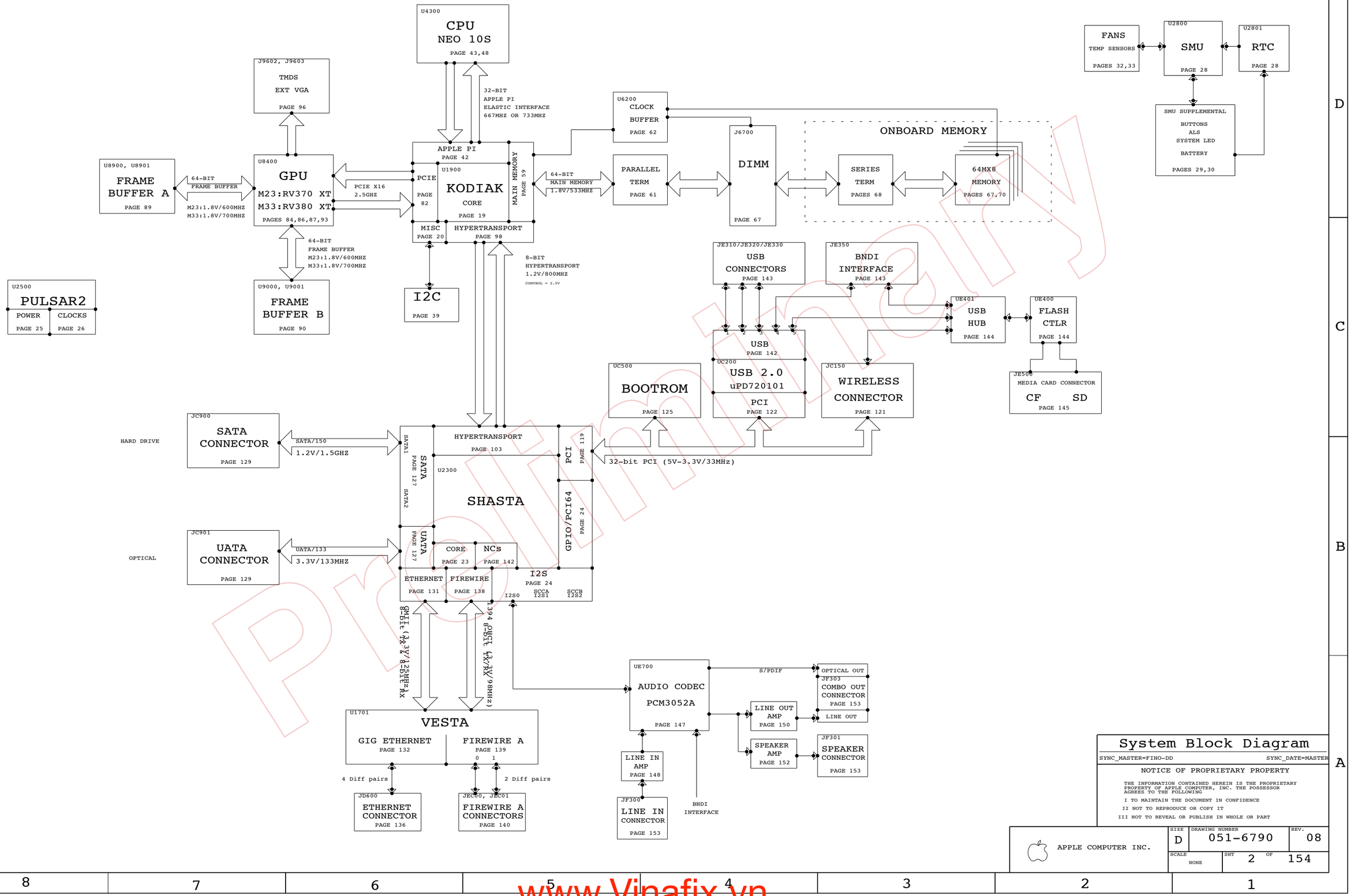
SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,FINO,M23

DRAWING NUMBER 051-6790 REV. 08

SHT 1 OF 154



System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	2	154

POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP12V_ALL	PP12V_RUN	PP5V_RUN	PP5V_ALL	PP3V3_ALL	PP3V3_RUN
FW CONN	20" PANEL POWER 17" LCD INVERTER	OPTICAL			PCI BUS AUDIO CODEC

SYS_POWERUP_L

SMU
POWER SEQUENCE PIN

NC_SMU_PWRSEQ_P1_0 — SMU_PWRSEQ_P1_0
NC_SMU_PWRSEQ_P1_4 — SMU_PWRSEQ_P1_4
TURN_ON_PP1V2_L — SMU_PWRSEQ_P1_1
PP3V3_PWRON
PWR_GOOD_PP1V2 — SMU_PWRSEQ_P9_5
PWR_GOOD_PP1V8 — SMU_PWRSEQ_P9_6
TURN_ON_PP3V3_PWRON_L — SMU_PWRSEQ_P1_2
SMU_PWRSEQ_P1_3

PP1V5_PWRON SWITCHER
PAGE 12
PULSAR
KODIAK CORE

PP1V5_RUN FET SWITCH
PAGE 12
EI

GPU CORE SWITCHER
PAGE 85

CPU CORE SWITCHER
PAGE 50

PP1V8_PWRON SWITCHER
PAGE 11
MAIN MEMORY

PP1V8_RUN
PP1V8_RUN POWER SW
PAGE 11
GPU MEMORY

PP0V9_GPU_VTT LINEAR
PAGE 91

PP4V5_RUN_AUDIO LINEAR
PAGE 154
AUDIO CODEC

PP5V_PWRON FET SWITCH
PAGE 16
USB CONN

PP3V3_PWRON FET SWITCH
PAGE 16
MODEM & BT
USB2 HOST

PP2V5_ALL LINEAR
PAGE 15
VESTA

PP2V5_PWRON FET SWITCH
PAGE 15

PP2V5_RUN FET SWITCH
PAGE 15

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 54

PP2V5_GPU_A2VDD LINEAR
PAGE 85

PP1V8_TPVDD LINEAR
PAGE 85

PP1V5_VDDC_CT LINEAR
PAGE 85

PP1V8_GPU LINEAR
PAGE 85

PP1V2_ALL SWITCHER
PAGE 13
VESTA CORE

PP1V2_TPVDD LINEAR
PAGE 85

PP1V2_PWRON FET SWITCH
PAGE 13
SHASTA CORE

PP1V2_RUN FET SWITCH
PAGE 13
HT BUS

PP1V2_PWRON

PP2V5_ALL
R431 10K 5% 1/16W MF-LF 402

PS_1V_REF
R430 100K 5% 1/16W MF-LF 402
COMPARE_PP1V2
C430 0.01UF 20% 16V CERM 402
LM339A SOI-LF
U400 V+ GND

PP2V5_ALL
R442 150K 5% 1/16W MF-LF 402
PS_1V_REF
R443 100K 1% 1/16W MF-LF 402

PP5V_ALL
LM339A SOI-LF
U400 V+ GND

PP2V5_ALL
R441 10K 5% 1/16W MF-LF 402

R440 100K 5% 1/16W MF-LF 402
COMPARE_PP1V8
C440 0.01UF 20% 16V CERM 402
C441 0.1UF 20% 10V CERM 402

PP2V5_ALL
U400P2
LM339A SOI-LF
U400 V+ GND

Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 4 OF 154	

PROCESSORS

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3158	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,CQA	2.0GHZ	1.15V	46W	50MV	U4300	CPU_2_0GHZ
337S3157	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.2G,85C,FQA	2.2GHZ	1.15V	51W	50MV	U4300	CPU_2_2GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3165	337S3158	CPU_2_0GHZ	U4300	IC,DD3.1,2.0G,CJA	1.20V
337S3164	337S3157	CPU_2_2GHZ	U4300	IC,DD3.1,2.0G,FJA	1.20V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0371	1	IC,KODIAK,V1.1,PBGA,200MM	U1900	
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	
343S0324	1	IC,ASIC,VESTA,V1.3	U1701	
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
825-6447	1	BARCODE LABEL, MLB	LBL1	
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500	
341T1752	1	PURCH ASSY, SMU BIG	U2800	
603-7318	1	M23 CPU HEATSINK	MECH1	17_INCH_LCD
603-7321	1	M33 CPU HEATSINK	MECH1	20_INCH_LCD
603-7322	1	M33 GPU HEATSINK	MECH2	20_INCH_LCD
875-1614	1	CPU GAP FILLER	GAP1	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702	KINGBRIGHT LED
376S0204	376S0130		Q5010,Q5020	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q5011,Q5021	MOSFET,N-CH,VISHAY

Table Items

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 5 OF 154

NO TEST XW NETS

D17	NO_TEST=YES	GND_U1100	11
D18	NO_TEST=YES	GND_U1200	12
D19	NO_TEST=YES	GND_U1300	13
D35	NO_TEST=YES	PP_2V5PWRONNBMISC	20
D37	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
D39	NO_TEST=YES	PP_3V3PWRONSBPCI64	23
D55	NO_TEST=YES	PP_2V5PWRONSB	23
D56	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
D84	NO_TEST=YES	PP_OVDD_PULSAR1	25
D85	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
D86	NO_TEST=YES	PP_1V5PULSAR2	25
D87	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
D88	NO_TEST=YES	GND_SMU_AVSS	28 55
D89	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
D90	NO_TEST=YES	PP_3V3ALLSMU	28
D91	NO_TEST=YES	PP_VEINB	41
D92	NO_TEST=YES	GND_CPU_AVDD	48
D93	NO_TEST=YES	VC_AGND	50
D94	NO_TEST=YES	VC_OUTSEN_R	50
D95	NO_TEST=YES	KPVDD2_FMAX	55
D96	NO_TEST=YES	GND_GPU_PVSS	86
D97	NO_TEST=YES	GND_GPU_MPVSS	87
D98	NO_TEST=YES	GND_AUDIO_MIC	153 154

D99	NO_TEST=YES	GND_GPU_TPVSS	93
D100	NO_TEST=YES	GND_GPU_TXVSSR	93
D99	NO_TEST=YES	GND_GPU_VSSDI	93
D100	NO_TEST=YES	GND_GPU_AVSSN	93
D100	NO_TEST=YES	GND_GPU_AVSSQ	93
D100	NO_TEST=YES	GND_GPU_A2VSSN	93
D100	NO_TEST=YES	GND_GPU_A2VSSQ	93
D100	NO_TEST=YES	KOD_L15_GND	98 101
D100	NO_TEST=YES	PP_3V3SBPCI_B9	119
D100	NO_TEST=YES	PP_2V5PWRONSB_B9	119
D100	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
D101	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
D101	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
D101	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
D101	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
D100	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
D100	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
D100	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
D101	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
D101	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
D101	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
D101	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
D101	NO_TEST=YES	GND_AUD_LOAMP	150 154

D101	NO_TEST=YES	GND_NEC_AVSS_R	142
D101	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
D101	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
D101	NO_TEST=YES	KPGND2_FMAX	55
D101	NO_TEST=YES	TDIODE_POS_FMAX	55
D101	NO_TEST=YES	TDIODE_NEG_FMAX	55
D101	NO_TEST=YES	DAGND	55
D101	NO_TEST=YES	INA138_OUT	55
D102	NO_TEST=YES	RAMCLK_AVSS	62
D102	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
D102	NO_TEST=YES	GND_AUDIO	7 154
D102	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
D103	NO_TEST=YES	KOD_H05_GND	82 97
D103	NO_TEST=YES	KOD_K07_GND	82 97
D103	NO_TEST=YES	KOD_G10_GND	82 97
D103	NO_TEST=YES	KOD_J13_GND	82 97
D103	NO_TEST=YES	KOD_L13_GND	82 97
D103	NO_TEST=YES	KOD_H08_GND	82 97
D103	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
D103	NO_TEST=YES	U8500_GND	85
D103	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

D955	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
D957	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
D958	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
D959	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
D960	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
D961	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
D962	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
D963	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
D964	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
D965	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56
D969	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
D971	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
D972	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
D973	NO_TEST=YES	NC_CPU_A1_QACK_L	56
D975	NO_TEST=YES	NC_CPU_B0_QACK_L	56
D974	NO_TEST=YES	NC_CPU_B1_QACK_L	56
D976	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
D978	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
D977	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
D982	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
D104	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
D104	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
D104	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
D104	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
D104	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
D104	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
D105	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
D105	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
D105	NO_TEST=YES	NC_A_AVREG_0	82
D105	NO_TEST=YES	NC_A_AVREG_1	82
D105	NO_TEST=YES	NC_A_AVREG_2	82
D105	NO_TEST=YES	NC_CPU_B_APSYNC	27
D105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
D106	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
D105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
D105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
D106	NO_TEST=YES	NC_J2904_11	29
D106	NO_TEST=YES	NC_J2904_12	29
D106	NO_TEST=YES	NC_NCV1009_1	55
D106	NO_TEST=YES	NC_NCV1009_2	55
D106	NO_TEST=YES	NC_NCV1009_3	55
D106	NO_TEST=YES	NC_NCV1009_4	55
D106	NO_TEST=YES	NC_NCV1009_5	55
D106	NO_TEST=YES	NC_NCV1009_ADJ	55
D106	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
D107	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
D107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
D107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4
D116	NO_TEST=YES	RFBD<38>	88 89
D116	NO_TEST=YES	RFBD<37>	88 89
D116	NO_TEST=YES	RFBD<36>	88 89
D116	NO_TEST=YES	RFBD<34>	88 89
D116	NO_TEST=YES	RFBD<33>	88 89
D116	NO_TEST=YES	RFBD<32>	88 89
D116	NO_TEST=YES	RFBD<31>	88 89
D116	NO_TEST=YES	RFBD<30>	88 89
D117	NO_TEST=YES	RFBD<28>	88 89
D117	NO_TEST=YES	RFBD<27>	88 89
D117	NO_TEST=YES	RFBD<26>	88 89
D117	NO_TEST=YES	RFBD<25>	88 89
D117	NO_TEST=YES	RFBD<23>	88 89
D117	NO_TEST=YES	RFBD<22>	88 89
D117	NO_TEST=YES	RFBD<21>	88 89

D109	NO_TEST=YES	KPVDD2	48 50 55
D109	NO_TEST=YES	KPGND2	48 50 55
D109	NO_TEST=YES	CPU_DIODE_POS	48 55
D109	NO_TEST=YES	CPU_DIODE_NEG	48 55
D110	NO_TEST=YES	FMAXT_P	55
D110	NO_TEST=YES	FMAXT_M	55
D110	NO_TEST=YES	CORE_ISNS_P	55
D110	NO_TEST=YES	CORE_ISNS_M	55
D110	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
D110	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
D110	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
D110	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
D110	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
D110	NO_TEST=YES	NC_I2S2_MCLK	154
D111	NO_TEST=YES	NC_SATA_RXD_N2_C	129
D111	NO_TEST=YES	NC_SATA_RXD_P2_C	129
D111	NO_TEST=YES	NC_SATA_TXD_N2	129
D111	NO_TEST=YES	NC_SATA_TXD_P2	129
D111	NO_TEST=YES	TP_SB<29>	142
D111	NO_TEST=YES	TP_SB<28>	142
D111	NO_TEST=YES	TP_SB<27>	142
D111	NO_TEST=YES	TP_SB<26>	142
D111	NO_TEST=YES	TP_SB<25>	142
D112	NO_TEST=YES	TP_SB<24>	142
D112	NO_TEST=YES	TP_SB<23>	142
D112	NO_TEST=YES	TP_SB<22>	142
D112	NO_TEST=YES	TP_SB<21>	142
D112	NO_TEST=YES	TP_SB<20>	142
D112	NO_TEST=YES	TP_SB<19>	142
D112	NO_TEST=YES	TP_SB<18>	142
D112	NO_TEST=YES	TP_SB<17>	142
D112	NO_TEST=YES	TP_SB<16>	142
D112	NO_TEST=YES	TP_SB<15>	142
D113	NO_TEST=YES	TP_SB<14>	142
D113	NO_TEST=YES	TP_SB<13>	142
D113	NO_TEST=YES	TP_SB<12>	142
D113	NO_TEST=YES	TP_SB<11>	142
D113	NO_TEST=YES	TP_SB<10>	142
D113	NO_TEST=YES	TP_SB<9>	142
D113	NO_TEST=YES	TP_SB<8>	142
D113	NO_TEST=YES	TP_SB<7>	142
D113	NO_TEST=YES	TP_SB<6>	142
D113	NO_TEST=YES	TP_SB<5>	142
D114	NO_TEST=YES	TP_SB<4>	142
D114	NO_TEST=YES	TP_SB<3>	142
D114	NO_TEST=YES	TP_SB<2>	142
D114	NO_TEST=YES	TP_SB<1>	142
D114	NO_TEST=YES	TP_SB<0>	142
D115	NO_TEST=YES	RFBD<61>	88 89
D115	NO_TEST=YES	RFBD<60>	88 89
D115	NO_TEST=YES	RFBD<59>	88 89
D117	NO_TEST=YES	RFBD<57>	88 89
D118	NO_TEST=YES	RFBD<56>	88 89
D118	NO_TEST=YES	RFBD<54>	88 89
D118	NO_TEST=YES	RFBD<53>	88 89
D118	NO_TEST=YES	RFBD<52>	88 89
D118	NO_TEST=YES	RFBD<50>	88 89
D118	NO_TEST=YES	RFBD<49>	88 89
D118	NO_TEST=YES	RFBD<48>	88 89
D118	NO_TEST=YES	RFBD<47>	88 89
D119	NO_TEST=YES	RFBD<45>	88 89
D119	NO_TEST=YES	RFBD<44>	88 89
D119	NO_TEST=YES	RFBD<42>	88 89
D119	NO_TEST=YES	RFBD<41>	88 89
D119	NO_TEST=YES	RFBD<40>	88 89

D119	NO_TEST=YES	RFBD<126>	88 90
D120	NO_TEST=YES	RFBD<125>	88 90
D119	NO_TEST=YES	RFBD<124>	88 90
D120	NO_TEST=YES	RFBD<122>	88 90
D120	NO_TEST=YES	RFBD<121>	88 90
D120	NO_TEST=YES	RFBD<120>	88 90
D120	NO_TEST=YES	RFBD<118>	88 90
D120	NO_TEST=YES	RFBD<117>	88 90
D120	NO_TEST=YES	RFBD<116>	88 90
D121	NO_TEST=YES	RFBD<114>	88 90
D121	NO_TEST=YES	RFBD<113>	88 90
D121	NO_TEST=YES	RFBD<112>	88 90
D121	NO_TEST=YES	RFBD<110>	88 90
D121	NO_TEST=YES	RFBD<109>	88 90
D121	NO_TEST=YES	RFBD<108>	88 90
D121	NO_TEST=YES	RFBD<106>	88 90
D122	NO_TEST=YES	RFBD<105>	88 90
D121	NO_TEST=YES	RFBD<104>	88 90
D122	NO_TEST=YES	RFBD<102>	88 90
D122	NO_TEST=YES	RFBD<101>	88 90
D122	NO_TEST=YES	RFBD<100>	88 90
D122	NO_TEST=YES	RFBD<98>	88 90
D122	NO_TEST=YES	RFBD<97>	88 90
D122	NO_TEST=YES	RFBD<96>	88 90
D122	NO_TEST=YES	RFBD<95>	88 90
D123	NO_TEST=YES	RFBD<94>	88 90
D123	NO_TEST=YES	RFBD<92>	88 90
D123	NO_TEST=YES	RFBD<91>	88 90
D123	NO_TEST=YES	RFBD<90>	88 90
D123	NO_TEST=YES	RFBD<88>	88 90
D123	NO_TEST=YES	RFBD<87>	88 90
D123	NO_TEST=YES	RFBD<86>	88 90
D123	NO_TEST=YES	RFBD<85>	88 90
D124	NO_TEST=YES	RFBD<83>	88 90
D124	NO_TEST=YES	RFBD<82>	88 90
D124	NO_TEST=YES	RFBD<81>	88 90
D124	NO_TEST=YES	RFBD<79>	88 90
D124	NO_TEST=YES	RFBD<78>	88 90
D124	NO_TEST=YES	RFBD<76>	88 90
D124	NO_TEST=YES	RFBD<75>	88 90
D125	NO_TEST=YES	RFBD<74>	88 90
D125	NO_TEST=YES	RFBD<72>	88 90
D125	NO_TEST=YES	RFBD<71>	88 90
D125	NO_TEST=YES	RFBD<70>	88 90
D125	NO_TEST=YES	RFBD<69>	88 90
D125	NO_TEST=YES	RFBD<67>	88 90
D125	NO_TEST=YES	RFBD<66>	88 90
D125	NO_TEST=YES	RFBD<65>	88 90
D126	NO_TEST=YES	RFBD<62>	88 89

D10	NO_TEST=YES	TP_FBBCS1_L	87
D82	NO_TEST=YES	AUD_4V5_FB	154
D83	NO_TEST=YES	ITS_RUNNING	7
D82	NO_TEST=YES	LED801_1	8
D83	NO_TEST=YES	LED802_1	8
D84	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
D84	NO_TEST=YES	Q800_D	8
D84	NO_TEST=YES	Q800_G	8
D84	NO_TEST=YES	Q801_B	8
D84	NO_TEST=YES	Q802_B	8
D85	NO_TEST=YES	Q802_E	8
D85	NO_TEST=YES	Q803_B	8
D42	NO_TEST=YES	TP_USB2_PWREN<0>	143
D42	NO_TEST=YES	TP_USB2_PWREN<1>	143
D87	NO_TEST=YES	TP_SB_FSTEST	24
D87	NO_TEST=YES	TP_SB_PLLTEST	24
D34	NO_TEST=YES	TP_USB2_PWREN<2>	143
D35	NO_TEST=YES	TP_USB2_PWREN<3>	143
D34	NO_TEST=YES	TP_USB2_PWREN<4>	143
D35	NO_TEST=YES	TP_NEC_NTEST1	122
D35	NO_TEST=YES	TP_NEC_SMC	122
D35	NO_TEST=YES	TP_NEC_SMI_L	122
D36	NO_TEST=YES	TP_NEC_SRCLK	122
D36	NO_TEST=YES	TP_NEC_SRMOD	122
D36	NO_TEST=YES	TP_NEC_TEST	122
D88	NO_TEST=YES	UATA_DASP_L_DS	129
D129	NO_TEST=YES	RFBD<19>	88 89
D129	NO_TEST=YES	RFBD<18>	88 89
D128	NO_TEST=YES	RFBD<16>	88 89
D128	NO_TEST=YES	RFBD<15>	88 89
D128	NO_TEST=YES	RFBD<14>	88 89
D128	NO_TEST=YES	RFBD<13>	88 89
D127	NO_TEST=YES	RFBD<11>	88 89
D127	NO_TEST=YES	RFBD<10>	88 89
D127	NO_TEST=YES	RFBD<8>	88 89
D127	NO_TEST=YES	RFBD<7>	88 89
D127	NO_TEST=YES	RFBD<6>	88 89
D127	NO_TEST=YES	RFBD<5>	88 89
D127	NO_TEST=YES	RFBD<3>	88 89
D126	NO_TEST=YES	RFBD<2>	88 89
D126	NO_TEST=YES	RFBD<1>	88 89
D126	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
D129	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<39>	61 68 70
D130	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
D131	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
D131	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
D131	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
D131	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
D131	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
D131	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
D131	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
D131	NO_TEST=YES	RAM_DQ_R<26>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
D132	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
D133	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
D133	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
D133	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
D133	NO_TEST=YES	RAM_DQ_R<11>	61 68 69

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

D108	FUNC_TEST=TRUE	PPVCORE_CPU	50
D108	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
D108	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
D105	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
D105	FUNC_TEST=TRUE	POWER_BUTTON_L	29
D105	FUNC_TEST=TRUE	RESET_BUTTON_L	29
D105	FUNC_TEST=TRUE	SMU_RESET_L	28 29
D105	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

D138	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
D138	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
D138	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
D138	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
D138	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
D138	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
D105	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29

PP1V2_ALL PP3V3_ALL PP5V_ALL

7 PP1V2_ALL FUNC_TEST=TRUE
7 PP3V3_ALL FUNC_TEST=TRUE
7 PP5V_ALL FUNC_TEST=TRUE

PP1V8_RUN PP2V5_RUN PP3V3_RUN PP12V_RUN

7 PP1V8_RUN FUNC_TEST=TRUE
7 PP2V5_RUN FUNC_TEST=TRUE
7 PP3V3_RUN FUNC_TEST=TRUE
7 PP12V_RUN FUNC_TEST=TRUE

PP1V5_PWRON

7 PP1V5_PWRON FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

D134	NO_TEST=YES	RAM_DQ_R<10>	61 68 69
D134	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
D134	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
D134	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
D134	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
D135	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
D134	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
D135	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

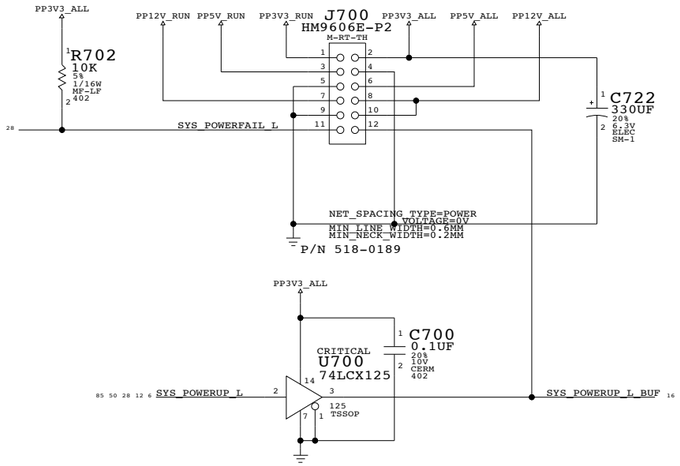
NOTICE OF PROPRIETARY PROPERTY

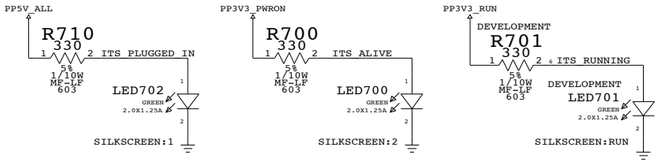
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

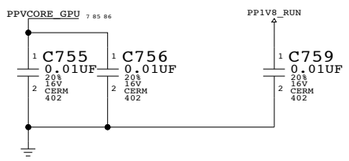
APPLE COMPUTER INC.

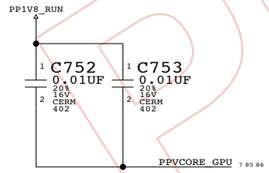
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 6 OF 154	

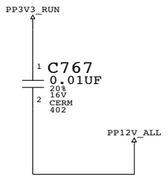




PLANE STICHING CAPS

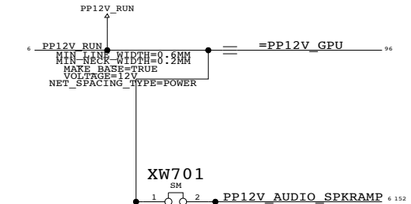


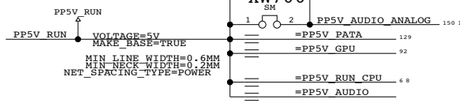


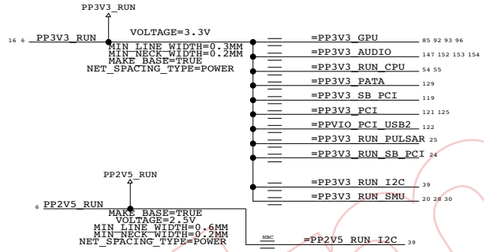


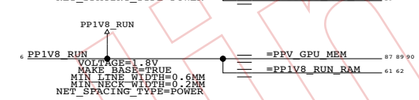
RUN RAILS

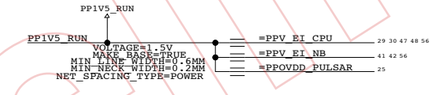
ONLY ON IN RUN

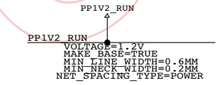






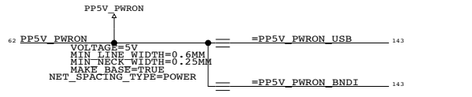


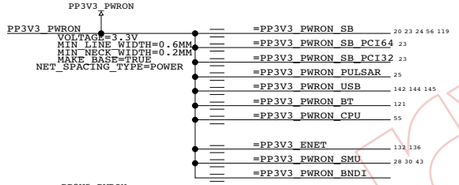


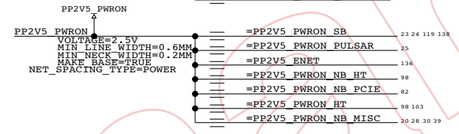


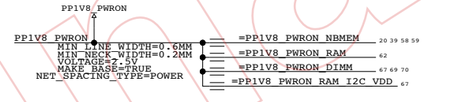
PWRON RAILS

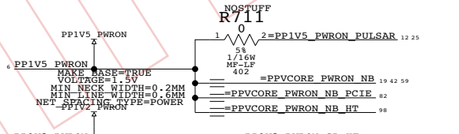
ON IN RUN AND SLEEP

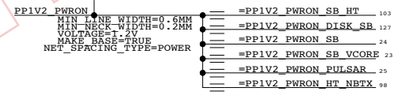


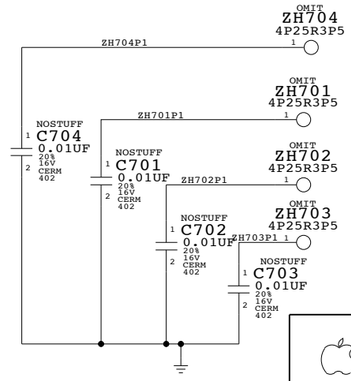






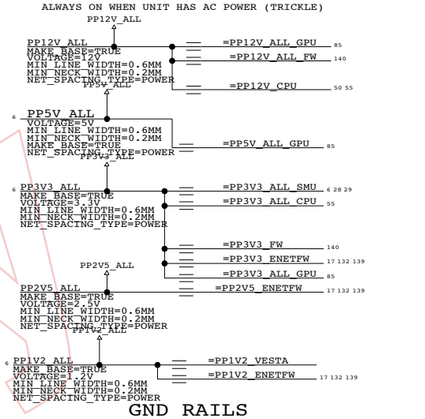




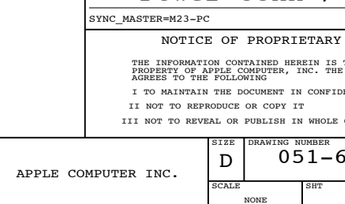


ALL RAILS

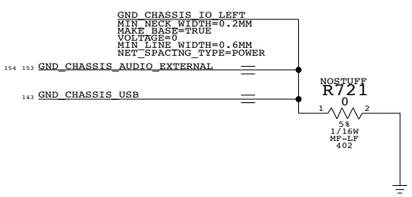
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

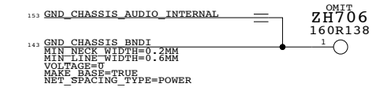


GND RAILS



CHASSIS GND





Power Conn / Alias

SYNC_MASTER=M23-PC SYNC_DATE=05/18/2005

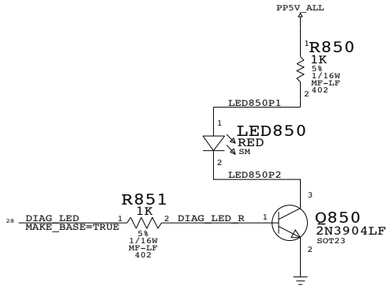
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

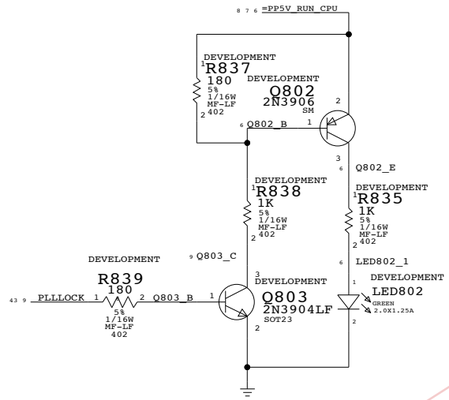
SCALE	SHT	OF
NONE	7	154

DIAG LED

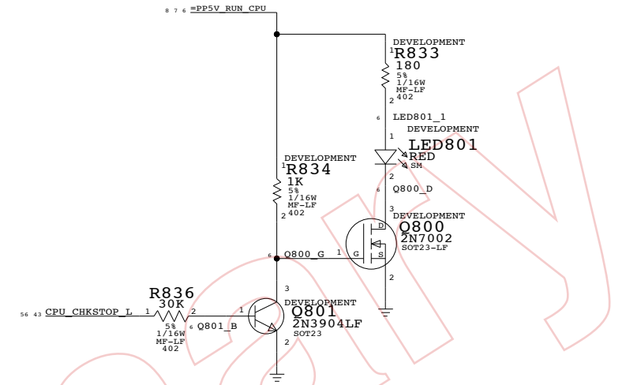
(OVERTEMP LED)



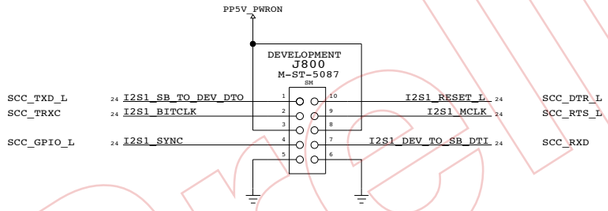
PLL LOCK LED



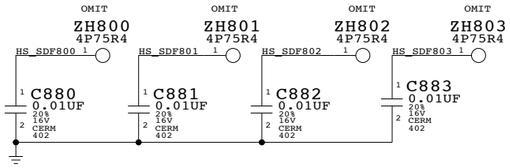
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 8 OF 154	

8	7	6	5	4	3	2	1

D

C

B

A

E1	NO_TEST=YES	ENET_TXD_R<7>	130 131
E2	NO_TEST=YES	ENET_TXD_R<6>	130 131
E3	NO_TEST=YES	ENET_TXD_R<5>	130 131
E4	NO_TEST=YES	ENET_TXD_R<4>	130 131
E5	NO_TEST=YES	ENET_TXD_R<3>	130 131
E6	NO_TEST=YES	ENET_TXD_R<2>	130 131
E7	NO_TEST=YES	ENET_TXD_R<1>	130 131
E8	NO_TEST=YES	ENET_TXD_R<0>	130 131
E9	NO_TEST=YES	ENET_TXD<7>	130 131 132
E10	NO_TEST=YES	ENET_TXD<6>	130 131 132
E12	NO_TEST=YES	ENET_TXD<5>	130 131 132
E11	NO_TEST=YES	ENET_TXD<4>	130 131 132
E13	NO_TEST=YES	ENET_TXD<3>	130 131 132
E14	NO_TEST=YES	ENET_TXD<2>	130 131 132
E15	NO_TEST=YES	ENET_TXD<1>	130 131 132
E16	NO_TEST=YES	ENET_TXD<0>	130 131 132
E18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
E17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
E19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
E20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
E21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
E22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
E24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
E23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
E25	NO_TEST=YES	ENET_RXD<7>	130 131
E26	NO_TEST=YES	ENET_RXD<6>	130 131
E27	NO_TEST=YES	ENET_RXD<5>	130 131
E28	NO_TEST=YES	ENET_RXD<4>	130 131
E30	NO_TEST=YES	ENET_RXD<3>	130 131
E29	NO_TEST=YES	ENET_RXD<2>	130 131
E31	NO_TEST=YES	ENET_RXD<1>	130 131
E32	NO_TEST=YES	ENET_RXD<0>	130 131
E33	NO_TEST=YES	ENET_TX_EN_R	130 131
E34	NO_TEST=YES	ENET_TX_ER_R	130 131
E36	NO_TEST=YES	ENET_TX_EN	130 131 132
E35	NO_TEST=YES	ENET_TX_ER	130 131 132
E37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
E38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
E39	NO_TEST=YES	NC_CPU_AFN	56
E40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
E42	NO_TEST=YES	NC_PSRO	56
E41	NO_TEST=YES	NC_PSRO_ENABLE	56
E43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
E44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
E45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
E46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
E48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
E47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
E49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
E50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
E51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
E52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
E54	NO_TEST=YES	NC_SMU_SER_SEL	31
E53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
E55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
E56	NO_TEST=YES	TP_VESTA_AN_EN	132
E57	NO_TEST=YES	TP_VESTA_DNC_C9	17
E58	NO_TEST=YES	TP_VESTA_DNC_E9	17
E60	NO_TEST=YES	TP_VESTA_EN_10B	132
E59	NO_TEST=YES	TP_VESTA_ER	132
E61	NO_TEST=YES	TP_VESTA_F1000	132
E62	NO_TEST=YES	TP_VESTA_FDX	132
E63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
E64	NO_TEST=YES	TP_VESTA_HUB	132
E66	NO_TEST=YES	TP_VESTA_LINK1_L	132
E65	NO_TEST=YES	TP_VESTA_LINK2_L	132
E67	NO_TEST=YES	TP_VESTA_MANMS	132
E68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
E69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
E70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
E72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
E71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
E73	NO_TEST=YES	TP_VESTA_RBC0	132
E74	NO_TEST=YES	TP_VESTA_RBC1	132
E75	NO_TEST=YES	TP_VESTA_REGCTL1	17
E76	NO_TEST=YES	TP_VESTA_REGCTL2	17
E78	NO_TEST=YES	TP_VESTA_REGSEN1	17
E77	NO_TEST=YES	TP_VESTA_REGSEN2	17
E79	NO_TEST=YES	TP_VESTA_REGSUP1	17
E80	NO_TEST=YES	TP_VESTA_REGSUP2	17
E81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
E82	NO_TEST=YES	TP_VESTA_SPD0	132
E84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
E83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
E85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
E86	NO_TEST=YES	TP_VESTA_TEST<0>	132
E87	NO_TEST=YES	TP_VESTA_TEST<1>	132
E88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
E90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
E89	NO_TEST=YES	TP_VESTA_TVCO	132
E222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
E223	NO_TEST=YES	TP_VESTA_FAVDDL	139
E224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
E225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

E91	NO_TEST=YES	TP_VESTA_TVCO_24	139
E92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
E93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
E94	NO_TEST=YES	TP_NB_APSYNC	44
E95	NO_TEST=YES	TP_SB_WATCHDOG	24
E96	NO_TEST=YES	NC_CPU_TBEN_CLK	27
E97	NO_TEST=YES	NC_J3108_10	31
E98	NO_TEST=YES	NC_J3108_11	31
E99	NO_TEST=YES	NC_J3108_12	31
E100	NO_TEST=YES	NC_J3108_8	31
E101	NO_TEST=YES	NC_J3108_9	31
E102	NO_TEST=YES	NC_JTAGMUX_3	30
E103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

E109	NO_TEST=YES	Q803_C	8
E110	NO_TEST=YES	PLLLOCK	8 43

E111	NO_TEST=YES	LED_PP1V8_RUN_P	11
E112	NO_TEST=YES	LED_PP1V8_RUN_N	11
E113	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
E114	NO_TEST=YES	LED_PP1V5_RUN_N	12
E115	NO_TEST=YES	LED_PP1V5_RUN_P	12
E116	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
E120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
E121	NO_TEST=YES	LED_PP1V2_RUN_N	13
E122	NO_TEST=YES	LED_PP1V2_RUN_P	13
E124	NO_TEST=YES	KP_V<1>	55
E123	NO_TEST=YES	KP_V<2>	55
E125	NO_TEST=YES	CPU_SENSE_KP_V	55
E126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
E127	NO_TEST=YES	NB_PLL_OUT_TRG	59
E128	NO_TEST=YES	PP5V_T555	92
E130	NO_TEST=YES	T555_DISC	92
E129	NO_TEST=YES	T555_THRES	92
E131	NO_TEST=YES	T555_OUT	92
E132	NO_TEST=YES	T555_PWM	92
E133	NO_TEST=YES	PP3V3_GPU_TSENSE	
E134	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
E135	NO_TEST=YES	TSENSE_GPU_ADD0	93
E136	NO_TEST=YES	TSENSE_GPU_ADD1	93
E137	NO_TEST=YES	GPU_DIODE_PLUS	93
E138	NO_TEST=YES	GPU_DIODE_MINUS	93
E139	NO_TEST=YES	LED8700_P	136
E140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

E141	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
E142	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
E143	NO_TEST=YES	CPU_A_APSYNC_R	26
E144	NO_TEST=YES	CPU_B_APSYNC_R	26
E145	NO_TEST=YES	NB_APSYNC_R	26
E146	NO_TEST=YES	HT_SB_REFCLK_R	26
E147	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
E148	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
E149	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
E150	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
E151	NO_TEST=YES	NB_PMR_CLK_P_R	26
E152	NO_TEST=YES	NB_PMR_CLK_N_R	26
E153	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
E154	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
E155	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
E156	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
E157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
E158	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
E159	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
E160	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
E161	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
E162	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
E163	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
E164	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
E165	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
E166	NO_TEST=YES	QUA0_REF_25MHZ_R	26
E167	NO_TEST=YES	SB_CLK25M_SATA_R	26
E168	NO_TEST=YES	QUA1_REF_25MHZ_R	26
E169	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
E170	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
E171	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
E172	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

E177	NO_TEST=YES	100M_N<0>	82 97
E178	NO_TEST=YES	100M_P<0>	82 97
E179	NO_TEST=YES	CKA_N<0>	84 97
E180	NO_TEST=YES	CKA_P<0>	84 97
E177	NO_TEST=YES	HT_NB_N<0>	98 101
E178	NO_TEST=YES	HT_NB_P<0>	98 101
E179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
E180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
E185	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
E186	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
E187	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
E188	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
E189	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
E190	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
E191	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
E192	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
E193	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	82 84 97
E194	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	82 84 97
E195	NO_TEST=YES	UATA_DA<0>	127 129
E196	NO_TEST=YES	UATA_DD<1>	127 129
E197	NO_TEST=YES	UATA_DD<14>	127 129
E198	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	82 84 97
E199	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	82 84 97
E197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	82 97
E198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	82 97
E199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	82 84 97
E200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	82 84 97
E201	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	82 97
E202	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	82 97
E203	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	82 97
E204	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	82 97
E205	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	82 97
E206	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
E207	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
E208	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
E209	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
E210	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
E211	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
E212	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
E213	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
E214	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
E215	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
E216	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	43 56
E217	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	43 56
E218	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
E219	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
E220	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	43 56
E221	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

E226	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
E227	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
E228	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
E229	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
E230	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24

E232	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
E234	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
E233	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
E231	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
E235	FUNC_TEST=TRUE	JTAG_NB_TRST_L	

E237	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	
E240	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	
E239	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	
E242	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	
E241	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	

E244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
E246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
E245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
E243	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
E247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

FUNC TEST 2 OF 2

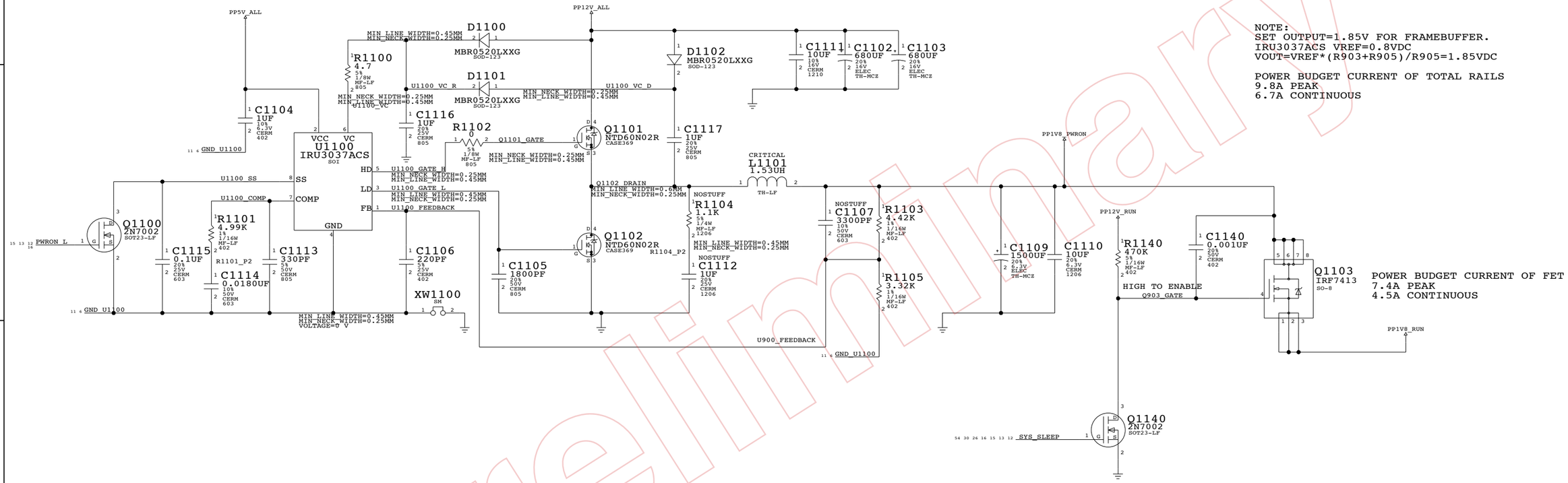
SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 9 OF 154

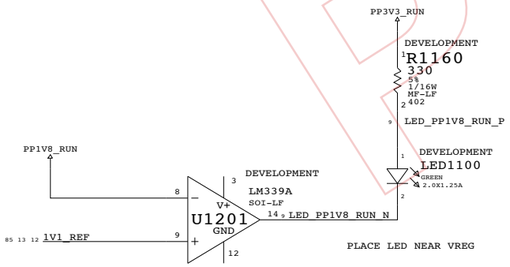
1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
9.8A PEAK
6.7A CONTINUOUS

POWER BUDGET CURRENT OF FET
7.4A PEAK
4.5A CONTINUOUS



1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 11 OF 154	

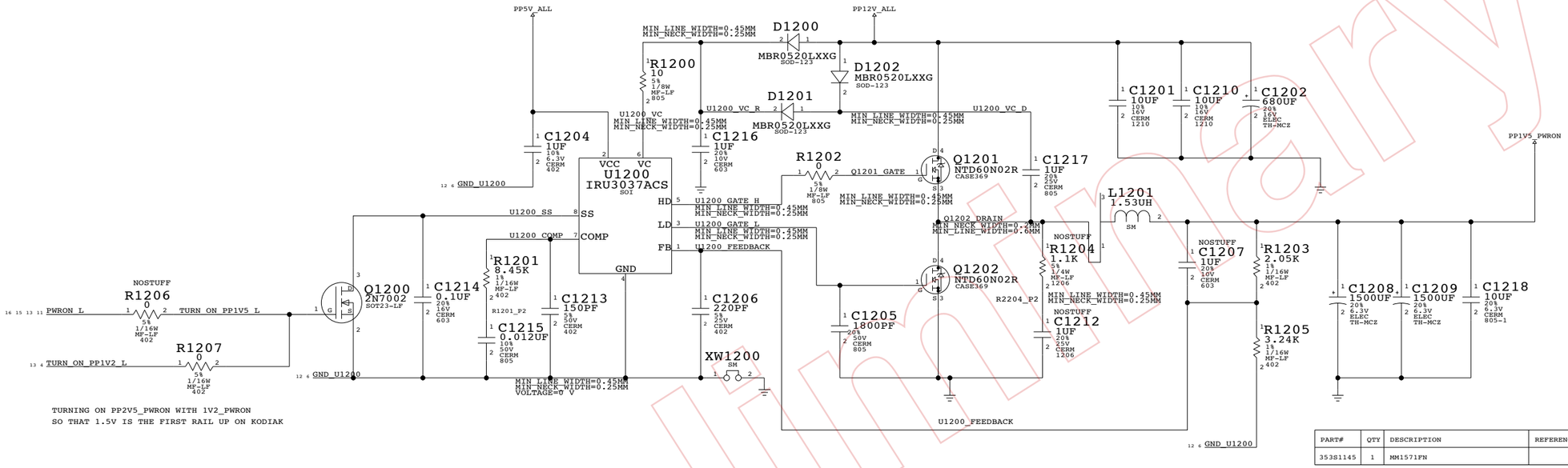
KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.30VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

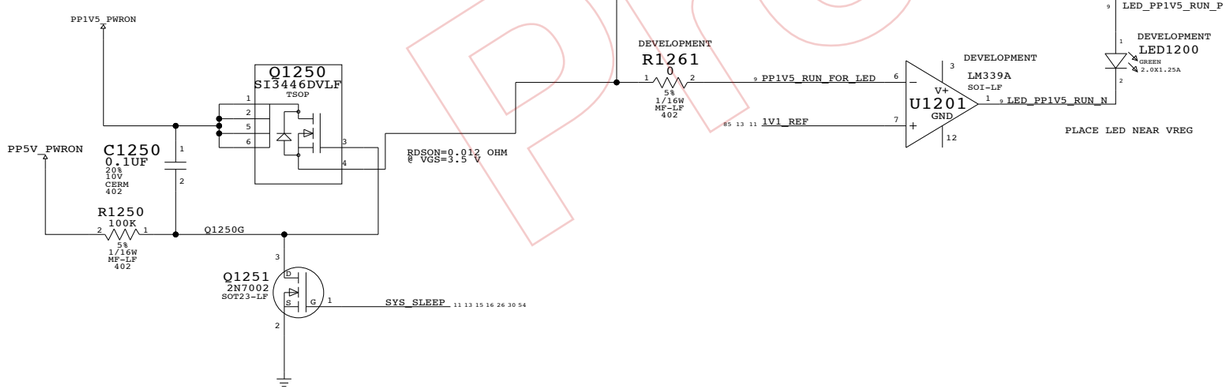
1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=4.02K



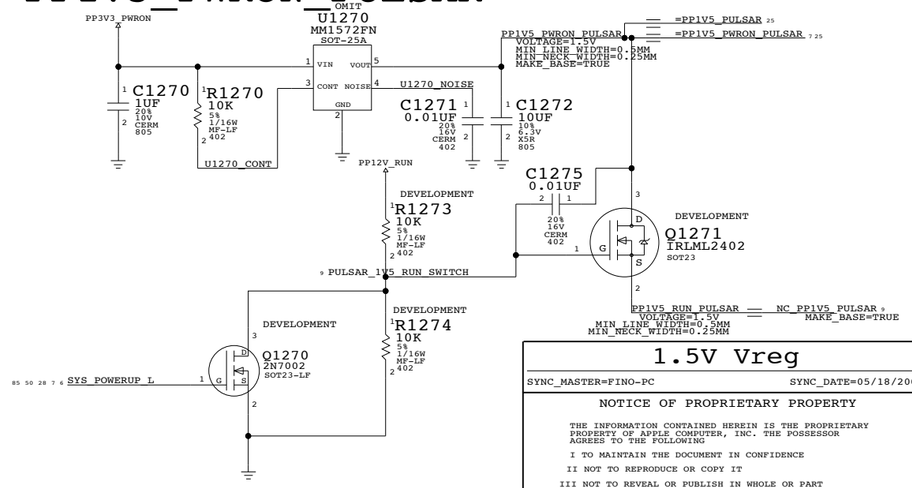
TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1145	1	MM1571FN	U1270	CRITICAL	

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW



PP1V5_PWRON_PULSAR



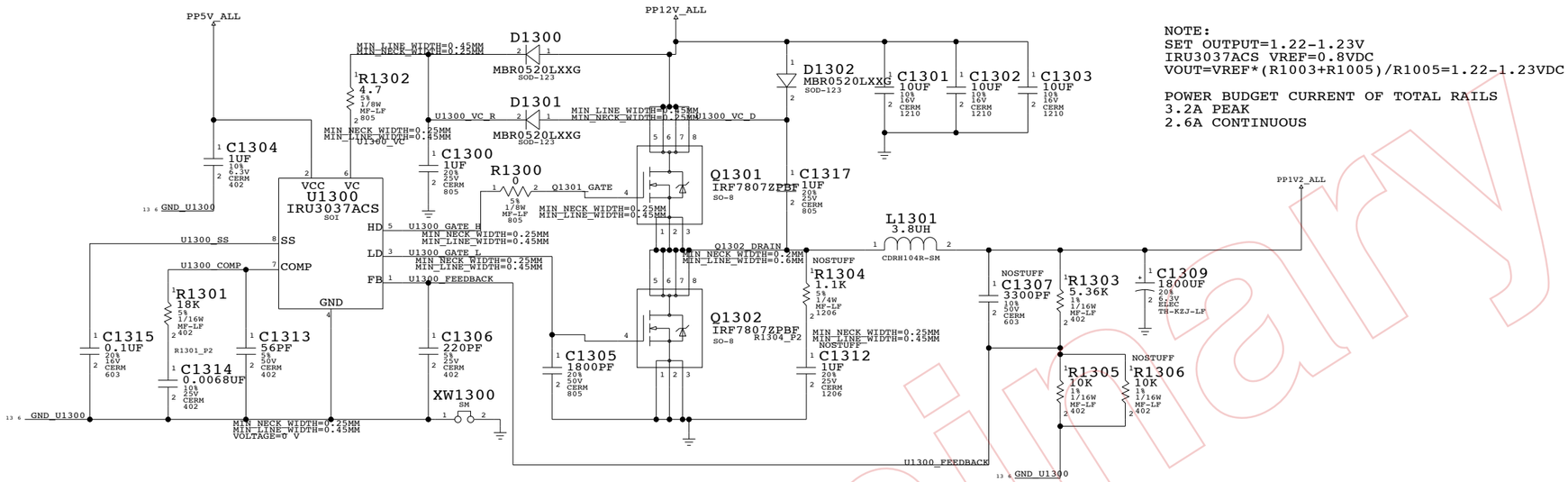
1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 12 OF 154	

PP1V2_ALL VOLTAGE REGULATOR

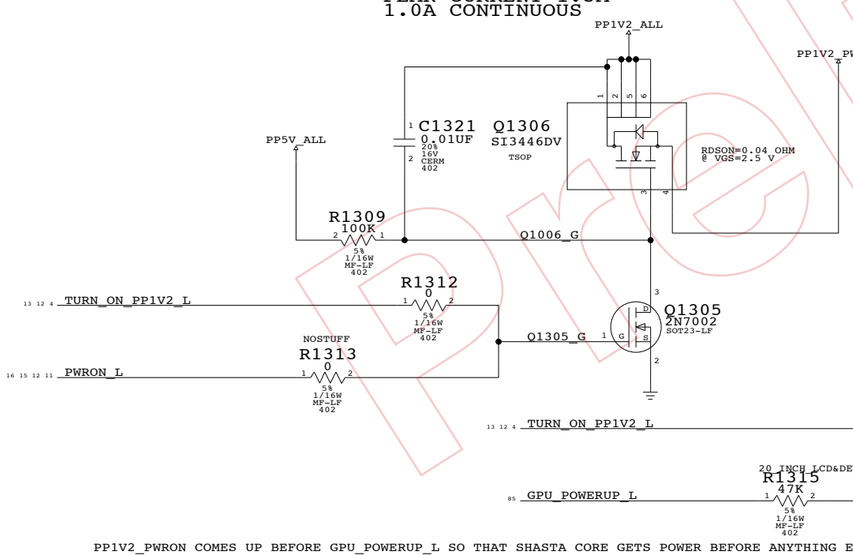


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

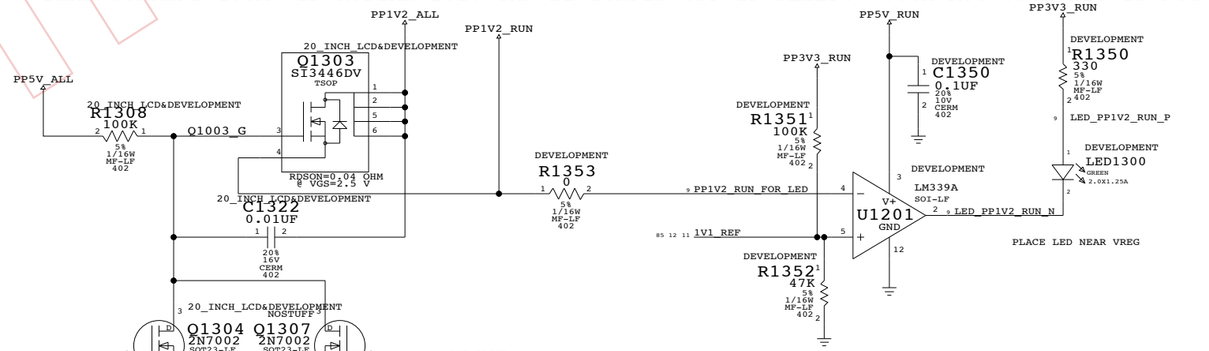
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg

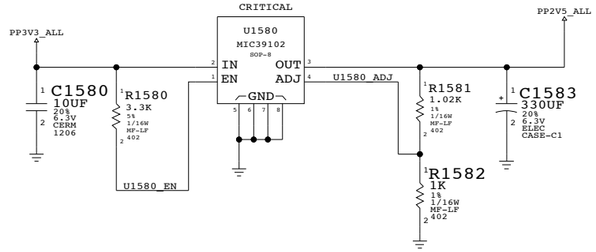
SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 13 OF 154

PP2V5_ALL VOLTAGE REGULATOR

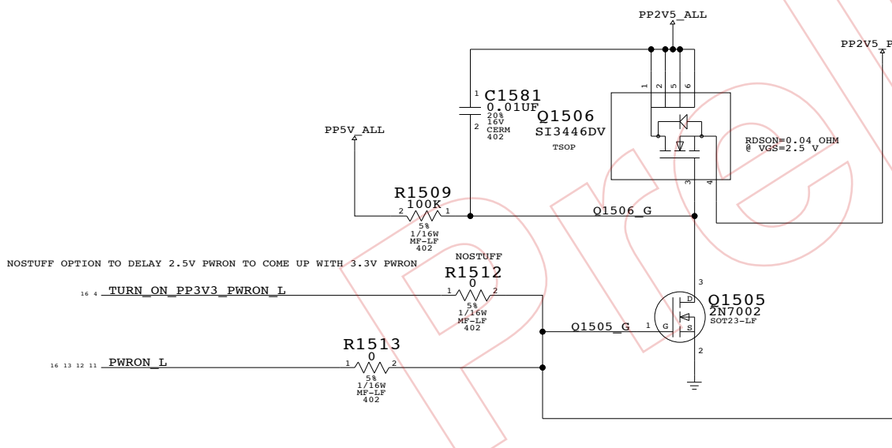


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

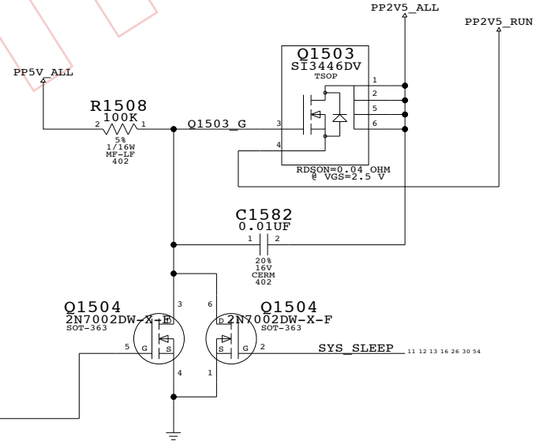
PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A

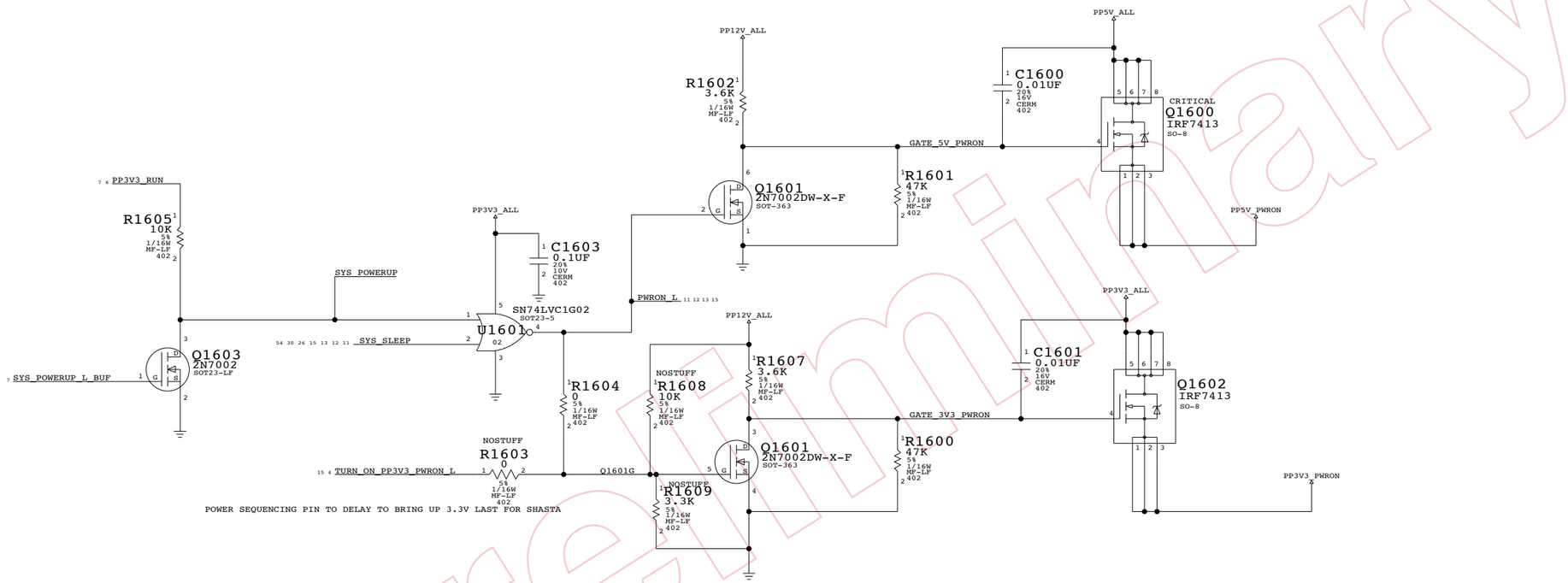


2.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 15 OF 154	



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 16 OF 154	

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

139 132 17 7 =PP3V3_ENETFW

VESTA HAS INTERNAL PULLUPS. MLB PULLUPS MAY BE NOSTUFFED IN EVT.

R1741 1K 5% 1/16W MF-LF 402
R1742 1K 5% 1/16W MF-LF 402
R1743 1K 5% 1/16W MF-LF 402

9 TP_JTAG_VESTA_TCK — MAKE_BASE=TRUE — =JTAG_VESTA_TCK 17
9 TP_JTAG_VESTA_TDI — MAKE_BASE=TRUE — =JTAG_VESTA_TDI 17
9 TP_JTAG_VESTA_TDO — MAKE_BASE=TRUE — =JTAG_VESTA_TDO 17
9 TP_JTAG_VESTA_TMS — MAKE_BASE=TRUE — =JTAG_VESTA_TMS 17
9 TP_JTAG_VESTA_TRST_L — MAKE_BASE=TRUE — =JTAG_VESTA_TRST_L

R1740 1K 5% 1/16W MF-LF 402

139 132 7 =PP1V2_ENETFW — L1700 FERR-EMI-600-OHM SM — PP1V2_VESTA_AVDDL (MIN_LINE_WIDTH=0.50 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.2V)

C1708 10UF 10% 6.3V X5R 805
C1700 0.1uF 20% 10V CERM 402 (L6/M6)
C1701 0.1uF 20% 10V CERM 402 (L9/M9)
C1702 0.1uF 20% 10V CERM 402 (N5/N6)
C1703 0.1uF 20% 10V CERM 402 (N9/N10)
C1714 10UF 10% 6.3V X5R 805
C1710 0.1uF 20% 10V CERM 402
C1711 0.1uF 20% 10V CERM 402
C1712 0.1uF 20% 10V CERM 402
C1713 0.1uF 20% 10V CERM 402

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1750 10K 5% 1/16W MF-LF 402
R1751 47K 5% 1/16W MF-LF 402
Q1750 2N7002DW-X-F SOT-363
C1750 1UF 10% 6.3V CERM 402
VESTA_RESET_RC

NOSTUFF
R1720 0 5% 1/16W MF-LF 402
24 ENETFW_RESET

=PP3V3_ENETFW 7 17 132 139

R1752 10K 5% 1/16W MF-LF 402
Q1750 2N7002DW-X-F SOT-363
132 VESTA_RESET_H

VESTA_RESET_L — SCHMITT TRIGGER W/ INTERNAL PULLUP

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

VESTA MISC

U1701 VESTA-V1.3 FBGA-200-LF 1 OF 3 (OMIT)

H4	RESET* IPU	
17 =JTAG_VESTA_TDI	D7	TDI IPU
17 =JTAG_VESTA_TDO	E10	TDO
17 =JTAG_VESTA_TCK	E7	TCK IPU
17 =JTAG_VESTA_TMS	E8	TMS IPU
17 =JTAG_VESTA_TRST_L	D8	TRST* IPU
9 TP_VESTA_DNC_C9	C9	DNC
9 TP_VESTA_DNC_E9	E9	DNC
NC C3		NC
NC H13		NC

DVDD B1 B15 C15 J1
AVDDL L6 L9 M6 M9 M5 M8 N9 M10
AVDD E4 P5 P10 P11 R3 R12
PVDD A15 N4
OVDD A1 A7 F15 K1
AGND H11 H12 J11 J12 L7 L8 M7 M8 N7 N8 P6 P7 P8 P9
GND A2 B2 B7 C14 F14 J2 K2

IPD 2.5V_EN M3 — TP_VESTA_2_5V_EN 9

REGSUP1 E1 — TP_VESTA_REGSUP1 9
REGSEN1 F1 — TP_VESTA_REGSEN1 9
REGCTL1 G5 — TP_VESTA_REGCTL1 9
REGSUP2 E2 — TP_VESTA_REGSUP2 9
REGSEN2 F2 — TP_VESTA_REGSEN2 9
REGCTL2 G4 — TP_VESTA_REGCTL2 9

M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS

=PP2V5_ENETFW 7 132 139
C1720 0.1uF 20% 10V CERM 402
C1721 0.1uF 20% 10V CERM 402
C1722 0.1uF 20% 10V CERM 402
C1723 0.1uF 20% 10V CERM 402
C1724 0.1uF 20% 10V CERM 402
C1725 0.1uF 20% 10V CERM 402
C1726 10UF 10% 6.3V X5R 805
C1730 0.1uF 20% 10V CERM 402
C1731 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139
C1740 0.1uF 20% 10V CERM 402
C1741 0.1uF 20% 10V CERM 402
C1742 0.1uF 20% 10V CERM 402
C1743 0.1uF 20% 10V CERM 402
C1744 10UF 10% 6.3V X5R 805

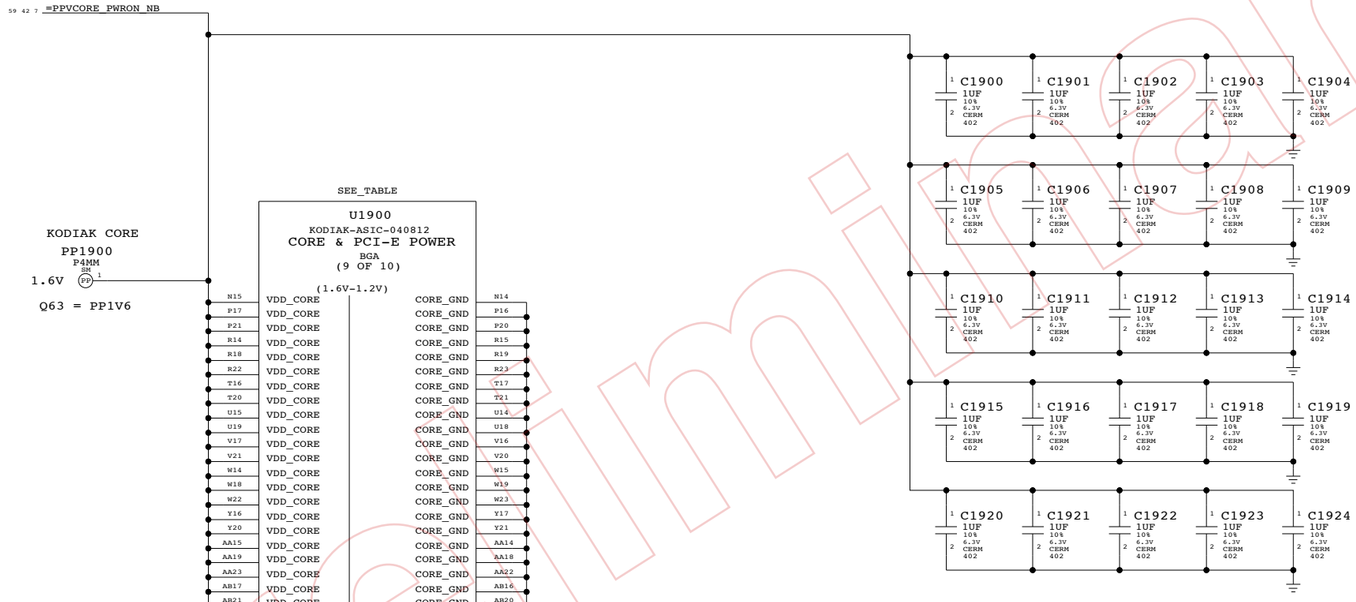
2.5V_EN
0 - OVDD=3.3V
1 - OVDD=2.5V
WHEN OVDD=2.5V GMII PINS ARE NOT 3.3V TOLERANT

Vesta Core / Misc

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 17 OF 154	



KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 19 OF 154	

SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

119 92 PCI_RESET_L — MAKE_BASE=TRUE
- =PCI_AIRPORT_RESET_L 121
- =PCI_ROM_RESET_L 125
- =PCI_USB2_RESET_L 122

24 NB_SLOT_RESET_L — MAKE_BASE=TRUE — =GPU_RESET_L 84

SHASTA JTAG

24 9 JTAG_SB_TRST_L — R2053 4.7K 5% 1/16W MF-LF 402

THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS

9 TP_JTAG_SB_TCK	MAKE_BASE=TRUE	JTAG_SB_TCK 24
9 TP_JTAG_SB_TDI	MAKE_BASE=TRUE	JTAG_SB_TDI 24
9 TP_JTAG_SB_TDO	MAKE_BASE=TRUE	JTAG_SB_TDO 24
9 TP_JTAG_SB_TMS	MAKE_BASE=TRUE	JTAG_SB_TMS 24

SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)

119 56 24 23 7 =PP3V3_PWRON_SB

24 RAI_EXP_INTR_L<3>	R2061 10K 5% 1/16W MF-LF 402	
24 RAI_EXP_INTR_L<2>	R2062 10K 5% 1/16W MF-LF 402	
24 RAI_EXP_INTR_L<1>	R2063 10K 5% 1/16W MF-LF 402	
24 RAI_EXP_INTR_L<0>	R2064 10K 5% 1/16W MF-LF 402	

KODIAK JTAG_TRST PULLED HIGH TO ALLOW SMU DEBUG ACCESS

KODIAK ALIASES

6 NC_PMR_CLK_DIS_L — MAKE_BASE=TRUE — PMR_CLK_DIS_L 20

=PP2V5_PWRON_NB_MISC 7 20 28 30 39

20 9 JTAG_NB_TRST_L — R2073 4.7K 5% 1/16W MF-LF 402 — NOSTUFF R2074 0 5% 1/16W MF-LF 402 — NB_PU_RST_L 20 30

NOSTUFF R2054 4.7K 5% 1/16W MF-LF 402

=PP1V8_PWRON_NBMEM 7 39 58 59

C2055 1UF 10% 6.3V CERM 402

C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP

NB_OVERTEMP

30 28 7 =PP3V3_RUN_SMU — R2082 200 5% 1/16W MF-LF 402

C2080 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.38MM
TSENSE_NB_VCC

TSENSE_NB_OVERTEMP_L — NOSTUFF R2087 0 5% 1/16W MF-LF 402 — SYS_OVERTEMP_L 24 28 93

U2080 MAX6690MEE
STBY, ALERT, SMBDATA, SMBCLK, DXP, DXN, VCC, ADD0, ADD1, QSOP (SYM_VER2), NC_1, NC_5, NC_9, NC_13, NC_16, GND

39 I2C_NB_TEMP_SDA
39 I2C_NB_TEMP_SCL

R2083 1K 5% 1/16W MF-LF 402 — NOSTUFF R2084 1K 5% 1/16W MF-LF 402
R2086 1K 5% 1/16W MF-LF 402 — NOSTUFF R2085 1K 5% 1/16W MF-LF 402

TSENSE_NB_ADD0
TSENSE_NB_ADD1

NEED TO CHECK ALL I2C ADDRESSES

A0	A1	ADDR
0	0	30/31
0	hiZ	32/33
0	1	34/35
hiZ	0	52/53
hiZ	hiZ	54/55
hiZ	1	56/57
1	0	98/99
1	hiZ	9A/9B
1	1	9C/9D

20 NB_THERM_A
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB
NET_PHYSICAL_TYPE=10MIL_WIDTH
NET_SPACING_TYPE=TSENSE_DIFPAIR
PLACE BY IC
C2081 0.0022UF 10% 50V CERM 402

20 NB_THERM_K
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB

NET_SPACING_TYPE=TSENSE_DIFPAIR
NET_PHYSICAL_TYPE=10MIL_WIDTH

20 NB_THERM_A
20 NB_THERM_K
39 30 28 20 7 =PP2V5_PWRON_NB_MISC

C2050 1UF 10% 6.3V CERM 402
C2051 1UF 10% 6.3V CERM 402
C2052 1UF 10% 6.3V CERM 402

R2000 0 5% 1/16W MF-LF 402

POWER/TEST/MISC

U1900 KODIAK-ASIC-040812 BGA (10 OF 10)

30 9 JTAG_NB_TCK	AJ04	CE1_LT_TCK	
30 9 JTAG_NB_TDI	AG07	CE1_MC_TDI	
30 9 JTAG_NB_TDO	AG05	CE1_B_TDO	
30 9 JTAG_NB_TMS	AL02	CE1_DI1_TMS	
20 9 JTAG_NB_TRST_L	AK06	CE1_DI2_TRST	
CE0TEST	AG08	CE0_TEST	
20 NB_THERM_A	F15	SYS_THDIO_D	
20 NB_THERM_K	G15	SYS_THDIO_G	
=PP2V5_PWRON_NB_MISC	AF02	VD5_0	
	AF05	VD5_1	
	AH01	VD5_2	
NORTH_BRIDGE_RESET_L	AL01		
HRESET_L	AG01		
SUSPENDACK_L	AJ03		
SUSPENDREQ_L	AJ01		
SYS_ISCA0	AG04		
SYS_ISCL0	AK03		
SYS_ISCA1	AH06		
SYS_ISCL1	AJ05		
API_ISCA	AG03		
API_ISCL	AH03		
PMR_CLK_P	AE09		
PMR_CLK_N	AE10		
PMR_CLK_STOP_L	AG02		

NORTH_BRIDGE_RESET_L — NB_PU_RST_L 20 30
HRESET_L — NB_HRST_L
SUSPENDACK_L — NB_SUSPEND_ACK_L 30 62
SUSPENDREQ_L — NB_SUSPEND_REQ_L 30
SYS_ISCA0 — I2C_NB_B_SDA 39
SYS_ISCL0 — I2C_NB_B_SCL 39
SYS_ISCA1 — I2C_NB_C_SDA 39
SYS_ISCL1 — I2C_NB_C_SCL 39
API_ISCA — I2C_NB_A_SDA 39
API_ISCL — I2C_NB_A_SCL 39
PMR_CLK_P — NB_PMR_CLK_P 26 27
PMR_CLK_N — NB_PMR_CLK_N 26 27

39 30 28 20 7 =PP2V5_PWRON_NB_MISC

P4MM SM TP2002 — R2003 1K 1% 1/16W MF-LF 402

NOSTUFF R2001 60.4 1% 1/16W MF-LF 402
NOSTUFF R2002 60.4 1% 1/16W MF-LF 402
TERM_RC

NOSTUFF C2053 1.5PF +/-0.25PF 50V CERM 402

PLACE TERM R/C CLOSE TO KODIAK

TP2000 P4MM SM — 1 PP_2V5PWRONNBMISC — XW2000 SM

R2013 10K 5% 1/16W MF-LF 402

NOSTUFF R2012 0 5% 1/16W MF-LF 402

20 PMR_CLK_DIS_L

NB_PMR_CLK_STOP_L
NOTE: LOW = DISABLE PMR_CLK

NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE: NONE — SHT 20 OF 154

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

=PP1V2_PWRON_SB_VCORE

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314
0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB
119 56 24 20 7

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339
0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.1
BGA-LF
(1 OF 8)

POWER

SEE_TABLE

VDDC
VDDIO33
VDDO25
VIO1
VIO2
VDDP_KL
GND

Shasta max (set 06/30/03) current:

DIGITAL	= 1.2V ~ 950 mA	(1175 mW)
ANALOG12	= 1.2V ~ 600 mA	(760 mW)
VDDPs	= 2.5V ~ 100 mA	(250 mW)
I/O 2.5	= 2.5V ~ 20 mA	(60 mW)
I/O 3.3	= 3.3V ~ 220 mA	(770 mW)
Total:		3015 mW

XW2300 SM 2 1 6 PP_1V2PWRONSBVCORE → P4MM SM PP → PP2300
XW2303 SM 2 1 6 PP_3V3PWRONSBPCI64 → P4MM SM PP → PP2303
XW2304 SM 2 1 6 NO_TEST=YES PP_2V5PWRONSB → P4MM SM PP → PP2304

=PP2V5_PWRON_SB
7 23 24 119 138

C2350 C2351
C2355 C2356 C2357
C2360 C2361 C2362
C2365
0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB_PCI64
=PP3V3_PWRON_SB_PCI32
=PP2V5_PWRON_SB

For PCI_AD<63..32>
For PCI_AD<31..0>

LAST_MODIFIED=Thu May 19 14:08:56 2005

Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE: NONE SHT 23 OF 154

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI 24 147
I2S0_SB_TO_DEV_DTO 24 147
I2S0_MCLK 24 154
I2S0_BITCLK 24 147
I2S0_SYNC 24 147
I2S1_DEV_TO_SB_DTI 8 24
I2S1_SB_TO_DEV_DTO 8 24
I2S1_MCLK 8 24
I2S1_BITCLK 8 24
I2S1_SYNC 8 24
I2S2_DEV_TO_SB_DTI 24 154
I2S2_SB_TO_DEV_DTO 24 154
I2S2_MCLK 24 154
I2S2_BITCLK 24 154
I2S2_SYNC 24 154
SB_CLK18M_XTALI 24
SB_CLK18M_XTALO 24
SB_CLK18M_XTALO_R 24
SB_CLK25M_SATA 24 26
NB_TO_SB_INT 24
SB_CPU_A0_INT_L 24
SB_CPU_A1_INT_L 24
SB_CPU_B0_INT_L 24
SB_CPU_B1_INT_L 24
PCI_AIRPORT_INT_L 24 121
PCI_USB2_INT_L 24 122
I2S0_RESET_L 24 147
I2S1_RESET_L 8 24
I2S2_RESET_L 24 154
MB_SLOT_RESET_L 24
NB_SLOT_RESET_L 20 24
SB_CPU_A0_SRESET_L 24 56
SB_CPU_A1_SRESET_L 24 56
SB_CPU_B0_SRESET_L 24 56
SB_CPU_B1_SRESET_L 24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing

PLACE R2402 CLOSE TO SHASTA

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

PLACE R2432 CLOSE TO SHASTA

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

Shasta Serial / Misc

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

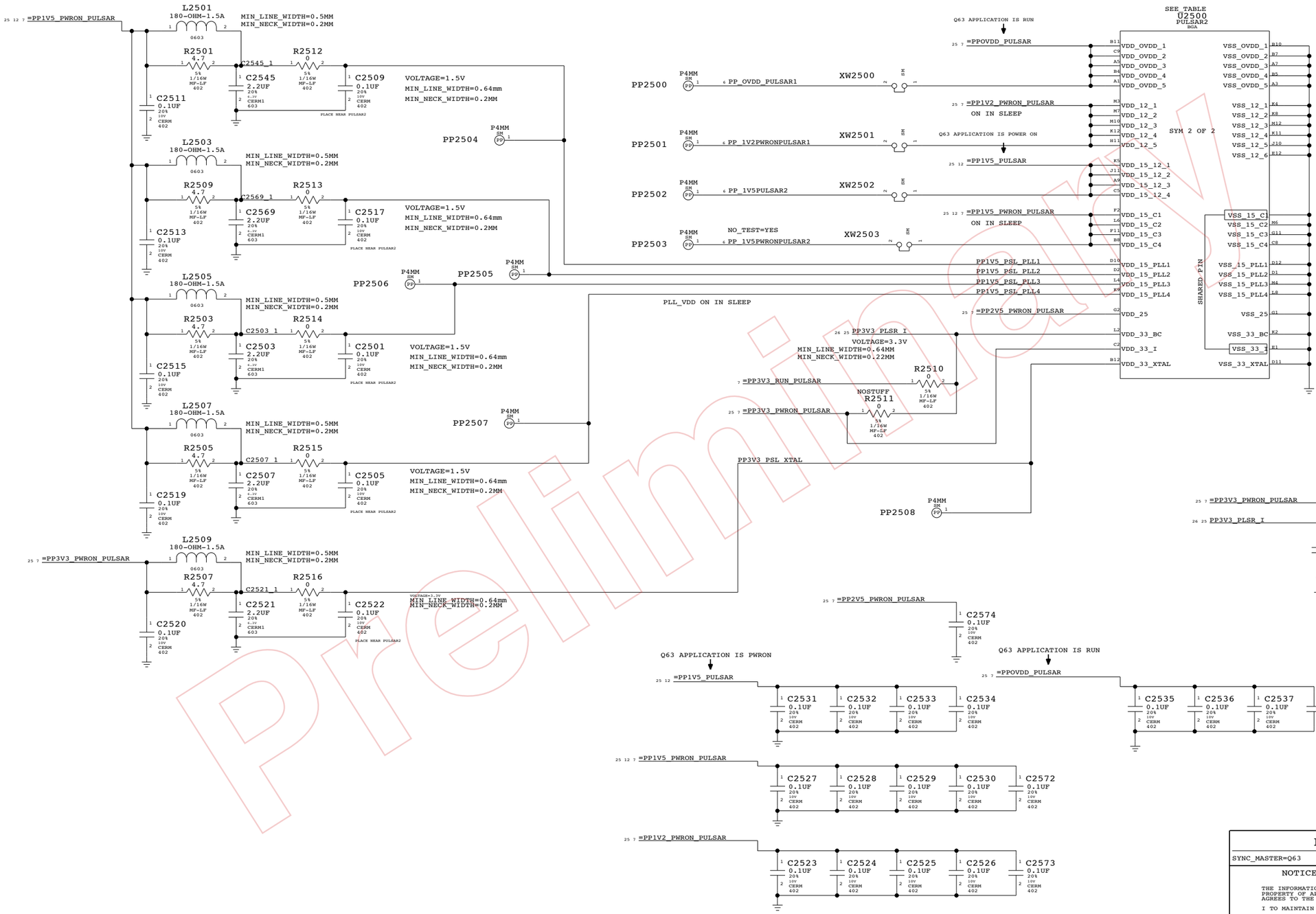
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 24 OF 154	

LAST_MODIFIED=Thu May 19 14:08:57 2005



PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	25	154

LAST_MODIFIED=Thu May 19 14:08:58 2005

DRAWING

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR

U2500
PULSAR2
BGA
SYM 1 OF 2

PP2602 P4MM SM
PP2601 P4MM SM
PP2600 P4MM SM

R2612 0 5% 402 — 28 CLOCK_RESET_L — PLS2_RESET_L
PLS2_ASEL_INT_L
39 I2C_CLOCK_B_SCL
39 I2C_CLOCK_B_SDA
PLS2_PD
PLS2_TM
PLS2_OEMODE
25 PP3V3_PLSR_I

R2613 10K 5% 1/16W MF-LF 402
R2614 NOSTUFF 10K 5% 1/16W MF-LF 402
R2616 10K 5% 1/16W MF-LF 402
R2623 0 5% 1/16W MF-LF 402
R2618 NOSTUFF 1K 1% 1/16W MF-LF 402
R2621 1K NOSTUFF 1% 1/16W MF-LF 402

R2600 0 5% 402 — 54 30 16 15 13 12 11 SYS_SLEEP

PLS2_X_IN
PLS2_X_OUT
PLS2_REF15
PLS2_REF25
PLS2_REF33

R2625 1K 1% 1/16W MF-LF 402
R2626 1K 1% 1/16W MF-LF 402
R2627 1K 1% 1/16W MF-LF 402

NOSTUFF J2600 U.FL-R_SMT F-ST-SM
R2662 NOSTUFF 24 5% 1/16W MF-LF 402
R2664 NOSTUFF 24 5% 1/16W MF-LF 402
PLS2_EXTCLK
PLS2_INTERM

NO STUFF R2652 0 5% 1/16W MF-LF 402
R2654 0 5% 1/16W MF-LF 402
NO STUFF R2658 330K 5% 1/16W MF-LF 402
R2656 0 5% 1/16W MF-LF 402

CRITICAL Y2601 25.0000M SM-2
PLS2_X_IN_B
PLS2_X_OUT_B

C2607 33PF 5% 50V CERM 402
C2605 33PF 5% 50V CERM 402

R2628 0 5% 1/16W MF-LF 402 — PULLED UP TO PP3V3_RUN ON P.28 — SYS_SLEWING_L — 24 28 50

SLEWING* A12 — SYS_SLEWING_L_R

HCLKP_0	A6	200MHZ, 1.5VOVDD	
HCLKN_0	B6	200MHZ, 1.5VOVDD	
HCLKP_1	C4	200MHZ, 1.5VOVDD	
HCLKN_1	A4	200MHZ, 1.5VOVDD	
HCLKP_2	B3	200MHZ, 1.5VOVDD	
HCLKN_2	A2	200MHZ, 1.5VOVDD	
HTBEN_0	A11	66MHZ, 1.5VOVDD	9 CPU_A_TBEN_CLK_R
HTBEN_1	A10	66MHZ, 1.5VOVDD	9 CPU_B_TBEN_CLK_R
HSYNC_0	A8	1.5VOVDD	9 CPU_A_APSYNC_R
HSYNC_1	B9	1.5VOVDD	9 CPU_B_APSYNC_R
HSYNC_2	C10	1.5VOVDD	9 NB_APSYNC_R
GPCLK12_C0	H12	66MHZ, 1.2V (150MHZ FOR ASPEN)	9 HT_SB_REFCLK_R
GPCLK12P_A0	K3	200MHZ, 1.2V	9 HT_NB_REFCLK_H0_R
GPCLK12N_A0	L3	200MHZ, 1.2V	9 HT_NB_REFCLK_L0_R
GPCLK12P_A1	M5	200MHZ, 1.2V	9 CLK_RAIREF_200M_P_R
GPCLK12N_A1	L5	200MHZ, 1.2V	9 CLK_RAIREF_200M_N_R
GPCLK12P_B0	L7	100MHZ, 1.2V	9 NB_PMR_CLK_P_R
GPCLK12N_B0	M8	100MHZ, 1.2V	9 NB_PMR_CLK_N_R
GPCLK12P_C0	M9	100MHZ, 1.2V	9 NB_PCIE_REFCLK_P_C
GPCLK12N_C0	L9	100MHZ, 1.2V	9 NB_PCIE_REFCLK_N_C
GPCLK12P_C1	L10	100MHZ, 1.2V	9 GFX_SLOT_PCIE_REFCLK_P_C
GPCLK12N_C1	M11	100MHZ, 1.2V	9 GFX_SLOT_PCIE_REFCLK_N_C
GPCLK12P_C2	L11	100MHZ, 1.2V	9 PCIE_A_REFCLKIN_P_C
GPCLK12N_C2	L12	100MHZ, 1.2V	9 PCIE_A_REFCLKIN_N_C
GPCLK12P_C3	K10	100MHZ, 1.2V	9 PCIE_B_REFCLKIN_P_C
GPCLK12N_C3	J12	100MHZ, 1.2V	9 PCIE_B_REFCLKIN_N_C
GPCLK12P_C4	G12		9 PCIE_C_REFCLKIN_P_C
GPCLK12N_C4	F12	100MHZ, 1.2V	9 PCIE_C_REFCLKIN_N_C
GPCLK12P_D0	E10	66MHZ, 1.2V	9 NB_DDR_REFCLK_P_R
GPCLK12N_D0	E11	66MHZ, 1.2V	9 NB_DDR_REFCLK_N_R
GPCLK25_E0	H1	25MHZ, 2.5V	9 CLK_RAI_GIGE_25MHZ_R
GPCLK25_E1	H3	25MHZ, 2.5V	9 QUA0_REF_25MHZ_R
GPCLK25_F0	H2	25MHZ, 2.5V	9 SB_CLK25M_SATA_R
GPCLK25_F1	J3	25MHZ, 2.5V	9 QUA1_REF_25MHZ_R
GPCLK33_E0	J1	66MHZ, 3.3V	6 PCI_CLK66M_SB_INT_R
GPCLK33_E1	J2	33MHZ, 3.3V	9 PCI_CLK33M_SB_EXT_R
GPCLK33_F0	K1	33MHZ, 3.3V	9 SB_AIRPRT_CLK_33MHZ_R
GPCLK33_F1	M1	66MHZ, 3.3V	9 CLK_RAI_REFCLK_66M_R
GPCLK33_F2	M2	33MHZ, 3.3V	9 SB_USB2_CLK_33MHZ_R

EI_CPU_A_SYSCLK_P 56
EI_CPU_A_SYSCLK_N 56
EI_CPU_B_SYSCLK_P 27
EI_CPU_B_SYSCLK_N 27
EI_NB_SYSCLK_P 42 56
EI_NB_SYSCLK_N 42 56

R2629 0 5% 1/16W MF-LF 402 — CPU_A_TBEN_CLK_US 56
R2630 0 NOSTUFF 5% 1/16W MF-LF 402 — NC_CPU_B_TBEN_CLK_US 6
R2631 0 5% 1/16W MF-LF 402 — CPU_A_APSYNC 56
R2632 0 5% 1/16W MF-LF 402 — CPU_B_APSYNC 27
R2633 0 5% 1/16W MF-LF 402 — NB_APSYNC 42 56
R2634 0 5% 1/16W MF-LF 402 — HT_CLK66M_SB 103
R2635 0 5% 1/16W MF-LF 402 — HT_NB_REFCLK_P<0> 98 101
R2636 0 5% 1/16W MF-LF 402 — HT_NB_REFCLK_N<0> 98 101
R2637 0 5% 1/16W MF-LF 402 — CLK_RAI_200M_P<0> 27
R2639 0 5% 1/16W MF-LF 402 — CLK_RAI_200M_N<0> 27
R2641 0 5% 1/16W MF-LF 402 — NB_PMR_CLK_P 20 27
R2643 0 5% 1/16W MF-LF 402 — NB_PMR_CLK_N 20 27
R2666 0 5% 1/16W MF-LF 402 — CLK_KOD_100M_P<0> 82 97
R2667 0 5% 1/16W MF-LF 402 — CLK_KOD_100M_N<0> 82 97
R2674 0 5% 1/16W MF-LF 402 — CLK_PCIE_SLOTA_P<0> 84 97
R2675 0 5% 1/16W MF-LF 402 — CLK_PCIE_SLOTA_N<0> 84 97
R2668 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEA_P<0> 27
R2669 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEA_N<0> 27
R2670 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEB_P<0> 27
R2671 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEB_N<0> 27
R2672 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEC_P<0> 27
R2673 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEC_N<0> 27
R2645 0 5% 1/16W MF-LF 402 — NB_DDR_REFCLK_P 59
R2647 0 5% 1/16W MF-LF 402 — NB_DDR_REFCLK_N 59
R2649 0 5% 1/16W MF-LF 402 — CLK_RAI_GIGE_25MHZ 27
R2651 0 5% 1/16W MF-LF 402 — RAM_ARB0_REF25MHZ 27
R2653 0 5% 1/16W MF-LF 402 — SB_CLK25M_SATA 24
R2655 0 5% 1/16W MF-LF 402 — RAM_ARB1_REF25MHZ 27
R2657 0 5% 1/16W MF-LF 402 — PCI_CLK66M_SB_INT 27 119
R2659 0 5% 402 MF-LF 1/16W — PCI_CLK33M_SB_EXT_RR 27 119
NOSTUFF R2601 49.9 1% 1/16W MF-LF 402 — PLACE R2602 BESIDE R2659 — CPU_TBEN_CLK 27
R2660 0 5% 1/16W MF-LF 402 — PCI_CLK33M_AIRPORT 121
R2663 0 5% 1/16W MF-LF 402 — CLK_RAI_REFCLK_66M 27 — MB_PCIX_REFCLK
R2665 0 5% 1/16W MF-LF 402 — PCI_CLK33M_USB2 27

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT: 26	OF: 154

LAST_MODIFIED=Thu May 19 14:08:58 2005

DRAWING

N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M — CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_GIGE_25MHZ — CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_P<0> — CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_N<0> — CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_P<0> — CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_N<0> — CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_P<0> — CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_N<0> — CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_P<0> — CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_N<0> — CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

9 NC_CPU_TBEN_CLK — CPU_TBEN_CLK 26
MAKE_BASE=TRUE

CPU_TBEN_CLK IS FOR Q63 ONLY
IT IS THE INPUT TO THE AND GATE WHICH
GENERATES CPUA AND CPUB TBEN_CLK

6 NC_EI_CPU_B_SYSCLK_P — EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

6 NC_EI_CPU_B_SYSCLK_N — EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

6 NC_CPU_B_APSYNC — CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ — RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

6 NC_RAM_ARB1_REF25MHZ — RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	167
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	168
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	169
26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB	170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 — =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 27 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	Net	Pages
SMU_CLK10M_XTAL	0.38MM SPACING		SMU_CLK10M_XIN	28
	0.38MM SPACING		SMU_CLK10M_XOUT	28
	0.38MM SPACING		SMU_CLK10M_XOUT_R	28
RTC_CLK32K_XTAL	0.38MM SPACING		RTC_CLK32K_X1	28
	0.38MM SPACING		RTC_CLK32K_X2	28
I473	P3MM SPACING		SMU_IO_RESET_L	28 30
I474	0.25MM SPACING		SYS_NORTH_RESET_L	28 30

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	Net	Pages
I456 SMU_RESET	0.25MM SPACING		SYS_NORTH_RESET_L	28 30
I457 SMU_RESET	0.25MM SPACING		SYS_IO_RESET_L	24 30 119 122
I472	P3MM SPACING		CLOCK_RESET_L	26 28
I475	P3MM SPACING		SYS_RESET_BUTTON_L	28 29

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

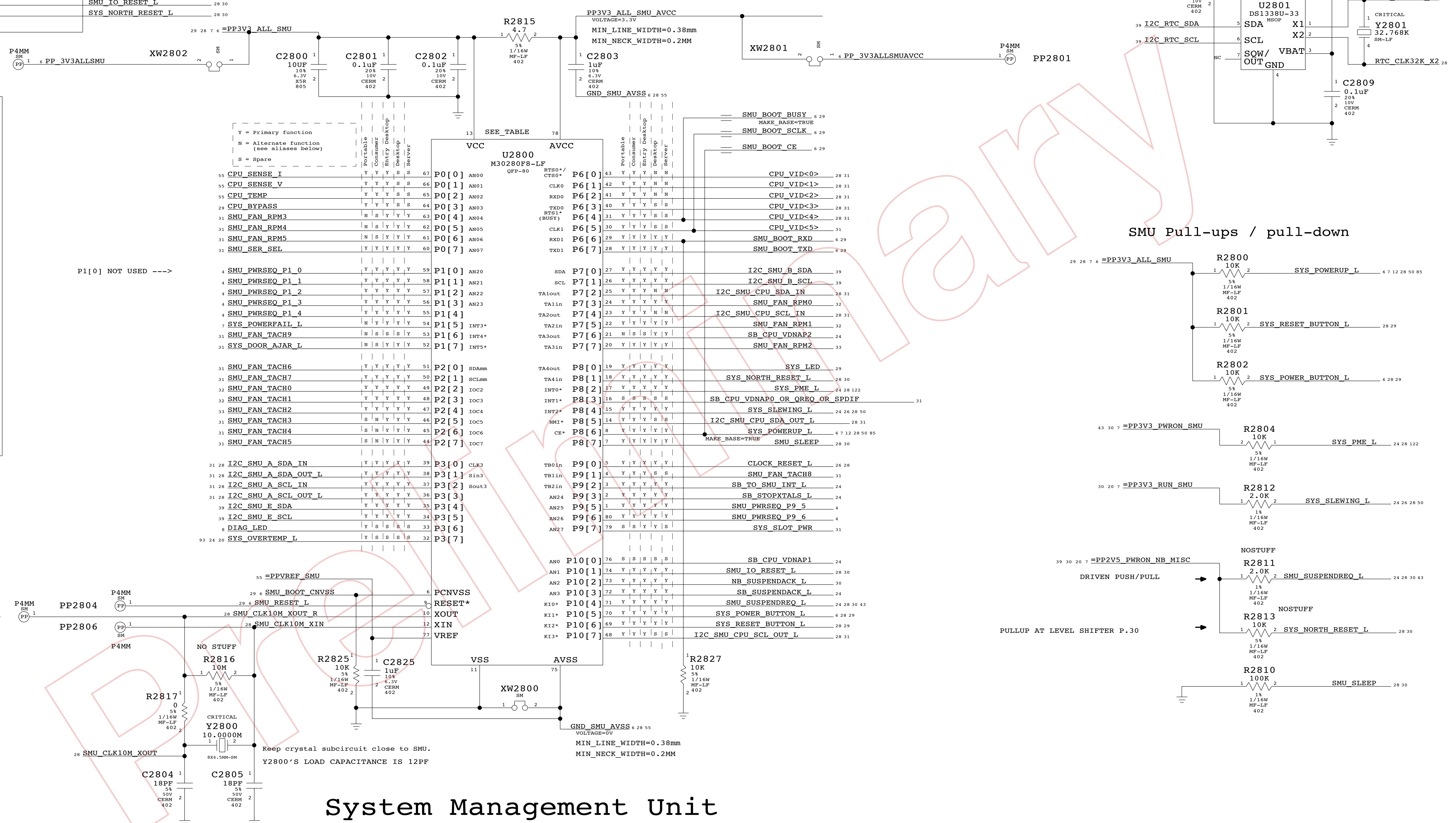
BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.



System Management Unit

Alternate Functions

Tower & Server

Pages	Signal	Port	Alternate	Pages
31 28	CPU_VID<0>	6.0	SAT_MRESET_L	
31 28	CPU_VID<1>	6.1	CPU_A_INSERTED_L	
31 28	CPU_VID<2>	6.2	CPU_B_INSERTED_L	
31 28	I2C_SMU_CPU_SDA_IN	7.2	SMU_FAN_PWM8	
31 28	I2C_SMU_CPU_SCL_IN	7.4	SMU_FAN_PWM9	
31 28	I2C_SMU_A_SDA_IN	3.0	I2C_SMU_A_SDA	31 39
31 28	I2C_SMU_A_SDA_OUT_L	3.1	I2C_SMU_A_SCL	31 39
31 28	CPU_VID<3>	6.3	SMU_FAN_RPM6	
31 28	CPU_VID<4>	6.4	SMU_FAN_RPM7	
31 28	I2C_SMU_A_SCL_IN	3.2	NB_TDI	
31 28	I2C_SMU_A_SCL_OUT_L	3.3	NB_TCK	
31 28	I2C_SMU_CPU_SDA_OUT_L	8.5	NB_TMS	
31 28	I2C_SMU_CPU_SCL_OUT_L	10.7	NB_TDO_SMU	

LAST_MODIFIED=Thu May 19 14:09:00 2005

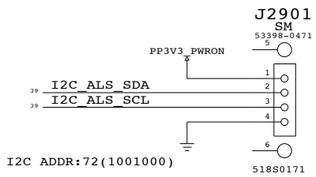
System Management Unit

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

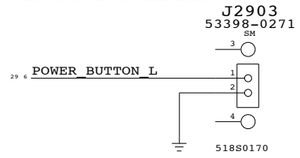
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 28	OF 154

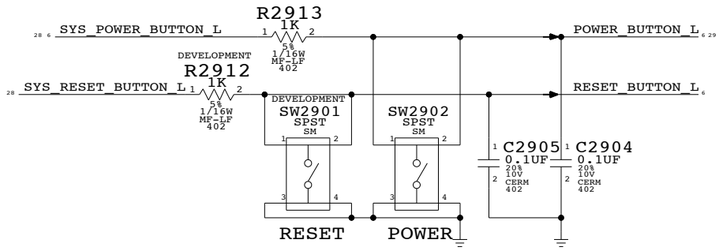
AMBIENT LIGHT SENSOR CONNECTOR



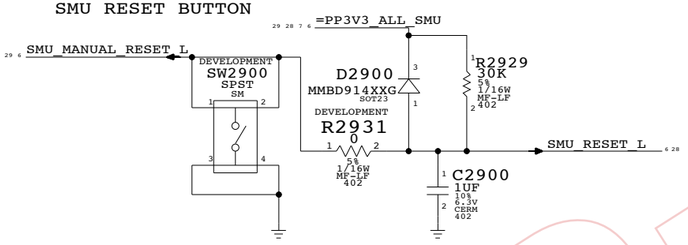
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

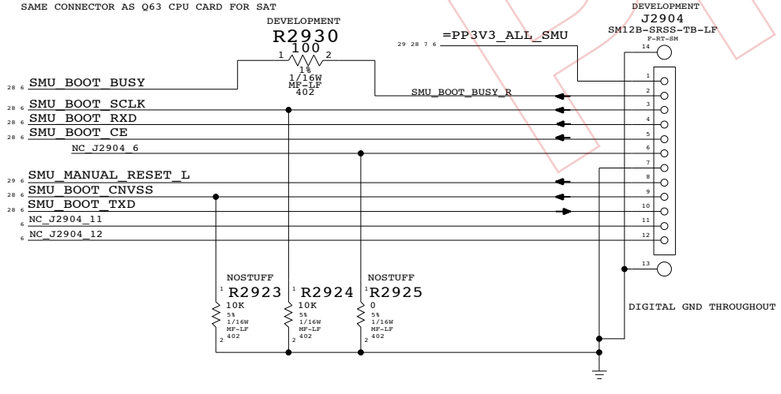


SMU RESET BUTTON

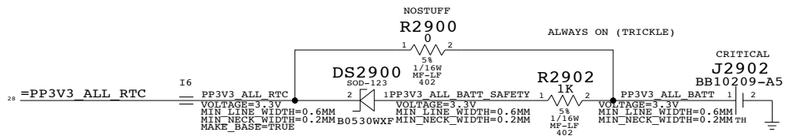


SMU DEBUG/DOWNLOAD CONNECTOR

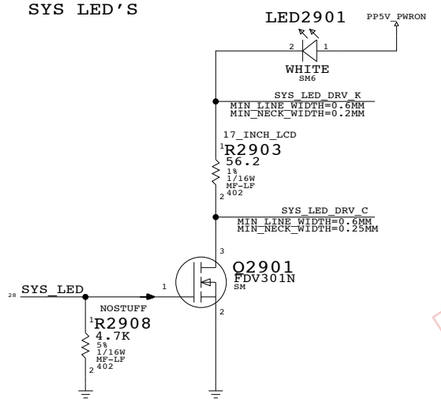
SAME CONNECTOR AS Q63 CPU CARD FOR SAT



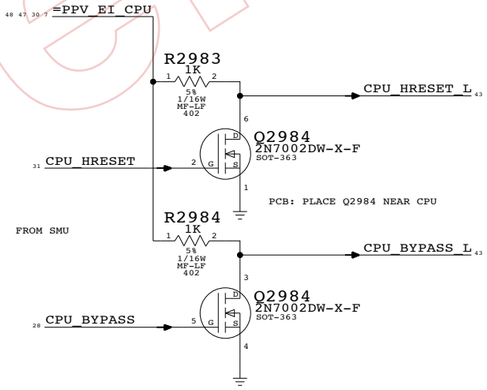
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483921	1	RES, 39.2 OHM, 1%, 402	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

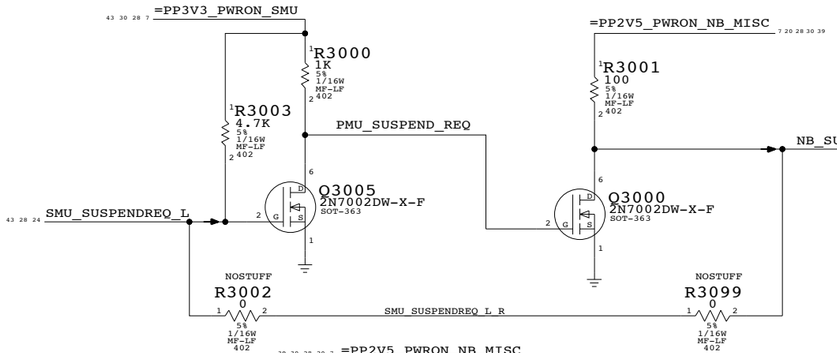
SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 29 OF 154	

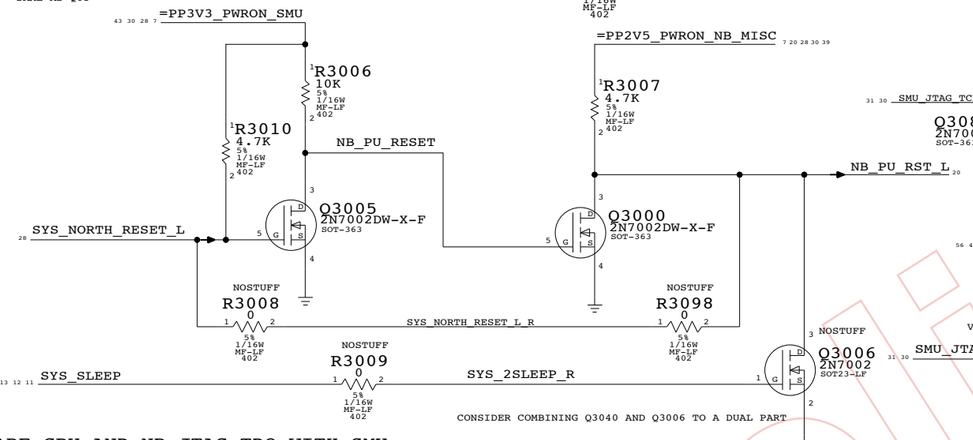
SMU TO NB SUSPEND_REQ

SAME AS Q63



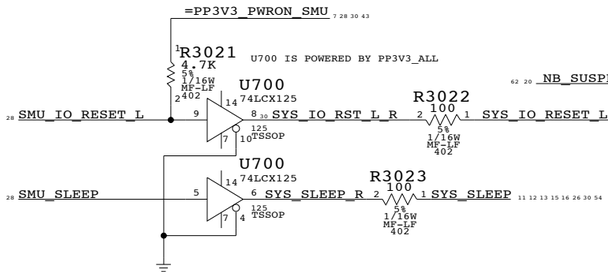
SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

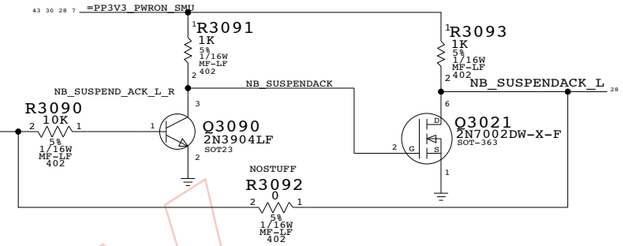


MISC. SMU BUFFERS

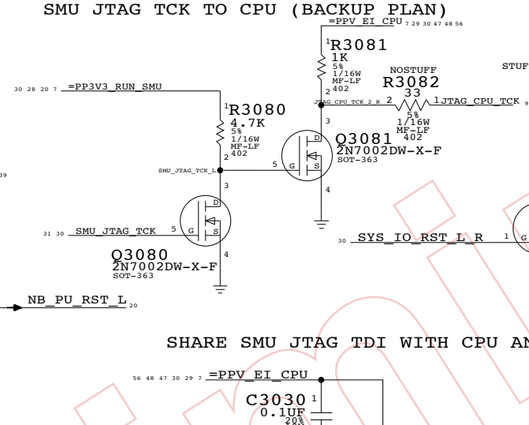
SAME AS (Q63).



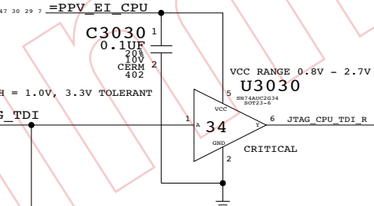
NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER



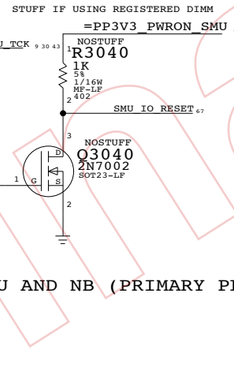
SMU JTAG TCK TO CPU (BACKUP PLAN)



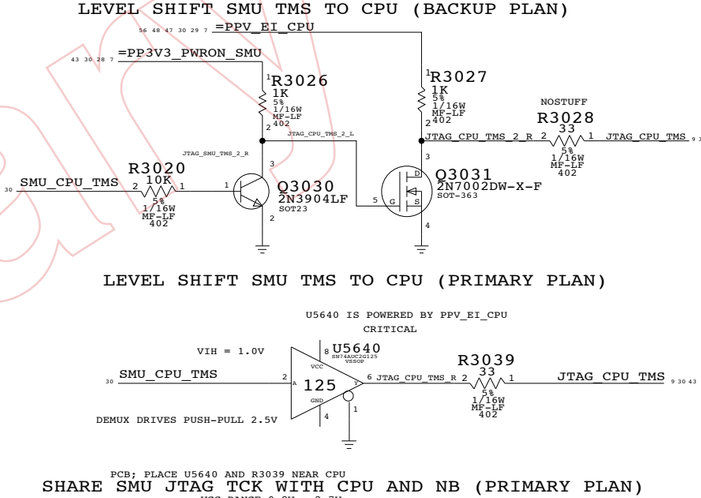
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)



STUFF IF USING REGISTERED DIMM



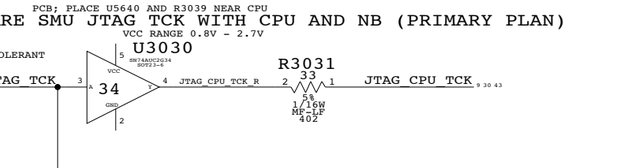
LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)



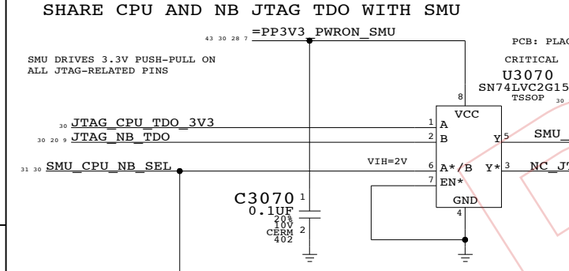
LEVEL SHIFT SMU TMS TO CPU (PRIMARY PLAN)

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)

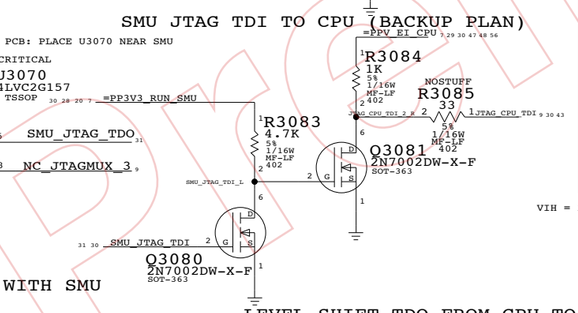
PCB; PLACE U5640 AND R3039 NEAR CPU



SHARE CPU AND NB JTAG TDO WITH SMU

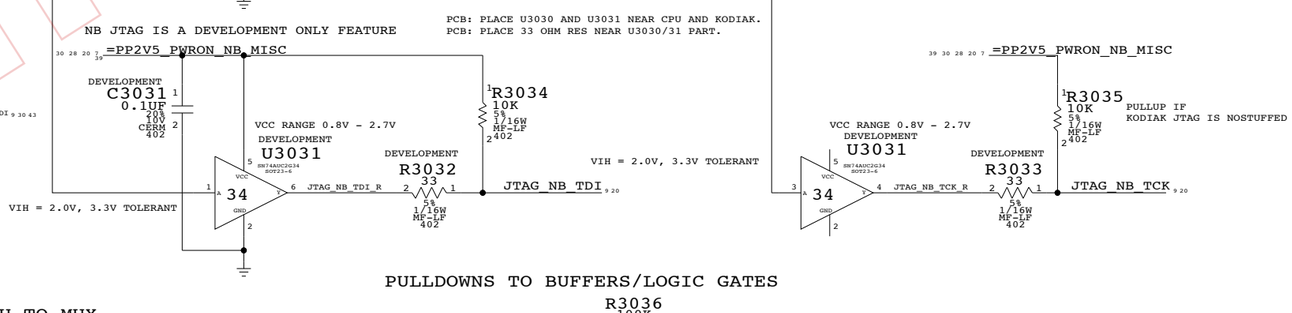


SMU JTAG TDI TO CPU (BACKUP PLAN)

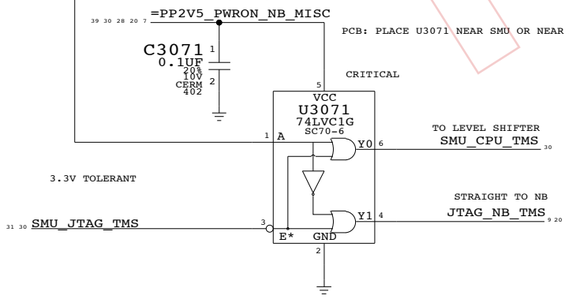


NB JTAG IS A DEVELOPMENT ONLY FEATURE

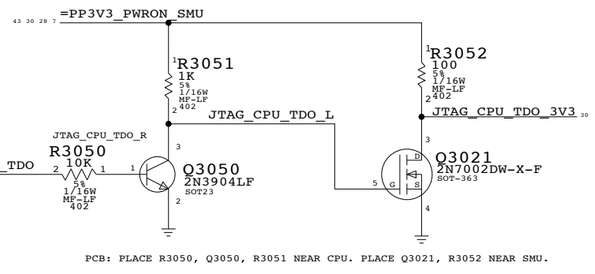
PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.
PCB: PLACE 33 OHM RES NEAR U3030/31 PART.



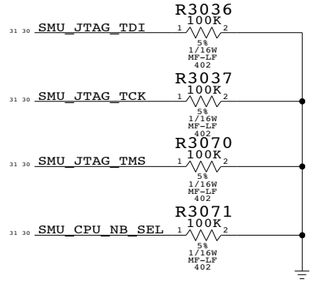
SHARE CPU AND NB JTAG TMS WITH SMU



LEVEL SHIFT TDO FROM CPU TO MUX



PULLDOWNS TO BUFFERS/LOGIC GATES



SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	08
	SCALE: NONE	SHT 30 OF 154	

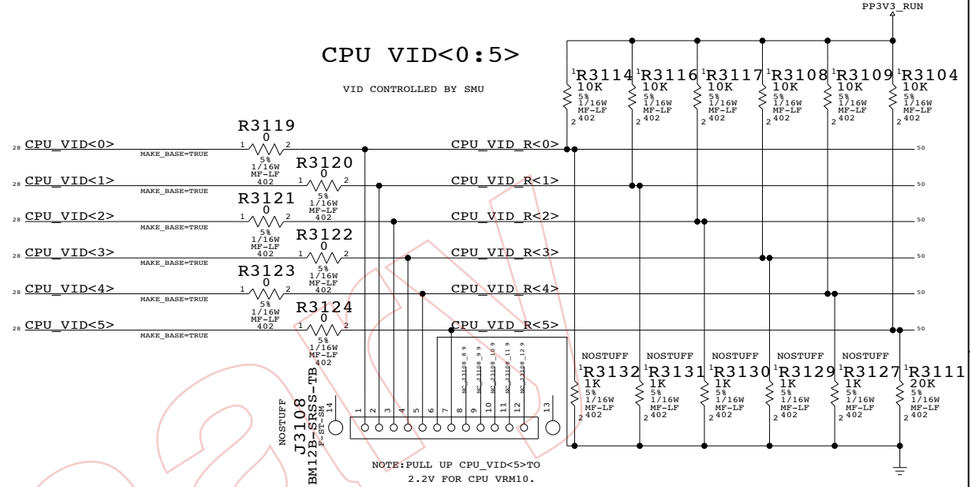
SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
Q63 NC'S THESE AS IT USES A SAT.		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
		CPU_TEMP0	P0.2	
		CPU_BYPASS	P0.3	
M23/M33 DOESN'T HAVE THOSE FANS.	NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3
	NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4
	NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_SENSE_V1	P1.1	
		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6
M23/M33 DOESN'T HAVE THIS FAN.	NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4
	NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN
	I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L
	SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN
	SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN — SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	SMU_CPU_NB_SEL	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF
		SLEWING*	P8.4	
	SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		PS9_5	P9.5	
		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L

CPU VID<0:5>

VID CONTROLLED BY SMU



NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

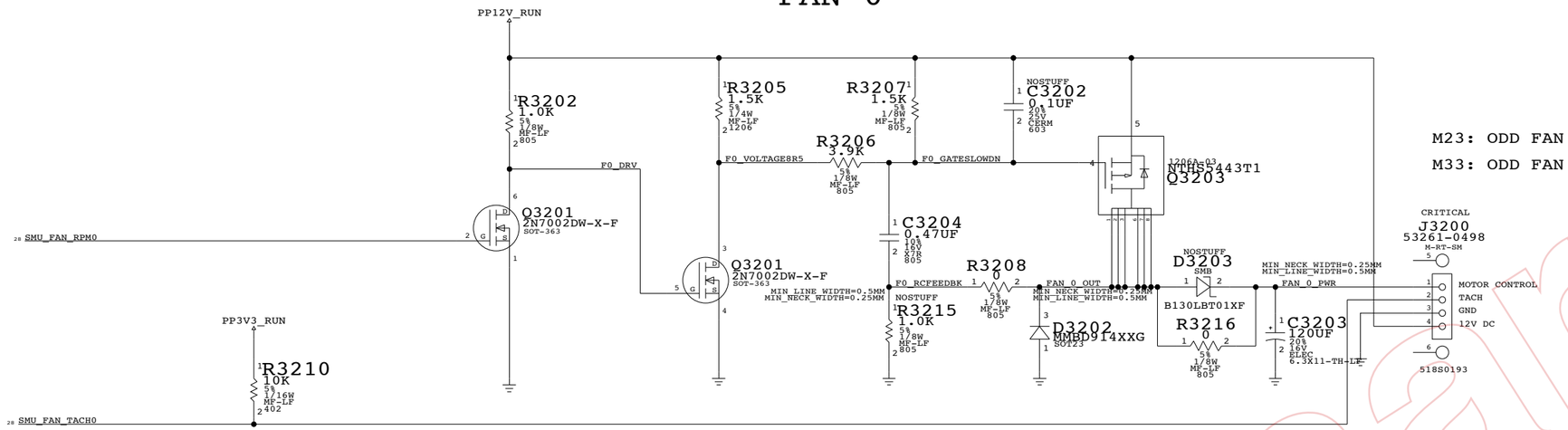
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

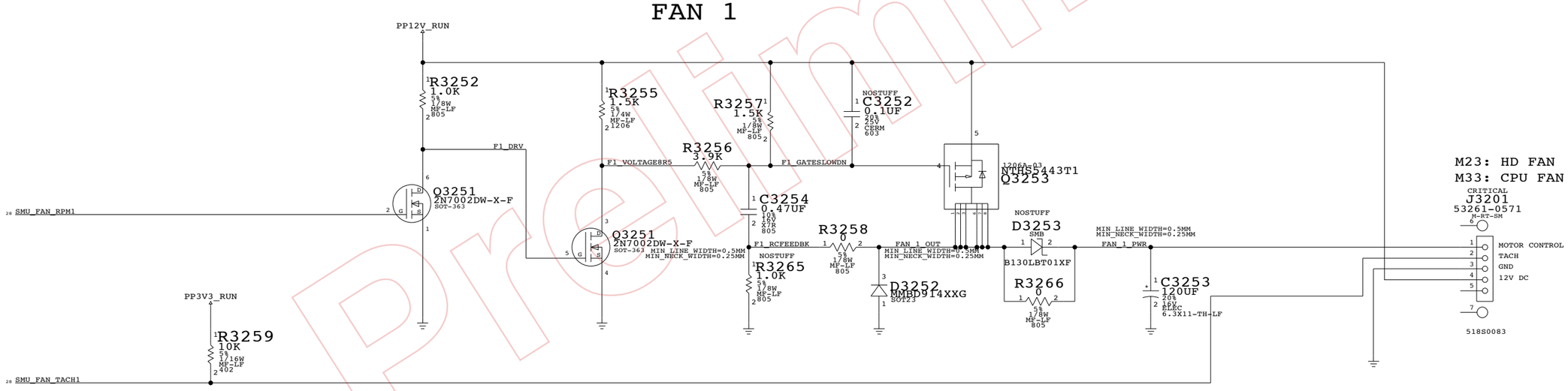
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 31 OF 154	

FAN 0



M23: ODD FAN
M33: ODD FAN

FAN 1



M23: HD FAN
M33: CPU FAN

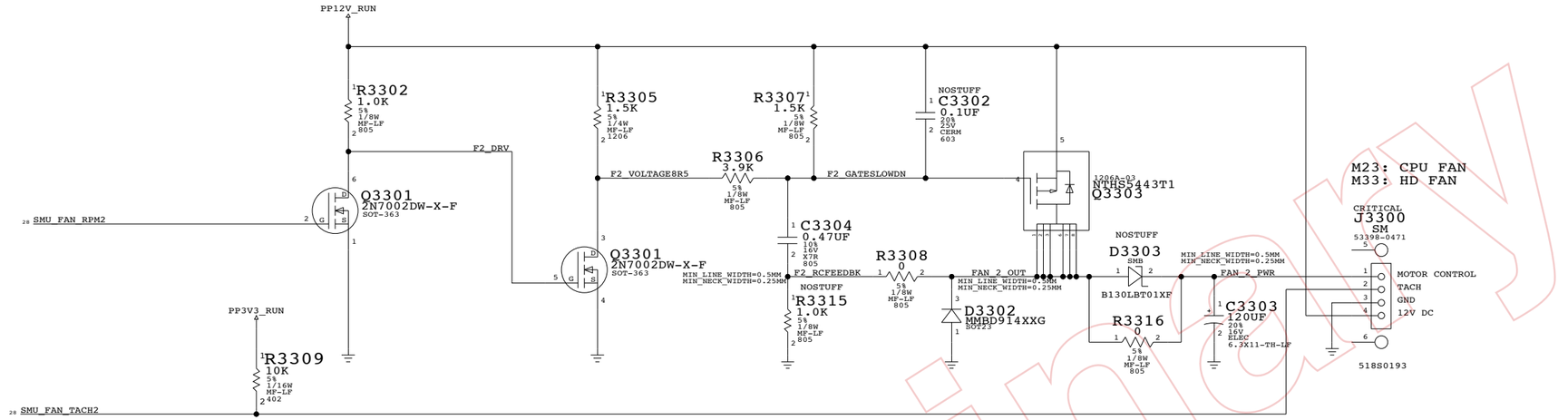
Fan 0, 1 & System Temp

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

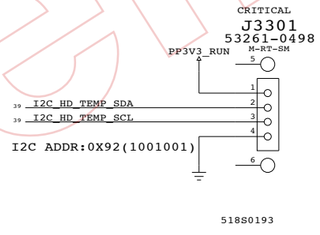
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 32 OF 154	

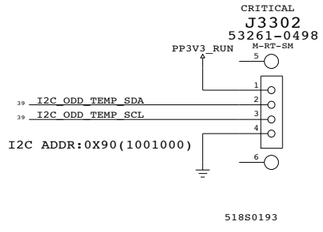
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR



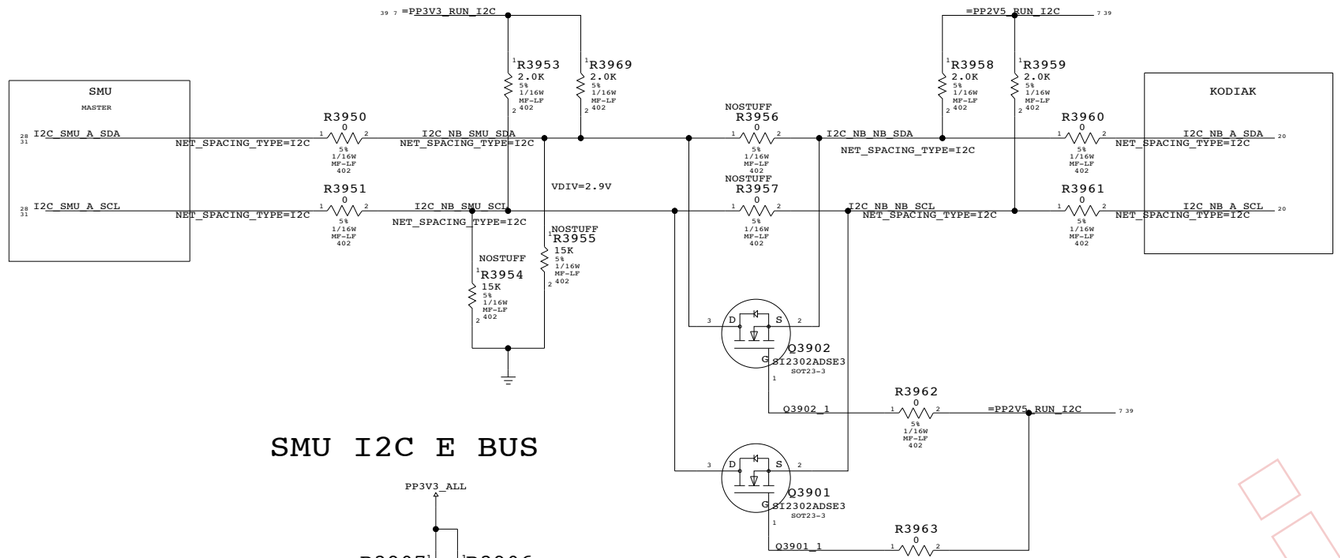
Fan 2 & HD Temp

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

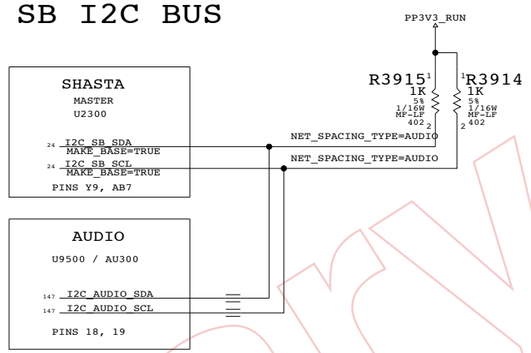
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 33 OF 154	

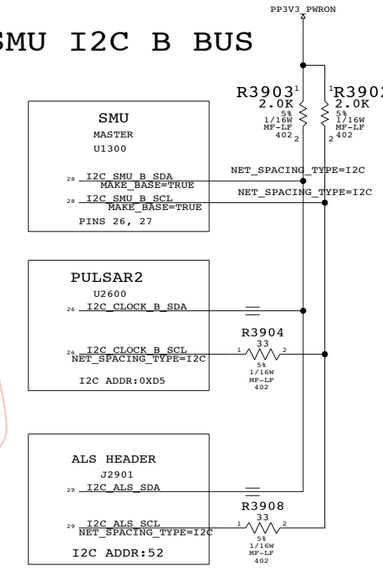
SMU AND NB I2C A BUS



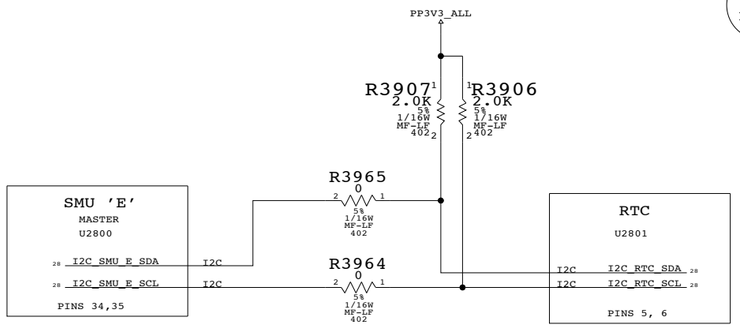
SB I2C BUS



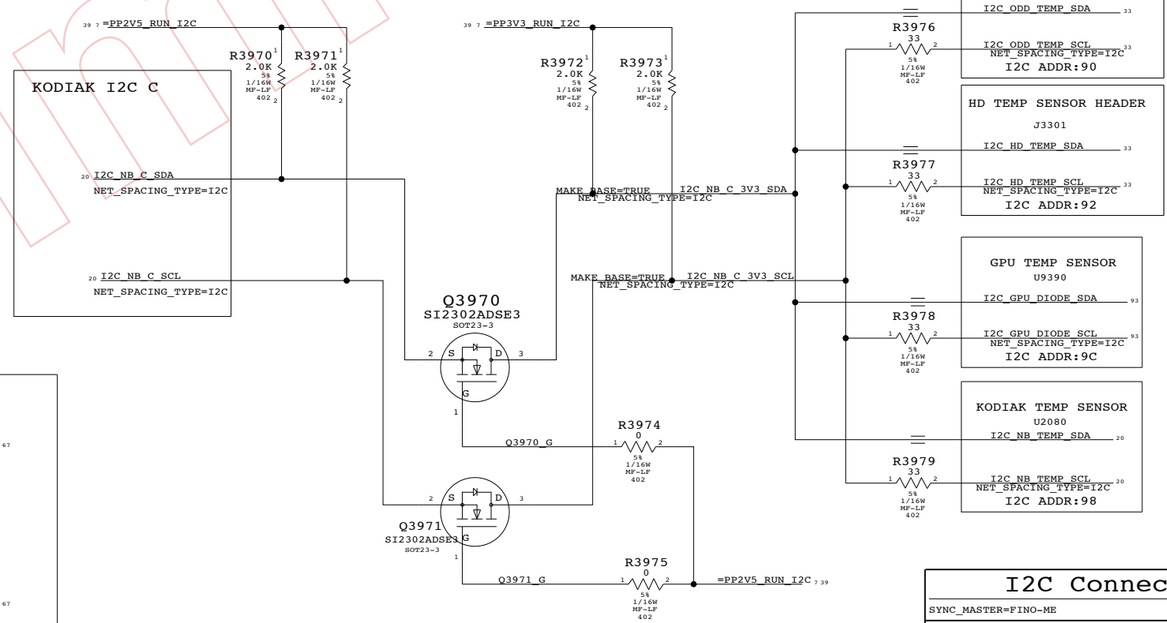
SMU I2C B BUS



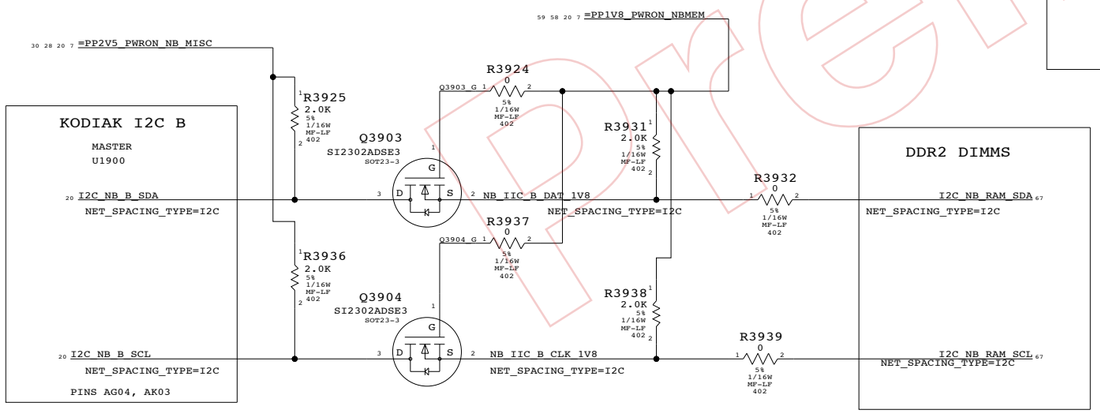
SMU I2C E BUS



NB I2C C BUS



NB I2C B BUS



I2C Connections

SYNC_MASTER=FINO-ME SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 39 OF 154	

Q63 APPLICATION IS PP1V5 PWRON

=PPV_EI_NB 7 41 42 56

XW4100 SM NO_TEST=YES 6 PP_VEINB P4MM SM 1 PP

PP4100

U1900
BGA
(7 OF 10)
PART 0
PWR/GND
KODIAK-ASIC-040812

AB01	GND_0	VD2_0	AB02
AB04	GND_1	VD2_1	AB05
AB07	GND_2	VD2_2	AB08
AB10	GND_3	VD2_3	AB11
AB12	GND_4	VD2_4	AB13
AD02	GND_5	VD2_5	AD01
AD05	GND_6	VD2_6	AD04
AD08	GND_7	VD2_7	AD07
AD11	GND_8	VD2_8	AD10
AD13	GND_9	VD2_9	AD12
AD17	GND_10	VD2_10	AD16
AD21	GND_11	VD2_11	AD20
AE15	GND_12	VD2_12	AE14
AE19	GND_13	VD2_13	AE18
AF07	GND_14	VD2_14	AF08
AF10	GND_15	VD2_15	AF11
AF13	GND_16	VD2_16	AF15
AF17	GND_17	VD2_17	AF19
AG11	GND_18	VD2_18	AG13
AG15	GND_19	VD2_19	AG17
AG19	GND_20	VD2_20	AG21
AH02	GND_21	VD2_21	AH04
AH05	GND_22	VD2_22	AH07
AH08	GND_23	VD2_23	AH09
AJ13	GND_24	VD2_24	AJ11
AJ17	GND_25	VD2_25	AJ15
AJ21	GND_26	VD2_26	AJ19
AK01	GND_27	VD2_27	AK02
AK04	GND_28	VD2_28	AK05
AK07	GND_29	VD2_29	AK09
AK11	GND_30	VD2_30	AK13
AK15	GND_31	VD2_31	AK17
AK19	GND_32	VD2_32	AK21
AM02	GND_33	VD2_33	AM01
AM05	GND_34	VD2_34	AM04
AM09	GND_35	VD2_35	AM07
AM13	GND_36	VD2_36	AM11
AM17	GND_37	VD2_37	AM15
AM21	GND_38	VD2_38	AM19
AN04	GND_39	VD2_39	AN05
AN07	GND_40	VD2_40	AN09
AN11	GND_41	VD2_41	AN13
AN15	GND_42	VD2_42	AN17
AN19	GND_43	VD2_43	AN21
AP01	GND_44	VD2_44	AP02
AR05	GND_45	VD2_45	AR03
AR09	GND_46	VD2_46	AR07
AR13	GND_47	VD2_47	AR11
AR17	GND_48	VD2_48	AR15
AR21	GND_49	VD2_49	AR19
AT03	GND_50	VD2_50	AT05
AT07	GND_51	VD2_51	AT09
AT11	GND_52	VD2_52	AT13
AT15	GND_53	VD2_53	AT17
AT19	GND_54	VD2_54	AT21
K01	GND_55	VD2_55	K02
K04	GND_56	VD2_56	K05
M02	GND_57	VD2_57	K08
M05	GND_58	VD2_58	M01
M08	GND_59	VD2_59	M04
P01	GND_60	VD2_60	M07
P04	GND_61	VD2_61	M10
P07	GND_62	VD2_62	P02
P10	GND_63	VD2_63	P05
P12	GND_64	VD2_64	P08
T02	GND_65	VD2_65	P11
T05	GND_66	VD2_66	P13
T08	GND_67	VD2_67	T01
T11	GND_68	VD2_68	T04
T13	GND_69	VD2_69	T07
V01	GND_70	VD2_70	T10
V04	GND_71	VD2_71	T12
V07	GND_72	VD2_72	V02
V10	GND_73	VD2_73	V05
V12	GND_74	VD2_74	V08
Y02	GND_75	VD2_75	V11
Y05	GND_76	VD2_76	V13
Y08	GND_77	VD2_77	Y01
Y11	GND_78	VD2_78	Y04
Y13	GND_79	VD2_79	Y07
AF01	GND_80	VD2_80	Y10
AF04	GND_81	VD2_81	Y12
AF21	GND_82		
AJ08	GND_83		
AJ09	GND_84		

Q63 APPLICATION IS PP1V5 PWRON

56 42 41 7 =PPV_EI_NB

C4168 C4146 C4143 C4139 C4137 C4113 C4112 C4106 C4122 C4100
C4169 C4147 C4145 C4140 C4138 C4114 C4110 C4107 C4133 C4111
C4170 C4149 C4148 C4142 C4141 C4115 C4109 C4108 C4155 C4144
C4171 C4161 C4159 C4152 C4150 C4125 C4118 C4116 C4181 C4166
C4172 C4162 C4160 C4153 C4151 C4126 C4124 C4117 C4101 C4177
C4174 C4165 C4163 C4157 C4154 C4127 C4123 C4104 C4102
C4173 C4167 C4164 C4158 C4156 C4128 C4121 C4120 C4105 C4103
C4180 C4179 C4178 C4176 C4175 C4136 C4135 C4134 C4130 C4129
C4132 C4131

All: 0.22UF 20% 6.3V X5R 402

KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

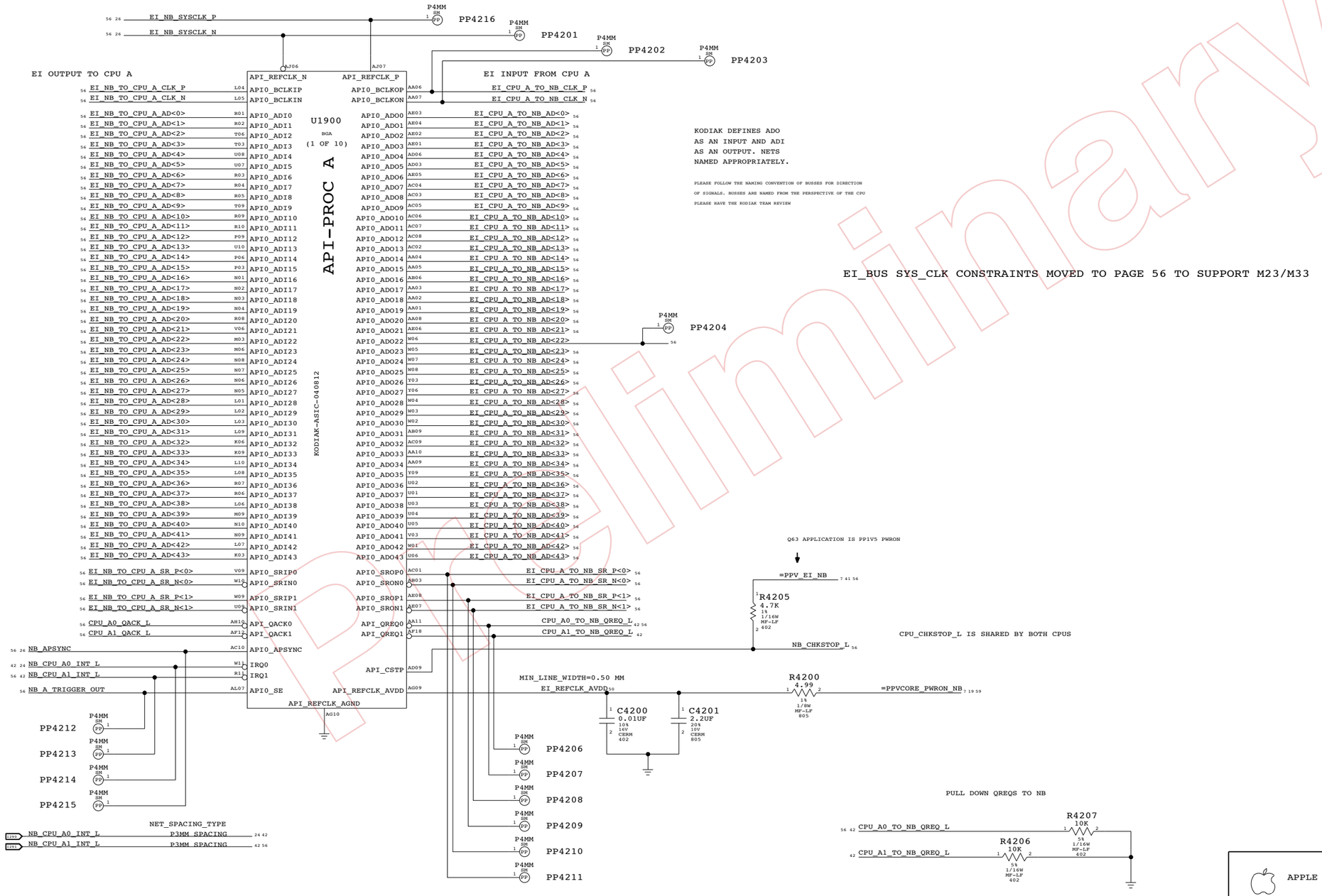
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT: 41	OF: 154

LAST_MODIFIED=Thu May 19 14:09:07 2005

DRAWING

TITLE=K51LOGBAA

NUMBER=V00A0360



56 EI_CPU_SYSCLK_P

PCB: PLACE R4303 AND R4301 AT PROCESSOR PINS

56 EI_CPU_SYSCLK_N

R22 SYSCLK* R22 SYSCLK

REMOVED BACKUP TERMINATION OPTIONS TO OPTIMIZE ROUTING.

OMIT
CRITICAL

U4300
CBGA
(1 OF 3)
NEO-10S-REV2
1.8GHZ-76C

56 9 EI_NB_TO_CPU_CLK_P	E24	EI_CLKI	EI_CLKO	D3	EI_CPU_TO_NB_CLK_P 9 56
56 9 EI_NB_TO_CPU_CLK_N	D23	EI_CLKI*	EI_CLKO*	E3	EI_CPU_TO_NB_CLK_N 9 56
56 EI_NB_TO_CPU_AD<0>	R21	EI_AD10	EI_AD00	E5	EI_CPU_TO_NB_AD<0> 56
56 EI_NB_TO_CPU_AD<1>	J21	EI_AD11	EI_AD01	E6	EI_CPU_TO_NB_AD<1> 56
56 EI_NB_TO_CPU_AD<2>	H22	EI_AD12	EI_AD02	E1	EI_CPU_TO_NB_AD<2> 56
56 EI_NB_TO_CPU_AD<3>	J23	EI_AD13	EI_AD03	L1	EI_CPU_TO_NB_AD<3> 56
56 EI_NB_TO_CPU_AD<4>	C13	EI_AD14	EI_AD04	K5	EI_CPU_TO_NB_AD<4> 56
56 EI_NB_TO_CPU_AD<5>	A13	EI_AD15	EI_AD05	K4	EI_CPU_TO_NB_AD<5> 56
56 EI_NB_TO_CPU_AD<6>	K22	EI_AD16	EI_AD06	K2	EI_CPU_TO_NB_AD<6> 56
56 EI_NB_TO_CPU_AD<7>	K23	EI_AD17	EI_AD07	K1	EI_CPU_TO_NB_AD<7> 56
56 EI_NB_TO_CPU_AD<8>	J24	EI_AD18	EI_AD08	H1	EI_CPU_TO_NB_AD<8> 56
56 EI_NB_TO_CPU_AD<9>	G25	EI_AD19	EI_AD09	G4	EI_CPU_TO_NB_AD<9> 56
56 EI_NB_TO_CPU_AD<10>	F23	EI_AD110	EI_AD010	F2	EI_CPU_TO_NB_AD<10> 56
56 EI_NB_TO_CPU_AD<11>	G23	EI_AD111	EI_AD011	F4	EI_CPU_TO_NB_AD<11> 56
56 EI_NB_TO_CPU_AD<12>	D22	EI_AD112	EI_AD012	E7	EI_CPU_TO_NB_AD<12> 56
56 EI_NB_TO_CPU_AD<13>	G24	EI_AD113	EI_AD013	E8	EI_CPU_TO_NB_AD<13> 56
56 EI_NB_TO_CPU_AD<14>	E19	EI_AD114	EI_AD014	H8	EI_CPU_TO_NB_AD<14> 56
56 EI_NB_TO_CPU_AD<15>	B15	EI_AD115	EI_AD015	G11	EI_CPU_TO_NB_AD<15> 56
56 EI_NB_TO_CPU_AD<16>	A14	EI_AD116	EI_AD016	E12	EI_CPU_TO_NB_AD<16> 56
56 EI_NB_TO_CPU_AD<17>	C15	EI_AD117	EI_AD017	A11	EI_CPU_TO_NB_AD<17> 56
56 EI_NB_TO_CPU_AD<18>	E15	EI_AD118	EI_AD018	E10	EI_CPU_TO_NB_AD<18> 56
56 EI_NB_TO_CPU_AD<19>	A15	EI_AD119	EI_AD019	C11	EI_CPU_TO_NB_AD<19> 56
56 EI_NB_TO_CPU_AD<20>	F22	EI_AD120	EI_AD020	G1	EI_CPU_TO_NB_AD<20> 56
56 EI_NB_TO_CPU_AD<21>	E20	EI_AD121	EI_AD021	C5	EI_CPU_TO_NB_AD<21> 56
56 EI_NB_TO_CPU_AD<22>	E21	EI_AD122	EI_AD022	B5	EI_CPU_TO_NB_AD<22> 56
56 EI_NB_TO_CPU_AD<23>	B23	EI_AD123	EI_AD023	D5	EI_CPU_TO_NB_AD<23> 56
56 EI_NB_TO_CPU_AD<24>	B24	EI_AD124	EI_AD024	A5	EI_CPU_TO_NB_AD<24> 56
56 EI_NB_TO_CPU_AD<25>	F21	EI_AD125	EI_AD025	A2	EI_CPU_TO_NB_AD<25> 56
56 EI_NB_TO_CPU_AD<26>	E17	EI_AD126	EI_AD026	C8	EI_CPU_TO_NB_AD<26> 56
56 EI_NB_TO_CPU_AD<27>	B19	EI_AD127	EI_AD027	D8	EI_CPU_TO_NB_AD<27> 56
56 EI_NB_TO_CPU_AD<28>	C18	EI_AD128	EI_AD028	C12	EI_CPU_TO_NB_AD<28> 56
56 EI_NB_TO_CPU_AD<29>	C13	EI_AD129	EI_AD029	A12	EI_CPU_TO_NB_AD<29> 56
56 EI_NB_TO_CPU_AD<30>	D19	EI_AD130	EI_AD030	B5	EI_CPU_TO_NB_AD<30> 56
56 EI_NB_TO_CPU_AD<31>	B21	EI_AD131	EI_AD031	B4	EI_CPU_TO_NB_AD<31> 56
56 EI_NB_TO_CPU_AD<32>	D20	EI_AD132	EI_AD032	C4	EI_CPU_TO_NB_AD<32> 56
56 EI_NB_TO_CPU_AD<33>	A22	EI_AD133	EI_AD033	A7	EI_CPU_TO_NB_AD<33> 56
56 EI_NB_TO_CPU_AD<34>	C19	EI_AD134	EI_AD034	C9	EI_CPU_TO_NB_AD<34> 56
56 EI_NB_TO_CPU_AD<35>	C16	EI_AD135	EI_AD035	C6	EI_CPU_TO_NB_AD<35> 56
56 EI_NB_TO_CPU_AD<36>	A16	EI_AD136	EI_AD036	C7	EI_CPU_TO_NB_AD<36> 56
56 EI_NB_TO_CPU_AD<37>	A23	EI_AD137	EI_AD037	A4	EI_CPU_TO_NB_AD<37> 56
56 EI_NB_TO_CPU_AD<38>	A19	EI_AD138	EI_AD038	A8	EI_CPU_TO_NB_AD<38> 56
56 EI_NB_TO_CPU_AD<39>	A18	EI_AD139	EI_AD039	D9	EI_CPU_TO_NB_AD<39> 56
56 EI_NB_TO_CPU_AD<40>	A17	EI_AD140	EI_AD040	A10	EI_CPU_TO_NB_AD<40> 56
56 EI_NB_TO_CPU_AD<41>	A21	EI_AD141	EI_AD041	C10	EI_CPU_TO_NB_AD<41> 56
56 EI_NB_TO_CPU_AD<42>	C14	EI_AD142	EI_AD042	E9	EI_CPU_TO_NB_AD<42> 56
56 EI_NB_TO_CPU_AD<43>	A20	EI_AD143	EI_AD043	E4	EI_CPU_TO_NB_AD<43> 56
56 9 EI_NB_TO_CPU_SR_P<0>	L24	EI_SRI0	EI_SRO0	L3	EI_CPU_TO_NB_SR_P<0> 56
56 9 EI_NB_TO_CPU_SR_N<0>	K24	EI_SRI0*	EI_SRO0*	L2	EI_CPU_TO_NB_SR_N<0> 56
56 9 EI_NB_TO_CPU_SR_P<1>	L23	EI_SRI1	EI_SRO1	G1	EI_CPU_TO_NB_SR_P<1> 9 56
56 EI_NB_TO_CPU_SR_N<1>	L22	EI_SRI1*	EI_SRO1*	F1	EI_CPU_TO_NB_SR_N<1> 9 56
56 CPU_QACK_L	V21	QACK*	QREQ*	AB12	CPU_QREQ_L 43
56 9 CPU_CHKSTOP_L	R20	CHKSTOP*	INT*	AB19	CPU_INT_L 56
56 EI_CPU_TBEN_CLK	AD17	TBEN			
56 CPU_APSYNCOUT	AD14	APSYNCOUT	APSYNCIN	AA10	EI_CPU_APSYNC 56
29 CPU_HRESET_L	V23	HRESET*			
56 CPU_SRESET_L	AB4	SRESET*	IIC_SCL	AA20	I2C_CPU_SCL 47
47 PROC_THERM_INT_L	V22	THERM_INT*	IIC_SDA	Y21	I2C_CPU_SDA 47
47 PROCID0	L19	PROCID0	I2CGO	A22	I2CGO 47
47 PROCID1	R19	PROCID1	CKTERMDIS	AA14	CKTERMDIS_L 47
47 PROCID2	R18	PROCID2	EI_DISABLE	Z20	EI_DISABLE 47
56 47 CPU_TRIGGER_IN	R21	TRIGGER_IN	BUSCFG0	AA19	BUSCFG0 47
56 CPU_TRIGGER_OUT	R19	TRIGGER_OUT	BUSCFG1	AC19	BUSCFG1 47
CPU_AFN	AA12	AFN	BUSCFG2	AA16	BUSCFG2 47
56 AVPRESET_L	W22	AVPRESET*	ATTENTION	AB12	CPU_ATTENTION 56
43 BIMODE_L	AC20	BIMODE*	GPUL_DBG	AA22	GPUL_DBG 47
43 C1UNDGLOBAL	AC19	C1UNDGLOBAL	SPARE2	Z8 UNDEFINED	CPU_SPARE2 47
43 C2UNDGLOBAL	AC15	C2UNDGLOBAL	TCK	AD21	JTAG_CPU_TCK 9 30
43 D2Z_L	U19	D2Z*	TDI	AB21	JTAG_CPU_TDI 9 30
47 LSSDMODE	AB5	LSSDMODE	TDO	AD13	JTAG_CPU_TDO 9 30 47
47 LSSDSCANENABLE	U18	LSSDSCANENABLE	TMS	AD22	JTAG_CPU_TMS 9 30
47 LSSDSTOPCZENABLE	AD6	LSSDSTOPCZENABLE	TRST*	W20	JTAG_CPU_TRST_L 9 47
47 LSSDSTOPCZSTARENABLE	AD3	LSSDSTOPCZSTARENABLE	BYPASS*	V24	CPU_BYPASS_L 29
47 LSSDSTOPENABLE	AD13	LSSDSTOPENABLE	PLLCLK	Y25	PLLCLOCK 8 9
56 CPU_MCP_L	AD16	MCP*	PLLMULT	AA8	PLLMULT 47
56 CPU_PSRO	Y23	PSRO1	PLLRANGE0	AB7	PLLRANGE0 47
56 CPU_PSRO_ENABLE	V5	PSRO_ENABLE	PLLRANGE1	AA9	PLLRANGE1 47
47 PULSESEL0	AC8	PULSESEL0	PLLTEST	W2	PLLTEST 47
43 PULSESEL1	AB11	PULSESEL1	PLLTESTOUT	Y19	PLLTESTOUT 47
43 PULSESEL2	AC10	PULSESEL2	SPARE	AA13	CPU_SPARE 47
43 RAMSTOPENABLE	AB6	RAMSTOPENABLE			
47 RI_L	AC9	RI*			
47 SYNCENABLE	AB23	SYNCENABLE*			

PCB: MATCH APSYNC LENGTH TO SYSCLK

56 55 52 50 49 48 =PPVCORE_CPU

PG 49 & 52 HAVE MORE CAPS

C4353 1UF 10% 6.3V CERM 402	C4347 1UF 10% 6.3V CERM 402	C4345 1UF 10% 6.3V CERM 402	C4339 1UF 10% 6.3V CERM 402	C4337 1UF 10% 6.3V CERM 402	C4328 1UF 10% 6.3V CERM 402	C4324 1UF 10% 6.3V CERM 402	C4320 1UF 10% 6.3V CERM 402	C4314 1UF 10% 6.3V CERM 402	C4312 1UF 10% 6.3V CERM 402
C4354 1UF 10% 6.3V CERM 402	C4348 1UF 10% 6.3V CERM 402	C4346 1UF 10% 6.3V CERM 402	C4340 1UF 10% 6.3V CERM 402	C4338 1UF 10% 6.3V CERM 402	C4329 1UF 10% 6.3V CERM 402	C4325 1UF 10% 6.3V CERM 402	C4321 1UF 10% 6.3V CERM 402	C4315 1UF 10% 6.3V CERM 402	C4313 1UF 10% 6.3V CERM 402
C4355 1UF 10% 6.3V CERM 402	C4351 1UF 10% 6.3V CERM 402	C4349 1UF 10% 6.3V CERM 402	C4343 1UF 10% 6.3V CERM 402	C4341 1UF 10% 6.3V CERM 402	C4330 1UF 10% 6.3V CERM 402	C4326 1UF 10% 6.3V CERM 402	C4322 1UF 10% 6.3V CERM 402	C4318 1UF 10% 6.3V CERM 402	C4316 1UF 10% 6.3V CERM 402
C4356 1UF 10% 6.3V CERM 402	C4352 1UF 10% 6.3V CERM 402	C4350 1UF 10% 6.3V CERM 402	C4344 1UF 10% 6.3V CERM 402	C4342 1UF 10% 6.3V CERM 402	C4331 1UF 10% 6.3V CERM 402	C4327 1UF 10% 6.3V CERM 402	C4323 1UF 10% 6.3V CERM 402	C4319 1UF 10% 6.3V CERM 402	C4317 1UF 10% 6.3V CERM 402
C4300 1UF 10% 6.3V CERM 402	C4360 1UF 10% 6.3V CERM 402	C4359 1UF 10% 6.3V CERM 402	C4358 1UF 10% 6.3V CERM 402	C4357 1UF 10% 6.3V CERM 402	C4336 1UF 10% 6.3V CERM 402	C4335 1UF 10% 6.3V CERM 402	C4334 1UF 10% 6.3V CERM 402	C4333 1UF 10% 6.3V CERM 402	C4332 1UF 10% 6.3V CERM 402
C4311 1UF 10% 6.3V CERM 402	C4310 1UF 10% 6.3V CERM 402	C4309 1UF 10% 6.3V CERM 402	C4308 1UF 10% 6.3V CERM 402	C4307 1UF 10% 6.3V CERM 402	C4306 1UF 10% 6.3V CERM 402	C4305 1UF 10% 6.3V CERM 402	C4304 1UF 10% 6.3V CERM 402	C4303 1UF 10% 6.3V CERM 402	C4302 1UF 10% 6.3V CERM 402

QREQ_L AND SUSPENDREQ_L AND HACK
SAME AS Q45

30 28 7 =PP3V3_PWRON_SMU

C4372 0.1UF 10% 10V CERM 402

CRITICAL
U4310
74LVC1G66DBVG4
SOT23-5
TI

VCC 5 | 1 | 2 | 4 | GND 3

43 CPU_QREQ_L → CPU_TO_NB_QREQ_L 56

30 28 24 SMU_SUSPENDREQ_L

NOSTUFF
R4310
0
5% 1/16W MF-LF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U4310	PERICOM ANALOG SWITCH CRITICAL

CPU EI AND IO

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 43 OF 154	

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI_NB_TO_CPU_B_CLK_P AT08 API1_BCLKIP
EI_NB_TO_CPU_B_CLK_N AR08 API1_BCLKIN
API1_BCLKOP AT16 EI_CPU_B_TO_NB_CLK_P
API1_BCLKON AR16 EI_CPU_B_TO_NB_CLK_N

EI_NB_TO_CPU_B_AD<0> AM12 API1_ADI0
EI_NB_TO_CPU_B_AD<1> AN12 API1_ADI1
EI_NB_TO_CPU_B_AD<2> AL12 API1_ADI2
EI_NB_TO_CPU_B_AD<3> AK12 API1_ADI3
EI_NB_TO_CPU_B_AD<4> AP11 API1_ADI4
EI_NB_TO_CPU_B_AD<5> AL11 API1_ADI5
EI_NB_TO_CPU_B_AD<6> AP12 API1_ADI6
EI_NB_TO_CPU_B_AD<7> AR12 API1_ADI7
EI_NB_TO_CPU_B_AD<8> AT12 API1_ADI8
EI_NB_TO_CPU_B_AD<9> AH12 API1_ADI9
EI_NB_TO_CPU_B_AD<10> AG12 API1_ADI10
EI_NB_TO_CPU_B_AD<11> AH13 API1_ADI11
EI_NB_TO_CPU_B_AD<12> AJ12 API1_ADI12
EI_NB_TO_CPU_B_AD<13> AG14 API1_ADI13
EI_NB_TO_CPU_B_AD<14> AM10 API1_ADI14
EI_NB_TO_CPU_B_AD<15> AL10 API1_ADI15
EI_NB_TO_CPU_B_AD<16> AN10 API1_ADI16
EI_NB_TO_CPU_B_AD<17> AP10 API1_ADI17
EI_NB_TO_CPU_B_AD<18> AR10 API1_ADI18
EI_NB_TO_CPU_B_AD<19> AT10 API1_ADI19
EI_NB_TO_CPU_B_AD<20> AK10 API1_ADI20
EI_NB_TO_CPU_B_AD<21> AJ10 API1_ADI21
EI_NB_TO_CPU_B_AD<22> AM08 API1_ADI22
EI_NB_TO_CPU_B_AD<23> AN08 API1_ADI23
EI_NB_TO_CPU_B_AD<24> AL08 API1_ADI24
EI_NB_TO_CPU_B_AD<25> AP07 API1_ADI25
EI_NB_TO_CPU_B_AD<26> AT06 API1_ADI26
EI_NB_TO_CPU_B_AD<27> AR06 API1_ADI27
EI_NB_TO_CPU_B_AD<28> AP08 API1_ADI28
EI_NB_TO_CPU_B_AD<29> AT04 API1_ADI29
EI_NB_TO_CPU_B_AD<30> AR04 API1_ADI30
EI_NB_TO_CPU_B_AD<31> AP05 API1_ADI31
EI_NB_TO_CPU_B_AD<32> AM06 API1_ADI32
EI_NB_TO_CPU_B_AD<33> AN06 API1_ADI33
EI_NB_TO_CPU_B_AD<34> AP06 API1_ADI34
EI_NB_TO_CPU_B_AD<35> AP04 API1_ADI35
EI_NB_TO_CPU_B_AD<36> AM03 API1_ADI36
EI_NB_TO_CPU_B_AD<37> AN01 API1_ADI37
EI_NB_TO_CPU_B_AD<38> AL06 API1_ADI38
EI_NB_TO_CPU_B_AD<39> AL05 API1_ADI39
EI_NB_TO_CPU_B_AD<40> AL04 API1_ADI40
EI_NB_TO_CPU_B_AD<41> AL03 API1_ADI41
EI_NB_TO_CPU_B_AD<42> AN02 API1_ADI42
EI_NB_TO_CPU_B_AD<43> AN03 API1_ADI43

U1900
BGA
(2 OF 10)
API-PROC B
KODIAK-ASIC-040812

API1_ADO0 AP20 EI_CPU_B_TO_NB_AD<0>
API1_ADO1 AN20 EI_CPU_B_TO_NB_AD<1>
API1_ADO2 AR20 EI_CPU_B_TO_NB_AD<2>
API1_ADO3 AT20 EI_CPU_B_TO_NB_AD<3>
API1_ADO4 AL19 EI_CPU_B_TO_NB_AD<4>
API1_ADO5 AP19 EI_CPU_B_TO_NB_AD<5>
API1_ADO6 AM20 EI_CPU_B_TO_NB_AD<6>
API1_ADO7 AM18 EI_CPU_B_TO_NB_AD<7>
API1_ADO8 AL18 EI_CPU_B_TO_NB_AD<8>
API1_ADO9 AN18 EI_CPU_B_TO_NB_AD<9>
API1_ADO10 AP18 EI_CPU_B_TO_NB_AD<10>
API1_ADO11 AR18 EI_CPU_B_TO_NB_AD<11>
API1_ADO12 AT18 EI_CPU_B_TO_NB_AD<12>
API1_ADO13 AK18 EI_CPU_B_TO_NB_AD<13>
API1_ADO14 AP17 EI_CPU_B_TO_NB_AD<14>
API1_ADO15 AL17 EI_CPU_B_TO_NB_AD<15>
API1_ADO16 AH20 EI_CPU_B_TO_NB_AD<16>
API1_ADO17 AJ20 EI_CPU_B_TO_NB_AD<17>
API1_ADO18 AK20 EI_CPU_B_TO_NB_AD<18>
API1_ADO19 AH19 EI_CPU_B_TO_NB_AD<19>
API1_ADO20 AG20 EI_CPU_B_TO_NB_AD<20>
API1_ADO21 AL20 EI_CPU_B_TO_NB_AD<21>
API1_ADO22 AM16 EI_CPU_B_TO_NB_AD<22>
API1_ADO23 AN16 EI_CPU_B_TO_NB_AD<23>
API1_ADO24 AL16 EI_CPU_B_TO_NB_AD<24>
API1_ADO25 AK16 EI_CPU_B_TO_NB_AD<25>
API1_ADO26 AP15 EI_CPU_B_TO_NB_AD<26>
API1_ADO27 AL15 EI_CPU_B_TO_NB_AD<27>
API1_ADO28 AP16 EI_CPU_B_TO_NB_AD<28>
API1_ADO29 AM14 EI_CPU_B_TO_NB_AD<29>
API1_ADO30 AL14 EI_CPU_B_TO_NB_AD<30>
API1_ADO31 AN14 EI_CPU_B_TO_NB_AD<31>
API1_ADO32 AP14 EI_CPU_B_TO_NB_AD<32>
API1_ADO33 AR14 EI_CPU_B_TO_NB_AD<33>
API1_ADO34 AT14 EI_CPU_B_TO_NB_AD<34>
API1_ADO35 AK14 EI_CPU_B_TO_NB_AD<35>
API1_ADO36 AP13 EI_CPU_B_TO_NB_AD<36>
API1_ADO37 AL13 EI_CPU_B_TO_NB_AD<37>
API1_ADO38 AG16 EI_CPU_B_TO_NB_AD<38>
API1_ADO39 AH15 EI_CPU_B_TO_NB_AD<39>
API1_ADO40 AJ14 EI_CPU_B_TO_NB_AD<40>
API1_ADO41 AH14 EI_CPU_B_TO_NB_AD<41>
API1_ADO42 AH16 EI_CPU_B_TO_NB_AD<42>
API1_ADO43 AH17 EI_CPU_B_TO_NB_AD<43>

API1_SROP0 AG18 EI_CPU_B_TO_NB_SR_P<0>
API1_SRON0 AJ16 EI_CPU_B_TO_NB_SR_N<0>
API1_SROP1 AJ18 EI_CPU_B_TO_NB_SR_P<1>
API1_SRON1 AH18 EI_CPU_B_TO_NB_SR_N<1>

CPU_B0_QACK_L AF19 API_QACK2
CPU_B1_QACK_L AC1 API_QACK3
API_QREQ2 AF16 CPU_B0_TO_NB_QREQ_L
API_QREQ3 AF20 CPU_B1_TO_NB_QREQ_L

NB_CPU_B0_INT_L N1 IRQ2
NB_CPU_B1_INT_L U1 IRQ3
TP_NB_APSYNC AH11 API1_APSYNC
NB_B_TRIGGER_OUT AK08 API1_SE

WIRE TP_NB_APSYNC TO A TEST POINT

PP4406 PP4407 PP4408 PP4410 PP4411 PP4413 PP4400 PP4401 PP4402 PP4403 PP4404 PP4405
P4MM SM 1 PP

NET_SPACING_TYPE
NB_CPU_B0_INT_L P3MM_SPACING
NB_CPU_B1_INT_L P3MM_SPACING

KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT ELECTRICAL_CONSTRAINT_SET FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

PULL DOWN QREQS TO NB

CPU_B0_TO_NB_QREQ_L
CPU_B1_TO_NB_QREQ_L
R4407 10K 5% 1/16W MF-LF 402
R4406 10K 5% 1/16W MF-LF 402

KODIAK EI B
SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 44 OF 154

LAST_MODIFIED=Thu May 19 14:09:09 2005

=PPV_EI_CPU 7 29 30 47 48 56

PULLUPS

43 C1UNDGLOBAL
- NOSTUFF R4777 4.7K 5% 1/16W MF-LF 402
- R4743 4.7K 5% 1/16W MF-LF 402

43 C2UNDGLOBAL
- NOSTUFF R4779 4.7K 5% 1/16W MF-LF 402
- R4769 4.7K 5% 1/16W MF-LF 402

43 PLLTEST
- NOSTUFF R4763 4.7K 5% 1/16W MF-LF 402
- R4761 4.7K 5% 1/16W MF-LF 402

43 CKTERMDIS_L
- NOSTUFF R4775 4.7K 5% 1/16W MF-LF 402
- R4773 4.7K 5% 1/16W MF-LF 402

43 GPUL_DBG
- R4740 4.7K 5% 1/16W MF-LF 402
- NOSTUFF R4742 4.7K 5% 1/16W MF-LF 402

M23/M33 IS JTAG ONLY, NO I2C

43 JTAG_CPU_TRST_L — R4709 4.7K 5% 1/16W MF-LF 402
43 BIMODE_L — R4731 4.7K 5% 1/16W MF-LF 402
43 DI2_L — R4733 4.7K 5% 1/16W MF-LF 402
43 RI_L — R4735 4.7K 5% 1/16W MF-LF 402
43 PROC_THERM_INT_L — R4765 4.7K 5% 1/16W MF-LF 402
43 I2CGO — R4787 4.7K 5% 1/16W MF-LF 402
43 I2C_CPU_SCL — R4788 4.7K 5% 1/16W MF-LF 402
43 I2C_CPU_SDA — R4789 4.7K 5% 1/16W MF-LF 402
43 30 9 JTAG_CPU_TDO — R4790 4.7K 5% 1/16W MF-LF 402

PULLDOWNS

43 CPU_SPARE2 — NOSTUFF R4739 0 5% 1/16W MF-LF 402
43 LSSDMODE — R4745 4.7K 5% 1/16W MF-LF 402
43 LSSDSCANENABLE — R4741 4.7K 5% 1/16W MF-LF 402
43 LSSDSTOPC2ENABLE — R4747 4.7K 5% 1/16W MF-LF 402
43 LSSDSTOPC2STARENABLE — R4749 4.7K 5% 1/16W MF-LF 402
43 LSSDSTOPENABLE — R4751 4.7K 5% 1/16W MF-LF 402
43 SYNCENABLE — R4737 4.7K 5% 1/16W MF-LF 402
43 RAMSTOPENABLE — R4755 4.7K 5% 1/16W MF-LF 402
43 CPU_SPARE — NOSTUFF R4767 4.7K 5% 1/16W MF-LF 402
56 43 CPU_TRIGGER_IN — R4781 4.7K 5% 1/16W MF-LF 402
43 PULSESEL0 — R4703 4.7K 5% 1/16W MF-LF 402
43 PULSESEL1 — R4705 4.7K 5% 1/16W MF-LF 402
43 PULSESEL2 — R4707 4.7K 5% 1/16W MF-LF 402
43 PROCID0 — R4702 4.7K 5% 1/16W MF-LF 402
43 PROCID1 — R4704 4.7K 5% 1/16W MF-LF 402
43 PROCID2 — R4706 4.7K 5% 1/16W MF-LF 402
43 PLLTESTOUT — NOSTUFF R4771 4.7K 5% 1/16W MF-LF 402

=PPV_EI_CPU 7 29 30 47 48 56
1 R4768 10K 5% 1/16W MF-LF 2 402

NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	>= 1.8 GHZ *
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION

56 48 47 30 29 7 =PPV_EI_CPU

SEE STUFFING OPTIONS ABOVE

1 OMIT R4708 1K 5% 1/16W MF-LF 2 402
1 OMIT R4710 1K 5% 1/16W MF-LF 2 402
1 OMIT R4712 1K 5% 1/16W MF-LF 2 402
1 OMIT R4714 1K 5% 1/16W MF-LF 2 402
1 OMIT R4716 1K 5% 1/16W MF-LF 2 402
1 OMIT R4718 1K 5% 1/16W MF-LF 2 402
1 OMIT R4720 1K 5% 1/16W MF-LF 2 402
1 OMIT R4722 1K 5% 1/16W MF-LF 2 402

43 BUSCFG0
43 BUSCFG1
43 BUSCFG2
43 PLLRANGE0
43 PLLRANGE1
43 PLLMULT
43 EI_DISABLE
43 AVPRESET_L

1 OMIT R4724 1K 5% 1/16W MF-LF 2 402
1 OMIT R4726 1K 5% 1/16W MF-LF 2 402
1 OMIT R4728 1K 5% 1/16W MF-LF 2 402
1 OMIT R4730 1K 5% 1/16W MF-LF 2 402
1 OMIT R4732 1K 5% 1/16W MF-LF 2 402
1 OMIT R4734 1K 5% 1/16W MF-LF 2 402
1 OMIT R4736 1K 5% 1/16W MF-LF 2 402
1 OMIT R4738 1K 5% 1/16W MF-LF 2 402

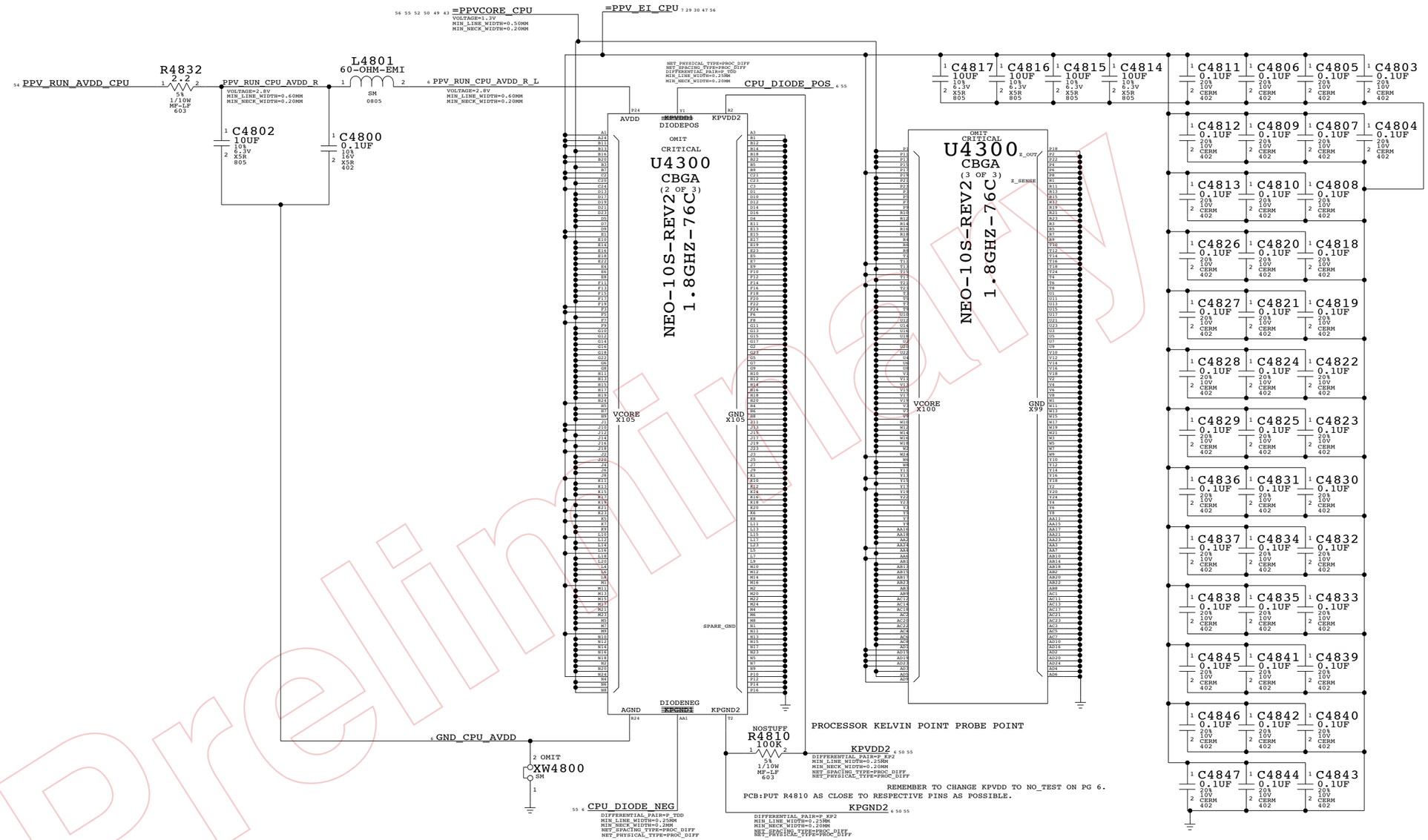
CPU STRAPS

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	47	154



CPU POWER AND BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	48	154

56 55 52 50 48 43 =PPVCORE_CPU

C4922 1UF 10% 6.3V CERM 402	C4921 1UF 10% 6.3V CERM 402	C4920 1UF 10% 6.3V CERM 402	C4919 1UF 10% 6.3V CERM 402	C4918 1UF 10% 6.3V CERM 402	C4917 1UF 10% 6.3V CERM 402	C4916 1UF 10% 6.3V CERM 402	C4915 1UF 10% 6.3V CERM 402	C4912 1UF 10% 6.3V CERM 402	C4900 1UF 10% 6.3V CERM 402
C4993 1UF 10% 6.3V CERM 402	C4968 1UF 10% 6.3V CERM 402	C4961 1UF 10% 6.3V CERM 402	C4959 1UF 10% 6.3V CERM 402	C4935 1UF 10% 6.3V CERM 402	C4932 1UF 10% 6.3V CERM 402	C4926 1UF 10% 6.3V CERM 402	C4924 1UF 10% 6.3V CERM 402	C4945 1UF 10% 6.3V CERM 402	C4923 1UF 10% 6.3V CERM 402
C4994 1UF 10% 6.3V CERM 402	C4969 1UF 10% 6.3V CERM 402	C4964 1UF 10% 6.3V CERM 402	C4960 1UF 10% 6.3V CERM 402	C4936 1UF 10% 6.3V CERM 402	C4933 1UF 10% 6.3V CERM 402	C4927 1UF 10% 6.3V CERM 402	C4925 1UF 10% 6.3V CERM 402	C4956 1UF 10% 6.3V CERM 402	C4934 1UF 10% 6.3V CERM 402
C4995 1UF 10% 6.3V CERM 402	C4971 1UF 10% 6.3V CERM 402	C4965 1UF 10% 6.3V CERM 402	C4962 1UF 10% 6.3V CERM 402	C4939 1UF 10% 6.3V CERM 402	C4937 1UF 10% 6.3V CERM 402	C4930 1UF 10% 6.3V CERM 402	C4928 1UF 10% 6.3V CERM 402	C4989 1UF 10% 6.3V CERM 402	C4967 1UF 10% 6.3V CERM 402
C4996 1UF 10% 6.3V CERM 402	C4970 1UF 10% 6.3V CERM 402	C4966 1UF 10% 6.3V CERM 402	C4963 1UF 10% 6.3V CERM 402	C4940 1UF 10% 6.3V CERM 402	C4938 1UF 10% 6.3V CERM 402	C4931 1UF 10% 6.3V CERM 402	C4929 1UF 10% 6.3V CERM 402	C4901 1UF 10% 6.3V CERM 402	C4978 1UF 10% 6.3V CERM 402
C4997 1UF 10% 6.3V CERM 402	C4982 1UF 10% 6.3V CERM 402	C4976 1UF 10% 6.3V CERM 402	C4972 1UF 10% 6.3V CERM 402	C4952 1UF 10% 6.3V CERM 402	C4950 1UF 10% 6.3V CERM 402	C4943 1UF 10% 6.3V CERM 402	C4941 1UF 10% 6.3V CERM 402	C4906 1UF 10% 6.3V CERM 402	C4904 1UF 10% 6.3V CERM 402
C4998 1UF 10% 6.3V CERM 402	C4981 1UF 10% 6.3V CERM 402	C4977 1UF 10% 6.3V CERM 402	C4973 1UF 10% 6.3V CERM 402	C4953 1UF 10% 6.3V CERM 402	C4951 1UF 10% 6.3V CERM 402	C4944 1UF 10% 6.3V CERM 402	C4942 1UF 10% 6.3V CERM 402	C4907 1UF 10% 6.3V CERM 402	C4905 1UF 10% 6.3V CERM 402
C4999 1UF 10% 6.3V CERM 402	C4984 1UF 10% 6.3V CERM 402	C4979 1UF 10% 6.3V CERM 402	C4974 1UF 10% 6.3V CERM 402	C4957 1UF 10% 6.3V CERM 402	C4954 1UF 10% 6.3V CERM 402	C4948 1UF 10% 6.3V CERM 402	C4946 1UF 10% 6.3V CERM 402	C4910 1UF 10% 6.3V CERM 402	C4908 1UF 10% 6.3V CERM 402
C4902 1UF 10% 6.3V CERM 402	C4983 1UF 10% 6.3V CERM 402	C4980 1UF 10% 6.3V CERM 402	C4975 1UF 10% 6.3V CERM 402	C4958 1UF 10% 6.3V CERM 402	C4955 1UF 10% 6.3V CERM 402	C4949 1UF 10% 6.3V CERM 402	C4947 1UF 10% 6.3V CERM 402	C4911 1UF 10% 6.3V CERM 402	C4909 1UF 10% 6.3V CERM 402
C4903 1UF 10% 6.3V CERM 402	C4992 1UF 10% 6.3V CERM 402	C4991 1UF 10% 6.3V CERM 402	C4990 1UF 10% 6.3V CERM 402	C4988 1UF 10% 6.3V CERM 402	C4987 1UF 10% 6.3V CERM 402	C4986 1UF 10% 6.3V CERM 402	C4985 1UF 10% 6.3V CERM 402	C4914 1UF 10% 6.3V CERM 402	C4913 1UF 10% 6.3V CERM 402

PROC DECOUPLING

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 49 OF 154	

VCORE VOLTAGE CONTROLLER (VC)

M23/M33: PP12V_CPU IS AN ALL RAIL

=PP12V_CPU
R5029 10 5% 1/16W MF-LF 402
VC_VCC
C5019 1UF 20% 16V CERM 1206
SYS_POWERUP_L
R5000 1.5K 5% 1/16W MF-LF 402
VRM_EN
Q5012 2N7002 SOT23-LF
C5001 1UF 10% 6.3V CERM 402
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
CPU_VID_R<3>
CPU_VID_R<4>
CPU_VID_R<5>
VC_AGND
VC_BGOUT
VC_OSCREF
U5000 SC2642 TSSOP
VCC
BGOUT
OSCREF
VID0
VID1
VID2
VID3
VID4
VID5
DACSTEP
FB
GSENSE
OS1
OS2
AGND
OUTSEN
OUT1
OUT2
PGOOD
EROUT
VC_OUTSEN
VC_OUT1
VC_OUT2
VC_PGOOD
PGOOD IS OC
R5030 0 5% 1/16W MF-LF 402
SYS_SLEWING_L
NOSTUFF R5003 2.7M 5% 1/10W MF-LF 603
VC_ERROUT
VC_VCC
VC_DACSTEP
R5001 20K 5% 1/16W MF-LF 402
NOSTUFF R5002 0 5% 1/16W MF-LF 402
VC_ERROUT_RC
C5002 470PF 10% 50V CERM 402
C5000 0.1UF 20% 10V CERM 402
R5028 221K 1% 1/16W MF-LF 402
VC_OS1
VC_OS2
OMIT XW5000 SM
VC_AUX1
VC_AUX2
R5013 20.5K 1% 1/16W MF-LF 402
R5016 20.5K 1% 1/16W MF-LF 402
NOSTUFF C5004 0.0082UF 10% 25V X7R 402
NOSTUFF R5014 20.5K 1% 1/16W MF-LF 402
NOSTUFF C5005 0.0082UF 10% 25V X7R 402
NOSTUFF R5015 20.5K 1% 1/16W MF-LF 402
VCORE_SENSE_GND
DIFFERENTIAL PAIR FOR REMOTE SENSE
VCORE_SENSE_VOUT
VC_OUTSEN
R5005 4.99K 1% 1/16W MF-LF 402
VC_OS_HUB
R5004 261 1% 1/16W MF-LF 402
C5008 0.068UF 10% 10V CERM 402
R5026 301 1% 1/16W MF-LF 402
AVP ADJUSTMENT
NOSTUFF R5024 330 5% 1/16W MF-LF 402
NOSTUFF R5025 1K 5% 1/16W MF-LF 402
VC_OS_HUB_RC
PCB:PLACE R5025 CLOSE TO INDUCTOR OUTPUT LEAD.
NOSTUFF C5009 0.015UF 10% 16V X7R 402
R5027 1.5K 1% 1/16W MF-LF 402
VC_OUTSEN_R
OMIT XW5002 SM
=PPVCORE_CPU
PCB:CONNECT BETWEEN THE INDUCTOR & BULK CAPS.

VC PROCESSOR VOLTAGE SENSING

CHOICE OF:
1) VCORE PLANE SENSING
2) KELVIN POINT SENSING

PPVCORE_CPU
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
UNDER PROCESSOR
R5035 0 5% 1/16W MF-LF 402
R5036 0 5% 1/16W MF-LF 402
VCORE_SENSE_VOUT
VCORE_SENSE_GND
NOSTUFF R5041 0 5% 1/16W MF-LF 402
NOSTUFF R5042 0 5% 1/16W MF-LF 402
CPU SENSE SIDE
KPVDD2
KPGND2

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD1_DRN	0.25 MM	0.25 MM	316
GD1_BST	0.25 MM	0.25 MM	317
GD1_VREG	0.25 MM	0.25 MM	318
GD1_VPN	0.25 MM	0.25 MM	319
GD1_TG	0.25 MM	0.25 MM	340
GD1_BG	0.25 MM	0.25 MM	341
GD1_FET_RC	0.25 MM	0.25 MM	342
GD1_PN	0.60 MM	0.25 MM	343
GD1_BST_R	0.25 MM	0.25 MM	353

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD2_DRN	0.25 MM	0.25 MM	344
GD2_BST	0.25 MM	0.25 MM	345
GD2_VREG	0.25 MM	0.25 MM	346
GD2_VPN	0.25 MM	0.25 MM	347
GD2_TG	0.25 MM	0.25 MM	348
GD2_BG	0.25 MM	0.25 MM	349
GD2_FET_RC	0.25 MM	0.25 MM	350
GD2_PN	0.60 MM	0.25 MM	351
GD2_BST_R	0.25 MM	0.25 MM	352

VCORE SUPPLY PHASE 1 (GD1)

PP12V_CPU_R_L
C5010 1UF 20% 16V CERM 1206
GD1_BST_R
GD1_DRN
U5010 SC1211 SOIC THMPAD
VIN
CO
DRN
BST
BG
VREG
TG
VPN
VC_OUT1
C5029 1UF 20% 16V CERM 1206
R5007 4.7 5% 1/10W MF-LF 603
GD1_BST
D5010 BAS16 SOT23
GD1_VREG
C5013 1UF 20% 16V CERM 1206
GD1_TG
CRITICAL Q5010 NTD60N02R CASE369
R5050 10K 5% 1/16W MF-LF 402
R5010 1 5% 1/16W MF-LF 402
GD1_PN
CRITICAL L5010 0.6UH-24A TH2
=PPVCORE_CPU
PPVCORE_CPU
MAKE_BASE=TRUE
C5011 680UF 20% 16V ELEC TH-MCZ
C5035 330UF 20% 16V ELEC SM-3
CRITICAL C5012 10UF 10% 16V CERM 1210
CRITICAL C5018 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5017 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5032 1800UF 20% 6.3V ELEC TH-KZJ-LF
CRITICAL C5037 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5038 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5039 1800UF 20% 6.3V ELEC TH-KZJ-LF
R5012 200 5% 1/16W MF-LF 402
VC_AUX1
C5014 470PF 10% 50V CERM 402
GD1_BG1
CRITICAL Q5011 NTD70N03R CASE369
CRITICAL Q5013 NTD70N03R CASE369
R5011 1 5% 1/8W FF 1206
GD1_FET_RC
C5015 0.0022UF 10% 50V CERM 402
C5016 4700PF 10% 50V CERM 1206

VCORE SUPPLY PHASE 2 (GD2)

PP12V_CPU_R_L
C5020 1UF 20% 16V CERM 1206
GD2_BST_R
GD2_DRN
U5020 SC1211 SOIC THMPAD
VIN
CO
DRN
BST
BG
VREG
TG
VPN
VC_OUT2
C5030 1UF 20% 16V CERM 1206
R5006 4.7 5% 1/10W MF-LF 603
GD2_BST
D5020 BAS16 SOT23
GD2_VREG
C5023 1UF 20% 16V CERM 1206
GD2_TG
CRITICAL Q5020 NTD60N02R CASE369
R5051 10K 5% 1/16W MF-LF 402
R5020 1 5% 1/16W MF-LF 402
GD2_PN
L5020 0.6UH-24A TH2
PPVCORE_CPU
C5028 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5033 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5040 1800UF 20% 6.3V ELEC TH-KZJ-LF
CRITICAL C5041 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5042 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5043 1800UF 20% 6.3V ELEC TH-KZJ-LF
R5022 200 5% 1/16W MF-LF 402
VC_AUX2
C5024 470PF 10% 50V CERM 402
GD2_BG1
CRITICAL Q5021 NTD70N03R CASE369
CRITICAL Q5023 NTD70N03R CASE369
R5021 1 5% 1/8W FF 1206
GD2_FET_RC
C5025 0.0022UF 10% 50V CERM 402
C5026 4700PF 10% 50V CERM 1206
C5021 1000UF 20% 16V ELEC TH-KZJ-LF
C5034 1000UF 20% 16V ELEC TH-KZJ-LF
C5022 10UF 10% 16V CERM 1210

PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
VC_OSCREF	0.25 MM	0.20 MM	320
CPU_VID_R<0..5>	0.25 MM	0.20 MM	330
VC_DACSTEP	0.25 MM	0.20 MM	321
VC_AGND	0.50 MM	0.20 MM	322
VC_BGOUT	0.25 MM	0.20 MM	323
VC_OS1	0.25 MM	0.20 MM	324
VC_OS2	0.25 MM	0.20 MM	325
VC_VCC	0.25 MM	0.25 MM	331
VC_OS_HUB	0.25 MM	0.20 MM	326
VC_OUTSEN	0.25 MM	0.20 MM	327
VC_OUTSEN_R	0.25 MM	0.20 MM	328
VCORE_SENSE_GND	0.25 MM	0.20 MM	329
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	332
VC_AUX1	0.25 MM	0.25 MM	333
VC_AUX2	0.25 MM	0.25 MM	334
VC_OUT1	0.45 MM	0.25 MM	335
VC_OUT2	0.45 MM	0.20 MM	336
VC_ERROUT	0.25 MM	0.20 MM	355
VC_ERROUT_RC	0.25 MM	0.20 MM	356
VC_OS_HUB_RC	0.25 MM	0.20 MM	354
EI_REFCLK_AVDD	0.50 MM	0.08 MM	360

CPU VCORE VREG

SYNC_MASTER=M23-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 50 OF 154	

56 55 50 49 48 42 =PPVCORE_CPU

CRITICAL

C5200 10UF 10% 6.3V X5R 805	C5212 10UF 10% 6.3V X5R 805	C5223 10UF 10% 6.3V X5R 805	C5234 10UF 10% 6.3V X5R 805	C5245 10UF 10% 6.3V X5R 805	C5201 10UF 10% 6.3V X5R 805	C5289 10UF 10% 6.3V X5R 805	C5278 10UF 10% 6.3V X5R 805	C5267 10UF 10% 6.3V X5R 805	C5256 10UF 10% 6.3V X5R 805
C5213 10UF 10% 6.3V X5R 805	C5211 10UF 10% 6.3V X5R 805	C5210 10UF 10% 6.3V X5R 805	C5209 10UF 10% 6.3V X5R 805	C5208 10UF 10% 6.3V X5R 805	C5207 10UF 10% 6.3V X5R 805	C5206 10UF 10% 6.3V X5R 805	C5205 10UF 10% 6.3V X5R 805	C5204 10UF 10% 6.3V X5R 805	C5203 10UF 10% 6.3V X5R 805
C5224 10UF 10% 6.3V X5R 805	C5222 10UF 10% 6.3V X5R 805	C5221 10UF 10% 6.3V X5R 805	C5220 10UF 10% 6.3V X5R 805	C5219 10UF 10% 6.3V X5R 805	C5218 10UF 10% 6.3V X5R 805	C5217 10UF 10% 6.3V X5R 805	C5216 10UF 10% 6.3V X5R 805	C5215 10UF 10% 6.3V X5R 805	C5214 10UF 10% 6.3V X5R 805
C5235 10UF 10% 6.3V X5R 805	C5233 10UF 10% 6.3V X5R 805	C5232 10UF 10% 6.3V X5R 805	C5231 10UF 10% 6.3V X5R 805	C5230 10UF 10% 6.3V X5R 805	C5229 10UF 10% 6.3V X5R 805	C5228 10UF 10% 6.3V X5R 805	C5227 10UF 10% 6.3V X5R 805	C5226 10UF 10% 6.3V X5R 805	C5225 10UF 10% 6.3V X5R 805
C5246 10UF 10% 6.3V X5R 805	C5244 10UF 10% 6.3V X5R 805	C5243 10UF 10% 6.3V X5R 805	C5242 10UF 10% 6.3V X5R 805	C5241 10UF 10% 6.3V X5R 805	C5240 10UF 10% 6.3V X5R 805	C5239 10UF 10% 6.3V X5R 805	C5238 10UF 10% 6.3V X5R 805	C5237 10UF 10% 6.3V X5R 805	C5236 10UF 10% 6.3V X5R 805
C5257 10UF 10% 6.3V X5R 805	C5255 10UF 10% 6.3V X5R 805	C5254 10UF 10% 6.3V X5R 805	C5253 10UF 10% 6.3V X5R 805	C5252 10UF 10% 6.3V X5R 805	C5251 10UF 10% 6.3V X5R 805	C5250 10UF 10% 6.3V X5R 805	C5249 10UF 10% 6.3V X5R 805	C5248 10UF 10% 6.3V X5R 805	C5247 10UF 10% 6.3V X5R 805
C5268 10UF 10% 6.3V X5R 805	C5266 10UF 10% 6.3V X5R 805	C5265 10UF 10% 6.3V X5R 805	C5264 10UF 10% 6.3V X5R 805	C5263 10UF 10% 6.3V X5R 805	C5262 10UF 10% 6.3V X5R 805	C5261 10UF 10% 6.3V X5R 805	C5260 10UF 10% 6.3V X5R 805	C5259 10UF 10% 6.3V X5R 805	C5258 10UF 10% 6.3V X5R 805
C5279 10UF 10% 6.3V X5R 805	C5277 10UF 10% 6.3V X5R 805	C5276 10UF 10% 6.3V X5R 805	C5275 10UF 10% 6.3V X5R 805	C5274 10UF 10% 6.3V X5R 805	C5273 10UF 10% 6.3V X5R 805	C5272 10UF 10% 6.3V X5R 805	C5271 10UF 10% 6.3V X5R 805	C5270 10UF 10% 6.3V X5R 805	C5269 10UF 10% 6.3V X5R 805
C5290 10UF 10% 6.3V X5R 805	C5288 10UF 10% 6.3V X5R 805	C5287 10UF 10% 6.3V X5R 805	C5286 10UF 10% 6.3V X5R 805	C5285 10UF 10% 6.3V X5R 805	C5284 10UF 10% 6.3V X5R 805	C5283 10UF 10% 6.3V X5R 805	C5282 10UF 10% 6.3V X5R 805	C5281 10UF 10% 6.3V X5R 805	C5280 10UF 10% 6.3V X5R 805
C5202 10UF 10% 6.3V X5R 805	C5299 10UF 10% 6.3V X5R 805	C5298 10UF 10% 6.3V X5R 805	C5297 10UF 10% 6.3V X5R 805	C5296 10UF 10% 6.3V X5R 805	C5295 10UF 10% 6.3V X5R 805	C5294 10UF 10% 6.3V X5R 805	C5293 10UF 10% 6.3V X5R 805	C5292 10UF 10% 6.3V X5R 805	C5291 10UF 10% 6.3V X5R 805

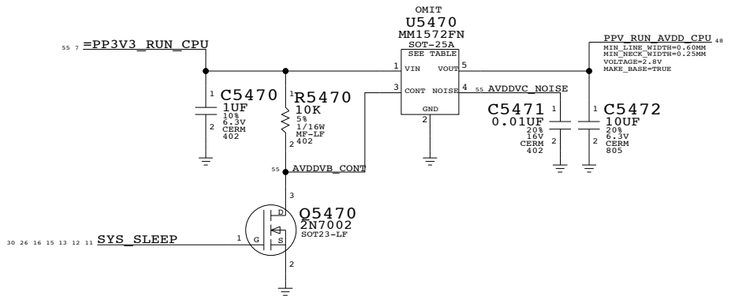
CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 52 OF 154	

PROCESSOR AVDD VREG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0671	1	IIC,MM1572FN,2.5V,150MA,REG,5P SOT-25A	U5470	AVDD_2V5
353S0807	1	IIC,MM1572,2.8V,150MA,REG,5P SOT-25A	U5470	AVDD_2V8

ZH5400 HOLE-VIA
ZH5401 HOLE-VIA
ZH5402 HOLE-VIA
ZH5403 HOLE-VIA
ZH5404 HOLE-VIA
ZH5405 HOLE-VIA
ZH5406 HOLE-VIA
ZH5407 HOLE-VIA
ZH5408 HOLE-VIA
ZH5409 HOLE-VIA
ZH5410 HOLE-VIA
ZH5411 HOLE-VIA
ZH5412 HOLE-VIA
ZH5413 HOLE-VIA
ZH5414 HOLE-VIA
ZH5415 HOLE-VIA
ZH5416 HOLE-VIA
ZH5417 HOLE-VIA
ZH5418 HOLE-VIA
ZH5419 HOLE-VIA
ZH5420 HOLE-VIA
ZH5421 HOLE-VIA
ZH5422 HOLE-VIA
ZH5423 HOLE-VIA
ZH5424 HOLE-VIA
ZH5425 HOLE-VIA
ZH5426 HOLE-VIA
ZH5427 HOLE-VIA
ZH5428 HOLE-VIA
ZH5429 HOLE-VIA
ZH5430 HOLE-VIA
ZH5431 HOLE-VIA
ZH5432 HOLE-VIA
ZH5433 HOLE-VIA
ZH5434 HOLE-VIA
ZH5435 HOLE-VIA
ZH5436 HOLE-VIA
ZH5437 HOLE-VIA
ZH5438 HOLE-VIA
ZH5439 HOLE-VIA
ZH5440 HOLE-VIA
ZH5441 HOLE-VIA
ZH5442 HOLE-VIA
ZH5443 HOLE-VIA
ZH5444 HOLE-VIA
ZH5445 HOLE-VIA
ZH5446 HOLE-VIA
ZH5447 HOLE-VIA
ZH5448 HOLE-VIA
ZH5449 HOLE-VIA
ZH5450 HOLE-VIA
ZH5451 HOLE-VIA
ZH5452 HOLE-VIA
ZH5453 HOLE-VIA
ZH5454 HOLE-VIA
ZH5455 HOLE-VIA
ZH5456 HOLE-VIA
ZH5457 HOLE-VIA
ZH5458 HOLE-VIA
ZH5459 HOLE-VIA
ZH5460 HOLE-VIA
ZH5461 HOLE-VIA
ZH5462 HOLE-VIA
ZH5463 HOLE-VIA
ZH5464 HOLE-VIA
ZH5465 HOLE-VIA
ZH5466 HOLE-VIA
ZH5467 HOLE-VIA
ZH5468 HOLE-VIA
ZH5469 HOLE-VIA
ZH5470 HOLE-VIA
ZH5471 HOLE-VIA

CPU AVDD VREG

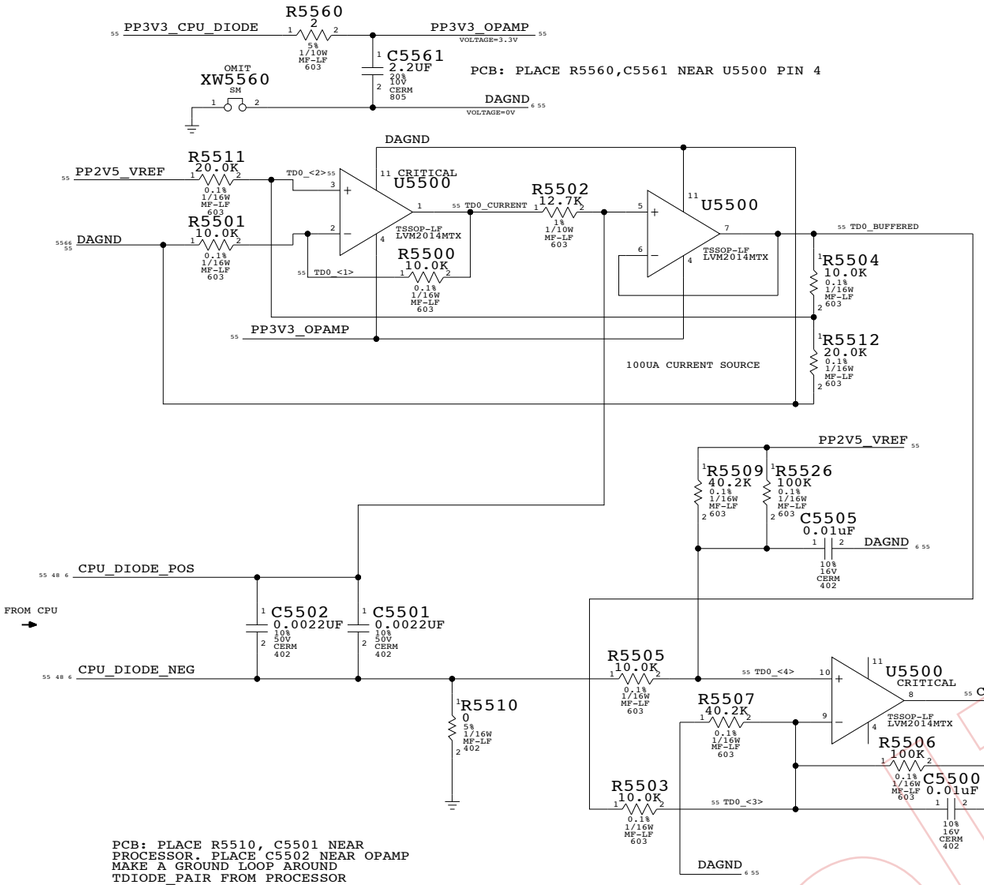
SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

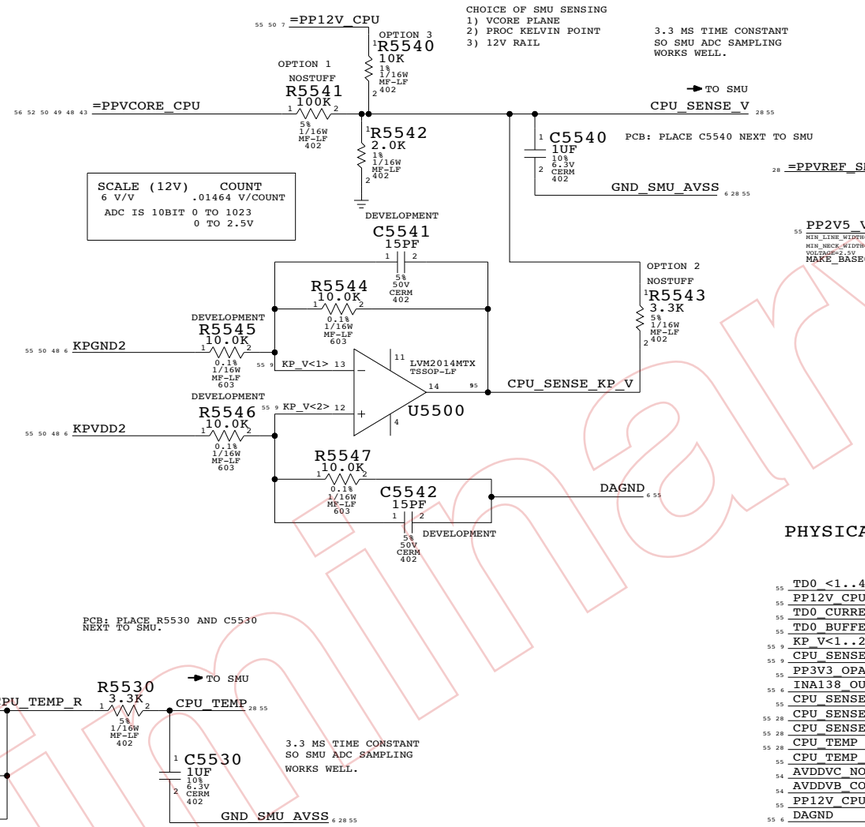
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 54 OF 154

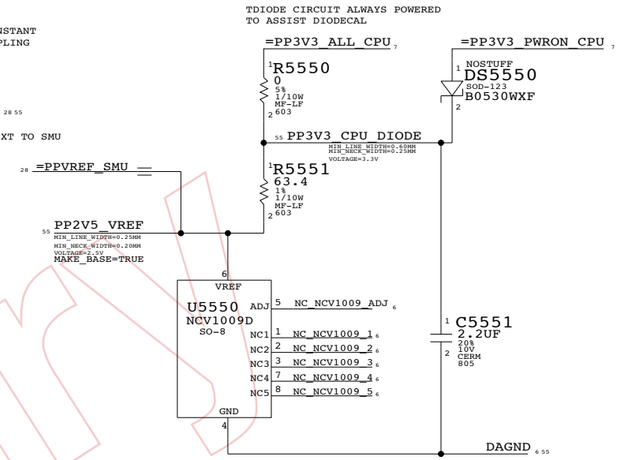
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



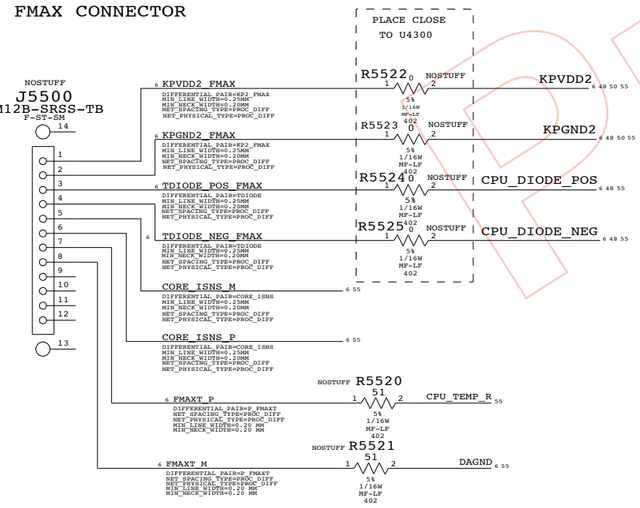
2.5V PRECISION VOLTAGE REFERENCE SOURCE



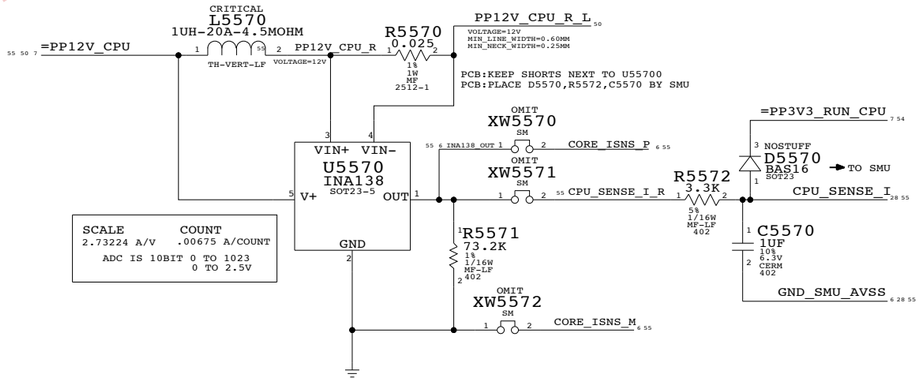
PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
TD0_<1..4>	0.25 MM	0.25 MM	A325
PP12V_CPU_R	0.60 MM	0.25 MM	A376
TD0_CURRENT	0.25 MM	0.25 MM	A323
TD0_BUFFERED	0.25 MM	0.25 MM	A321
KP_V<1..2>	0.25 MM	0.25 MM	A355
CPU_SENSE_KP_V	0.25 MM	0.25 MM	A356
PP3V3_OPAMP	0.60 MM	0.25 MM	A375
INA138_OUT	0.25 MM	0.25 MM	A357
CPU_SENSE_I_R	0.25 MM	0.25 MM	A360
CPU_SENSE_I	0.25 MM	0.25 MM	A359
CPU_SENSE_V	0.25 MM	0.25 MM	A361
CPU_TEMP	0.25 MM	0.20 MM	A362
CPU_TEMP_R	0.25 MM	0.20 MM	A370
AVDDVC_NOISE	0.25 MM	0.20 MM	A380
AVDDVB_CONT	0.25 MM	0.20 MM	A381
PP12V_CPU_R	0.60 MM	0.25 MM	A382
DAGND	0.60 MM	0.25 MM	A385

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T,V,I SENSORS

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 55 OF 154	

CONNECT PULSAR CLKS TO CPU/NB

EI_CPU_SYSCLK_P	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_P	26
EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N	26
EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC	26
EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US	26
EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC	26 42

CONNECT KODIAK EI A TO/FROM CPU

EI_NB_TO_CPU_CLK_P		EI_NB_TO_CPU_A_CLK_P	42
EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N	42
EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43>	42
EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1>	42
EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1>	42
	MAKE_BASE=TRUE		
EI_CPU_TO_NB_CLK_P		EI_CPU_A_TO_NB_CLK_P	42
EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N	42
EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43>	42
EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1>	42
EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1>	42
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK QREQ A0

CPU_TO_NB_QREQ_L		CPU_A0_TO_NB_QREQ_L	42
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

CPU_QACK_L		CPU_A0_QACK_L	42
NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L	42
NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L	44
NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L	44
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

CPU_INT_L		CPU_A0_INT_R_L	24 56
NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L	42
NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L	44
NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L	44
	MAKE_BASE=TRUE		

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

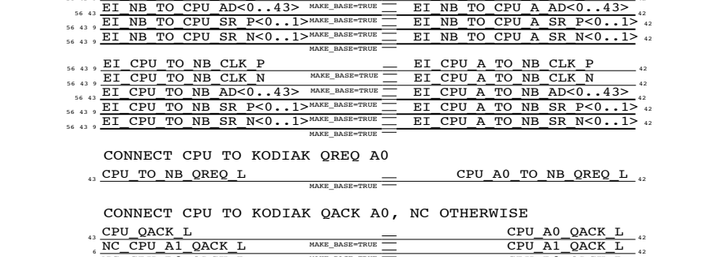
CPU_SRESET_L_R		SB_CPU_A0_SRESET_L	24 56
NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L	24 56
NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L	24 56
NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L	24 56
	MAKE_BASE=TRUE		

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

TP_NB_B_TRIGGER_OUT		NB_B_TRIGGER_OUT	44
TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT	42
TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT	43
TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN	43 47
TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT	43
NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO	43
NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE	43
TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION	43
NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN	43
	MAKE_BASE=TRUE		

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	130
EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		136
EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		137
EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		139
EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	140
EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	141
EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	143
EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	142
EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		4135
EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		4136

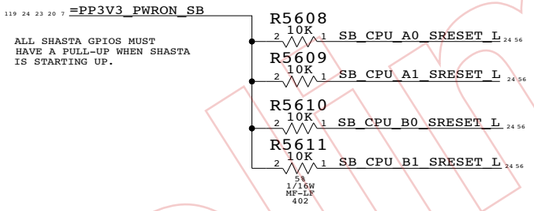
NC KODIAK EI B OUTPUT PORT

NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P	44
NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N	44
NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43>	44
NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1>	44
NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1>	44
	MAKE_BASE=TRUE		

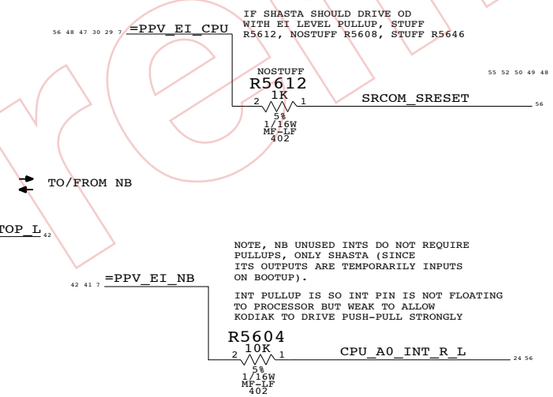
NC KODIAK EI B INPUT PORT

NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P	44
NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N	44
NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43>	44
NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1>	44
NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1>	44
	MAKE_BASE=TRUE		

PULLUPS FOR SRESET'S FROM SHASTA

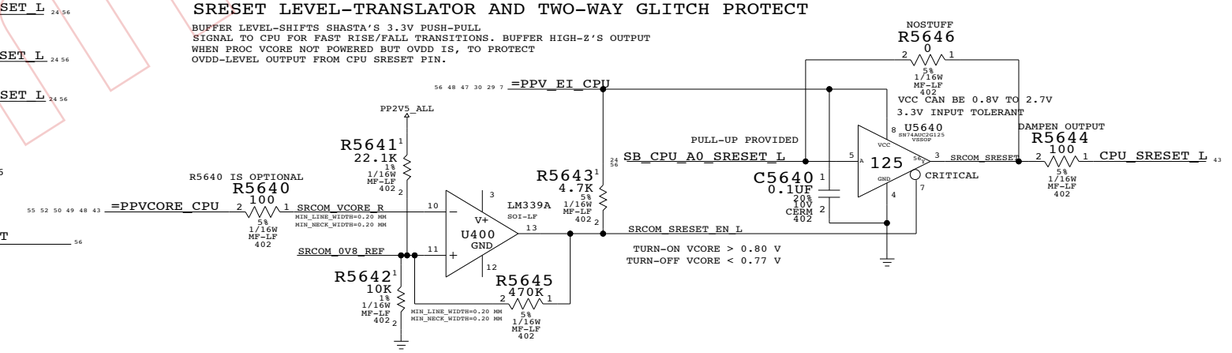


ALL SHASTA GPIOS MUST HAVE A PULL-UP WHEN SHASTA IS STARTING UP.



SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.

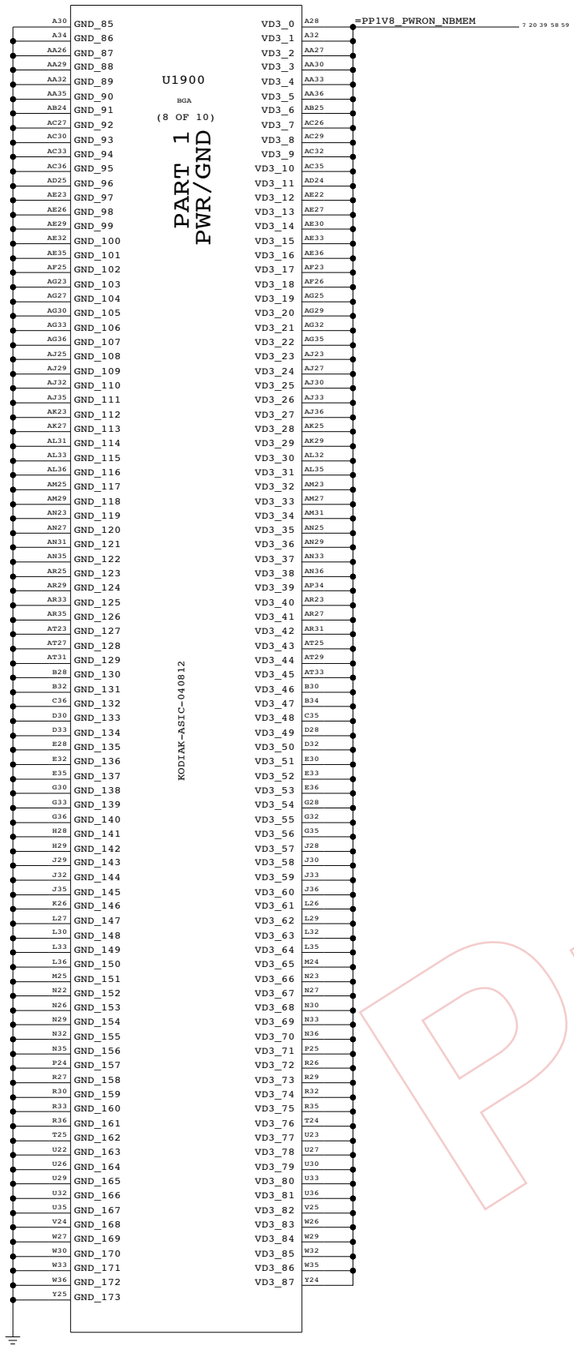


CPU ALIASES & MISC

SYNC_MASTER=FINO-MS SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 56 OF 154	



59 58 39 20 7 =PP1V8_PWRON_NBMEM

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

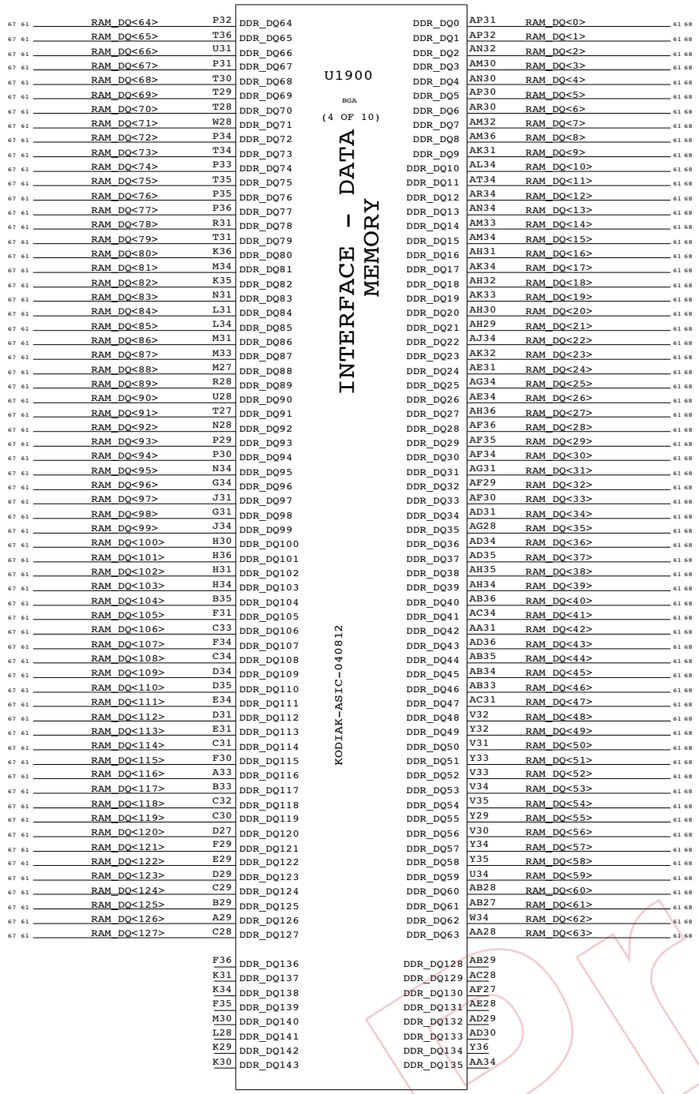
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

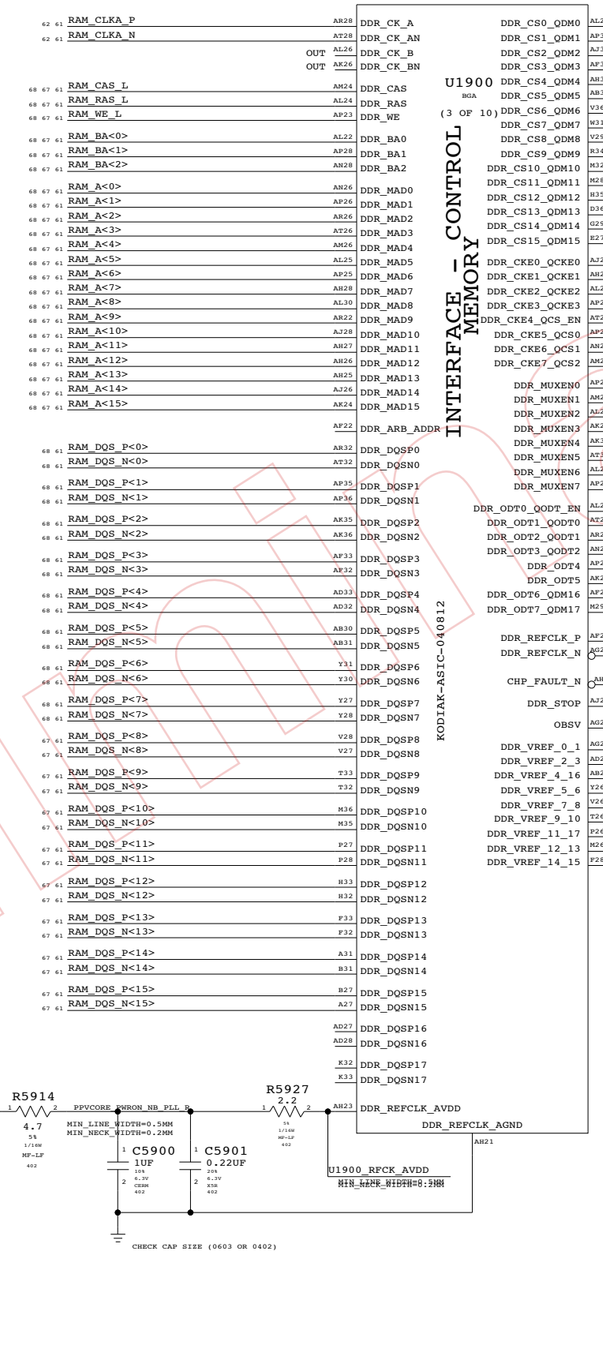
SCALE: NONE SHT 58 OF 154

LAST_MODIFIED=Thu May 19 14:09:19 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

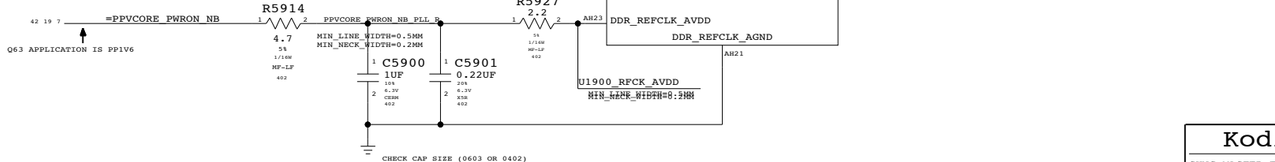


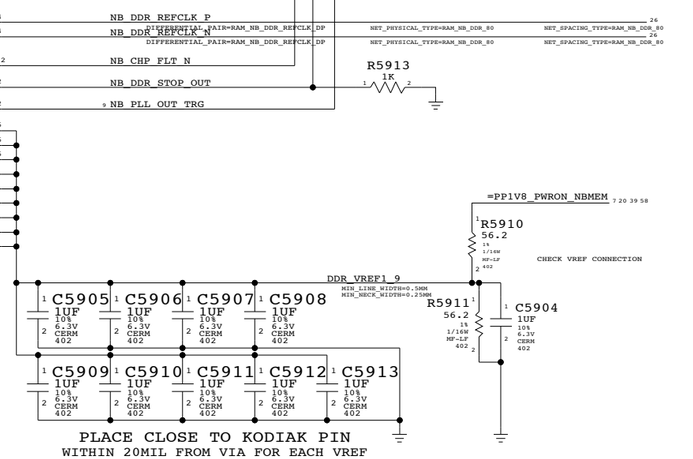
Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	–	*unused*	0:63
B2	8	0	4	J6700 rank 1	64:127
B3	9	1	–	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	–	*unused*	0:63
D6	10	2	5	*unused*	64:127
D7	11	3	–	*unused*	64:127
E8	4	4	2	*unused*	0:63
E9	5	5	–	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	–	*unused*	64:127
G12	7	7	3	*unused*	0:63
G13	7	7	–	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	–	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	–	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	–	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	–	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	–	*unused*	64:127





KODIAK MEMORY INTERFACE

Kodiak Memory Dq/Ctl

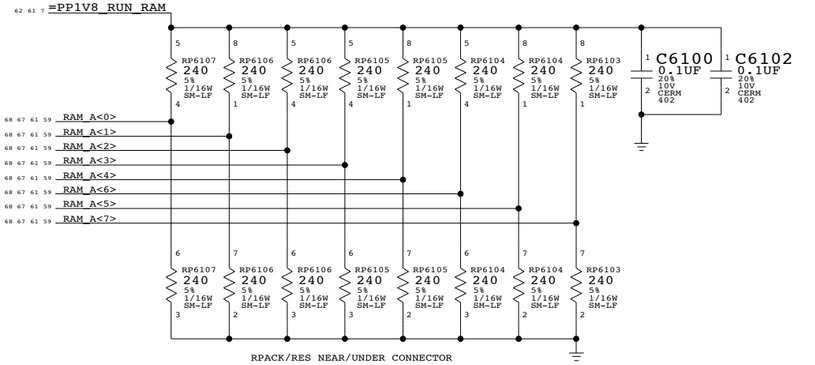
SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

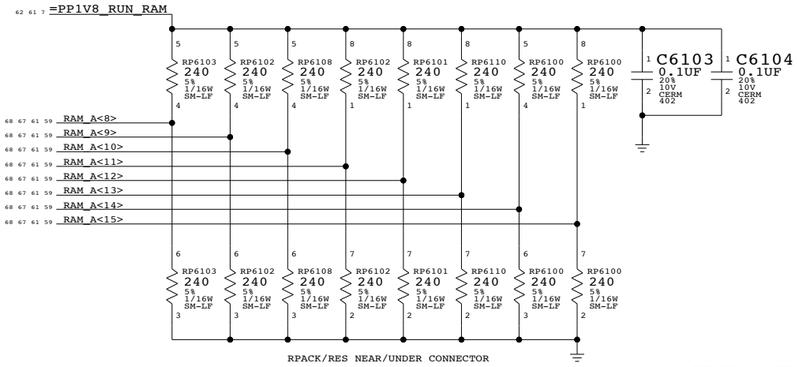
APPLE COMPUTER INC.

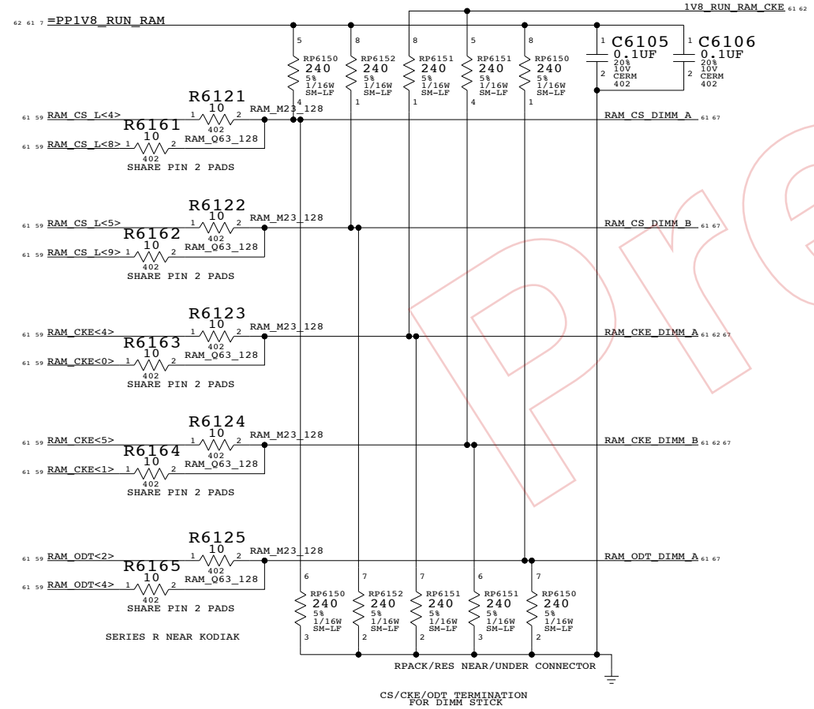
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

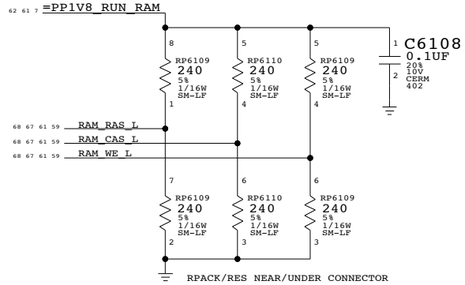
SCALE	SHT	OF
NONE	59	154

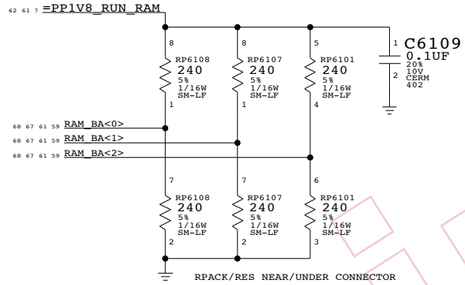
ALL R PACKS ARE 1/16W 5%

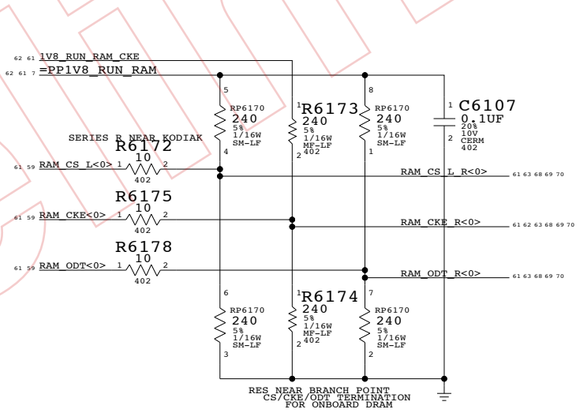












RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	7243
RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	7487
RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	7242
RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT	7245
RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT	7244
RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	7238
RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	7241
RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	7575
RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	7234
RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	7236
RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT	7235
RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT	7237
RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	7230
RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT	7592
RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	7232
RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT	7574
RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT	7576
RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT	7577
RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT	7593
RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT	7594

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	7206
RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	7207
RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	7230
RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	7231
RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	7232
RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	7233
RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	7234
RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	7235
RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	7216
RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	7217
RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	7218
RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	7219
RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	7220
RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	7221
RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	7222
RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	7223
RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	7224
RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	7225
RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	7226
RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	7227
RAM_DQ<7..0>	RAM_DQS0_EC	RAM_CAD	RAM_CAD		7248
RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	7470
RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	7471
RAM_DQ<15..8>	RAM_DQS1_EC	RAM_CAD	RAM_CAD		7252
RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	7251
RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	7472
RAM_DQ<23..16>	RAM_DQS2_EC	RAM_CAD	RAM_CAD		7254
RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	7253
RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	7473
RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD		7256
RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	7255
RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	7474
RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD		7258
RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	7257
RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	7475
RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD		7260
RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	7259
RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	7476
RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD		7262
RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	7261
RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	7477
RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD		7264
RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	7263
RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	7478
RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD		7229
RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	7245
RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	7479
RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD		7268
RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	7266
RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	7480
RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD		7269
RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	7270
RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	7481
RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD		7271
RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	7272
RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	7482
RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD		7273
RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	7274
RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	7483
RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD		7277
RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	7276
RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	7484
RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD		7278
RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	7279
RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	7485
RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD		7280
RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	7281
RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	7486
RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		7244
RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS		7355
RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS		7486
RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7572
RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7208
RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7256
RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		7573
RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7257
RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7258
RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7259
RAM_A_R<15..0>		RAM_CAD	RAM_CAD		7380
RAM_BA_R<2..0>		RAM_CAD	RAM_CAD		7381
RAM_RAS_L_R		RAM_CAD	RAM_CAD		7383
RAM_CAS_L_R		RAM_CAD	RAM_CAD		7382
RAM_WE_L_R		RAM_CAD	RAM_CAD		7384

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

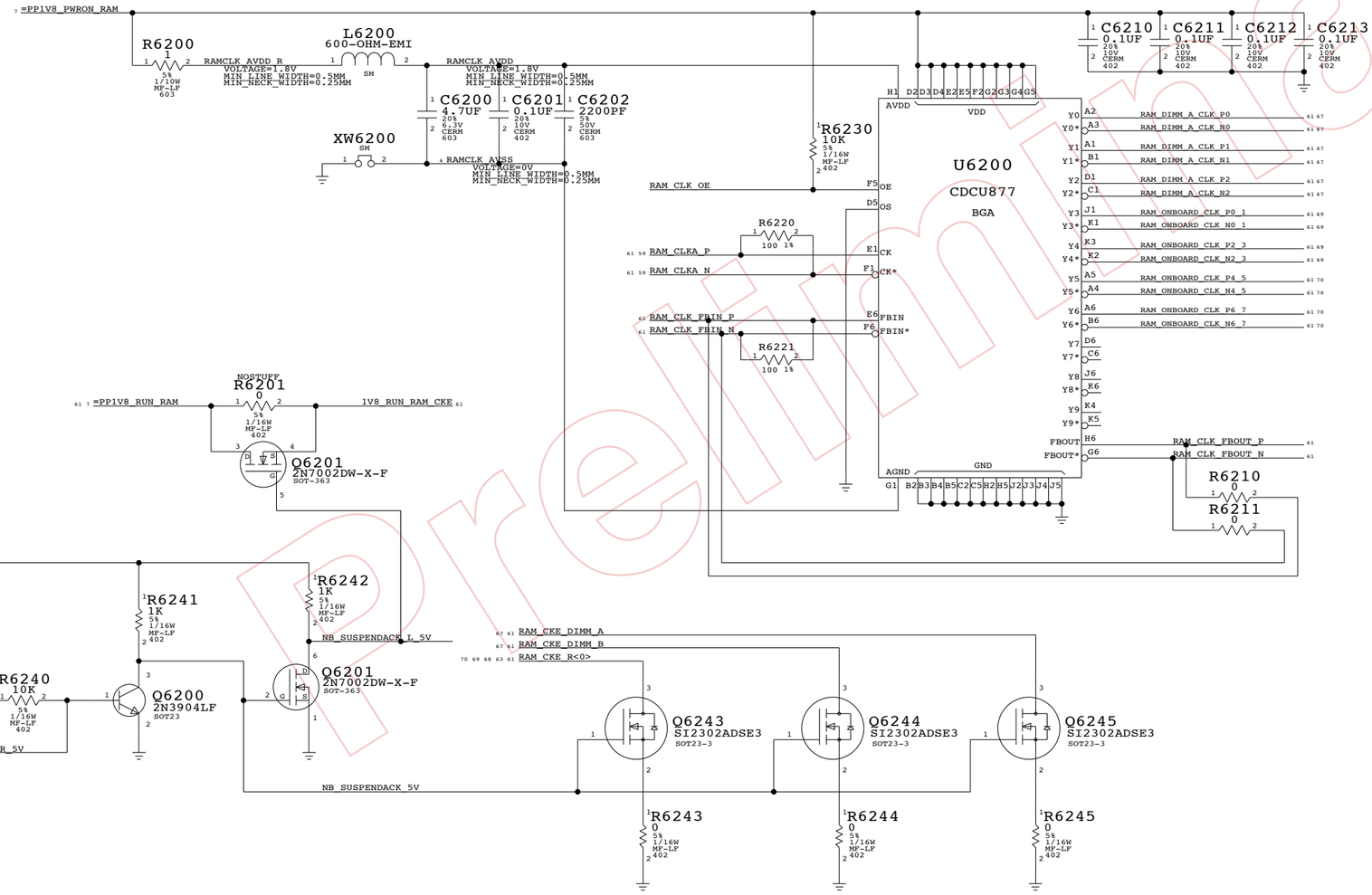
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 61 OF 154	



Main Memory Clock Buffer

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

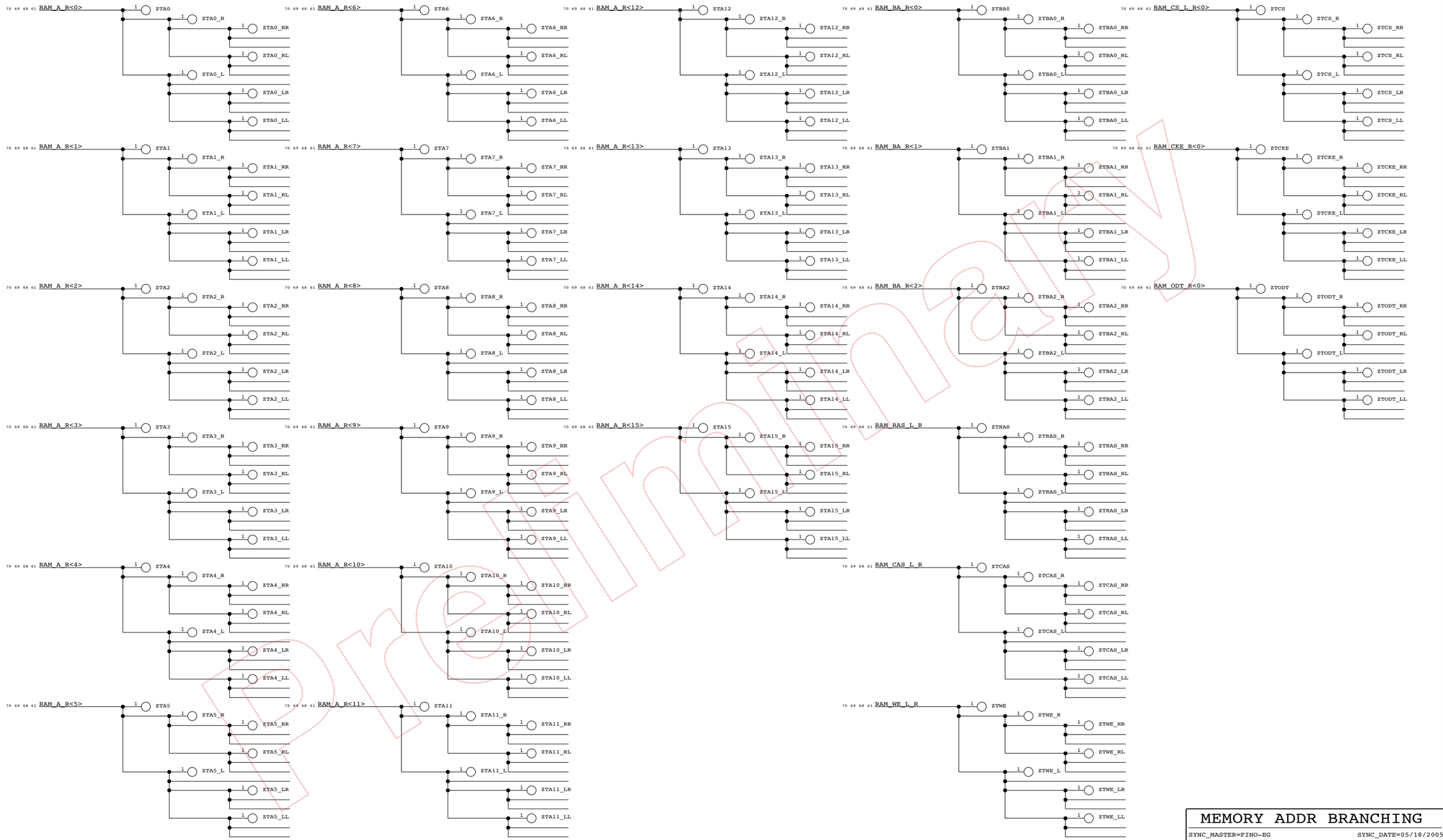
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 62 OF 154	



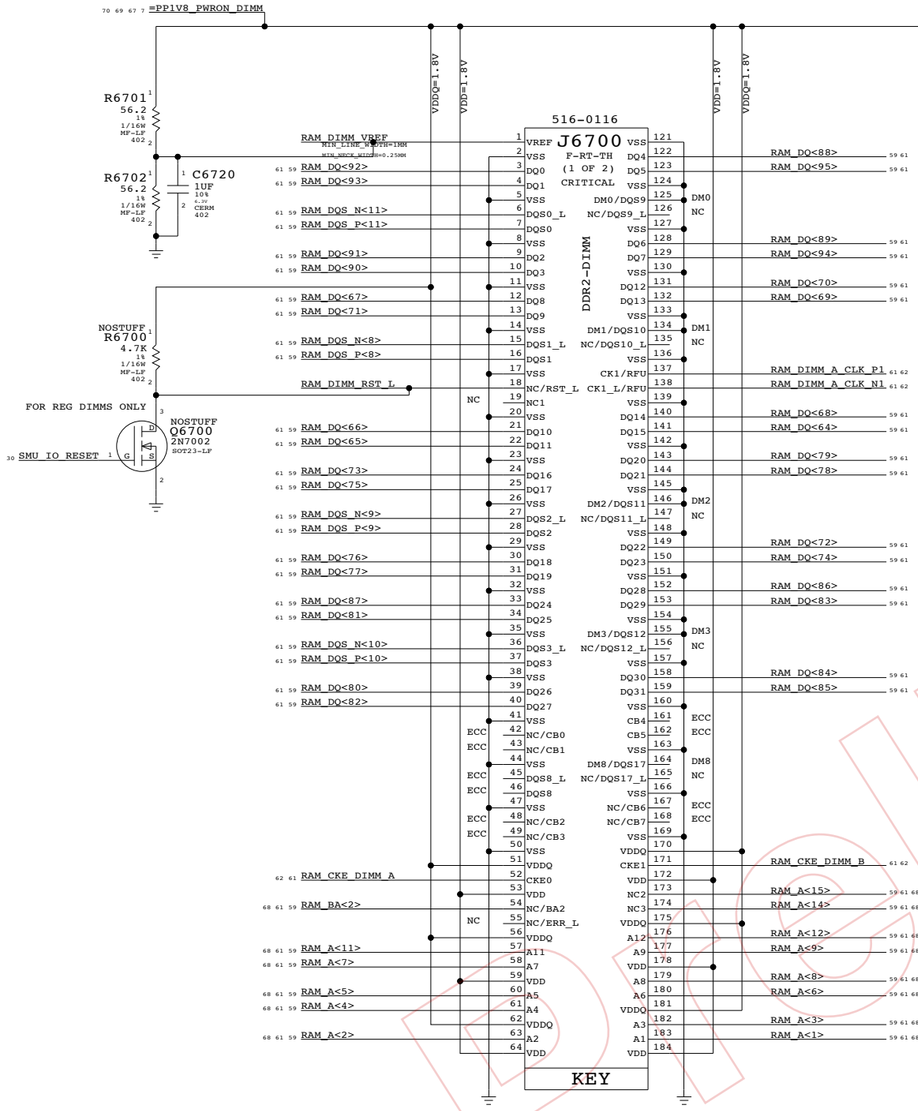
MEMORY ADDR BRANCHING

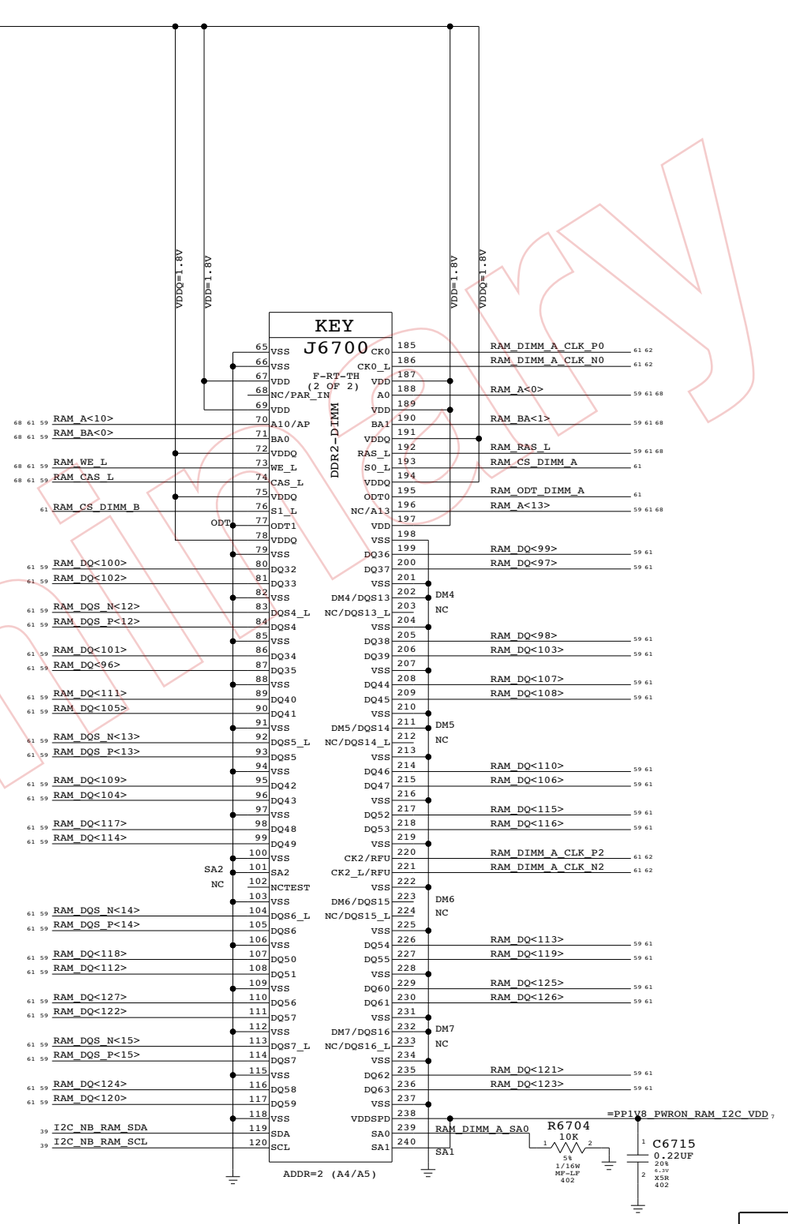
SYNC_MASTER=FINO-EG SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

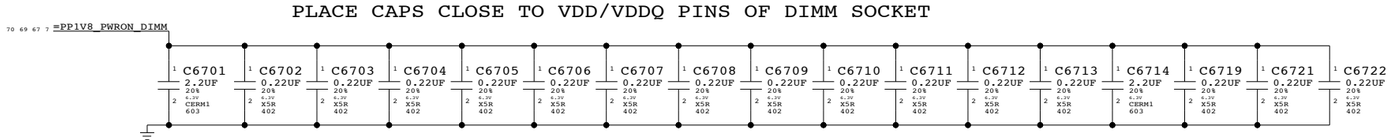
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE NONE SHT 63 OF 154





PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



Memory Dimm A

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 67 OF 154	

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

61 59	RAM_DQ<0>	22	4	5	RP6800	RAM_DQ_R<0>	61 69
61 59	RAM_DQ<1>	22	3	6	RP6800	RAM_DQ_R<1>	61 69
61 59	RAM_DQ<2>	22	1	8	RP6801	RAM_DQ_R<2>	61 69
61 59	RAM_DQ<3>	22	3	6	RP6801	RAM_DQ_R<3>	61 69
61 59	RAM_DQ<4>	22	4	5	RP6801	RAM_DQ_R<4>	61 69
61 59	RAM_DQ<5>	22	2	7	RP6800	RAM_DQ_R<5>	61 69
61 59	RAM_DQ<6>	22	2	7	RP6801	RAM_DQ_R<6>	61 69
61 59	RAM_DQ<7>	22	1	8	RP6800	RAM_DQ_R<7>	61 69
61 59	RAM_DQ<8>	22	3	6	RP6802	RAM_DQ_R<8>	61 69
61 59	RAM_DQ<9>	22	4	5	RP6803	RAM_DQ_R<9>	61 69
61 59	RAM_DQ<10>	22	1	8	RP6803	RAM_DQ_R<10>	61 69
61 59	RAM_DQ<11>	22	4	5	RP6802	RAM_DQ_R<11>	61 69
61 59	RAM_DQ<12>	22	3	6	RP6803	RAM_DQ_R<12>	61 69
61 59	RAM_DQ<13>	22	2	7	RP6802	RAM_DQ_R<13>	61 69
61 59	RAM_DQ<14>	22	2	7	RP6803	RAM_DQ_R<14>	61 69
61 59	RAM_DQ<15>	22	1	8	RP6802	RAM_DQ_R<15>	61 69
61 59	RAM_DQ<16>	22	3	6	RP6805	RAM_DQ_R<16>	61 69
61 59	RAM_DQ<17>	22	4	5	RP6805	RAM_DQ_R<17>	61 69
61 59	RAM_DQ<18>	22	1	8	RP6804	RAM_DQ_R<18>	61 69
61 59	RAM_DQ<19>	22	2	7	RP6805	RAM_DQ_R<19>	61 69
61 59	RAM_DQ<20>	22	2	7	RP6804	RAM_DQ_R<20>	61 69
61 59	RAM_DQ<21>	22	4	5	RP6804	RAM_DQ_R<21>	61 69
61 59	RAM_DQ<22>	22	3	6	RP6804	RAM_DQ_R<22>	61 69
61 59	RAM_DQ<23>	22	1	8	RP6805	RAM_DQ_R<23>	61 69
61 59	RAM_DQ<24>	22	4	5	RP6807	RAM_DQ_R<24>	61 69
61 59	RAM_DQ<25>	22	2	7	RP6806	RAM_DQ_R<25>	61 69
61 59	RAM_DQ<26>	22	4	5	RP6806	RAM_DQ_R<26>	61 69
61 59	RAM_DQ<27>	22	1	8	RP6807	RAM_DQ_R<27>	61 69
61 59	RAM_DQ<28>	22	3	6	RP6807	RAM_DQ_R<28>	61 69
61 59	RAM_DQ<29>	22	3	6	RP6806	RAM_DQ_R<29>	61 69
61 59	RAM_DQ<30>	22	2	7	RP6807	RAM_DQ_R<30>	61 69
61 59	RAM_DQ<31>	22	1	8	RP6806	RAM_DQ_R<31>	61 69
61 59	RAM_DQ<32>	22	4	5	RP6809	RAM_DQ_R<32>	61 70
61 59	RAM_DQ<33>	22	2	7	RP6808	RAM_DQ_R<33>	61 70
61 59	RAM_DQ<34>	22	3	6	RP6808	RAM_DQ_R<34>	61 70
61 59	RAM_DQ<35>	22	1	8	RP6809	RAM_DQ_R<35>	61 70
61 59	RAM_DQ<36>	22	2	7	RP6809	RAM_DQ_R<36>	61 70
61 59	RAM_DQ<37>	22	1	8	RP6808	RAM_DQ_R<37>	61 70
61 59	RAM_DQ<38>	22	3	6	RP6809	RAM_DQ_R<38>	61 70
61 59	RAM_DQ<39>	22	4	5	RP6808	RAM_DQ_R<39>	61 70
61 59	RAM_DQ<40>	22	4	5	RP6810	RAM_DQ_R<40>	61 70
61 59	RAM_DQ<41>	22	3	6	RP6811	RAM_DQ_R<41>	61 70
61 59	RAM_DQ<42>	22	1	8	RP6811	RAM_DQ_R<42>	61 70
61 59	RAM_DQ<43>	22	2	7	RP6810	RAM_DQ_R<43>	61 70
61 59	RAM_DQ<44>	22	4	5	RP6811	RAM_DQ_R<44>	61 70
61 59	RAM_DQ<45>	22	3	6	RP6810	RAM_DQ_R<45>	61 70
61 59	RAM_DQ<46>	22	2	7	RP6811	RAM_DQ_R<46>	61 70
61 59	RAM_DQ<47>	22	1	8	RP6810	RAM_DQ_R<47>	61 70
61 59	RAM_DQ<48>	22	3	6	RP6812	RAM_DQ_R<48>	61 70
61 59	RAM_DQ<49>	22	4	5	RP6812	RAM_DQ_R<49>	61 70
61 59	RAM_DQ<50>	22	2	7	RP6813	RAM_DQ_R<50>	61 70
61 59	RAM_DQ<51>	22	1	8	RP6813	RAM_DQ_R<51>	61 70
61 59	RAM_DQ<52>	22	3	6	RP6813	RAM_DQ_R<52>	61 70
61 59	RAM_DQ<53>	22	4	5	RP6813	RAM_DQ_R<53>	61 70
61 59	RAM_DQ<54>	22	2	7	RP6812	RAM_DQ_R<54>	61 70
61 59	RAM_DQ<55>	22	1	8	RP6812	RAM_DQ_R<55>	61 70
61 59	RAM_DQ<56>	22	3	6	RP6814	RAM_DQ_R<56>	61 70
61 59	RAM_DQ<57>	22	4	5	RP6815	RAM_DQ_R<57>	61 70
61 59	RAM_DQ<58>	22	2	7	RP6815	RAM_DQ_R<58>	61 70
61 59	RAM_DQ<59>	22	3	6	RP6815	RAM_DQ_R<59>	61 70
61 59	RAM_DQ<60>	22	2	7	RP6814	RAM_DQ_R<60>	61 70
61 59	RAM_DQ<61>	22	1	8	RP6814	RAM_DQ_R<61>	61 70
61 59	RAM_DQ<62>	22	1	8	RP6815	RAM_DQ_R<62>	61 70
61 59	RAM_DQ<63>	22	4	5	RP6814	RAM_DQ_R<63>	61 70

61 59	RAM_DQS_P<0>	22	1	2	R6800	RAM_DQS_P_R<0>	61 69
61 59	RAM_DQS_N<0>	22	1	2	R6810	RAM_DQS_N_R<0>	61 69
61 59	RAM_DQS_P<1>	22	1	2	R6801	RAM_DQS_P_R<1>	61 69
61 59	RAM_DQS_N<1>	22	1	2	R6811	RAM_DQS_N_R<1>	61 69
61 59	RAM_DQS_P<2>	22	1	2	R6802	RAM_DQS_P_R<2>	61 69
61 59	RAM_DQS_N<2>	22	1	2	R6812	RAM_DQS_N_R<2>	61 69
61 59	RAM_DQS_P<3>	22	1	2	R6803	RAM_DQS_P_R<3>	61 69
61 59	RAM_DQS_N<3>	22	1	2	R6813	RAM_DQS_N_R<3>	61 69
61 59	RAM_DQS_P<4>	22	1	2	R6804	RAM_DQS_P_R<4>	61 70
61 59	RAM_DQS_N<4>	22	1	2	R6814	RAM_DQS_N_R<4>	61 70
61 59	RAM_DQS_P<5>	22	1	2	R6805	RAM_DQS_P_R<5>	61 70
61 59	RAM_DQS_N<5>	22	1	2	R6815	RAM_DQS_N_R<5>	61 70
61 59	RAM_DQS_P<6>	22	1	2	R6806	RAM_DQS_P_R<6>	61 70
61 59	RAM_DQS_N<6>	22	1	2	R6816	RAM_DQS_N_R<6>	61 70
61 59	RAM_DQS_P<7>	22	1	2	R6807	RAM_DQS_P_R<7>	61 70
61 59	RAM_DQS_N<7>	22	1	2	R6817	RAM_DQS_N_R<7>	61 70

67 61 59	RAM_A<0>	5.1	1	8	RP6824	RAM_A_R<0>	61 63 69 70
67 61 59	RAM_A<1>	5.1	1	8	RP6823	RAM_A_R<1>	61 63 69 70
67 61 59	RAM_A<2>	5.1	2	7	RP6823	RAM_A_R<2>	61 63 69 70
67 61 59	RAM_A<3>	5.1	4	5	RP6822	RAM_A_R<3>	61 63 69 70
67 61 59	RAM_A<4>	5.1	3	6	RP6822	RAM_A_R<4>	61 63 69 70
67 61 59	RAM_A<5>	5.1	2	7	RP6822	RAM_A_R<5>	61 63 69 70
67 61 59	RAM_A<6>	5.1	1	8	RP6822	RAM_A_R<6>	61 63 69 70
67 61 59	RAM_A<7>	5.1	3	6	RP6821	RAM_A_R<7>	61 63 69 70
67 61 59	RAM_A<8>	5.1	4	5	RP6821	RAM_A_R<8>	61 63 69 70
67 61 59	RAM_A<9>	5.1	1	8	RP6821	RAM_A_R<9>	61 63 69 70
67 61 59	RAM_A<10>	5.1	3	6	RP6824	RAM_A_R<10>	61 63 69 70
67 61 59	RAM_A<11>	5.1	2	7	RP6821	RAM_A_R<11>	61 63 69 70
67 61 59	RAM_A<12>	5.1	4	5	RP6820	RAM_A_R<12>	61 63 69 70
67 61 59	RAM_A<13>	5.1	4	5	RP6825	RAM_A_R<13>	61 63 69 70
67 61 59	RAM_A<14>	5.1	2	7	RP6820	RAM_A_R<14>	61 63 69 70
67 61 59	RAM_A<15>	5.1	1	8	RP6820	RAM_A_R<15>	61 63 69 70

RAM_A_R<0>	1	ZT6800	1	
RAM_A_R<1>	1	ZT6801	1	
RAM_A_R<2>	1	ZT6802	1	
RAM_A_R<3>	1	ZT6803	1	
RAM_A_R<4>	1	ZT6804	1	
RAM_A_R<5>	1	ZT6805	1	
RAM_A_R<6>	1	ZT6806	1	
RAM_A_R<7>	1	ZT6807	1	
RAM_A_R<8>	1	ZT6808	1	
RAM_A_R<9>	1	ZT6809	1	
RAM_A_R<10>	1	ZT6810	1	
RAM_A_R<11>	1	ZT6811	1	
RAM_A_R<12>	1	ZT6812	1	
RAM_A_R<13>	1	ZT6813	1	
RAM_A_R<14>	1	ZT6814	1	
RAM_A_R<15>	1	ZT6815	1	

VIAS FOR ECC STUB

67 61 59	RAM_BA<0>	5.1	4	5	RP6824	RAM_BA_R<0>	61 63 69 70
67 61 59	RAM_BA<1>	5.1	2	7	RP6824	RAM_BA_R<1>	61 63 69 70
67 61 59	RAM_BA<2>	5.1	3	6	RP6820	RAM_BA_R<2>	61 63 69 70
67 61 59	RAM_RAS_L	5.1	1	8	RP6825	RAM_RAS_L_R	61 63 69 70
67 61 59	RAM_CAS_L	5.1	3	6	RP6825	RAM_CAS_L_R	61 63 69 70
67 61 59	RAM_WE_L	5.1	2	7	RP6825	RAM_WE_L_R	61 63 69 70

RAM_BA_R<0>	1	ZT6820
RAM_BA_R<1>	1	ZT6821
RAM_BA_R<2>	1	ZT6822
RAM_RAS_L_R	1	ZT6825
RAM_CAS_L_R	1	ZT6826
RAM_WE_L_R	1	ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870 24PF 5% 50V C0G 402		RAM_CS_L_R<0> 61 63 69 70	C6871 2PF +/-0.25PF 50V C0G 402-1
C6880 24PF 5% 50V C0G 402		RAM_CKE_R<0> 61 62 63 69 70	C6881 2PF +/-0.25PF 50V C0G 402-1
C6890 24PF 5% 50V C0G 402		RAM_ODT_R<0> 61 63 69 70	C6891 2PF +/-0.25PF 50V C0G 402-1

MLB Mem Series Term

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

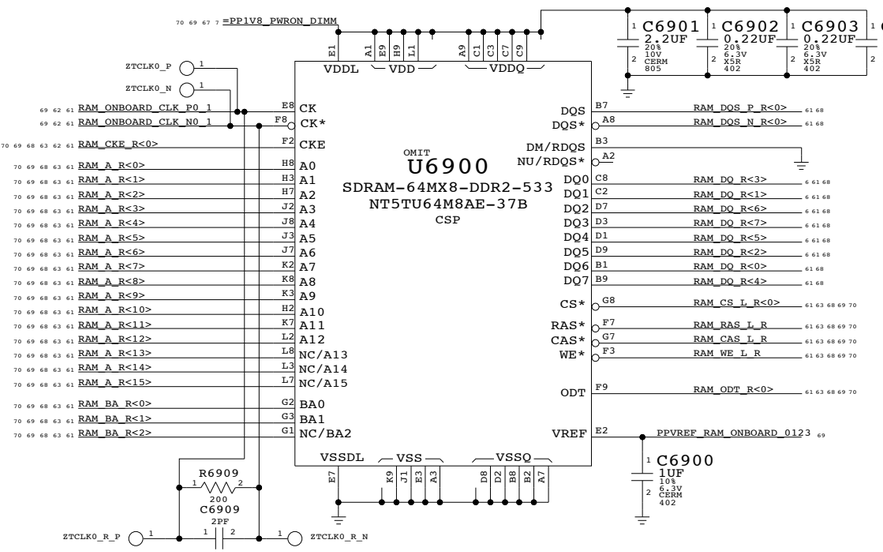
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

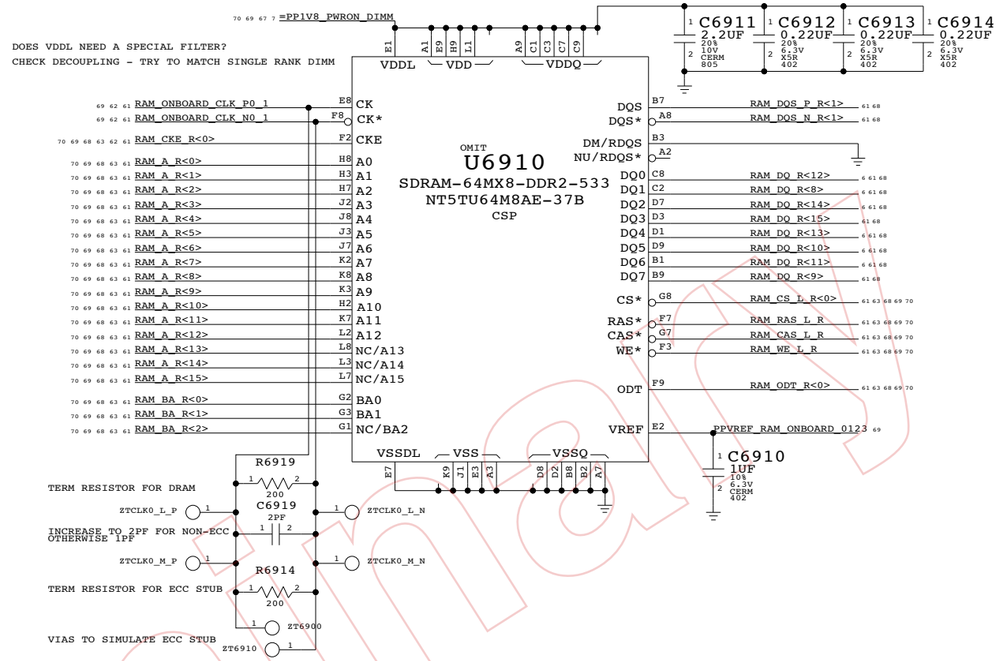
II NOT TO REPRODUCE OR COPY IT

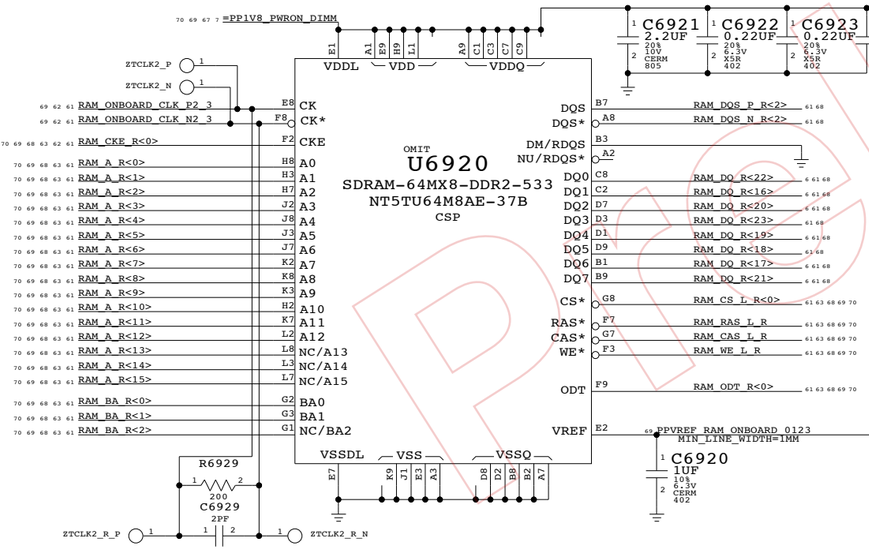
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

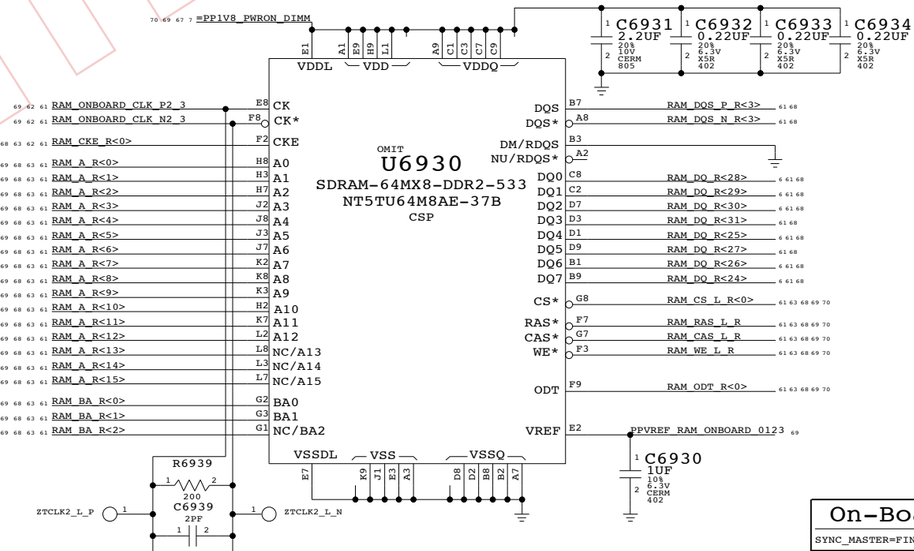
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 68 OF 154	









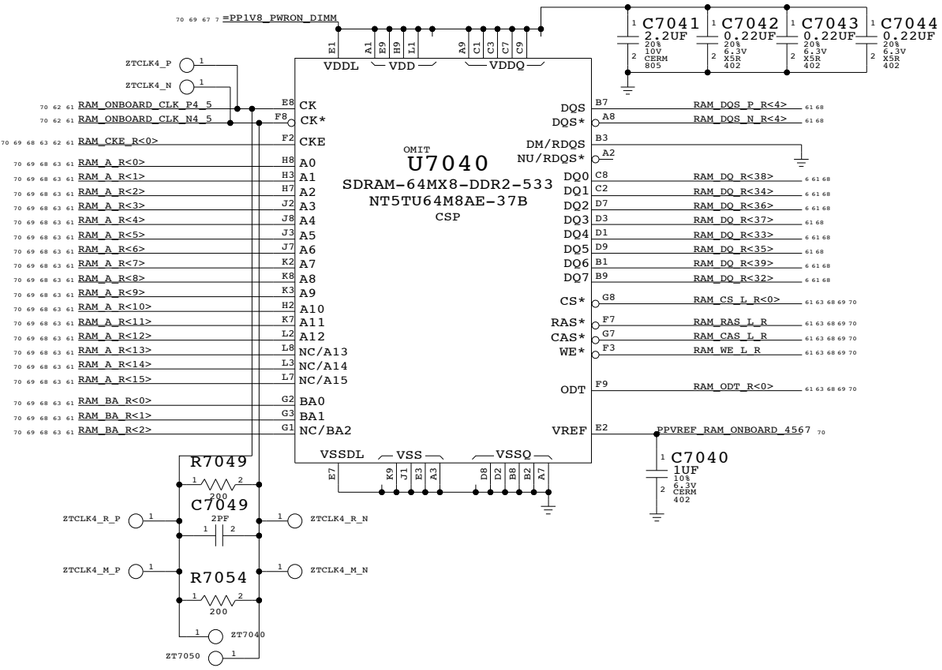
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	

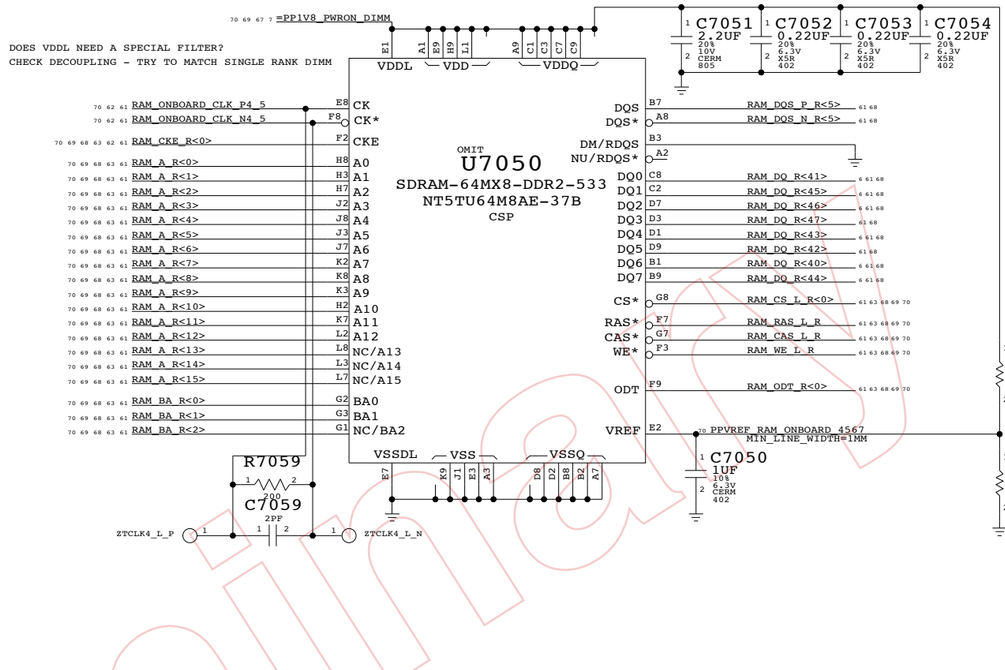
On-Board DDR SDRAM

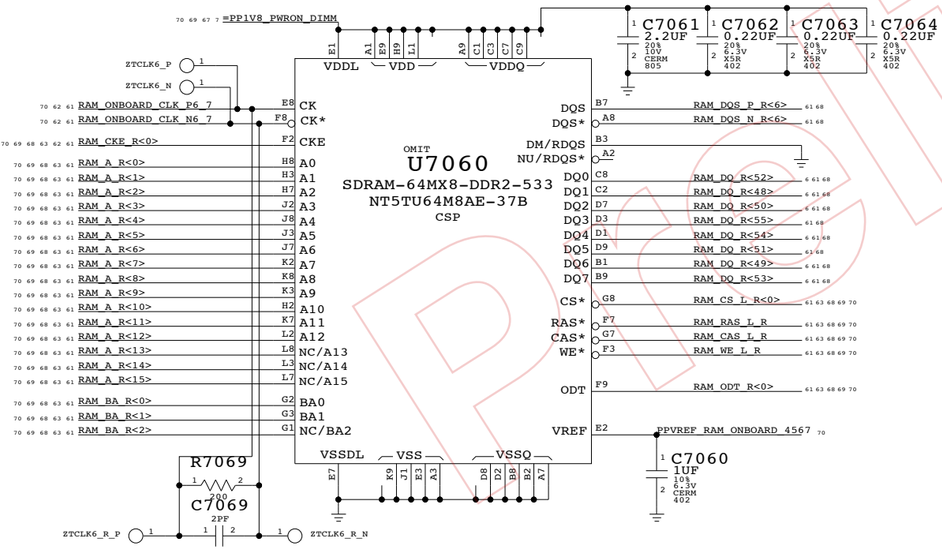
SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

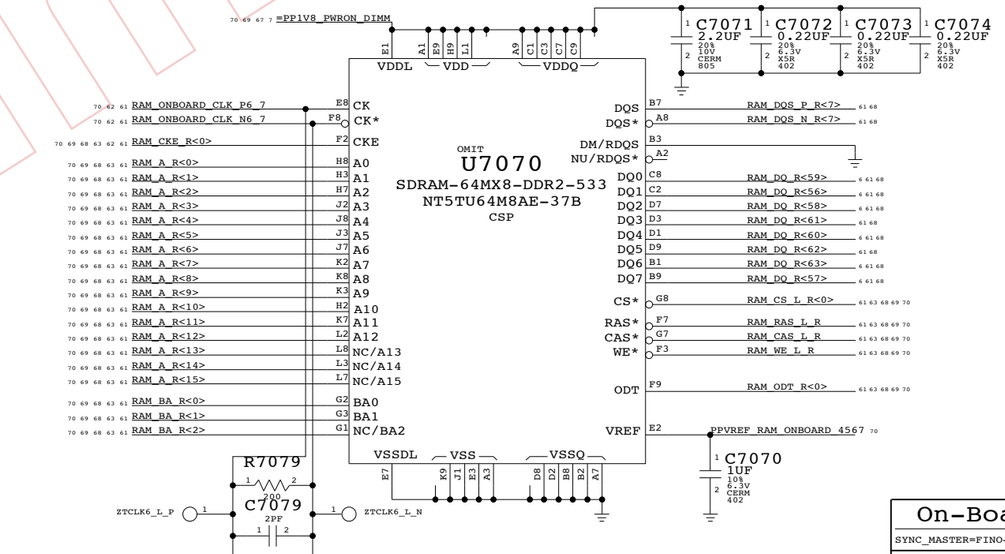
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 69 OF 154	









On-Board DDR SDRAM

SYNC_MASTER=FINO-RT SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 70 OF 154	

KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

82 7 =PP2V5_PWRON_NB_PCIE
L8200 0.22UH 0805-1
C8200 0.01UF 10% 16V CERM 402
C8201 10UF 10% 6.3V X5R 805
C8202 1UF 10% 6.3V CERM 402
PWR_PCIE_A_AVDD_2 82 97
97 82 6 KOD_G10_GND (THIS PAGE)

82 7 =PP2V5_PWRON_NB_PCIE
L8201 0.22UH 0805-1
C8203 0.01UF 10% 16V CERM 402
C8204 10UF 10% 6.3V X5R 805
C8205 1UF 10% 6.3V CERM 402
PWR_PCIE_A_AVDD_1 82 97
97 82 6 KOD_K07_GND (THIS PAGE)

82 7 =PP2V5_PWRON_NB_PCIE
L8202 0.22UH 0805-1
C8206 0.01UF 10% 16V CERM 402
C8207 10UF 10% 6.3V X5R 805
C8208 1UF 10% 6.3V CERM 402
PWR_PCIE_A_AVDD_0 82 97
97 82 6 KOD_H05_GND (THIS PAGE)

97 82 PWR_PCIE_A_AVDD_2
97 82 PWR_PCIE_A_AVDD_1
97 82 PWR_PCIE_A_AVDD_0
97 PWR_PCIE_A_AVDD_A
97 PWR_PCIE_A_AVDD_B
97 PWR_PCIE_A_AVDD_C

J06 PCIE_AVDD_0 (1.65V-2.75V) SERDES
J07 PCIE_AVDD_1 (1.65V-2.75V) SERDES
H11 PCIE_AVDD_2 (1.65V-2.75V) SERDES
J12 PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL
K13 PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL
J09 PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL

U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE

(1.6V-1.2V)
A04 PCIE_VDD
A08 PCIE_VDD
A12 PCIE_VDD
B06 PCIE_VDD
B10 PCIE_VDD
C03 PCIE_VDD
D01 PCIE_VDD
D04 PCIE_VDD
D08 PCIE_VDD
D12 PCIE_VDD
E06 PCIE_VDD
E10 PCIE_VDD
E14 PCIE_VDD
82 7 =PPVCORE_PWRON_NB_PCIE

(1.6V-1.2V)
F02 PCIE_VDD
F05 PCIE_VDD
G08 PCIE_VDD
G12 PCIE_VDD
H01 PCIE_VDD
H04 PCIE_VDD
H07 PCIE_VDD
H10 PCIE_VDD
H14 PCIE_VDD
K12 PCIE_VDD
L11 PCIE_VDD
L14 PCIE_VDD
M12 PCIE_VDD
=PPVCORE_PWRON_NB_PCIE 7 82

L8203 0.22UH 0805-1
=PP2V5_PWRON_NB_PCIE 7 82
97 PWR_PCIE_A_AVDD
C8222 1UF 10% 6.3V CERM 402
C8225 1UF 10% 6.3V CERM 402
C8223 10UF 10% 6.3V X5R 805
C8224 0.01UF 10% 16V CERM 402
KOD_L13_GND 6 82 97 (THIS PAGE)
KOD_J13_GND 6 82 97 (THIS PAGE)

L8205 0.22UH 0805-1
=PP2V5_PWRON_NB_PCIE 7 82
C8228 1UF 10% 6.3V CERM 402
C8229 10UF 10% 6.3V X5R 805
C8230 0.01UF 10% 16V CERM 402
KOD_H08_GND 6 82 97 (THIS PAGE)

KODIAK PCI-E 100MHZ REFCLK
PP8201 P4MM SM
100+ 97 9 CLK_KOD_100M_PF<0>
100- 97 9 CLK_KOD_100M_NF<0>
P4MM SM PP8200

82 7 =PPVCORE_PWRON_NB_PCIE
NOSTUFF R8206 8.2K 5% 1/16W MF-LF 402
R8202 20.5 1% 1/16W MF-LF 402
97 26 CLK_KOD_100M_P<0>
97 9 100M_P<0>
C8245 0.01UF 10% 16V CERM 402
NOSTUFF C8244 0.01UF 10% 16V CERM 402
100M_G
R8203 29.4 1% 1/16W MF-LF 402
R8204 29.4 1% 1/16W MF-LF 402
R8205 20.5 1% 1/16W MF-LF 402
97 26 CLK_KOD_100M_N<0>
97 9 100M_N<0>
C8246 0.01UF 10% 16V CERM 402
NOSTUFF R8207 8.2K 5% 1/16W MF-LF 402

KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

82 7 =PP2V5_PWRON_NB_PCIE
R8200 8.2K 5% 1/16W MF-LF 402
84 6 PCIE_SLOTA_PRSNT_L
R8201 200 1% 1/16W MF-LF 402

J11 PCIE_REFCLK_P
J10 PCIE_REFCLK_N (100MHZ)

97 84 9 PCIE_SLOTA_TO_NB_N<0> G05 PCIE_HSIN0
97 84 9 PCIE_SLOTA_TO_NB_P<0> G04 PCIE_HSIP0
97 84 9 PCIE_SLOTA_TO_NB_N<1> G01 PCIE_HSIN1
97 84 9 PCIE_SLOTA_TO_NB_P<1> G02 PCIE_HSIP1
97 84 9 PCIE_SLOTA_TO_NB_N<2> C04 PCIE_HSIN2
97 84 9 PCIE_SLOTA_TO_NB_P<2> C05 PCIE_HSIP2
97 84 9 PCIE_SLOTA_TO_NB_N<3> C07 PCIE_HSIN3
97 84 9 PCIE_SLOTA_TO_NB_P<3> C06 PCIE_HSIP3
97 84 9 PCIE_SLOTA_TO_NB_N<4> E01 PCIE_HSIN4
97 84 9 PCIE_SLOTA_TO_NB_P<4> E02 PCIE_HSIP4
97 84 9 PCIE_SLOTA_TO_NB_N<5> J05 PCIE_HSIN5
97 84 9 PCIE_SLOTA_TO_NB_P<5> J04 PCIE_HSIP5
97 84 9 PCIE_SLOTA_TO_NB_N<6> H06 PCIE_HSIN6
97 84 9 PCIE_SLOTA_TO_NB_P<6> G06 PCIE_HSIP6
97 84 9 PCIE_SLOTA_TO_NB_N<7> E05 PCIE_HSIN7
97 84 9 PCIE_SLOTA_TO_NB_P<7> D05 PCIE_HSIP7
97 84 9 PCIE_SLOTA_TO_NB_N<8> D11 PCIE_HSIN8
97 84 9 PCIE_SLOTA_TO_NB_P<8> E11 PCIE_HSIP8
97 84 9 PCIE_SLOTA_TO_NB_N<9> F12 PCIE_HSIN9
97 84 9 PCIE_SLOTA_TO_NB_P<9> F13 PCIE_HSIP9
97 84 9 PCIE_SLOTA_TO_NB_N<10> H09 PCIE_HSIN10
97 84 9 PCIE_SLOTA_TO_NB_P<10> G09 PCIE_HSIP10
97 84 9 PCIE_SLOTA_TO_NB_N<11> F09 PCIE_HSIN11
97 84 9 PCIE_SLOTA_TO_NB_P<11> F08 PCIE_HSIP11
97 84 9 PCIE_SLOTA_TO_NB_N<12> G13 PCIE_HSIN12
97 84 9 PCIE_SLOTA_TO_NB_P<12> N13 PCIE_HSIP12
97 84 9 PCIE_SLOTA_TO_NB_N<13> C13 PCIE_HSIN13
97 84 9 PCIE_SLOTA_TO_NB_P<13> C12 PCIE_HSIP13
97 84 9 PCIE_SLOTA_TO_NB_N<14> D07 PCIE_HSIN14
97 84 9 PCIE_SLOTA_TO_NB_P<14> E07 PCIE_HSIP14
97 84 9 PCIE_SLOTA_TO_NB_N<15> G07 PCIE_HSIN15
97 84 9 PCIE_SLOTA_TO_NB_P<15> F07 PCIE_HSIP15
AJ02 PCIE_PRESENTN
F14 PCIE_VCAL_RES0
J14 PCIE_VCAL_RES1

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)
=PPVCORE_PWRON_NB_PCIE 7 82
C8209 C8210 C8211 C8212
C8213 C8214 C8215 C8216
C8217 C8218 C8219 C8220 C8221
1UF 10% 6.3V CERM 402

A06 PCIE_GND
A10 PCIE_GND
B02 PCIE_GND
B04 PCIE_GND
B08 PCIE_GND
B12 PCIE_GND
D02 PCIE_GND
D06 PCIE_GND
D10 PCIE_GND
D14 PCIE_GND
E08 PCIE_GND
E12 PCIE_GND
F01 PCIE_GND

F04 PCIE_GND
F06 PCIE_GND
G14 PCIE_GND
H02 PCIE_GND
H12 PCIE_GND
K10 PCIE_GND
K14 PCIE_GND
L12 PCIE_GND
M11 PCIE_GND
M13 PCIE_GND

AVDD_0_GND AVDD_1_GND AVDD_2_GND REFCLK_AGNDA REFCLK_AGNDB REFCLK_AGND2
H05 K07 G10 J13 L13 H08
97 82 6 KOD_H05_GND
97 82 6 KOD_K07_GND
97 82 6 KOD_G10_GND (THIS PAGE, X3)
XW8200 XW8201 XW8202 XW8203 XW8204 XW8205
KOD_H08_GND 6 82 97
KOD_L13_GND 6 82 97
KOD_J13_GND 6 82 97 (THIS PAGE, X3)

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

PCIE_HSON0	D03	97 PCIE_NB_TO_SLOTA_NF<0>	0.1UF	C8247	PCIE_NB_TO_SLOTA_N<0>	84 97
PCIE_HSOP0	E03	97 PCIE_NB_TO_SLOTA_PF<0>	0.1UF	C8248	PCIE_NB_TO_SLOTA_P<0>	84 97
PCIE_HSON1	J01	97 PCIE_NB_TO_SLOTA_NF<1>	0.1UF	C8249	PCIE_NB_TO_SLOTA_N<1>	84 97
PCIE_HSOP1	J02	97 PCIE_NB_TO_SLOTA_PF<1>	0.1UF	C8250	PCIE_NB_TO_SLOTA_P<1>	84 97
PCIE_HSON2	C01	97 PCIE_NB_TO_SLOTA_NF<2>	0.1UF	C8251	PCIE_NB_TO_SLOTA_N<2>	84 97
PCIE_HSOP2	C02	97 PCIE_NB_TO_SLOTA_PF<2>	0.1UF	C8252	PCIE_NB_TO_SLOTA_P<2>	84 97
PCIE_HSON3	A07	97 PCIE_NB_TO_SLOTA_NF<3>	0.1UF	C8253	PCIE_NB_TO_SLOTA_N<3>	84 97
PCIE_HSOP3	B07	97 PCIE_NB_TO_SLOTA_PF<3>	0.1UF	C8254	PCIE_NB_TO_SLOTA_P<3>	84 97
PCIE_HSON4	F03	97 PCIE_NB_TO_SLOTA_NF<4>	0.1UF	C8255	PCIE_NB_TO_SLOTA_N<4>	84 97
PCIE_HSOP4	G03	97 PCIE_NB_TO_SLOTA_PF<4>	0.1UF	C8256	PCIE_NB_TO_SLOTA_P<4>	84 97
PCIE_HSON5	H03	97 PCIE_NB_TO_SLOTA_NF<5>	0.1UF	C8257	PCIE_NB_TO_SLOTA_N<5>	84 97
PCIE_HSOP5	J03	97 PCIE_NB_TO_SLOTA_PF<5>	0.1UF	C8258	PCIE_NB_TO_SLOTA_P<5>	84 97
PCIE_HSON6	A03	97 PCIE_NB_TO_SLOTA_NF<6>	0.1UF	C8259	PCIE_NB_TO_SLOTA_N<6>	84 97
PCIE_HSOP6	B03	97 PCIE_NB_TO_SLOTA_PF<6>	0.1UF	C8260	PCIE_NB_TO_SLOTA_P<6>	84 97
PCIE_HSON7	A05	97 PCIE_NB_TO_SLOTA_NF<7>	0.1UF	C8261	PCIE_NB_TO_SLOTA_N<7>	84 97
PCIE_HSOP7	B05	97 PCIE_NB_TO_SLOTA_PF<7>	0.1UF	C8262	PCIE_NB_TO_SLOTA_P<7>	84 97
PCIE_HSON8	C11	97 PCIE_NB_TO_SLOTA_NF<8>	0.1UF	C8263	PCIE_NB_TO_SLOTA_N<8>	84 97
PCIE_HSOP8	C10	97 PCIE_NB_TO_SLOTA_PF<8>	0.1UF	C8264	PCIE_NB_TO_SLOTA_P<8>	84 97
PCIE_HSON9	B11	97 PCIE_NB_TO_SLOTA_NF<9>	0.1UF	C8265	PCIE_NB_TO_SLOTA_N<9>	84 97
PCIE_HSOP9	A11	97 PCIE_NB_TO_SLOTA_PF<9>	0.1UF	C8266	PCIE_NB_TO_SLOTA_P<9>	84 97
PCIE_HSON10	F11	97 PCIE_NB_TO_SLOTA_NF<10>	0.1UF	C8267	PCIE_NB_TO_SLOTA_N<10>	84 97
PCIE_HSOP10	F10	97 PCIE_NB_TO_SLOTA_PF<10>	0.1UF	C8268	PCIE_NB_TO_SLOTA_P<10>	84 97
PCIE_HSON11	B09	97 PCIE_NB_TO_SLOTA_NF<11>	0.1UF	C8269	PCIE_NB_TO_SLOTA_N<11>	84 97
PCIE_HSOP11	A09	97 PCIE_NB_TO_SLOTA_PF<11>	0.1UF	C8270	PCIE_NB_TO_SLOTA_P<11>	84 97
PCIE_HSON12	D13	97 PCIE_NB_TO_SLOTA_NF<12>	0.1UF	C8271	PCIE_NB_TO_SLOTA_N<12>	84 97
PCIE_HSOP12	E13	97 PCIE_NB_TO_SLOTA_PF<12>	0.1UF	C8272	PCIE_NB_TO_SLOTA_P<12>	84 97
PCIE_HSON13	B13	97 PCIE_NB_TO_SLOTA_NF<13>	0.1UF	C8273	PCIE_NB_TO_SLOTA_N<13>	84 97
PCIE_HSOP13	A13	97 PCIE_NB_TO_SLOTA_PF<13>	0.1UF	C8274	PCIE_NB_TO_SLOTA_P<13>	84 97
PCIE_HSON14	D09	97 PCIE_NB_TO_SLOTA_NF<14>	0.1UF	C8275	PCIE_NB_TO_SLOTA_N<14>	84 97
PCIE_HSOP14	E09	97 PCIE_NB_TO_SLOTA_PF<14>	0.1UF	C8276	PCIE_NB_TO_SLOTA_P<14>	84 97
PCIE_HSON15	C08	97 PCIE_NB_TO_SLOTA_NF<15>	0.1UF	C8277	PCIE_NB_TO_SLOTA_N<15>	84 97
PCIE_HSOP15	C09	97 PCIE_NB_TO_SLOTA_PF<15>	0.1UF	C8278	PCIE_NB_TO_SLOTA_P<15>	84 97

(DNU)
PCIE_AVREG_2 G11 NC_A_AVREG_2 6
PCIE_AVREG_1 J08 NC_A_AVREG_1 6
PCIE_AVREG_0 E04 NC_A_AVREG_0 6

=PPVCORE_PWRON_NB_PCIE 7 82
C8231 C8232 C8233 C8234 C8235 C8236
C8241 C8242 C8243 C8237 C8238 C8239 C8240
1UF 10% 6.3V CERM 402

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

PAGE 82

KODIAK PCI-E X16

SYNC_MASTER=Q63	SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY
LAST MODIFIED=Thu May 19 14:09:36 2005
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 82 OF 154	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT
338S0244	1	IC,RV380 XT, GRAPHICS CTLR	U8400	RV380XT

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

THIS SHOULD BE ALIASED TO PPVCORE_GPU WITH RV370 AND PP1V2_RUN WITH RV380

SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN

PLACE R8470 CLOSE TO U9670

GROUND VIAS FOR LAYER TRANSITIONS

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

GPU PCIe

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 84	OF 154

GPU VCORE VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505 M23=1.250V M33=1.295V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

DEREK: IS 30MV RIPPLE ACCEPTABLE? IF NOT STUFF MORE CAPS

U700 74LCX125 TSSOP
SYS_POWERUP_L → GPU_POWERUP_L

U8500 IRU3037ACS SOI
VCC VC
HD U8500_GATE_H
LD U8500_GATE_L
FB U8500_FEEDBACK
SS U8500_SS
COMP U8500_COMP
GND

Q8500 2N7002 SOT23-LF
Q8501 IRF7807ZPBF SO-8
Q8502 IRF7807ZPBF SO-8

D8501 MBR0520LXXG SOD-123
D8502 MBR0520LXXG SOD-123
D8503 MBR0520LXXG SOD-123

R8500 4.7 5% 1/8W MF-LF 805
R8502 0 5% 1/8W MF-LF 805
R8501 8.2K 5% 1/16W MF-LF 402
R8504 0.51 1% 1/4W FF 1206-LF
R8505 10K 1% 1/16W MF-LF 402
R8503 5.62K 1% 1/16W MF-LF 402
R8511 100K 5% 1/16W MF-LF 402

L8501 1.53UH SM

XW8500 SM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0291	1	RES,5.62K OHM,1/16W,1%,0402	R8503	RV370XT
114S0295	1	RES,6.19K OHM,1/16W,1%,0402	R8503	RV380XT

GPU 1.7V VDDC_CT

U8590 FAN2558 SOT23-6
VIN VOUT PG EN ADJ GND

R8597 3.3K 5% 1/16W MF-LF 402
R8590 10K 1% 1/16W MF-LF 402
R8591 5.36K 1% 1/16W MF-LF 402
R8594 100K 5% 1/16W MF-LF 402

Q8590 2N7002 SOT23-LF

PP1V7_GPU_VDDC_CT
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

VOUT = 0.59V * [1 + R8590 / R8591]
VOUT = 1.691V

GPU 1.20V PCIE PVDD

U8540 FAN2558 SOT23-6
VIN VOUT PG EN ADJ GND

R8542 3.3K 5% 1/16W MF-LF 402
R8540 10K 1% 1/16W MF-LF 402
R8541 9.53K 1% 1/16W MF-LF 402
R8544 47K 5% 1/16W MF-LF 402

Q8540 2N7002 SOT23-LF

PP1V2_GPU_PCIE_PVDD
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

VOUT = 0.59V * [1 + R8540 / R8541]
VOUT = 1.209V

GPU 1.80V TPVDD

U8560 FAN2558 SOT23-6
VIN VOUT PG EN ADJ GND

R8562 3.3K 5% 1/16W MF-LF 402
R8560 10K 1% 1/16W MF-LF 402
R8561 4.87K 1% 1/16W MF-LF 402

Q8560 2N7002 SOT23-LF

PP1V8_GPU_TPVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

VOUT = 0.59V * [1 + R8560 / R8561]
VOUT = 1.802V

GPU 2.5V A2VDD

U8570 MM1572FN SOT-25A
VIN VOUT CONT NOISE GND

R8570 10K 5% 1/16W MF-LF 402

Q8570 2N7002 SOT23-LF

PP2V5_GPU_A2VDD
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

GPU 1.8V VREG

U8580 MIC39102 SOP-8
IN OUT EN ADJ GND

R8580 3.3K 1% 1/16W MF-LF 402
R8581 453 1% 1/16W MF-LF 402
R8582 1K 1% 1/16W MF-LF 402

Q8580 2N7002 SOT23-LF

PP1V8_GPU
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE

POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

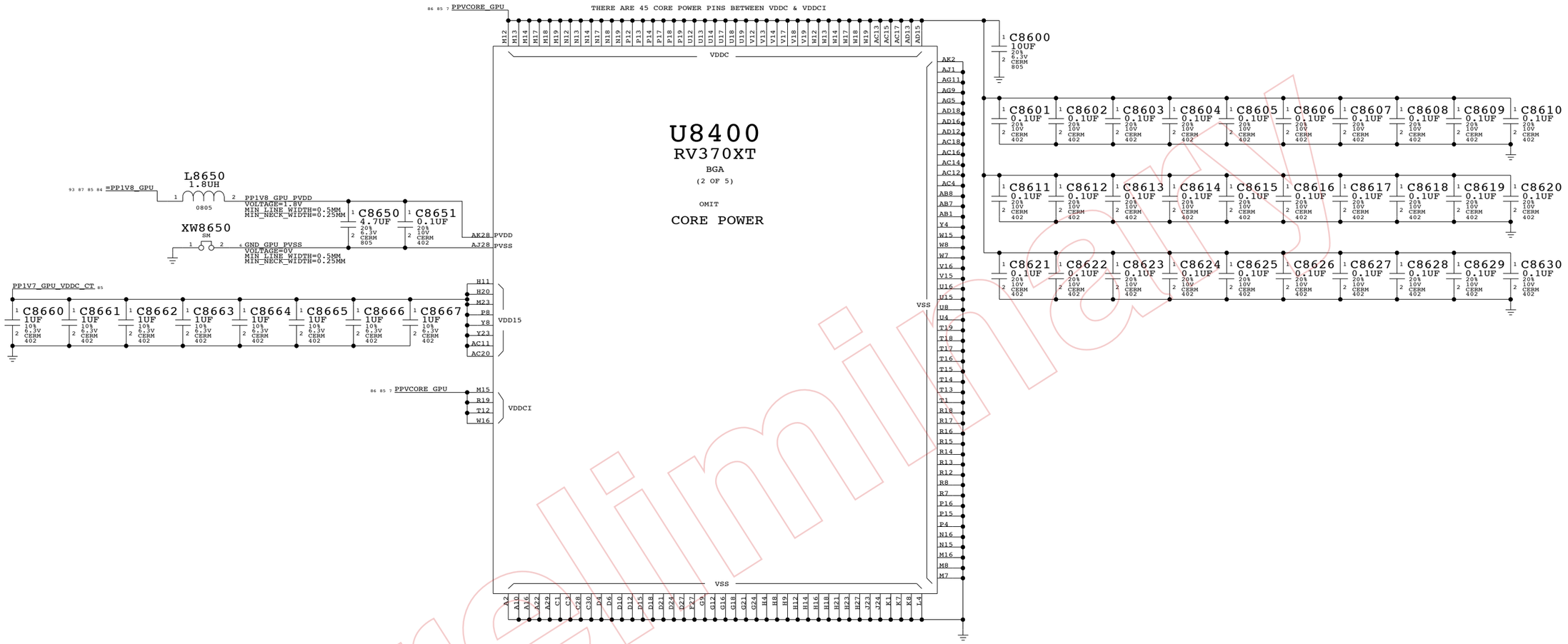
Graphics Vregs

SYNC_MASTER=M23-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE: NONE SHT 85 OF 154



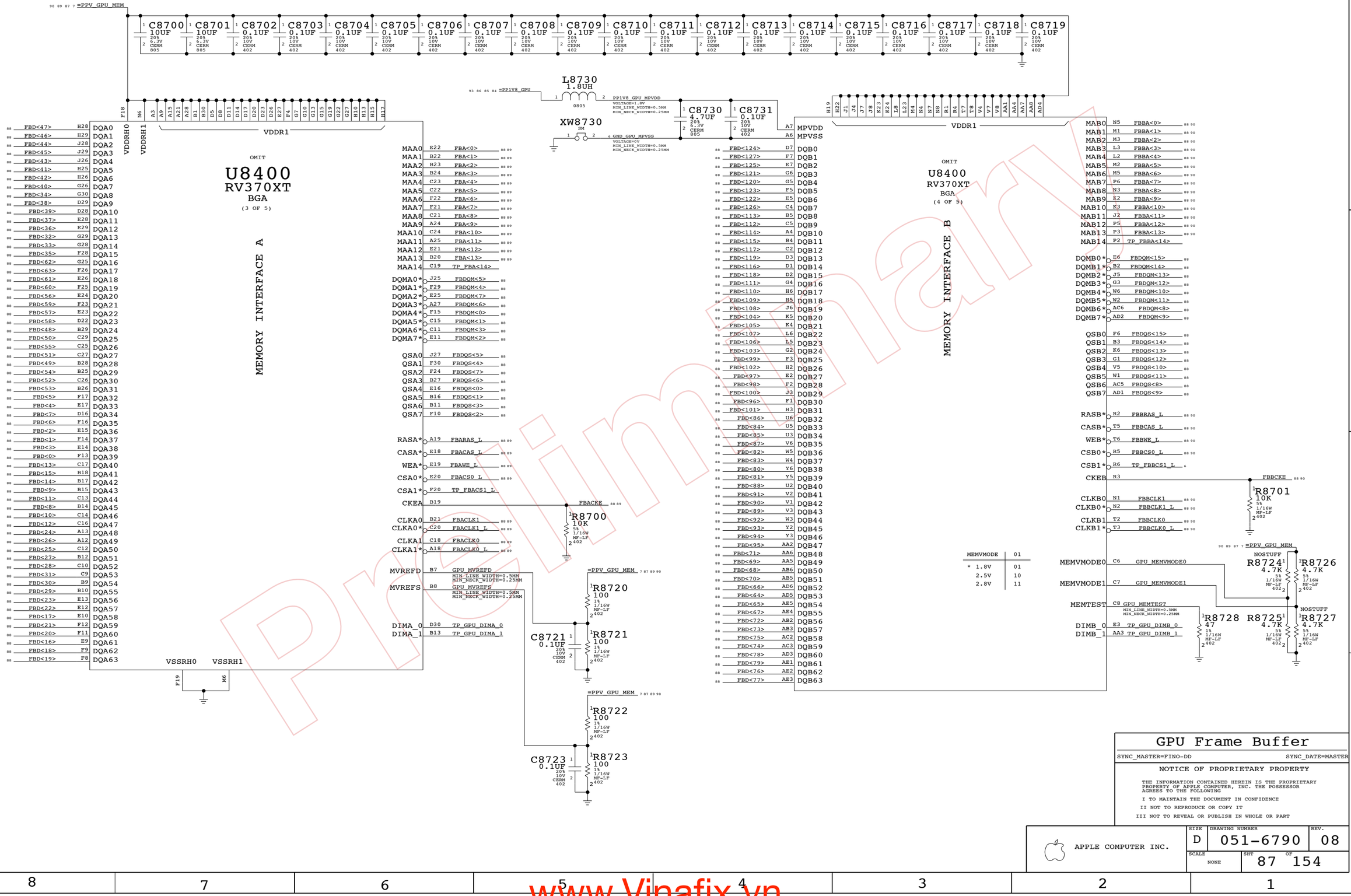
GPU Core Power

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

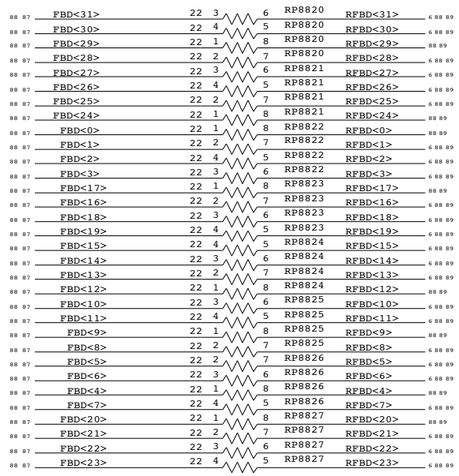
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

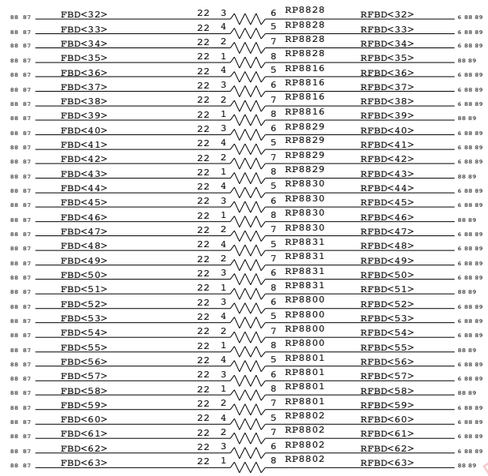
SCALE	SHT	OF
NONE	86	154

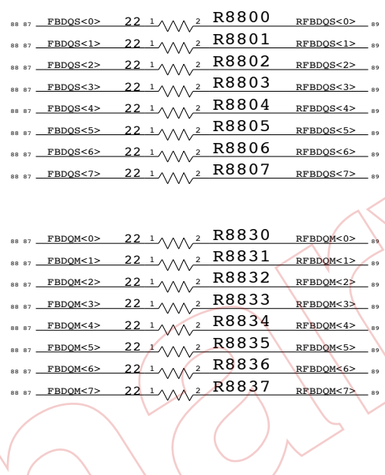


FRAME BUFFER A TERMINATION

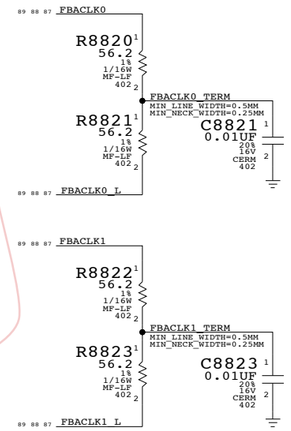
PLACE R'S CLOSE TO MEMORY



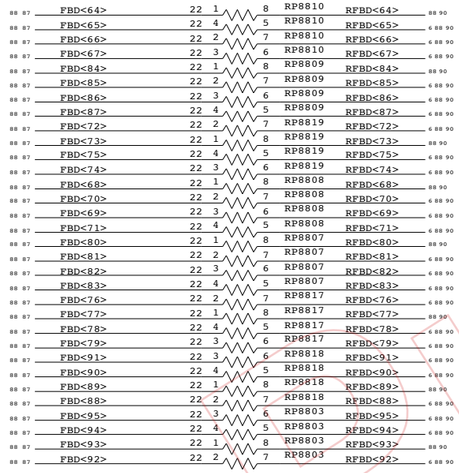


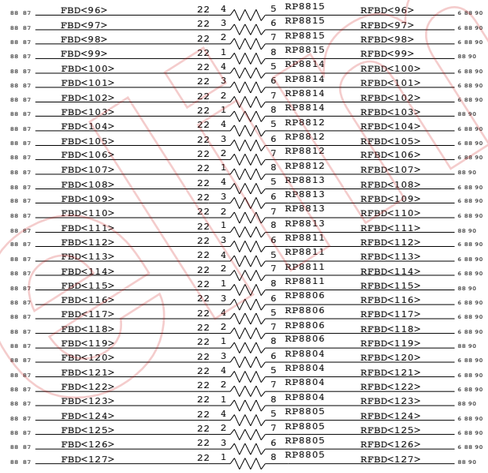


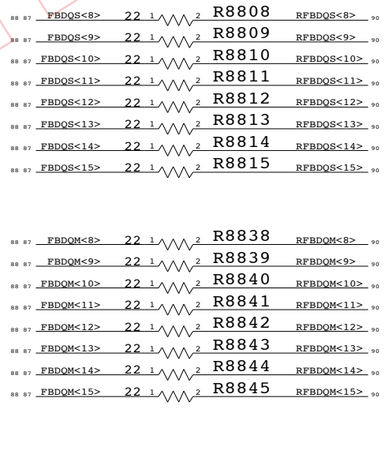
PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

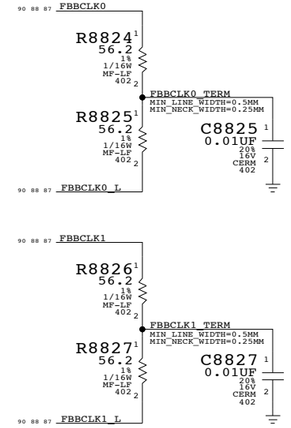


FRAME BUFFER B TERMINATION









	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FBD<127..0>		GPU_FB	GPU_FB		4425
RFBD<127..0>		GPU_FB	GPU_FB		4426
FBA<13..0>		GPU_FB	GPU_FB		4427
FBBA<13..0>		GPU_FB	GPU_FB		4429
FBDQM<15..0>		GPU_FB	GPU_FB		4430
FBDQS<15..0>		GPU_FB	GPU_FBDQS		4431
FBARAS_L		GPU_FB	GPU_FB		4436
FBACAS_L		GPU_FB	GPU_FB		4437
FBAWE_L		GPU_FB	GPU_FB		4438
FBACS0_L		GPU_FB	GPU_FB		4439
FBACKE		GPU_FB	GPU_FB		4440
FBBRAS_L		GPU_FB	GPU_FB		4444
FBBCAS_L		GPU_FB	GPU_FB		4445
FBBWE_L		GPU_FB	GPU_FB		4446
FBBCS0_L		GPU_FB	GPU_FB		4447
FBBCKE		GPU_FB	GPU_FB		4448

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0	4483
FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0	4484
FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1	4489
FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1	4490
FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0	4491
FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0	4492
FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1	4496
FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1	4497

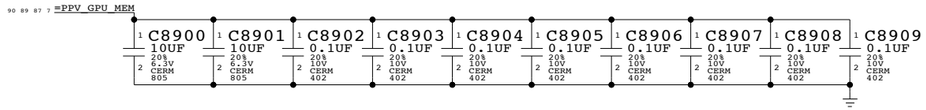
FB Series Termination

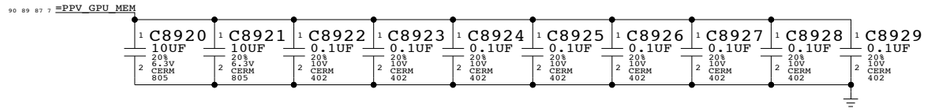
SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

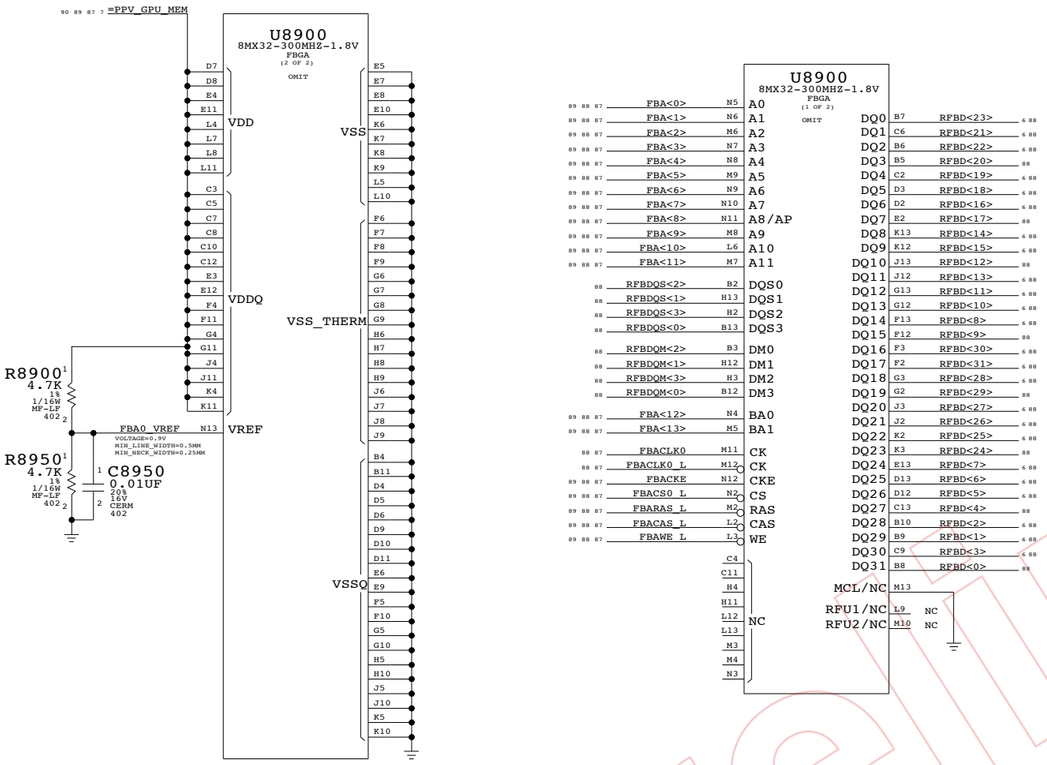
APPLE COMPUTER INC.

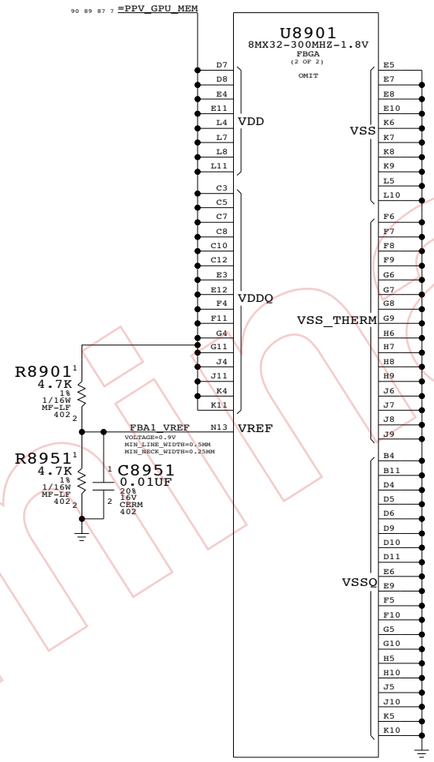
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

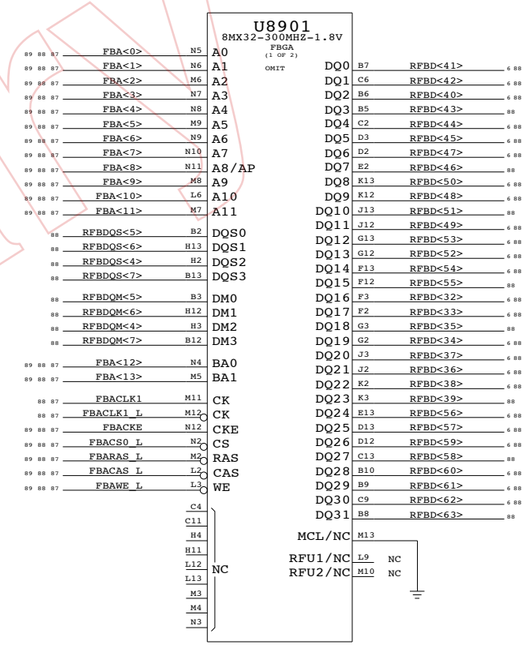
SCALE	SHT	OF
NONE	88	154

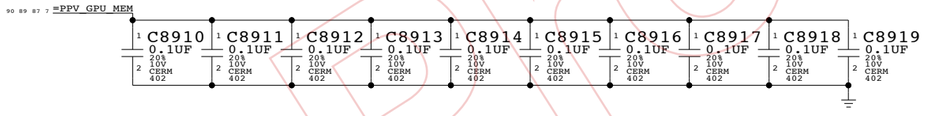


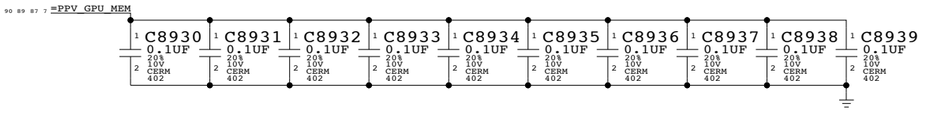




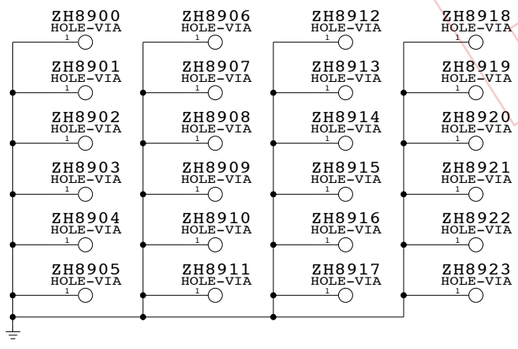








GROUND VIAS FOR SIGNAL LAYER TRANSITIONS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM A

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

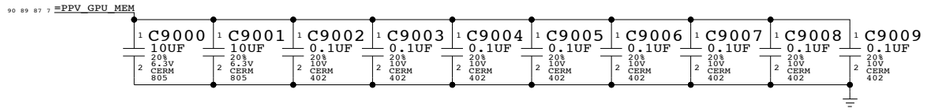
II NOT TO REPRODUCE OR COPY IT

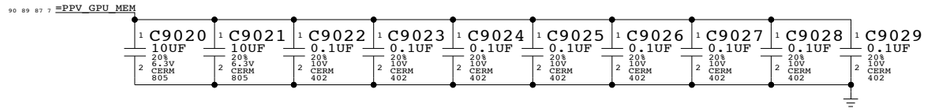
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

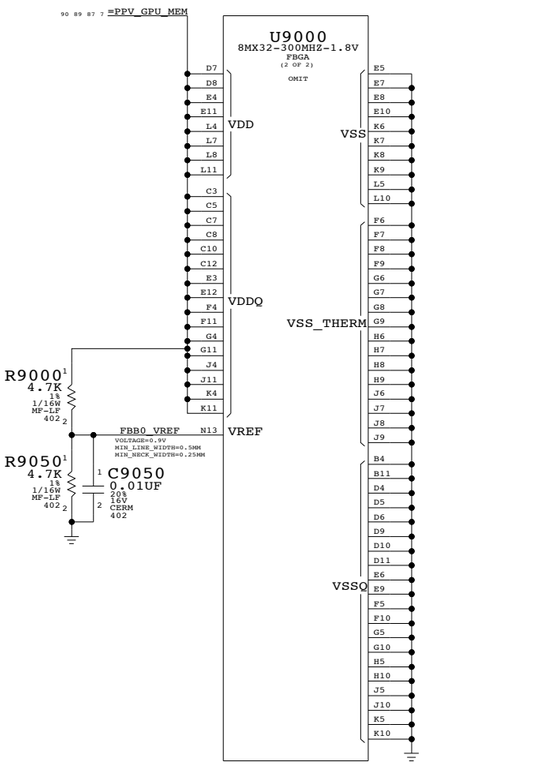
APPLE COMPUTER INC.

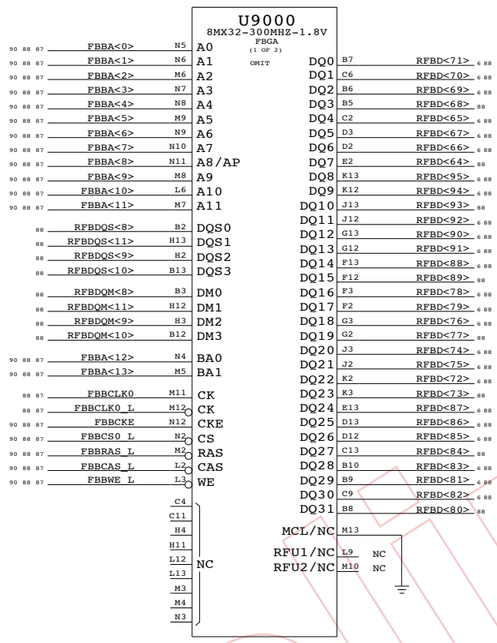
SIZE	DRAWING NUMBER	REV.
D	051-6790	08

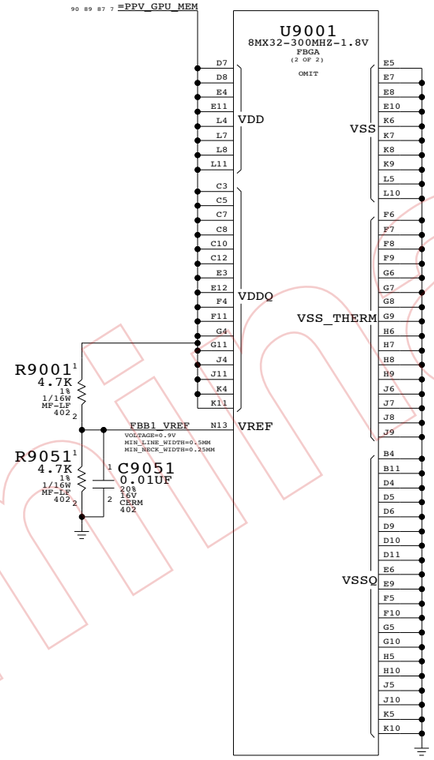
SCALE	SHT	OF
NONE	89	154

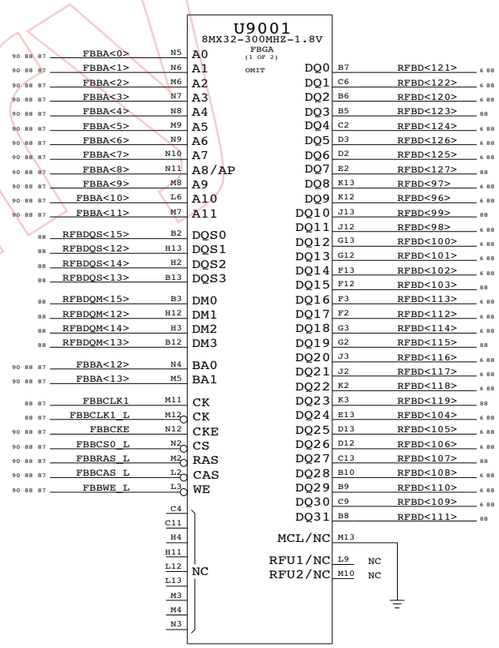


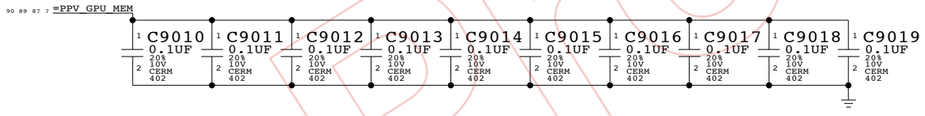


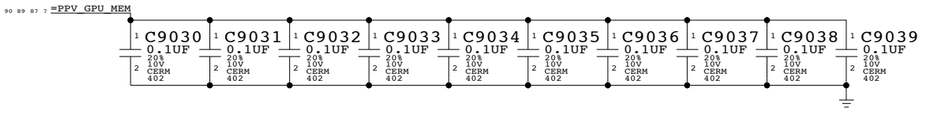




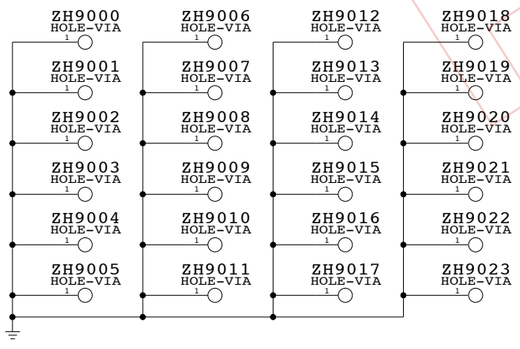








GROUND VIAS FOR SIGNAL LAYER TRANSITIONS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM B

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

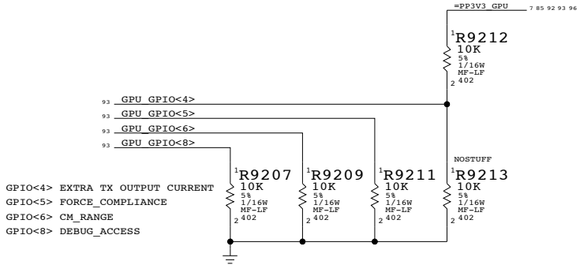
II NOT TO REPRODUCE OR COPY IT

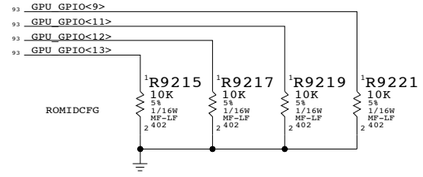
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

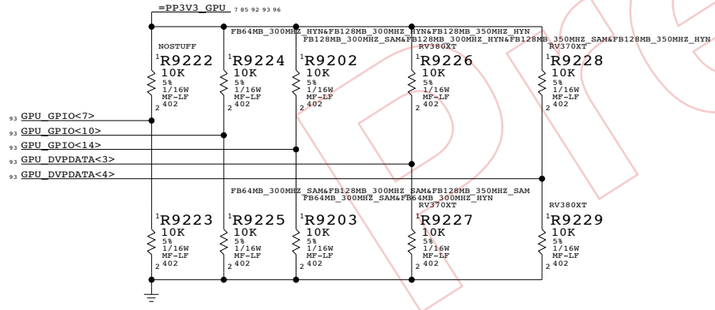
SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 90 OF 154	

ATI STRAPS



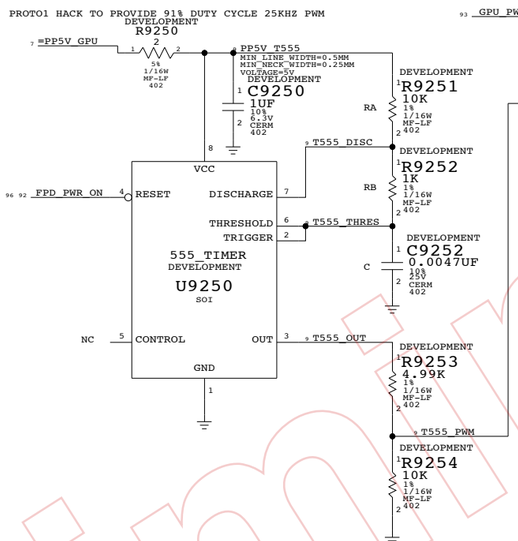


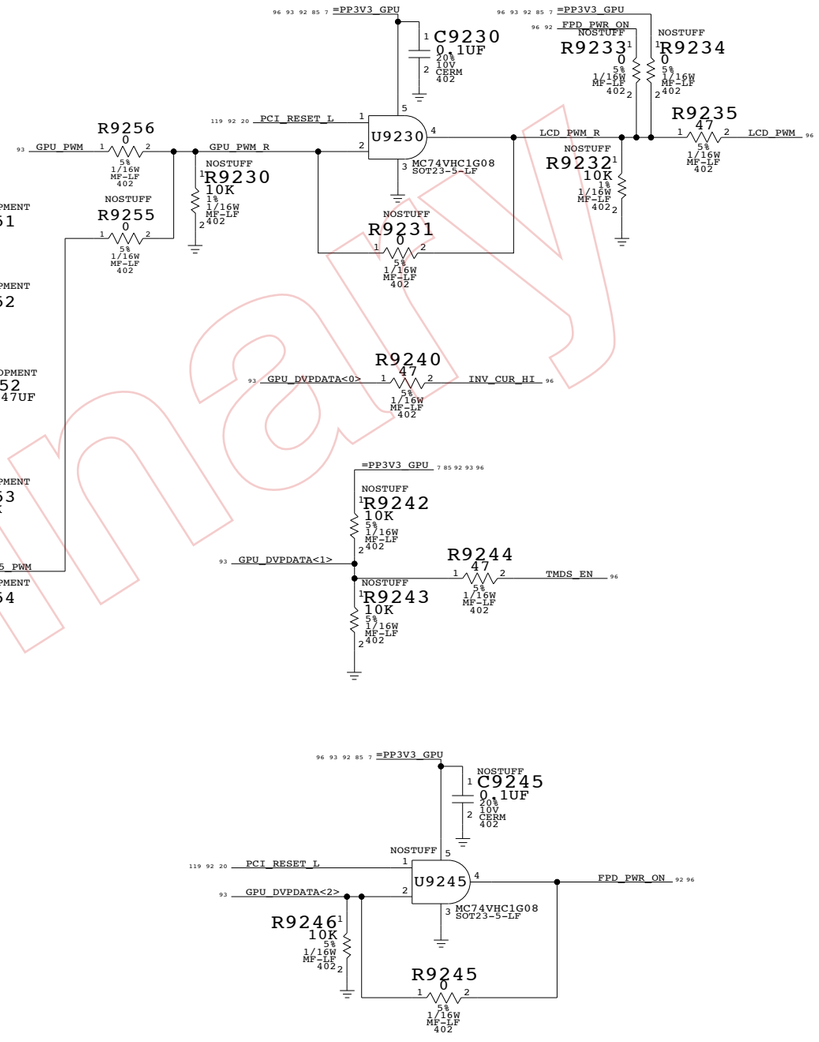
MEMORY STRAPS



GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS





GPU Straps

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT: 92	OF: 154

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

(PLACE R9371 CLOSE TO OSC)

(PLACE THE OSCILLATOR AND R9372 AND R9373 CLOSE TO ATI PIN AH28)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0131	1	RES,130 OHM,1/16W,1%,0402	R9373	RV370XT
114S0134	1	RES,140 OHM,1/16W,1%,0402	R9373	RV380XT

U8400 RV370XT BGA (5 OF 5)

OMIT

NC NO CONNECTS NC

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_TCKM	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	I2C	I2C	
	I2C	I2C	
	I2C	I2C	
	I2C	I2C	

GPU THERMAL SENSOR

PLACE C9392 CLOSE TO TEMP SENSOR

PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

GPU DVI & DACs

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE: NONE SHT 93 OF 154

INTERNAL LCD

NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TCKP	GPU_TMDS	TCK
TCKM	GPU_TMDS	TCK
TD0P	GPU_TMDS	TD0
TD0M	GPU_TMDS	TD0
TD1P	GPU_TMDS	TD1
TD1M	GPU_TMDS	TD1
TD2P	GPU_TMDS	TD2
TD2M	GPU_TMDS	TD2

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

TMDS_D2M — R9604 332 1% 1/16W MF-LF 402 — TD2M
TMDS_D2P — NOSTUFF R9626 0 — L9602 90-OHM — NOSTUFF R9627 0 — TD2P
TMDS_D1M — R9603 332 1% 1/16W MF-LF 402 — TD1M
TMDS_D1P — NOSTUFF R9628 0 — L9608 90-OHM — NOSTUFF R9629 0 — TD1P
TMDS_D0M — R9602 332 1% 1/16W MF-LF 402 — TD0M
TMDS_D0P — NOSTUFF R9630 0 — L9609 90-OHM — NOSTUFF R9631 0 — TD0P
TMDS_CKM — R9601 165 1% 1/16W MF-LF 402 — TCKM
TMDS_CK_TERM MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM — C9600 22PF 5% 50V CERM 402 — R9600 165 1% 1/16W MF-LF 402 — L9610 90-OHM — NOSTUFF R9632 0 — NOSTUFF R9633 0 — TCKP
TMDS_CKP

=PP3V3_GPU — R9605 2.0K 5% 1/16W MF-LF 402 — R9607 2.0K 5% 1/16W MF-LF 402 — R9682 0 5% 1/8W MF-LF 805 — PP3V3_DDC — C9601 0.01UF 10% 16V CERM 402

I2C_GPU_TMDS_SCL — R9608 33 5% 1/16W MF-LF 402 — I2C_TMDS_SCL

I2C_GPU_TMDS_SDA — R9606 33 5% 1/16W MF-LF 402 — I2C_TMDS_SDA

INTERNAL TMDS CONNECTOR

SDF9600 STDOFF-118OD-181H-TH — GND_CHASSIS_TMDS0 — C9620 0.01UF 10% 16V CERM 402

(516S0241) J9602 53307-3072 F-ST-SM

PPVCC_TMDS — PP3V3_DDC VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

TD0M, TD0P, TD2M, TD2P, I2C_TMDS_SDA — TCKM, TCKP, TD1M, TD1P, I2C_TMDS_SCL

C9616 10UF 10% 16V CERM 1210 — C9615 0.01UF 10% 16V CERM 402

SDF9601 STDOFF-118OD-181H-TH — GND_CHASSIS_TMDS1 — C9621 0.01UF 10% 16V CERM 402

PANEL POWER SEQUENCING

=PP3V3_GPU — NOSTUFF Q9600 IRF7410PBF SO-8 — =PP3V3_GPU — R9634 0 5% 1/8W MF-LF 805

NOSTUFF C9619 0.01UF 20% 16V CERM 402 — NOSTUFF R9625 100K 5% 1/16W MF-LF 402 — 376S0337 — NOSTUFF C9618 0.022UF 20% 16V CERM 402

PPVCC_TMDS VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

FPD_PWR_SW_G — R9613 10K 5% 1/16W MF-LF 402 — FPD_PWR_ON_D — NOSTUFF Q9601 2N7002 SOT23-LF — FPD_PWR_ON

D9614 MMBD914XXG SOT23 — C9617 10UF 20% 6.3V CERM 805 — NOSTUFF R9660 10K 5% 1/16W MF-LF 402

TMDS_EN_R — R9614 10K 5% 1/16W MF-LF 402 — TMDS_EN

U9670 74LCX125 — FPD_PWR_ON — LED5900_PWR — R9612 330 5% 1/10W MF-LF 603 — LED5900_P1 — LED9600 GREEN 2.0X1.25A

SILKSCREEN: 3

INVERTER INTERFACE

=PP12V_GPU — C9642 4.7UF 20% 6.3V CERM 805 — CRITICAL J9601 53261-0498 M-RT-SM

LCD_PWM, INV_CUR_HI

518S0193

EXTERNAL VGA CONNECTOR

NET_PHYSICAL_TYPE	NET_SPACING_TYPE
FILT_ANALOG_GRN	GPU_VGA
FILT_ANALOG_RED	GPU_VGA
FILT_ANALOG_BLU	GPU_VGA
VGA_VSYNC	GPU_VGA
VGA_VSYNC_R	GPU_VGA
VGA_HSYNC	GPU_VGA
VGA_HSYNC_R	GPU_VGA

PP5V_USB2 — R9680 0 5% 1/8W MF-LF 805 — PP5V_VGA VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM — C9602 0.01UF 10% 16V CERM 402 — GND_CHASSIS_VGA

=PP3V3_GPU — C9670 0.1UF 20% 10V CERM 402 — CRITICAL U9670 74LCX125 TSSOP

ANALOG_VSYNC — VGA_VSYNC — R9671 33 5% 1/16W MF-LF 402 — VGA_VSYNC_R

U9670 74LCX125 TSSOP

ANALOG_HSYNC — VGA_HSYNC — R9672 33 5% 1/16W MF-LF 402 — NOSTUFF C9607 22PF 5% 50V CERM 402 — NOSTUFF C9608 22PF 5% 50V CERM 402 — GND_CHASSIS_VGA

=PP3V3_GPU — R9673 10K 5% 1/16W MF-LF 402 — R9674 10K 5% 1/16W MF-LF 402

Q9675 2N7002DW-X-F SOT-363 — I2C_GPU_MON_SCL — I2C_MON_SCL — R9675 100 5% 1/16W MF-LF 402 — I2C_MON_SCL_R

Q9675 2N7002DW-X-F SOT-363 — I2C_GPU_MON_SDA — I2C_MON_SDA — R9676 100 5% 1/16W MF-LF 402 — I2C_MON_SDA_R

PP5V_VGA — R9677 4.7K 5% 1/16W MF-LF 402 — R9678 4.7K 5% 1/16W MF-LF 402

C9677 47PF 5% 50V CERM 402 — C9678 47PF 5% 50V CERM 402 — GND_CHASSIS_VGA

NOSTUFF FL9600 LCFILTER SM-220MHZ — ANALOG_RED — R9640 0 5% 1/8W MF-LF 402

NOSTUFF FL9601 LCFILTER SM-220MHZ — ANALOG_GRN — R9641 0 5% 1/8W MF-LF 402

NOSTUFF FL9602 LCFILTER SM-220MHZ — ANALOG_BLU — R9642 0 5% 1/8W MF-LF 402

PLACE R9321-3 & FL9600-2 CLOSE TO J9603

M23: 514S0089

CRITICAL J9603 MINI-VGA F-ST-SM

NC — PIN 15 NC REQUESTED BY EMC

VGA_HSYNC_R, FILT_ANALOG_RED, FILT_ANALOG_GRN, FILT_ANALOG_BLU, I2C_MON_SCL_R, MON_DETECT — VGA_VSYNC_R, (RED_RTN), (GRN_RTN), PP5V_VGA, I2C_MON_SDA_R, (BLU_RTN)

C9605 0.01UF 10% 16V CERM 402 — C9604 0.01UF 10% 16V CERM 402 — C9603 0.01UF 10% 16V CERM 402 — GND_CHASSIS_VGA

TMDS/Inverter/ExtVGA

SYNC_MASTER=M23-DD — SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	96	154

KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

KODIAK PCI-E CONST

SYNC_MASTER=FINO-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	97	154

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)

=PPVCORE_PWRON_NB_HT 7 98

C9806 1UF 10% 6.3V CERM 402
C9807 1UF 10% 6.3V CERM 402
C9808 1UF 10% 6.3V CERM 402
C9809 1UF 10% 6.3V CERM 402
C9810 1UF 10% 6.3V CERM 402
C9811 1UF 10% 6.3V CERM 402
C9812 1UF 10% 6.3V CERM 402
C9813 1UF 10% 6.3V CERM 402
C9814 1UF 10% 6.3V CERM 402
C9815 1UF 10% 6.3V CERM 402

PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT

98 7 =PPVCORE_PWRON_NB_HT — C9834 0.1UF 20% 10V CERM 402 — =PP1V2_PWRON_HT_NBTX 7 98

KODIAK CORES

PP9806 P4MM SM — 1.6V — Q63 = PP1V6

98 7 =PPVCORE_PWRON_NB_HT

98 7 =PP2V5_PWRON_NB_HT — L9800 0.22UH 0805-1 — PWR_HT_AVDD

C9800 0.01UF 10% 16V CERM 402
C9801 10UF 10% 6.3V X5R 805
C9802 1UF 10% 6.3V CERM 402

101 98 6 KOD_L15_GND (THIS PAGE)

PP9807 P4MM SM — 1.2V — Q63 = PP1V2

=PP1V2_PWRON_HT_NBTX 7 98

101 PWR_HT_AVDD2 — L9801 0.22UH 0805-1 — =PP2V5_PWRON_NB_HT 7 98

C9803 1UF 10% 6.3V CERM 402
C9804 10UF 10% 6.3V X5R 805
C9805 0.01UF 10% 16V CERM 402

KOD_L15_GND 6 98 101 (THIS PAGE)

98 7 =PP1V2_PWRON_HT_NBTX

C9817 1UF 10% 6.3V CERM 402
C9818 1UF 10% 6.3V CERM 402
C9819 1UF 10% 6.3V CERM 402
C9820 1UF 10% 6.3V CERM 402
C9821 1UF 10% 6.3V CERM 402
C9822 1UF 10% 6.3V CERM 402
C9823 1UF 10% 6.3V CERM 402
C9824 1UF 10% 6.3V CERM 402
C9825 1UF 10% 6.3V CERM 402
C9826 1UF 10% 6.3V CERM 402

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)

98 7 =PP1V2_PWRON_HT_NBTX

C9827 1UF 10% 6.3V CERM 402
C9828 1UF 10% 6.3V CERM 402
C9829 1UF 10% 6.3V CERM 402
C9830 1UF 10% 6.3V CERM 402
C9831 1UF 10% 6.3V CERM 402
C9832 1UF 10% 6.3V CERM 402
C9833 1UF 10% 6.3V CERM 402
C9839 1UF 10% 6.3V CERM 402
C9840 1UF 10% 6.3V CERM 402
C9841 1UF 10% 6.3V CERM 402
C9847 1UF 10% 6.3V CERM 402
C9842 1UF 10% 6.3V CERM 402
C9843 1UF 10% 6.3V CERM 402
C9844 1UF 10% 6.3V CERM 402
C9845 1UF 10% 6.3V CERM 402
C9846 1UF 10% 6.3V CERM 402

PP9808 P4MM SM — HTM2NC0- / HTM2NC0+ — PP9809 P4MM SM

98 7 =PP1V2_PWRON_HT_NBTX

101 HT_MB_TO_NB_CLK_N<0>
101 HT_MB_TO_NB_CLK_P<0>
101 HT_MB_TO_NB_CTL_N<0>
101 HT_MB_TO_NB_CTL_P<0>

PP9800 P4MM SM — MHT0- / MHT0+ — SM P4MM PP9801

KODIAK HT RECEIVE CLOCKS

PP9802 P4MM SM — MHT1- / MHT1+ — SM P4MM PP9803

R9806 8.2K 5% 1/16W MF-LF 402
R9807 8.2K 5% 1/16W MF-LF 402

101 HT_MB_TO_NB_CLK_N<1>
101 HT_MB_TO_NB_CLK_P<1>

9 HT_MB_TO_NB_CTL_N<1>
9 HT_MB_TO_NB_CTL_P<1>

KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

R9800 100 1% 1/16W MF-LF 402
R9801 200 1% 1/16W MF-LF 402

101 26 HT_NB_REFCLK_P<0>
101 26 HT_NB_REFCLK_N<0>

R9802 20.5 1% 1/16W MF-LF 402
R9803 29.4 1% 1/16W MF-LF 402
R9804 29.4 1% 1/16W MF-LF 402
R9805 20.5 1% 1/16W MF-LF 402

C9837 0.01UF 10% 16V CERM 402
C9838 0.01UF 10% 16V CERM 402
NOSTUFF C9836 0.01UF 10% 16V CERM 402

101 HT_NB_G

PP9804 P4MM SM — HREF0- / HREF0+ — SM P4MM PP9805

KODIAK HT REFCLK

HT_REFCLK_AVDD (1.65V-2.75V) (1.6V-1.2V)

K15

E25	HT_CLK_RXN0	HT_RX_VDD	A24
D25	HT_CLK_RXP0	HT_RX_VDD	B22
J27	HT_CTL_RXN0	HT_RX_VDD	B26
K27	HT_CTL_RXP0	HT_RX_VDD	D24
F26	HT_CAD_RXN0	HT_RX_VDD	E22
F27	HT_CAD_RXP0	HT_RX_VDD	E26
F25	HT_CAD_RXN1	HT_RX_VDD	G24
F24	HT_CAD_RXP1	HT_RX_VDD	H26
A25	HT_CAD_RXN2	HT_RX_VDD	K24
B25	HT_CAD_RXP2	HT_RX_VDD	L22
G25	HT_CAD_RXN3		
H25	HT_CAD_RXP3		
L25	HT_CAD_RXN4		
K25	HT_CAD_RXP4		
G27	HT_CAD_RXN5		
H27	HT_CAD_RXP5		
J25	HT_CAD_RXN6		
J26	HT_CAD_RXP6		
C26	HT_CAD_RXN7		
C27	HT_CAD_RXP7		
F22	HT_CLK_RXN1		
F23	HT_CLK_RXP1		
E21	HT_CTL_RXP1		
D21	HT_CTL_RXN1		
B23	HT_CAD_RXN8		
D23	HT_CAD_RXP8		
A23	HT_CAD_RXN9		
B23	HT_CAD_RXP9		
H23	HT_CAD_RXN10		
G23	HT_CAD_RXP10		
C22	HT_CAD_RXN11		
C23	HT_CAD_RXP11		
K23	HT_CAD_RXN12		
L23	HT_CAD_RXP12		
J23	HT_CAD_RXN13		
J24	HT_CAD_RXP13		
A21	HT_CAD_RXN14		
B21	HT_CAD_RXP14		
C24	HT_CAD_RXN15		
C25	HT_CAD_RXP15		
K19	HT_PVTREF0		
L19	HT_PVTREF1		
L17	HT_PVTREF2_ALT		
K17	HT_PVTREF3_ALT		
J16	HT_REFCLK_N		
J15	HT_REFCLK_P		

HT_KOD_PVTREF0
HT_KOD_PVTREF1
HT_KOD_PVTREF2_ALT
HT_KOD_PVTREF3_ALT

(200MHZ)

HT_REFCLK_AGND — L15 — KOD_L15_GND (THIS PAGE)

XW9800 SM

101 9 HT_NB_REFCLK_PF<0>
101 9 HT_NB_REFCLK_NF<0>

HT_REFCLK_AVDD2 (1.65V-2.75V) (1.6V-1.2V)

H15

A16	HT_VD4	HT_CLK_TXN0	J19
A20	HT_VD4	HT_CLK_TXP0	J20
B14	HT_VD4	HT_CTL_TXN0	J22
B18	HT_VD4	HT_CTL_TXP0	J21
D16	HT_VD4	HT_CAD_TXN0	F16
D20	HT_VD4	HT_CAD_TXP0	F17
E18	HT_VD4	HT_CAD_TXN1	G17
G16	HT_VD4	HT_CAD_TXP1	H17
G20	HT_VD4	HT_CAD_TXN2	J18
H18	HT_VD4	HT_CAD_TXP2	J17
H22	HT_VD4	HT_CAD_TXN3	F18
K16	HT_VD4	HT_CAD_TXP3	F19
K20	HT_VD4	HT_CAD_TXN4	G19
L18	HT_VD4	HT_CAD_TXP4	H19
M17	HT_VD4	HT_CAD_TXN5	G21
M21	HT_VD4	HT_CAD_TXP5	H21
N19	HT_VD4	HT_CAD_TXN6	F21
		HT_CAD_TXP6	F20
		HT_CAD_TXN7	K21
		HT_CAD_TXP7	L21
		HT_CLK_TXN1	C16
		HT_CLK_TXP1	C17
		HT_CTL_TXP1	E15
		HT_CTL_TXN1	D15
		HT_CAD_TXN8	D19
		HT_CAD_TXP8	E19
		HT_CAD_TXN9	D17
		HT_CAD_TXP9	E17
		HT_CAD_TXN10	C19
		HT_CAD_TXP10	C18
		HT_CAD_TXN11	A15
		HT_CAD_TXP11	B15
		HT_CAD_TXN12	A17
		HT_CAD_TXP12	B17
		HT_CAD_TXN13	B19
		HT_CAD_TXP13	A19
		HT_CAD_TXN14	C15
		HT_CAD_TXP14	C14
		HT_CAD_TXN15	C20
		HT_CAD_TXP15	C21
		HT_LDTSTOP_L	AP06
		HT_LDTREQ_L	AP09
		HT_PWROK	AP03
		HT_RESET_L	AE11

U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE

A14	HT_VD4_GND	HT_RX_GND	A22
A18	HT_VD4_GND	HT_RX_GND	A26
B16	HT_VD4_GND	HT_RX_GND	B24
B20	HT_VD4_GND	HT_RX_GND	D22
D18	HT_VD4_GND	HT_RX_GND	D26
E16	HT_VD4_GND	HT_RX_GND	E24
E20	HT_VD4_GND	HT_RX_GND	G26
G18	HT_VD4_GND	HT_RX_GND	H24
G22	HT_VD4_GND	HT_RX_GND	K22
H16	HT_VD4_GND	HT_RX_GND	L24
H20	HT_VD4_GND		
K18	HT_VD4_GND		
L16	HT_VD4_GND		
L20	HT_VD4_GND		
M16	HT_VD4_GND		
M20	HT_VD4_GND		
N18	HT_VD4_GND		

=PP1V2_PWRON_HT_NBTX 7 98

NOSTUFF R9808 8.2K 5% 1/16W MF-LF 402
NOSTUFF R9809 8.2K 5% 1/16W MF-LF 402

9 HT_NB_TO_MB_CTL_P<1>
9 HT_NB_TO_MB_CTL_N<1>

=PP2V5_PWRON_HT 7 103

R9810 1K 5% 1/16W MF-LF 402
R9811 1K 5% 1/16W MF-LF 402
R9812 1K 5% 1/16W MF-LF 402
R9813 1K 5% 1/16W MF-LF 402

HT_LDTSTOP_L 103
HT_LDTREQ_L 103
HT_PWROK 103
HT_LDTRESET_L 103

PAGE 98

KODIAK HT16

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 98 OF 154	

DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT_NB_TO_MB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CLK_P<0>	TRUE	H1_NB_TO_SB_CLK	H1_NB_TO_SB_PP	H1_CAD	H1_NB_TO_SB_CLK
HT_NB_TO_MB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<0>	TRUE	H1_NB_TO_SB_CAD0	H1_NB_TO_SB_PP	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<1>	TRUE	H1_NB_TO_SB_CAD1	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<2>	TRUE	H1_NB_TO_SB_CAD2	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<3>	TRUE	H1_NB_TO_SB_CAD3	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<4>	TRUE	H1_NB_TO_SB_CAD4	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<5>	TRUE	H1_NB_TO_SB_CAD5	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<6>	TRUE	H1_NB_TO_SB_CAD6	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<7>	TRUE	H1_NB_TO_SB_CAD7	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_P<0>	TRUE	H1_NB_TO_SB_CTL0	H1_NB_TO_SB	H1_CAD	H1_NB_TO_SB_CAD
HT_MB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CLK_P<0>	TRUE	H1_SB_TO_NB_CLK	H1_SB_TO_NB_PP	H1_CAD	H1_SB_TO_NB_CLK
HT_MB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<0>	TRUE	H1_SB_TO_NB_CAD0	H1_SB_TO_NB_PP	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<1>	TRUE	H1_SB_TO_NB_CAD1	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<2>	TRUE	H1_SB_TO_NB_CAD2	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<3>	TRUE	H1_SB_TO_NB_CAD3	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<4>	TRUE	H1_SB_TO_NB_CAD4	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<5>	TRUE	H1_SB_TO_NB_CAD5	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<6>	TRUE	H1_SB_TO_NB_CAD6	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<7>	TRUE	H1_SB_TO_NB_CAD7	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_P<0>	TRUE	H1_SB_TO_NB_CTL0	H1_SB_TO_NB	H1_CAD	H1_SB_TO_NB_CAD
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE				
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE				
TP_HT_MB_TO_NB_CLK_N<1>	TRUE				
TP_HT_MB_TO_NB_CLK_P<1>	TRUE				
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE				
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE				
NC_HT_NB_TO_MB_CLK_N<1>	TRUE				
NC_HT_NB_TO_MB_CLK_P<1>	TRUE				
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0		HT_CLK	HT_CLK
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0

HT ALIASES

FINO-EG 05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE NONE	SHT 101 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	
HT_CLK66M_SB	0.38mm SPACING	
	P3MM SPACING	

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.

HT_CLK66M_SB_C 103
HT_CLK66M_SB 26 103
HT_LDTRESET_L 98 103

103 7 =PP1V2_PWRON_SB_HT
RA300 3.3 5% 1/8W MF-LF 805
PP1V2_PWRON_HT_PLLDVDD VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CA300 10UF 10% 6.3V X5R 805
CA301 1uF 10% 6.3V CERM 402
RA310 3.3 5% 1/8W MF-LF 805
PP1V2_PWRON_HT_PLLAVDD VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CA310 10UF 10% 6.3V X5R 805
CA311 1uF 10% 6.3V CERM 402

=PP2V5_PWRON_HT 7 98
CA320 0.1uF 20% 16V CERM 402
=PP1V2_PWRON_SB_HT 7 103
CA302 10UF 10% 6.3V X5R 805
CA330 0.1uF 20% 10V CERM 402
CA331 0.1uF 20% 10V CERM 402
CA332 0.1uF 20% 10V CERM 402
=PP1V2_PWRON_SB_HT 7 103
CA309 10UF 10% 6.3V X5R 805
CA340 0.1uF 20% 10V CERM 402
CA341 0.1uF 20% 10V CERM 402
CA342 0.1uF 20% 10V CERM 402

HTS2MC0+ PPA300 P4MM SM
HTS2MC0- PPA301 P4MM SM
HTS2MC0+ PPA303 P4MM SM
HTS2MC0- PPA304 P4MM SM

U2300 SHASTA V1.1 BGA-LF SEE_TABLE
HYPERTRANSPORT
AVDD DVDD VDDP HT_RXVDD HT_TXVDD HT_PLL HT

101	HT_MB_TO_SB_CLK_P<0>	D15	HT_CLKIN_P	B10	HT_CLKOUT_P
101	HT_MB_TO_SB_CLK_N<0>	C15	HT_CLKIN_N	A10	HT_CLKOUT_N
101	HT_MB_TO_SB_CAD_P<0>	D17	HT_CADIN_0_P	D10	HT_CADOUT_0_P
101	HT_MB_TO_SB_CAD_N<0>	C17	HT_CADIN_0_N	C10	HT_CADOUT_0_N
101	HT_MB_TO_SB_CAD_P<1>	B18	HT_CADIN_1_P	B8	HT_CADOUT_1_P
101	HT_MB_TO_SB_CAD_N<1>	A18	HT_CADIN_1_N	A8	HT_CADOUT_1_N
101	HT_MB_TO_SB_CAD_P<2>	F15	HT_CADIN_2_P	E11	HT_CADOUT_2_P
101	HT_MB_TO_SB_CAD_N<2>	E15	HT_CADIN_2_N	F11	HT_CADOUT_2_N
101	HT_MB_TO_SB_CAD_P<3>	D16	HT_CADIN_3_P	D11	HT_CADOUT_3_P
101	HT_MB_TO_SB_CAD_N<3>	C16	HT_CADIN_3_N	C11	HT_CADOUT_3_N
101	HT_MB_TO_SB_CAD_P<4>	B16	HT_CADIN_4_P	A11	HT_CADOUT_4_P
101	HT_MB_TO_SB_CAD_N<4>	A16	HT_CADIN_4_N	B11	HT_CADOUT_4_N
101	HT_MB_TO_SB_CAD_P<5>	D14	HT_CADIN_5_P	C12	HT_CADOUT_5_P
101	HT_MB_TO_SB_CAD_N<5>	C14	HT_CADIN_5_N	D12	HT_CADOUT_5_N
101	HT_MB_TO_SB_CAD_P<6>	E14	HT_CADIN_6_P	E12	HT_CADOUT_6_P
101	HT_MB_TO_SB_CAD_N<6>	F14	HT_CADIN_6_N	F12	HT_CADOUT_6_N
101	HT_MB_TO_SB_CAD_P<7>	B14	HT_CADIN_7_P	A13	HT_CADOUT_7_P
101	HT_MB_TO_SB_CAD_N<7>	A14	HT_CADIN_7_N	B13	HT_CADOUT_7_N
101	HT_MB_TO_SB_CTL_P<0>	F13	HT_CTLIN_P	C13	HT_CTLOUT_P
101	HT_MB_TO_SB_CTL_N<0>	E13	HT_CTLIN_N	D13	HT_CTLOUT_N
98	HT_PWROK	E16	HT_PWROK_H		
103 98	HT_LDTRESET_L	C18	HT_RESET_L		
98	HT_LDTSTOP_L	E17	HT_LDTSTOP_L		
103	HT_CLK66M_SB_C	C8	HT_REFCLK		
	SB_HT_S100M66M	D8	HT_S100M66M		
	SB_SELHT100	V6	SEL_HT00_H		
				A19	HT_LDTREQ_L
				E10	HT_R100P
				F10	HT_R100N

HT_PLL AGND DGND HT_RXGND HT_TXGND

HT_LDTREQ_L HT_LDTREQ_SB_L
RA301 0 5% 1/16W MF-LF 402
HT_LDTREQ_L 98
SB_HT_R100_P
SB_HT_R100_N
RA350 82.5 1% 1/16W MF-LF 402
CA350 47pF 5% 50V CERM 402
CA351 47pF 5% 50V CERM 402

P4MM SM PPA302
RA355 0 5% 1/16W MF-LF 402
103 26 HT_CLK66M_SB
1.0V pk-pk
103 7 =PP1V2_PWRON_SB_HT
NOSTUFF RA352 4.7K 1% 1/16W MF-LF 402
NOSTUFF RA354 10K 5% 1/16W MF-LF 402
1 = 100MHz
1 = 100MHz
RA353 4.7K 1% 1/16W MF-LF 402
RA351 1K 1% 1/16W MF-LF 402
0 = 66MHz
0 = 200MHz

HT RefClk	HT I/F Speed	
1 = 100MHz	1 = 100MHz	DETERMINES THE OPERATING FREQUENCY OF HT CORE
0 = 66MHz	0 = 200MHz	1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
		0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 103 OF 154	

LAST_MODIFIED=Thu May 19 14:08:29 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
		PCI_AD<31..28> 120 121 122 125
		PCI_AD<27> 120 121 122 125
		PCI_AD<26..24> 120 121 122 125
		PCI_AD<23> 120 121 122
		PCI_AD<22> 120 121 122
		PCI_AD<21> 120 121 122
		PCI_AD<20> 120 121 122 125
		PCI_AD<19..18> 120 121 122 125
		PCI_AD<17> 120 121 122 125
		PCI_AD<16..0> 120 121 122 125
		PCI_CBE_L<3..0> 120 121 122
		PCI_PAR 120 121 122
		PCI_DEVSEL_L 119 120 121 122
		PCI_FRAME_L 119 120 121 122
		PCI_IRDY_L 119 120 121 122
		PCI_TRDY_L 119 120 121 122
		PCI_STOP_L 119 120 121 122
183	P3MM_SPACING	PCI_CLK66M_SB_INT 26 27 119

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

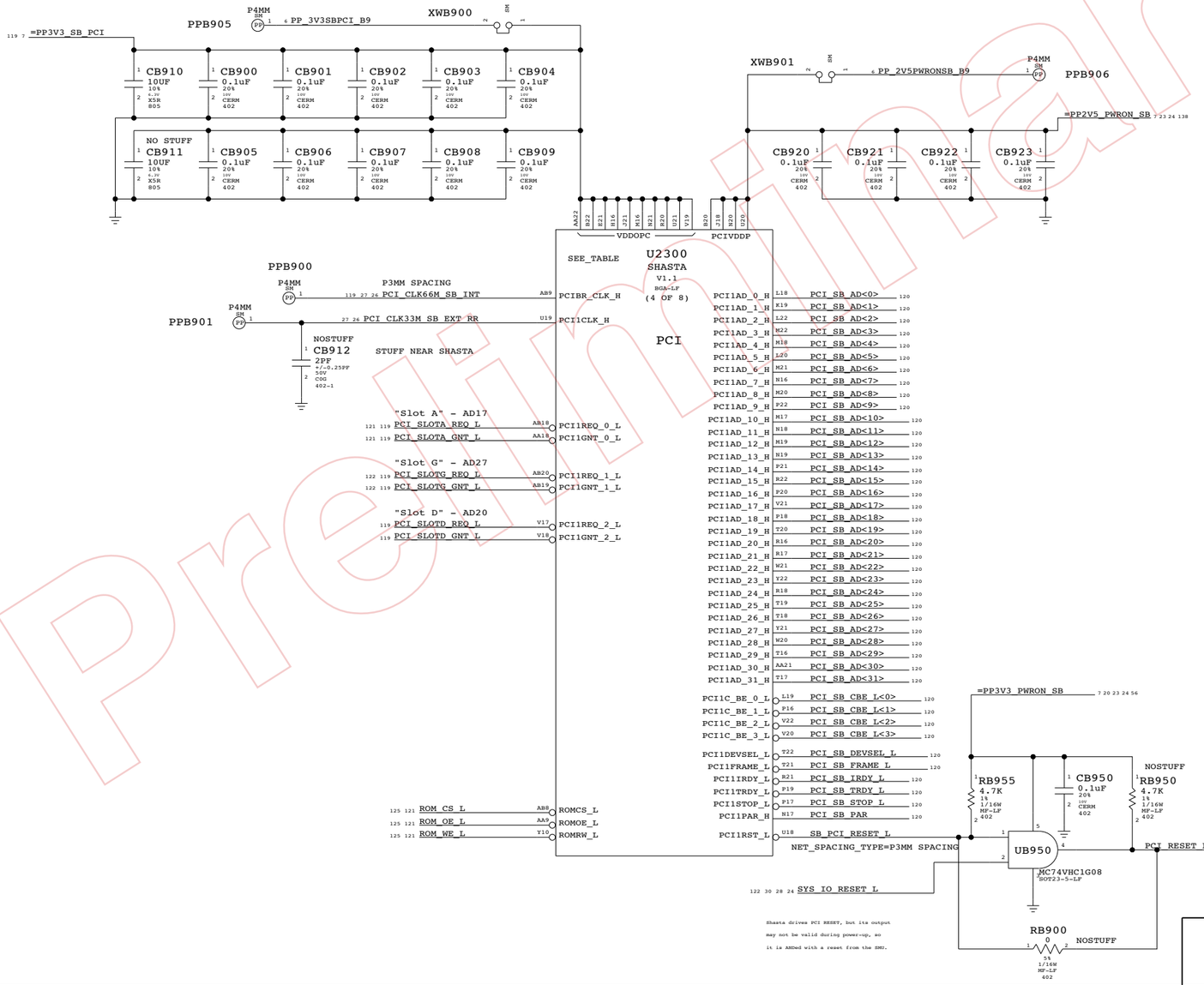
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN



Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 119 OF 154	

LAST_MODIFIED=Thu May 19 14:08:34 2005

DRAWING

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119 121 122 125
119	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119 121 122 125

RC000

119	PCI_SB_AD<17>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<17>	119 121 122 125

119	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119 121 122
119	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119 121 122
119	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119 121 122 125

RC001

119	PCI_SB_AD<27>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<27>	119 121 122 125

119	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-EG SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT OF
NONE	120 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

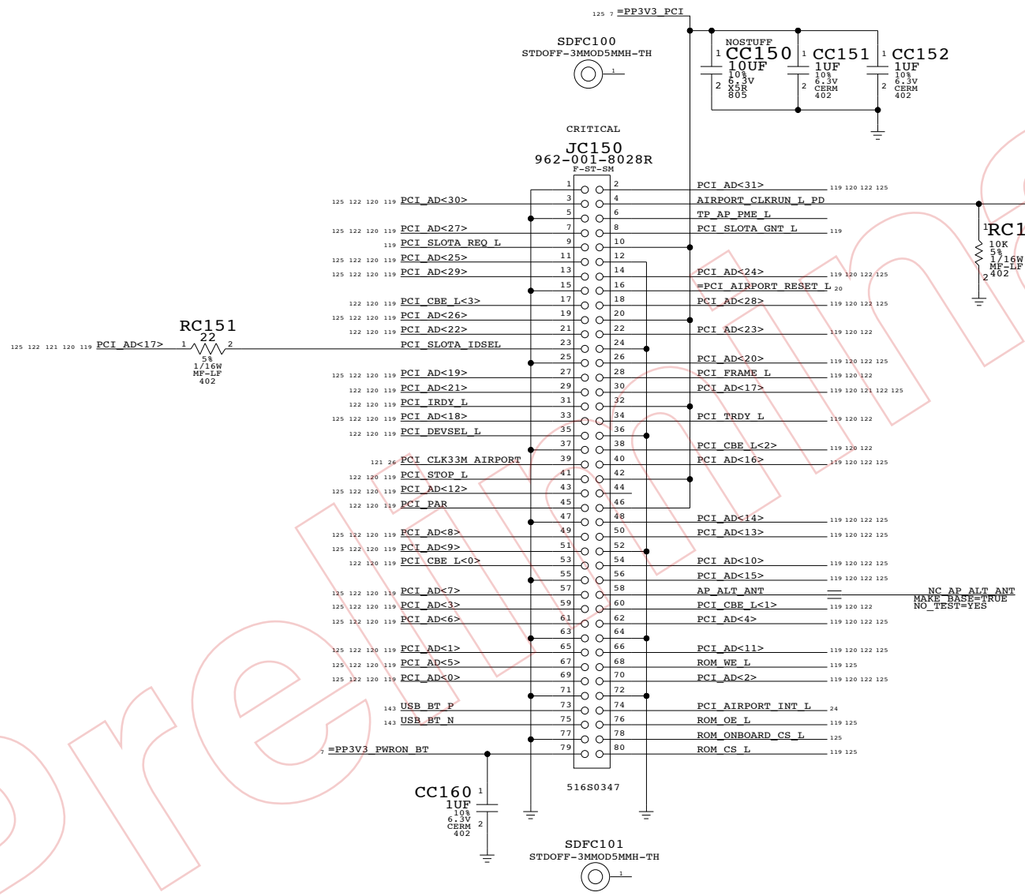
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-EG SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	121	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 27 122

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122 7 =PPVIO_PCI_USB2

CC201 0.1uF 20% 10V CERM 402
CC202 0.1uF 20% 10V CERM 402
CC203 0.1uF 20% 10V CERM 402

XWC200 SM 2 1 6 PP_VIOPCIUSB2_C2

P4MM SM 1 PP PPC203

VDD_PCI

UC200
NEC_UPD720101_USB2
FBGA-LF

125 121 120 119 PCI_AD<0>	M5	AD0	
125 121 120 119 PCI_AD<1>	P5	AD1	
125 121 120 119 PCI_AD<2>	N5	AD2	
125 121 120 119 PCI_AD<3>	P4	AD3	
125 121 120 119 PCI_AD<4>	N4	AD4	
125 121 120 119 PCI_AD<5>	M1	AD5	
125 121 120 119 PCI_AD<6>	N1	AD6	
125 121 120 119 PCI_AD<7>	M3	AD7	
125 121 120 119 PCI_AD<8>	L2	AD8	
125 121 120 119 PCI_AD<9>	L1	AD9	
125 121 120 119 PCI_AD<10>	K2	AD10	
125 121 120 119 PCI_AD<11>	L3	AD11	
125 121 120 119 PCI_AD<12>	K1	AD12	
125 121 120 119 PCI_AD<13>	K3	AD13	
125 121 120 119 PCI_AD<14>	J2	AD14	
125 121 120 119 PCI_AD<15>	J1	AD15	
125 121 120 119 PCI_AD<16>	F2	AD16	
125 121 120 119 PCI_AD<17>	E1	AD17	
125 121 120 119 PCI_AD<18>	E2	AD18	
125 121 120 119 PCI_AD<19>	D1	AD19	
125 121 120 119 PCI_AD<20>	D2	AD20	
121 120 119 PCI_AD<21>	D3	AD21	
121 120 119 PCI_AD<22>	C1	AD22	
121 120 119 PCI_AD<23>	C2	AD23	
125 121 120 119 PCI_AD<24>	B1	AD24	
125 121 120 119 PCI_AD<25>	A2	AD25	
125 121 120 119 PCI_AD<26>	B2	AD26	
125 121 120 119 PCI_AD<27>	C4	AD27	
125 121 120 119 PCI_AD<28>	A3	AD28	
125 121 120 119 PCI_AD<29>	C5	AD29	
125 121 120 119 PCI_AD<30>	B4	AD30	
125 121 120 119 PCI_AD<31>	A4	AD31	
121 120 119 PCI_CBE_L<0>	M2	CBE0	
121 120 119 PCI_CBE_L<1>	J3	CBE1	
121 120 119 PCI_CBE_L<2>	F1	CBE2	
121 120 119 PCI_CBE_L<3>	C3	CBE3	
121 120 119 PCI_PAR	J4	PAR	
121 120 119 PCI_FRAME_L	F3	FRAME	
121 120 119 PCI_IRDY_L	F4	IRDY	
121 120 119 PCI_TRDY_L	G1	TRDY	
121 120 119 PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B3	IDSEL	
121 120 119 PCI_DEVSEL_L	G2	DEVSEL	
119 PCI_SLOTG_REQ_L	C6	REQ	
119 PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR (OD)	
NEC_INTA_L	C7	INTA (OD)	
NEC_INTB_L	B7	INTB (OD)	
NEC_INTC_L	A7	INTC (OD)	
122 27 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST (CHIP RESET)	
NEC_CRUN_L_PD	M6	CRUN	
NEC_PME_L	D5	PME (OD)	
	C5	VCCRST (PCI RESET)	
6 TP_NEC_SMI_L	L6	SMI (OD)	
NEC_LEGC_PD	L7	LEGC	

IPD	NTEST1	M8	TP_NEC_NTEST1 6
IPD	SMC	M7	TP_NEC_SMC 6
IPD	TEB	N7	TP_NEC_TEB
IPD	AMC	P7	TP_NEC_AMC
IPD	TEST	L8	TP_NEC_TEST 6
	NANDTEST	M10	TP_NEC_NANDTEST
	SRCLK	M9	TP_NEC_SRCLK 6
	SRDTA	N9	TP_NEC_SRDATA
IPD	SRMOD	P9	TP_NEC_SRMOD 6

ALL NETS TO FUNCTIONAL TEST PAGE

RC214 22 5% 1/16W MF-LF 402

122 7 =PPVIO_PCI_USB2

RC216 10K 5% 1/16W MF-LF 402
RC213 10K 5% 1/16W MF-LF 402

24 PCI_USB2_INT_L
RPC203 47 5% 1/16W SM-LF
RPC203 47 5% 1/16W SM-LF
RPC203 47 5% 1/16W SM-LF

119 30 28 24 SYS_IO_RESET_L
RC250 47 5% 1/16W MF-LF 402

28 24 SYS_PME_L
RC251 47 5% 1/16W MF-LF 402

20 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

RC215 4.7K 1% 1/16W MF-LF 402
RPC203 47 5% 1/16W SM-LF

PPC200 P4MM SM PP 1
PPC201 P4MM SM PP 1

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 122 OF 154	

LAST_MODIFIED=Thu May 19 14:08:36 2005

DRAWING

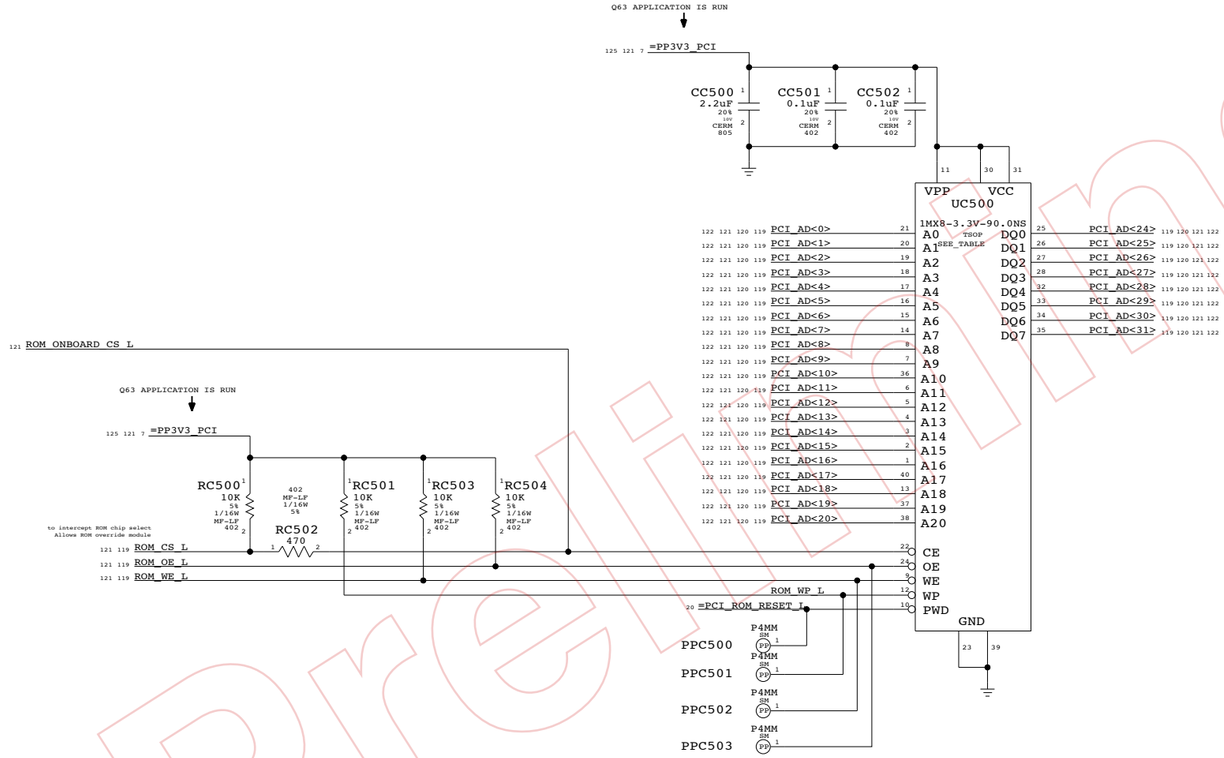
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	125	154

LAST_MODIFIED=Thu May 19 14:08:37 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C 127 129
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C 127 129
	SATA	SATA	SATA_TXD1	SATA_TXD_P1 127 129
	SATA	SATA	SATA_TXD1	SATA_TXD_N1 127 129
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C 127 129
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C 127 129
	SATA	SATA	SATA_TXD2	SATA_TXD_P2 127 129
	SATA	SATA	SATA_TXD2	SATA_TXD_N2 127 129
				UATA_DD<15..8> 9 127 129
				UATA_DD<7> 127 129
				UATA_DD<6..0> 9 127 129
				UATA_DA<2..0> 9 127 129
				UATA_CS0_L 127 129
				UATA_CS1_L 127 129
				UATA_HSTROBE 127 129
				UATA_STOP 127 129
				UATA_DMACK_L 127 129
	UATA_NETSPA			UATA_RESET_L 127 129
				UATA_DSTROBE 127 129
				UATA_DMARQ 127 129
				UATA_INTRQ 127 129
				UATA_DD_R<15..8> 127 129
				UATA_DD_R<7> 127 129
				UATA_DD_R<6..0> 127 129
				UATA_DA_R<2..0> 127 129
				UATA_CS0_L_R 127 129
				UATA_CS1_L_R 127 129
				UATA_DMACK_L_R 127 129
				UATA_HSTROBE_R 127 129
				UATA_STOP_R 127 129
				UATA_RESET_L_R 127 129

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A 0805 → PP1V2_SATA_VDD

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM

CC705 2.2UF 20% 6.3V CERM1 603
CC700 0.1UF 20% 10V CERM 402
CC701 0.1UF 20% 10V CERM 402
CC702 0.1UF 20% 10V CERM 402
CC703 0.1UF 20% 10V CERM 402
CC704 0.1UF 20% 10V CERM 402

SATA_VDD x 5

XWCC00 → PP_1V2PWRONDISKSB_CC NO_TEST=YES → P4MM SM PP → PPCC00

SATA_VDD (AB14, AB17, T14, W15, Y18)

U2300 SHASTA V1.1 BGA-LF (5 OF 8) SEE_TABLE

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>	127 129
UD_IDEDD_1_H	H7	UATA_DD_R<1>	127 129
UD_IDEDD_2_H	H6	UATA_DD_R<2>	127 129
UD_IDEDD_3_H	K2	UATA_DD_R<3>	127 129
UD_IDEDD_4_H	C1	UATA_DD_R<4>	127 129
UD_IDEDD_5_H	C2	UATA_DD_R<5>	127 129
UD_IDEDD_6_H	K3	UATA_DD_R<6>	127 129
UD_IDEDD_7_H	G6	UATA_DD_R<7>	127 129
UD_IDEDD_8_H	G5	UATA_DD_R<8>	127 129
UD_IDEDD_9_H	D4	UATA_DD_R<9>	127 129
UD_IDEDD_10_H	G7	UATA_DD_R<10>	127 129
UD_IDEDD_11_H	F6	UATA_DD_R<11>	127 129
UD_IDEDD_12_H	C3	UATA_DD_R<12>	127 129
UD_IDEDD_13_H	F5	UATA_DD_R<13>	127 129
UD_IDEDD_14_H	E5	UATA_DD_R<14>	127 129
UD_IDEDD_15_H	D5	UATA_DD_R<15>	127 129
UD_IDEDA0_H	E6	UATA_DA_R<0>	127 129
UD_IDEDA1_H	C4	UATA_DA_R<1>	127 129
UD_IDEDA2_H	D6	UATA_DA_R<2>	127 129
UD_IDECS1FX_L	B3	UATA_CS0_L_R	127 129
UD_IDECS3FX_L	B4	UATA_CS1_L_R	127 129
UD_IDEDMACK_L	E8	UATA_DMACK_L_R	127 129
UD_IDERD_L	E4	UATA_HSTROBE_R	127 129
UD_IDEWR_L	D3	UATA_STOP_R	127 129
UD_IDERST_L	E7	UATA_RESET_L_R	127 129

DSTROBE aka: IORDY/HDMARDY*
HSTROBE aka: DIOR*
STOP aka: DIOW*

129 127 UATA_DSTROBE	F9	UD_IDECHRDY_H	
129 127 UATA_DMARQ	D7	UD_IDEDMARQ_H	
129 127 UATA_INTRQ	C5	UD_IDEINTRQ_H	

SATA 0

129 127 SATA_RXD_P1_C	Y17	RXDP1	TXDP1 AA16 SATA_TXD_P1 127 129
129 127 SATA_RXD_N1_C	Y16	RXDN1	TXDN1 AB16 SATA_TXD_N1 127 129

SATA 1

129 127 SATA_RXD_P2_C	AB15	RXDP2	TXDP2 Y15 SATA_TXD_P2 127 129
129 127 SATA_RXD_N2_C	AA15	RXDN2	TXDN2 Y14 SATA_TXD_N2 127 129

SATA_GND (AA14, AA17, T13, W20)

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

P4MM SM PP → PPCC01

PLACE TERMINATION RESISTORS AT UATA CONNECTOR JC901

DIOR- :HDMARDY- :HSTROBE >
DIOW- :STOP >

RC706 33 5% 1/16W MF-LF 402
RC704 22 5% 1/16W MF-LF 402
RC702 22 5% 1/16W MF-LF 402
RC703 22 5% 1/16W MF-LF 402
RC700 33 5% 1/16W MF-LF 402
RC701 33 5% 1/16W MF-LF 402

129 127 UATA_RESET_L_R	RC706	UATA_RESET_L 127 129
129 127 UATA_DMACK_L_R	RC704	UATA_DMACK_L 127 129
129 127 UATA_HSTROBE_R	RC702	UATA_HSTROBE 127 129
129 127 UATA_STOP_R	RC703	UATA_STOP 127 129
129 127 UATA_CS0_L_R	RC700	UATA_CS0_L 127 129
129 127 UATA_CS1_L_R	RC701	UATA_CS1_L 127 129

SPARE
RPC704 33 5% 1/16W SM-LF

RPC704 33 5% 1/16W SM-LF
RPC700 33 5% 1/16W SM-LF
RPC703 33 5% 1/16W SM-LF
RPC702 33 5% 1/16W SM-LF
RPC701 33 5% 1/16W SM-LF

129 127 UATA_DA_R<0>	RPC704	UATA_DA<0> 9 127 129
129 127 UATA_DA_R<1>	RPC704	UATA_DA<1> 127 129
129 127 UATA_DA_R<2>	RPC704	UATA_DA<2> 127 129
129 127 UATA_DD_R<0>	RPC700	UATA_DD<0> 127 129
129 127 UATA_DD_R<1>	RPC700	UATA_DD<1> 9 127 129
129 127 UATA_DD_R<2>	RPC700	UATA_DD<2> 127 129
129 127 UATA_DD_R<3>	RPC703	UATA_DD<3> 127 129
129 127 UATA_DD_R<4>	RPC701	UATA_DD<4> 127 129
129 127 UATA_DD_R<5>	RPC701	UATA_DD<5> 127 129
129 127 UATA_DD_R<6>	RPC703	UATA_DD<6> 127 129
129 127 UATA_DD_R<7>	RPC702	UATA_DD<7> 127 129
129 127 UATA_DD_R<8>	RPC702	UATA_DD<8> 127 129
129 127 UATA_DD_R<9>	RPC703	UATA_DD<9> 127 129
129 127 UATA_DD_R<10>	RPC700	UATA_DD<10> 127 129
129 127 UATA_DD_R<11>	RPC702	UATA_DD<11> 127 129
129 127 UATA_DD_R<12>	RPC701	UATA_DD<12> 127 129
129 127 UATA_DD_R<13>	RPC702	UATA_DD<13> 127 129
129 127 UATA_DD_R<14>	RPC701	UATA_DD<14> 9 127 129
129 127 UATA_DD_R<15>	RPC703	UATA_DD<15> 127 129

RC705 10K 5% 1/16W MF-LF 402

Shasta Disk

SYNC_MASTER=M23-MB SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

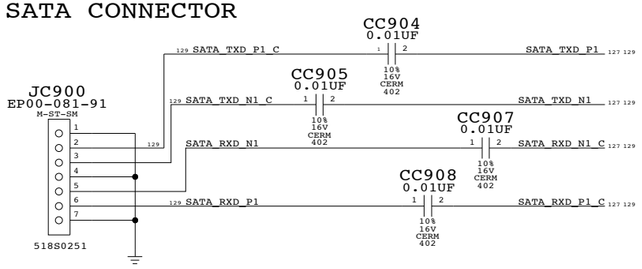
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 127 OF 154	

LAST_MODIFIED=Thu May 19 14:08:37 2005
DRAWING

SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

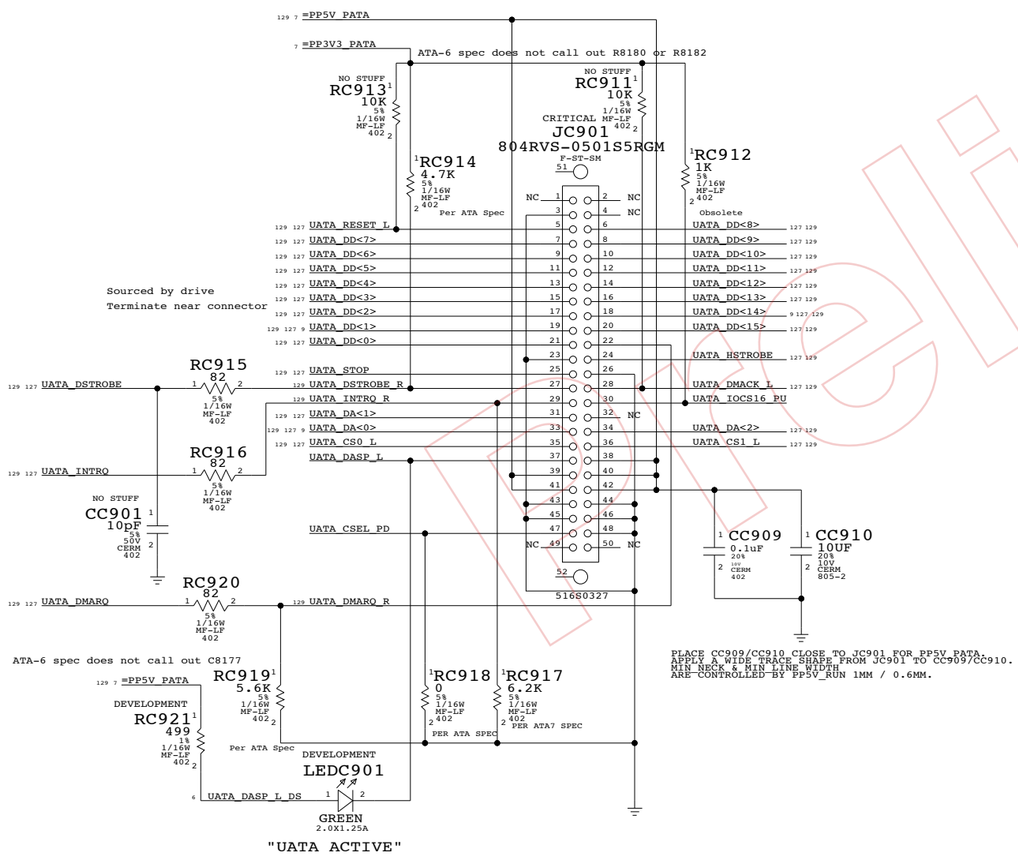
SATA_TXD_P2	NC_SATA_TXD_P2	MAKE_BASE=TRUE
SATA_TXD_N2	NC_SATA_TXD_N2	MAKE_BASE=TRUE
SATA_RXD_N2_C	NC_SATA_RXD_N2_C	MAKE_BASE=TRUE
SATA_RXD_P2_C	NC_SATA_RXD_P2_C	MAKE_BASE=TRUE

SATA DIFF PAIR GND VIAS

GV901 HOLE-VIA-P5RP25
GV902 HOLE-VIA-P5RP25
GV903 HOLE-VIA-P5RP25
GV904 HOLE-VIA-P5RP25
GV905 HOLE-VIA-P5RP25
GV906 HOLE-VIA-P5RP25
GV907 HOLE-VIA-P5RP25
GV908 HOLE-VIA-P5RP25

4-12-05
ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA NO CLOSER THAN 0.152MM TO SIGNAL VIA.

PATA CONNECTOR



PLACE CC909/CC910 CLOSE TO JC901 FOR PP5V_PATA.
APPLY A WIDE TRACE SHAPE FROM JC901 TO CC909/CC910.
MIN NECK & MIN LINE WIDTH
ARE CONTROLLED BY PP5V_RUN 1MM / 0.6MM.

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM RPAKS TO JC901

UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA		RP92
UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA		RP91
UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA		RP94
UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA		RP93
UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA		RP96
UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA		RP97
UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA		RP98
UATA_STOP_R		UATA_NETPH	UATA_NETSPA		RP99
UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA		RP100
UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA		RP101
UATA_DSTROBE		UATA_NETPH	UATA_NETSPA		RP102
UATA_DMARQ		UATA_NETPH	UATA_NETSPA		RP103
UATA_INTRQ		UATA_NETPH	UATA_NETSPA		RP104

UATA FROM SHASTA U2300 TO RPAKS

SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M23-MB SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 129 OF 154	

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE: NONE SHT 130 OF 154

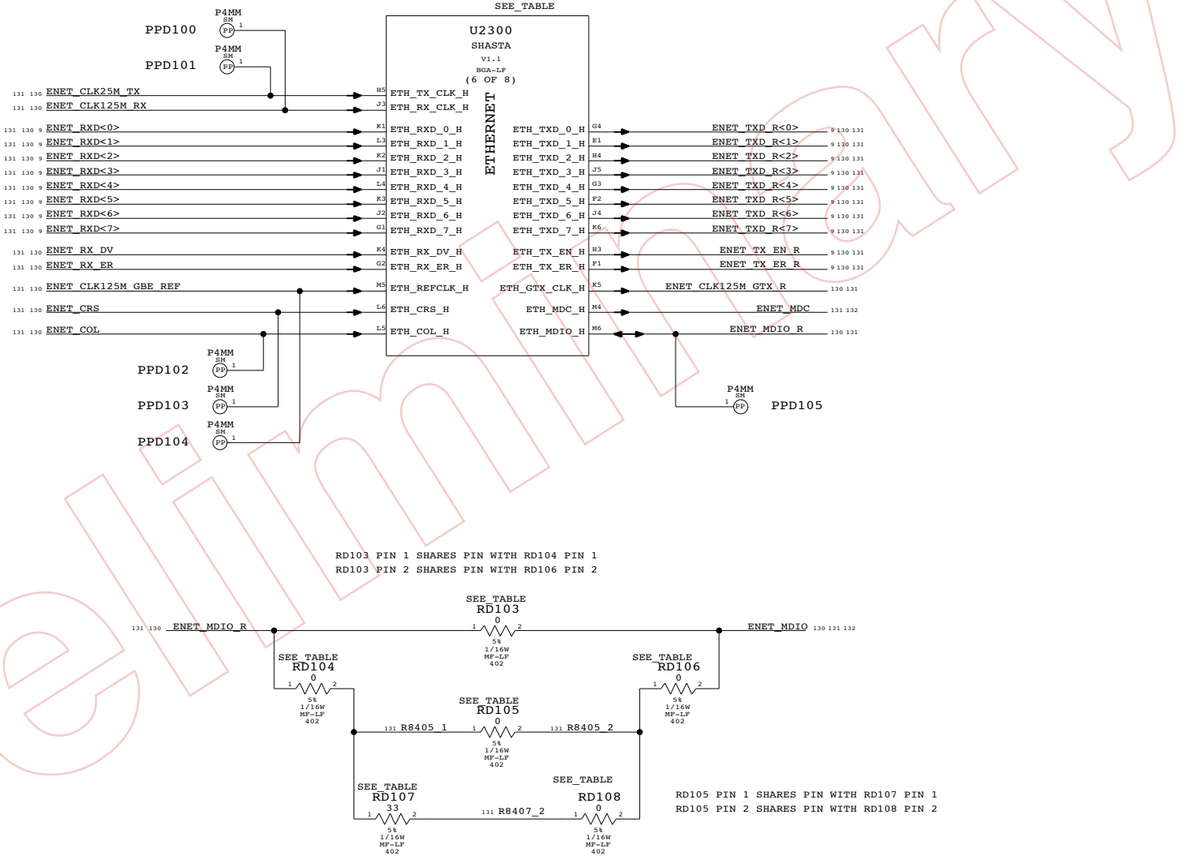
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I47	0.38mm SPACING		ENET_CLK25M_TX 130 131
I46	0.38mm SPACING		ENET_CLK125M_RX 130 131
I49	0.38mm SPACING		ENET_CLK125M_GBE_REF 130 131
I22	0.38mm SPACING		ENET_CLK125M_GTX 130 132
I50	0.38mm SPACING		ENET_CLK125M_GTX_R 130 131
I51	ENET_FW_2X		ENET_RXD_R<7..0> 9 130 132
I52	ENET_FW_3X		ENET_RX_DV_R 130 132
I53	ENET_FW_3X		ENET_RX_ER_R 130 132
I54	ENET_FW_2X		ENET_RXD<7..0> 9 130 131
I55	ENET_FW_3X		ENET_RX_DV 130 131
I56	ENET_FW_3X		ENET_RX_ER 130 131
I58	ENET_FW_2X		ENET_TXD_R<7..0> 9 130 131
I57	ENET_FW_3X		ENET_TX_EN_R 9 130 131
I59	ENET_FW_3X		ENET_TX_ER_R 9 130 131
I60	ENET_FW_2X		ENET_TXD<7..0> 9 130 132
I61	ENET_FW_3X		ENET_TX_EN 9 130 132
I62	ENET_FW_3X		ENET_TX_ER 9 130 132
I63	ENET_FW_3X		ENET_CRS_R 130 132
I64	ENET_FW_3X		ENET_COL_R 130 132
I65	ENET_FW_3X		ENET_CRS 130 131
I66	ENET_FW_3X		ENET_COL 130 131
I40	ENET_FW_3X		ENET_MDC 131 132
I41	ENET_FW_3X		ENET_MDIO 130 131 132
I42	ENET_FW_3X		ENET_MDIO_R 130 131
I43	ENET_FW_3X		R8405_1 131
I45	ENET_FW_3X		R8405_2 131
I44	ENET_FW_3X		R8407_2 131

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2

RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 131 OF 154	

LAST_MODIFIED=Thu May 19 12:15:17 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
115	0.38mm_SPACING		ENET_CLK125M_GBE_REF_R 130 132
122	0.38mm_SPACING		ENET_CLK125M_RX_R 130 132
124	0.38mm_SPACING		ENET_CLK25M_TX_R 130 132
110	ENET	ENET_MDI0	ENET_MDI_P<0> 132 136
111	ENET	ENET_MDI0	ENET_MDI_N<0> 132 136
113	ENET	ENET_MDI1	ENET_MDI_P<1> 132 136
114	ENET	ENET_MDI1	ENET_MDI_N<1> 132 136
117	ENET	ENET_MDI2	ENET_MDI_P<2> 132 136
118	ENET	ENET_MDI2	ENET_MDI_N<2> 132 136
120	ENET	ENET_MDI3	ENET_MDI_P<3> 132 136
121	ENET	ENET_MDI3	ENET_MDI_N<3> 132 136
85	0.38mm_SPACING		VESTA_CLK25M_XTALI 132
84	0.38mm_SPACING		VESTA_CLK25M_XTALO 132
86	0.38mm_SPACING		VESTA_CLK25M_XTALO_R 132

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL
139 17 7 =PP2V5_ENETFW
LD200 FERR-EMI-600-OHM SM
PP2V5_VESTA_BIASVDD1 6 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD201 0.1uF 20% 10V CERM 402
LD201 FERR-EMI-600-OHM SM
PP2V5_VESTA_XTALVDD1 6 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD202 10UF 10% 6.3V X5R 805
CD203 0.001uF 20% 50V CERM 402
XWD200 SM OMIT TP_VESTA_BIASVDD1 P4MM SM PPD239
XWD201 SM OMIT TP_VESTA_XTALVDD1 P4MM SM PPD201
XWD202 SM OMIT TP_VESTA_PLLVDD1 P4MM SM PPD238
PP1V2_VESTA_PLLVDD1 6 VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD204 0.001uF 20% 50V CERM 402
CD205 10UF 10% 6.3V X5R 805
LD202 FERR-EMI-600-OHM SM
Q63 APPLICATION IS ALL
=PP1V2_ENETFW 7 17 139
VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms
P4MM SM PPD200
131 130 ENET_CLK125M_GTX

XTALVDD1 BIASVDD1 PLLVDD1

VESTA ENET
U1701
VESTA-V1.3
FBGA-200-LF
2 OF 3

GTXCLK	A4	IPD	CLK125	D1	ENET_CLK125M_GBE_REF_R 130 132
			TXC	A6	ENET_CLK25M_TX_R 130 132
			RXC	C1	ENET_CLK125M_RX_R 130 132
TXD[0]	B6	IPD	RXD[0]	F4	ENET_RXD_R<0> 9 130 131
TXD[1]	C6	IPD	RXD[1]	F5	ENET_RXD_R<1> 9 130 131
TXD[2]	C7	IPD	RXD[2]	E5	ENET_RXD_R<2> 9 130 131
TXD[3]	D6	IPD	RXD[3]	E4	ENET_RXD_R<3> 9 130 131
TXD[4]	E6	IPD	RXD[4]	E3	ENET_RXD_R<4> 9 130 131
TXD[5]	C5	IPD	RXD[5]	D5	ENET_RXD_R<5> 9 130 131
TXD[6]	B5	IPD	RXD[6]	D4	ENET_RXD_R<6> 9 130 131
TXD[7]	A5	IPD	RXD[7]	D3	ENET_RXD_R<7> 9 130 131
TX_EN	B4	IPD	RX_DV	D2	ENET_RX_DV_R 130 131
TX_ER	C4	IPD	RX_ER	C2	ENET_RX_ER_R 130 131
MDC	G1	IPD	COL	F3	ENET_COL_R 130 131
MDIO	G2	IPU	CRS	G3	ENET_CRS_R 130 131
LOWPWR	H5	IPD	RBC0	A3	TP_VESTA_RBC0 9
			RBC1	B3	TP_VESTA_RBC1 9
PHYA[0]	L5	IPD	TRD+[0]	R4	ENET_MDI_P<0> 132 136
PHYA[1]	L4	IPD	TRD-[0]	R5	ENET_MDI_N<0> 132 136
PHYA[2]	L3	IPD	TRD+[1]	R7	ENET_MDI_P<1> 132 136
PHYA[3]	L2	IPD	TRD-[1]	R6	ENET_MDI_N<1> 132 136
PHYA[4]	L1	IPD	TRD+[2]	R8	ENET_MDI_P<2> 132 136
			TRD-[2]	R9	ENET_MDI_N<2> 132 136
EN_10B	K3	IPD	TRD+[3]	R11	ENET_MDI_P<3> 132 136
RGMIIEN	B8	IPD	TRD-[3]	R10	ENET_MDI_N<3> 132 136
FDX	C8	IPU	INTR*/ENERGYDET	D10	ENET_ENERGYDET 24
F1000	K4	IPU	SLAVE*/AN_EN	C10	IPU TP_VESTA_AN_EN 9
SPD0	K5	IPD	QUALITY*/TXC_RXC_DELAY	A8	IPD TP_VESTA_TXC_RXC_DELAY 9
MANMS	D9	IPD	LINK1*	A10	IPD TP_VESTA_LINK1_L 9
HUB	A9	IPD	LINK2*	B11	IPD TP_VESTA_LINK2_L 9
ER	H3	IPD	FDXLED*	B10	IPD TP_VESTA_FDXLED_L 9
TEST[0]	M4		XMTLED*	B12	IPU TP_VESTA_XMTLED_L 136
TEST[1]	M5		ACTLED*	B11	IPU TP_VESTA_ACTLED_L 136
TVCO	N3				
XTALI	N2				
XTALO	P2		RDAC1	R1	VESTA_RDAC1_PD

XTALGND BIASGND PLLGND1

TERMINATION OFF PAGE

Q63 APPLICATION IS ALL
139 17 7 =PP3V3_ENETFW
RD204 1K 1% 1/16W MF-LF 402
QD200 2N7002DW-X-F SOT-363
136 132 7 =PP3V3_ENET
CD206 1UF 10% 6.3V CERM 402
QD200 2N7002DW-X-F SOT-363
17 VESTA_RESET_H
136 132 7 =PP3V3_ENET
RD250 1.5K 5% 1/16W MF-LF 402
131 ENET_MDC
131 130 ENET_MDIO
VESTA_ENET_LOWPWR
9 TP_VESTA_PHYA<0>
9 TP_VESTA_PHYA<1>
9 TP_VESTA_PHYA<2>
9 TP_VESTA_PHYA<3>
9 TP_VESTA_PHYA<4>
9 TP_VESTA_EN_10B
9 TP_VESTA_RGMIIEN
9 TP_VESTA_FDX
9 TP_VESTA_F1000
9 TP_VESTA_SPD0
9 TP_VESTA_MANMS
9 TP_VESTA_HUB
9 TP_VESTA_ER
9 TP_VESTA_TEST<0>
9 TP_VESTA_TEST<1>
9 TP_VESTA_TVCO
IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP
Put crystal circuit close to PHY
132 VESTA_CLK25M_XTALI
132 VESTA_CLK25M_XTALO_R
RD209 0 5% 1/16W MF-LF 402
CRITICAL
YD200 25.0000M SM-2
VESTA_CLK25M_XTALO 132
CD218 33pF 5% 50V CERM 402
CD219 33pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 20PF
RD213 1.24K 1% 1/16W MF-LF 402

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 132 OF 154	

LAST_MODIFIED=Thu May 19 14:08:40 2005
DRAWING

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

P292	ENET	ENET_MDI_P<0>	132 136
P296	ENET	ENET_MDI_N<0>	132 136
P297	ENET	ENET_MDI_P<1>	132 136
P298	ENET	ENET_MDI_N<1>	132 136
P299	ENET	ENET_MDI_P<2>	132 136
P300	ENET	ENET_MDI_N<2>	132 136
P301	ENET	ENET_MDI_P<3>	132 136
P302	ENET	ENET_MDI_N<3>	132 136

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD601 330 5% 1/10W MF-LF 603
LED8700_P
DEVELOPMENT
LEDD600 GREEN 2.0X1.25A

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>
RD604 49.9 1% 1/16W MF-LF 402
RD605 49.9 1% 1/16W MF-LF 402
ENET_MDI0
136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>
CD606 0.01UF 20% 16V CERM 402
RD606 49.9 1% 1/16W MF-LF 402
RD607 49.9 1% 1/16W MF-LF 402
ENET_MDI1
136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>
RD608 49.9 1% 1/16W MF-LF 402
RD609 49.9 1% 1/16W MF-LF 402
CD607 0.01UF 20% 16V CERM 402
ENET_MDI2
136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>
CD608 0.01UF 20% 16V CERM 402
RD610 49.9 1% 1/16W MF-LF 402
RD611 49.9 1% 1/16W MF-LF 402
ENET_MDI3
CD609 0.01UF 20% 16V CERM 402

LD600
FERR-EMI-600-OHM
SM
7 =PP2V5_ENET
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.20mm
MIN_NECK_WIDTH=0.138mm
VOLTAGE=2.5V
CD600 0.1UF 20% 10V CERM 402
CD601 0.1UF 20% 10V CERM 402
7 GND_CHASSIS_RJ45
CD604 0.001UF 10% 50V CERM 402

(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
RJ45 CHIP SIDE
1CT:1CT
75 OHM
SECONDARY
J1 J2 J3 J4 J5 J6 J7 J8
RJ45 CABLE SIDE
SHIELD 1000PF, 2000V
CD605 0.001UF 10% 50V CERM 402

132 TP_VESTA_XMTLED_L
VESTA_XMTLED_L
MAKE_BASE=TRUE

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD603 330 5% 1/10W MF-LF 603
LED8701_P
DEVELOPMENT
LEDD601 GREEN 2.0X1.25A

132 TP_VESTA_ACTLED_L
VESTA_ACTLED_L
MAKE_BASE=TRUE

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE-VIA
ZHD691 HOLE-VIA
ZHD692 HOLE-VIA
ZHD693 HOLE-VIA

ETHERNET CONNECTOR

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 136 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	0.38mm_SPACING	
	0.38mm_SPACING	
	0.38mm_SPACING	

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

119 24 23 7 =PP2V5_PWRON_SB

CD800 0.1uF 20% 10V CERM 402
CD801 0.1uF 20% 10V CERM 402
CD802 0.1uF 20% 10V CERM 402

FWVDDP
U2300
SHASTA
V1.1
BGA-LF
SEE TABLE (7 OF 8)

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	138 139
PHY_DATA_1_H	P5	FW_DATA<1>	138 139
PHY_DATA_2_H	N1	FW_DATA<2>	138 139
PHY_DATA_3_H	M7	FW_DATA<3>	138 139
PHY_DATA_4_H	N6	FW_DATA<4>	138 139
PHY_DATA_5_H	L1	FW_DATA<5>	138 139
PHY_DATA_6_H	M3	FW_DATA<6>	138 139
PHY_DATA_7_H	L2	FW_DATA<7>	138 139
PHY_CTL_0_H	N2	139 128 FW_CTL_S<0>	RD801 0 5% 1/16W MF-LF 402 FW_CTL<0> 138 139
PHY_CTL_1_H	N3	139 138 FW_CTL_S<1>	RD802 0 5% 1/16W MF-LF 402 FW_CTL<1> 138 139
PHY_LPS_H	P6	FW_LPS	138 139
PHY_LREQ_H	P1	FW_LREQ	138 139
PHY_SCLK_H	P2	139 138 FW_CLK98M_PCLK	
PHY_PINT_L	P3	139 138 FW_PINT	
PHY_LCLK_H	R1	138 FW_CLK98M_LCLK_R	RD800 22 5% 1/16W MF-LF 402 FW_CLK98M_LCLK 138 139
PHY_LINKON_L	N7	FW_LINKON	139

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 138 OF 154	

LAST_MODIFIED=Thu May 19 14:08:42 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)		0.38mm SPACING		FW_CLK98M_PCLK_R 139
	FW	FW	FW_TPA0	FW_TPA_P<0> 139 140
	FW	FW	FW_TPA0	FW_TPA_N<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_P<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_N<0> 139 140
	FW	FW	FW_TPA1	FW_TPA_P<1> 139 140
	FW	FW	FW_TPA1	FW_TPA_N<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_P<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_N<1> 139 140
ETHERNET SPACING TO ROUTE ON LAYER 6	FW	FW	FW_TPA2	FW_TPA_P<2> 139 140
	FW	FW	FW_TPA2	FW_TPA_N<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_P<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_N<2> 139 140
		0.38mm SPACING		VESTA_CLK24M_XTALI 139
		0.38mm SPACING		VESTA_CLK24M_XTALO 139
		0.38mm SPACING		VESTA_CLK24M_XTALO_R 139
	FW_CTL			FW_CTL_S<1..0> 138
	FW_CTL			FW_CTL<1..0> 138 139
	FW_CTL			FW_CTL_R<1..0> 138 139

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

ESDET[0]
1=PORTS 1 AND 2 DS ONLY
0=PARTS 1 AND 2 BI-LINGUAL
ESDET[1]
1=PORT 1 PRESENT
0=PORT 1 NOT PRESENT
ESDET[2]
1=PORT 2 PRESENT
0=PORT 2 NOT PRESENT

CRYSTAL LOAD CAPACITANCE IS 12PF

IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP

LAST_MODIFIED=Thu May 19 14:08:43 2005

Vesta FireWire PHY		
SYNC_MASTER=Q63	SYNC_DATE=05/18/2005	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790 / REV. 08
	SCALE NONE	SHT 139 OF 154

NET_TYPE		
SPACING	PHYSICAL	DIFFERENTIAL_PAIR

R401	FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL
R400	FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL
R402	FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL
R404	FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL
R403	FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL
R405	FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL
R407	FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL
R406	FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL

=PP12V_ALL_FW

8 WATTS MAX
12 VOLTS

RE056 1.3 20% 1W FF 2512 — PP12V_FW (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V, MAKE_BASE=TRUE)

I443 =PPFW_PHY 139 — TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XKG SMC

FW_VP_R (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, MAKE_BASE=TRUE, VOLTAGE=24V)

CRITICAL
RE002 1.3 20% 1W FF 2512

FW_VP (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=24V)

FE002 0.75AMP-13.2V MINISMD

PPFW_PORT0_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

FE000 1.5AMP-33V SM

PPFW_PORT1_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V) 140

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

CE009 0.1UF 10% 50V X7R 603-1

FW_VP MAX IS 24V

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
FW_TPBIAS<1> 139
FW_TPBIAS<0> 139
VOLTAGE=1.86V

CE050 1uF 10% 6.3V CERM 402
CE060 1uF 10% 6.3V CERM 402

RE050 56.2 1% 1/16W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/16W MF-LF 402

FW_TPA_P<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPA_P 140
FW_TPA_N<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPA_N 140
FW_TPB_P<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPB_P 140
FW_TPB_N<0> 139	MAKE_BASE=TRUE	FW_PORT0_TPB_N 140
FW_TPA_P<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPA_P 140
FW_TPA_N<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPA_N 140
FW_TPB_P<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPB_P 140
FW_TPB_N<1> 139	MAKE_BASE=TRUE	FW_PORT1_TPB_N 140

RE052 56.2 1% 1/16W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/16W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V
FW_TPA_C<1> VOLTAGE=0V

RE054 4.99K 1% 1/16W MF-LF 402
CE054 270pF 5% 25V CERM 402
CE064 270pF 5% 25V CERM 402
RE064 4.99K 1% 1/16W MF-LF 402

3rd TPA/TPB pair unused

FW_TPBIAS<2> 139	NC_FW_TPBIAS2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPA_P<2> 139	NC_FW_TPA_P2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPA_N<2> 139	NC_FW_TPA_N2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPB_P<2> 139	FW_TPB2_PD	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPB_N<2> 139		

RE070 1K 5% 1/16W MF-LF 402

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

=PP3V3_FW 7 — RE090 215 1% 1/16W MF-LF 402 — PP3V3_FW_ESD_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — LE090 400-OHM-EMI SM-1 — PP3V3_FW_ESD 140 (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD 140

DPE010 BAV99DW-X-F SOT-363
DPE011 BAV99DW-X-F SOT-363

CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402
CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE 7 140

FLE010 120-OHM 2012 SM_YBK-1
FLE011 120-OHM 2012 SM_YBK-1

FW_PORT0_TPA_P 140
FW_PORT0_TPA_N 140
FW_PORT0_TPB_P 140
FW_PORT0_TPB_N 140

LE010 FERR-160-OHM 1206-LF

PORT 0
1394A
OMIT

JE000 UF01613-M33-4F F-ST-TH

TPO	(TPA+)	FW_PORT0_TPA_P_FL 140
TPO#	(TPA-)	FW_PORT0_TPA_N_FL 140
TPI	(TPB+)	FW_PORT0_TPB_P_FL 140
TPI#	(TPB-)	FW_PORT0_TPB_N_FL 140
VP		PPFW_PORT0_VP_FL (VOLTAGE=24V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm)
VGND		

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE 7 140

CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01uF 20% 16V CERM 402

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD 140

DPE020 BAV99DW-X-F SOT-363
DPE021 BAV99DW-X-F SOT-363

CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402
CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE 140

FLE020 120-OHM 2012 SM_YBK-1
FLE021 120-OHM 2012 SM_YBK-1

FW_PORT1_TPA_P 140
FW_PORT1_TPA_N 140
FW_PORT1_TPB_P 140
FW_PORT1_TPB_N 140

PPFW_PORT1_VP 140

LE020 FERR-160-OHM 1206-LF

PORT 1
1394A
OMIT

JE001 UF01613-M33-4F F-ST-TH

TPO	(TPA+)	FW_PORT1_TPA_P_FL 140
TPO#	(TPA-)	FW_PORT1_TPA_N_FL 140
TPI	(TPB+)	FW_PORT1_TPB_P_FL 140
TPI#	(TPB-)	FW_PORT1_TPB_N_FL 140
VP		PPFW_PORT1_VP_FL (VOLTAGE=24V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm)
VGND		

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE 7 140

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01uF 20% 16V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-HC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 140 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2_S	USB2_0	USB2_P<0>
	USB2	USB2_S	USB2_0	USB2_N<0>
	USB2	USB2_S	USB2_1	USB2_P<1>
	USB2	USB2_S	USB2_1	USB2_N<1>
	USB2	USB2_S	USB2_2	USB2_P<2>
	USB2	USB2_S	USB2_2	USB2_N<2>
	USB2	USB2	USB2_3	USB2_P<3>
	USB2	USB2	USB2_3	USB2_N<3>
	USB2	USB2	USB2_4	USB2_P<4>
	USB2	USB2	USB2_4	USB2_N<4>
	0.38mm SPACING			NEC_CLK30M_XT1
	0.38mm SPACING			NEC_CLK30M_XT2
	0.38mm SPACING			NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

U2300 SHASTA V1.1 BGA-LF (8 OF 8)
NC0 P7 TP_SB<0>
NC1 P8 TP_SB<1>
NC2 R3 TP_SB<2>
NC3 R4 TP_SB<3>
NC4 R5 TP_SB<4>
NC5 R6 TP_SB<5>
NC6 R7 TP_SB<6>
NC7 R8 TP_SB<7>
NC8 T1 TP_SB<8>
NC9 T2 TP_SB<9>
NC10 T3 TP_SB<10>
NC11 T4 TP_SB<11>
NC12 T5 TP_SB<12>
NC13 T6 TP_SB<13>
NC14 T7 TP_SB<14>
NC15 T8 TP_SB<15>
NC16 U1 TP_SB<16>
NC17 U2 TP_SB<17>
NC18 U3 TP_SB<18>
NC19 U4 TP_SB<19>
NC20 U5 TP_SB<20>
NC21 U6 TP_SB<21>
NC22 V1 TP_SB<22>
NC23 V2 TP_SB<23>
NC24 V3 TP_SB<24>
NC25 V4 TP_SB<25>
NC26 W1 TP_SB<26>
NC27 W3 TP_SB<27>
NC28 Y1 TP_SB<28>
NC29 Y3 TP_SB<29>

LE235 FERR-EMI-100-OHM SM
RE235 4.7 5% 1/10W MF-LF 603
=PP3V3_PWRON_USB
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
CE235 10UF 10% 6.3V X5R 805
CE236 0.1uF 20% 10V CERM 402
CE237 0.1uF 20% 10V CERM 402
XWE200 SM OMIT
TP_NEC_AVDD
P4MM SM PPE2000
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
GND_NEC_AVSS_R
CE220 10UF 10% 6.3V X5R 805
CE221 CE222 CE223 CE224 CE225 0.1uF 20% 10V CERM 402
CE226 CE227 CE228 CE229 CE230 0.1uF 20% 10V CERM 402
VDD
AVDD

UC200 NEC_UPD720101_USB2 FBGA-LF

RE210 33K 5% 1/16W MF-LF 402
RPE210 10K 5% 1/16W SM-LF
USB2_OC<0> B12 OCI1
USB2_OC<1> B11 OCI2
USB2_OC<2> B10 OCI3
USB2_OC<3> A10 OCI4
USB2_OC<4> B9 OCI5
USB2_PWREN<0> C12 PPON1
USB2_PWREN<1> A11 PPON2
USB2_PWREN<2> C11 PPON3
USB2_PWREN<3> C10 PPON4
USB2_PWREN<4> A9 PPON5

RE240 1.5K 5% 1/16W MF-LF 402
RE241 1.5K 5% 1/16W MF-LF
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

NEC_CLK30M_XT1 L9 XT1/SCLK
NEC_CLK30M_XT2_R P8 XT2
RE245 100 1% 1/16W MF-LF 402
YE245 30.0000M CRYSTAL SM-1
NEC_CLK30M_XT2
CE245 22pF 5% 50V CERM 402
CE246 22pF 5% 50V CERM 402
SPEC SHOWS LOAD CAPACITANCE OF 16PF

RSDM1 M14 USB_NEC_N<0> — RE200 36 1% 1/16W MF-LF 402 — USB2_N<0>
DM1 M13 — USB2_N<0>
DP1 L14 — USB2_P<0>
RSDP1 K13 USB_NEC_P<0> — RE201 36 1% 1/16W MF-LF 402 — USB2_P<0>

P4MM SM PPE2002

RSDM2 K14 USB_NEC_N<1> — RE202 36 1% 1/16W MF-LF 402 — USB2_N<1>
DM2 K12 — USB2_N<1>
DP2 J14 — USB2_P<1>
RSDP2 J12 USB_NEC_P<1> — RE203 36 1% 1/16W MF-LF 402 — USB2_P<1>

P4MM SM PPE2001

RSDM3 H11 USB_NEC_N<2> — RE204 36 1% 1/16W MF-LF 402 — USB2_N<2>
DM3 G11 — USB2_N<2>
DP3 G13 — USB2_P<2>
RSDP3 G14 USB_NEC_P<2> — RE205 36 1% 1/16W MF-LF 402 — USB2_P<2>

40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

RSDM4 F12 USB_NEC_N<3> — RE206 36 1% 1/16W MF-LF 402 — USB2_N<3>
DM4 F14 — USB2_N<3>
DP4 E12 — USB2_P<3>
RSDP4 E14 USB_NEC_P<3> — RE207 36 1% 1/16W MF-LF 402 — USB2_P<3>

RSDM5 E13 USB_NEC_N<4> — RE208 36 1% 1/16W MF-LF 402 — USB2_N<4>
DM5 D14 — USB2_N<4>
DP5 C13 — USB2_P<4>
RSDP5 C14 USB_NEC_P<4> — RE209 36 1% 1/16W MF-LF 402 — USB2_P<4>

BLUTOOTH CONNECTOR,(PORT #4)

RREF P11 NEC_RREF_PD
RE238 9.09K 1% 1/16W MF-LF 402
MINIMIZE TRACE LENGTH TO PINS
GND_NEC_AVSS_R VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

VSS B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 E8
AVSS P13 M12 N11 AVSS(R)
XWE201 SM OMIT
Tie to GND at ball N11

USB Host Interfaces

SYNC_MASTER=Q63 SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 142 OF 154	

LAST_MODIFIED=Thu May 19 14:08:45 2005
DRAWING
TITLE=K61LOGBAA
SHEET=SHEET142

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
142 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
142 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
142 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
142 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

External USB Ports

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0247	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0250	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_P_F	USB2	USB2_PORT1_P_F 143
	USB2	USB2_PORT1_P_F	USB2	USB2_PORT1_N_F 143
	USB2	USB2_PORT2_P_F	USB2	USB2_PORT2_P_F 143
	USB2	USB2_PORT2_P_F	USB2	USB2_PORT2_N_F 143
	USB2	USB2_PORT3_P_F	USB2	USB2_PORT3_P_F 143
	USB2	USB2_PORT3_P_F	USB2	USB2_PORT3_N_F 143
E608	USB2	USB2_HUB_P_F	USB2	USB2_HUB_P_L<2> 143
E609	USB2	USB2_HUB_P_F	USB2	USB2_HUB_N_L<2> 143
E610	USB2	USB2_BNDI_F	USB2	USB2_P_L<3> 143
E611	USB2	USB2_BNDI_F	USB2	USB2_N_L<3> 143

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT
142 USB2_P<4> — USB2_HUB_P<0> 144 MAKE_BASE=TRUE
142 USB2_N<4> — USB2_HUB_N<0> 144 MAKE_BASE=TRUE

SENDS USB HUB PORT 3 TO BLUETOOTH MODULE
121 USB_BT_P — USB2_HUB_P<3> 144 MAKE_BASE=TRUE
121 USB_BT_N — USB2_HUB_N<3> 144 MAKE_BASE=TRUE

USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEED HERE

USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEEDED HERE

USB Device Interfaces

SYNC_MASTER=FINO-MB SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

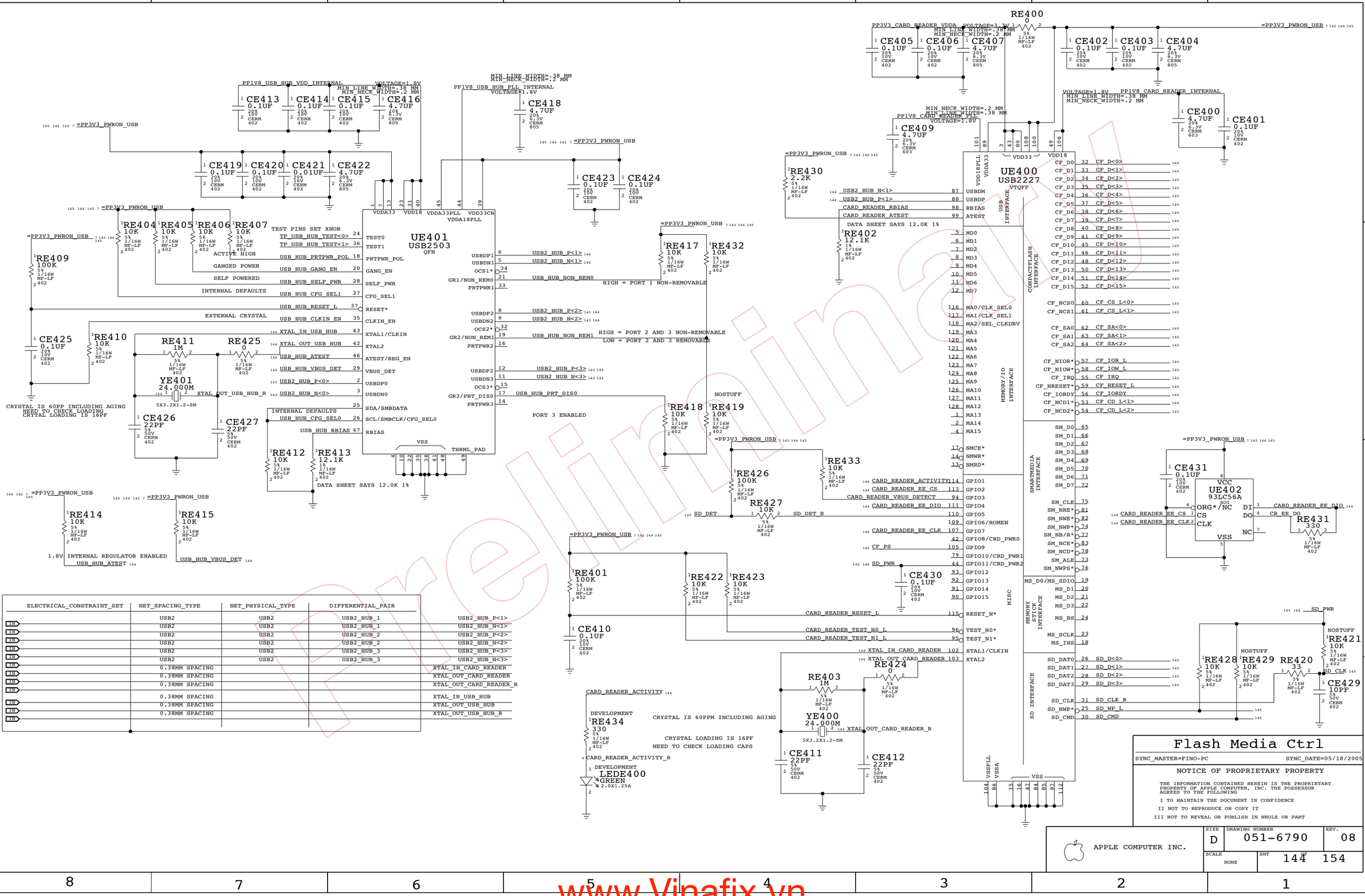
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 143 OF 154	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
	0.38MM SPACING			XTAL_IN_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER_R
	0.38MM SPACING			XTAL_IN_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

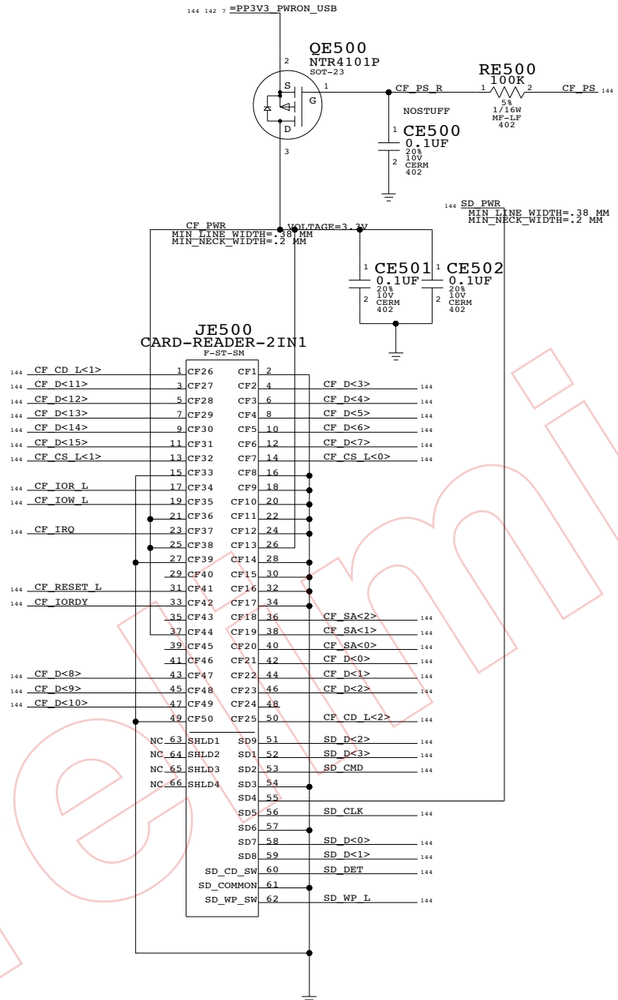
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 144 OF 154	



Flash Connector

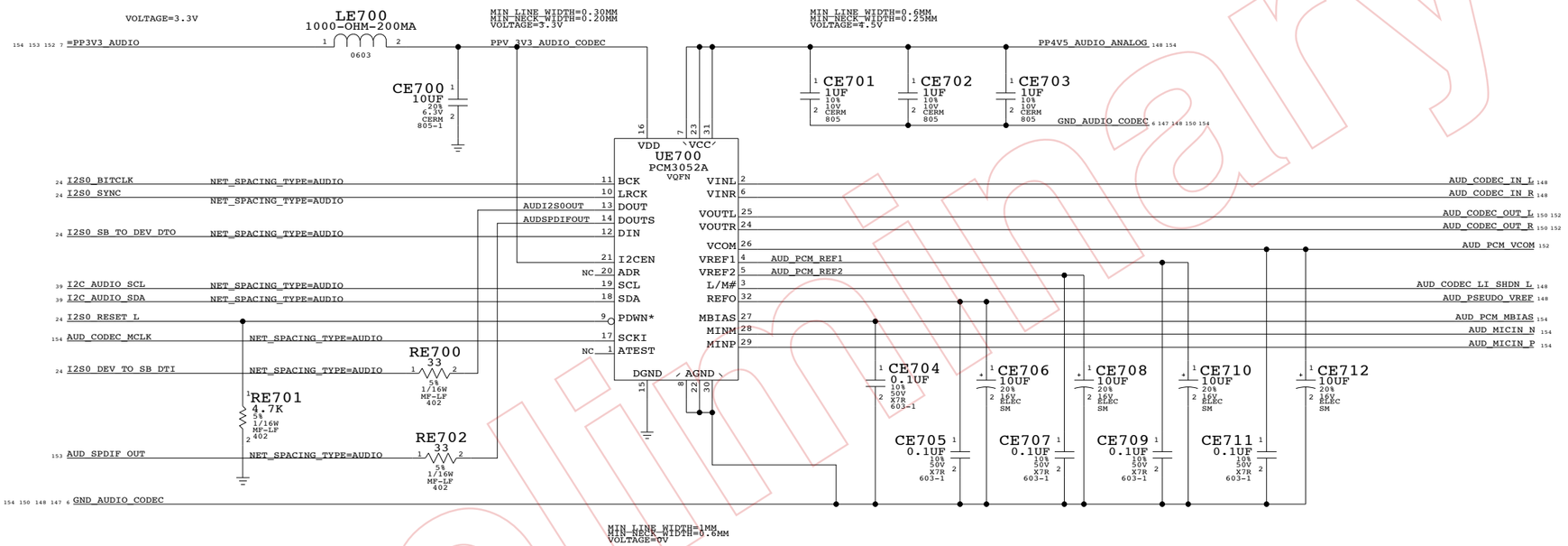
SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT
NONE	145 OF 154

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

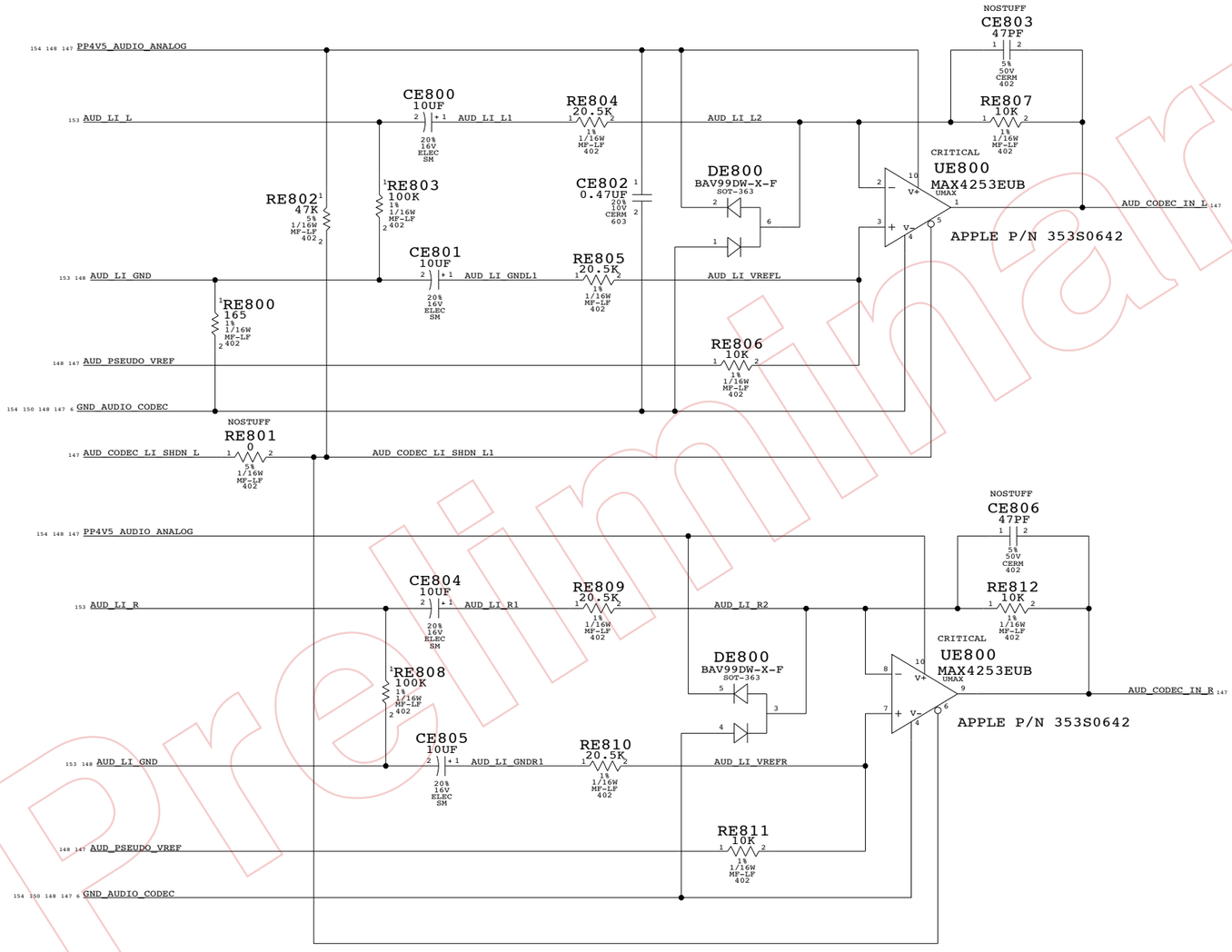
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 147 OF 154	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

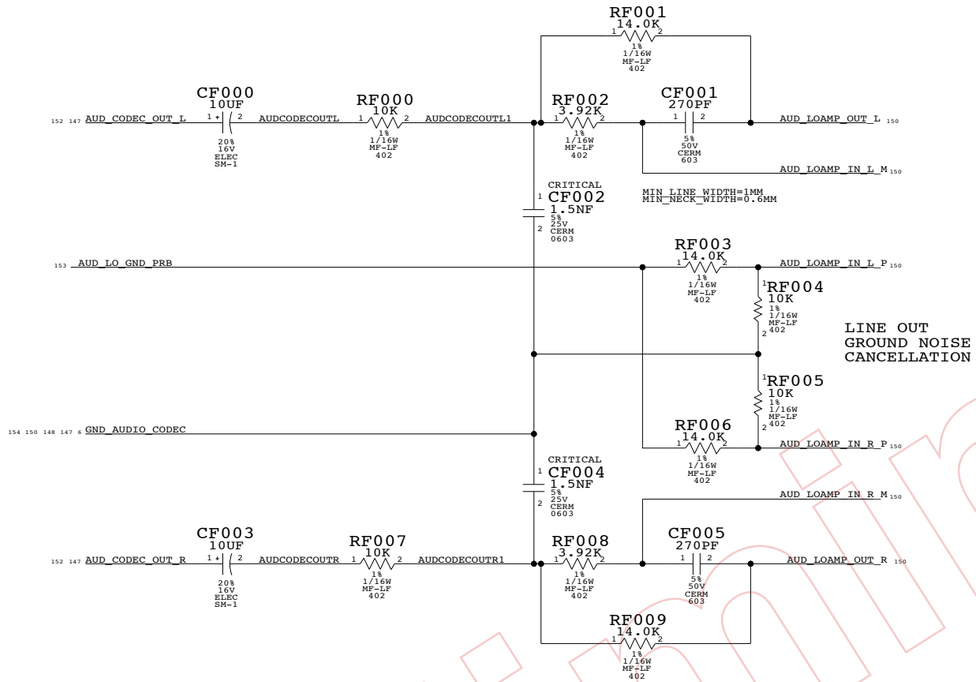
SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 148 OF 154	

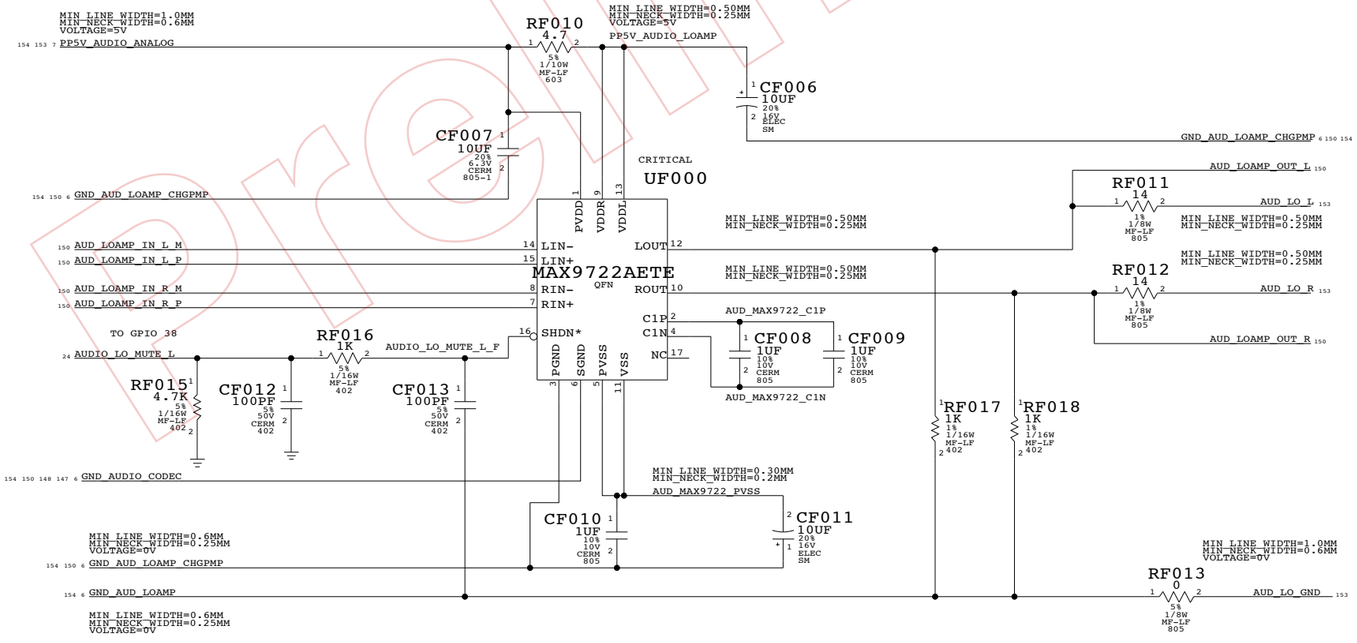
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 150 OF 154	

SPEAKER AMP

APPLE P/N 353S0680

NET_SPACING_TYPE=AUDIO
DIFFERENTIAL_PAIR=AUD_SPKRAMP_PWR
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.30MM
VOLTAGE=12V

7 6 PP12V_AUDIO_SPKRAMP

LF200
FERR-250-OHM
SM-1

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.30MM
VOLTAGE=12V

PP12V_AUD_SPKRAMP_PLANE

CF217 220UF 20% 16V ELEC SM-2
CF200 220UF 20% 16V ELEC SM-2
CF201 10UF 10% 16V CERM 1210
CF218 0.1UF 20% 16V CERM 603
CF202 1UF 20% 16V CERM 1206
CF219 0.1UF 20% 16V CERM 603
CF203 10UF 10% 16V CERM 1210
CF223 10UF 10% 16V CERM 1210

154 152 6 GND_AUDIO_SPKRAMP_PLANE

GND_AUDIO_SPKRAMP_PLANE 6 152 154

=PP3V3_AUDIO 7 147 152 153 154

RF214 10K 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM
AUDSAMPOUTLP

LF201 180-OHM-1.5A 0603
AUD_SPKR_OUTL_P 153

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM

150 147 AUD_CODEC_OUT_L

LF205 1000-OHM-200MA 0603
CF204 0.47UF 10% 16V X7R 805
AUDSAMPINLN
CF215 100PF 5% 50V CERM 402

AUD_SAMP_INL_N 9 INL-
AUD_SAMP_INL_P 10 INL+

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM
AUDSAMPOUTLN

LF202 180-OHM-1.5A 0603
AUD_SPKR_OUTL_N 153

147 AUD_PCM_VCOM

LF206 1000-OHM-200MA 0603
CF205 0.47UF 10% 16V X7R 805
AUDSAMPINLP

AUD_SAMP_INR_P 16 INR+
AUD_SAMP_INR_N 15 INR-

UF200
MAX9714
QFN

VDD 3 4 21 22
CHOLD 7
OUTL+ 31
OUTL+ 32
OUTL- 29
OUTL- 30
C1+ 6
C1- 5
OUTR+ 27
OUTR+ 28
OUTR- 25
OUTR- 26
SS 12

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP

CF208 0.1UF 10% 50V X7R 603-1

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPN

152 AUD_SAMP_G1 17 G1
152 AUD_SAMP_G2 18 G2
152 AUD_SAMP_FS1 19 FS1
152 AUD_SAMP_FS2 20 FS2
AUD_SAMP_SHDN_L 11 SHDN*
NC 8 NC
AUD_MAX9714_VREG 14 REG

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM

THM AGND PAD PGND
13 33 1 2 23 24

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM
AUDSAMPOUTRP

LF203 180-OHM-1.5A 0603
AUD_SPKR_OUTR_P 153

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM

150 147 AUD_CODEC_OUT_R

LF208 1000-OHM-200MA 0603
CF207 0.47UF 10% 16V X7R 805
AUDSAMPINRN

CF216 100PF 5% 50V CERM 402
CF206 0.47UF 10% 16V X7R 805
AUDSAMPINRP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM
AUDSAMPOUTRN

LF204 180-OHM-1.5A 0603
AUD_SPKR_OUTR_N 153

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCSS

CF209 0.47UF 10% 16V X7R 805

CF210 1000PF 5% 25V CERM 603
CF211 1000PF 5% 25V CERM 603
CF212 1000PF 5% 25V CERM 603
CF213 1000PF 5% 25V CERM 603

154 153 152 147 7 =PP3V3_AUDIO

RF215 10K 1% 1/16W MF-LF 402
AUDIO_SPKR_MUTE_L_INV

TIE TO GPIO 40

24 AUDIO_SPKR_MUTE_L

RF213 47K 5% 1/16W MF-LF 402
AUDIO_SPKR_MUTE_L_F 2

QF200 2N7002DW SOT-363
QF200 2N7002DW SOT-363

RF212 4.7K 5% 1/16W MF-LF 402
CF220 100PF 5% 50V CERM 402
CF221 100PF 5% 50V CERM 402

CF214 0.47UF 10% 16V X7R 805

XCF200 50R28

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.25MM
AUDIO_SPKRAMP_PWR

XWF201 SM OMIT

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.25MM

154 7 6 GND_AUDIO_SPKRAMP

154 152 6 GND_AUDIO_SPKRAMP_PLANE

GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

154 153 152 147 7 =PP3V3_AUDIO

RPF200 47K 5% 1/16W SM-LF
8 7 6 5
1 2 3 4

152 AUD_SAMP_FS2
152 AUD_SAMP_FS1
152 AUD_SAMP_G2
152 AUD_SAMP_G1

RF208 0 5% 1/16W MF-LF 402

154 152 6 GND_AUDIO_SPKRAMP_PLANE

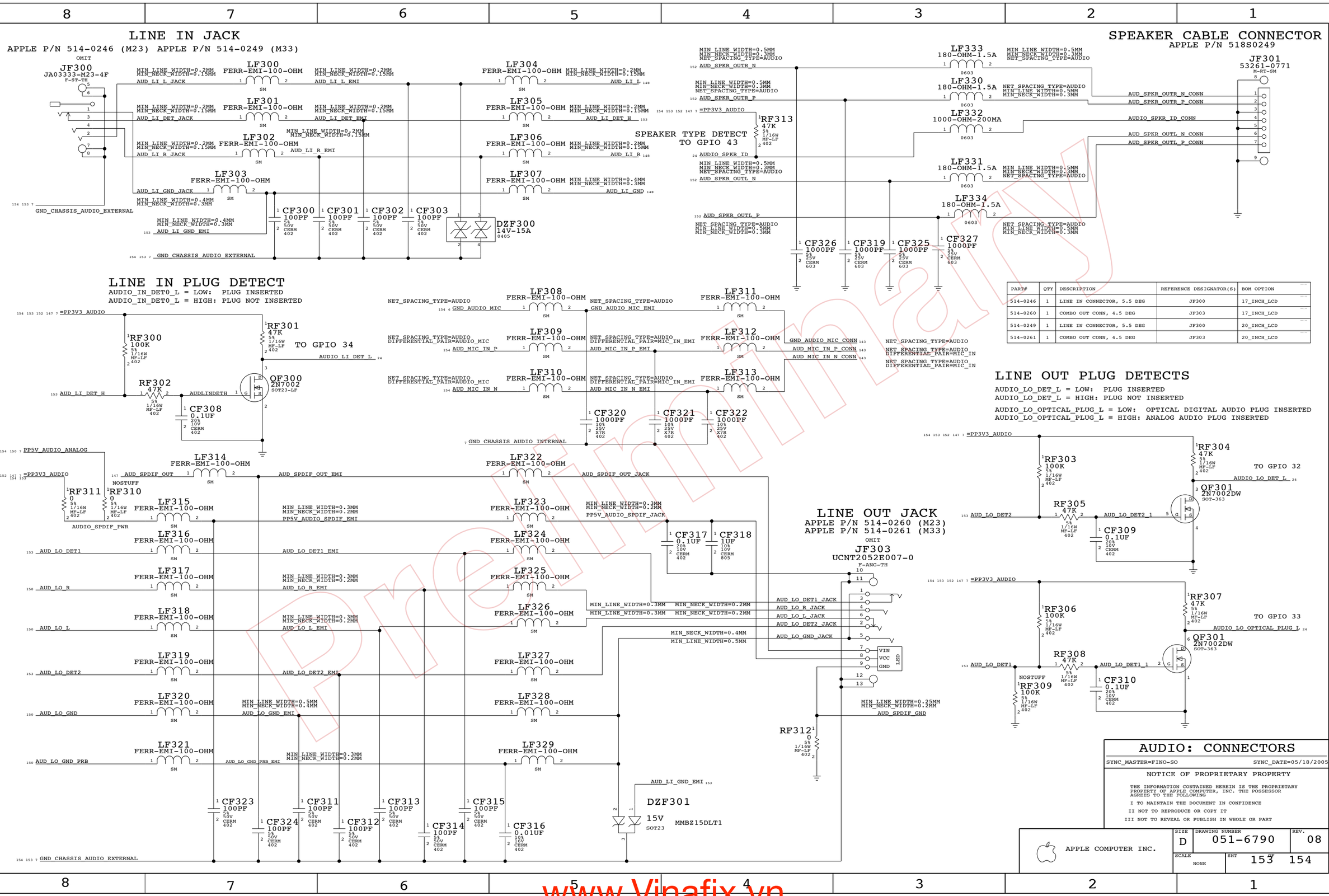
AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08

SCALE	SHT	OF
NONE	152	154

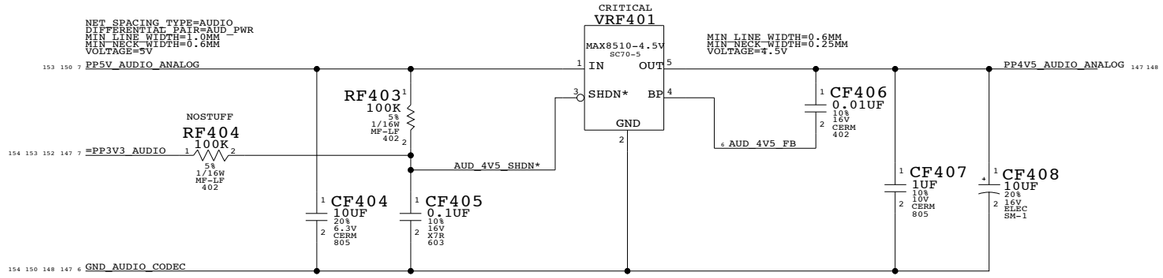


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

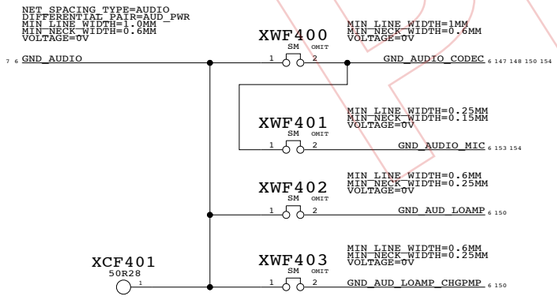
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733



AUDIO GROUND RETURNS



PLACE ACROSS GROUND SPLIT

NOSTUFF

RF416

152 6 GND_AUDIO_SPKRAMP_PLANE — GND_AUDIO_CODEC 6 147 148 150 154

PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE

NOSTUFF

RF417

152 7 6 GND_AUDIO_SPKRAMP

PLACE ACROSS GROUND SPLIT AT CODEC UE700

RF405

154 150 148 147 6 GND_AUDIO_CODEC

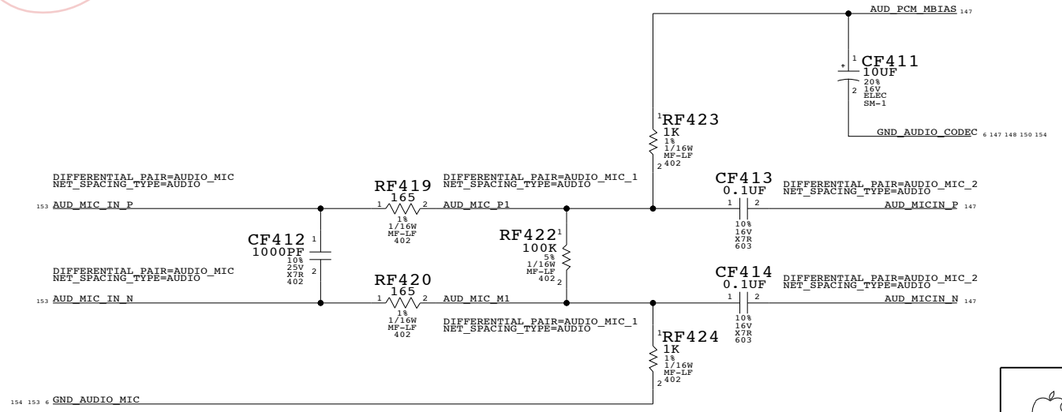
PLACE AT JF303

NOSTUFF

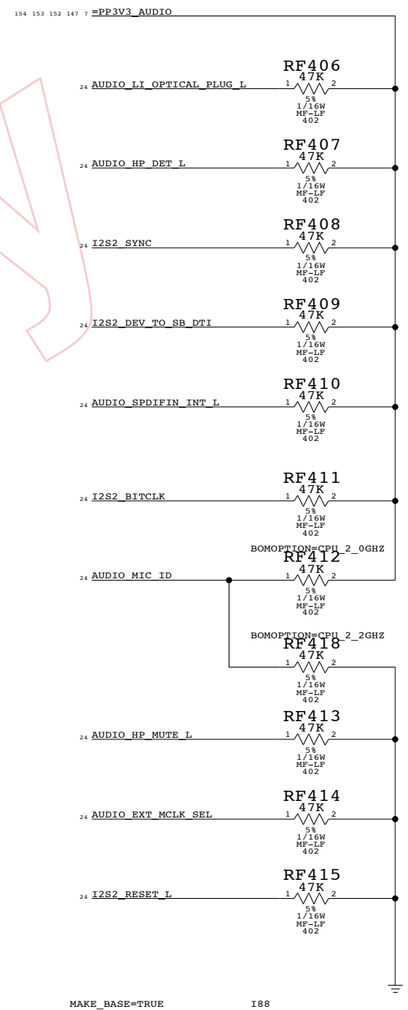
RF429

153 7 GND_CHASSIS_AUDIO_EXTERNAL

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	08
SCALE: NONE	SHT 154 OF 154	