1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

FINO M33
5/19/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
07		381758	ENGINEERING RELEASED	05/19/05	?

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9	11	1.8V VREG		M33-PC	05/19/2005
10	12	1.5V Vreg		FINO-PC	05/19/2005
11	13	1.2V Vreg		FINO-PC	05/19/2005
12	15	2.5V Vreg		FINO-PC	05/19/2005
13	16	5V & 3.3V Fets		FINO-PC	05/19/2005
14	17	Vesta Core / Misc		FINO-HC	05/19/2005
15	19	KODIAK CORE & BYPASS		Q63	05/19/2005
16	20	KODIAK & SHASTA MISC		FINO-ME	05/19/2005
17	23	Shasta Core Power		Q63	05/19/2005
18	24	Shasta Serial / Misc		FINO-ME	05/19/2005
19	25	PULSAR2 POWER		Q63	05/19/2005
20	26	PULSAR2 CLOCKS		FINO-ME	05/19/2005
21	27	Pulsar Aliases		FINO-ME	05/19/2005
22	28	System Management Unit		Q63	05/19/2005
23	29	SMU SUPPLEMENTAL (2)		FINO-MS	05/19/2005
24	30	SMU SUPPLEMENTAL (3)		FINO-MS	05/19/2005
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26	32	Fan 0, 1 & System Temp		FINO-PC	05/19/2005
27	33	Fan 2 & HD Temp		FINO-PC	05/19/2005
28	39	I2C Connections		FINO-ME	05/19/2005
29	41	KODIAK EI PWR & CAPS		Q63	05/19/2005
30	42	KODIAK EI A		Q63	05/19/2005
31	43	CPU EI AND IO		FINO-MS	05/19/2005
32	44	KODIAK EI B		Q63	05/19/2005
33	47	CPU STRAPS		FINO-MS	05/19/2005
34	48	CPU POWER AND BYPASS		FINO-MS	05/19/2005
35	49	PROC DECOUPLING		FINO-MS	05/19/2005
36	50	CPU VCORE VREG		M33-MS	05/19/2005
37	52	CPU VCORE MORE BYPASS		FINO-MS	05/19/2005
38	54	CPU AVDD VREG		FINO-MS	05/19/2005
39	55	T,V,I SENSORS		FINO-MS	05/19/2005
40	56	CPU ALIASES & MISC		FINO-MS	05/19/2005
41	58	KODIAC NBMEM PWR & CAPS		Q63	05/19/2005
42	59	Kodiak Memory Dq/Ctl		FINO-RT	05/19/2005
43	61	Parallel Term		FINO-RT	05/19/2005
44	62	Main Memory Clock Buffer		FINO-RT	05/19/2005
45	63	MEMORY ADDR BRANCHING		FINO-EG	05/19/2005
46	67	Memory Dimm A		FINO-RT	05/19/2005
47	68	MLB Mem Series Term		FINO-RT	05/19/2005
48	69	On-Board DDR SDRAM		FINO-RT	05/19/2005
49	70	On-Board DDR SDRAM		FINO-RT	05/19/2005
50	82	KODIAK PCI-E X16		Q63	05/19/2005
51	84	GPU PCIe		FINO-DD	05/19/2005
52	85	Graphics Vregs		M33-DD	MASTER
53	86	GPU Core Power		FINO-DD	05/19/2005
54	87	GPU Frame Buffer		FINO-DD	05/19/2005
55	88	FB Series Termination		FINO-DD	05/19/2005
56	89	GPU GDDR SDRAM A		FINO-DD	05/19/2005
57	90	GPU GDDR SDRAM B		FINO-DD	05/19/2005
58	91	FB Parallel Termination		M33-DD	MASTER
59	92	GPU Straps		FINO-DD	05/19/2005
60	93	GPU DVI & DACs		FINO-DD	05/19/2005
61	96	TMDS / ExtVGA		M33-DD	MASTER
62	97	KODIAK PCI-E CONST		FINO-DD	05/19/2005
63	98	KODIAK HT16		Q63	05/19/2005
64	101	HT ALIASES		FINO-EG	05/19/2005
65	103	Shasta HyperTransport		Q63	05/19/2005
66	119	Shasta PCI Interface		Q63	05/19/2005
67	120	PCI SERIES TERMINATION		FINO-EG	05/19/2005
68	121	AIRPORT & BLUETOOTH		FINO-EG	05/19/2005
69	122	USB 2.0 PCI Interface		Q63	05/19/2005
70	125	BootROM		Q63	05/19/2005
71	127	Shasta Disk		M33-MB	05/19/2005
72	129	Disk Connectors		M33-MB	05/19/2005
73	130	ENET SERIES TERM		FINO-HC	05/19/2005
74	131	Shasta Ethernet		Q63	05/19/2005
75	132	Vesta Ethernet PHY		Q63	05/19/2005
76	136	ETHERNET CONNECTOR		FINO-HC	05/19/2005
77	138	Shasta FireWire		Q63	05/19/2005
78	139	Vesta FireWire PHY		Q63	05/19/2005
79	140	FIREWIRE CONNECTORS		FINO-HC	05/19/2005
80	142	USB Host Interfaces		Q63	05/19/2005
81	143	USB Device Interfaces		FINO-MB	05/19/2005
82	144	Flash Media Ctrl		FINO-PC	05/19/2005
83	145	Flash Connector		FINO-PC	05/19/2005
84	147	AUDIO: CODEC		FINO-SO	05/19/2005
85	148	AUDIO: LINE INPUT AMP		FINO-SO	05/19/2005
86	150	AUDIO: LINE OUT AMP		FINO-SO	05/19/2005
87	152	AUDIO: SPEAKER AMP		FINO-SO	05/19/2005
88	153	AUDIO: CONNECTORS		FINO-SO	05/19/2005
89	154	AUDIO: POWER SUPPLIES		FINO-SO	05/19/2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

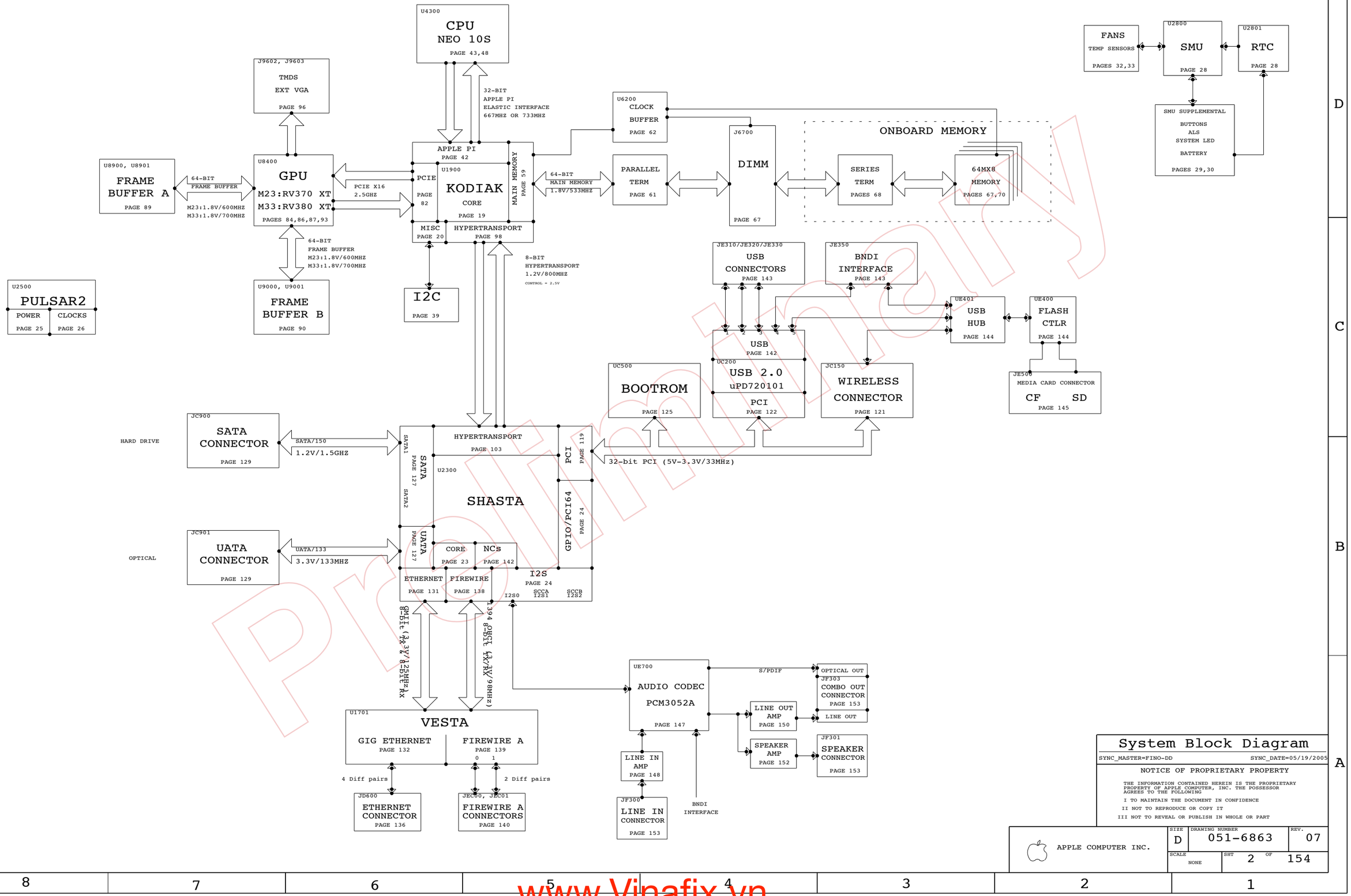
SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,FINO,M33

DRAWING NUMBER 051-6863 REV. 07

SHT 1 OF 154



System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

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POWER CONNECTOR

J700
PAGE 7

PP12V_ALL — FW CONN
PP12V_RUN — 20" PANEL POWER, 17" LCD INVERTER
PP5V_RUN — OPTICAL
PP5V_ALL
PP3V3_ALL
PP3V3_RUN — PCI BUS, AUDIO CODEC
SYS_POWERUP_L

SMU

SYS_POWERUP_L
POWER SEQUENCE PIN

NC_SMU_PWRSEQ_P1_0	SMU_PWRSEQ_P1_0	28
NC_SMU_PWRSEQ_P1_4	SMU_PWRSEQ_P1_4	28
TURN_ON_PP1V2_L	SMU_PWRSEQ_P1_1	28
PWR_GOOD_PP1V2	SMU_PWRSEQ_P9_5	28
PWR_GOOD_PP1V8	SMU_PWRSEQ_P9_6	28
TURN_ON_PP3V3_PWRON_L	SMU_PWRSEQ_P1_2	28
	SMU_PWRSEQ_P1_3	28

PP3V3_PWRON

PP1V5_PWRON SWITCHER — PAGE 12 — PULSAR, KODIAK CORE
PP1V5_RUN FET SWITCH — PAGE 12 — EI
CPU CORE SWITCHER — PAGE 50
GPU CORE SWITCHER — PAGE 85
PP1V8_PWRON SWITCHER — PAGE 11 — MAIN MEMORY
PP1V8_RUN POWER SW — PAGE 11 — GPU MEMORY
PP0V9_GPU_VTT LINEAR — PAGE 91
PP4V5_RUN_AUDIO LINEAR — PAGE 154 — AUDIO CODEC
PP5V_PWRON FET SWITCH — PAGE 16 — USB CONN
PP2V5_ALL LINEAR — PAGE 15 — VESTA
PP2V5_PWRON FET SWITCH — PAGE 15
PP2V5_RUN FET SWITCH — PAGE 15
PP3V3_PWRON FET SWITCH — PAGE 16 — MODEM & BT USB2 HOST
PP2V5_RUN_CPU_AVDD LINEAR — PAGE 54
PP2V5_GPU_A2VDD LINEAR — PAGE 85
PP1V8_TPVDD LINEAR — PAGE 85
PP1V5_VDDC_CT LINEAR — PAGE 85
PP1V8_GPU LINEAR — PAGE 85
PP1V2_ALL SWITCHER — PAGE 13 — VESTA CORE
PP1V2_TPVDD LINEAR — PAGE 85
PP1V2_PWRON FET SWITCH — PAGE 13 — SHASTA CORE
PP1V2_RUN FET SWITCH — PAGE 13 — HT BUS
PP1V2_PWRON

R431 10K 5% 1/16W MF-LF 402 — PP2V5_ALL
R430 100K 5% 1/16W MF-LF 402 — COMPARE_PP1V2
C430 0.01UF 20% 16V CERM 402
U400 LM339A SOI-LF — PS_1V_REF
R442 150K 5% 1/16W MF-LF 402 — PP2V5_ALL
R441 10K 5% 1/16W MF-LF 402 — PP2V5_ALL
R440 100K 5% 1/16W MF-LF 402 — COMPARE_PP1V8
C440 0.01UF 20% 16V CERM 402
R443 100K 1% 1/16W MF-LF 402
C441 0.1UF 20% 10V CERM 402
PP5V_ALL

PP2V5_ALL
U400P2
U400 LM339A SOI-LF

Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
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PROCESSORS

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3158	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,CQA	2.0GHZ	1.15V	46W	50MV	U4300	CPU_2_0GHZ
337S3157	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.2G,85C,FQA	2.2GHZ	1.15V	51W	50MV	U4300	CPU_2_2GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3165	337S3158	CPU_2_0GHZ	U4300	IC,DD3.1,2.0G,CJA	1.20V
337S3164	337S3157	CPU_2_2GHZ	U4300	IC,DD3.1,2.0G,FJA	1.20V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0371	1	IC,KODIAK,V1.1,PBGA,200MM	U1900	
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	
343S0324	1	IC,ASIC,VESTA,V1.3	U1701	
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
825-6447	1	BARCODE LABEL, MLB	LBL1	
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500	
341T1752	1	PURCH ASSY, SMU BIG	U2800	
603-7318	1	M23 CPU HEATSINK	MECH1	17_INCH_LCD
603-7321	1	M33 CPU HEATSINK	MECH1	20_INCH_LCD
603-7322	1	M33 GPU HEATSINK	MECH2	20_INCH_LCD
875-1614	1	CPU GAP FILLER	GAP1	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702	KINGBRIGHT LED
376S0204	376S0130		Q5010,Q5020	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q5011,Q5021	MOSFET,N-CH,VISHAY

Table Items

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 5 OF 154	

NO TEST XW NETS

D17	NO_TEST=YES	GND_U1100	11
D18	NO_TEST=YES	GND_U1200	12
D19	NO_TEST=YES	GND_U1300	13
D35	NO_TEST=YES	PP_2V5PWRONNBMISC	20
D35	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
D35	NO_TEST=YES	PP_3V3PWRONSBPCI64	23
D35	NO_TEST=YES	PP_2V5PWRONSB	23
D35	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
D35	NO_TEST=YES	PP_OVDD_PULSAR1	25
D35	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
D35	NO_TEST=YES	PP_1V5PULSAR2	25
D35	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
D35	NO_TEST=YES	GND_SMU_AVSS	28 55
D35	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
D35	NO_TEST=YES	PP_3V3ALLSMU	28
D41	NO_TEST=YES	PP_VEINB	41
D48	NO_TEST=YES	GND_CPU_AVDD	48
D50	NO_TEST=YES	VC_AGND	50
D50	NO_TEST=YES	VC_OUTSEN_R	50
D55	NO_TEST=YES	KPVDD2_FMAX	55
D86	NO_TEST=YES	GND_GPU_PVSS	86
D87	NO_TEST=YES	GND_GPU_MPVSS	87
D154	NO_TEST=YES	GND_AUDIO_MIC	153 154

D93	NO_TEST=YES	GND_GPU_TPVSS	93
D93	NO_TEST=YES	GND_GPU_TXVSSR	93
D93	NO_TEST=YES	GND_GPU_VSSDI	93
D93	NO_TEST=YES	GND_GPU_AVSSN	93
D93	NO_TEST=YES	GND_GPU_AVSSQ	93
D93	NO_TEST=YES	GND_GPU_A2VSSN	93
D93	NO_TEST=YES	GND_GPU_A2VSSQ	93
D101	NO_TEST=YES	KOD_L15_GND	98 101
D119	NO_TEST=YES	PP_3V3SBPCI_B9	119
D119	NO_TEST=YES	PP_2V5PWRONSB_B9	119
D122	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
D127	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
D132	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
D132	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
D132	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
D139	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
D139	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
D139	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
D139	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
D139	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
D139	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
D142	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
D150	NO_TEST=YES	GND_AUD_LOAMP	150 154

D62	NO_TEST=YES	GND_NEC_AVSS_R	142
D152	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
D147	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
D55	NO_TEST=YES	KPGND2_FMAX	55
D55	NO_TEST=YES	TDIODE_POS_FMAX	55
D55	NO_TEST=YES	TDIODE_NEG_FMAX	55
D55	NO_TEST=YES	DAGND	55
D55	NO_TEST=YES	INA138_OUT	55
D62	NO_TEST=YES	RAMCLK_AVSS	62
D7 152	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
D7 154	NO_TEST=YES	GND_AUDIO	7 154
D7 152 154	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
D82 97	NO_TEST=YES	KOD_H05_GND	82 97
D82 97	NO_TEST=YES	KOD_K07_GND	82 97
D82 97	NO_TEST=YES	KOD_G10_GND	82 97
D82 97	NO_TEST=YES	KOD_J13_GND	82 97
D82 97	NO_TEST=YES	KOD_L13_GND	82 97
D82 97	NO_TEST=YES	KOD_H08_GND	82 97
D82 84	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
D85	NO_TEST=YES	U8500_GND	85
D150 154	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

E55	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
E57	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
E58	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
E59	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
E60	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
E61	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
E62	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
E63	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
E64	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
E65	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56
E69	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
E71	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
E72	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
E73	NO_TEST=YES	NC_CPU_A1_QACK_L	56
E75	NO_TEST=YES	NC_CPU_B0_QACK_L	56
E74	NO_TEST=YES	NC_CPU_B1_QACK_L	56
E76	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
E78	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
E77	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
E82	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
E104	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
E104	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
E104	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
E104	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
E104	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
E105	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
E105	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
E105	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
E105	NO_TEST=YES	NC_A_AVREG_0	82
E105	NO_TEST=YES	NC_A_AVREG_1	82
E105	NO_TEST=YES	NC_A_AVREG_2	82
E105	NO_TEST=YES	NC_CPU_B_APSYNC	27
E105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
E106	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
E105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
E105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
E106	NO_TEST=YES	NC_J2904_11	29
E106	NO_TEST=YES	NC_J2904_12	29
E104	NO_TEST=YES	NC_NCV1009_1	55
E104	NO_TEST=YES	NC_NCV1009_2	55
E104	NO_TEST=YES	NC_NCV1009_3	55
E104	NO_TEST=YES	NC_NCV1009_4	55
E104	NO_TEST=YES	NC_NCV1009_5	55
E104	NO_TEST=YES	NC_NCV1009_ADJ	55
E106	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
E107	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
E107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
E107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4
E116	NO_TEST=YES	RFBD<38>	88 89
E116	NO_TEST=YES	RFBD<37>	88 89
E116	NO_TEST=YES	RFBD<36>	88 89
E116	NO_TEST=YES	RFBD<34>	88 89
E116	NO_TEST=YES	RFBD<33>	88 89
E116	NO_TEST=YES	RFBD<32>	88 89
E116	NO_TEST=YES	RFBD<31>	88 89
E116	NO_TEST=YES	RFBD<30>	88 89
E117	NO_TEST=YES	RFBD<28>	88 89
E117	NO_TEST=YES	RFBD<27>	88 89
E117	NO_TEST=YES	RFBD<26>	88 89
E117	NO_TEST=YES	RFBD<25>	88 89
E117	NO_TEST=YES	RFBD<23>	88 89
E117	NO_TEST=YES	RFBD<22>	88 89
E117	NO_TEST=YES	RFBD<21>	88 89

E109	NO_TEST=YES	KPVDD2	48 50 55
E109	NO_TEST=YES	KPGND2	48 50 55
E109	NO_TEST=YES	CPU_DIODE_POS	48 55
E109	NO_TEST=YES	CPU_DIODE_NEG	48 55
E110	NO_TEST=YES	FMAXT_P	55
E110	NO_TEST=YES	FMAXT_M	55
E110	NO_TEST=YES	CORE_ISNS_P	55
E110	NO_TEST=YES	CORE_ISNS_M	55
E110	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
E110	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
E110	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
E110	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
E110	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
E110	NO_TEST=YES	NC_I2S2_MCLK	154
E111	NO_TEST=YES	NC_SATA_RXD_N2_C	129
E111	NO_TEST=YES	NC_SATA_RXD_P2_C	129
E111	NO_TEST=YES	NC_SATA_TXD_N2	129
E111	NO_TEST=YES	NC_SATA_TXD_P2	129
E111	NO_TEST=YES	TP_SB<29>	142
E111	NO_TEST=YES	TP_SB<28>	142
E111	NO_TEST=YES	TP_SB<27>	142
E111	NO_TEST=YES	TP_SB<26>	142
E111	NO_TEST=YES	TP_SB<25>	142
E112	NO_TEST=YES	TP_SB<24>	142
E112	NO_TEST=YES	TP_SB<23>	142
E112	NO_TEST=YES	TP_SB<22>	142
E112	NO_TEST=YES	TP_SB<21>	142
E112	NO_TEST=YES	TP_SB<20>	142
E112	NO_TEST=YES	TP_SB<19>	142
E112	NO_TEST=YES	TP_SB<18>	142
E112	NO_TEST=YES	TP_SB<17>	142
E112	NO_TEST=YES	TP_SB<16>	142
E112	NO_TEST=YES	TP_SB<15>	142
E113	NO_TEST=YES	TP_SB<14>	142
E113	NO_TEST=YES	TP_SB<13>	142
E113	NO_TEST=YES	TP_SB<12>	142
E113	NO_TEST=YES	TP_SB<11>	142
E113	NO_TEST=YES	TP_SB<10>	142
E113	NO_TEST=YES	TP_SB<9>	142
E113	NO_TEST=YES	TP_SB<8>	142
E113	NO_TEST=YES	TP_SB<7>	142
E113	NO_TEST=YES	TP_SB<6>	142
E113	NO_TEST=YES	TP_SB<5>	142
E114	NO_TEST=YES	TP_SB<4>	142
E114	NO_TEST=YES	TP_SB<3>	142
E114	NO_TEST=YES	TP_SB<2>	142
E114	NO_TEST=YES	TP_SB<1>	142
E114	NO_TEST=YES	TP_SB<0>	142
E115	NO_TEST=YES	RFBD<61>	88 89
E115	NO_TEST=YES	RFBD<60>	88 89
E115	NO_TEST=YES	RFBD<59>	88 89
E117	NO_TEST=YES	RFBD<57>	88 89
E118	NO_TEST=YES	RFBD<56>	88 89
E118	NO_TEST=YES	RFBD<54>	88 89
E118	NO_TEST=YES	RFBD<53>	88 89
E118	NO_TEST=YES	RFBD<52>	88 89
E118	NO_TEST=YES	RFBD<50>	88 89
E118	NO_TEST=YES	RFBD<49>	88 89
E118	NO_TEST=YES	RFBD<48>	88 89
E118	NO_TEST=YES	RFBD<47>	88 89
E119	NO_TEST=YES	RFBD<45>	88 89
E119	NO_TEST=YES	RFBD<44>	88 89
E119	NO_TEST=YES	RFBD<42>	88 89
E119	NO_TEST=YES	RFBD<41>	88 89
E119	NO_TEST=YES	RFBD<40>	88 89

E119	NO_TEST=YES	RFBD<126>	88 90
E120	NO_TEST=YES	RFBD<125>	88 90
E115	NO_TEST=YES	RFBD<124>	88 90
E120	NO_TEST=YES	RFBD<122>	88 90
E120	NO_TEST=YES	RFBD<121>	88 90
E120	NO_TEST=YES	RFBD<120>	88 90
E120	NO_TEST=YES	RFBD<118>	88 90
E120	NO_TEST=YES	RFBD<117>	88 90
E120	NO_TEST=YES	RFBD<116>	88 90
E121	NO_TEST=YES	RFBD<114>	88 90
E121	NO_TEST=YES	RFBD<113>	88 90
E121	NO_TEST=YES	RFBD<112>	88 90
E121	NO_TEST=YES	RFBD<110>	88 90
E121	NO_TEST=YES	RFBD<109>	88 90
E121	NO_TEST=YES	RFBD<108>	88 90
E121	NO_TEST=YES	RFBD<106>	88 90
E122	NO_TEST=YES	RFBD<105>	88 90
E121	NO_TEST=YES	RFBD<104>	88 90
E122	NO_TEST=YES	RFBD<102>	88 90
E122	NO_TEST=YES	RFBD<101>	88 90
E122	NO_TEST=YES	RFBD<100>	88 90
E122	NO_TEST=YES	RFBD<98>	88 90
E122	NO_TEST=YES	RFBD<97>	88 90
E122	NO_TEST=YES	RFBD<96>	88 90
E122	NO_TEST=YES	RFBD<95>	88 90
E123	NO_TEST=YES	RFBD<94>	88 90
E123	NO_TEST=YES	RFBD<92>	88 90
E123	NO_TEST=YES	RFBD<91>	88 90
E123	NO_TEST=YES	RFBD<90>	88 90
E123	NO_TEST=YES	RFBD<88>	88 90
E123	NO_TEST=YES	RFBD<87>	88 90
E123	NO_TEST=YES	RFBD<86>	88 90
E123	NO_TEST=YES	RFBD<85>	88 90
E124	NO_TEST=YES	RFBD<83>	88 90
E124	NO_TEST=YES	RFBD<82>	88 90
E124	NO_TEST=YES	RFBD<81>	88 90
E124	NO_TEST=YES	RFBD<79>	88 90
E124	NO_TEST=YES	RFBD<78>	88 90
E124	NO_TEST=YES	RFBD<76>	88 90
E124	NO_TEST=YES	RFBD<75>	88 90
E125	NO_TEST=YES	RFBD<74>	88 90
E125	NO_TEST=YES	RFBD<72>	88 90
E125	NO_TEST=YES	RFBD<71>	88 90
E125	NO_TEST=YES	RFBD<70>	88 90
E125	NO_TEST=YES	RFBD<69>	88 90
E125	NO_TEST=YES	RFBD<67>	88 90
E125	NO_TEST=YES	RFBD<66>	88 90
E125	NO_TEST=YES	RFBD<65>	88 90
E126	NO_TEST=YES	RFBD<62>	88 89

E87	NO_TEST=YES	TP_FBBCS1_L	87
E82	NO_TEST=YES	AUD_4V5_FB	154
E83	NO_TEST=YES	ITS_RUNNING	7
E83	NO_TEST=YES	LED801_1	8
E83	NO_TEST=YES	LED802_1	8
E84	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
E84	NO_TEST=YES	Q800_D	8
E84	NO_TEST=YES	Q800_G	8
E84	NO_TEST=YES	Q801_B	8
E84	NO_TEST=YES	Q802_B	8
E85	NO_TEST=YES	Q802_E	8
E85	NO_TEST=YES	Q803_B	8
E142	NO_TEST=YES	TP_USB2_PWREN<0>	143
E142	NO_TEST=YES	TP_USB2_PWREN<1>	143
E87	NO_TEST=YES	TP_SB_FSTEST	24
E87	NO_TEST=YES	TP_SB_PLLTEST	24
E134	NO_TEST=YES	TP_USB2_PWREN<2>	143
E135	NO_TEST=YES	TP_USB2_PWREN<3>	143
E134	NO_TEST=YES	TP_USB2_PWREN<4>	143
E135	NO_TEST=YES	TP_NEC_NTEST1	122
E135	NO_TEST=YES	TP_NEC_SMC	122
E135	NO_TEST=YES	TP_NEC_SMI_L	122
E136	NO_TEST=YES	TP_NEC_SRCLK	122
E136	NO_TEST=YES	TP_NEC_SRMOD	122
E136	NO_TEST=YES	TP_NEC_TEST	122
E88	NO_TEST=YES	UATA_DASP_L_DS	129
E129	NO_TEST=YES	RFBD<19>	88 89
E129	NO_TEST=YES	RFBD<18>	88 89
E129	NO_TEST=YES	RFBD<16>	88 89
E129	NO_TEST=YES	RFBD<15>	88 89
E129	NO_TEST=YES	RFBD<14>	88 89
E129	NO_TEST=YES	RFBD<13>	88 89
E127	NO_TEST=YES	RFBD<11>	88 89
E127	NO_TEST=YES	RFBD<10>	88 89
E127	NO_TEST=YES	RFBD<8>	88 89
E127	NO_TEST=YES	RFBD<7>	88 89
E127	NO_TEST=YES	RFBD<6>	88 89
E127	NO_TEST=YES	RFBD<5>	88 89
E127	NO_TEST=YES	RFBD<3>	88 89
E128	NO_TEST=YES	RFBD<2>	88 89
E128	NO_TEST=YES	RFBD<1>	88 89
E128	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
E128	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
E129	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<39>	61 68 70
E130	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
E131	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
E131	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
E131	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
E131	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
E131	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
E131	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
E131	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
E131	NO_TEST=YES	RAM_DQ_R<26>	61 68 69
E132	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
E132	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
E132	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
E132	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
E132	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
E132	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
E133	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
E133	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
E133	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
E133	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
E133	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
E133	NO_TEST=YES	RAM_DQ_R<11>	61 68 69
E134	NO_TEST=YES	RAM_DQ_R<10>	61 68 69
E134	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
E134	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
E134	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
E134	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
E135	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
E134	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
E135	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

E108	FUNC_TEST=TRUE	PPVCORE_CPU	50
E108	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
E108	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
E108	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
E109	FUNC_TEST=TRUE	POWER_BUTTON_L	29
E109	FUNC_TEST=TRUE	RESET_BUTTON_L	29
E109	FUNC_TEST=TRUE	SMU_RESET_L	28 29
E109	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

E139	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
E139	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
E139	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
E139	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
E139	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
E139	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
E109	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29

PP1V2_ALL PP3V3_ALL PP5V_ALL

7 PP1V2_ALL FUNC_TEST=TRUE
7 PP3V3_ALL FUNC_TEST=TRUE
7 PP5V_ALL FUNC_TEST=TRUE

PP1V8_RUN PP2V5_RUN PP3V3_RUN PP12V_RUN

7 PP1V8_RUN FUNC_TEST=TRUE
7 PP2V5_RUN FUNC_TEST=TRUE
7 PP3V3_RUN FUNC_TEST=TRUE
7 PP12V_RUN FUNC_TEST=TRUE

PP1V5_PWRON

7 PP1V5_PWRON FUNC_TEST=TRUE

GND FUNC_TEST=TRUE

FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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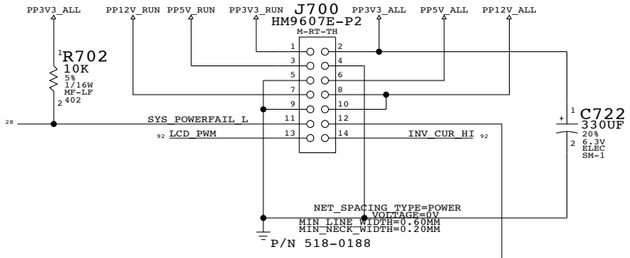
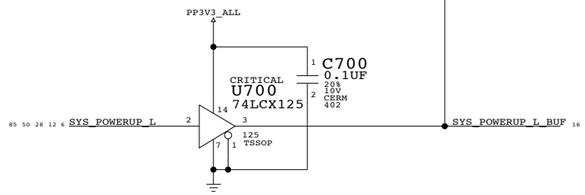
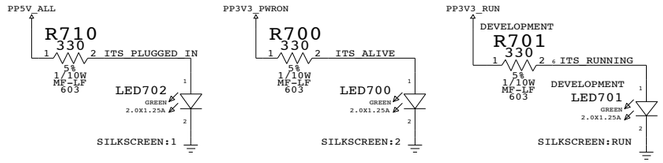
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 6 OF 154	

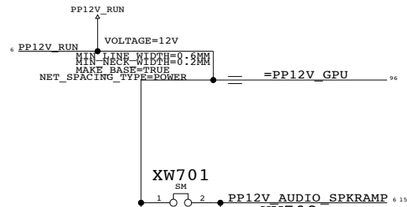


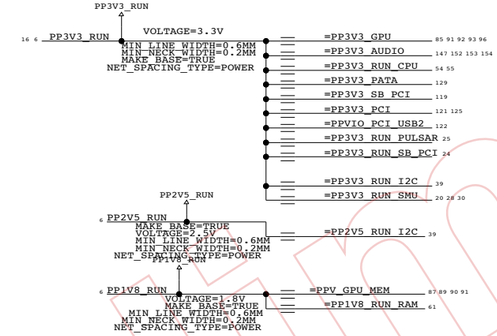




RUN RAILS

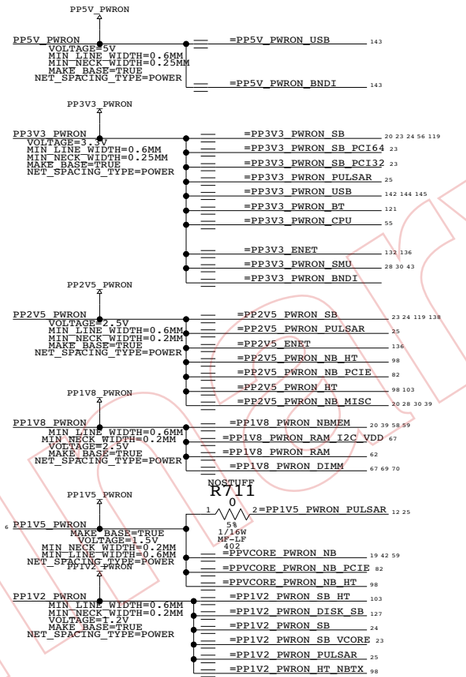
ONLY ON IN RUN





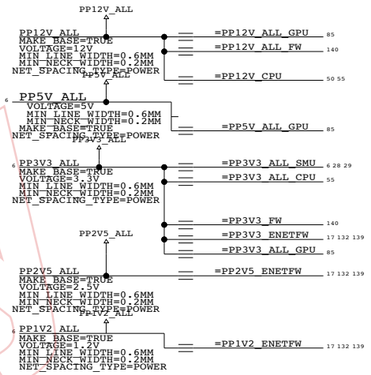
PWRON RAILS

ON IN RUN AND SLEEP

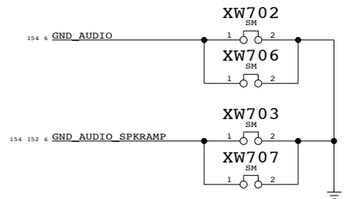


ALL RAILS

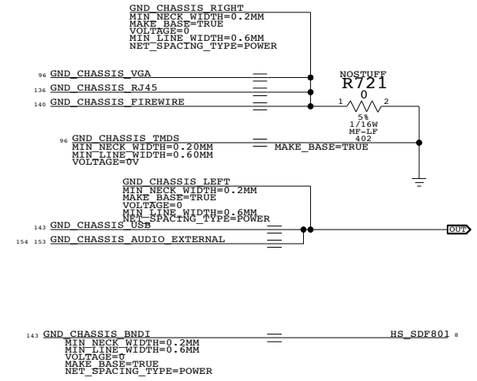
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



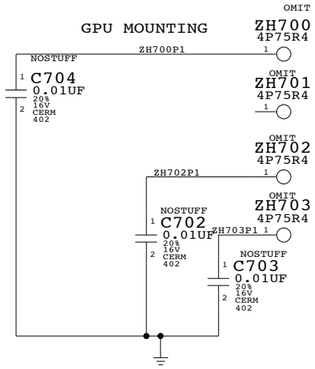
GND RAILS



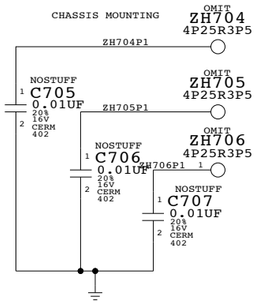
CHASSIS GND



GPU MOUNTING



CHASSIS MOUNTING



POWER CONN / ALIAS

SYNC_MASTER=M33-PC SYNC_DATE=05/19/2005

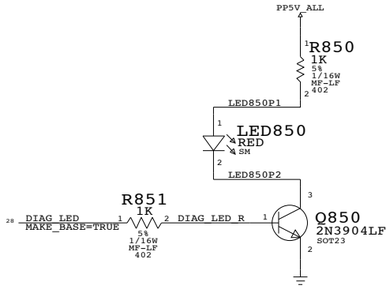
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

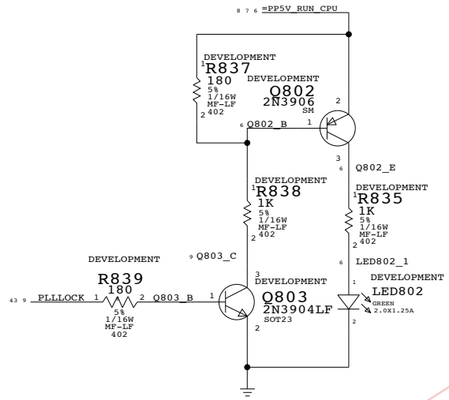
SCALE	SHT	OF
NONE	7	154

DIAG LED

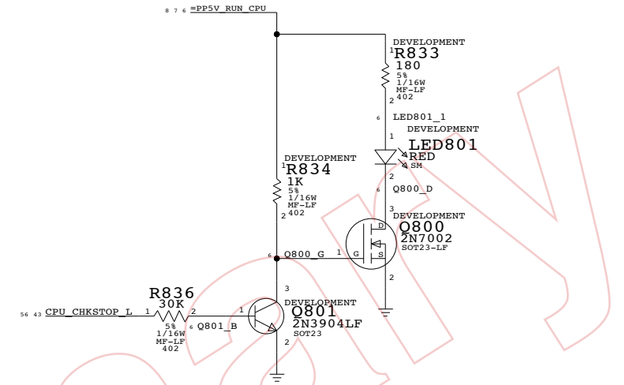
(OVERTEMP LED)



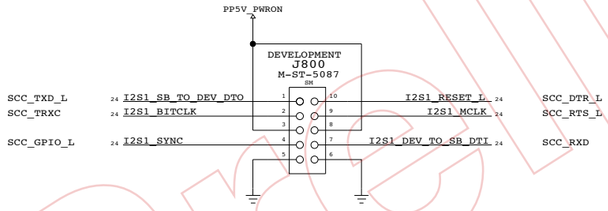
PLL LOCK LED



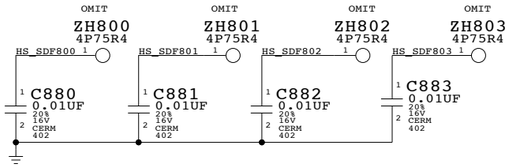
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 8 OF 154	

8	7	6	5	4	3	2	1

D

C

B

A

E1	NO_TEST=YES	ENET_TXD_R<7>	130 131
E2	NO_TEST=YES	ENET_TXD_R<6>	130 131
E3	NO_TEST=YES	ENET_TXD_R<5>	130 131
E4	NO_TEST=YES	ENET_TXD_R<4>	130 131
E5	NO_TEST=YES	ENET_TXD_R<3>	130 131
E6	NO_TEST=YES	ENET_TXD_R<2>	130 131
E7	NO_TEST=YES	ENET_TXD_R<1>	130 131
E8	NO_TEST=YES	ENET_TXD_R<0>	130 131
E9	NO_TEST=YES	ENET_TXD<7>	130 131 132
E10	NO_TEST=YES	ENET_TXD<6>	130 131 132
E12	NO_TEST=YES	ENET_TXD<5>	130 131 132
E11	NO_TEST=YES	ENET_TXD<4>	130 131 132
E13	NO_TEST=YES	ENET_TXD<3>	130 131 132
E14	NO_TEST=YES	ENET_TXD<2>	130 131 132
E15	NO_TEST=YES	ENET_TXD<1>	130 131 132
E16	NO_TEST=YES	ENET_TXD<0>	130 131 132
E18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
E17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
E19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
E20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
E21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
E22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
E24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
E23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
E25	NO_TEST=YES	ENET_RXD<7>	130 131
E26	NO_TEST=YES	ENET_RXD<6>	130 131
E27	NO_TEST=YES	ENET_RXD<5>	130 131
E28	NO_TEST=YES	ENET_RXD<4>	130 131
E30	NO_TEST=YES	ENET_RXD<3>	130 131
E29	NO_TEST=YES	ENET_RXD<2>	130 131
E31	NO_TEST=YES	ENET_RXD<1>	130 131
E32	NO_TEST=YES	ENET_RXD<0>	130 131
E33	NO_TEST=YES	ENET_TX_EN_R	130 131
E34	NO_TEST=YES	ENET_TX_ER_R	130 131
E36	NO_TEST=YES	ENET_TX_EN	130 131 132
E35	NO_TEST=YES	ENET_TX_ER	130 131 132
E37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
E38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
E39	NO_TEST=YES	NC_CPU_AFN	56
E40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
E42	NO_TEST=YES	NC_PSRO	56
E41	NO_TEST=YES	NC_PSRO_ENABLE	56
E43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
E44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
E45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
E46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
E48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
E47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
E49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
E50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
E51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
E52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
E54	NO_TEST=YES	NC_SMU_SER_SEL	31
E53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
E55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
E56	NO_TEST=YES	TP_VESTA_AN_EN	132
E57	NO_TEST=YES	TP_VESTA_DNC_C9	17
E58	NO_TEST=YES	TP_VESTA_DNC_E9	17
E60	NO_TEST=YES	TP_VESTA_EN_10B	132
E59	NO_TEST=YES	TP_VESTA_ER	132
E61	NO_TEST=YES	TP_VESTA_F1000	132
E62	NO_TEST=YES	TP_VESTA_FDX	132
E63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
E64	NO_TEST=YES	TP_VESTA_HUB	132
E66	NO_TEST=YES	TP_VESTA_LINK1_L	132
E65	NO_TEST=YES	TP_VESTA_LINK2_L	132
E67	NO_TEST=YES	TP_VESTA_MANMS	132
E68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
E69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
E70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
E72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
E71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
E73	NO_TEST=YES	TP_VESTA_RBC0	132
E74	NO_TEST=YES	TP_VESTA_RBC1	132
E75	NO_TEST=YES	TP_VESTA_REGCTL1	17
E76	NO_TEST=YES	TP_VESTA_REGCTL2	17
E78	NO_TEST=YES	TP_VESTA_REGSEN1	17
E77	NO_TEST=YES	TP_VESTA_REGSEN2	17
E79	NO_TEST=YES	TP_VESTA_REGSUP1	17
E80	NO_TEST=YES	TP_VESTA_REGSUP2	17
E81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
E82	NO_TEST=YES	TP_VESTA_SPD0	132
E84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
E83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
E85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
E86	NO_TEST=YES	TP_VESTA_TEST<0>	132
E87	NO_TEST=YES	TP_VESTA_TEST<1>	132
E88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
E90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
E89	NO_TEST=YES	TP_VESTA_TVCO	132
E222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
E223	NO_TEST=YES	TP_VESTA_FAVDDL	139
E224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
E225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

E91	NO_TEST=YES	TP_VESTA_TVCO_24	139
E92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
E93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
E94	NO_TEST=YES	TP_NB_APSYNC	44
E95	NO_TEST=YES	TP_SB_WATCHDOG	24
E96	NO_TEST=YES	NC_CPU_TBEN_CLK	27
E97	NO_TEST=YES	NC_J3108_10	31
E98	NO_TEST=YES	NC_J3108_11	31
E99	NO_TEST=YES	NC_J3108_12	31
E100	NO_TEST=YES	NC_J3108_8	31
E101	NO_TEST=YES	NC_J3108_9	31
E102	NO_TEST=YES	NC_JTAGMUX_3	30
E106	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

E107	NO_TEST=YES	Q803_C	8
E109	NO_TEST=YES	PLLLOCK	8 43
E111	NO_TEST=YES	LED_PP1V8_RUN_P	11
E112	NO_TEST=YES	LED_PP1V8_RUN_N	11
E110	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
E113	NO_TEST=YES	LED_PP1V5_RUN_N	12
E111	NO_TEST=YES	LED_PP1V5_RUN_P	12
E114	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
E120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
E121	NO_TEST=YES	LED_PP1V2_RUN_N	13
E122	NO_TEST=YES	LED_PP1V2_RUN_P	13
E123	NO_TEST=YES	KP_V<1>	55
E124	NO_TEST=YES	KP_V<2>	55
E125	NO_TEST=YES	CPU_SENSE_KP_V	55
E126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
E127	NO_TEST=YES	NB_PLL_OUT_TRG	59
E128	NO_TEST=YES	PP5V_T555	92
E131	NO_TEST=YES	T555_DISC	92
E132	NO_TEST=YES	T555_THRES	92
E129	NO_TEST=YES	T555_OUT	92
E133	NO_TEST=YES	T555_PWM	92
E134	NO_TEST=YES	PP3V3_GPU_TSENSE	
E135	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
E136	NO_TEST=YES	TSENSE_GPU_ADD0	93
E138	NO_TEST=YES	TSENSE_GPU_ADD1	93
E137	NO_TEST=YES	GPU_DIODE_PLUS	93
E139	NO_TEST=YES	GPU_DIODE_MINUS	93
E139	NO_TEST=YES	LED8700_P	136
E140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

E141	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
E142	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
E143	NO_TEST=YES	CPU_A_APSYNC_R	26
E144	NO_TEST=YES	CPU_B_APSYNC_R	26
E145	NO_TEST=YES	NB_APSYNC_R	26
E146	NO_TEST=YES	HT_SB_REFCLK_R	26
E147	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
E148	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
E149	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
E150	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
E151	NO_TEST=YES	NB_PMR_CLK_P_R	26
E152	NO_TEST=YES	NB_PMR_CLK_N_R	26
E153	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
E154	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
E155	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
E156	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
E157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
E158	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
E159	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
E160	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
E161	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
E162	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
E163	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
E164	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
E165	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
E166	NO_TEST=YES	QUA0_REF_25MHZ_R	26
E167	NO_TEST=YES	SB_CLK25M_SATA_R	26
E168	NO_TEST=YES	QUA1_REF_25MHZ_R	26
E169	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
E170	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
E171	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
E172	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

E177	NO_TEST=YES	100M_N<0>	82 97
E178	NO_TEST=YES	100M_P<0>	82 97
E179	NO_TEST=YES	CKA_N<0>	84 97
E180	NO_TEST=YES	CKA_P<0>	84 97
E177	NO_TEST=YES	HT_NB_N<0>	98 101
E179	NO_TEST=YES	HT_NB_P<0>	98 101
E179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
E180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
E185	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
E187	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
E186	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
E188	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
E189	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
E189	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
E187	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
E189	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
E188	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	82 84 97
E190	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	82 84 97
E190	NO_TEST=YES	UATA_DA<0>	127 129
E190	NO_TEST=YES	UATA_DD<1>	127 129
E190	NO_TEST=YES	UATA_DD<14>	127 129
E190	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	82 84 97
E190	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	82 84 97
E197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	82 97
E198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	82 97
E199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	82 84 97
E200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	82 84 97
E204	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	82 97
E207	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	82 97
E205	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	82 97
E206	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	82 97
E208	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	82 97
E206	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
E208	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
E209	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
E210	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
E209	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
E211	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
E215	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
E216	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
E213	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
E215	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
E214	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	43 56
E216	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	43 56
E213	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
E217	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
E222	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	43 56
E220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

E224	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
E222	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
E226	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
E224	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
E230	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24
E232	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
E234	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
E233	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
E231	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
E235	FUNC_TEST=TRUE	JTAG_NB_TRST_L	
E231	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	
E234	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	
E233	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	
E234	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	
E241	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	
E244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
E246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
E245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
E244	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
E247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47
E240	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
E240	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
E247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

FUNC TEST 2 OF 2

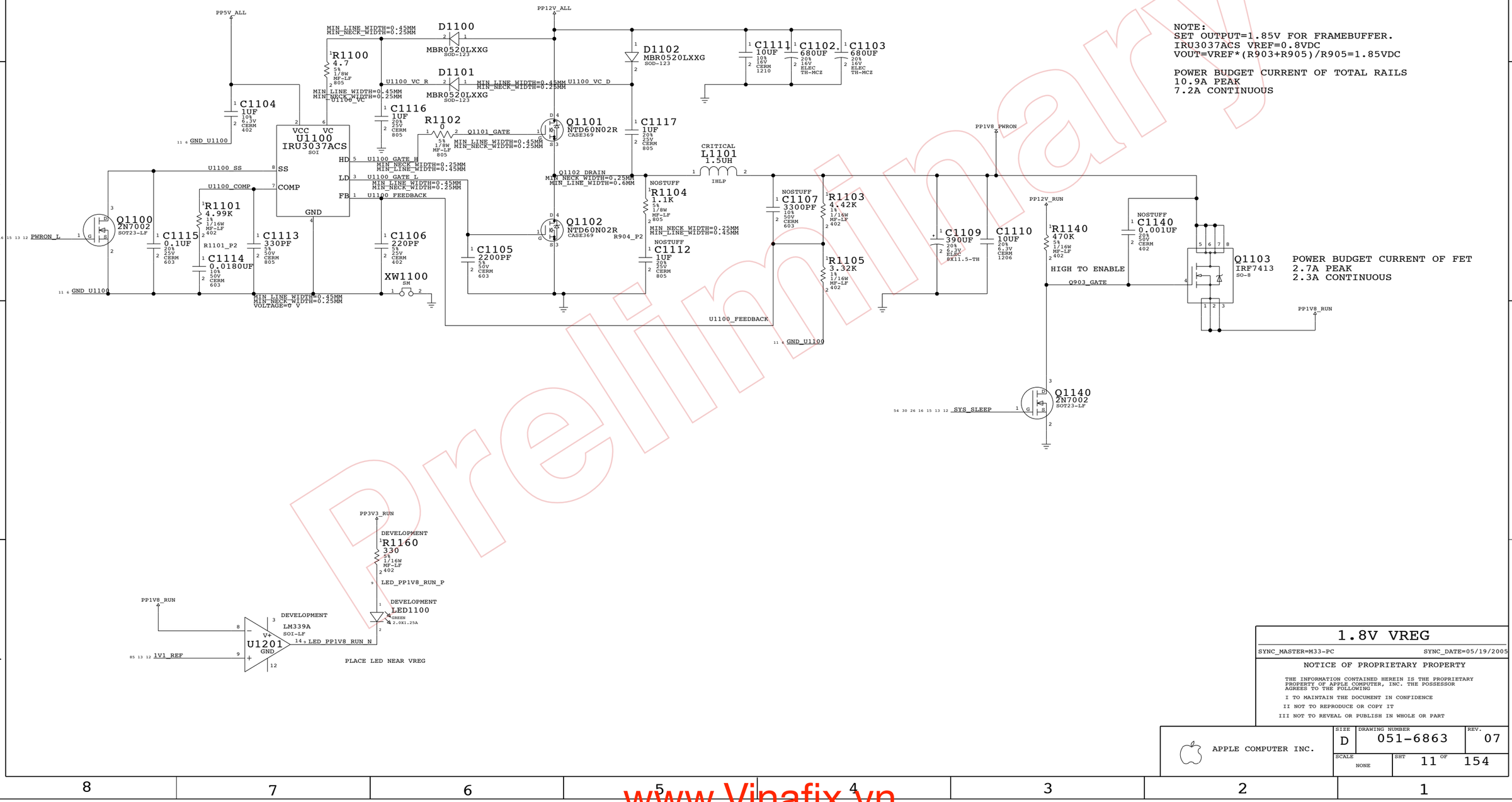
SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE NONE SHT 9 OF 154

1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
10.9A PEAK
7.2A CONTINUOUS

POWER BUDGET CURRENT OF FET
2.7A PEAK
2.3A CONTINUOUS

1.8V VREG		
SYNC_MASTER=M33-PC	SYNC_DATE=05/19/2005	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
	SCALE: NONE	SHT 11 OF 154	

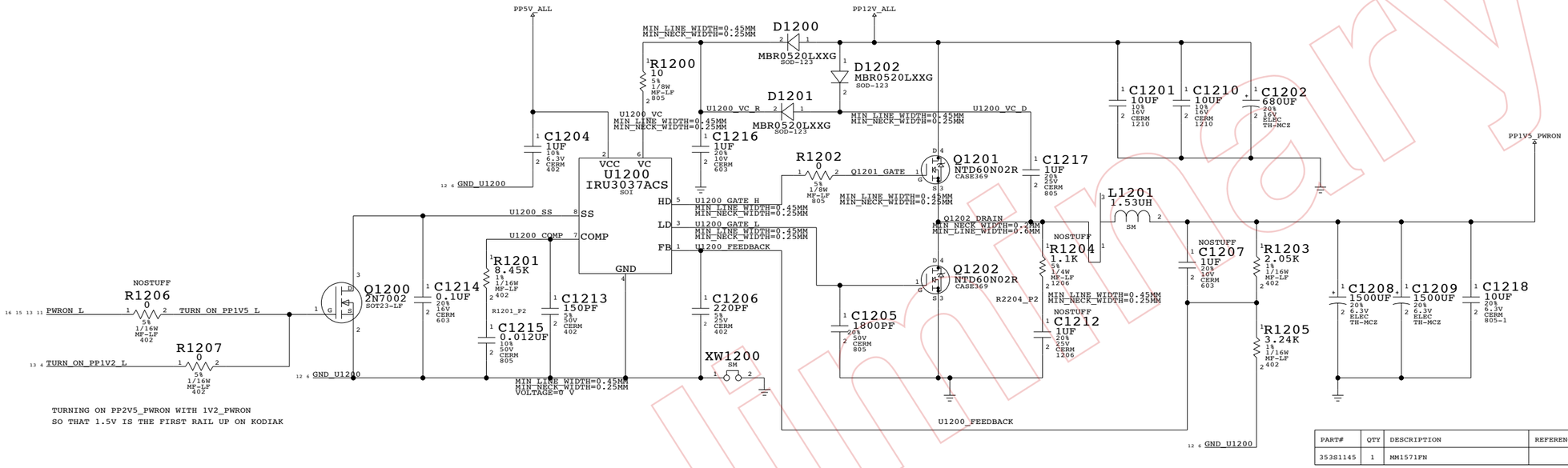
KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.30VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

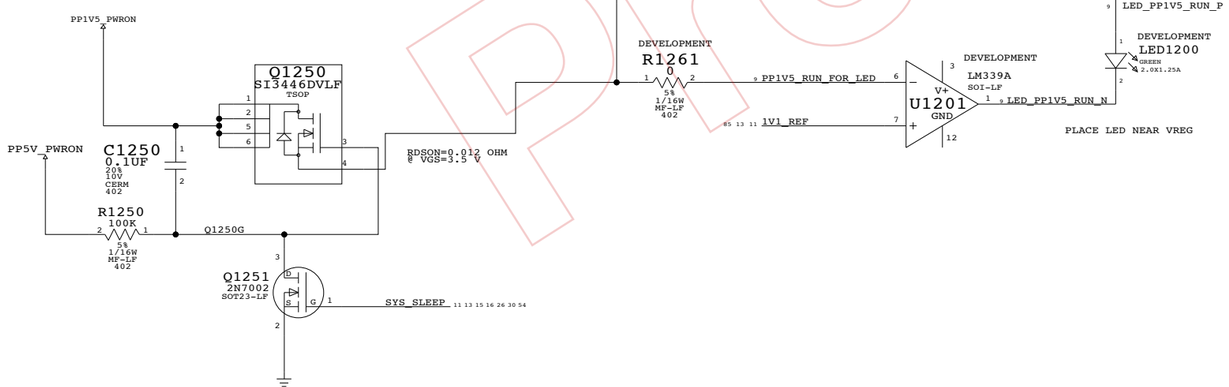
1.35V R1205=2.87K
1.30V R1205=3.24K
1.25V R1205=4.02K



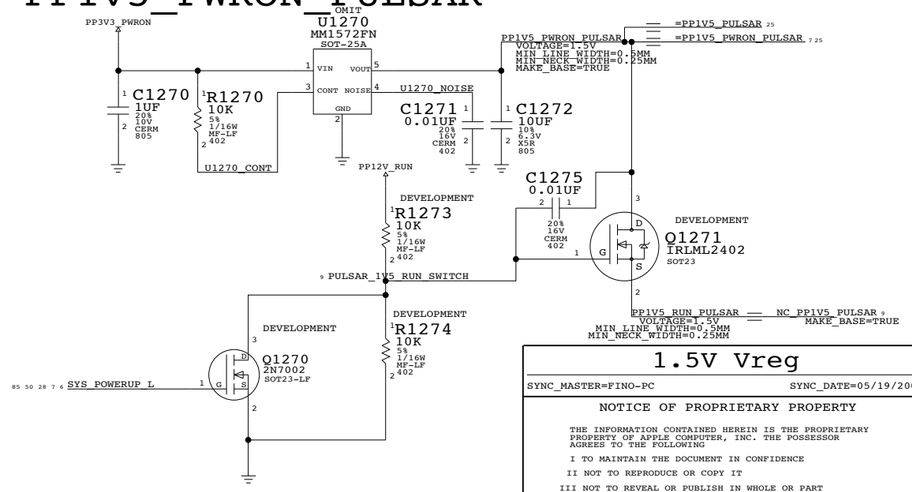
TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1145	1	MM1571FN	U1270	CRITICAL	

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW



PP1V5_PWRON_PULSAR



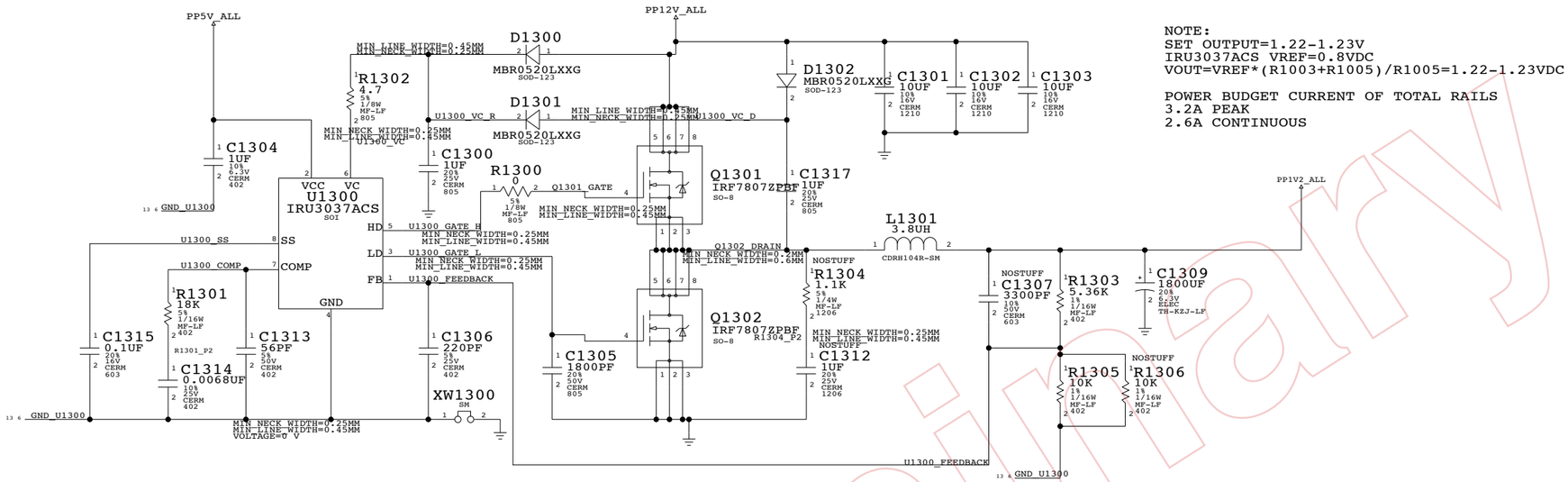
1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

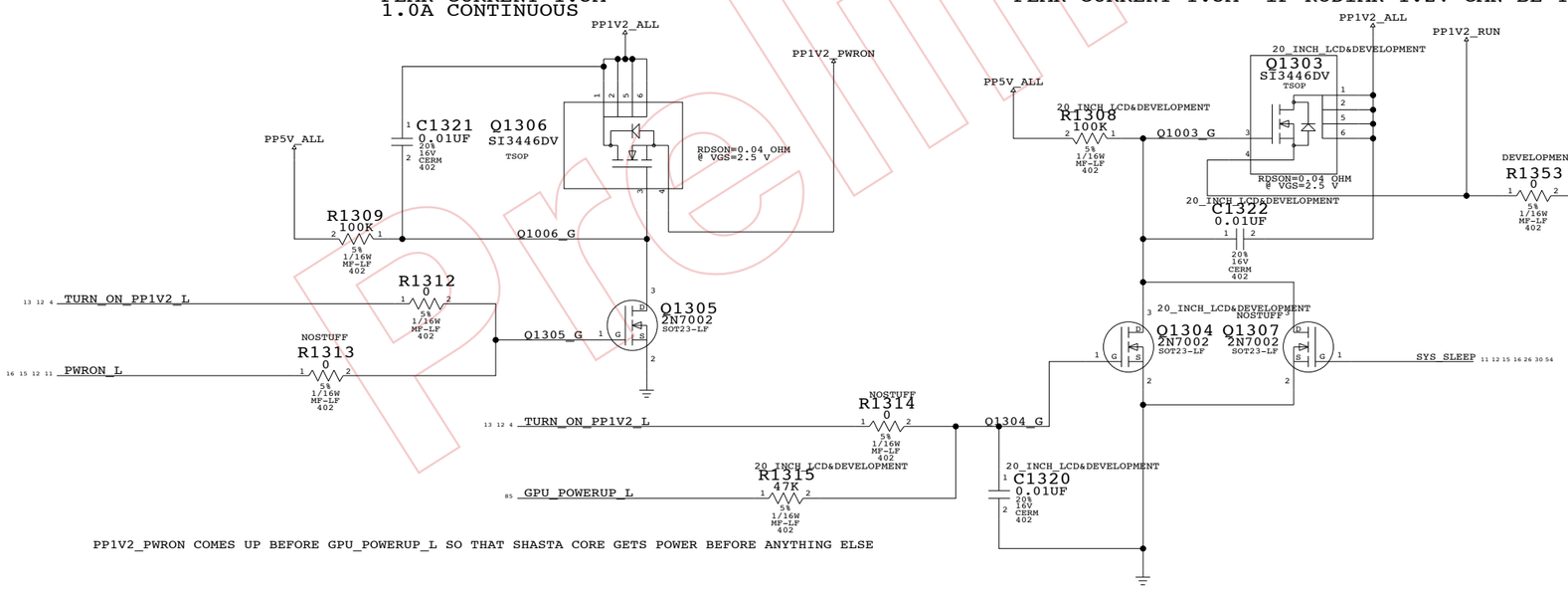
SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 12 OF 154	

PP1V2_ALL VOLTAGE REGULATOR



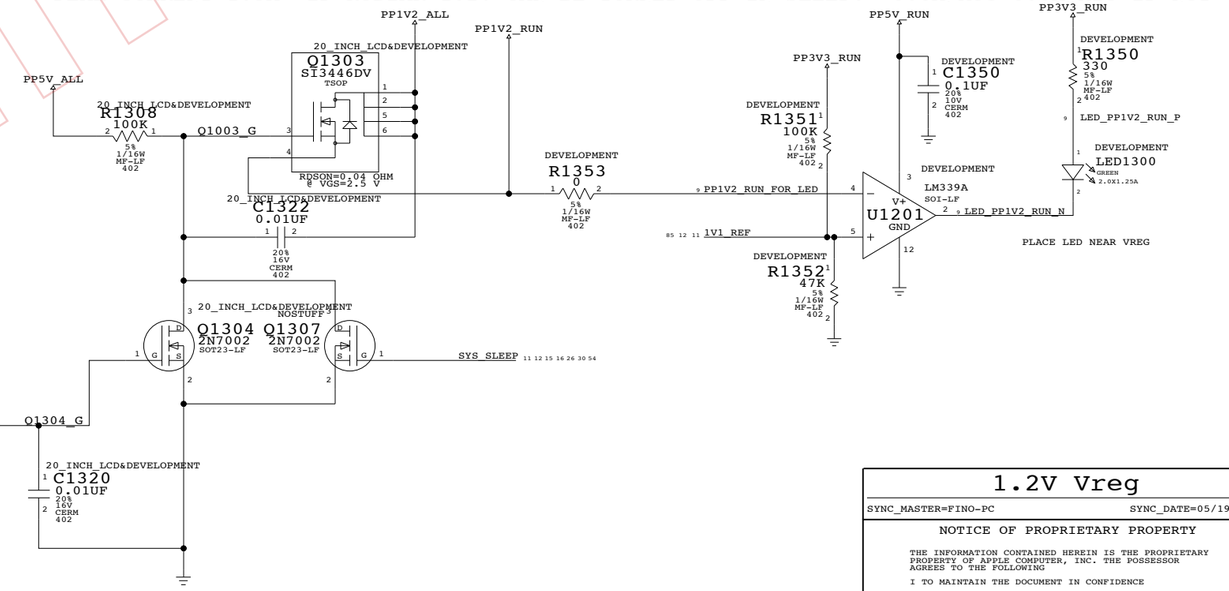
PP1V2_PWRON FET SWITCH

PEAK CURRENT 1.3A
1.0A CONTINUOUS



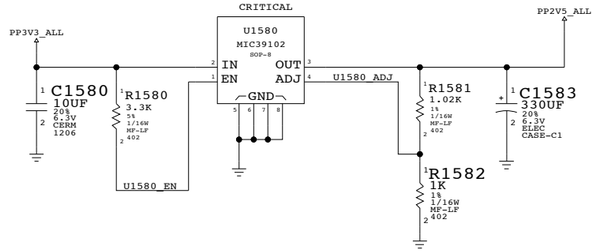
PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg			
SYNC_MASTER=FINO-PC	SYNC_DATE=05/19/2005		
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. 07
	SCALE NONE	SHT 13 OF 154	

PP2V5_ALL VOLTAGE REGULATOR

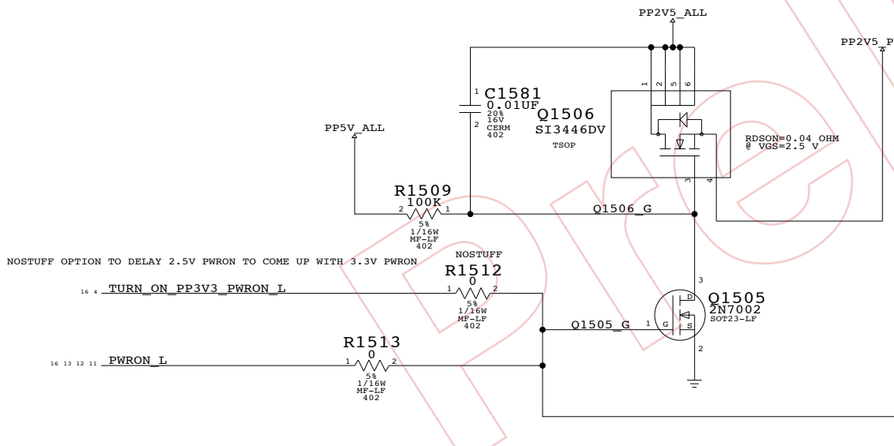


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

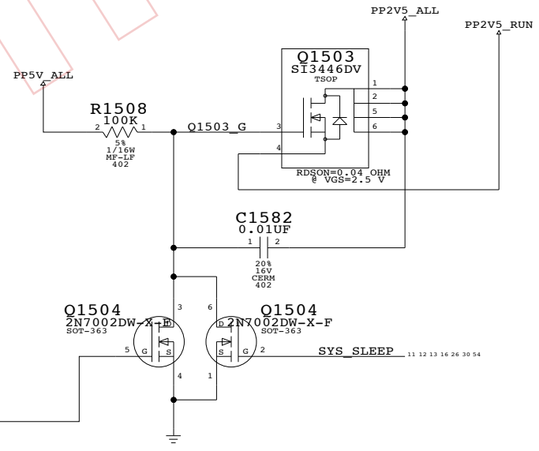
PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A

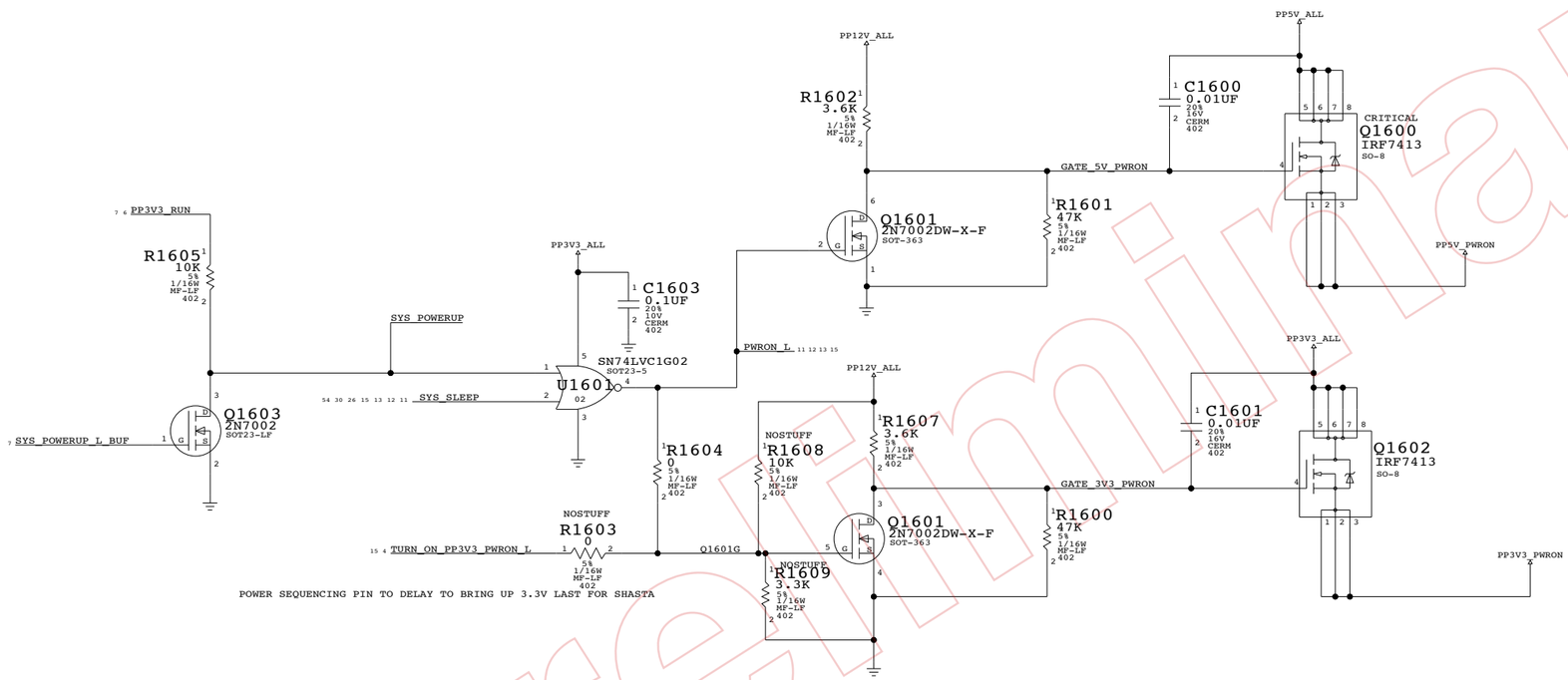


2.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 15 OF 154	



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

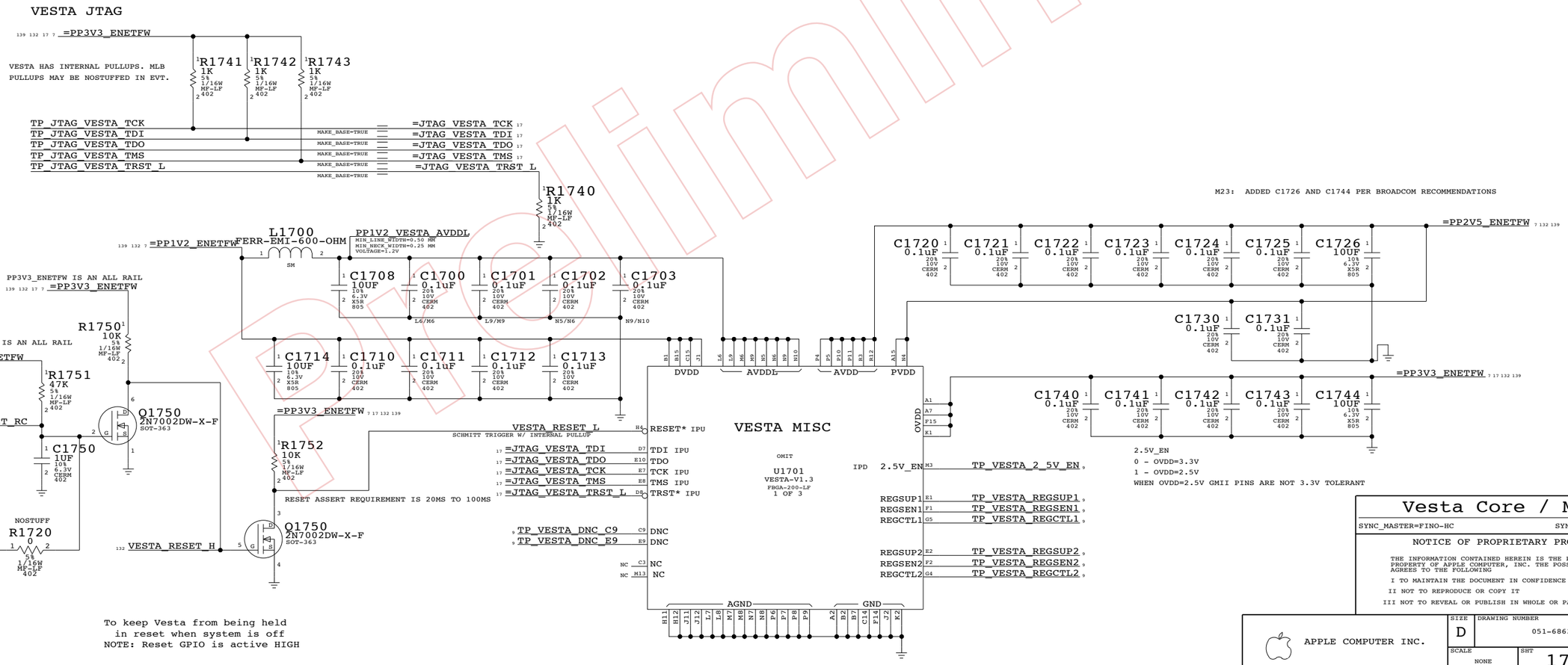
SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 16 OF 154	

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.



Vesta Core / Misc

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 17 OF 154	

59A6 42A4 20A8 3A4 =PPVCORE_PWRON_NB

KODIAK CORE
PP1900
P4MM
1.6V PP 1
Q63 = PP1V6

SEE_TABLE

U1900
KODIAK-ASIC-040812
CORE & PCI-E POWER
BGA
(9 OF 10)
(1.6V-1.2V)

N15	VDD_CORE	CORE_GND	N14
P17	VDD_CORE	CORE_GND	P16
P21	VDD_CORE	CORE_GND	P20
R14	VDD_CORE	CORE_GND	R15
R18	VDD_CORE	CORE_GND	R19
R22	VDD_CORE	CORE_GND	R23
T16	VDD_CORE	CORE_GND	T17
T20	VDD_CORE	CORE_GND	T21
U15	VDD_CORE	CORE_GND	U14
U19	VDD_CORE	CORE_GND	U18
V17	VDD_CORE	CORE_GND	V16
V21	VDD_CORE	CORE_GND	V20
W14	VDD_CORE	CORE_GND	W15
W18	VDD_CORE	CORE_GND	W19
W22	VDD_CORE	CORE_GND	W23
Y16	VDD_CORE	CORE_GND	Y17
Y20	VDD_CORE	CORE_GND	Y21
AA15	VDD_CORE	CORE_GND	AA14
AA19	VDD_CORE	CORE_GND	AA18
AA23	VDD_CORE	CORE_GND	AA22
AB17	VDD_CORE	CORE_GND	AB16
AB21	VDD_CORE	CORE_GND	AB20
AC14	VDD_CORE	CORE_GND	AC15
AC18	VDD_CORE	CORE_GND	AC19
AC22	VDD_CORE	CORE_GND	AC23

C1900 1UF 10% 6.3V CERM 402
C1901 1UF 10% 6.3V CERM 402
C1902 1UF 10% 6.3V CERM 402
C1903 1UF 10% 6.3V CERM 402
C1904 1UF 10% 6.3V CERM 402
C1905 1UF 10% 6.3V CERM 402
C1906 1UF 10% 6.3V CERM 402
C1907 1UF 10% 6.3V CERM 402
C1908 1UF 10% 6.3V CERM 402
C1909 1UF 10% 6.3V CERM 402
C1910 1UF 10% 6.3V CERM 402
C1911 1UF 10% 6.3V CERM 402
C1912 1UF 10% 6.3V CERM 402
C1913 1UF 10% 6.3V CERM 402
C1914 1UF 10% 6.3V CERM 402
C1915 1UF 10% 6.3V CERM 402
C1916 1UF 10% 6.3V CERM 402
C1917 1UF 10% 6.3V CERM 402
C1918 1UF 10% 6.3V CERM 402
C1919 1UF 10% 6.3V CERM 402
C1920 1UF 10% 6.3V CERM 402
C1921 1UF 10% 6.3V CERM 402
C1922 1UF 10% 6.3V CERM 402
C1923 1UF 10% 6.3V CERM 402
C1924 1UF 10% 6.3V CERM 402

KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07
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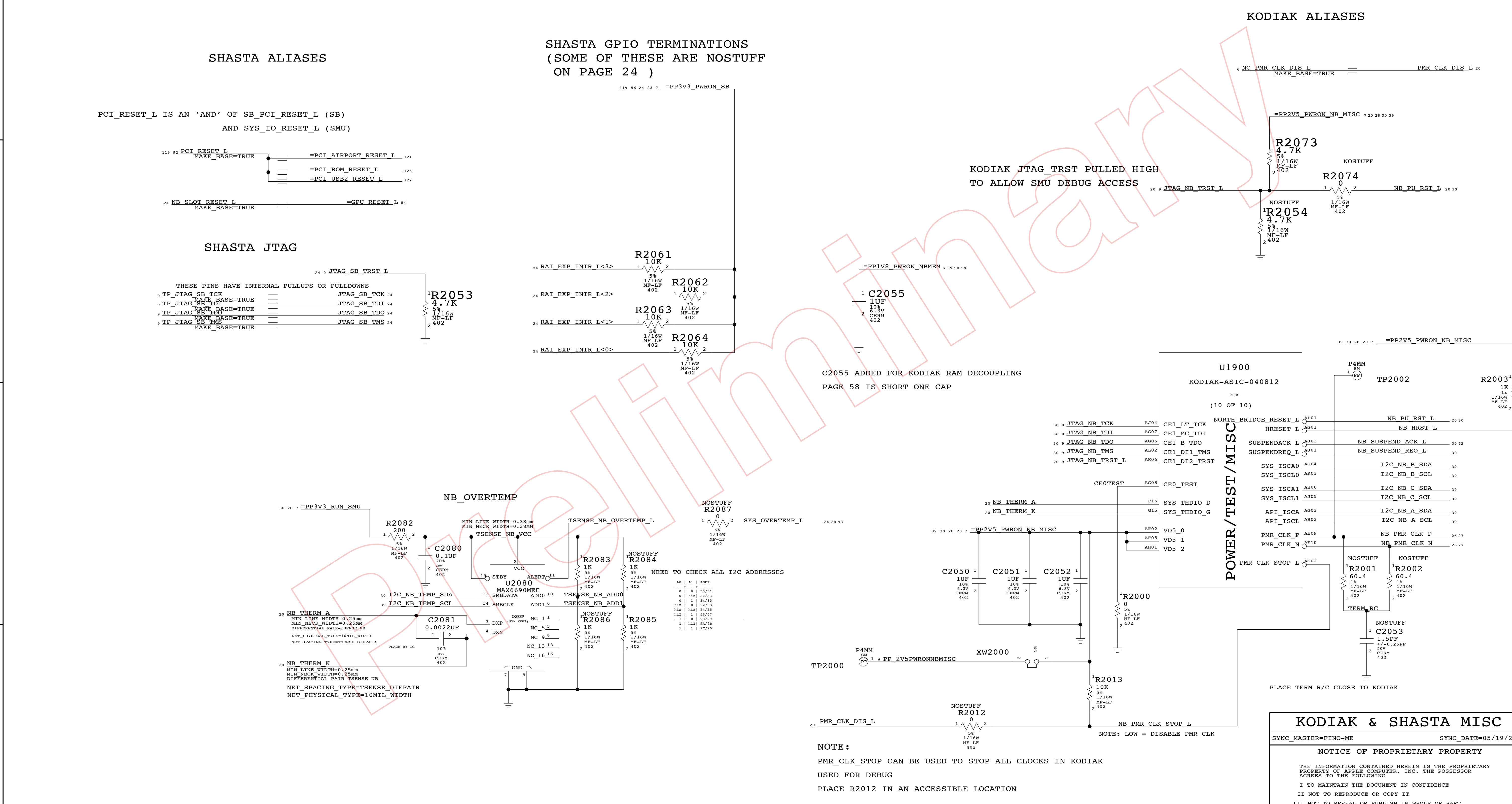
DRAWING


SHASTA ALIASES
PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)
PCI_RESET_L
MAKE_BASE=TRUE
=PCI_AIRPORT_RESET_L
=PCI_ROM_RESET_L
=PCI_USB2_RESET_L
NB_SLOT_RESET_L
MAKE_BASE=TRUE
=GPU_RESET_L
SHASTA JTAG
JTAG_SB_TRST_L
THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS
TP_JTAG_SB_TCK
TP_JTAG_SB_TDI
TP_JTAG_SB_TDO
TP_JTAG_SB_TMS
MAKE_BASE=TRUE
JTAG_SB_TCK
JTAG_SB_TDI
JTAG_SB_TDO
JTAG_SB_TMS
R2053
4.7K
SHASTA GPIO TERMINATIONS
(SOME OF THESE ARE NOSTUFF
ON PAGE 24)
=PP3V3_PWRON_SB
RAI_EXP_INTR_L<3>
RAI_EXP_INTR_L<2>
RAI_EXP_INTR_L<1>
RAI_EXP_INTR_L<0>
R2061
10K
R2062
10K
R2063
10K
R2064
10K
=PP1V8_PWRON_NBMEM
C2055
1UF
C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP
KODIAK ALIASES
NC_PMR_CLK_DIS_L
MAKE_BASE=TRUE
PMR_CLK_DIS_L
=PP2V5_PWRON_NB_MISC
R2073
4.7K
KODIAK JTAG_TRST PULLED HIGH
TO ALLOW SMU DEBUG ACCESS
JTAG_NB_TRST_L
NOSTUFF
R2074
0
NB_PU_RST_L
R2054
4.7K
NB_OVERTEMP
=PP3V3_RUN_SMU
R2082
200
C2080
0.1UF
TSENSE_NB_VCC
TSENSE_NB_OVERTEMP_L
NOSTUFF
R2087
0
SYS_OVERTEMP_L
U2080
MAX6690MEE
I2C_NB_TEMP_SDA
I2C_NB_TEMP_SCL
TSENSE_NB_ADD0
TSENSE_NB_ADD1
R2083
1K
NOSTUFF
R2084
1K
NOSTUFF
R2086
1K
R2085
1K
NEED TO CHECK ALL I2C ADDRESSES
NB_THERM_A
C2081
0.0022UF
NB_THERM_K
NET_SPACING_TYPE=TSENSE_DIFPAIR
NET_PHYSICAL_TYPE=10MIL_WIDTH
U1900
KODIAK-ASIC-040812
(10 OF 10)
POWER/TEST/MISC
JTAG_NB_TCK
JTAG_NB_TDI
JTAG_NB_TDO
JTAG_NB_TMS
JTAG_NB_TRST_L
CEOTEST
NB_THERM_A
NB_THERM_K
=PP2V5_PWRON_NB_MISC
NORTH_BRIDGE_RESET_L
HRESET_L
SUSPENDACK_L
SUSPENDREQ_L
SYS_ISCA0
SYS_ISCL0
SYS_ISCA1
SYS_ISCL1
API_ISCA
API_ISCL
PMR_CLK_P
PMR_CLK_N
PMR_CLK_STOP_L
NB_PU_RST_L
NB_HRST_L
NB_SUSPEND_ACK_L
NB_SUSPEND_REQ_L
I2C_NB_B_SDA
I2C_NB_B_SCL
I2C_NB_C_SDA
I2C_NB_C_SCL
I2C_NB_A_SDA
I2C_NB_A_SCL
NB_PMR_CLK_P
NB_PMR_CLK_N
TP2002
R2003
1K
C2050
1UF
C2051
1UF
C2052
1UF
R2000
0
NOSTUFF
R2001
60.4
NOSTUFF
R2002
60.4
TERM_RC
NOSTUFF
C2053
1.5PF
PLACE TERM R/C CLOSE TO KODIAK
TP2000
PP_2V5PWRONNBMISC
XW2000
R2013
10K
NOSTUFF
R2012
0
PMR_CLK_DIS_L
NB_PMR_CLK_STOP_L
NOTE: LOW = DISABLE PMR_CLK
NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

3B2 =PP1V2_PWRON_SB_VCORE

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314
0.1uF 20% 10V CERM 402

149A3 120C4 119A3 29C7 29B4 24D2 24C3 24B7 24A6 20D2 3A3 154D2 =PP3V3_PWRON_SB

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339
0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.1
BGA-LP
(1 OF 8)

POWER

SEE_TABLE

VDDC
VDDIO33
GND

Shasta max (est 06/30/03) current:

DIGITAL	1.2V	950 mA (1175 mW)
ANALOG12	1.2V	400 mA (760 mW)
VDDPs	2.5V	100 mA (250 mW)
I/O 2.5	2.5V	20 mA (60 mW)
I/O 3.3	3.3V	220 mA (770 mW)
Total:		3015 mW

XW2300 SM 2 1 PP_1V2PWRONSBVCORE P4MM SM PP PP2300
XW2303 SM 2 1 PP_3V3PWRONSBPCI64 P4MM SM PP PP2303
XW2304 SM 2 1 NO_TEST=YES PP_2V5PWRONSB P4MM SM PP PP2304

VDDO25 VIO1 VIO2 VDDP_KL

=PP2V5_PWRON_SB 3C1 23B2 24D5 119C3 138C6
C2350 C2351 0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB_PCI64 3A2
C2355 C2356 C2357 0.1uF 20% 10V CERM 402
For PCI_AD<63..32>

=PP3V3_PWRON_SB_PCI32 3A2
C2360 C2361 C2362 0.1uF 20% 10V CERM 402
For PCI_AD<31..0>

=PP2V5_PWRON_SB 3C1 23C2 24D5 119C3 138C6
C2365 0.1uF 20% 10V CERM 402

Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.

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D	051-6863	07

SCALE: NONE SHT 23 OF 154

LAST_MODIFIED=Thu May 19 14:26:40 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI 24 147
I2S0_SB_TO_DEV_DTO 24 147
I2S0_MCLK 24 154
I2S0_BITCLK 24 147
I2S0_SYNC 24 147
I2S1_DEV_TO_SB_DTI 8 24
I2S1_SB_TO_DEV_DTO 8 24
I2S1_MCLK 8 24
I2S1_BITCLK 8 24
I2S1_SYNC 8 24
I2S2_DEV_TO_SB_DTI 24 154
I2S2_SB_TO_DEV_DTO 24 154
I2S2_MCLK 24 154
I2S2_BITCLK 24 154
I2S2_SYNC 24 154
SB_CLK18M_XTALI 24
SB_CLK18M_XTALO 24
SB_CLK18M_XTALO_R 24
SB_CLK25M_SATA 24 26
NB_TO_SB_INT 24
SB_CPU_A0_INT_L 24
SB_CPU_A1_INT_L 24
SB_CPU_B0_INT_L 24
SB_CPU_B1_INT_L 24
PCI_AIRPORT_INT_L 24 121
PCI_USB2_INT_L 24 122
I2S0_RESET_L 24 147
I2S1_RESET_L 8 24
I2S2_RESET_L 24 154
MB_SLOT_RESET_L 24
NB_SLOT_RESET_L 20 24
SB_CPU_A0_SRESET_L 24 56
SB_CPU_A1_SRESET_L 24 56
SB_CPU_B0_SRESET_L 24 56
SB_CPU_B1_SRESET_L 24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

=PP3V3_RUN_SB_PCI 7 24
R2476 10K 5% 1/16W MF-LF 402 To SouthBridge ->
NB_TO_SB_INT 24

MPIC_SB
42 NB_CPU_A0_INT_L (FROM NORTHBRIDGE) — R2475 10K 5% 1/16W MF-LF 402 — NB_INT_L_R
R2479 MPIC_NB 0 5% 1/16W MF-LF 402
56 CPU_A0_INT_R_L (TO CPU) — R2478 0 5% 1/16W MF-LF 402 — MPIC_SB SB_CPU_A0_INT_L (FROM SOUTHBRIDGE) 24
MPIC_SB Q2476 2N3904LF SOT23

NorthBridge / SouthBridge MPIC Routing

=PP2V5_PWRON_SB 7 23 119 130

R2405 3.3 5% 1/8W MF-LF 805 — PP2V5_PWRON_SB_XTAL18VDD (VOLTAGE=2.5V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — C2400 10UF 10% 6.3V X5R 805; C2401 1uF 10% 6.3V CERM 402

R2410 3.3 5% 1/8W MF-LF 805 — PP2V5_PWRON_SB_XTALVDD (VOLTAGE=2.5V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — C2410 10UF 10% 6.3V X5R 805; C2411 1uF 10% 6.3V CERM 402

Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

I2S0_DEV_TO_SB_DTI					I2S0_DEV_TO_SB_DTI	W7
I2S0_SB_TO_DEV_DTO	RP2410	3	6	33	I2S0_SB_TO_DEV_DTO_R	Y5
I2S0_MCLK	RP2410	4	5	33	I2S0_MCLK_R	U8
I2S0_BITCLK	RP2420	1	8	33	I2S0_BITCLK_R	AA4
I2S0_SYNC	RP2410	2	7	33	I2S0_SYNC_R	Y6
I2S1_DEV_TO_SB_DTI					I2S1_DEV_TO_SB_DTI	V10
I2S1_SB_TO_DEV_DTO	RP2420	3	6	33	I2S1_SB_TO_DEV_DTO_R	AB5
I2S1_MCLK	RP2430	2	7	33	I2S1_MCLK_R	V9
I2S1_BITCLK	RP2430	3	6	33	I2S1_BITCLK_R	AA8
I2S1_SYNC	RP2410	1	8	33	I2S1_SYNC_R	AA7
I2S1_RESET_L					(I2S1_RESET_L)	V5
I2S2_DEV_TO_SB_DTI					(I2S2_DEV_TO_SB_DTI)	AA5
I2S2_SB_TO_DEV_DTO	RP2430	4	5	33	I2S2_SB_TO_DEV_DTO_R	Y8
I2S2_MCLK	RP2420	4	5	33	I2S2_MCLK_R	Y7
I2S2_BITCLK	RP2420	2	7	33	I2S2_BITCLK_R	AB4
I2S2_SYNC	RP2430	1	8	33	I2S2_SYNC_R	W9
I2S2_RESET_L					(I2S2_RESET_L)	Y2

AUDIO GPIO - see note on right

119 56 24 23 20 7 =PP3V3_PWRON_SB
R2400 10K 5% 1/16W MF-LF 402
R2402 0 5% 1/16W MF-LF 402
122 119 30 28 SYS_IO_RESET_L

PLACE R2402 CLOSE TO SHASTA

119 56 24 23 20 7 =PP3V3_PWRON_SB
24 SB_CPU_A0_INT_L — R2408 10K — MPIC_NB
24 SB_CPU_A1_INT_L — R2409 10K — MPIC_NB
24 SB_CPU_B0_INT_L — R2412 10K — MPIC_NB
24 SB_CPU_B1_INT_L — R2418 10K — MPIC_NB
5% 1/16W MF-LF 402

24 7 =PP3V3_RUN_SB_PCI
R2456 10K 5% 1/16W MF-LF 402 — PCI_AIRPORT_INT_L 24 121
R2459 10K 5% 1/16W MF-LF 402 — PCI_USB2_INT_L 24 122
SAT_RUN
R2416 1K 1% 1/16W MF-LF 402 — SYS_OVERTEMP_L 20 24 28 93
NOSTUFF R2417 10K 5% 1/16W MF-LF 402 — MAKE_TBEN_SYNC_L 24

R2480 4.7K 1% 1/16W MF-LF 402
24 SB_CLK18M_XTALI
24 SB_CLK18M_XTALO_R
26 24 SB_CLK25M_SATA
R2490 200 1% 1/16W MF-LF 402
PP2406 P4MM SM
SB_CLK18M_XTALO 24
Y2490 18.432M CRITICAL SM
C2490 22pF 5% 50V CERM 402
C2491 22pF 5% 50V CERM 402

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

U2300 SHASTA V1.1 BGA-LF (2 OF 8)

I2S0	I2S0DTI_H	W7	
	I2S0DTO_H	Y5	
	I2S0MCLK_H	U8	
	I2S0BITCLK_H	AA4	
	I2S0SYNC_H	Y6	
I2S1	I2S1DTI_H	V10	
	I2S1DTO_H	AB5	
	I2S1MCLK_H	V9	
	I2S1BITCLK_H	AA8	
	I2S1SYNC_H	AA7	
	GPIO_H_0	V5	
I2S2	I2S2DTI_H	AA5	
	I2S2DTO_H	Y8	
	I2S2MCLK_H	Y7	
	I2S2BITCLK_H	AB4	
	I2S2SYNC_H	W9	
	GPIO_H_1	Y2	
GPIO	GPIO_H_2	AB3	
	GPIO_H_3	W8	
	PCI_SEL32BIT_H	W6	
I2C	I2CCLK_H	Y9	
	I2CDATA_H	AB7	
PWR_MGT	RESET_L	E9	
	STOPXTALS_L	W10	
	SUSPENDREQ_L	U11	
	SUSPENDACK_L	V11	
	PCI1PME_L	W18	
	INTRWD_H	V12	
TEST	TDI	AA11	
	TDO	W11	
	TCK	AB11	
	TMS	Y11	
	TRST_L	W12	
	TEST_MODE_H	AJ	
	PLLTEST	U14	
	FSTEST	V14	
XTALS	XTAL_18_I	W13	
	XTAL_18_O	V13	
	XTALI	U15	
	XTALO	V15	

XTAL VDD: AB13, AB12 — PLL 45 GND: AA13 — PLL 49 GND: AA12

PCI	PCI1REQ_3_L	U17	NB_CHP_FLT_N_B 24
	PCI1GNT_3_L	AA19	SB_SFC_RESET_L 24
	PCI1REQ_4_L	AB21	SB_CPU_VDNAP1 24 28
	PCI1GNT_4_L	AA20	SB_CPU_VDNAP2 24 28
	PCI1REQ_5_L	U16	SB_TO_SMU_INT_L 24 28
	PCI1GNT_5_L	Y20	LOGIC_BRD_GOOD 24
	PCI1AD_32_H	D18	SB_VDNAP0 24 31
	PCI1AD_33_H	A20	SYS_OVERTEMP_L 20 24 28 93
	PCI1AD_34_H	F18	SB_GPIO14 24 143
	PCI1AD_35_H	F17	MB_SLOT_RESET_L 24
	PCI1AD_36_H	G16	NB_SLOT_RESET_L_R
	PCI1AD_37_H	F16	PCI_AIRPORT_INT_L 24 121
	PCI1AD_38_H	A21	PCIX_INT_L 24
	PCI1AD_39_H	B21	RAI_EXP_INTR_L<3> 20
	PCI1AD_40_H	C20	RAI_EXP_INTR_L<2> 20
	PCI1AD_41_H	G17	RAI_EXP_INTR_L<1> 20
	PCI1AD_42_H	G18	RAI_EXP_INTR_L<0> 20
	PCI1AD_43_H	E19	GIGE_P1_INTA_L 24
	PCI1AD_44_H	F19	GIGE_P2_INTB_L 24
	PCI1AD_45_H	D20	RAI_ALERT_L 24
	PCI1AD_46_H	E20	RAI_FATAL_L 24
	PCI1AD_47_H	C21	PCI_USB2_INT_L 24 122
	PCI1AD_48_H	F20	FW_LOWPWR_R 24
	PCI1AD_49_H	G19	ENETFW_RESET 17 24
	PCI1AD_50_H	C22	MAKE_TBEN_SYNC_L 24
	PCI1AD_51_H	D21	ENET_ENERGYDET 24 132
	PCI1AD_52_H	G20	AUDIO_LO_DET_L 153
	PCI1AD_53_H	D22	AUDIO_LO_OPTICAL_PLUG_L 153
	PCI1AD_54_H	K18	AUDIO_LI_DET_L 153
	PCI1AD_55_H	H19	AUDIO_LI_OPTICAL_PLUG_L 154
	PCI1AD_56_H	J17	AUDIO_HP_DET_L 154
	PCI1AD_57_H	F21	AUDIO_MIC_ID 154
	PCI1AD_58_H	G21	AUDIO_LO_MUTE_L 150
	PCI1AD_59_H	H20	AUDIO_HP_MUTE_L 154
	PCI1AD_60_H	J19	AUDIO_SPKR_MUTE_L 152
	PCI1AD_61_H	F22	AUDIO_EXT_MCLK_SEL 154
	PCI1AD_62_H	G22	AUDIO_SPDIFIN_INT_L 154
	PCI1AD_63_H	H21	AUDIO_SPKR_ID 153
	PCI1C_BE_4_L	J20	SB_CPU_A0_INT_L 24
	PCI1C_BE_5_L	H22	SB_CPU_A1_INT_L 24
	PCI1C_BE_6_L	K22	SB_CPU_B0_INT_L 24
	PCI1C_BE_7_L	K20	SB_CPU_B1_INT_L 24
	PCI1REQ64_L	K17	SYS_SLEWING_L 24 26 28 50
	PCI1ACK64_L	L17	SB_CPU_A0_SRESET_L 24 56
	PCI1PAR64_H	E18	SB_CPU_A1_SRESET_L 24 56
XGI	XGI_CLK_H	Y4	SB_CPU_B0_SRESET_L 24 56
	XGI_DTO0_H	U7	SB_CPU_B1_SRESET_L 24 56
	XGI_DTO1_H	T9	NB_TO_SB_INT 24
	XGI_DTI_H	W2	SMU_TO_SB_INT_L 24

XW2400 — PP_1V2PWRONSBPLL45VDD — P4MM SM — PP2400

PP1V2_PWRON_SB_PLL45VDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
C2421 1uF 10% 6.3V CERM 402; C2420 10UF 10% 6.3V X5R 805
R2420 3.3 5% 1/8W MF-LF 805 — =PP1V2_PWRON_SB 7

PP1V2_PWRON_SB_PLL49VDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
C2431 1uF 10% 6.3V CERM 402; C2430 10UF 10% 6.3V X5R 805
R2430 3.3 5% 1/8W MF-LF 805

=PP3V3_PWRON_SB 7 20 23 24 56 119
C2440 0.1uF 20% 25V CERM 402

NET_SPACING_TYPE=P3MM SPACING — P4MM SM — PP2405

R2432 0 5% 1/16W MF-LF 402 — NB_SLOT_RESET_L 20 24

PLACE R2432 CLOSE TO SHASTA

AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

119 56 24 23 20 7 =PP3V3_PWRON_SB

24 8	I2S1_RESET_L	R2464 10K 5% 1/16W MF-LF 402	
24	SB_GPIO_H_3	R2463 10K 5% 1/16W MF-LF 402	
24	NB_CHP_FLT_N_B	R2450 10K 5% 1/16W MF-LF 402	
24	SB_SFC_RESET_L	R2451 10K 5% 1/16W MF-LF 402	
28 24	SB_CPU_VDNAP1	R2452 10K 5% 1/16W MF-LF 402	
28 24	SB_CPU_VDNAP2	R2453 10K 5% 1/16W MF-LF 402	
28 24	SB_TO_SMU_INT_L	R2454 10K 5% 1/16W MF-LF 402	
24	LOGIC_BRD_GOOD	R2455 10K 5% 1/16W MF-LF 402	
31 24	SB_VDNAP0	R2404 10K 5% 1/16W MF-LF 402	
93 28 24 20	SAT_PWRON SYS_OVERTEMP_L	R2460 1K 1% 1/16W MF-LF 402	
143 24	SB_GPIO14	R2422 10K 5% 1/16W MF-LF 402	
24	MB_SLOT_RESET_L	R2461 4.7K 5% 1/16W MF-LF 402	
24 20	NB_SLOT_RESET_L	NOSTUFF R2406 4.7K 5% 1/16W MF-LF 402	
24	PCIX_INT_L	R2419 10K 5% 1/16W MF-LF 402	
24	GIGE_P1_INTA_L	R2457 10K 5% 1/16W MF-LF 402	
24	GIGE_P2_INTB_L	R2413 10K 5% 1/16W MF-LF 402	
24	RAI_ALERT_L	R2414 10K 5% 1/16W MF-LF 402	
24	RAI_FATAL_L	R2465 10K 5% 1/16W MF-LF 402	
50 28 26 24	SYS_SLEWING_L	NOSTUFF R2462 1K 1% 1/16W MF-LF 402	
24	SMU_TO_SB_INT_L	R2421 10K 5% 1/16W MF-LF 402	
24	MAKE_TBEN_SYNC_L	R2415 10K 5% 1/16W MF-LF 402	

R2407 0 NO STUFF 5% 1/16W MF-LF 402 — FW_LOWPWR 139
24 FW_LOWPWR_R — R2466 10K 5% 1/16W MF-LF 402
24 17 ENETFW_RESET — R2467 10K 5% 1/16W MF-LF 402
132 24 ENET_ENERGYDET — R2468 10K 5% 1/16W MF-LF 402

Shasta Serial / Misc

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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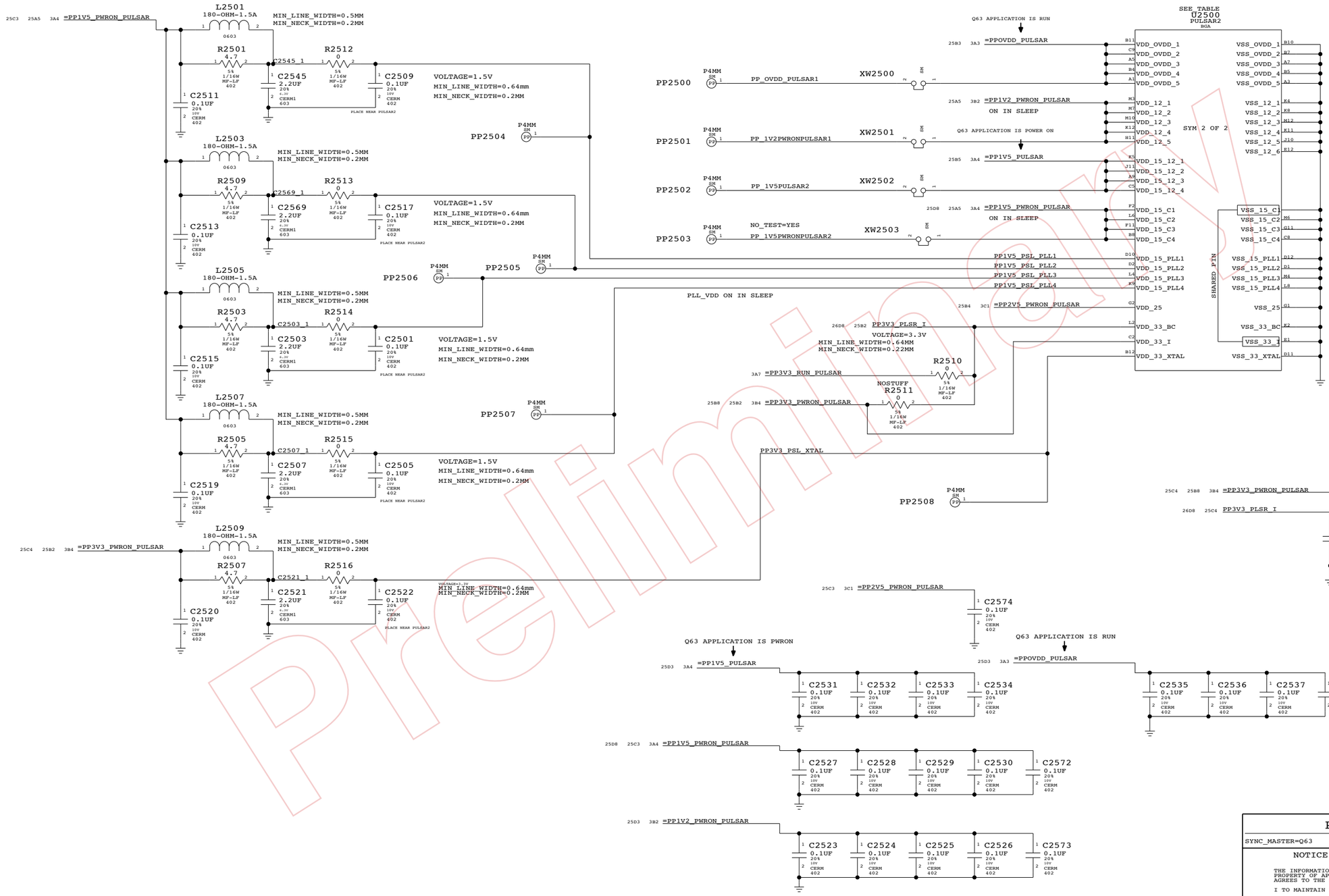
SCALE: NONE	SHT 24 OF 154	

DRAWING
TITLE=$TITLEBANNER
ABBREV=$ABBREVS

LAST_MODIFIED=Thu May 19 14:26:41 2005



PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 25 OF 154	

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DRAWING

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR

U2500
PULSAR2
BGA
SYM 1 OF 2

PP2602 P4MM SM
PP2601 P4MM SM
PP2600 P4MM SM

R2612 0 5% 1/16W MF-LF 402 — 28 CLOCK_RESET_L — PLS2_RESET_L
R2628 0 5% 1/16W MF-LF 402 — SLEWING* — SYS_SLEWING_L_R — SYS_SLEWING_L — 24 28 50 — PULLED UP TO PP3V3_RUN ON P.28

PP3V3_PLSR_I — 25

R2613 10K 5% 1/16W MF-LF 402
NOSTUFF R2614 10K 5% 1/16W MF-LF 402
R2616 10K 5% 1/16W MF-LF 402
R2623 0 5% 1/16W MF-LF 402
NOSTUFF R2618 1K 1% 1/16W MF-LF 402
R2621 1K 1% 1/16W MF-LF 402 NOSTUFF
R2600 0 5% 402 — 54 30 16 15 13 12 11 SYS_SLEEP

PLSR2_RESET_L — C3 RESET*
PLSR2_ASEL_INT_L — D3 ASEL_INT*
I2C_CLOCK_B_SCL — 39 — B1 SCLK
I2C_CLOCK_B_SDA — 39 — B2 SDATA
PLSR2_PD — C1 PD
PLSR2_TM — E2 TEST_MODE
PLSR2_OEMODE — E3 OEMODE
PLS2_X_IN — C12 XIN
PLS2_X_OUT — C11 XOUT
PLS2_REF15 — H10 REF_15
PLS2_REF25 — F1 REF_25
PLS2_REF33 — L1 REF_33

R2625 1K 1% 1/16W MF-LF 402
R2626 1K 1% 1/16W MF-LF 402
R2627 1K 1% 1/16W MF-LF 402

NOSTUFF J2600 U.FL-R_SMT F-ST-SM
PLS2_EXTCLK — NOSTUFF R2662 24 5% 1/16W MF-LF 402 — PLS2_INTERM — NOSTUFF R2664 24 5% 1/16W MF-LF 402
NO STUFF R2652 0 5% 1/16W MF-LF 402
R2654 0 5% 1/16W MF-LF 402
NO STUFF R2658 330K 5% 1/16W MF-LF 402
R2656 0 5% 1/16W MF-LF 402
CRITICAL Y2601 25.0000M SM-2
PLS2_X_IN_B — PLS2_X_OUT_B
C2607 33PF 5% 50V CERM 402
C2605 33PF 5% 50V CERM 402

HCLKP_0	A6	200MHZ, 1.5VOVDD		
HCLKN_0	B6	200MHZ, 1.5VOVDD		
HCLKP_1	C4	200MHZ, 1.5VOVDD		
HCLKN_1	A4	200MHZ, 1.5VOVDD		
HCLKP_2	B3	200MHZ, 1.5VOVDD		
HCLKN_2	A2	200MHZ, 1.5VOVDD		
HTBEN_0	A11	66MHZ, 1.5VOVDD	9 CPU_A_TBEN_CLK_R	
HTBEN_1	A10	66MHZ, 1.5VOVDD	9 CPU_B_TBEN_CLK_R	
HSYNC_0	A8	1.5VOVDD	9 CPU_A_APSYNC_R	
HSYNC_1	B9	1.5VOVDD	9 CPU_B_APSYNC_R	
HSYNC_2	C10	1.5VOVDD	9 NB_APSYNC_R	
GPCLK12_C0	H12	66MHZ, 1.2V (150MHZ FOR ASPEN)	9 HT_SB_REFCLK_R	
GPCLK12P_A0	K3	200MHZ, 1.2V	9 HT_NB_REFCLK_H0_R	
GPCLK12N_A0	L3	200MHZ, 1.2V	9 HT_NB_REFCLK_L0_R	
GPCLK12P_A1	M5	200MHZ, 1.2V	9 CLK_RAIREF_200M_P_R	
GPCLK12N_A1	L5	200MHZ, 1.2V	9 CLK_RAIREF_200M_N_R	
GPCLK12P_B0	L7	100MHZ, 1.2V	9 NB_PMR_CLK_P_R	
GPCLK12N_B0	M8	100MHZ, 1.2V	9 NB_PMR_CLK_N_R	
GPCLK12P_C0	M9	100MHZ, 1.2V	9 NB_PCIE_REFCLK_P_C	
GPCLK12N_C0	L9	100MHZ, 1.2V	9 NB_PCIE_REFCLK_N_C	
GPCLK12P_C1	L10	100MHZ, 1.2V	9 GFX_SLOT_PCIE_REFCLK_P_C	
GPCLK12N_C1	M11	100MHZ, 1.2V	9 GFX_SLOT_PCIE_REFCLK_N_C	
GPCLK12P_C2	L11	100MHZ, 1.2V	9 PCIE_A_REFCLKIN_P_C	
GPCLK12N_C2	L12	100MHZ, 1.2V	9 PCIE_A_REFCLKIN_N_C	
GPCLK12P_C3	K10	100MHZ, 1.2V	9 PCIE_B_REFCLKIN_P_C	
GPCLK12N_C3	J12	100MHZ, 1.2V	9 PCIE_B_REFCLKIN_N_C	
GPCLK12P_C4	G12		9 PCIE_C_REFCLKIN_P_C	
GPCLK12N_C4	F12	100MHZ, 1.2V	9 PCIE_C_REFCLKIN_N_C	
GPCLK12P_D0	E10	66MHZ, 1.2V	9 NB_DDR_REFCLK_P_R	
GPCLK12N_D0	E11	66MHZ, 1.2V	9 NB_DDR_REFCLK_N_R	
GPCLK25_E0	H1	25MHZ, 2.5V	9 CLK_RAI_GIGE_25MHZ_R	
GPCLK25_E1	H3	25MHZ, 2.5V	9 QUA0_REF_25MHZ_R	
GPCLK25_F0	H2	25MHZ, 2.5V	9 SB_CLK25M_SATA_R	
GPCLK25_F1	J3	25MHZ, 2.5V	9 QUA1_REF_25MHZ_R	
GPCLK33_E0	J1	66MHZ, 3.3V	6 PCI_CLK66M_SB_INT_R	
GPCLK33_E1	J2	33MHZ, 3.3V	9 PCI_CLK33M_SB_EXT_R	
GPCLK33_F0	K1	33MHZ, 3.3V	9 SB_AIRPRT_CLK_33MHZ_R	
GPCLK33_F1	M1	66MHZ, 3.3V	9 CLK_RAI_REFCLK_66M_R	
GPCLK33_F2	M2	33MHZ, 3.3V	9 SB_USB2_CLK_33MHZ_R	

EI_CPU_A_SYSCLK_P — 56
EI_CPU_A_SYSCLK_N — 56
EI_CPU_B_SYSCLK_P — 27
EI_CPU_B_SYSCLK_N — 27
EI_NB_SYSCLK_P — 42 56
EI_NB_SYSCLK_N — 42 56
R2629 0 5% 1/16W MF-LF 402 — CPU_A_TBEN_CLK_US — 56
R2630 0 5% 1/16W MF-LF 402 NOSTUFF — NC_CPU_B_TBEN_CLK_US — 6
R2631 0 5% 1/16W MF-LF 402 — CPU_A_APSYNC — 56
R2632 0 5% 1/16W MF-LF 402 — CPU_B_APSYNC — 27
R2633 0 5% 1/16W MF-LF 402 — NB_APSYNC — 42 56
R2634 0 5% 1/16W MF-LF 402 — HT_CLK66M_SB — 103
R2635 0 5% 1/16W MF-LF 402 — HT_NB_REFCLK_P<0> — 98 101
R2636 0 5% 1/16W MF-LF 402 — HT_NB_REFCLK_N<0> — 98 101
R2637 0 5% 1/16W MF-LF 402 — CLK_RAI_200M_P<0> — 27
R2639 0 5% 1/16W MF-LF 402 — CLK_RAI_200M_N<0> — 27
R2641 0 5% 1/16W MF-LF 402 — NB_PMR_CLK_P — 20 27
R2643 0 5% 1/16W MF-LF 402 — NB_PMR_CLK_N — 20 27
R2666 0 5% 1/16W MF-LF 402 — CLK_KOD_100M_P<0> — 82 97
R2667 0 5% 1/16W MF-LF 402 — CLK_KOD_100M_N<0> — 82 97
R2674 0 5% 1/16W MF-LF 402 — CLK_PCIE_SLOTA_P<0> — 84 97
R2675 0 5% 1/16W MF-LF 402 — CLK_PCIE_SLOTA_N<0> — 84 97
R2668 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEA_P<0> — 27
R2669 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEA_N<0> — 27
R2670 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEB_P<0> — 27
R2671 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEB_N<0> — 27
R2672 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEC_P<0> — 27
R2673 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEC_N<0> — 27
R2645 0 5% 1/16W MF-LF 402 — NB_DDR_REFCLK_P — 59
R2647 0 5% 1/16W MF-LF 402 — NB_DDR_REFCLK_N — 59
R2649 0 5% 1/16W MF-LF 402 — CLK_RAI_GIGE_25MHZ — 27
R2651 0 5% 1/16W MF-LF 402 — RAM_ARB0_REF25MHZ — 27
R2653 0 5% 1/16W MF-LF 402 — SB_CLK25M_SATA — 24
R2655 0 5% 1/16W MF-LF 402 — RAM_ARB1_REF25MHZ — 27
R2657 0 5% 1/16W MF-LF 402 — PCI_CLK66M_SB_INT — 27 119
R2659 0 5% 402 MF-LF 1/16W — PCI_CLK33M_SB_EXT_RR — 27 119
NOSTUFF R2601 49.9 1% 1/16W MF-LF 402 PLACE R2602 BESIDE R2659 — CPU_TBEN_CLK — 27
R2660 0 5% 1/16W MF-LF 402 — PCI_CLK33M_AIRPORT — 121
R2663 0 5% 1/16W MF-LF 402 — CLK_RAI_REFCLK_66M — 27
MB_PCIX_REFCLK
R2665 0 5% 1/16W MF-LF 402 — PCI_CLK33M_USB2 — 27

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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DRAWING

N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M — MAKE_BASE=TRUE — CLK_RAI_REFCLK_66M 26

6 NC_CLK_RAI_GIGE_25MHZ — MAKE_BASE=TRUE — CLK_RAI_GIGE_25MHZ 26

6 NC_CLK_RAI_200M_P<0> — MAKE_BASE=TRUE — CLK_RAI_200M_P<0> 26

6 NC_CLK_RAI_200M_N<0> — MAKE_BASE=TRUE — CLK_RAI_200M_N<0> 26

6 NC_CLK_RAI_PCIEA_P<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEA_P<0> 26

6 NC_CLK_RAI_PCIEA_N<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEA_N<0> 26

6 NC_CLK_RAI_PCIEB_P<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEB_P<0> 26

6 NC_CLK_RAI_PCIEB_N<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEB_N<0> 26

6 NC_CLK_RAI_PCIEC_P<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEC_P<0> 26

6 NC_CLK_RAI_PCIEC_N<0> — MAKE_BASE=TRUE — CLK_RAI_PCIEC_N<0> 26

N/C CPUB CLOCKS

9 NC_CPU_TBEN_CLK — MAKE_BASE=TRUE — CPU_TBEN_CLK 26

CPU_TBEN_CLK IS FOR Q63 ONLY
IT IS THE INPUT TO THE AND GATE WHICH
GENERATES CPUA AND CPUB TBEN_CLK

6 NC_EI_CPU_B_SYSCLK_P — MAKE_BASE=TRUE — EI_CPU_B_SYSCLK_P 26

6 NC_EI_CPU_B_SYSCLK_N — MAKE_BASE=TRUE — EI_CPU_B_SYSCLK_N 26

6 NC_CPU_B_APSYNC — MAKE_BASE=TRUE — CPU_B_APSYNC 26

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ — MAKE_BASE=TRUE — RAM_ARB0_REF25MHZ 26

6 NC_RAM_ARB1_REF25MHZ — MAKE_BASE=TRUE — RAM_ARB1_REF25MHZ 26

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	167
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	168
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	169
26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB	170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 — MAKE_BASE=TRUE — =PCI_CLK33M_USB2 122

Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
RTC_CLK32K_XTAL	0.38MM SPACING	
	0.38MM SPACING	
	P3MM SPACING	
	0.25MM SPACING	

SMU_CLK10M_XIN 28B6
SMU_CLK10M_XOUT 28A7
SMU_CLK10M_XOUT_R 28B6
RTC_CLK32K_X1 28D1
RTC_CLK32K_X2 28D1
SMU_IO_RESET_L 28B3 29D8 30B8
SYS_NORTH_RESET_L 6B7 20C3 28B1 28C3 28D3 30D8

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	0.25MM SPACING	
SMU_RESET	0.25MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

SYS_NORTH_RESET_L 6B7 20C3 28B1 28C3 28D6 30D8
SYS_IO_RESET_L 21C5 24B7 29D6 119A4 122A7 29D7 29D3 29C7 29B7 29A6 28D6 28C2 8A5 3B6 157D3 157A6 38B3 30B6 30A6
CLOCK_RESET_L 26D7 28B3
SYS_RESET_BUTTON_L 6C7 8D6 28B3 28C1

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

Real Time Clock

=PP3V3_ALL_RTC 3C4
=PP3V3_ALL_SMU 3B6 30A6
C2808 0.1uF 20% 10V CERM 402
U2801 DS1338U-33 MSOP
VCC 8
SDA 5
SCL 6
SQW/OUT 7
VBAT 3
GND 4
X1 1
X2 2
NC 1
I2C_RTC_SDA 39B5
I2C_RTC_SCL 39B5
RTC_CLK32K_X1
RTC_CLK32K_X2
CRITICAL
Y2801 32.768K SM-LF
C2809 0.1uF 20% 10V CERM 402

SMU Pull-ups / pull-down

=PP3V3_ALL_SMU 38B3 30B6 30A6 29D7 29C7 29B7 29A6 28D6 28D2 8A5 3B6 157D3 157A6
R2800 10K 5% 1/16W MF-LF 402 — SYS_POWERUP_L 8A6 16C8 28B3
R2801 10K 5% 1/16W MF-LF 402 — SYS_RESET_BUTTON_L 6C7 8D6 28B3 28D3
R2802 10K 5% 1/16W MF-LF 402 — SYS_POWER_BUTTON_L 6C7 8D6 28B3 157C6
=PP3V3_PWRON_SMU 38B3 30D8 30C8 30C5 30B7 29D7 3B4
R2804 10K 5% 1/16W MF-LF 402 — SYS_PME_L 21C1 24B5 28C3 113A6 122A7
=PP3V3_RUN_SMU 157D6 157D5
R2812 2.0K 1% 1/16W MF-LF 402 — SYS_SLEWING_L 24A3 24B2 26D4 28C3 43A6 45A6
NOSTUFF
R2811 2.0K 1% 1/16W MF-LF 402 — SMU_SUSPENDREQ_L 24B5 28B3 30A5 30A7 30C8
=PP2V5_PWRON_NB_MISC
DRIVEN PUSH/PULL
NOSTUFF
R2813 10K 5% 1/16W MF-LF 402 — SYS_NORTH_RESET_L 6B7 20C3 28C3 28D3 28D6 30D8
PULLUP AT LEVEL SHIFTER P.30
R2810 100K 1% 1/16W MF-LF 402 — SMU_SLEEP 6C7 28B3 29D8 30C8

Alternate Functions

Tower & Server

		Port			Port	
28C3	CPU_VID<0>	6.0	SAT_MRESET_L	29A5	6.3	SMU_FAN_RPM6
28C3	CPU_VID<1>	6.1	CPU_A_INSERTED_L	30D4	6.4	SMU_FAN_RPM7
28C3	CPU_VID<2>	6.2	CPU_B_INSERTED_L	30C3	3.2	NB_TDI
28C3	I2C_SMU_CPU_SDA_IN	7.2	SMU_FAN_PWM8	32B5	3.3	NB_TCK
28C3	I2C_SMU_CPU_SCL_IN	7.4	SMU_FAN_PWM9	32D8	8.5	NB_TMS
28B6	I2C_SMU_A_SDA_IN	3.0	I2C_SMU_A_SDA	32A5	10.7	NB_TDO_SMU
28B6	I2C_SMU_A_SDA_OUT_L	3.1	I2C_SMU_A_SCL	32C8 39D8		

28B3	I2C_SMU_CPU_SDA_OUT_L	39D8	20B3
28B3	I2C_SMU_CPU_SCL_OUT_L	39D8	29D7

System Management Unit

SYNC_MASTER=Q63	SYNC_DATE=05/19/2005

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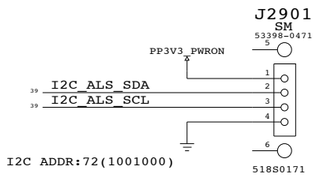
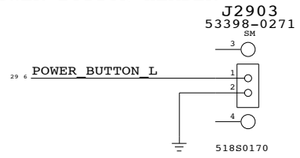
DRAWING

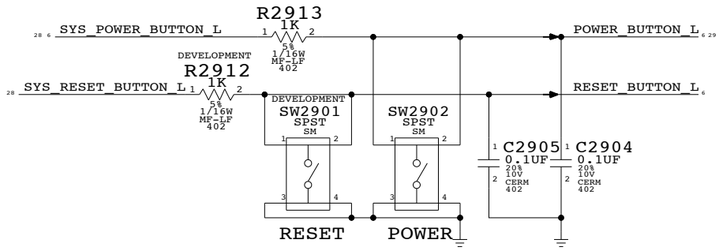
AMBIENT LIGHT SENSOR CONNECTOR



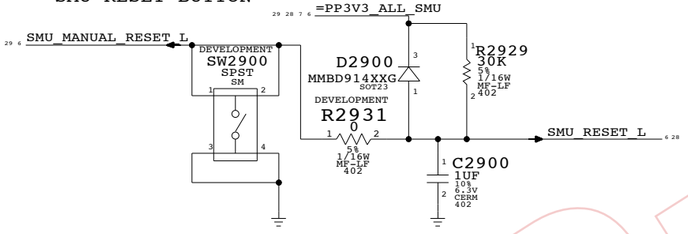
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

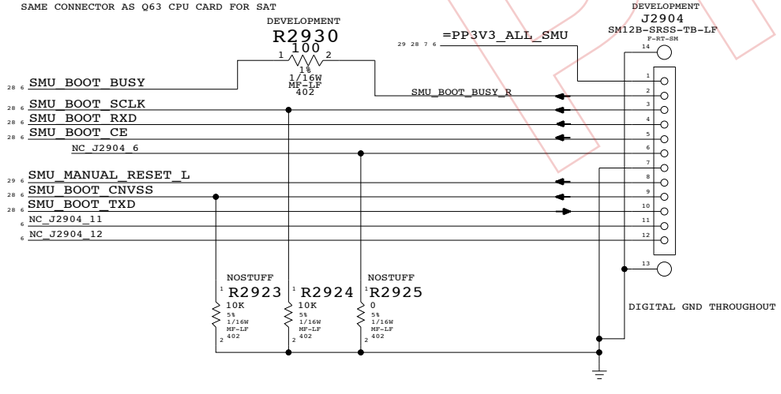


SMU RESET BUTTON

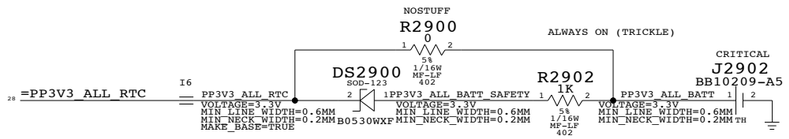


SMU DEBUG/DOWNLOAD CONNECTOR

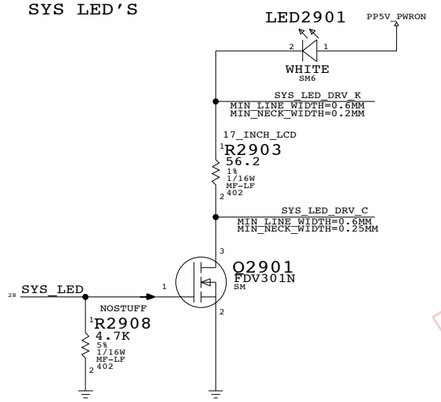
SAME CONNECTOR AS Q63 CPU CARD FOR SAT



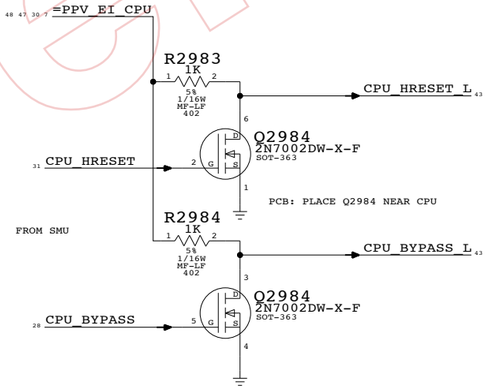
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483921	1	RES, 39.2 OHM, 1%, 402	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

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NONE	29	154

SMU TO NB SUSPEND_REQ

SAME AS Q63

=PP3V3_PWRON_SMU

R3000 1K 5% 1/16W MF-LF 402

R3003 4.7K 5% 1/16W MF-LF 402

PMU_SUSPEND_REQ

Q3005 2N7002DW-X-F SOT-363

SMU_SUSPENDREQ_L

=PP2V5_PWRON_NB_MISC

R3001 100 5% 1/16W MF-LF 402

Q3000 2N7002DW-X-F SOT-363

NB_SUSPEND_REQ_L

NOSTUFF R3002 0 5% 1/16W MF-LF 402

SMU_SUSPENDREQ_L_R

NOSTUFF R3099 0 5% 1/16W MF-LF 402

SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

=PP3V3_PWRON_SMU

R3006 10K 5% 1/16W MF-LF 402

R3010 4.7K 5% 1/16W MF-LF 402

NB_PU_RESET

Q3005 2N7002DW-X-F SOT-363

SYS_NORTH_RESET_L

=PP2V5_PWRON_NB_MISC

R3007 4.7K 5% 1/16W MF-LF 402

Q3000 2N7002DW-X-F SOT-363

NB_PU_RST_L

NOSTUFF R3008 0 5% 1/16W MF-LF 402

SYS_NORTH_RESET_L_R

NOSTUFF R3098 0 5% 1/16W MF-LF 402

NOSTUFF R3009 0 5% 1/16W MF-LF 402

SYS_SLEEP

SYS_2SLEEP_R

NOSTUFF Q3006 2N7002 SOT23-LF

CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART

SHARE CPU AND NB JTAG TDO WITH SMU

=PP3V3_PWRON_SMU

SMU DRIVES 3.3V PUSH-PULL ON ALL JTAG-RELATED PINS

PCB: PLACE U3070 NEAR SMU

CRITICAL

U3070 SN74LVC2G157 TSSOP

JTAG_CPU_TDO_3V3

JTAG_NB_TDO

SMU_CPU_NB_SEL

VIH=2V

SMU_JTAG_TDO

NC_JTAGMUX_3

C3070 0.1UF 20% 10V CERM 402

SHARE CPU AND NB JTAG TMS WITH SMU

=PP2V5_PWRON_NB_MISC

C3071 0.1UF 20% 10V CERM 402

PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.

CRITICAL

U3071 74LVC1G SC70-6

TO LEVEL SHIFTER SMU_CPU_TMS

3.3V TOLERANT

STRAIGHT TO NB JTAG_NB_TMS

SMU_JTAG_TMS

MISC. SMU BUFFERS

SAME AS (Q63).

=PP3V3_PWRON_SMU

R3021 4.7K 5% 1/16W MF-LF 402

U700 IS POWERED BY PP3V3_ALL

U700 74LCX125 TSSOP

SMU_IO_RESET_L

SYS_IO_RST_L_R

R3022 100 5% 1/16W MF-LF 402

SYS_IO_RESET_L

SMU_SLEEP

SYS_SLEEP_R

R3023 100 5% 1/16W MF-LF 402

SYS_SLEEP

SMU JTAG TCK TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3081 1K 5% 1/16W MF-LF 402

R3080 4.7K 5% 1/16W MF-LF 402

NOSTUFF R3082 33 5% 1/16W MF-LF 402

JTAG_CPU_TCK

Q3081 2N7002DW-X-F SOT-363

SMU_JTAG_TCK_L

SMU_JTAG_TCK

Q3080 2N7002DW-X-F SOT-363

STUFF IF USING REGISTERED DIMM

=PP3V3_PWRON_SMU

R3040 1K 5% 1/16W MF-LF 402

SMU_IO_RESET

NOSTUFF Q3040 2N7002 SOT23-LF

SYS_IO_RST_L_R

SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)

=PPV_EI_CPU

C3030 0.1UF 20% 10V CERM 402

VCC RANGE 0.8V - 2.7V

U3030 SN74AUC2G34 SOT23-6

VIH = 1.0V, 3.3V TOLERANT

SMU_JTAG_TDI

R3030 33 5% 1/16W MF-LF 402

JTAG_CPU_TDI

CRITICAL

SMU JTAG TDI TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3084 1K 5% 1/16W MF-LF 402

NOSTUFF R3085 33 5% 1/16W MF-LF 402

JTAG_CPU_TDI

Q3081 2N7002DW-X-F SOT-363

SMU_JTAG_TDI_L

SMU_JTAG_TDI

Q3080 2N7002DW-X-F SOT-363

NB JTAG IS A DEVELOPMENT ONLY FEATURE

=PP2V5_PWRON_NB_MISC

DEVELOPMENT C3031 0.1UF 20% 10V CERM 402

VCC RANGE 0.8V - 2.7V

DEVELOPMENT U3031 SN74AUC2G34 SOT23-6

DEVELOPMENT R3032 33 5% 1/16W MF-LF 402

JTAG_NB_TDI

VIH = 2.0V, 3.3V TOLERANT

R3034 10K 5% 1/16W MF-LF 402

LEVEL SHIFT TDO FROM CPU TO MUX

=PP3V3_PWRON_SMU

R3051 1K 5% 1/16W MF-LF 402

JTAG_CPU_TDO_L

R3052 100 5% 1/16W MF-LF 402

JTAG_CPU_TDO_3V3

JTAG_CPU_TDO_R

R3050 10K 5% 1/16W MF-LF 402

JTAG_CPU_TDO

Q3050 2N3904LF SOT23

Q3021 2N7002DW-X-F SOT-363

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER

=PP3V3_PWRON_SMU

R3091 1K 5% 1/16W MF-LF 402

R3093 1K 5% 1/16W MF-LF 402

NB_SUSPEND_ACK_L_R

NB_SUSPENDACK

NB_SUSPENDACK_L

NB_SUSPEND_ACK_L

R3090 10K 5% 1/16W MF-LF 402

Q3090 2N3904LF SOT23

Q3021 2N7002DW-X-F SOT-363

NOSTUFF R3092 0 5% 1/16W MF-LF 402

LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)

=PPV_EI_CPU

=PP3V3_PWRON_SMU

R3026 1K 5% 1/16W MF-LF 402

R3027 1K 5% 1/16W MF-LF 402

JTAG_SMU_TMS_2_R

JTAG_CPU_TMS_2_R

NOSTUFF R3028 33 5% 1/16W MF-LF 402

JTAG_CPU_TMS

SMU_CPU_TMS

R3020 10K 5% 1/16W MF-LF 402

Q3030 2N3904LF SOT23

Q3031 2N7002DW-X-F SOT-363

LEVEL SHIFT SMU TMS TO CPU (PRIMARY PLAN)

U5640 IS POWERED BY PPV_EI_CPU

CRITICAL

VIH = 1.0V

SMU_CPU_TMS

U5640 PBT4A3UC0123 VSSOP

125

R3039 33 5% 1/16W MF-LF 402

JTAG_CPU_TMS

DEMUX DRIVES PUSH-PULL 2.5V

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)

PCB; PLACE U5640 AND R3039 NEAR CPU

VCC RANGE 0.8V - 2.7V

U3030 SN74AUC2G34 SOT23-6

VIH = 1.0V, 3.3V TOLERANT

SMU_JTAG_TCK

R3031 33 5% 1/16W MF-LF 402

JTAG_CPU_TCK

PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.

PCB: PLACE 33 OHM RES NEAR U3030/31 PART.

VIH = 2.0V, 3.3V TOLERANT

PULLUP IF KODIAK JTAG IS NOSTUFFED

R3035 10K 5% 1/16W MF-LF 402

U3031 SN74AUC2G34 SOT23-6

R3033 33 5% 1/16W MF-LF 402

JTAG_NB_TCK

PULLDOWNS TO BUFFERS/LOGIC GATES

R3036 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TDI

R3037 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TCK

R3070 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TMS

R3071 100K 5% 1/16W MF-LF 402 — SMU_CPU_NB_SEL

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
		CPU_TEMP0	P0.2	
Q63 NC'S THESE AS IT USES A SAT.		CPU_BYPASS	P0.3	
	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3 28
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
		CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L 28
	30 SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN 28
	30 SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN — SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	30 SMU_CPU_NB_SEL	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING*	P8.4	
	30 SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		PS9_5	P9.5	
		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR 28
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	30 SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L 28

CPU VID<0:5>

VID CONTROLLED BY SMU

PP3V3_RUN

28 CPU_VID<0>	R3119 0 5% 1/16W MF-LF 402	CPU_VID_R<0>	R3114 10K 5% 1/16W MF-LF 402
28 CPU_VID<1>	R3120 0 5% 1/16W MF-LF 402	CPU_VID_R<1>	R3116 10K 5% 1/16W MF-LF 402
28 CPU_VID<2>	R3121 0 5% 1/16W MF-LF 402	CPU_VID_R<2>	R3117 10K 5% 1/16W MF-LF 402
28 CPU_VID<3>	R3122 0 5% 1/16W MF-LF 402	CPU_VID_R<3>	R3108 10K 5% 1/16W MF-LF 402
28 CPU_VID<4>	R3123 0 5% 1/16W MF-LF 402	CPU_VID_R<4>	R3109 10K 5% 1/16W MF-LF 402
28 CPU_VID<5>	R3124 0 5% 1/16W MF-LF 402	CPU_VID_R<5>	R3104 10K 5% 1/16W MF-LF 402

All CPU_VID<n> nets: MAKE_BASE=TRUE

NOSTUFF J3108 BM12B-SRSS-TB (LF)(SN)

NOSTUFF R3132 1K 5% 1/16W MF-LF 402; NOSTUFF R3131 1K 5% 1/16W MF-LF 402; NOSTUFF R3130 1K 5% 1/16W MF-LF 402; NOSTUFF R3129 1K 5% 1/16W MF-LF 402; NOSTUFF R3127 1K 5% 1/16W MF-LF 402; R3111 20K 5% 1/16W MF-LF 402

NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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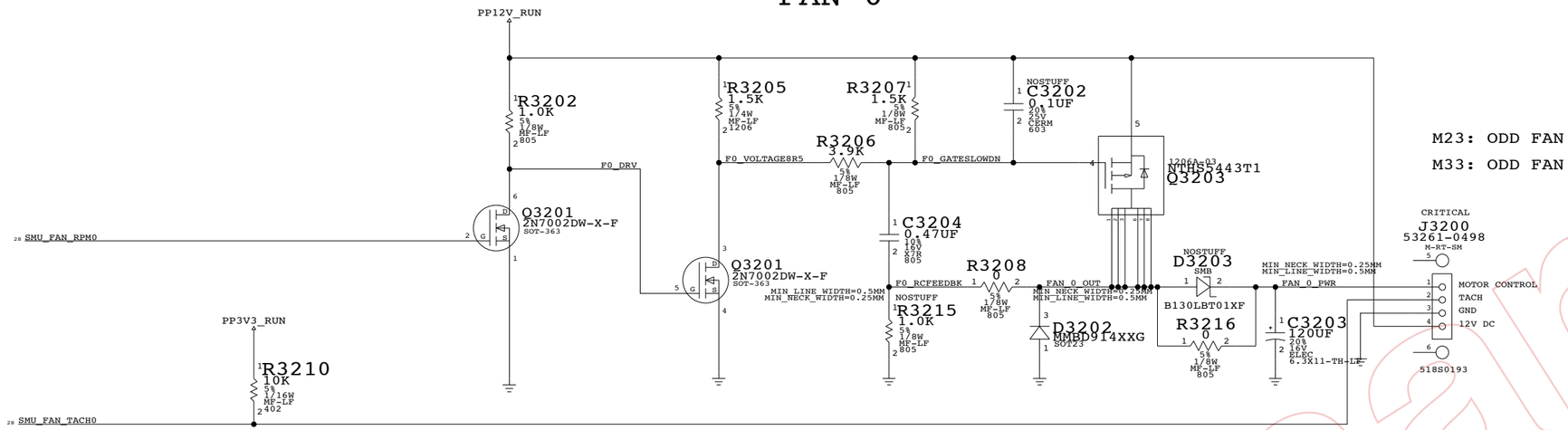
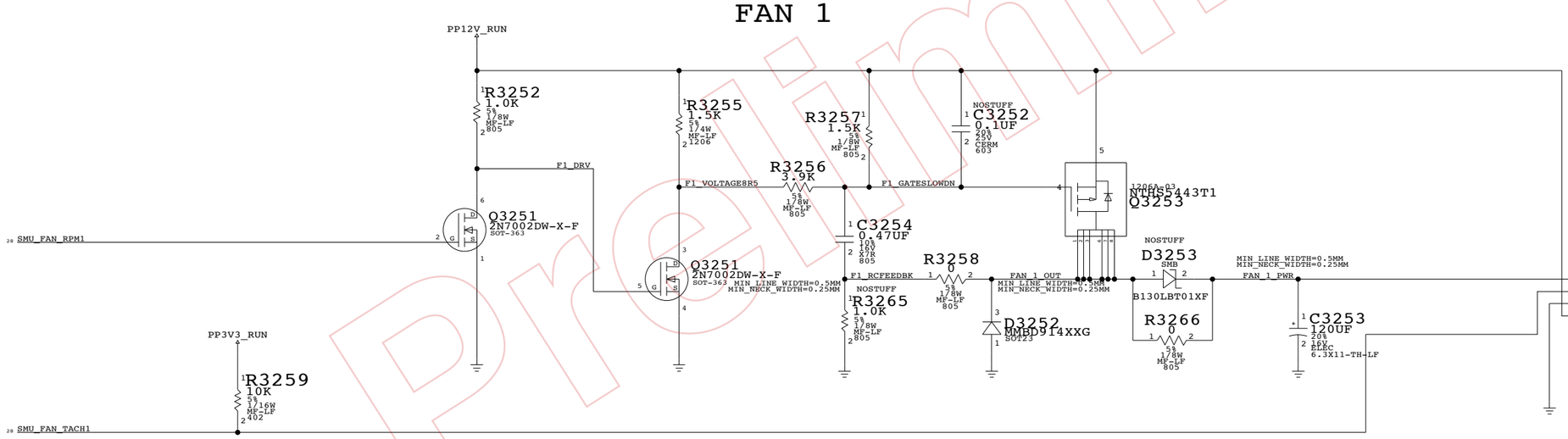
FAN 0



M23: ODD FAN

M33: ODD FAN

FAN 1



M23: HD FAN

M33: CPU FAN

Fan 0, 1 & System Temp

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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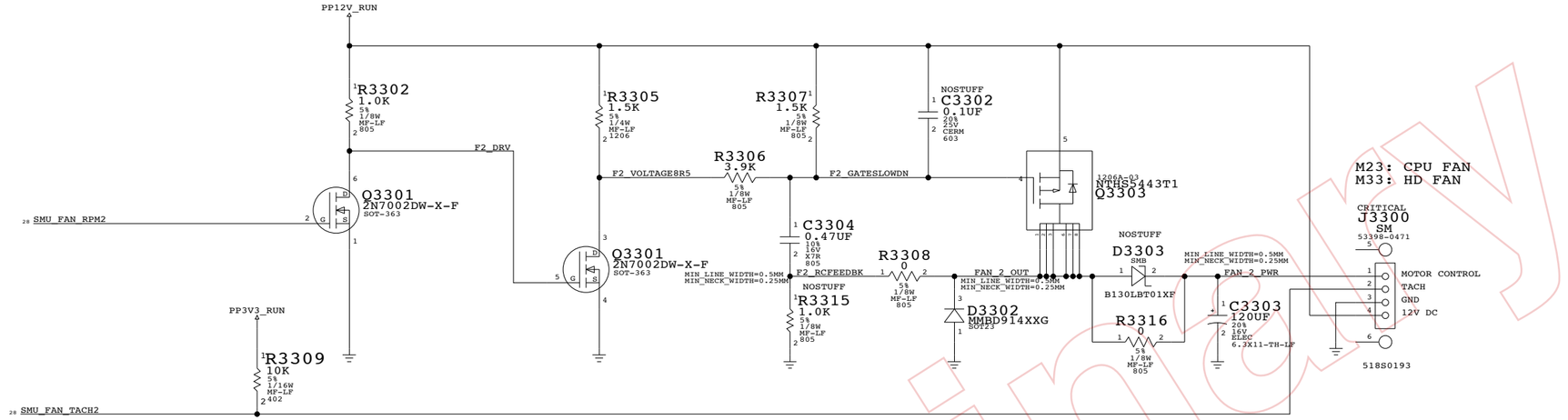
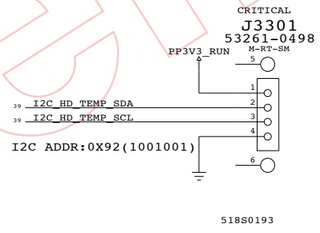
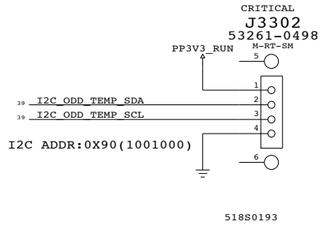
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR



Fan 2 & HD Temp

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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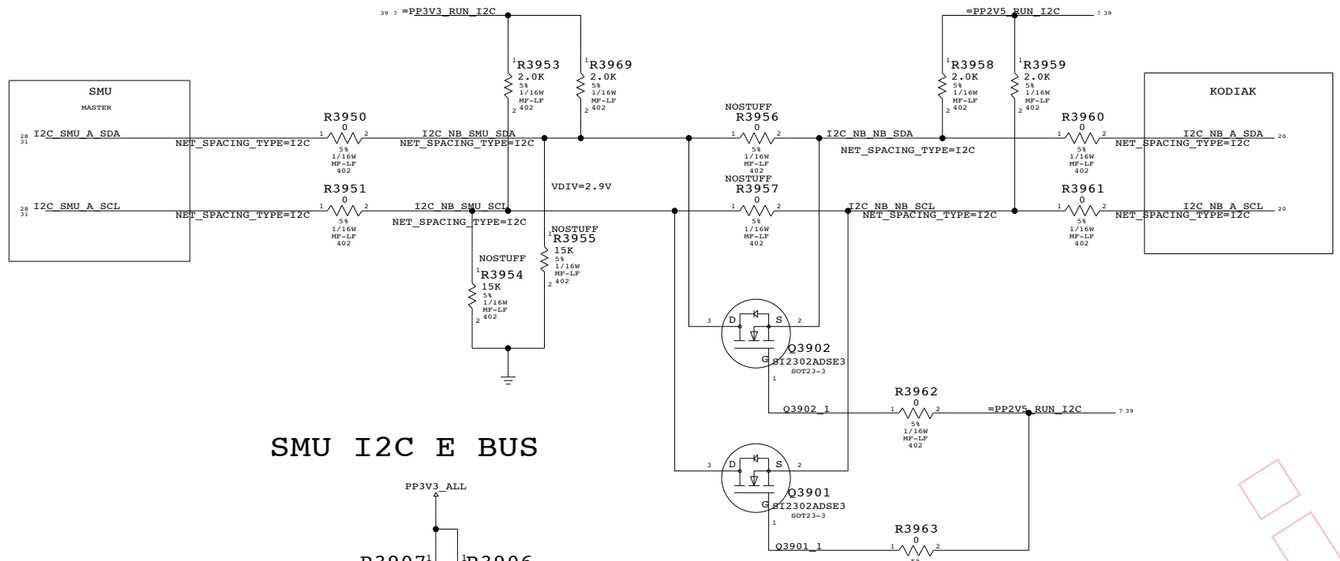
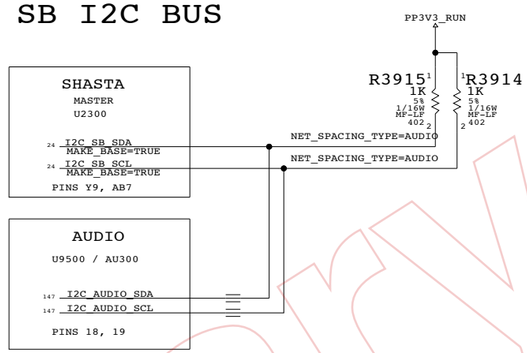
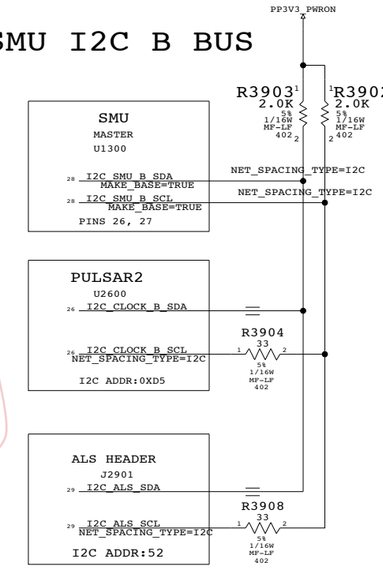
SMU AND NB I2C A BUS



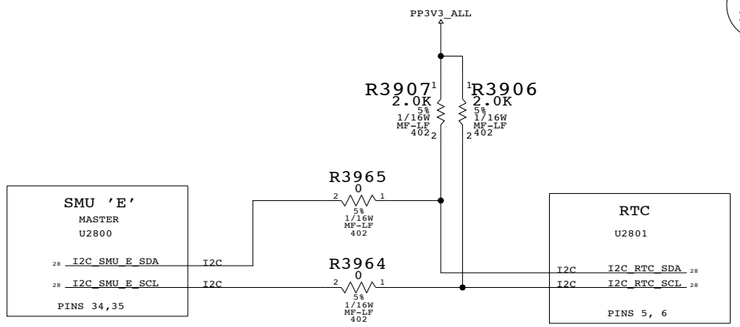
SB I2C BUS



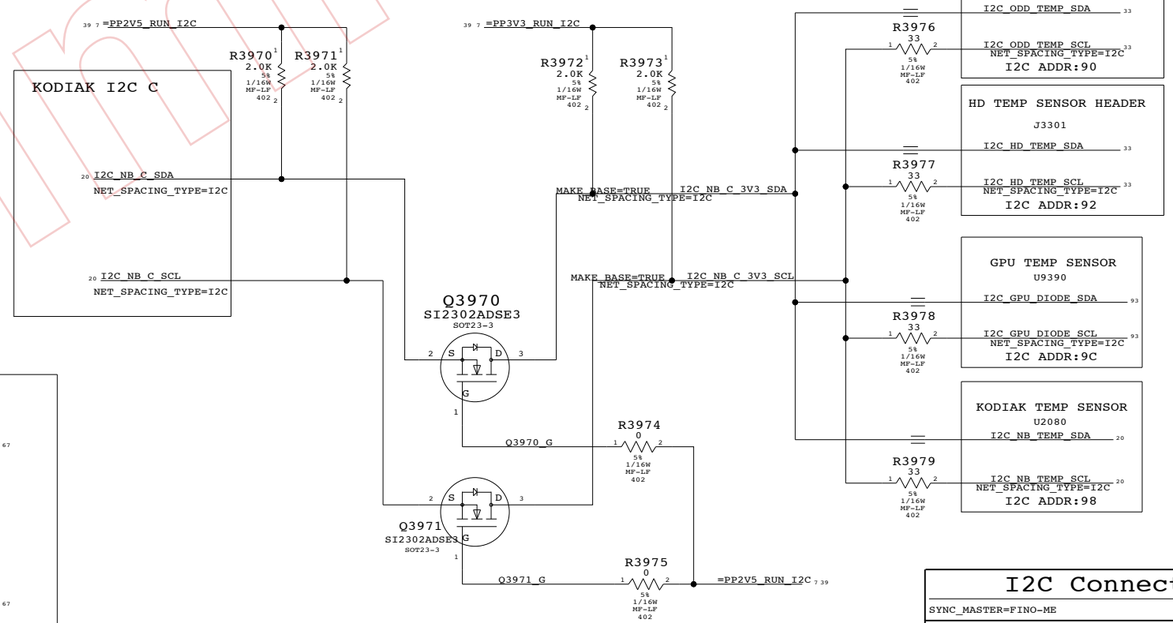
SMU I2C B BUS



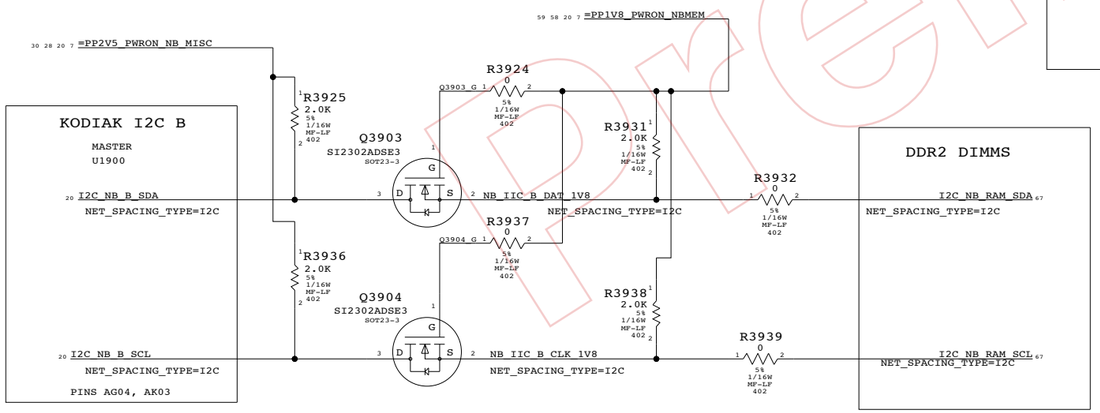
SMU I2C E BUS



NB I2C C BUS



NB I2C B BUS



I2C Connections

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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SCALE: NONE	SHT 39 OF 154	

LAST_MODIFIED=Thu May 19 14:26:53 2005

KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.

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D	051-6863	07
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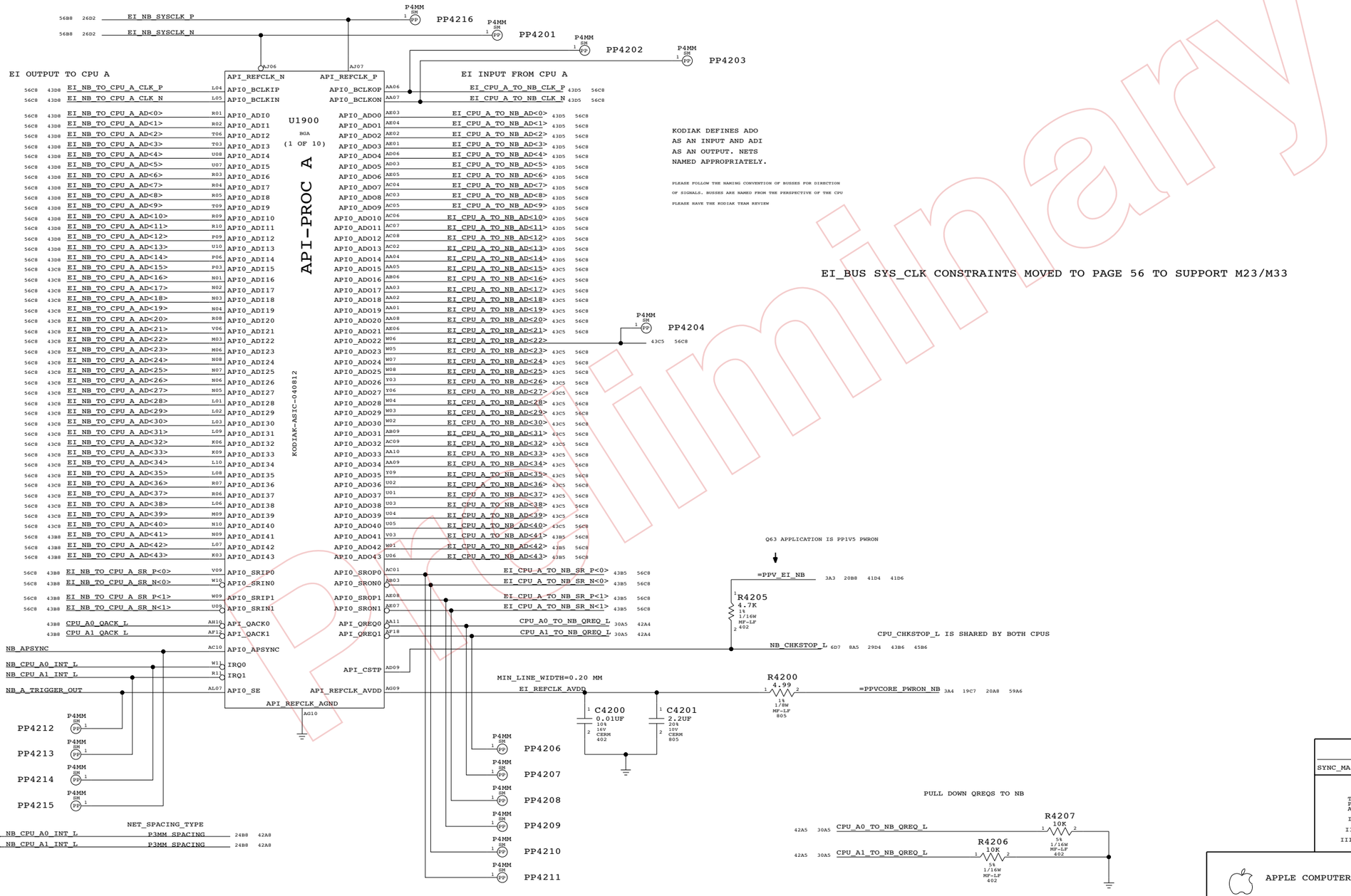

KODIAK EI A

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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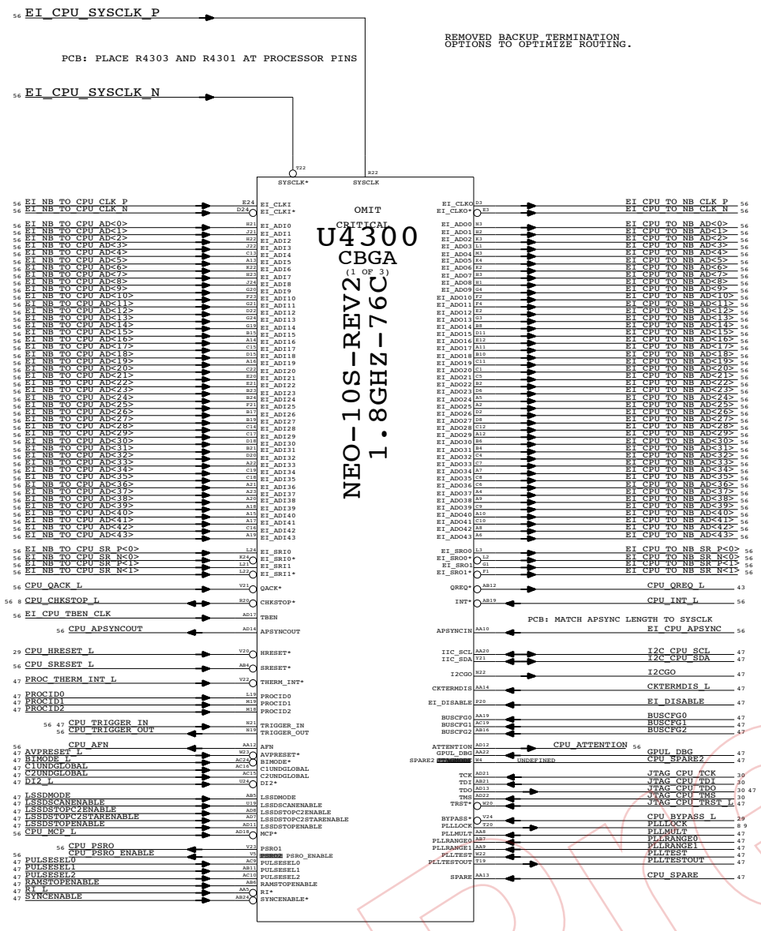
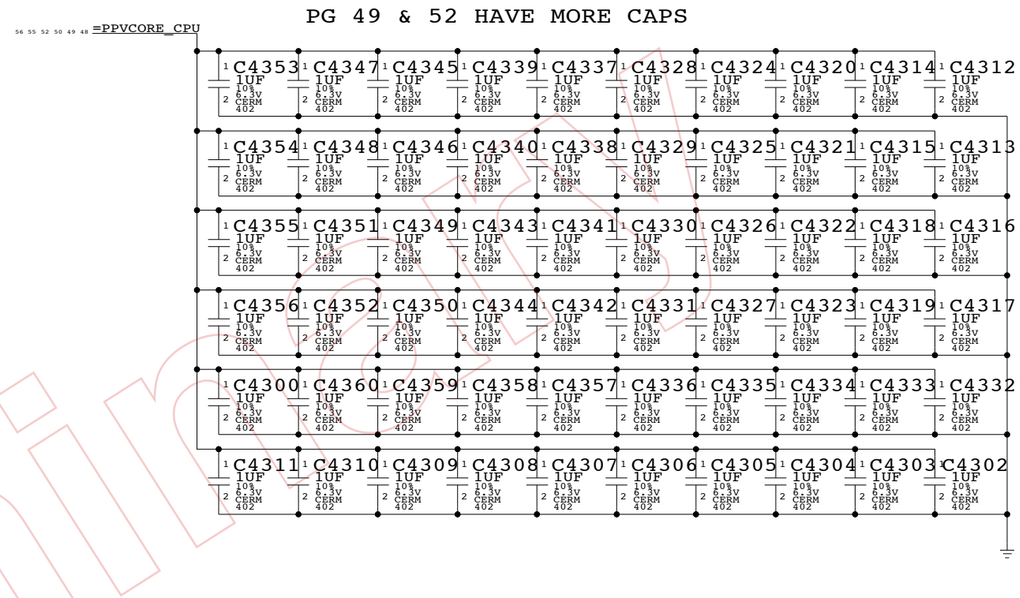
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

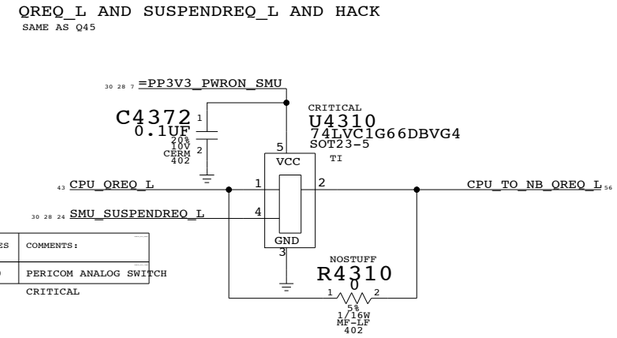
SCALE	SHT	OF
NONE	42	154

LAST_MODIFIED=Thu May 19 14:26:53 2005

DRAWING







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U4310	PERICOM ANALOG SWITCH CRITICAL

CPU EI AND IO

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	43	154

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

56B8	45D8	EI_NB_TO_CPU_B_CLK_P	AT08	API1_BCLKIP	
56B8	45D8	EI_NB_TO_CPU_B_CLK_N	AR08	API1_BCLKIN	
56B8	45D8	EI_NB_TO_CPU_B_AD<0>	AM12	API1_ADI0	
56B8	45D8	EI_NB_TO_CPU_B_AD<1>	AN12	API1_ADI1	
56B8	45D8	EI_NB_TO_CPU_B_AD<2>	AL12	API1_ADI2	
56B8	45D8	EI_NB_TO_CPU_B_AD<3>	AK12	API1_ADI3	
56B8	45D8	EI_NB_TO_CPU_B_AD<4>	AP11	API1_ADI4	
56B8	45D8	EI_NB_TO_CPU_B_AD<5>	AL11	API1_ADI5	
56B8	45D8	EI_NB_TO_CPU_B_AD<6>	AP12	API1_ADI6	
56B8	45D8	EI_NB_TO_CPU_B_AD<7>	AR12	API1_ADI7	
56B8	45D8	EI_NB_TO_CPU_B_AD<8>	AT12	API1_ADI8	
56B8	45D8	EI_NB_TO_CPU_B_AD<9>	AH12	API1_ADI9	
56B8	45D8	EI_NB_TO_CPU_B_AD<10>	AG12	API1_ADI10	
56B8	45D8	EI_NB_TO_CPU_B_AD<11>	AH13	API1_ADI11	
56B8	45D8	EI_NB_TO_CPU_B_AD<12>	AJ12	API1_ADI12	
56B8	45D8	EI_NB_TO_CPU_B_AD<13>	AG14	API1_ADI13	
56B8	45C8	EI_NB_TO_CPU_B_AD<14>	AM10	API1_ADI14	
56B8	45C8	EI_NB_TO_CPU_B_AD<15>	AL10	API1_ADI15	
56B8	45C8	EI_NB_TO_CPU_B_AD<16>	AN10	API1_ADI16	
56B8	45C8	EI_NB_TO_CPU_B_AD<17>	AP10	API1_ADI17	
56B8	45C8	EI_NB_TO_CPU_B_AD<18>	AR10	API1_ADI18	
56B8	45C8	EI_NB_TO_CPU_B_AD<19>	AT10	API1_ADI19	
56B8	45C8	EI_NB_TO_CPU_B_AD<20>	AK10	API1_ADI20	
56B8	45C8	EI_NB_TO_CPU_B_AD<21>	AJ10	API1_ADI21	
56B8	45C8	EI_NB_TO_CPU_B_AD<22>	AM08	API1_ADI22	
56B8	45C8	EI_NB_TO_CPU_B_AD<23>	AN08	API1_ADI23	
56B8	45C8	EI_NB_TO_CPU_B_AD<24>	AL08	API1_ADI24	
56B8	45C8	EI_NB_TO_CPU_B_AD<25>	AP07	API1_ADI25	
56B8	45C8	EI_NB_TO_CPU_B_AD<26>	AT06	API1_ADI26	
56B8	45C8	EI_NB_TO_CPU_B_AD<27>	AR06	API1_ADI27	
56B8	45C8	EI_NB_TO_CPU_B_AD<28>	AP08	API1_ADI28	
56B8	45C8	EI_NB_TO_CPU_B_AD<29>	AT04	API1_ADI29	
56B8	45C8	EI_NB_TO_CPU_B_AD<30>	AR04	API1_ADI30	
56B8	45C8	EI_NB_TO_CPU_B_AD<31>	AP05	API1_ADI31	
56B8	45C8	EI_NB_TO_CPU_B_AD<32>	AM06	API1_ADI32	
56B8	45C8	EI_NB_TO_CPU_B_AD<33>	AN06	API1_ADI33	
56B8	45C8	EI_NB_TO_CPU_B_AD<34>	AP06	API1_ADI34	
56B8	45C8	EI_NB_TO_CPU_B_AD<35>	AP04	API1_ADI35	
56B8	45C8	EI_NB_TO_CPU_B_AD<36>	AM03	API1_ADI36	
56B8	45C8	EI_NB_TO_CPU_B_AD<37>	AN01	API1_ADI37	
56B8	45C8	EI_NB_TO_CPU_B_AD<38>	AL06	API1_ADI38	
56B8	45C8	EI_NB_TO_CPU_B_AD<39>	AL05	API1_ADI39	
56B8	45B8	EI_NB_TO_CPU_B_AD<40>	AL04	API1_ADI40	
56B8	45B8	EI_NB_TO_CPU_B_AD<41>	AL03	API1_ADI41	
56B8	45B8	EI_NB_TO_CPU_B_AD<42>	AN02	API1_ADI42	
56B8	45B8	EI_NB_TO_CPU_B_AD<43>	AN03	API1_ADI43	
56B8	45B8	EI_NB_TO_CPU_B_SR_P<0>	AP09	API1_SRIP0	
56B8	45B8	EI_NB_TO_CPU_B_SR_N<0>	AL09	API1_SRIN0	
56B8	45B8	EI_NB_TO_CPU_B_SR_P<1>	AR02	API1_SRIP1	
56B8	45B8	EI_NB_TO_CPU_B_SR_N<1>	AP03	API1_SRIN1	
	45B8	CPU_B0_QACK_L	AF14	API_QACK2	
	45B8	CPU_B1_QACK_L	AC13	API_QACK3	
44A7	24B8	NB_CPU_B0_INT_L	N11	IRQ2	
44A7	24A8	NB_CPU_B1_INT_L	U11	IRQ3	
		TP_NB_APSYNC	AH11	API1_APSYNC	
	45A6	NB_B_TRIGGER_OUT	AK08	API1_SE	

U1900
BGA
(2 OF 10)

API-PROC B

KODIAK-ASIC-040812

EI INPUT FROM CPU B

API1_BCLKOP	AT16	EI_CPU_B_TO_NB_CLK_P	45D6	56B8	
API1_BCLKON	AR16	EI_CPU_B_TO_NB_CLK_N	45D6	56B8	
API1_ADO0	AP20	EI_CPU_B_TO_NB_AD<0>	45D6	56B8	
API1_ADO1	AN20	EI_CPU_B_TO_NB_AD<1>	45D6	56B8	
API1_ADO2	AR20	EI_CPU_B_TO_NB_AD<2>	45D6	56B8	
API1_ADO3	AT20	EI_CPU_B_TO_NB_AD<3>	45D6	56B8	
API1_ADO4	AL19	EI_CPU_B_TO_NB_AD<4>	45D6	56B8	
API1_ADO5	AP19	EI_CPU_B_TO_NB_AD<5>	45D6	56B8	
API1_ADO6	AM20	EI_CPU_B_TO_NB_AD<6>	45D6	56B8	
API1_ADO7	AM18	EI_CPU_B_TO_NB_AD<7>	45D6	56B8	
API1_ADO8	AL18	EI_CPU_B_TO_NB_AD<8>	45D6	56B8	
API1_ADO9	AN18	EI_CPU_B_TO_NB_AD<9>	45D6	56B8	
API1_ADO10	AP18	EI_CPU_B_TO_NB_AD<10>	45D6	56B8	
API1_ADO11	AR18	EI_CPU_B_TO_NB_AD<11>	45D6	56B8	
API1_ADO12	AT18	EI_CPU_B_TO_NB_AD<12>	45D6	56B8	
API1_ADO13	AK18	EI_CPU_B_TO_NB_AD<13>	45D6	56B8	
API1_ADO14	AP17	EI_CPU_B_TO_NB_AD<14>	45C6	56B8	
API1_ADO15	AL17	EI_CPU_B_TO_NB_AD<15>	45C6	56B8	
API1_ADO16	AH20	EI_CPU_B_TO_NB_AD<16>	45C6	56B8	
API1_ADO17	AJ20	EI_CPU_B_TO_NB_AD<17>	45C6	56B8	
API1_ADO18	AK20	EI_CPU_B_TO_NB_AD<18>	45C6	56B8	
API1_ADO19	AH19	EI_CPU_B_TO_NB_AD<19>	45C6	56B8	
API1_ADO20	AG20	EI_CPU_B_TO_NB_AD<20>	45C6	56B8	
API1_ADO21	AL20	EI_CPU_B_TO_NB_AD<21>	45C6	56B8	
API1_ADO22	AM16	EI_CPU_B_TO_NB_AD<22>	45C6	56B8	
API1_ADO23	AN16	EI_CPU_B_TO_NB_AD<23>	45C6	56B8	
API1_ADO24	AL16	EI_CPU_B_TO_NB_AD<24>	45C6	56B8	
API1_ADO25	AK16	EI_CPU_B_TO_NB_AD<25>	45C6	56B8	
API1_ADO26	AP15	EI_CPU_B_TO_NB_AD<26>	45C6	56B8	
API1_ADO27	AL15	EI_CPU_B_TO_NB_AD<27>	45C6	56B8	
API1_ADO28	AP16	EI_CPU_B_TO_NB_AD<28>	45C6	56B8	
API1_ADO29	AM14	EI_CPU_B_TO_NB_AD<29>	45C6	56B8	
API1_ADO30	AL14	EI_CPU_B_TO_NB_AD<30>	45C6	56B8	
API1_ADO31	AN14	EI_CPU_B_TO_NB_AD<31>	45C6	56B8	
API1_ADO32	AP14	EI_CPU_B_TO_NB_AD<32>	45C6	56B8	
API1_ADO33	AR14	EI_CPU_B_TO_NB_AD<33>	45C6	56B8	
API1_ADO34	AT14	EI_CPU_B_TO_NB_AD<34>	45C6	56B8	
API1_ADO35	AK14	EI_CPU_B_TO_NB_AD<35>	45C6	56B8	
API1_ADO36	AP13	EI_CPU_B_TO_NB_AD<36>	45C6	56B8	
API1_ADO37	AL13	EI_CPU_B_TO_NB_AD<37>	45C6	56B8	
API1_ADO38	AG16	EI_CPU_B_TO_NB_AD<38>	45C6	56B8	
API1_ADO39	AH15	EI_CPU_B_TO_NB_AD<39>	45C6	56B8	
API1_ADO40	AJ14	EI_CPU_B_TO_NB_AD<40>	45B6	56B8	
API1_ADO41	AH14	EI_CPU_B_TO_NB_AD<41>	45B6	56B8	
API1_ADO42	AH16	EI_CPU_B_TO_NB_AD<42>	45B6	56B8	
API1_ADO43	AH17	EI_CPU_B_TO_NB_AD<43>	45B6	56B8	
API1_SROP0	AG18	EI_CPU_B_TO_NB_SR_P<0>	45B6	56B8	
API1_SRON0	AJ16	EI_CPU_B_TO_NB_SR_N<0>	45B6	56B8	
API1_SROP1	AJ18	EI_CPU_B_TO_NB_SR_P<1>	45B6	56B8	
API1_SRON1	AH18	EI_CPU_B_TO_NB_SR_N<1>	45B6	56B8	
API_QREQ2	AF16	CPU_B0_TO_NB_QREQ_L	30A3	44A5	
API_QREQ3	AF20	CPU_B1_TO_NB_QREQ_L	30A3	44A5	

KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT ELECTRICAL_CONSTRAINT_SET FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

P4MM SM 1 PP
PP4410, PP4411, PP4413, PP4400, PP4401, PP4402, PP4403, PP4404, PP4405, PP4406, PP4407, PP4408

WIRE TP_NB_APSYNC TO A TEST POINT

NET_SPACING_TYPE

NB_CPU_B0_INT_L	P3MM_SPACING	24B8	44B8	
NB_CPU_B1_INT_L	P3MM_SPACING	24A8	44B8	

PULL DOWN QREQS TO NB

44B5	30A3	CPU_B0_TO_NB_QREQ_L	R4407	10K	5% 1/16W MF-LF 402
44B5	30A3	CPU_B1_TO_NB_QREQ_L	R4406	10K	5% 1/16W MF-LF 402

KODIAK EI B

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	44	154

LAST_MODIFIED=Thu May 19 14:26:55 2005

DRAWING

=PPV_EI_CPU 7 29 30 47 48 56

PULLUPS

43 C1UNDGLOBAL
- NOSTUFF R4777 4.7K 5% 1/16W MF-LF 402
- R4743 4.7K 5% 1/16W MF-LF 402

43 C2UNDGLOBAL
- NOSTUFF R4779 4.7K 5% 1/16W MF-LF 402
- R4769 4.7K 5% 1/16W MF-LF 402

43 PLLTEST
- NOSTUFF R4763 4.7K 5% 1/16W MF-LF 402
- R4761 4.7K 5% 1/16W MF-LF 402

43 CKTERMDIS_L
- NOSTUFF R4775 4.7K 5% 1/16W MF-LF 402
- R4773 4.7K 5% 1/16W MF-LF 402

43 GPUL_DBG
- R4740 4.7K 5% 1/16W MF-LF 402
- NOSTUFF R4742 4.7K 5% 1/16W MF-LF 402

M23/M33 IS JTAG ONLY, NO I2C

43 JTAG_CPU_TRST_L — R4709 4.7K 5% 1/16W MF-LF 402
43 BIMODE_L — R4731 4.7K 5% 1/16W MF-LF 402
43 DI2_L — R4733 4.7K 5% 1/16W MF-LF 402
43 RI_L — R4735 4.7K 5% 1/16W MF-LF 402
43 PROC_THERM_INT_L — R4765 4.7K 5% 1/16W MF-LF 402
43 I2CGO — R4787 4.7K 5% 1/16W MF-LF 402
43 I2C_CPU_SCL — R4788 4.7K 5% 1/16W MF-LF 402
43 I2C_CPU_SDA — R4789 4.7K 5% 1/16W MF-LF 402
43 30 JTAG_CPU_TDO — R4790 4.7K 5% 1/16W MF-LF 402

PULLDOWNS

43 CPU_SPARE2 — NOSTUFF R4739 0 5% 1/16W MF-LF 402
43 LSSDMODE — R4745 4.7K 5% 1/16W MF-LF 402
43 LSSDSCANENABLE — R4741 4.7K 5% 1/16W MF-LF 402
43 LSSDSTOPC2ENABLE — R4747 4.7K 5% 1/16W MF-LF 402
43 LSSDSTOPC2STARENABLE — R4749 4.7K 5% 1/16W MF-LF 402
43 LSSDSTOPENABLE — R4751 4.7K 5% 1/16W MF-LF 402
43 SYNCENABLE — R4737 4.7K 5% 1/16W MF-LF 402
43 RAMSTOPENABLE — R4755 4.7K 5% 1/16W MF-LF 402
43 CPU_SPARE — NOSTUFF R4767 4.7K 5% 1/16W MF-LF 402
56 43 CPU_TRIGGER_IN — R4781 4.7K 5% 1/16W MF-LF 402
43 PULSESEL0 — R4703 4.7K 5% 1/16W MF-LF 402
43 PULSESEL1 — R4705 4.7K 5% 1/16W MF-LF 402
43 PULSESEL2 — R4707 4.7K 5% 1/16W MF-LF 402
43 PROCID0 — R4702 4.7K 5% 1/16W MF-LF 402
43 PROCID1 — R4704 4.7K 5% 1/16W MF-LF 402
43 PROCID2 — R4706 4.7K 5% 1/16W MF-LF 402
43 PLLTESTOUT — NOSTUFF R4771 4.7K 5% 1/16W MF-LF 402

=PPV_EI_CPU 7 29 30 47 48 56
1 R4768 10K 5% 1/16W MF-LF 2 402

NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	
>= 1.8 GHZ *	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION

56 48 47 30 29 7 =PPV_EI_CPU

SEE STUFFING OPTIONS ABOVE

1 OMIT R4708 1K 5% 1/16W MF-LF 2 402	1 OMIT R4710 1K 5% 1/16W MF-LF 2 402	1 OMIT R4712 1K 5% 1/16W MF-LF 2 402	1 OMIT R4714 1K 5% 1/16W MF-LF 2 402	1 OMIT R4716 1K 5% 1/16W MF-LF 2 402	1 OMIT R4718 1K 5% 1/16W MF-LF 2 402	1 OMIT R4720 1K 5% 1/16W MF-LF 2 402	1 OMIT R4722 1K 5% 1/16W MF-LF 2 402	
43 BUSCFG0								
43 BUSCFG1								
43 BUSCFG2								
43 PLLRANGE0								
43 PLLRANGE1								
43 PLLMULT								
43 EI_DISABLE								
43 AVPRESET_L								
1 OMIT R4724 1K 5% 1/16W MF-LF 2 402	1 OMIT R4726 1K 5% 1/16W MF-LF 2 402	1 OMIT R4728 1K 5% 1/16W MF-LF 2 402	1 OMIT R4730 1K 5% 1/16W MF-LF 2 402	1 OMIT R4732 1K 5% 1/16W MF-LF 2 402	1 OMIT R4734 1K 5% 1/16W MF-LF 2 402	1 OMIT R4736 1K 5% 1/16W MF-LF 2 402	1 OMIT R4738 1K 5% 1/16W MF-LF 2 402	

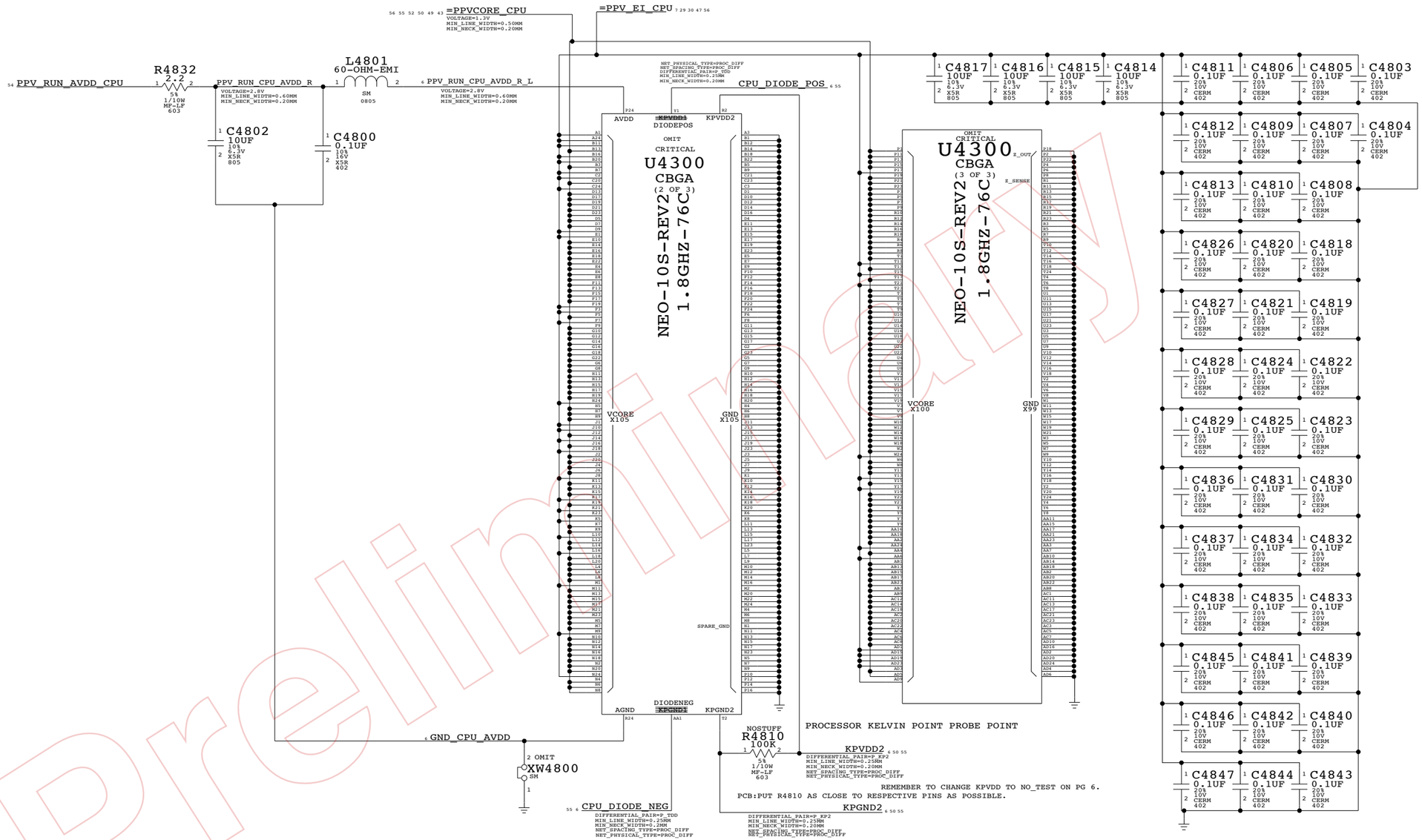
CPU STRAPS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	47	154



CPU POWER AND BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	48	154

56 55 52 50 48 43 =PPVCORE_CPU

C4922 1UF 10% 6.3V CERM 402	C4921 1UF 10% 6.3V CERM 402	C4920 1UF 10% 6.3V CERM 402	C4919 1UF 10% 6.3V CERM 402	C4918 1UF 10% 6.3V CERM 402	C4917 1UF 10% 6.3V CERM 402	C4916 1UF 10% 6.3V CERM 402	C4915 1UF 10% 6.3V CERM 402	C4912 1UF 10% 6.3V CERM 402	C4900 1UF 10% 6.3V CERM 402
C4993 1UF 10% 6.3V CERM 402	C4968 1UF 10% 6.3V CERM 402	C4961 1UF 10% 6.3V CERM 402	C4959 1UF 10% 6.3V CERM 402	C4935 1UF 10% 6.3V CERM 402	C4932 1UF 10% 6.3V CERM 402	C4926 1UF 10% 6.3V CERM 402	C4924 1UF 10% 6.3V CERM 402	C4945 1UF 10% 6.3V CERM 402	C4923 1UF 10% 6.3V CERM 402
C4994 1UF 10% 6.3V CERM 402	C4969 1UF 10% 6.3V CERM 402	C4964 1UF 10% 6.3V CERM 402	C4960 1UF 10% 6.3V CERM 402	C4936 1UF 10% 6.3V CERM 402	C4933 1UF 10% 6.3V CERM 402	C4927 1UF 10% 6.3V CERM 402	C4925 1UF 10% 6.3V CERM 402	C4956 1UF 10% 6.3V CERM 402	C4934 1UF 10% 6.3V CERM 402
C4995 1UF 10% 6.3V CERM 402	C4971 1UF 10% 6.3V CERM 402	C4965 1UF 10% 6.3V CERM 402	C4962 1UF 10% 6.3V CERM 402	C4939 1UF 10% 6.3V CERM 402	C4937 1UF 10% 6.3V CERM 402	C4930 1UF 10% 6.3V CERM 402	C4928 1UF 10% 6.3V CERM 402	C4989 1UF 10% 6.3V CERM 402	C4967 1UF 10% 6.3V CERM 402
C4996 1UF 10% 6.3V CERM 402	C4970 1UF 10% 6.3V CERM 402	C4966 1UF 10% 6.3V CERM 402	C4963 1UF 10% 6.3V CERM 402	C4940 1UF 10% 6.3V CERM 402	C4938 1UF 10% 6.3V CERM 402	C4931 1UF 10% 6.3V CERM 402	C4929 1UF 10% 6.3V CERM 402	C4901 1UF 10% 6.3V CERM 402	C4978 1UF 10% 6.3V CERM 402
C4997 1UF 10% 6.3V CERM 402	C4982 1UF 10% 6.3V CERM 402	C4976 1UF 10% 6.3V CERM 402	C4972 1UF 10% 6.3V CERM 402	C4952 1UF 10% 6.3V CERM 402	C4950 1UF 10% 6.3V CERM 402	C4943 1UF 10% 6.3V CERM 402	C4941 1UF 10% 6.3V CERM 402	C4906 1UF 10% 6.3V CERM 402	C4904 1UF 10% 6.3V CERM 402
C4998 1UF 10% 6.3V CERM 402	C4981 1UF 10% 6.3V CERM 402	C4977 1UF 10% 6.3V CERM 402	C4973 1UF 10% 6.3V CERM 402	C4953 1UF 10% 6.3V CERM 402	C4951 1UF 10% 6.3V CERM 402	C4944 1UF 10% 6.3V CERM 402	C4942 1UF 10% 6.3V CERM 402	C4907 1UF 10% 6.3V CERM 402	C4905 1UF 10% 6.3V CERM 402
C4999 1UF 10% 6.3V CERM 402	C4984 1UF 10% 6.3V CERM 402	C4979 1UF 10% 6.3V CERM 402	C4974 1UF 10% 6.3V CERM 402	C4957 1UF 10% 6.3V CERM 402	C4954 1UF 10% 6.3V CERM 402	C4948 1UF 10% 6.3V CERM 402	C4946 1UF 10% 6.3V CERM 402	C4910 1UF 10% 6.3V CERM 402	C4908 1UF 10% 6.3V CERM 402
C4902 1UF 10% 6.3V CERM 402	C4983 1UF 10% 6.3V CERM 402	C4980 1UF 10% 6.3V CERM 402	C4975 1UF 10% 6.3V CERM 402	C4958 1UF 10% 6.3V CERM 402	C4955 1UF 10% 6.3V CERM 402	C4949 1UF 10% 6.3V CERM 402	C4947 1UF 10% 6.3V CERM 402	C4911 1UF 10% 6.3V CERM 402	C4909 1UF 10% 6.3V CERM 402
C4903 1UF 10% 6.3V CERM 402	C4992 1UF 10% 6.3V CERM 402	C4991 1UF 10% 6.3V CERM 402	C4990 1UF 10% 6.3V CERM 402	C4988 1UF 10% 6.3V CERM 402	C4987 1UF 10% 6.3V CERM 402	C4986 1UF 10% 6.3V CERM 402	C4985 1UF 10% 6.3V CERM 402	C4914 1UF 10% 6.3V CERM 402	C4913 1UF 10% 6.3V CERM 402

PROC DECOUPLING

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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SCALE NONE	SHT 49 OF 154	

VCORE VOLTAGE CONTROLLER (VC)

M23/M33: PP12V_CPU IS AN ALL RAIL

=PP12V_CPU
R5029 10 5% 1/16W MF-LF 402
VC_VCC
C5019 1UF 20% 16V CERM 1206
SYS_POWERUP_L
R5000 1.5K 5% 1/16W MF-LF 402
VRM_EN
Q5012 2N7002 SOT23-LF
C5001 1UF 10% 6.3V CERM 402
VC_AGND
VC_BGOUT
VC_OSCREF
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
CPU_VID_R<3>
CPU_VID_R<4>
CPU_VID_R<5>
U5000 SC2642 TSSOP
BGOUT OSCREF VID0 VID1 VID2 VID3 VID4 VID5 DACSTEP FB GSENSE OS1 OS2 VCC OUTSEN OUT1 OUT2 PGOOD ERROUT AGND
VC_OUTSEN
VC_OUT1
VC_OUT2
VC_PGOOD
PGOOD IS OC
R5030 0 5% 1/16W MF-LF 402
SYS_SLEWING_L
NOSTUFF R5003 2.7M 5% 1/10W MF-LF 603
VC_VCC
VC_DACSTEP
VC_ERROUT
R5001 20K 5% 1/16W MF-LF 402
NOSTUFF R5002 0 5% 1/16W MF-LF 402
VC_ERROUT_RC
C5002 470PF 10% 50V CERM 402
OMIT XW5000 SM
VC_OS1
VC_OS2
C5000 0.1UF 20% 10V CERM 402
R5028 221K 1% 1/16W MF-LF 402
VC_AGND

VC_AUX1
VC_AUX2
R5013 20.5K 1% 1/16W MF-LF 402
R5016 20.5K 1% 1/16W MF-LF 402
C5004 0.0082UF 10% 25V X7R 402
NOSTUFF R5014 20.5K 1% 1/16W MF-LF 402
C5005 0.0082UF 10% 25V X7R 402
NOSTUFF R5015 20.5K 1% 1/16W MF-LF 402
VCORE_SENSE_GND
DIFFERENTIAL PAIR FOR REMOTE SENSE
VCORE_SENSE_VOUT
VC_OUTSEN
R5005 4.99K 1% 1/16W MF-LF 402
VC_VCC
VC_OS_HUB
R5004 261 1% 1/16W MF-LF 402
C5008 0.068UF 10% 10V CERM 402
R5026 301 1% 1/16W MF-LF 402
AVP ADJUSTMENT
NOSTUFF R5024 330 5% 1/16W MF-LF 402
NOSTUFF R5025 1K 1% 1/16W MF-LF 402
VC_OS_HUB_RC
PCB:PLACE R5025 CLOSE TO INDUCTOR OUTPUT LEAD.
NOSTUFF C5009 0.015UF 10% 16V X7R 402
R5027 1.5K 1% 1/16W MF-LF 402
VC_OUTSEN_R
OMIT XW5002 SM
=PPVCORE_CPU
PCB:CONNECT BETWEEN THE INDUCTOR & BULK CAPS.

VC PROCESSOR VOLTAGE SENSING

CHOICE OF:
1) VCORE PLANE SENSING
2) KELVIN POINT SENSING

_PPVCORE_CPU
R5035 0 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
UNDER PROCESSOR
R5036 0 5% 1/16W MF-LF 402
VCORE_SENSE_VOUT
VCORE_SENSE_GND
KPVDD2
NOSTUFF R5041 0 5% 1/16W MF-LF 402
CPU SENSE SIDE
KPGND2
NOSTUFF R5042 0 5% 1/16W MF-LF 402

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD1_DRN	0.25 MM	0.25 MM
GD1_BST	0.25 MM	0.25 MM
GD1_VREG	0.25 MM	0.25 MM
GD1_VPN	0.25 MM	0.25 MM
GD1_TG	0.25 MM	0.25 MM
GD1_BG	0.25 MM	0.25 MM
GD1_FET_RC	0.25 MM	0.25 MM
GD1_PN	0.60 MM	0.25 MM
GD1_BST_R	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD2_DRN	0.25 MM	0.25 MM
GD2_BST	0.25 MM	0.25 MM
GD2_VREG	0.25 MM	0.25 MM
GD2_VPN	0.25 MM	0.25 MM
GD2_TG	0.25 MM	0.25 MM
GD2_BG	0.25 MM	0.25 MM
GD2_FET_RC	0.25 MM	0.25 MM
GD2_PN	0.60 MM	0.25 MM
GD2_BST_R	0.25 MM	0.25 MM

VCORE SUPPLY PHASE 1 (GD1)

C5010 1UF 20% 16V CERM 1206
GD1_BST_R
GD1_DRN
PP12V_CPU_R_L
U5010 SC1211 SOIC
VIN CO DRN BST BG VREG TG VPN THMPAD
VC_OUT1
C5029 1UF 20% 16V CERM 1206
R5007 2.2 5% 1/10W MF-LF 603
GD1_BST
D5010 BAS16 SOT23
GD1_VREG
C5013 1UF 20% 16V CERM 1206
GD1_TG
Q5010 NTD60N02R CASE369 CRITICAL
R5050 10K 5% 1/16W MF-LF 402
R5010 1 5% 1/16W MF-LF 402
GD1_VPN
R5012 200 5% 1/16W MF-LF 402
VC_AUX1
C5014 470PF 10% 50V CERM 402
GD1_PN
C5011 330UF 20% 16V ELEC SM-3
C5035 330UF 20% 16V ELEC SM-3
C5012 10UF 10% 16V CERM 1210 CRITICAL
L5010 0.36UH-30A-0.80MOHM SM
=PPVCORE_CPU
PPVCORE_CPU MAKE_BASE=TRUE
C5018 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5017 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5032 1500UF 20% 6.3V ELEC TH-MCZ
C5038 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
R5011 1 5% 1/8W MF-LF 805
GD1_BG
Q5011 NTD70N03R CASE369 CRITICAL
GD1_FET_RC
Q5013 NTD70N03R CASE369 CRITICAL
NOSTUFF C5015 0.0022UF 10% 50V CERM 402
C5016 0.0047UF 10% 25V CERM 402
NEED TO CHANGE TO 10MOHM CAPS - 8 PCS

VCORE SUPPLY PHASE 2 (GD2)

C5020 1UF 20% 16V CERM 1206
GD2_BST_R
GD2_DRN
PP12V_CPU_R_L
U5020 SC1211 SOIC
VIN CO DRN BST BG VREG TG VPN THMPAD
VC_OUT2
C5030 1UF 20% 16V CERM 1206
R5006 2.2 5% 1/10W MF-LF 603
GD2_BST
D5020 BAS16 SOT23
GD2_VREG
C5023 1UF 20% 16V CERM 1206
GD2_TG
Q5020 NTD60N02R CASE369 CRITICAL
R5051 10K 5% 1/16W MF-LF 402
R5020 1 5% 1/16W MF-LF 402
GD2_VPN
R5022 200 5% 1/16W MF-LF 402
VC_AUX2
C5024 470PF 10% 50V CERM 402
GD2_PN
C5021 1000UF 20% 16V ELEC TH-REJ-LF
C5022 10UF 10% 16V CERM 1210
L5020 0.36UH-30A-0.80MOHM SM
PPVCORE_CPU
C5028 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5033 1800UF 20% 6.3V ELEC TH-KZJ-LF
C5040 1500UF 20% 6.3V ELEC TH-MCZ
C5041 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5042 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
R5021 1 5% 1/8W MF-LF 805
GD2_BG
Q5021 NTD70N03R CASE369 CRITICAL
GD2_FET_RC
Q5023 NTD70N03R CASE369 CRITICAL
NOSTUFF C5025 0.0022UF 10% 50V CERM 402
C5026 0.0047UF 10% 25V CERM 402
NEED TO CHANGE TO 10MOHM CAPS - 8 PCS

PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
VC_OSCREF	0.25 MM	0.20 MM
CPU_VID_R<0..5>	0.25 MM	0.20 MM
VC_DACSTEP	0.25 MM	0.20 MM
VC_AGND	0.50 MM	0.20 MM
VC_BGOUT	0.25 MM	0.20 MM
VC_OS1	0.25 MM	0.20 MM
VC_OS2	0.25 MM	0.20 MM
VC_VCC	0.25 MM	0.25 MM
VC_OS_HUB	0.25 MM	0.20 MM
VC_OUTSEN	0.25 MM	0.20 MM
VC_OUTSEN_R	0.25 MM	0.20 MM
VCORE_SENSE_GND	0.25 MM	0.20 MM
VCORE_SENSE_VOUT	0.25 MM	0.20 MM
VC_AUX1	0.25 MM	0.25 MM
VC_AUX2	0.25 MM	0.25 MM
VC_OUT1	0.45 MM	0.25 MM
VC_OUT2	0.45 MM	0.25 MM
VC_ERROUT	0.25 MM	0.20 MM
VC_ERROUT_RC	0.25 MM	0.20 MM
VC_OS_HUB_RC	0.25 MM	0.20 MM
EI_REFCLK_AVDD	0.20 MM	0.08 MM

CPU VCORE VREG

SYNC_MASTER=M33-MS SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. 07

SCALE NONE | SHT 50 OF 154

56 55 50 49 48 42 =PPVCORE_CPU

CRITICAL

C5200 10UF 10% 6.3V X5R 805	C5212 10UF 10% 6.3V X5R 805	C5223 10UF 10% 6.3V X5R 805	C5234 10UF 10% 6.3V X5R 805	C5245 10UF 10% 6.3V X5R 805	C5201 10UF 10% 6.3V X5R 805	C5289 10UF 10% 6.3V X5R 805	C5278 10UF 10% 6.3V X5R 805	C5267 10UF 10% 6.3V X5R 805	C5256 10UF 10% 6.3V X5R 805
C5213 10UF 10% 6.3V X5R 805	C5211 10UF 10% 6.3V X5R 805	C5210 10UF 10% 6.3V X5R 805	C5209 10UF 10% 6.3V X5R 805	C5208 10UF 10% 6.3V X5R 805	C5207 10UF 10% 6.3V X5R 805	C5206 10UF 10% 6.3V X5R 805	C5205 10UF 10% 6.3V X5R 805	C5204 10UF 10% 6.3V X5R 805	C5203 10UF 10% 6.3V X5R 805
C5224 10UF 10% 6.3V X5R 805	C5222 10UF 10% 6.3V X5R 805	C5221 10UF 10% 6.3V X5R 805	C5220 10UF 10% 6.3V X5R 805	C5219 10UF 10% 6.3V X5R 805	C5218 10UF 10% 6.3V X5R 805	C5217 10UF 10% 6.3V X5R 805	C5216 10UF 10% 6.3V X5R 805	C5215 10UF 10% 6.3V X5R 805	C5214 10UF 10% 6.3V X5R 805
C5235 10UF 10% 6.3V X5R 805	C5233 10UF 10% 6.3V X5R 805	C5232 10UF 10% 6.3V X5R 805	C5231 10UF 10% 6.3V X5R 805	C5230 10UF 10% 6.3V X5R 805	C5229 10UF 10% 6.3V X5R 805	C5228 10UF 10% 6.3V X5R 805	C5227 10UF 10% 6.3V X5R 805	C5226 10UF 10% 6.3V X5R 805	C5225 10UF 10% 6.3V X5R 805
C5246 10UF 10% 6.3V X5R 805	C5244 10UF 10% 6.3V X5R 805	C5243 10UF 10% 6.3V X5R 805	C5242 10UF 10% 6.3V X5R 805	C5241 10UF 10% 6.3V X5R 805	C5240 10UF 10% 6.3V X5R 805	C5239 10UF 10% 6.3V X5R 805	C5238 10UF 10% 6.3V X5R 805	C5237 10UF 10% 6.3V X5R 805	C5236 10UF 10% 6.3V X5R 805
C5257 10UF 10% 6.3V X5R 805	C5255 10UF 10% 6.3V X5R 805	C5254 10UF 10% 6.3V X5R 805	C5253 10UF 10% 6.3V X5R 805	C5252 10UF 10% 6.3V X5R 805	C5251 10UF 10% 6.3V X5R 805	C5250 10UF 10% 6.3V X5R 805	C5249 10UF 10% 6.3V X5R 805	C5248 10UF 10% 6.3V X5R 805	C5247 10UF 10% 6.3V X5R 805
C5268 10UF 10% 6.3V X5R 805	C5266 10UF 10% 6.3V X5R 805	C5265 10UF 10% 6.3V X5R 805	C5264 10UF 10% 6.3V X5R 805	C5263 10UF 10% 6.3V X5R 805	C5262 10UF 10% 6.3V X5R 805	C5261 10UF 10% 6.3V X5R 805	C5260 10UF 10% 6.3V X5R 805	C5259 10UF 10% 6.3V X5R 805	C5258 10UF 10% 6.3V X5R 805
C5279 10UF 10% 6.3V X5R 805	C5277 10UF 10% 6.3V X5R 805	C5276 10UF 10% 6.3V X5R 805	C5275 10UF 10% 6.3V X5R 805	C5274 10UF 10% 6.3V X5R 805	C5273 10UF 10% 6.3V X5R 805	C5272 10UF 10% 6.3V X5R 805	C5271 10UF 10% 6.3V X5R 805	C5270 10UF 10% 6.3V X5R 805	C5269 10UF 10% 6.3V X5R 805
C5290 10UF 10% 6.3V X5R 805	C5288 10UF 10% 6.3V X5R 805	C5287 10UF 10% 6.3V X5R 805	C5286 10UF 10% 6.3V X5R 805	C5285 10UF 10% 6.3V X5R 805	C5284 10UF 10% 6.3V X5R 805	C5283 10UF 10% 6.3V X5R 805	C5282 10UF 10% 6.3V X5R 805	C5281 10UF 10% 6.3V X5R 805	C5280 10UF 10% 6.3V X5R 805
C5202 10UF 10% 6.3V X5R 805	C5299 10UF 10% 6.3V X5R 805	C5298 10UF 10% 6.3V X5R 805	C5297 10UF 10% 6.3V X5R 805	C5296 10UF 10% 6.3V X5R 805	C5295 10UF 10% 6.3V X5R 805	C5294 10UF 10% 6.3V X5R 805	C5293 10UF 10% 6.3V X5R 805	C5292 10UF 10% 6.3V X5R 805	C5291 10UF 10% 6.3V X5R 805

CPU VCORE MORE BYPASS

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APPLE COMPUTER INC.

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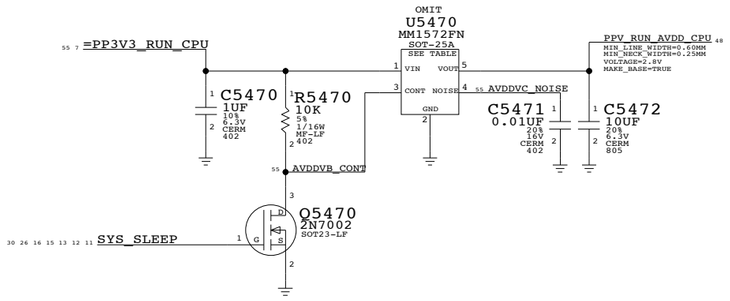
PROCESSOR AVDD VREG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0671	1	IIC,MM1572FN,2.5V,150MA,REG,5P SOT-25A	U5470	AVDD_2V5
353S0807	1	IIC,MM1572,2.8V,150MA,REG,5P SOT-25A	U5470	AVDD_2V8

ZH5400 HOLE-VIA
ZH5401 HOLE-VIA
ZH5402 HOLE-VIA
ZH5403 HOLE-VIA
ZH5404 HOLE-VIA
ZH5405 HOLE-VIA
ZH5406 HOLE-VIA
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CPU AVDD VREG

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APPLE COMPUTER INC.

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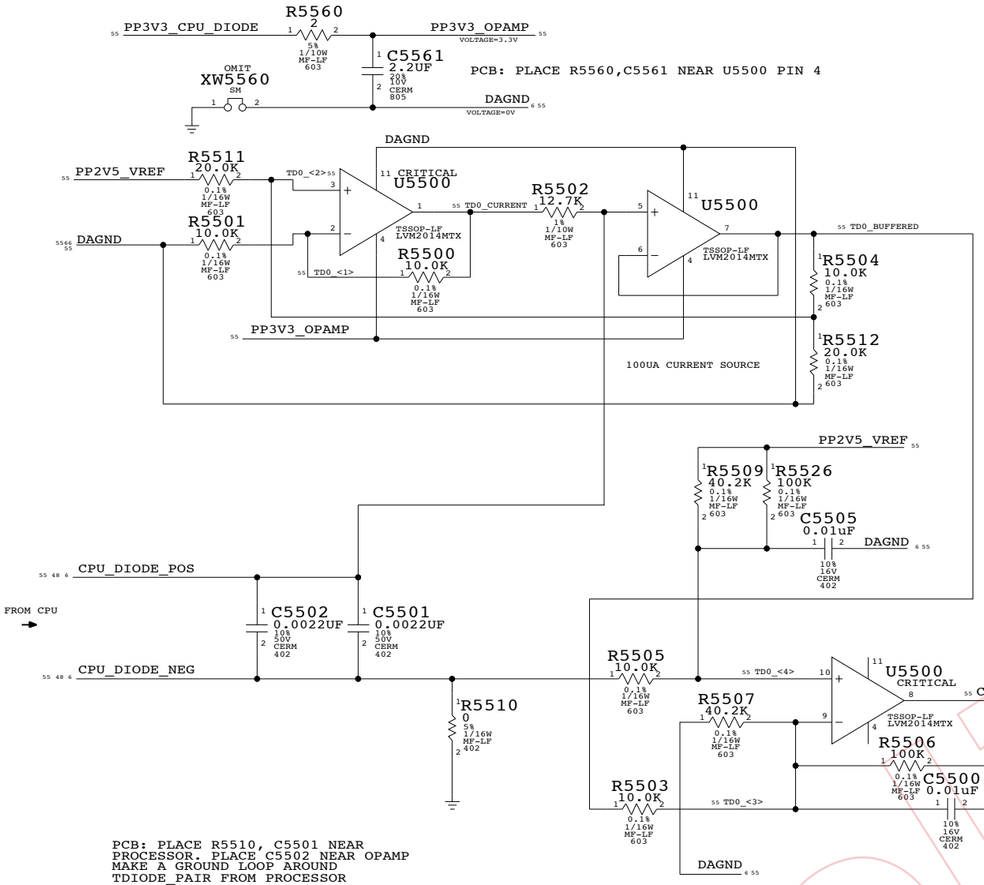
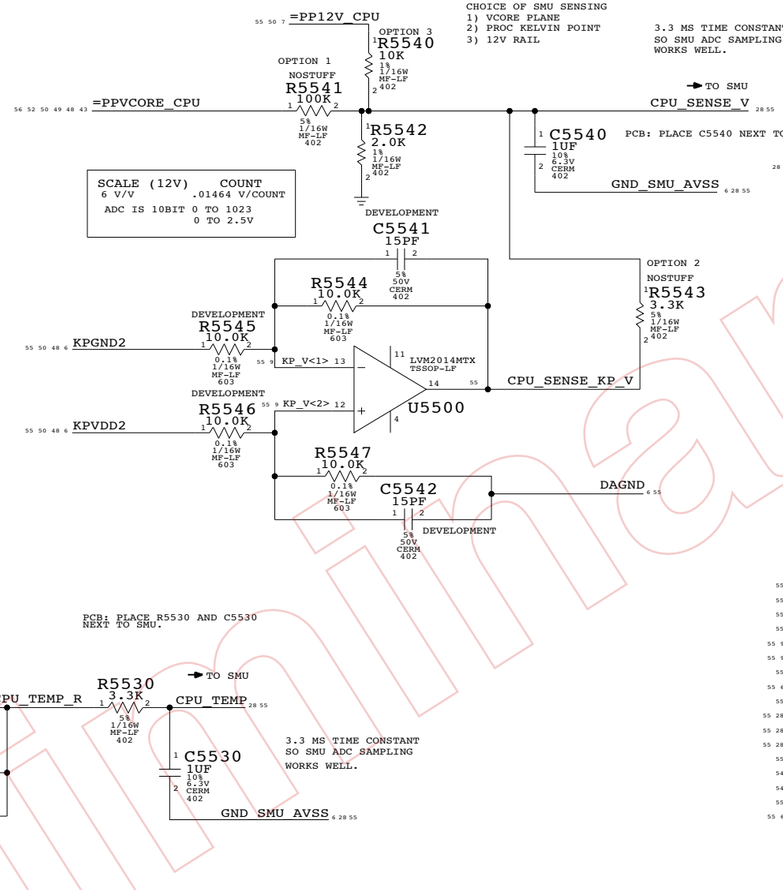
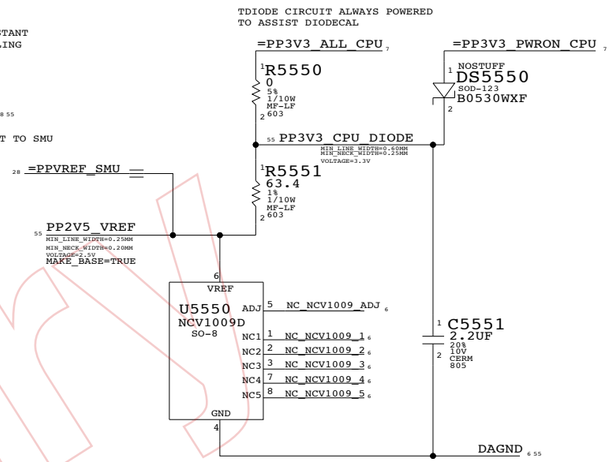
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



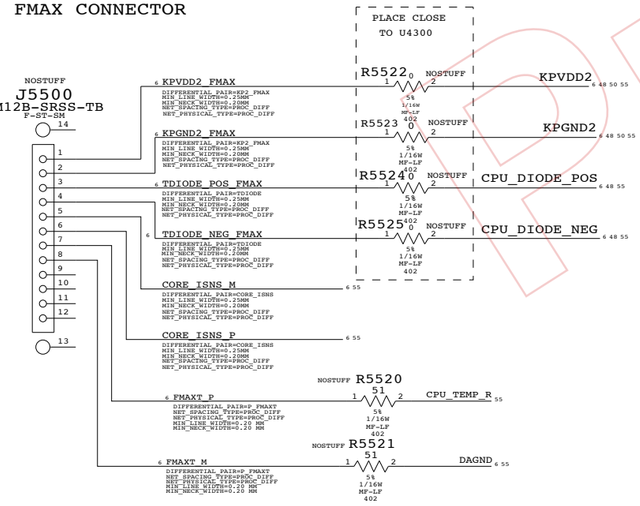
2.5V PRECISION VOLTAGE REFERENCE SOURCE



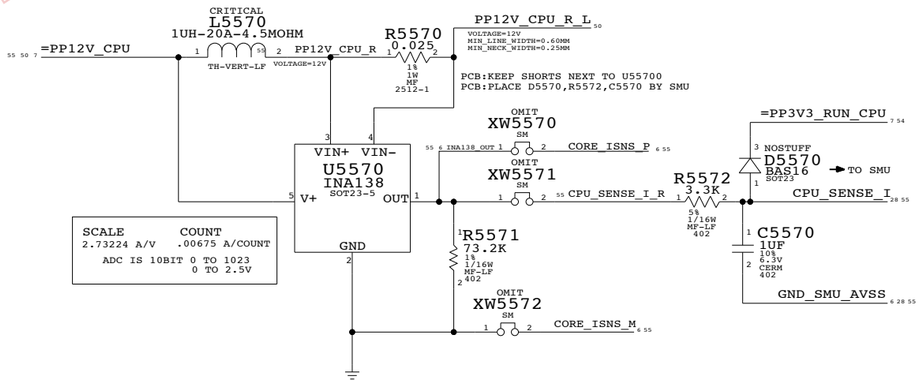
PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
TD0_<1..4>	0.25 MM	0.25 MM	A325
PP12V_CPU_R	0.60 MM	0.25 MM	A376
TD0_CURRENT	0.25 MM	0.25 MM	A323
TD0_BUFFERED	0.25 MM	0.25 MM	A321
KP_V<1..2>	0.25 MM	0.25 MM	A355
CPU_SENSE_KP_V	0.25 MM	0.25 MM	A356
PP3V3_OPAMP	0.60 MM	0.25 MM	A375
INA138_OUT	0.25 MM	0.25 MM	A357
CPU_SENSE_I_R	0.25 MM	0.25 MM	A360
CPU_SENSE_I	0.25 MM	0.25 MM	A359
CPU_SENSE_V	0.25 MM	0.25 MM	A361
CPU_TEMP	0.25 MM	0.20 MM	A362
CPU_TEMP_R	0.25 MM	0.20 MM	A370
AVDDVC_NOISE	0.25 MM	0.20 MM	A380
AVDDVB_CONT	0.25 MM	0.20 MM	A381
PP12V_CPU_R	0.60 MM	0.25 MM	A382
DAGND	0.60 MM	0.25 MM	A385

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



PCB: PLACE R5530 AND C5530 NEXT TO SMU.

T,V,I SENSORS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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CONNECT PULSAR CLKS TO CPU/NB

EI_CPU_SYSCLK_P	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_P	26
EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N	26
EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC	26
EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US	26
EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC	26 42

CONNECT KODIAK EI A TO/FROM CPU

EI_NB_TO_CPU_CLK_P		EI_NB_TO_CPU_A_CLK_P	42
EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N	42
EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43>	42
EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1>	42
EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1>	42
	MAKE_BASE=TRUE		
EI_CPU_TO_NB_CLK_P		EI_CPU_A_TO_NB_CLK_P	42
EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N	42
EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43>	42
EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1>	42
EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1>	42
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK QREQ A0

CPU_TO_NB_QREQ_L		CPU_A0_TO_NB_QREQ_L 42
	MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

CPU_QACK_L		CPU_A0_QACK_L	42
NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L	42
NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L	44
NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L	44
	MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

CPU_INT_L		CPU_A0_INT_R_L	24 56
NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L	42
NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L	44
NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L	44
	MAKE_BASE=TRUE		

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

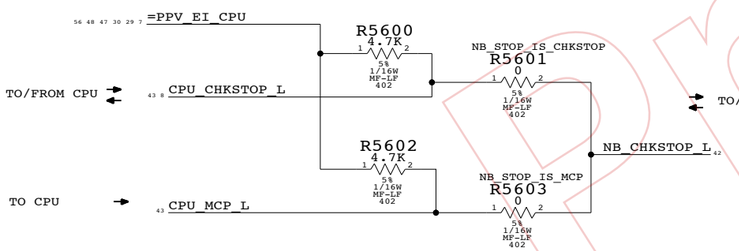
CPU_SRESET_L_R		SB_CPU_A0_SRESET_L	24 56
NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L	24 56
NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L	24 56
NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L	24 56
	MAKE_BASE=TRUE		

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

TP_NB_B_TRIGGER_OUT		NB_B_TRIGGER_OUT	44
TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT	42
TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT	43
TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN	43 47
TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT	43
NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO	43
NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE	43
TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION	43
NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN	43
	MAKE_BASE=TRUE		

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	130
EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		136
EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		137
EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		139
EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	140
EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	141
EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	143
EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	142
EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1198
EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1196

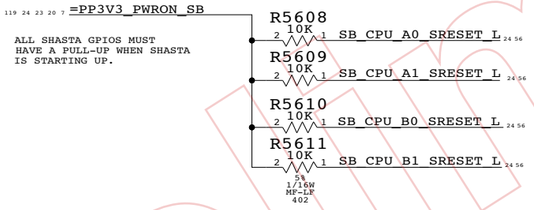
NC KODIAK EI B OUTPUT PORT

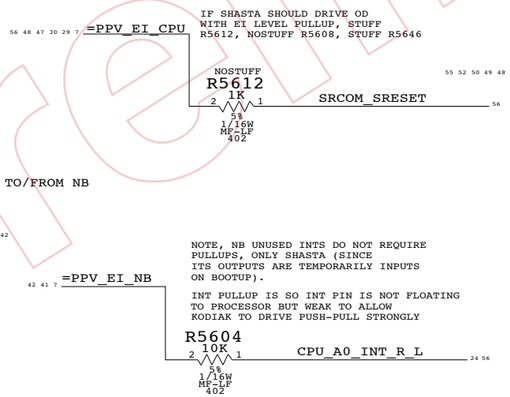
NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P	44
NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N	44
NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43>	44
NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1>	44
NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1>	44
	MAKE_BASE=TRUE		

NC KODIAK EI B INPUT PORT

NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P	44
NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N	44
NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43>	44
NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1>	44
NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1>	44
	MAKE_BASE=TRUE		

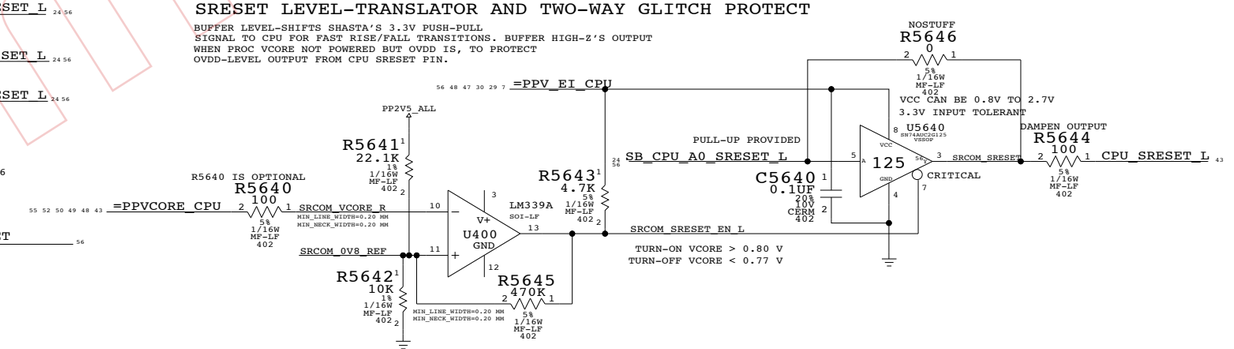
PULLUPS FOR SRESET'S FROM SHASTA





SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.



CPU ALIASES & MISC

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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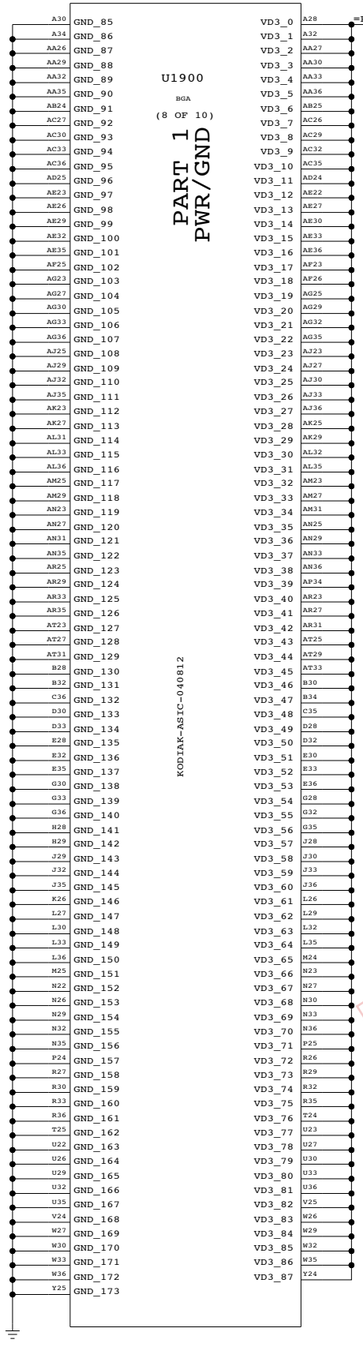

=PP1V8_PWRON_NBMEM 3B2 20D4 20D8 39D3 58D4 59B1

59B1 58D6 39D3 20D8 20D4 3B2 =PP1V8_PWRON_NBMEM

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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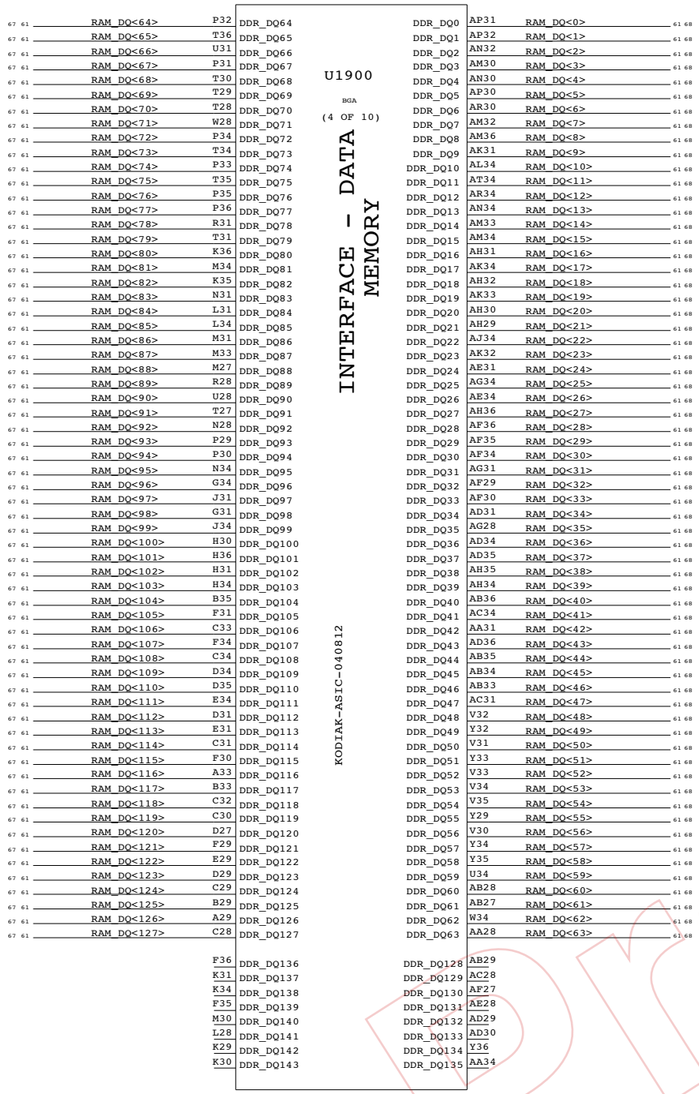
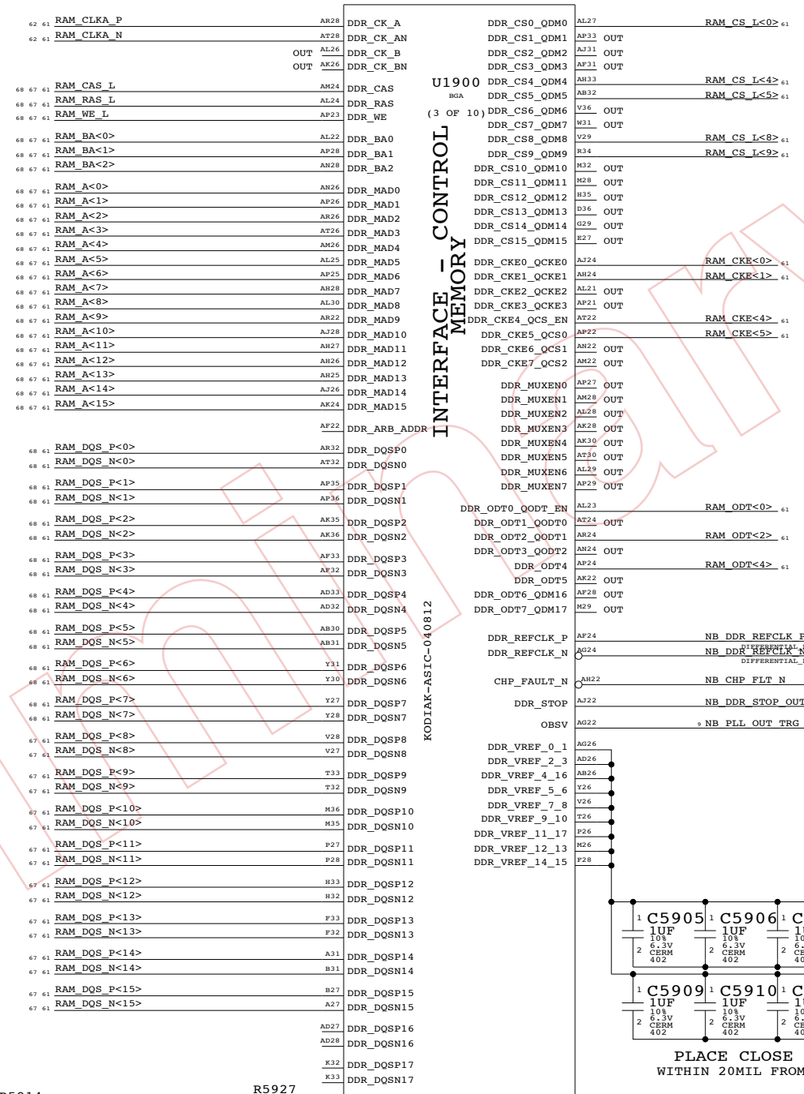
LAST_MODIFIED=Thu May 19 14:27:05 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS



Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	–	*unused*	0:63
B2	8	0	4	J6700 rank 1	64:127
B3	9	1	–	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	–	*unused*	0:63
D6	10	2	5	*unused*	64:127
D7	11	3	–	*unused*	64:127
E8	4	4	2	*unused*	0:63
E9	5	5	–	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	–	*unused*	64:127
G12	6	6	3	*unused*	0:63
G13	7	7	–	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	–	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	–	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	–	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	–	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	–	*unused*	64:127

Kodiak Memory Dq/Ctl

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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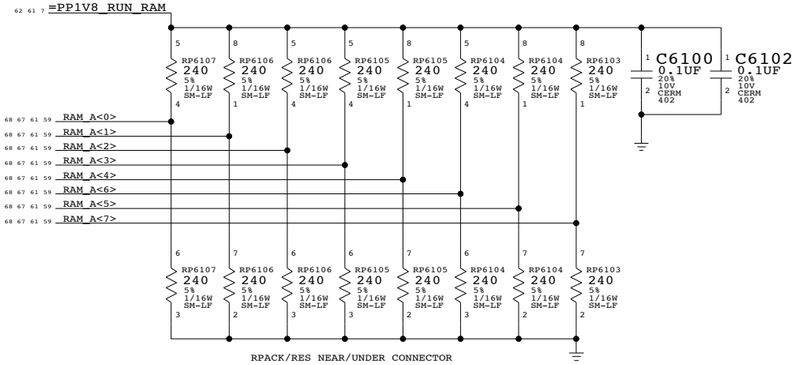
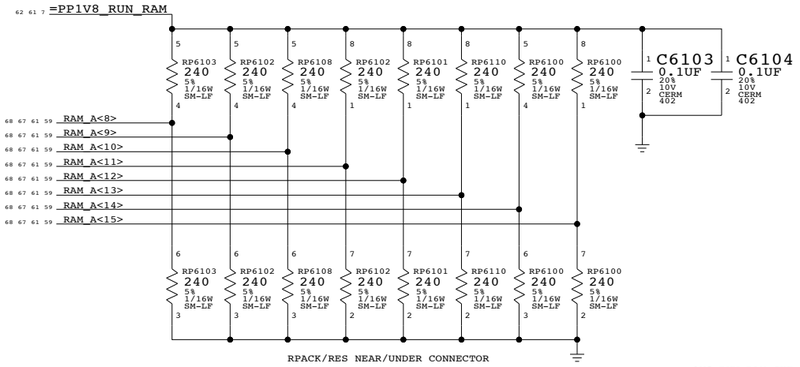
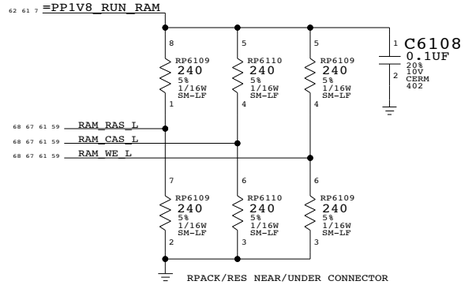
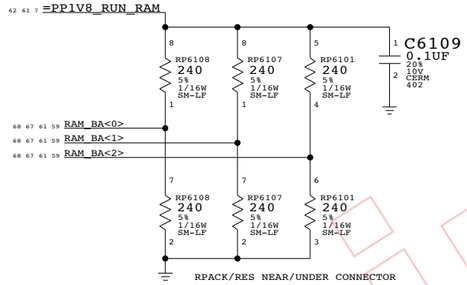
KODIAK MEMORY INTERFACE

ALL R PACKS ARE 1/16W 5%









RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		7243
RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		7487
RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		7242
RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT		7245
RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT		7244
RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		7238
RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		7241
RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT		7575
RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		7234
RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		7236
RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT		7235
RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT		7237
RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		7239
RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT		7592
RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		7232
RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		7574
RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		7576
RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT		7577
RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		7593
RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		7594

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	7206
RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	7207
RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	7230
RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	7231
RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	7232
RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	7233
RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	7234
RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	7235
RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	7216
RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	7217
RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	7218
RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	7219
RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	7220
RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	7221
RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	7222
RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	7223
RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	7224
RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	7225
RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	7226
RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	7227
RAM_DQ<7..0>	RAM_DQS0_EC	RAM_CAD	RAM_CAD		7248
RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	7246
RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	7470
RAM_DQ<15..8>	RAM_DQS1_EC	RAM_CAD	RAM_CAD		7252
RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	7251
RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	7471
RAM_DQ<23..16>	RAM_DQS2_EC	RAM_CAD	RAM_CAD		7254
RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	7253
RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	7472
RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD		7256
RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	7255
RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	7473
RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD		7258
RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	7257
RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	7474
RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD		7260
RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	7259
RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	7475
RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD		7262
RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	7261
RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	7476
RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD		7264
RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	7263
RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	7477
RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD		7267
RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	7265
RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	7478
RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD		7268
RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	7266
RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	7479
RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD		7269
RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	7270
RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	7480
RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD		7271
RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	7272
RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	7481
RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD		7273
RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	7274
RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	7482
RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD		7277
RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	7276
RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	7483
RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD		7278
RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	7279
RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	7484
RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD		7280
RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	7281
RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	7485
RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		7244
RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS		7355
RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS		7486
RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7572
RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7208
RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7256
RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		7573
RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7257
RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7258
RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		7259
RAM_A_R<15..0>		RAM_CAD	RAM_CAD		7380
RAM_BA_R<2..0>		RAM_CAD	RAM_CAD		7381
RAM_RAS_L_R		RAM_CAD	RAM_CAD		7383
RAM_CAS_L_R		RAM_CAD	RAM_CAD		7382
RAM_WE_L_R		RAM_CAD	RAM_CAD		7384

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

Parallel Term

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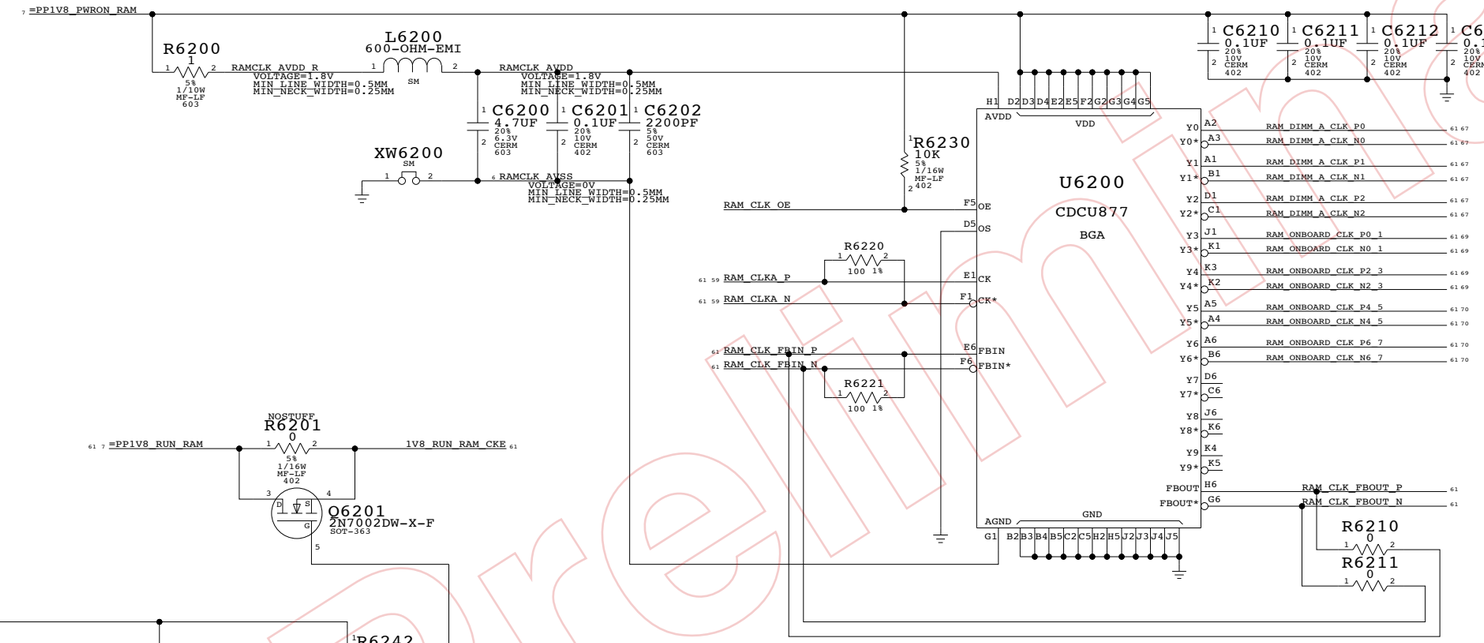

Main Memory Clock Buffer

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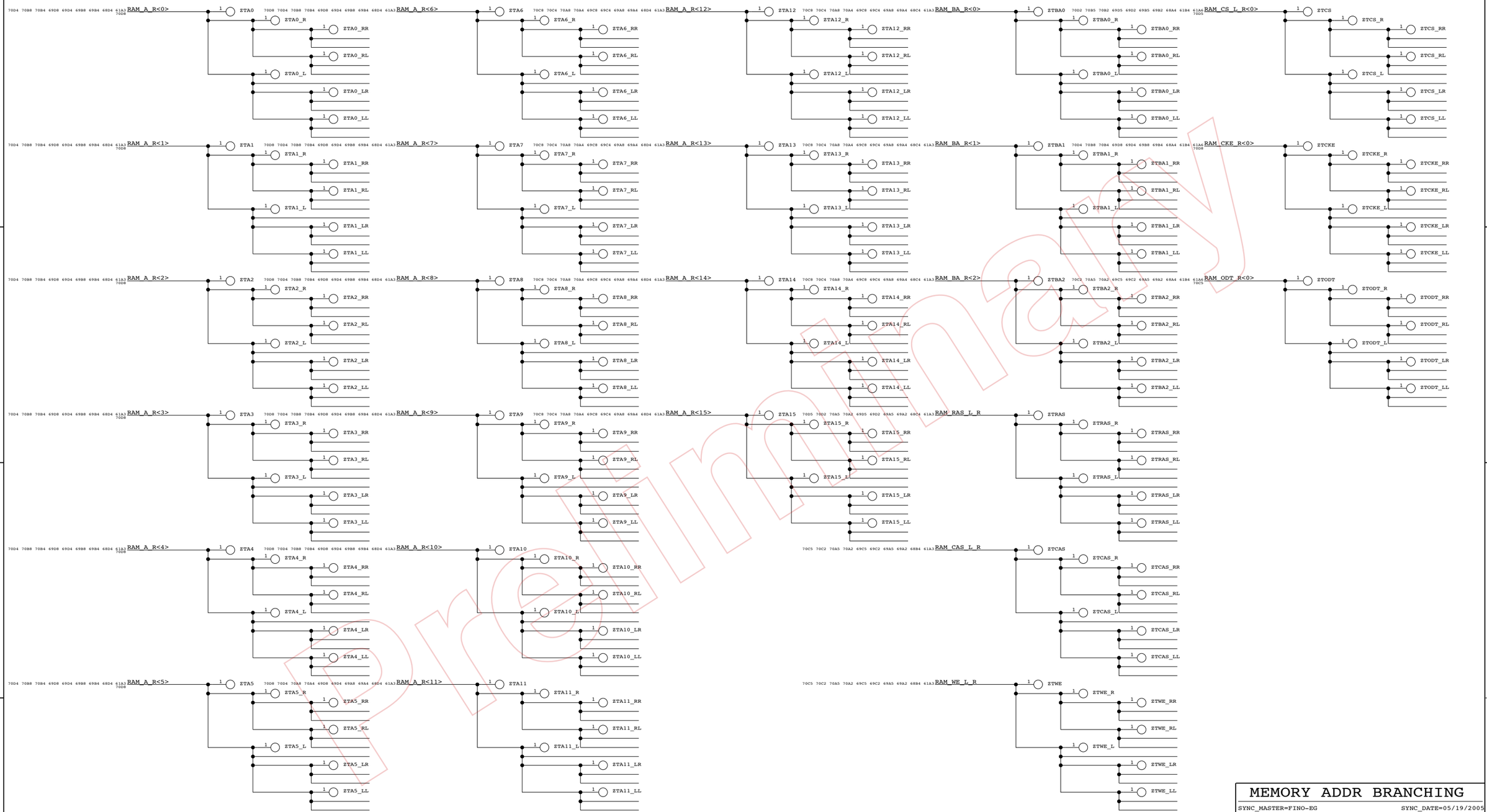

MEMORY ADDR BRANCHING

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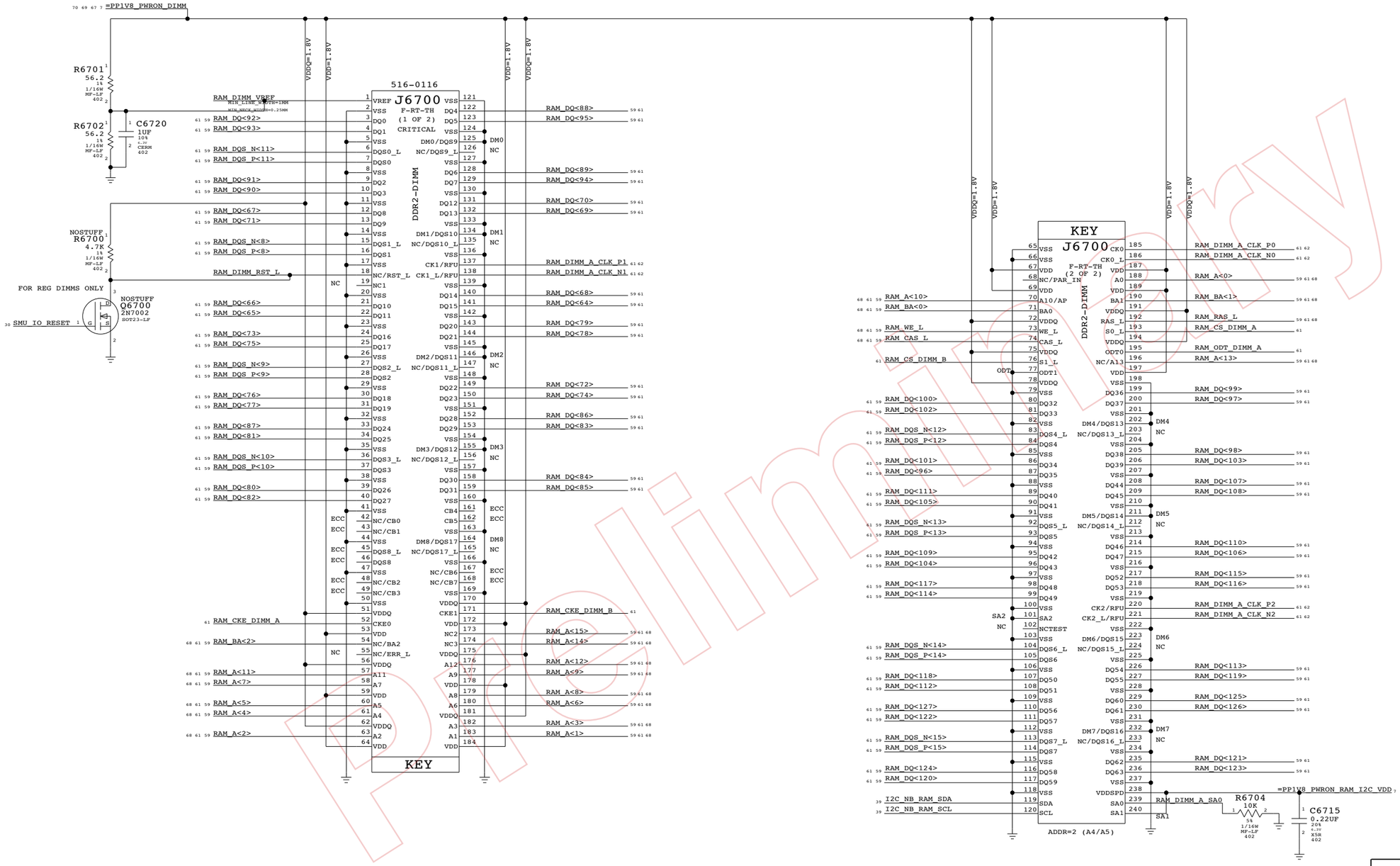
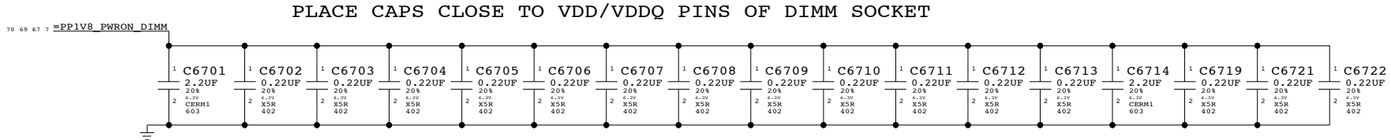


PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



Memory Dimm A

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APPLE COMPUTER INC.

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ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

RAM_DQ<0>	22	4	5	RP6800	RAM_DQ_R<0>	61 69	
RAM_DQ<1>	22	3	6	RP6800	RAM_DQ_R<1>	6 61 69	
RAM_DQ<2>	22	1	8	RP6801	RAM_DQ_R<2>	6 61 69	
RAM_DQ<3>	22	3	6	RP6801	RAM_DQ_R<3>	6 61 69	
RAM_DQ<4>	22	4	5	RP6801	RAM_DQ_R<4>	61 69	
RAM_DQ<5>	22	2	7	RP6800	RAM_DQ_R<5>	6 61 69	
RAM_DQ<6>	22	2	7	RP6801	RAM_DQ_R<6>	6 61 69	
RAM_DQ<7>	22	1	8	RP6800	RAM_DQ_R<7>	6 61 69	
RAM_DQ<8>	22	3	6	RP6802	RAM_DQ_R<8>	6 61 69	
RAM_DQ<9>	22	4	5	RP6803	RAM_DQ_R<9>	61 69	
RAM_DQ<10>	22	1	8	RP6803	RAM_DQ_R<10>	6 61 69	
RAM_DQ<11>	22	4	5	RP6802	RAM_DQ_R<11>	6 61 69	
RAM_DQ<12>	22	3	6	RP6803	RAM_DQ_R<12>	6 61 69	
RAM_DQ<13>	22	2	7	RP6802	RAM_DQ_R<13>	6 61 69	
RAM_DQ<14>	22	2	7	RP6803	RAM_DQ_R<14>	6 61 69	
RAM_DQ<15>	22	1	8	RP6802	RAM_DQ_R<15>	61 69	
RAM_DQ<16>	22	3	6	RP6805	RAM_DQ_R<16>	6 61 69	
RAM_DQ<17>	22	4	5	RP6805	RAM_DQ_R<17>	6 61 69	
RAM_DQ<18>	22	1	8	RP6804	RAM_DQ_R<18>	61 69	
RAM_DQ<19>	22	2	7	RP6805	RAM_DQ_R<19>	6 61 69	
RAM_DQ<20>	22	2	7	RP6804	RAM_DQ_R<20>	6 61 69	
RAM_DQ<21>	22	4	5	RP6804	RAM_DQ_R<21>	6 61 69	
RAM_DQ<22>	22	3	6	RP6804	RAM_DQ_R<22>	6 61 69	
RAM_DQ<23>	22	1	8	RP6805	RAM_DQ_R<23>	61 69	
RAM_DQ<24>	22	4	5	RP6807	RAM_DQ_R<24>	6 61 69	
RAM_DQ<25>	22	2	7	RP6806	RAM_DQ_R<25>	6 61 69	
RAM_DQ<26>	22	4	5	RP6806	RAM_DQ_R<26>	6 61 69	
RAM_DQ<27>	22	1	8	RP6807	RAM_DQ_R<27>	61 69	
RAM_DQ<28>	22	3	6	RP6807	RAM_DQ_R<28>	6 61 69	
RAM_DQ<29>	22	3	6	RP6806	RAM_DQ_R<29>	6 61 69	
RAM_DQ<30>	22	2	7	RP6807	RAM_DQ_R<30>	6 61 69	
RAM_DQ<31>	22	1	8	RP6806	RAM_DQ_R<31>	61 69	
RAM_DQ<32>	22	4	5	RP6809	RAM_DQ_R<32>	6 61 70	
RAM_DQ<33>	22	2	7	RP6808	RAM_DQ_R<33>	6 61 70	
RAM_DQ<34>	22	3	6	RP6808	RAM_DQ_R<34>	6 61 70	
RAM_DQ<35>	22	1	8	RP6809	RAM_DQ_R<35>	61 70	
RAM_DQ<36>	22	2	7	RP6809	RAM_DQ_R<36>	6 61 70	
RAM_DQ<37>	22	1	8	RP6808	RAM_DQ_R<37>	61 70	
RAM_DQ<38>	22	3	6	RP6809	RAM_DQ_R<38>	6 61 70	
RAM_DQ<39>	22	4	5	RP6808	RAM_DQ_R<39>	6 61 70	
RAM_DQ<40>	22	4	5	RP6810	RAM_DQ_R<40>	6 61 70	
RAM_DQ<41>	22	3	6	RP6811	RAM_DQ_R<41>	6 61 70	
RAM_DQ<42>	22	1	8	RP6811	RAM_DQ_R<42>	61 70	
RAM_DQ<43>	22	2	7	RP6810	RAM_DQ_R<43>	6 61 70	
RAM_DQ<44>	22	4	5	RP6811	RAM_DQ_R<44>	6 61 70	
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RAM_DQ<48>	22	3	6	RP6812	RAM_DQ_R<48>	6 61 70	
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RAM_DQ<51>	22	1	8	RP6813	RAM_DQ_R<51>	61 70	
RAM_DQ<52>	22	3	6	RP6813	RAM_DQ_R<52>	6 61 70	
RAM_DQ<53>	22	4	5	RP6813	RAM_DQ_R<53>	6 61 70	
RAM_DQ<54>	22	2	7	RP6812	RAM_DQ_R<54>	6 61 70	
RAM_DQ<55>	22	1	8	RP6812	RAM_DQ_R<55>	61 70	
RAM_DQ<56>	22	3	6	RP6814	RAM_DQ_R<56>	6 61 70	
RAM_DQ<57>	22	4	5	RP6815	RAM_DQ_R<57>	6 61 70	
RAM_DQ<58>	22	2	7	RP6815	RAM_DQ_R<58>	6 61 70	
RAM_DQ<59>	22	3	6	RP6815	RAM_DQ_R<59>	6 61 70	
RAM_DQ<60>	22	2	7	RP6814	RAM_DQ_R<60>	6 61 70	
RAM_DQ<61>	22	1	8	RP6814	RAM_DQ_R<61>	61 70	
RAM_DQ<62>	22	1	8	RP6815	RAM_DQ_R<62>	61 70	
RAM_DQ<63>	22	4	5	RP6814	RAM_DQ_R<63>	6 61 70	

RAM_DQS_P<0>	22	1	2	R6800	RAM_DQS_P_R<0>
RAM_DQS_N<0>	22	1	2	R6810	RAM_DQS_N_R<0>
RAM_DQS_P<1>	22	1	2	R6801	RAM_DQS_P_R<1>
RAM_DQS_N<1>	22	1	2	R6811	RAM_DQS_N_R<1>
RAM_DQS_P<2>	22	1	2	R6802	RAM_DQS_P_R<2>
RAM_DQS_N<2>	22	1	2	R6812	RAM_DQS_N_R<2>
RAM_DQS_P<3>	22	1	2	R6803	RAM_DQS_P_R<3>
RAM_DQS_N<3>	22	1	2	R6813	RAM_DQS_N_R<3>
RAM_DQS_P<4>	22	1	2	R6804	RAM_DQS_P_R<4>
RAM_DQS_N<4>	22	1	2	R6814	RAM_DQS_N_R<4>
RAM_DQS_P<5>	22	1	2	R6805	RAM_DQS_P_R<5>
RAM_DQS_N<5>	22	1	2	R6815	RAM_DQS_N_R<5>
RAM_DQS_P<6>	22	1	2	R6806	RAM_DQS_P_R<6>
RAM_DQS_N<6>	22	1	2	R6816	RAM_DQS_N_R<6>
RAM_DQS_P<7>	22	1	2	R6807	RAM_DQS_P_R<7>
RAM_DQS_N<7>	22	1	2	R6817	RAM_DQS_N_R<7>

RAM_A<0>	5.1	1	8	RP6824	RAM_A_R<0>	1	ZT6800
RAM_A<1>	5.1	1	8	RP6823	RAM_A_R<1>	1	ZT6801
RAM_A<2>	5.1	2	7	RP6823	RAM_A_R<2>	1	ZT6802
RAM_A<3>	5.1	4	5	RP6822	RAM_A_R<3>	1	ZT6803
RAM_A<4>	5.1	3	6	RP6822	RAM_A_R<4>	1	ZT6804
RAM_A<5>	5.1	2	7	RP6822	RAM_A_R<5>	1	ZT6805
RAM_A<6>	5.1	1	8	RP6822	RAM_A_R<6>	1	ZT6806
RAM_A<7>	5.1	3	6	RP6821	RAM_A_R<7>	1	ZT6807
RAM_A<8>	5.1	4	5	RP6821	RAM_A_R<8>	1	ZT6808
RAM_A<9>	5.1	1	8	RP6821	RAM_A_R<9>	1	ZT6809
RAM_A<10>	5.1	3	6	RP6824	RAM_A_R<10>	1	ZT6810
RAM_A<11>	5.1	2	7	RP6821	RAM_A_R<11>	1	ZT6811
RAM_A<12>	5.1	4	5	RP6820	RAM_A_R<12>	1	ZT6812
RAM_A<13>	5.1	4	5	RP6825	RAM_A_R<13>	1	ZT6813
RAM_A<14>	5.1	2	7	RP6820	RAM_A_R<14>	1	ZT6814
RAM_A<15>	5.1	1	8	RP6820	RAM_A_R<15>	1	ZT6815

VIAS FOR ECC STUB

RAM_BA<0>	5.1	4	5	RP6824	RAM_BA_R<0>	ZT6820
RAM_BA<1>	5.1	2	7	RP6824	RAM_BA_R<1>	ZT6821
RAM_BA<2>	5.1	3	6	RP6820	RAM_BA_R<2>	ZT6822
RAM_RAS_L	5.1	1	8	RP6825	RAM_RAS_L_R	ZT6825
RAM_CAS_L	5.1	3	6	RP6825	RAM_CAS_L_R	ZT6826
RAM_WE_L	5.1	2	7	RP6825	RAM_WE_L_R	ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870 24PF 5% 50V C0G 402	RAM_CS_L_R<0>	C6871 2PF +/-0.25PF 50V C0G 402-1
C6880 24PF 5% 50V C0G 402	RAM_CKE_R<0>	C6881 2PF +/-0.25PF 50V C0G 402-1
C6890 24PF 5% 50V C0G 402	RAM_ODT_R<0>	C6891 2PF +/-0.25PF 50V C0G 402-1

MLB Mem Series Term

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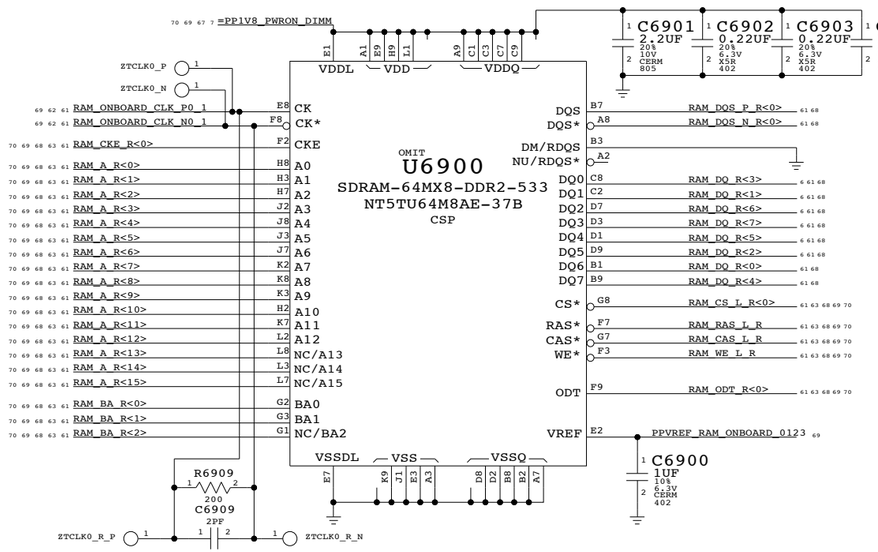

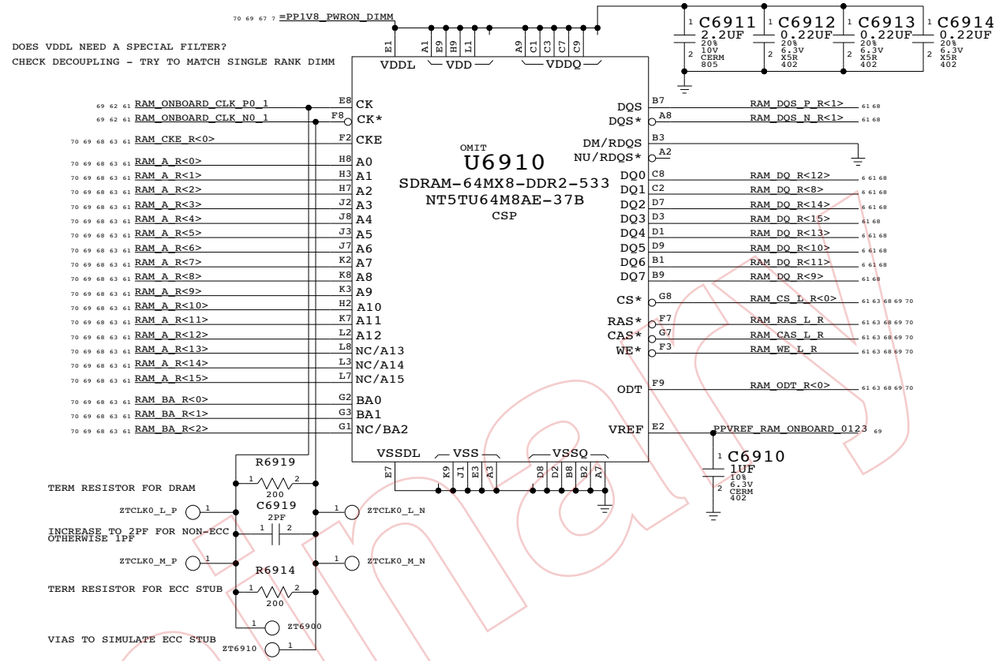

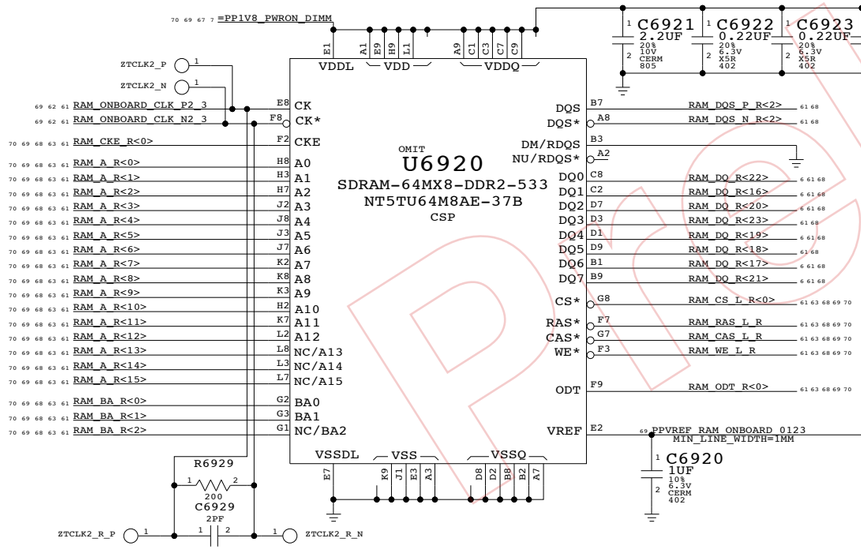

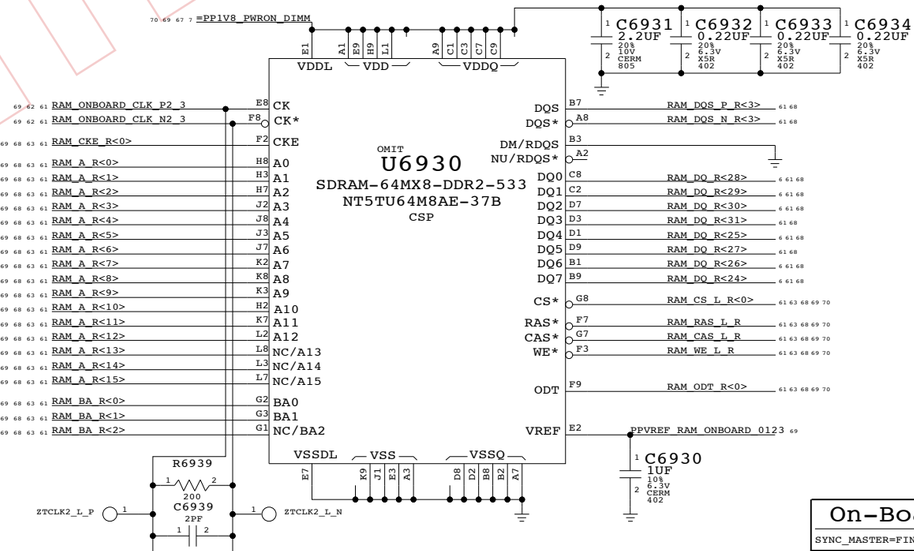

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	

On-Board DDR SDRAM

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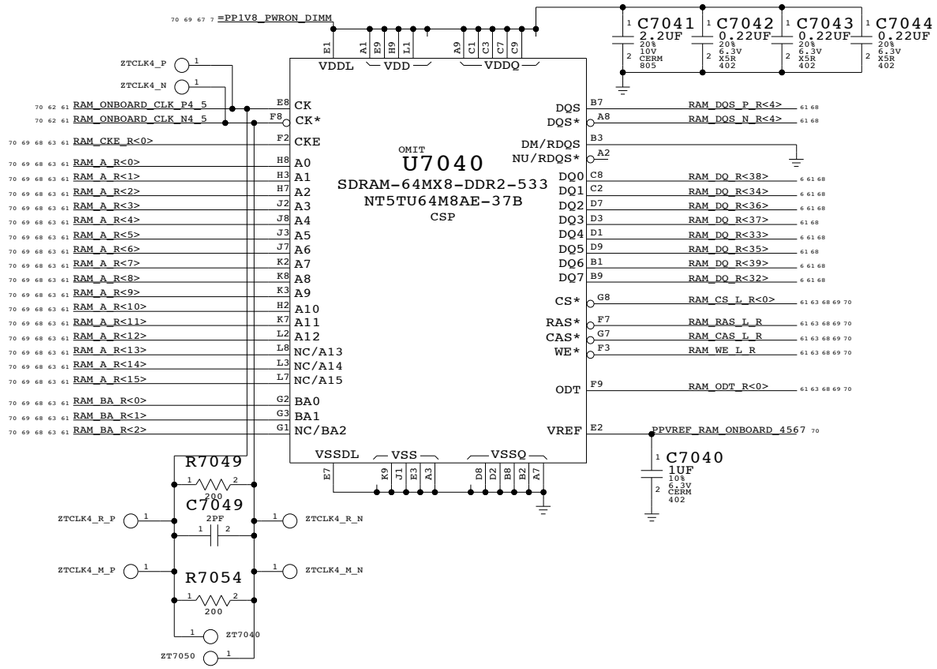

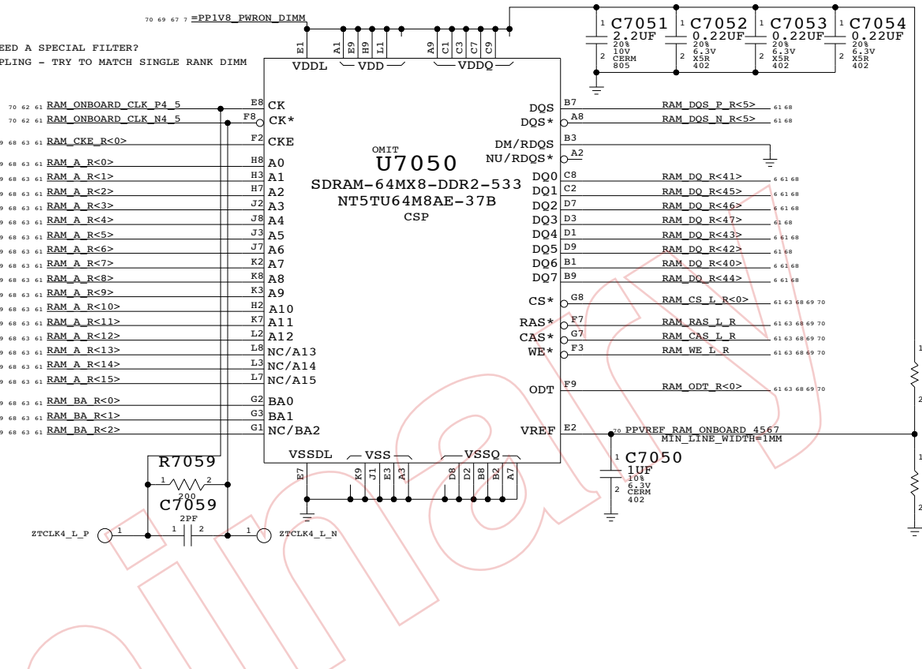

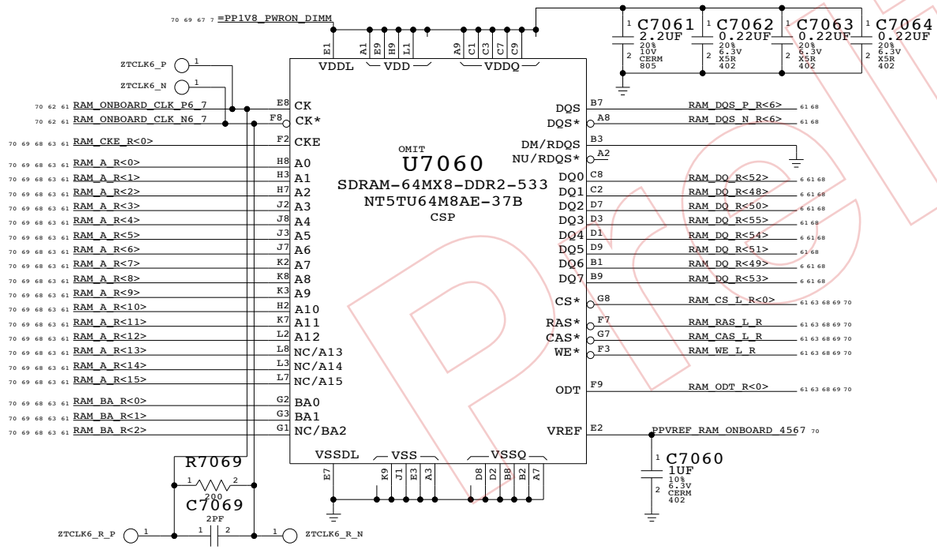

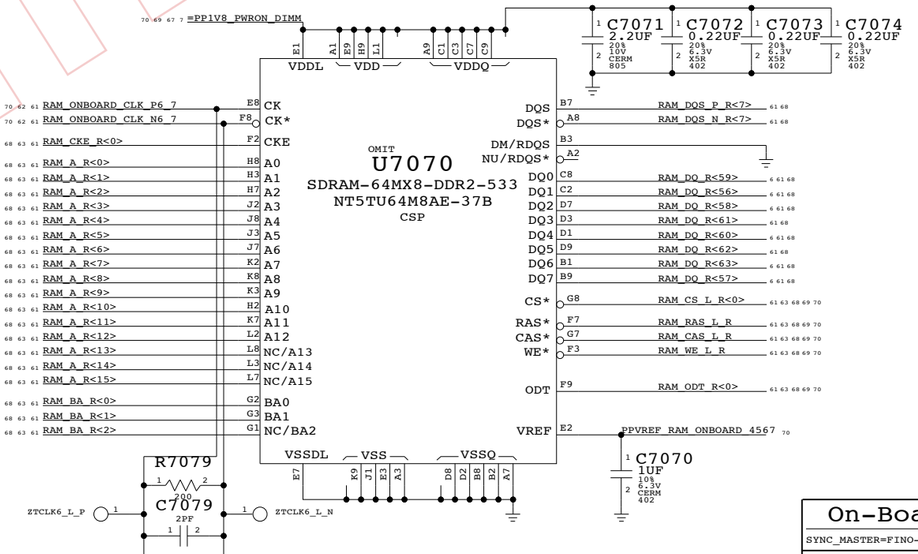

On-Board DDR SDRAM

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE	SHT	OF
NONE	70	154

KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

L8200 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE → PWR_PCIE_A_AVDD_2
- C8200 0.01UF 10% 16V CERM 402
- C8201 10UF 10% 6.3V X5R 805
- C8202 1UF 10% 6.3V CERM 402

L8201 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE → PWR_PCIE_A_AVDD_1
- C8203 0.01UF 10% 16V CERM 402
- C8204 10UF 10% 6.3V X5R 805
- C8205 1UF 10% 6.3V CERM 402

L8202 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE → PWR_PCIE_A_AVDD_0
- C8206 0.01UF 10% 16V CERM 402
- C8207 10UF 10% 6.3V X5R 805
- C8208 1UF 10% 6.3V CERM 402

KOD_G10_GND, KOD_K07_GND, KOD_H05_GND (THIS PAGE)

PWR_PCIE_A_AVDD_2 / PWR_PCIE_A_AVDD_1 / PWR_PCIE_A_AVDD_0

PWR_PCIE_A_AVDD_A / PWR_PCIE_A_AVDD_B / PWR_PCIE_A_AVDD_C → PWR_PCIE_A_AVDD

L8203 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE
- C8222 1UF 10% 6.3V CERM 402
- C8225 1UF 10% 6.3V CERM 402
- C8223 10UF 10% 6.3V X5R 805
- C8224 0.01UF 10% 16V CERM 402

KOD_L13_GND, KOD_J13_GND (THIS PAGE)

L8205 0.22UH 0805-1 — =PP2V5_PWRON_NB_PCIE
- C8228 1UF 10% 6.3V CERM 402
- C8229 10UF 10% 6.3V X5R 805
- C8230 0.01UF 10% 16V CERM 402

KOD_H08_GND (THIS PAGE)

U1900
KODIAK-ASIC-040812

PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE

PCIE_AVDD_0 (1.65V-2.75V) SERDES	PCIE_AVDD_1 (1.65V-2.75V) SERDES	PCIE_AVDD_2 (1.65V-2.75V) SERDES	PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL	PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL	PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL
J06	J07	H11	J12	K13	J09

(1.6V-1.2V)

PCIE_VDD	A04	PCIE_VDD	F02
PCIE_VDD	A08	PCIE_VDD	F05
PCIE_VDD	A12	PCIE_VDD	G08
PCIE_VDD	B06	PCIE_VDD	G12
PCIE_VDD	B10	PCIE_VDD	H01
PCIE_VDD	C03	PCIE_VDD	H04
PCIE_VDD	D01	PCIE_VDD	H07
PCIE_VDD	D04	PCIE_VDD	H10
PCIE_VDD	D08	PCIE_VDD	H14
PCIE_VDD	D12	PCIE_VDD	K12
PCIE_VDD	E06	PCIE_VDD	L11
PCIE_VDD	E10	PCIE_VDD	L14
PCIE_VDD	E14	PCIE_VDD	M12

82B2 82A8 3A4 =PPVCORE_PWRON_NB_PCIE — 3A4 82A8 82B2 82C6 82C8

PCIE_REFCLK_P / PCIE_REFCLK_N (100MHZ)

PCIE_HSIN0	G05	PCIE_HSOP0	B03
PCIE_HSIP0	G04	PCIE_HSON0	D03
PCIE_HSIN1	G01	PCIE_HSOP1	J02
PCIE_HSIP1	G02	PCIE_HSON1	J01
PCIE_HSIN2	C04	PCIE_HSOP2	C02
PCIE_HSIP2	C05	PCIE_HSON2	C01
PCIE_HSIN3	C07	PCIE_HSOP3	B07
PCIE_HSIP3	C06	PCIE_HSON3	A07
PCIE_HSIN4	E01	PCIE_HSOP4	B03
PCIE_HSIP4	E02	PCIE_HSON4	D03
PCIE_HSIN5	J05	PCIE_HSOP5	B01
PCIE_HSIP5	J04	PCIE_HSON5	H03
PCIE_HSIN6	H06	PCIE_HSOP6	B03
PCIE_HSIP6	G06	PCIE_HSON6	A03
PCIE_HSIN7	E05	PCIE_HSOP7	B05
PCIE_HSIP7	D05	PCIE_HSON7	A05
PCIE_HSIN8	D11	PCIE_HSOP8	C11
PCIE_HSIP8	E11	PCIE_HSON8	C10
PCIE_HSIN9	F12	PCIE_HSOP9	B11
PCIE_HSIP9	F13	PCIE_HSON9	A11
PCIE_HSIN10	H09	PCIE_HSOP10	F11
PCIE_HSIP10	G09	PCIE_HSON10	F10
PCIE_HSIN11	F09	PCIE_HSOP11	B09
PCIE_HSIP11	F08	PCIE_HSON11	A09
PCIE_HSIN12	G13	PCIE_HSOP12	D13
PCIE_HSIP12	H13	PCIE_HSON12	E13
PCIE_HSIN13	C13	PCIE_HSOP13	B13
PCIE_HSIP13	C12	PCIE_HSON13	A13
PCIE_HSIN14	D07	PCIE_HSOP14	D09
PCIE_HSIP14	E07	PCIE_HSON14	E09
PCIE_HSIN15	G07	PCIE_HSOP15	C08
PCIE_HSIP15	F07	PCIE_HSON15	C09

PCIE_PRESENTN — AJ02 — 113C7 84C7 PCIE_SLOTA_PRSNT_L

PCIE_UCAL_RES0 — F14 — 6A5 PCIE_VCAL_RES0

PCIE_UCAL_RES1 — J14 — PCIE_VCAL_RES1

(DNU)
PCIE_AVREG_2 — G11 — NC_A_AVREG_2
PCIE_AVREG_1 — J08 — NC_A_AVREG_1
PCIE_AVREG_0 — E04 — NC_A_AVREG_0

PCIE_GND	A06	PCIE_GND	F04
PCIE_GND	A10	PCIE_GND	F06
PCIE_GND	B02	PCIE_GND	G14
PCIE_GND	B04	PCIE_GND	H02
PCIE_GND	B08	PCIE_GND	H12
PCIE_GND	B12	PCIE_GND	K10
PCIE_GND	D02	PCIE_GND	K14
PCIE_GND	D06	PCIE_GND	L12
PCIE_GND	D10	PCIE_GND	M11
PCIE_GND	D14	PCIE_GND	M13
PCIE_GND	E08		
PCIE_GND	E12		
PCIE_GND	F01		

AVDD_0_GND (H05) AVDD_1_GND (K07) AVDD_2_GND (G10) REFCLK_AGNDA (J13) REFCLK_AGNDB (L13) REFCLK_AGND2 (H08)

97D4 82C7 6A3 KOD_H05_GND
97D4 82D7 6A3 KOD_K07_GND
97D4 82D7 6A3 KOD_G10_GND
(THIS PAGE, X3)

KOD_H08_GND 6A3 82C2 97D4
KOD_L13_GND 6A3 82D2 97D4
KOD_J13_GND 6A3 82D2 97D4
(THIS PAGE, X3)

XW8200 XW8201 XW8202 XW8203 XW8204 XW8205 (SM)

KODIAK PCI-E REFCLK 100MHZ REFCLK

PP8201 P4MM (SM) 100+ / 100-
97D8 CLK_KOD_100M_PF<0>
97D8 CLK_KOD_100M_NF<0>

PP8200 P4MM (SM) 82B2 82B8 3A4 82C6 =PPVCORE_PWRON_NB_PCIE

26C2 97D8 CLK_KOD_100M_P<0> — R8202 20.5 1% 1/16W MF-LF 402 — 97D8 100M_P<0>
- NOSTUFF R8206 8.2K 5% 1/16W MF-LF 402
- C8245 0.01UF 10% 16V CERM 402

26B2 97D8 CLK_KOD_100M_N<0> — R8205 20.5 1% 1/16W MF-LF 402 — 100M_N<0>
- NOSTUFF R8207 8.2K 5% 1/16W MF-LF 402
- C8246 0.01UF 10% 16V CERM 402

100M_G
- C8244 0.01UF 10% 16V CERM 402
- R8204 29.4 1% 1/16W MF-LF 402

KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

82D8 82D1 82C8 3C1 =PP2V5_PWRON_NB_PCIE
- R8200 8.2K 5% 1/16W MF-LF 402
- R8201 200 1% 1/16W MF-LF 402

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

=PPVCORE_PWRON_NB_PCIE 3A4 82B2 82C2 82C6 82C8

C8209 C8210 C8211 C8212
C8213 C8214 C8215 C8216
C8217 C8218 C8219 C8220 C8221
(1UF 10% 6.3V CERM 402)

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

PCIE_HSON0	D03 97D8	PCIE_NB_TO_SLOTA_NF<0>	0.1UF	C8247	PCIE_NB_TO_SLOTA_N<0>	84C6	97B8
PCIE_HSOP0	B03 97D8	PCIE_NB_TO_SLOTA_PF<0>	0.1UF	C8248	PCIE_NB_TO_SLOTA_P<0>	84C6	97B8
PCIE_HSON1	J01 97D8	PCIE_NB_TO_SLOTA_NF<1>	0.1UF	C8249	PCIE_NB_TO_SLOTA_N<1>	84C6	97B8
PCIE_HSOP1	J02 97D8	PCIE_NB_TO_SLOTA_PF<1>	0.1UF	C8250	PCIE_NB_TO_SLOTA_P<1>	84C6	97B8
PCIE_HSON2	C01 97C8	PCIE_NB_TO_SLOTA_NF<2>	0.1UF	C8251	PCIE_NB_TO_SLOTA_N<2>	84C6	97B8
PCIE_HSOP2	C02 97C8	PCIE_NB_TO_SLOTA_PF<2>	0.1UF	C8252	PCIE_NB_TO_SLOTA_P<2>	84C6	97B8
PCIE_HSON3	A07 97C8	PCIE_NB_TO_SLOTA_NF<3>	0.1UF	C8253	PCIE_NB_TO_SLOTA_N<3>	84C6	97B8
PCIE_HSOP3	B07 97C8	PCIE_NB_TO_SLOTA_PF<3>	0.1UF	C8254	PCIE_NB_TO_SLOTA_P<3>	84C6	97B8
PCIE_HSON4	B03 97C8	PCIE_NB_TO_SLOTA_NF<4>	0.1UF	C8255	PCIE_NB_TO_SLOTA_N<4>	84B6	97B8
PCIE_HSOP4	G03 97C8	PCIE_NB_TO_SLOTA_PF<4>	0.1UF	C8256	PCIE_NB_TO_SLOTA_P<4>	84C6	97B8
PCIE_HSON5	H03 97C8	PCIE_NB_TO_SLOTA_NF<5>	0.1UF	C8257	PCIE_NB_TO_SLOTA_N<5>	84B6	97B8
PCIE_HSOP5	J03 97C8	PCIE_NB_TO_SLOTA_PF<5>	0.1UF	C8258	PCIE_NB_TO_SLOTA_P<5>	84B6	97B8
PCIE_HSON6	A03 97C8	PCIE_NB_TO_SLOTA_NF<6>	0.1UF	C8259	PCIE_NB_TO_SLOTA_N<6>	84B6	97B8
PCIE_HSOP6	B03 97C8	PCIE_NB_TO_SLOTA_PF<6>	0.1UF	C8260	PCIE_NB_TO_SLOTA_P<6>	84B6	97B8
PCIE_HSON7	A05 97C8	PCIE_NB_TO_SLOTA_NF<7>	0.1UF	C8261	PCIE_NB_TO_SLOTA_N<7>	84B6	97B8
PCIE_HSOP7	B05 97C8	PCIE_NB_TO_SLOTA_PF<7>	0.1UF	C8262	PCIE_NB_TO_SLOTA_P<7>	84B6	97B8
PCIE_HSON8	C11 97C8	PCIE_NB_TO_SLOTA_NF<8>	0.1UF	C8263	PCIE_NB_TO_SLOTA_N<8>	84B6	97B8
PCIE_HSOP8	C10 97C8	PCIE_NB_TO_SLOTA_PF<8>	0.1UF	C8264	PCIE_NB_TO_SLOTA_P<8>	84B6	97B8
PCIE_HSON9	B11 97C8	PCIE_NB_TO_SLOTA_NF<9>	0.1UF	C8265	PCIE_NB_TO_SLOTA_N<9>	84B6	97B8
PCIE_HSOP9	A11 97C8	PCIE_NB_TO_SLOTA_PF<9>	0.1UF	C8266	PCIE_NB_TO_SLOTA_P<9>	84B6	97B8
PCIE_HSON10	F11 97C8	PCIE_NB_TO_SLOTA_NF<10>	0.1UF	C8267	PCIE_NB_TO_SLOTA_N<10>	84B6	97B8
PCIE_HSOP10	F10 97C8	PCIE_NB_TO_SLOTA_PF<10>	0.1UF	C8268	PCIE_NB_TO_SLOTA_P<10>	84B6	97B8
PCIE_HSON11	B09 97C8	PCIE_NB_TO_SLOTA_NF<11>	0.1UF	C8269	PCIE_NB_TO_SLOTA_N<11>	84A6	97B8
PCIE_HSOP11	A09 97C8	PCIE_NB_TO_SLOTA_PF<11>	0.1UF	C8270	PCIE_NB_TO_SLOTA_P<11>	84A6	97A8
PCIE_HSON12	D13 97C8	PCIE_NB_TO_SLOTA_NF<12>	0.1UF	C8271	PCIE_NB_TO_SLOTA_N<12>	84A6	97A8
PCIE_HSOP12	E13 97C8	PCIE_NB_TO_SLOTA_PF<12>	0.1UF	C8272	PCIE_NB_TO_SLOTA_P<12>	84A6	97A8
PCIE_HSON13	B13 97C8	PCIE_NB_TO_SLOTA_NF<13>	0.1UF	C8273	PCIE_NB_TO_SLOTA_N<13>	84A6	97A8
PCIE_HSOP13	A13 97C8	PCIE_NB_TO_SLOTA_PF<13>	0.1UF	C8274	PCIE_NB_TO_SLOTA_P<13>	84A6	97A8
PCIE_HSON14	D09 97C8	PCIE_NB_TO_SLOTA_NF<14>	0.1UF	C8275	PCIE_NB_TO_SLOTA_N<14>	84A6	97A8
PCIE_HSOP14	E09 97C8	PCIE_NB_TO_SLOTA_PF<14>	0.1UF	C8276	PCIE_NB_TO_SLOTA_P<14>	84A6	97A8
PCIE_HSON15	C08 97B8	PCIE_NB_TO_SLOTA_NF<15>	0.1UF	C8277	PCIE_NB_TO_SLOTA_N<15>	84A6	97A8
PCIE_HSOP15	C09 97B8	PCIE_NB_TO_SLOTA_PF<15>	0.1UF	C8278	PCIE_NB_TO_SLOTA_P<15>	84A6	97A8

=PPVCORE_PWRON_NB_PCIE 3A4 82A8 82C2 82C6 82C8

C8231 C8232 C8233 C8234 C8235 C8236
C8241 C8242 C8243 C8237 C8238 C8239 C8240
(1UF 10% 6.3V CERM 402)

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

KODIAK PCI-E X16

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 82 OF 154	

DRAWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT
338S0244	1	IC,RV380 XT, GRAPHICS CTLR	U8400	RV380XT

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

=PP1V2_GPU_PCIE

THIS SHOULD BE ALIASED TO PPVCORE_GPU WITH RV370 AND PP1V2_RUN WITH RV380

L8460 1.8UH 0805
L8461 1.8UH 0805

PP1V2_GPU_PCIE_VDDR
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8460 1UF 10% 6.3V CERM 402
C8461 1UF 10% 6.3V CERM 402
C8462 1UF 10% 6.3V CERM 402
C8463 0.1UF 20% 10V CERM 402
C8464 0.1UF 20% 10V CERM 402
C8465 0.1UF 20% 10V CERM 402
C8466 0.1UF 20% 10V CERM 402

PP1V2_GPU_PCIE_PVDD

SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN

C8450 1UF 10% 6.3V CERM 402
C8451 1UF 10% 6.3V CERM 402
C8452 0.1UF 20% 10V CERM 402
C8453 0.1UF 20% 10V CERM 402
C8454 0.1UF 20% 10V CERM 402
C8455 0.1UF 20% 10V CERM 402

=PP1V8_GPU

L8440 1.8UH 0805

PP1V8_GPU_PCIE_PVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8440 1UF 10% 6.3V CERM 402
C8441 1UF 10% 6.3V CERM 402
C8442 0.1UF 20% 10V CERM 402
C8443 0.1UF 20% 10V CERM 402
C8444 0.1UF 20% 10V CERM 402
C8445 0.1UF 20% 10V CERM 402

PLACE R8470 CLOSE TO U9670

=GPU_RESET_L

U9670 74LCX125 TSSOP

ATI_RESET_L

R8470 33 5% 1/16W MF-LF 402

R8469 8.2K 5% 1/16W MF-LF 402

PERST* AD25 ATI_RESET_L_R

PP1V2_GPU_PCIE_PVDD

R8471 301 1% 1/16W MF-LF 402
R8472 21 1% 1/16W MF-LF 402
R8473 21 1% 1/16W MF-LF 402
R8474 60.4 1% 1/16W MF-LF 402
R8475 21 1% 1/16W MF-LF 402
R8476 60.4 1% 1/16W MF-LF 402
R8477 21 1% 1/16W MF-LF 402
R8478 301 1% 1/16W MF-LF 402

CKA P<0>
CKA N<0>

C8472 5PF +/-0.25PF 50V CERM 402
C8473 5PF +/-0.25PF 50V CERM 402

CLK_PCIE_SLOTA_P<0>
CLK_PCIE_SLOTA_N<0>

PP1V2_GPU_PCIE_PVDD

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

CLK_PCIE_SLOTA_PF<0> AF27 PCIE_REFCLKP
CLK_PCIE_SLOTA_NF<0> AE27 PCIE_REFCLKN

U8400
RV370XT
BGA
(1 OF 5)
OMIT
PCI-E

PCIE_NB_TO_SLOTA_P<0>	AH30	PCIE_RX0P
PCIE_NB_TO_SLOTA_N<0>	AG30	PCIE_RX0N
PCIE_NB_TO_SLOTA_P<1>	AG29	PCIE_RX1P
PCIE_NB_TO_SLOTA_N<1>	AF29	PCIE_RX1N
PCIE_NB_TO_SLOTA_P<2>	AE29	PCIE_RX2P
PCIE_NB_TO_SLOTA_N<2>	AE30	PCIE_RX2N
PCIE_NB_TO_SLOTA_P<3>	AD30	PCIE_RX3P
PCIE_NB_TO_SLOTA_N<3>	AD29	PCIE_RX3N
PCIE_NB_TO_SLOTA_P<4>	AC29	PCIE_RX4P
PCIE_NB_TO_SLOTA_N<4>	AB29	PCIE_RX4N
PCIE_NB_TO_SLOTA_P<5>	AB30	PCIE_RX5P
PCIE_NB_TO_SLOTA_N<5>	AA30	PCIE_RX5N
PCIE_NB_TO_SLOTA_P<6>	AA29	PCIE_RX6P
PCIE_NB_TO_SLOTA_N<6>	Y29	PCIE_RX6N
PCIE_NB_TO_SLOTA_P<7>	W29	PCIE_RX7P
PCIE_NB_TO_SLOTA_N<7>	W30	PCIE_RX7N
PCIE_NB_TO_SLOTA_P<8>	V30	PCIE_RX8P
PCIE_NB_TO_SLOTA_N<8>	V29	PCIE_RX8N
PCIE_NB_TO_SLOTA_P<9>	U29	PCIE_RX9P
PCIE_NB_TO_SLOTA_N<9>	T29	PCIE_RX9N
PCIE_NB_TO_SLOTA_P<10>	T30	PCIE_RX10P
PCIE_NB_TO_SLOTA_N<10>	R30	PCIE_RX10N
PCIE_NB_TO_SLOTA_P<11>	R29	PCIE_RX11P
PCIE_NB_TO_SLOTA_N<11>	P29	PCIE_RX11N
PCIE_NB_TO_SLOTA_P<12>	N29	PCIE_RX12P
PCIE_NB_TO_SLOTA_N<12>	N30	PCIE_RX12N
PCIE_NB_TO_SLOTA_P<13>	M30	PCIE_RX13P
PCIE_NB_TO_SLOTA_N<13>	M29	PCIE_RX13N
PCIE_NB_TO_SLOTA_P<14>	L29	PCIE_RX14P
PCIE_NB_TO_SLOTA_N<14>	K29	PCIE_RX14N
PCIE_NB_TO_SLOTA_P<15>	K30	PCIE_RX15P
PCIE_NB_TO_SLOTA_N<15>	J30	PCIE_RX15N

PCIE_TX0P	AF26	PCIE_SLOTA_TO_NB_PF<0>
PCIE_TX0N	AE26	PCIE_SLOTA_TO_NB_NF<0>
PCIE_TX1P	AC25	PCIE_SLOTA_TO_NB_PF<1>
PCIE_TX1N	AB25	PCIE_SLOTA_TO_NB_NF<1>
PCIE_TX2P	AC27	PCIE_SLOTA_TO_NB_PF<2>
PCIE_TX2N	AB27	PCIE_SLOTA_TO_NB_NF<2>
PCIE_TX3P	AC26	PCIE_SLOTA_TO_NB_PF<3>
PCIE_TX3N	AB26	PCIE_SLOTA_TO_NB_NF<3>
PCIE_TX4P	Y25	PCIE_SLOTA_TO_NB_PF<4>
PCIE_TX4N	W25	PCIE_SLOTA_TO_NB_NF<4>
PCIE_TX5P	Y27	PCIE_SLOTA_TO_NB_PF<5>
PCIE_TX5N	W27	PCIE_SLOTA_TO_NB_NF<5>
PCIE_TX6P	Y26	PCIE_SLOTA_TO_NB_PF<6>
PCIE_TX6N	W26	PCIE_SLOTA_TO_NB_NF<6>
PCIE_TX7P	U25	PCIE_SLOTA_TO_NB_PF<7>
PCIE_TX7N	T25	PCIE_SLOTA_TO_NB_NF<7>
PCIE_TX8P	U27	PCIE_SLOTA_TO_NB_PF<8>
PCIE_TX8N	T27	PCIE_SLOTA_TO_NB_NF<8>
PCIE_TX9P	U26	PCIE_SLOTA_TO_NB_PF<9>
PCIE_TX9N	T26	PCIE_SLOTA_TO_NB_NF<9>
PCIE_TX10P	P25	PCIE_SLOTA_TO_NB_PF<10>
PCIE_TX10N	N25	PCIE_SLOTA_TO_NB_NF<10>
PCIE_TX11P	P27	PCIE_SLOTA_TO_NB_PF<11>
PCIE_TX11N	N27	PCIE_SLOTA_TO_NB_NF<11>
PCIE_TX12P	P26	PCIE_SLOTA_TO_NB_PF<12>
PCIE_TX12N	N26	PCIE_SLOTA_TO_NB_NF<12>
PCIE_TX13P	L25	PCIE_SLOTA_TO_NB_PF<13>
PCIE_TX13N	K25	PCIE_SLOTA_TO_NB_NF<13>
PCIE_TX14P	L27	PCIE_SLOTA_TO_NB_PF<14>
PCIE_TX14N	K27	PCIE_SLOTA_TO_NB_NF<14>
PCIE_TX15P	L26	PCIE_SLOTA_TO_NB_PF<15>
PCIE_TX15N	K26	PCIE_SLOTA_TO_NB_NF<15>

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

0.1UF	C8400	PCIE_SLOTA_TO_NB_P<0>	0.1UF	C8419	PCIE_SLOTA_TO_NB_N<9>
0.1UF	C8401	PCIE_SLOTA_TO_NB_N<0>	0.1UF	C8420	PCIE_SLOTA_TO_NB_P<10>
0.1UF	C8402	PCIE_SLOTA_TO_NB_P<1>	0.1UF	C8421	PCIE_SLOTA_TO_NB_N<10>
0.1UF	C8403	PCIE_SLOTA_TO_NB_N<1>	0.1UF	C8422	PCIE_SLOTA_TO_NB_P<11>
0.1UF	C8404	PCIE_SLOTA_TO_NB_P<2>	0.1UF	C8423	PCIE_SLOTA_TO_NB_N<11>
0.1UF	C8405	PCIE_SLOTA_TO_NB_N<2>	0.1UF	C8424	PCIE_SLOTA_TO_NB_P<12>
0.1UF	C8406	PCIE_SLOTA_TO_NB_P<3>	0.1UF	C8425	PCIE_SLOTA_TO_NB_N<12>
0.1UF	C8407	PCIE_SLOTA_TO_NB_N<3>	0.1UF	C8426	PCIE_SLOTA_TO_NB_P<13>
0.1UF	C8408	PCIE_SLOTA_TO_NB_P<4>	0.1UF	C8427	PCIE_SLOTA_TO_NB_N<13>
0.1UF	C8409	PCIE_SLOTA_TO_NB_N<4>	0.1UF	C8428	PCIE_SLOTA_TO_NB_P<14>
0.1UF	C8410	PCIE_SLOTA_TO_NB_P<5>	0.1UF	C8429	PCIE_SLOTA_TO_NB_N<14>
0.1UF	C8411	PCIE_SLOTA_TO_NB_N<5>	0.1UF	C8430	PCIE_SLOTA_TO_NB_P<15>
0.1UF	C8412	PCIE_SLOTA_TO_NB_P<6>	0.1UF	C8431	PCIE_SLOTA_TO_NB_N<15>
0.1UF	C8413	PCIE_SLOTA_TO_NB_N<6>			
0.1UF	C8414	PCIE_SLOTA_TO_NB_P<7>			
0.1UF	C8415	PCIE_SLOTA_TO_NB_N<7>			
0.1UF	C8416	PCIE_SLOTA_TO_NB_P<8>			
0.1UF	C8417	PCIE_SLOTA_TO_NB_N<8>			
0.1UF	C8418	PCIE_SLOTA_TO_NB_P<9>			

GROUND VIAS FOR LAYER TRANSITIONS

ZH8400 HOLE-VIA
ZH8401 HOLE-VIA
ZH8402 HOLE-VIA
ZH8403 HOLE-VIA
ZH8404 HOLE-VIA
ZH8405 HOLE-VIA
ZH8406 HOLE-VIA
ZH8407 HOLE-VIA
ZH8408 HOLE-VIA
ZH8409 HOLE-VIA
ZH8410 HOLE-VIA
ZH8411 HOLE-VIA
ZH8412 HOLE-VIA
ZH8413 HOLE-VIA
ZH8414 HOLE-VIA
ZH8415 HOLE-VIA
ZH8416 HOLE-VIA
ZH8417 HOLE-VIA
ZH8418 HOLE-VIA
ZH8419 HOLE-VIA

PCIE_CALRN AB24 GPU_PCIE_CALRN
PCIE_CALRP AC23 GPU_PCIE_CALRP

R8400 100 1% 1/16W MF-LF 402
R8401 150 1% 1/16W MF-LF 402

PCIE_CALI AB23 GPU_PCIE_CALI
PCIE_TEST AE25 GPU_PCIE_TEST

R8402 10K 1% 1/16W MF-LF 402
R8403 10K 1% 1/16W MF-LF 402

PCIE_VSS

K28	L28	M24	M25	M26	M27	M28	N28	P28	R23	AH29	AF28	AE28	AD28	AD27	AD26
AD24	AC28	AB28	AA28	R24	R25	R26	R27	R28	T24	T28	U28	V24	V25	V26	V27
V28	W24	W28	Y28	AA23	AA24	AA25	AA26	AA27							

PCIE_PVDD_18: T23 U23 V23 W23
PCIE_PVDD_12: N23 N24 P23
PCIE_VDDR_12: AG26 AG27 AG28 AJ30 AK29

XW8405 SM
PCIE_SLOTA_PRSNT_L

APPLE COMPUTER INC.

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D	051-6863	07
SCALE: NONE	SHT 84 OF 154	

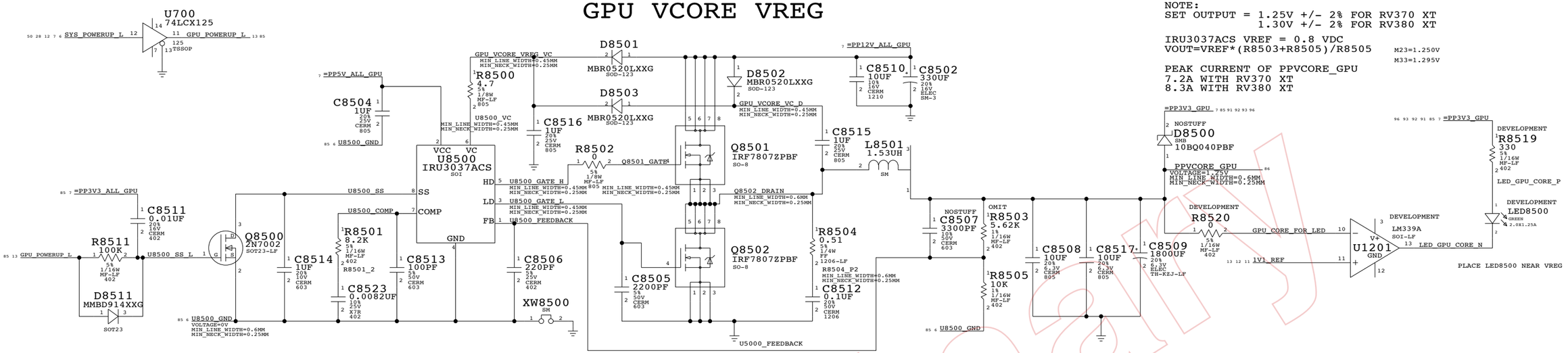
GPU VCORE VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505

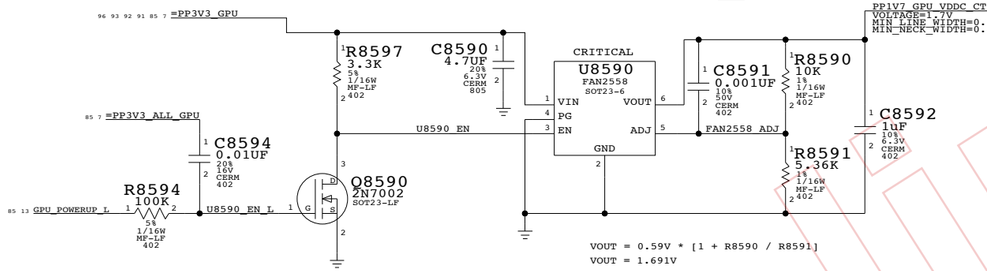
M23=1.250V
M33=1.295V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

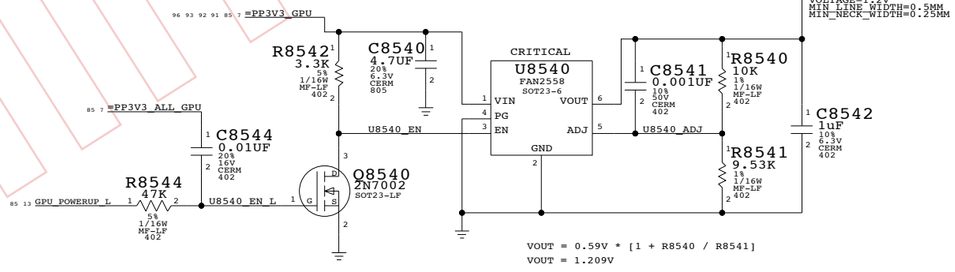


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0291	1	RES,5.62K OHM,1/16W,1%,0402	R8503	RV370XT
114S0295	1	RES,6.19K OHM,1/16W,1%,0402	R8503	RV380XT

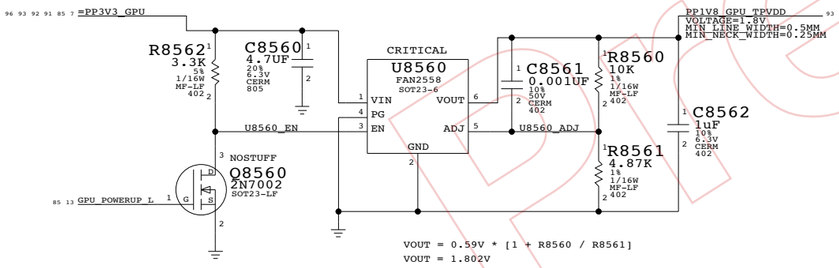
GPU 1.7V VDDC_CT



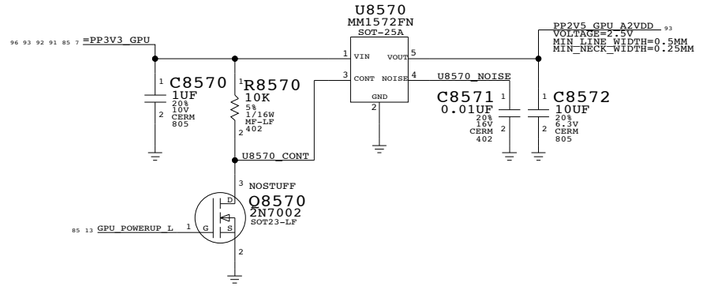
GPU 1.20V PCIE PVDD



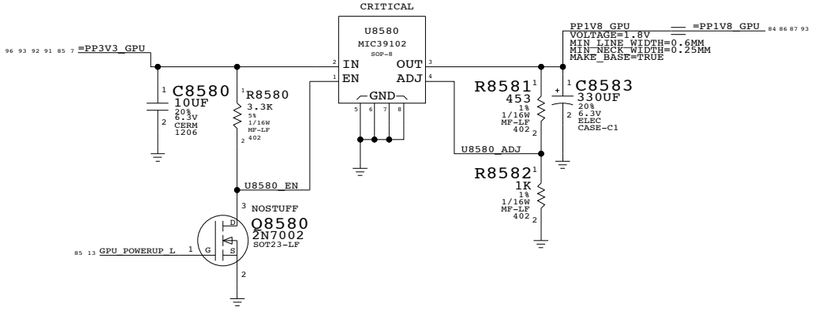
GPU 1.80V TPVDD



GPU 2.5V A2VDD



GPU 1.8V VREG



POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

Graphics Vregs

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

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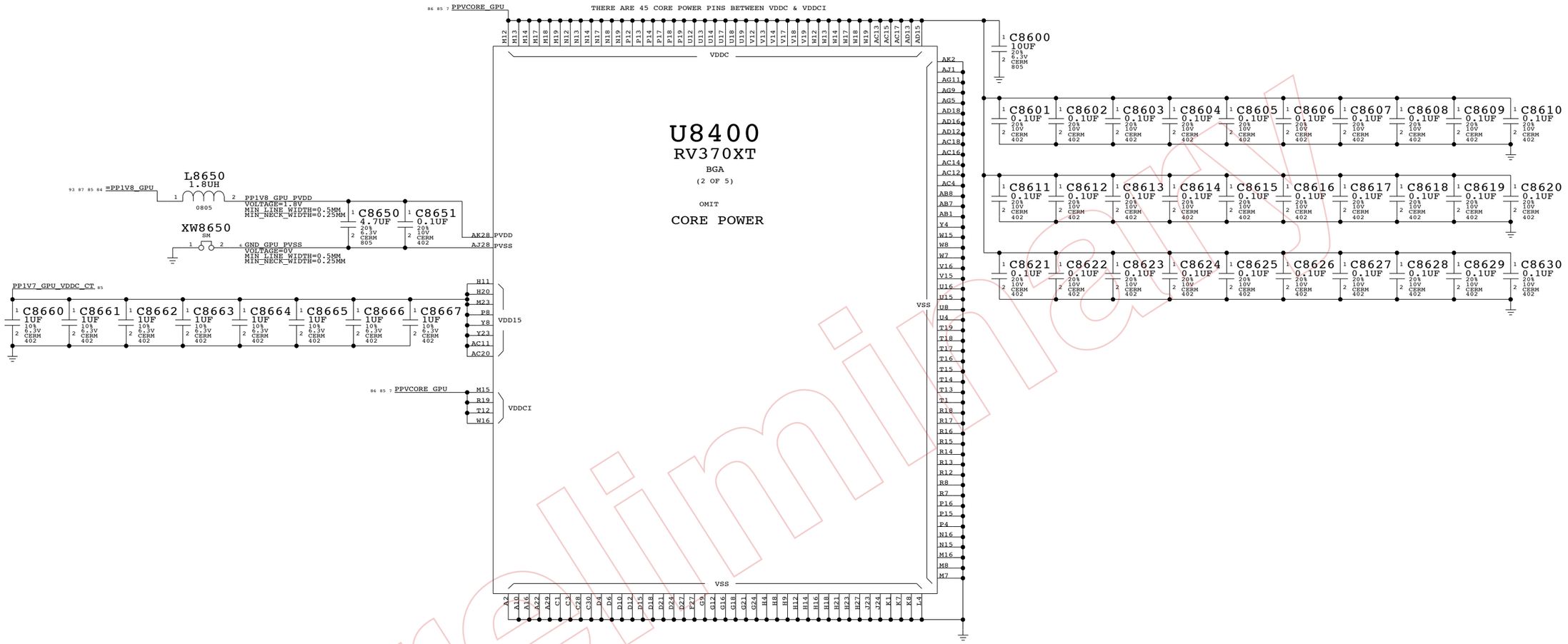
SCALE: NONE	SHT 85 OF 154	



GPU Core Power

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

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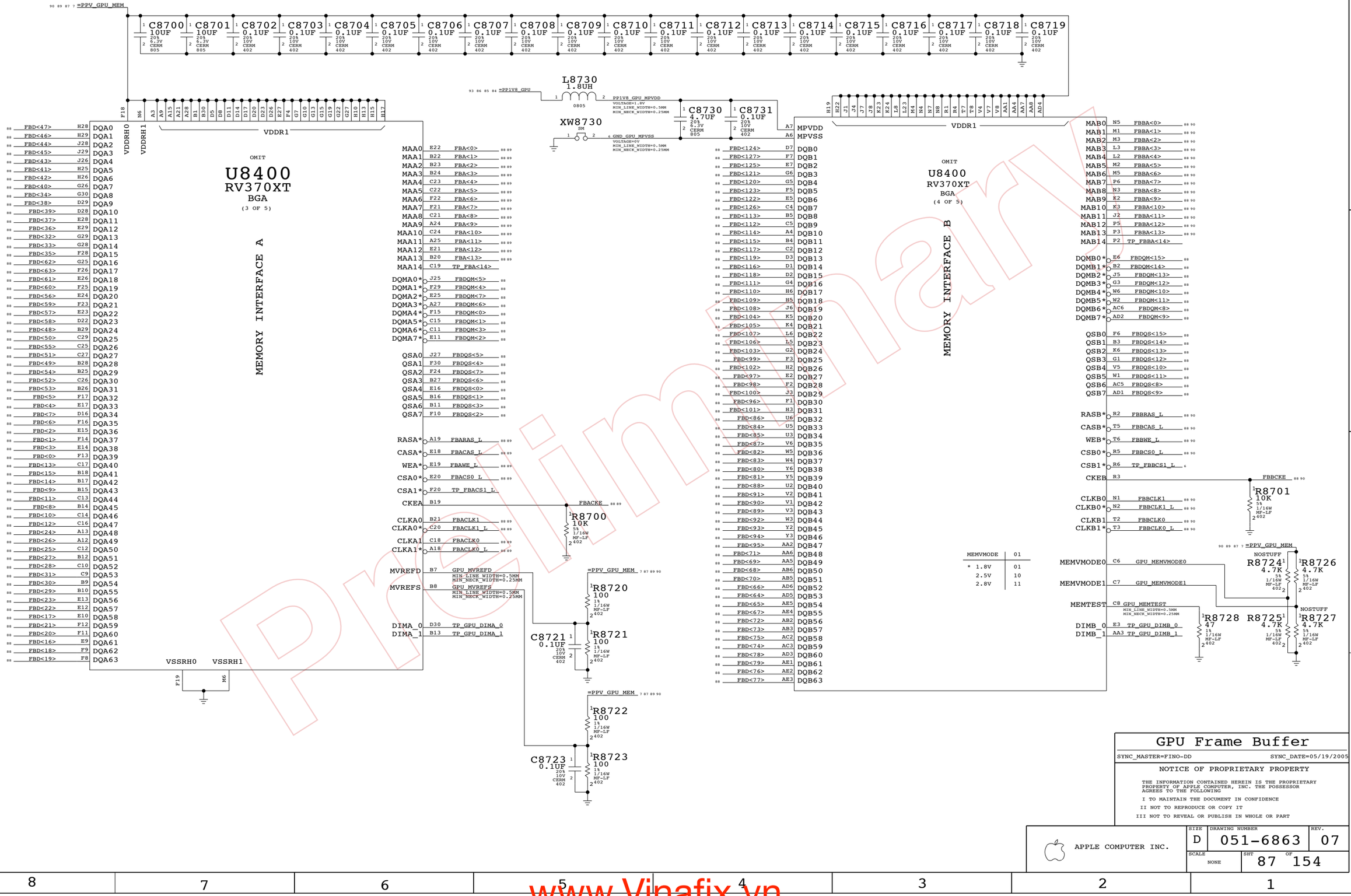
SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 86 OF 154	



FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

FBD<31>	22	3	6	RP8820	RFBD<31>
FBD<30>	22	4	5	RP8820	RFBD<30>
FBD<29>	22	1	8	RP8820	RFBD<29>
FBD<28>	22	2	7	RP8820	RFBD<28>
FBD<27>	22	3	6	RP8821	RFBD<27>
FBD<26>	22	4	5	RP8821	RFBD<26>
FBD<25>	22	2	7	RP8821	RFBD<25>
FBD<24>	22	1	8	RP8821	RFBD<24>
FBD<0>	22	1	8	RP8822	RFBD<0>
FBD<1>	22	2	7	RP8822	RFBD<1>
FBD<2>	22	4	5	RP8822	RFBD<2>
FBD<3>	22	3	6	RP8822	RFBD<3>
FBD<17>	22	1	8	RP8823	RFBD<17>
FBD<16>	22	2	7	RP8823	RFBD<16>
FBD<18>	22	3	6	RP8823	RFBD<18>
FBD<19>	22	4	5	RP8823	RFBD<19>
FBD<15>	22	4	5	RP8824	RFBD<15>
FBD<14>	22	3	6	RP8824	RFBD<14>
FBD<13>	22	2	7	RP8824	RFBD<13>
FBD<12>	22	1	8	RP8824	RFBD<12>
FBD<10>	22	3	6	RP8825	RFBD<10>
FBD<11>	22	4	5	RP8825	RFBD<11>
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FBD<8>	22	2	7	RP8825	RFBD<8>
FBD<5>	22	2	7	RP8826	RFBD<5>
FBD<6>	22	3	6	RP8826	RFBD<6>
FBD<4>	22	1	8	RP8826	RFBD<4>
FBD<7>	22	4	5	RP8826	RFBD<7>
FBD<20>	22	1	8	RP8827	RFBD<20>
FBD<21>	22	2	7	RP8827	RFBD<21>
FBD<22>	22	3	6	RP8827	RFBD<22>
FBD<23>	22	4	5	RP8827	RFBD<23>

FBD<32>	22	3	6	RP8828	RFBD<32>
FBD<33>	22	4	5	RP8828	RFBD<33>
FBD<34>	22	2	7	RP8828	RFBD<34>
FBD<35>	22	1	8	RP8828	RFBD<35>
FBD<36>	22	4	5	RP8816	RFBD<36>
FBD<37>	22	3	6	RP8816	RFBD<37>
FBD<38>	22	2	7	RP8816	RFBD<38>
FBD<39>	22	1	8	RP8816	RFBD<39>
FBD<40>	22	3	6	RP8829	RFBD<40>
FBD<41>	22	4	5	RP8829	RFBD<41>
FBD<42>	22	2	7	RP8829	RFBD<42>
FBD<43>	22	1	8	RP8829	RFBD<43>
FBD<44>	22	4	5	RP8830	RFBD<44>
FBD<45>	22	3	6	RP8830	RFBD<45>
FBD<46>	22	1	8	RP8830	RFBD<46>
FBD<47>	22	2	7	RP8830	RFBD<47>
FBD<48>	22	4	5	RP8831	RFBD<48>
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FBD<51>	22	1	8	RP8831	RFBD<51>
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FBD<54>	22	2	7	RP8800	RFBD<54>
FBD<55>	22	1	8	RP8800	RFBD<55>
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FBD<57>	22	3	6	RP8801	RFBD<57>
FBD<58>	22	1	8	RP8801	RFBD<58>
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FBD<61>	22	2	7	RP8802	RFBD<61>
FBD<62>	22	3	6	RP8802	RFBD<62>
FBD<63>	22	1	8	RP8802	RFBD<63>

FBDQS<0>	22	1	R8800 RFBDQS<0>
FBDQS<1>	22	1	R8801 RFBDQS<1>
FBDQS<2>	22	1	R8802 RFBDQS<2>
FBDQS<3>	22	1	R8803 RFBDQS<3>
FBDQS<4>	22	1	R8804 RFBDQS<4>
FBDQS<5>	22	1	R8805 RFBDQS<5>
FBDQS<6>	22	1	R8806 RFBDQS<6>
FBDQS<7>	22	1	R8807 RFBDQS<7>

FBDQM<0>	22	1	R8830 RFBDQM<0>
FBDQM<1>	22	1	R8831 RFBDQM<1>
FBDQM<2>	22	1	R8832 RFBDQM<2>
FBDQM<3>	22	1	R8833 RFBDQM<3>
FBDQM<4>	22	1	R8834 RFBDQM<4>
FBDQM<5>	22	1	R8835 RFBDQM<5>
FBDQM<6>	22	1	R8836 RFBDQM<6>
FBDQM<7>	22	1	R8837 RFBDQM<7>

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

FBACLK0
R8820 56.2 1% 1/16W MF-LF 402
FBACLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8821 56.2 1% 1/16W MF-LF 402
C8821 0.01UF 20% 16V CERM 402
FBACLK0_L

FBACLK1
R8822 56.2 1% 1/16W MF-LF 402
FBACLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8823 56.2 1% 1/16W MF-LF 402
C8823 0.01UF 20% 16V CERM 402
FBACLK1_L

FRAME BUFFER B TERMINATION

FBD<64>	22	1	8	RP8810	RFBD<64>
FBD<65>	22	4	5	RP8810	RFBD<65>
FBD<66>	22	2	7	RP8810	RFBD<66>
FBD<67>	22	3	6	RP8810	RFBD<67>
FBD<84>	22	1	8	RP8809	RFBD<84>
FBD<85>	22	2	7	RP8809	RFBD<85>
FBD<86>	22	3	6	RP8809	RFBD<86>
FBD<87>	22	4	5	RP8809	RFBD<87>
FBD<72>	22	2	7	RP8819	RFBD<72>
FBD<73>	22	1	8	RP8819	RFBD<73>
FBD<75>	22	4	5	RP8819	RFBD<75>
FBD<74>	22	3	6	RP8819	RFBD<74>
FBD<68>	22	1	8	RP8808	RFBD<68>
FBD<70>	22	2	7	RP8808	RFBD<70>
FBD<69>	22	3	6	RP8808	RFBD<69>
FBD<71>	22	4	5	RP8808	RFBD<71>
FBD<80>	22	1	8	RP8807	RFBD<80>
FBD<81>	22	2	7	RP8807	RFBD<81>
FBD<82>	22	3	6	RP8807	RFBD<82>
FBD<83>	22	4	5	RP8807	RFBD<83>
FBD<76>	22	2	7	RP8817	RFBD<76>
FBD<77>	22	1	8	RP8817	RFBD<77>
FBD<78>	22	4	5	RP8817	RFBD<78>
FBD<79>	22	3	6	RP8817	RFBD<79>
FBD<91>	22	3	6	RP8818	RFBD<91>
FBD<90>	22	4	5	RP8818	RFBD<90>
FBD<89>	22	1	8	RP8818	RFBD<89>
FBD<88>	22	2	7	RP8818	RFBD<88>
FBD<95>	22	3	6	RP8803	RFBD<95>
FBD<94>	22	4	5	RP8803	RFBD<94>
FBD<93>	22	1	8	RP8803	RFBD<93>
FBD<92>	22	2	7	RP8803	RFBD<92>

FBD<96>	22	4	5	RP8815	RFBD<96>
FBD<97>	22	3	6	RP8815	RFBD<97>
FBD<98>	22	2	7	RP8815	RFBD<98>
FBD<99>	22	1	8	RP8815	RFBD<99>
FBD<100>	22	4	5	RP8814	RFBD<100>
FBD<101>	22	3	6	RP8814	RFBD<101>
FBD<102>	22	2	7	RP8814	RFBD<102>
FBD<103>	22	1	8	RP8814	RFBD<103>
FBD<104>	22	4	5	RP8812	RFBD<104>
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FBD<106>	22	2	7	RP8812	RFBD<106>
FBD<107>	22	1	8	RP8812	RFBD<107>
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FBD<112>	22	3	6	RP8811	RFBD<112>
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FBD<114>	22	2	7	RP8811	RFBD<114>
FBD<115>	22	1	8	RP8811	RFBD<115>
FBD<116>	22	3	6	RP8806	RFBD<116>
FBD<117>	22	4	5	RP8806	RFBD<117>
FBD<118>	22	2	7	RP8806	RFBD<118>
FBD<119>	22	1	8	RP8806	RFBD<119>
FBD<120>	22	3	6	RP8804	RFBD<120>
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FBD<125>	22	2	7	RP8805	RFBD<125>
FBD<126>	22	3	6	RP8805	RFBD<126>
FBD<127>	22	1	8	RP8805	RFBD<127>

FBDQS<8>	22	1	R8808 RFBDQS<8>
FBDQS<9>	22	1	R8809 RFBDQS<9>
FBDQS<10>	22	1	R8810 RFBDQS<10>
FBDQS<11>	22	1	R8811 RFBDQS<11>
FBDQS<12>	22	1	R8812 RFBDQS<12>
FBDQS<13>	22	1	R8813 RFBDQS<13>
FBDQS<14>	22	1	R8814 RFBDQS<14>
FBDQS<15>	22	1	R8815 RFBDQS<15>

FBDQM<8>	22	1	R8838 RFBDQM<8>
FBDQM<9>	22	1	R8839 RFBDQM<9>
FBDQM<10>	22	1	R8840 RFBDQM<10>
FBDQM<11>	22	1	R8841 RFBDQM<11>
FBDQM<12>	22	1	R8842 RFBDQM<12>
FBDQM<13>	22	1	R8843 RFBDQM<13>
FBDQM<14>	22	1	R8844 RFBDQM<14>
FBDQM<15>	22	1	R8845 RFBDQM<15>

FBBCLK0
R8824 56.2 1% 1/16W MF-LF 402
FBBCLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8825 56.2 1% 1/16W MF-LF 402
C8825 0.01UF 20% 16V CERM 402
FBBCLK0_L

FBBCLK1
R8826 56.2 1% 1/16W MF-LF 402
FBBCLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8827 56.2 1% 1/16W MF-LF 402
C8827 0.01UF 20% 16V CERM 402
FBBCLK1_L

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBD<127..0>		GPU_FB	GPU_FB	
RFBD<127..0>		GPU_FB	GPU_FB	
FBA<13..0>		GPU_FB	GPU_FB	
FBBA<13..0>		GPU_FB	GPU_FB	
FBDQM<15..0>		GPU_FB	GPU_FB	
FBDQS<15..0>		GPU_FB	GPU_FBDQS	
FBARAS_L		GPU_FB	GPU_FB	
FBACAS_L		GPU_FB	GPU_FB	
FBAWE_L		GPU_FB	GPU_FB	
FBACS0_L		GPU_FB	GPU_FB	
FBACKE		GPU_FB	GPU_FB	
FBBRAS_L		GPU_FB	GPU_FB	
FBBCAS_L		GPU_FB	GPU_FB	
FBBWE_L		GPU_FB	GPU_FB	
FBBCS0_L		GPU_FB	GPU_FB	
FBBCKE		GPU_FB	GPU_FB	

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1
FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1

FB Series Termination

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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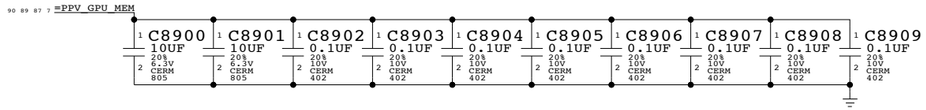

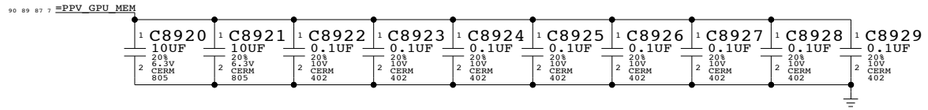

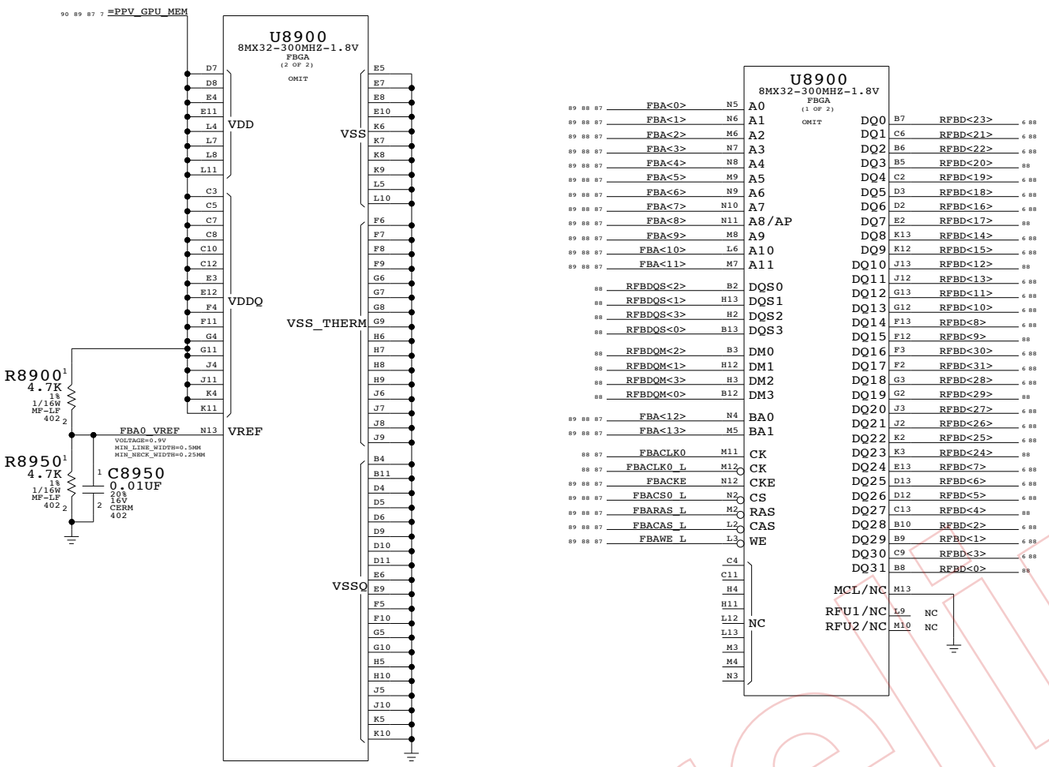

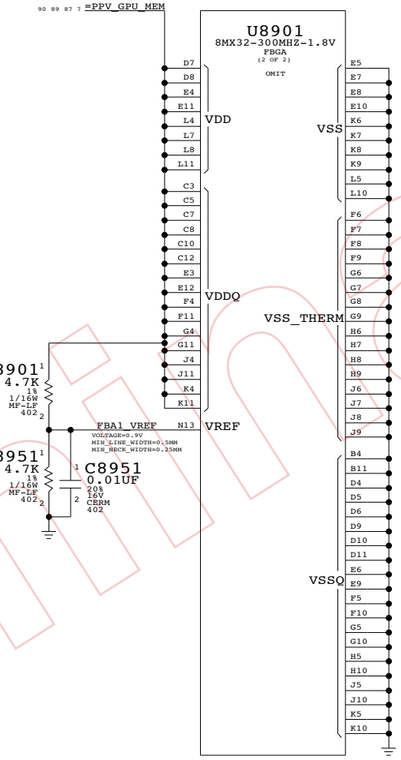

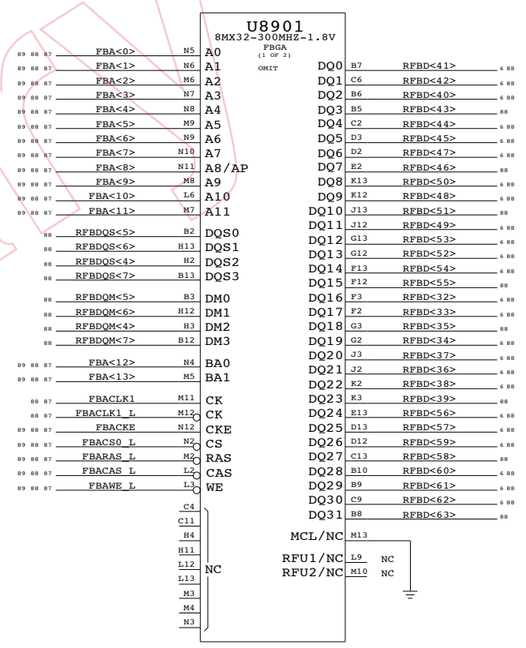

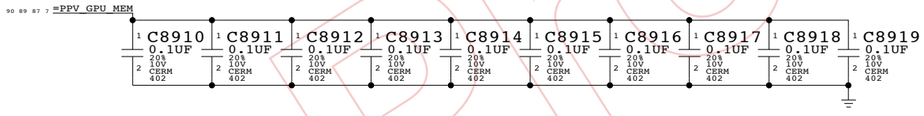

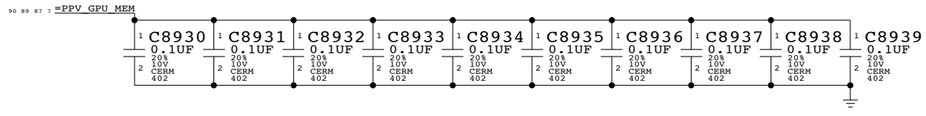

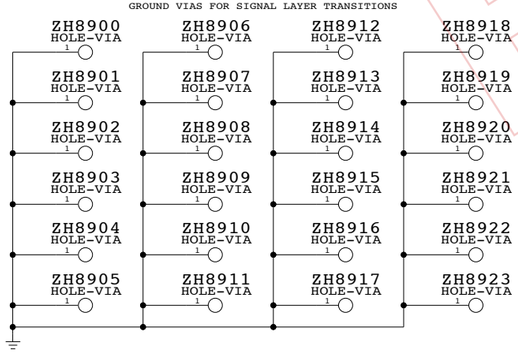

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM A

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APPLE COMPUTER INC.

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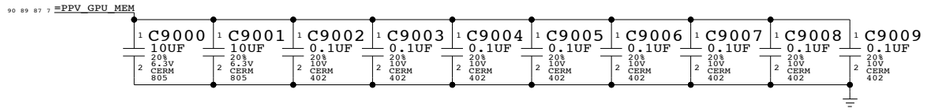
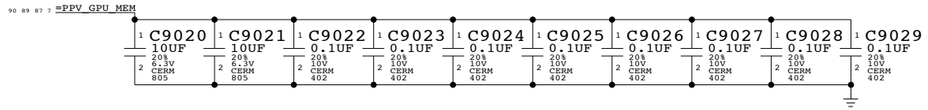
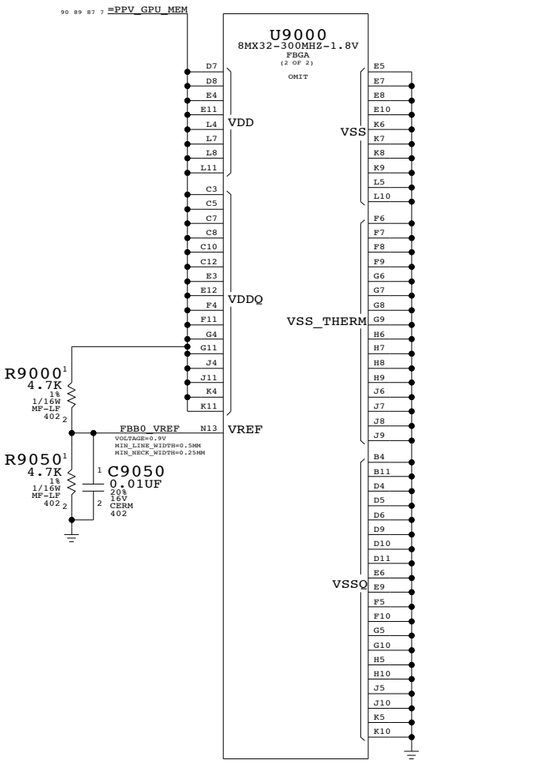
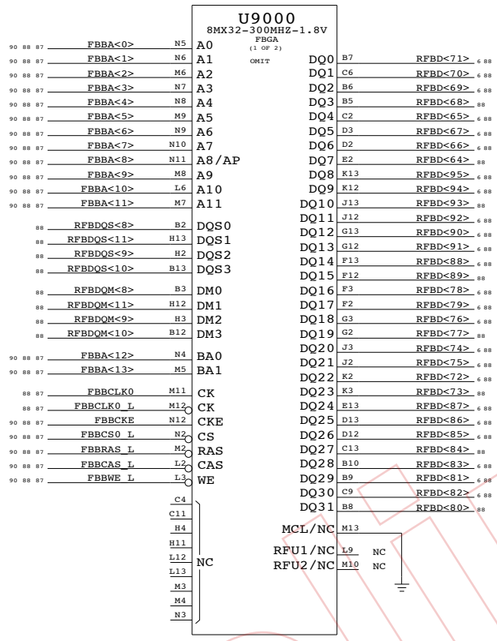
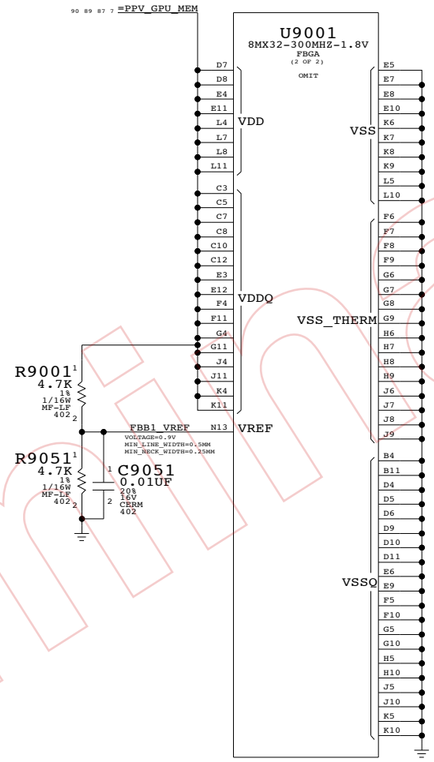
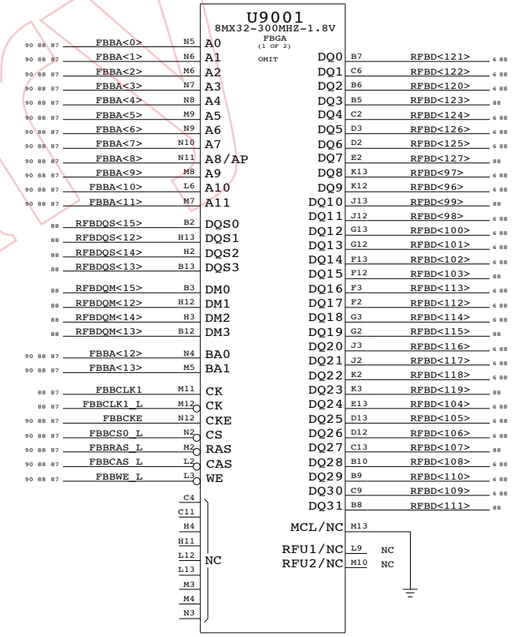


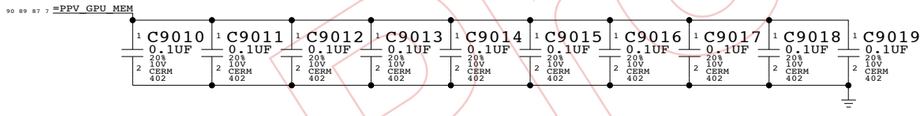


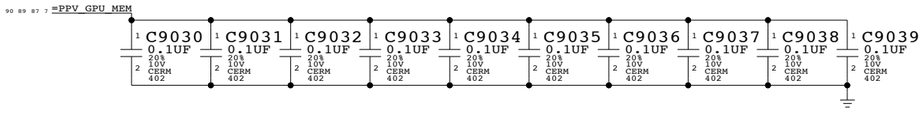




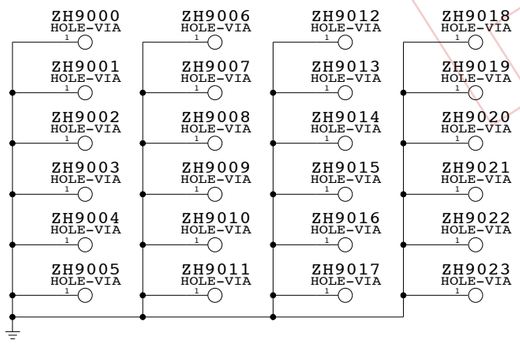








GROUND VIAS FOR SIGNAL LAYER TRANSITIONS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM B

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APPLE COMPUTER INC.

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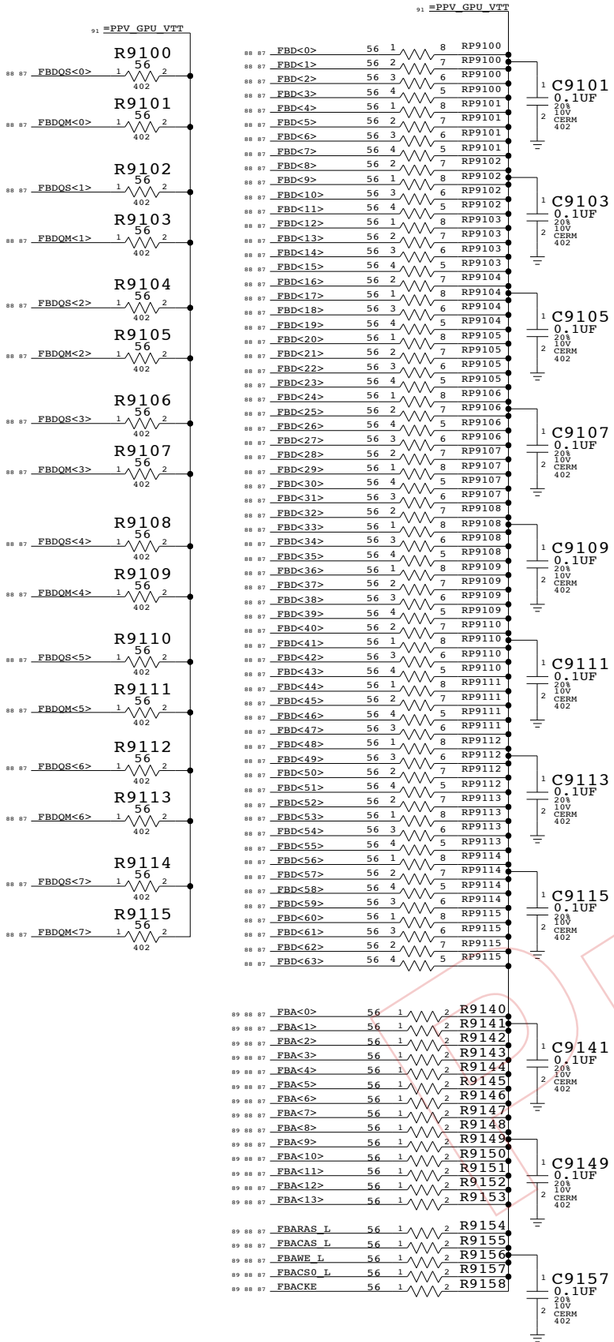
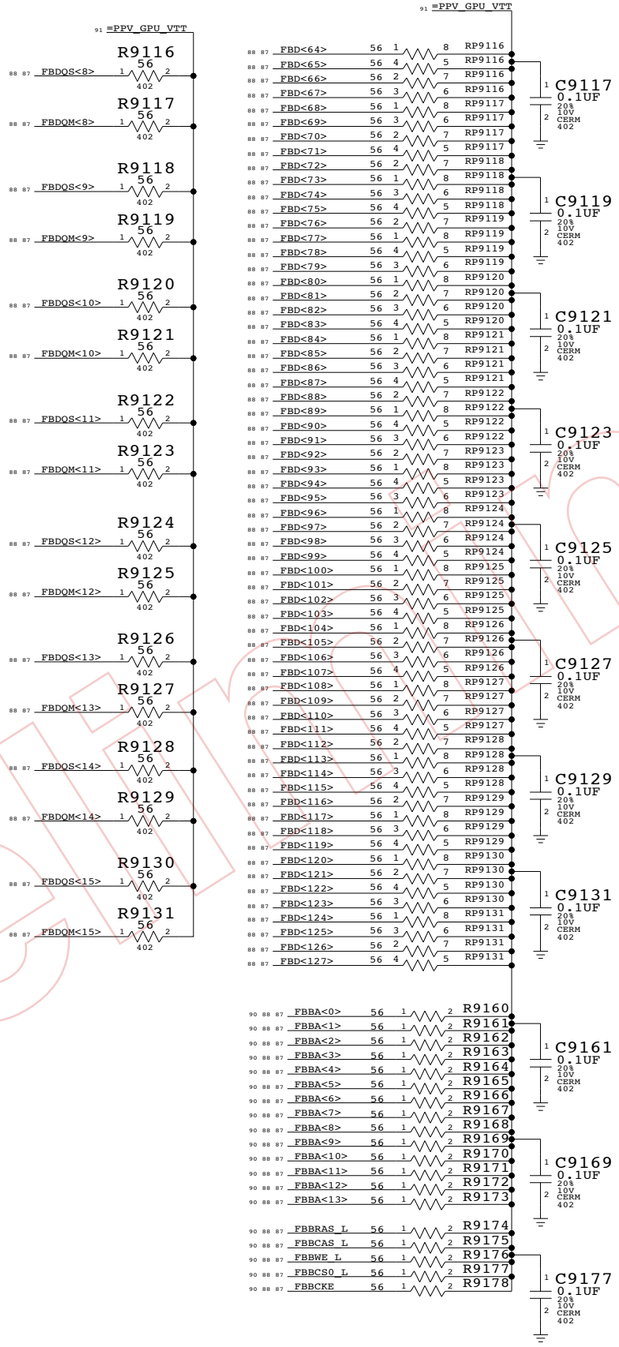
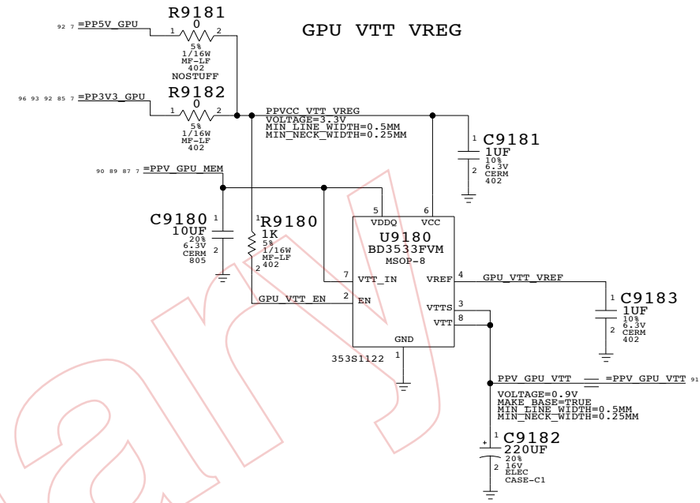
FRAME BUFFER A TERMINATION



FRAME BUFFER B TERMINATION

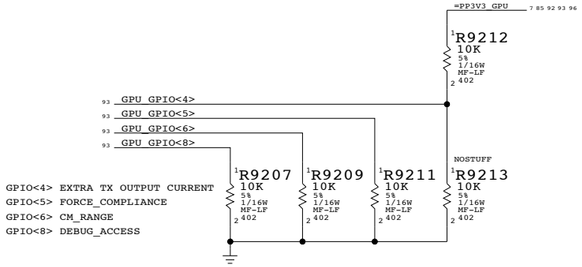


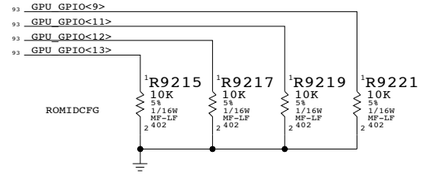
GPU VTT VREG



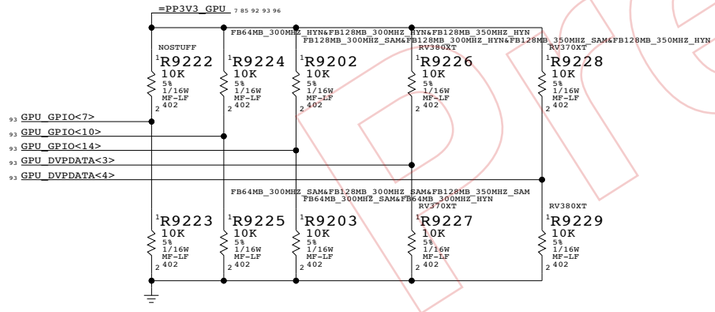
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
	SCALE: NONE	SHT 91 OF 154	

ATI STRAPS



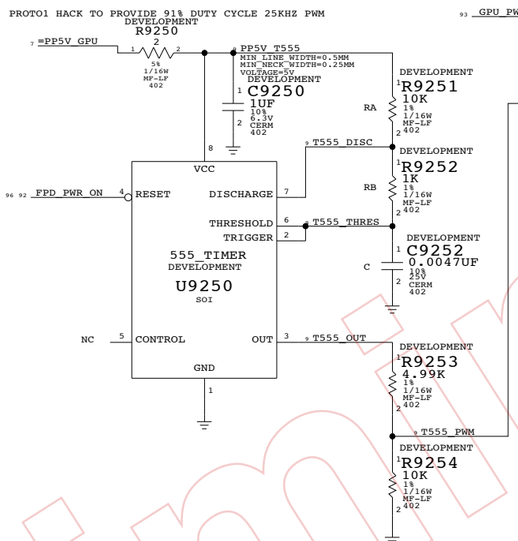


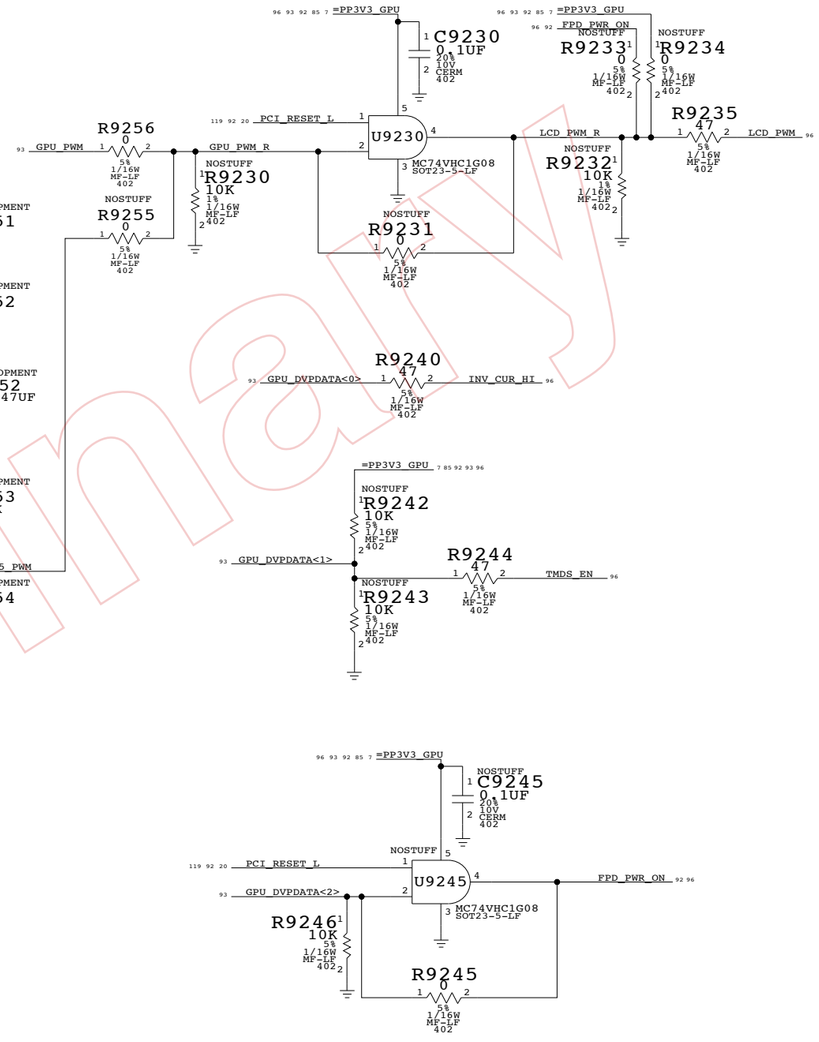
MEMORY STRAPS



GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS





GPU Straps

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APPLE COMPUTER INC.

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SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

(PLACE R9371 CLOSE TO OSC)

L9370 FERR-EMI-100-OHM (PLACE THE OSCILLATOR AND R9372 AND R9373 CLOSE TO ATI PIN AH28)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0131	1	RES,130 OHM,1/16W,1%,0402	R9373	RV370XT
114S0134	1	RES,140 OHM,1/16W,1%,0402	R9373	RV380XT

U8400 RV370XT BGA (5 OF 5) OMIT

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_TCKM	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	I2C	I2C	
	I2C	I2C	
	I2C	I2C	
	I2C	I2C	

GPU THERMAL SENSOR

PLACE C9392 CLOSE TO TEMP SENSOR

PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

GPU DVI & DACs

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APPLE COMPUTER INC.

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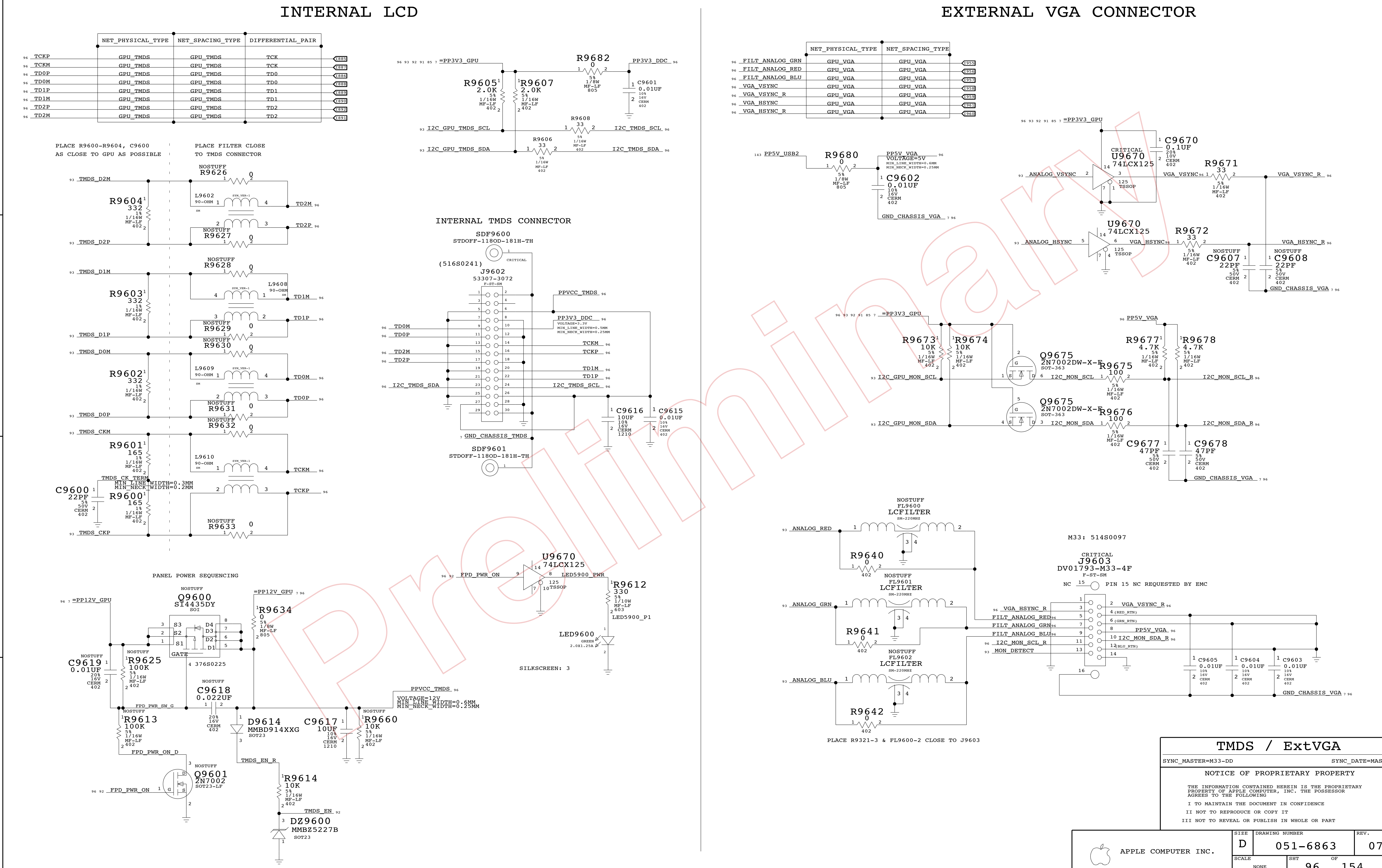
INTERNAL LCD

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TCKP	GPU_TMDS	GPU_TMDS	TCK
TCKM	GPU_TMDS	GPU_TMDS	TCK
TD0P	GPU_TMDS	GPU_TMDS	TD0
TD0M	GPU_TMDS	GPU_TMDS	TD0
TD1P	GPU_TMDS	GPU_TMDS	TD1
TD1M	GPU_TMDS	GPU_TMDS	TD1
TD2P	GPU_TMDS	GPU_TMDS	TD2
TD2M	GPU_TMDS	GPU_TMDS	TD2

EXTERNAL VGA CONNECTOR

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
FILT_ANALOG_GRN	GPU_VGA	GPU_VGA
FILT_ANALOG_RED	GPU_VGA	GPU_VGA
FILT_ANALOG_BLU	GPU_VGA	GPU_VGA
VGA_VSYNC	GPU_VGA	GPU_VGA
VGA_VSYNC_R	GPU_VGA	GPU_VGA
VGA_HSYNC	GPU_VGA	GPU_VGA
VGA_HSYNC_R	GPU_VGA	GPU_VGA



TMDS / ExtVGA

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-6863 REV. 07

SCALE NONE SHT 96 OF 154

KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
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PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
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PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
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PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

KODIAK PCI-E CONST

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	97	154

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

PLANE-SPLIT AC RETURN PATHS

LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)

=PPVCORE_PWRON_NB_HT 3A4 98D5 98D7

C9806 1UF 10% 6.3V CERM 402
C9807 1UF 10% 6.3V CERM 402
C9808 1UF 10% 6.3V CERM 402
C9809 1UF 10% 6.3V CERM 402
C9810 1UF 10% 6.3V CERM 402
C9811 1UF 10% 6.3V CERM 402
C9812 1UF 10% 6.3V CERM 402
C9813 1UF 10% 6.3V CERM 402
C9814 1UF 10% 6.3V CERM 402
C9815 1UF 10% 6.3V CERM 402

98D7 98D5 3A4 =PPVCORE_PWRON_NB_HT
C9834 0.1UF 20% 10V CERM 402
=P1V2_PWRON_HT_NBTX 3C2 98B1 98C8 98D1 98D3 98D4

KODIAK CORES

PP9806 P4MM SM
1.6V
Q63 = PP1V6

98D7 3A4 =PPVCORE_PWRON_NB_HT

98D2 3C1 =PP2V5_PWRON_NB_HT
L9800 0.22UH 0805-1
104D4 PWR_HT_AVDD
C9800 0.01UF 10% 16V CERM 402
C9801 10UF 10% 6.3V X5R 805
C9802 1UF 10% 6.3V CERM 402
104D4 98C3 98A6 6A3 KOD_L15_GND (THIS PAGE)

PP9807 P4MM SM
1.2V
Q63 = PP1V2

=PP1V2_PWRON_HT_NBTX 3C2 98B1 98C8 98D1 98D3 98D5
104D4 PWR_HT_AVDD2
L9801 0.22UH 0805-1
=PP2V5_PWRON_NB_HT 3C1 98D7
C9803 1UF 10% 6.3V CERM 402
C9804 10UF 10% 6.3V X5R 805
C9805 0.01UF 10% 16V CERM 402
KOD_L15_GND 6A3 98A6 98C6 104D4 (THIS PAGE)

98D5 98D4 98D1 98C8 98B1 3C2 =P1V2_PWRON_HT_NBTX
C9817 1UF 10% 6.3V CERM 402
C9818 1UF 10% 6.3V CERM 402
C9819 1UF 10% 6.3V CERM 402
C9820 1UF 10% 6.3V CERM 402
C9821 1UF 10% 6.3V CERM 402
C9822 1UF 10% 6.3V CERM 402
C9823 1UF 10% 6.3V CERM 402
C9824 1UF 10% 6.3V CERM 402
C9825 1UF 10% 6.3V CERM 402
C9826 1UF 10% 6.3V CERM 402

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)

98D5 98D4 98D3 98C8 98B1 3C2 =P1V2_PWRON_HT_NBTX
C9827 1UF 10% 6.3V CERM 402
C9828 1UF 10% 6.3V CERM 402
C9829 1UF 10% 6.3V CERM 402
C9830 1UF 10% 6.3V CERM 402
C9831 1UF 10% 6.3V CERM 402
C9832 1UF 10% 6.3V CERM 402
C9833 1UF 10% 6.3V CERM 402
C9839 1UF 10% 6.3V CERM 402
C9840 1UF 10% 6.3V CERM 402
C9841 1UF 10% 6.3V CERM 402
C9847 1UF 10% 6.3V CERM 402
C9842 1UF 10% 6.3V CERM 402
C9843 1UF 10% 6.3V CERM 402
C9844 1UF 10% 6.3V CERM 402
C9845 1UF 10% 6.3V CERM 402
C9846 1UF 10% 6.3V CERM 402

98D5 98D4 98D3 98D1 98B1 3C2 =P1V2_PWRON_HT_NBTX

104B8 100D3 99C4 HT_MB_TO_NB_CLK_N<0>
104B8 100D3 99C4 HT_MB_TO_NB_CLK_P<0>
104B8 100B3 99D4 HT_MB_TO_NB_CTL_N<0>
104B8 100B3 99D4 HT_MB_TO_NB_CTL_P<0>

PP9808 P4MM SM
HTM2NC0-
HTM2NC0+
PP9809 P4MM SM

K15
HT_REFCLK_AVDD (1.65V-2.75V) (1.6V-1.2V)

E25 HT_CLK_RXN0
D25 HT_CLK_RXP0
J27 HT_CTL_RXN0
K27 HT_CTL_RXP0
F26 HT_CAD_RXN0
F27 HT_CAD_RXP0
F25 HT_CAD_RXN1
F24 HT_CAD_RXP1
A25 HT_CAD_RXN2
B25 HT_CAD_RXP2
G25 HT_CAD_RXN3
H25 HT_CAD_RXP3
L25 HT_CAD_RXN4
K25 HT_CAD_RXP4
G27 HT_CAD_RXN5
H27 HT_CAD_RXP5
J25 HT_CAD_RXN6
J26 HT_CAD_RXP6
C26 HT_CAD_RXN7
C27 HT_CAD_RXP7
F22 HT_CLK_RXN1
F23 HT_CLK_RXP1
E21 HT_CTL_RXP1
D21 HT_CTL_RXN1
E23 HT_CAD_RXN8
D23 HT_CAD_RXP8
A23 HT_CAD_RXN9
B23 HT_CAD_RXP9
H23 HT_CAD_RXN10
G23 HT_CAD_RXP10
C22 HT_CAD_RXN11
C23 HT_CAD_RXP11
K23 HT_CAD_RXN12
L23 HT_CAD_RXP12
J23 HT_CAD_RXN13
J24 HT_CAD_RXP13
A21 HT_CAD_RXN14
B21 HT_CAD_RXP14
C24 HT_CAD_RXN15
C25 HT_CAD_RXP15
K19 HT_PVTREF0
L19 HT_PVTREF1
L17 HT_PVTREF2_ALT
K17 HT_PVTREF3_ALT
J16 HT_REFCLK_N
J15 HT_REFCLK_P
(200MHZ)
HT_REFCLK_AGND

A22 HT_RX_GND
A26 HT_RX_GND
B24 HT_RX_GND
D22 HT_RX_GND
D26 HT_RX_GND
E24 HT_RX_GND
G26 HT_RX_GND
H24 HT_RX_GND
K22 HT_RX_GND
L24 HT_RX_GND

HT_RX_VDD A24
HT_RX_VDD B22
HT_RX_VDD B26
HT_RX_VDD D24
HT_RX_VDD E22
HT_RX_VDD E26
HT_RX_VDD G24
HT_RX_VDD H26
HT_RX_VDD K24
HT_RX_VDD L22

H15
HT_REFCLK_AVDD2 (1.65V-2.75V) (1.6V-1.2V)

A16 HT_VD4
A20 HT_VD4
B14 HT_VD4
B18 HT_VD4
D16 HT_VD4
D20 HT_VD4
E18 HT_VD4
G16 HT_VD4
G20 HT_VD4
H18 HT_VD4
H22 HT_VD4
K16 HT_VD4
K20 HT_VD4
L18 HT_VD4
M17 HT_VD4
M21 HT_VD4
N19 HT_VD4

A14 HT_VD4_GND
A18 HT_VD4_GND
B16 HT_VD4_GND
B20 HT_VD4_GND
D18 HT_VD4_GND
E16 HT_VD4_GND
E20 HT_VD4_GND
G18 HT_VD4_GND
G22 HT_VD4_GND
H16 HT_VD4_GND
H20 HT_VD4_GND
K18 HT_VD4_GND
L16 HT_VD4_GND
L20 HT_VD4_GND
M16 HT_VD4_GND
M20 HT_VD4_GND
N18 HT_VD4_GND

U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE

HT_CLK_TXN0 J19 HT_NB_TO_MB_CLK_N<0> 99C7 100D7 104D8
HT_CLK_TXP0 J20 HT_NB_TO_MB_CLK_P<0> 99C7 100D7 104D8
HT_CTL_TXN0 J22 HT_NB_TO_MB_CTL_N<0> 99D7 100B6 104D8
HT_CTL_TXP0 J21 HT_NB_TO_MB_CTL_P<0> 99D7 100B6 104D8
HT_CAD_TXN0 F16 HT_NB_TO_MB_CAD_N<0> 99C7 100D6 104D8
HT_CAD_TXP0 F17 HT_NB_TO_MB_CAD_P<0> 99C7 100D6 104D8
HT_CAD_TXN1 G17 HT_NB_TO_MB_CAD_N<1> 99C7 100C6 104D8
HT_CAD_TXP1 H17 HT_NB_TO_MB_CAD_P<1> 99C7 100C6 104C8
HT_CAD_TXN2 J18 HT_NB_TO_MB_CAD_N<2> 99B7 100C6 104C8
HT_CAD_TXP2 J17 HT_NB_TO_MB_CAD_P<2> 99B7 100C6 104C8
HT_CAD_TXN3 F18 HT_NB_TO_MB_CAD_N<3> 99B7 100C6 104C8
HT_CAD_TXP3 F19 HT_NB_TO_MB_CAD_P<3> 99B7 100C6 104C8
HT_CAD_TXN4 G19 HT_NB_TO_MB_CAD_N<4> 99B5 100C6 104C8
HT_CAD_TXP4 H19 HT_NB_TO_MB_CAD_P<4> 99B5 100C6 104C8
HT_CAD_TXN5 G21 HT_NB_TO_MB_CAD_N<5> 99C5 100C6 104C8
HT_CAD_TXP5 H21 HT_NB_TO_MB_CAD_P<5> 99C5 100C6 104C8
HT_CAD_TXN6 F21 HT_NB_TO_MB_CAD_N<6> 99C5 100C6 104C8
HT_CAD_TXP6 F20 HT_NB_TO_MB_CAD_P<6> 99C5 100C6 104C8
HT_CAD_TXN7 K21 HT_NB_TO_MB_CAD_N<7> 99C5 100C6 104C8
HT_CAD_TXP7 L21 HT_NB_TO_MB_CAD_P<7> 99C5 100C6 104C8
HT_CLK_TXN1 C16 HT_NB_TO_MB_CLK_N<1> 99A5 100C7 104D8
HT_CLK_TXP1 C17 HT_NB_TO_MB_CLK_P<1> 99B5 100C7 104D8
HT_CTL_TXP1 E15 HT_NB_TO_MB_CTL_P<1>
HT_CTL_TXN1 D15 HT_NB_TO_MB_CTL_N<1>
HT_CAD_TXN8 D19 HT_NB_TO_MB_CAD_N<8> 99D7 100C6 104C8
HT_CAD_TXP8 E19 HT_NB_TO_MB_CAD_P<8> 99D7 100C6 104C8
HT_CAD_TXN9 D17 HT_NB_TO_MB_CAD_N<9> 99C7 100C6 104C8
HT_CAD_TXP9 E17 HT_NB_TO_MB_CAD_P<9> 99C7 100C6 104C8
HT_CAD_TXN10 C19 HT_NB_TO_MB_CAD_N<10> 99C5 100C6 104C8
HT_CAD_TXP10 C18 HT_NB_TO_MB_CAD_P<10> 99D5 100C6 104C8
HT_CAD_TXN11 A15 HT_NB_TO_MB_CAD_N<11> 99D5 100C6 104C8
HT_CAD_TXP11 B15 HT_NB_TO_MB_CAD_P<11> 99D5 100C6 104C8
HT_CAD_TXN12 A17 HT_NB_TO_MB_CAD_N<12> 99D5 100B6 104C8
HT_CAD_TXP12 B17 HT_NB_TO_MB_CAD_P<12> 99D5 100B6 104C8
HT_CAD_TXN13 B19 HT_NB_TO_MB_CAD_N<13> 99D7 100B6 104C8
HT_CAD_TXP13 A19 HT_NB_TO_MB_CAD_P<13> 99D7 100B6 104C8
HT_CAD_TXN14 C15 HT_NB_TO_MB_CAD_N<14> 99D5 100B6 104C8
HT_CAD_TXP14 C14 HT_NB_TO_MB_CAD_P<14> 99D5 100B6 104C8
HT_CAD_TXN15 C20 HT_NB_TO_MB_CAD_N<15> 99A4 100B6 104B8
HT_CAD_TXP15 C21 HT_NB_TO_MB_CAD_P<15> 99A4 100B6 104B8
HT_LDTSTOP_L AF06 HT_LDTSTOP_L 99A5 101A4 102A6
HT_LDTREQ_L AF09 HT_LDTREQ_L 103B6 99A4 101A4 102B4
HT_PWROK AF03 HT_PWROK 103B3 99A5 101A7 102A6
HT_RESET_L AE11 HT_RESET_L 103B6 99A4 101A7 102B4

=PP1V2_PWRON_HT_NBTX 3C2 98C8 98D1 98D3 98D4 98D5
NOSTUFF R9808 8.2K 5% 1/16W MF-LF 402
NOSTUFF R9809 8.2K 5% 1/16W MF-LF 402

=PP2V5_PWRON_HT 101D5 102B2 102B7 3C1 99B3 99B7 100D3 100D7 101B7 101D2 103D3
R9810 1K 5% 1/16W MF-LF 402
R9811 1K 5% 1/16W MF-LF 402
R9812 1K 5% 1/16W MF-LF 402
R9813 1K 5% 1/16W MF-LF 402

KODIAK HT RECEIVE CLOCKS

PP9802 P4MM SM
MHT1-
MHT1+
PP9803 P4MM SM

R9806 8.2K 5% 1/16W MF-LF 402
R9807 8.2K 5% 1/16W MF-LF 402

104B8 100C3 99D7 HT_MB_TO_NB_CLK_N<1>
104B8 100C3 99D7 HT_MB_TO_NB_CLK_P<1>

PP9800 P4MM SM
MHT0-
MHT0+
PP9801 P4MM SM

KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

104D8 26C2 HT_NB_REFCLK_P<0>
R9802 20.5 1% 1/16W MF-LF 402
C9837 0.01UF 10% 16V CERM 402
104D8 HT_NB_P<0>
R9803 29.4 1% 1/16W MF-LF 402
NOSTUFF C9836 0.01UF 10% 16V CERM 402
HT_NB_G
R9804 29.4 1% 1/16W MF-LF 402
C9838 0.01UF 10% 16V CERM 402
104D8 HT_NB_N<0>
R9805 20.5 1% 1/16W MF-LF 402
104D8 26C2 HT_NB_REFCLK_N<0>

R9800 100 1% 1/16W MF-LF 402
R9801 200 1% 1/16W MF-LF 402

104D8 HT_NB_REFCLK_PF<0>
104D8 HT_NB_REFCLK_NF<0>

PP9804 P4MM SM
HREF0-
HREF0+
PP9805 P4MM SM

104D4 98C3 98C6 6A3 KOD_L15_GND (THIS PAGE)
L15
XW9800 SM

KODIAK HT REFCLK

KODIAK HT16

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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LAST_MODIFIED=Thu May 19 14:27:39 2005
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 98 OF 154	

DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT_NB_TO_MB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_MB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE				HT_MB_TO_NB_CAD_P<8..15>
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE				HT_MB_TO_NB_CAD_N<8..15>
TP_HT_MB_TO_NB_CLK_N<1>	TRUE				HT_MB_TO_NB_CLK_N<1>
TP_HT_MB_TO_NB_CLK_P<1>	TRUE				HT_MB_TO_NB_CLK_P<1>
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE				HT_NB_TO_MB_CAD_P<8..15>
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE				HT_NB_TO_MB_CAD_N<8..15>
NC_HT_NB_TO_MB_CLK_N<1>	TRUE				HT_NB_TO_MB_CLK_N<1>
NC_HT_NB_TO_MB_CLK_P<1>	TRUE				HT_NB_TO_MB_CLK_P<1>
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0		HT_CLK	HT_CLK
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0

HT ALIASES

FINO-EG 05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE NONE	SHT 101 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	
HT_CLK66M_SB	0.38mm SPACING	
	P3MM SPACING	

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.

HT_CLK66M_SB_C 103B6
HT_CLK66M_SB 26C2 103B7
HT_LDTRESET_L 98A1 99A4 101A7 102B4 103B6

103D3 103C2 103A7 3B2 =PP1V2_PWRON_SB_HT

RA300 3.3 5% 1/8W MF-LF 805
PP1V2_PWRON_HT_PLLDVDD VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CA300 10UF 10% 6.3V X5R 805
CA301 1uF 10% 6.3V CERM 402

RA310 3.3 5% 1/8W MF-LF 805
PP1V2_PWRON_HT_PLLAVDD VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CA310 10UF 10% 6.3V X5R 805
CA311 1uF 10% 6.3V CERM 402

=PP2V5_PWRON_HT 3C1 98B1 99B3 99B7 100D3 100D7 101B7 101D2 101D5 102B2 102B7
CA320 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT 3B2 103A7 103C2 103D6
CA302 10UF 10% 6.3V X5R 805
CA330 0.1uF 20% 10V CERM 402
CA331 0.1uF 20% 10V CERM 402
CA332 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT 3B2 103A7 103D3 103D6
CA309 10UF 10% 6.3V X5R 805
CA340 0.1uF 20% 10V CERM 402
CA341 0.1uF 20% 10V CERM 402
CA342 0.1uF 20% 10V CERM 402

HTS2MC0+ PPA300 P4MM SM
HTS2MC0- PPA301 P4MM SM
HTS2MC0+ PPA303 P4MM SM
HTS2MC0- PPA304 P4MM SM

U2300 SHASTA V1.1 BGA-LF (3 OF 8) SEE_TABLE

AVDD	DVDD	VDDP	HT_RXVDD	HT_TXVDD		
HT_PLL		HT				
C7	B6	B19	B15	B17	G13	B12	B9	G11

HYPERTRANSPORT

104C4	102D7	101C1	HT_MB_TO_SB_CLK_P<0>	D15	HT_CLKIN_P	HT_CLKOUT_P	B10	HT_SB_TO_MB_CLK_P<0>	101C5	102B6	104B4
104C4	102D7	101C1	HT_MB_TO_SB_CLK_N<0>	C15	HT_CLKIN_N	HT_CLKOUT_N	A10	HT_SB_TO_MB_CLK_N<0>	101C5	102B6	104B4
104C4	102C7	101C1	HT_MB_TO_SB_CAD_P<0>	D17	HT_CADIN_0_P	HT_CADOUT_0_P	D10	HT_SB_TO_MB_CAD_P<0>	101C4	102D4	104B4
104C4	102C7	101C1	HT_MB_TO_SB_CAD_N<0>	C17	HT_CADIN_0_N	HT_CADOUT_0_N	C10	HT_SB_TO_MB_CAD_N<0>	101C4	102D4	104B4
104B4	102C5	101C1	HT_MB_TO_SB_CAD_P<1>	B18	HT_CADIN_1_P	HT_CADOUT_1_P	B8	HT_SB_TO_MB_CAD_P<1>	101C4	102D2	104B4
104C4	102C5	101C1	HT_MB_TO_SB_CAD_N<1>	A18	HT_CADIN_1_N	HT_CADOUT_1_N	A8	HT_SB_TO_MB_CAD_N<1>	101C4	102D2	104B4
104B4	102C7	101C1	HT_MB_TO_SB_CAD_P<2>	F15	HT_CADIN_2_P	HT_CADOUT_2_P	E11	HT_SB_TO_MB_CAD_P<2>	101C4	102D4	104B4
104B4	102C7	101C1	HT_MB_TO_SB_CAD_N<2>	E15	HT_CADIN_2_N	HT_CADOUT_2_N	F11	HT_SB_TO_MB_CAD_N<2>	101C4	102D4	104B4
104B4	102C5	101C1	HT_MB_TO_SB_CAD_P<3>	D16	HT_CADIN_3_P	HT_CADOUT_3_P	D11	HT_SB_TO_MB_CAD_P<3>	101C4	102D2	104B4
104B4	102C5	101C1	HT_MB_TO_SB_CAD_N<3>	C16	HT_CADIN_3_N	HT_CADOUT_3_N	C11	HT_SB_TO_MB_CAD_N<3>	101C4	102D2	104B4
104B4	102C7	101C1	HT_MB_TO_SB_CAD_P<4>	B16	HT_CADIN_4_P	HT_CADOUT_4_P	A11	HT_SB_TO_MB_CAD_P<4>	101C4	102D4	104A4
104B4	102D7	101C1	HT_MB_TO_SB_CAD_N<4>	A16	HT_CADIN_4_N	HT_CADOUT_4_N	B11	HT_SB_TO_MB_CAD_N<4>	101C4	102C4	104A4
104B4	102D5	101C1	HT_MB_TO_SB_CAD_P<5>	D14	HT_CADIN_5_P	HT_CADOUT_5_P	C12	HT_SB_TO_MB_CAD_P<5>	101C4	102C2	104A4
104B4	102D5	101C1	HT_MB_TO_SB_CAD_N<5>	C14	HT_CADIN_5_N	HT_CADOUT_5_N	D12	HT_SB_TO_MB_CAD_N<5>	101C4	102C2	104A4
104B4	102D7	101C1	HT_MB_TO_SB_CAD_P<6>	E14	HT_CADIN_6_P	HT_CADOUT_6_P	E12	HT_SB_TO_MB_CAD_P<6>	101C4	102C4	104A4
104B4	102D7	101C1	HT_MB_TO_SB_CAD_N<6>	F14	HT_CADIN_6_N	HT_CADOUT_6_N	F12	HT_SB_TO_MB_CAD_N<6>	101C4	102C4	104A4
104B4	102D5	101C1	HT_MB_TO_SB_CAD_P<7>	B14	HT_CADIN_7_P	HT_CADOUT_7_P	A13	HT_SB_TO_MB_CAD_P<7>	101C4	102C2	104A4
104B4	102D5	101C1	HT_MB_TO_SB_CAD_N<7>	A14	HT_CADIN_7_N	HT_CADOUT_7_N	B13	HT_SB_TO_MB_CAD_N<7>	101C4	102C2	104A4
104C4	102A4	101B1	HT_MB_TO_SB_CTL_P<0>	F13	HT_CTLIN_P	HT_CTLOUT_P	C13	HT_SB_TO_MB_CTL_P<0>	101B4	102C4	104B4
104C4	102A4	101B1	HT_MB_TO_SB_CTL_N<0>	E13	HT_CTLIN_N	HT_CTLOUT_N	D13	HT_SB_TO_MB_CTL_N<0>	101B4	102C4	104B4

102A6	101A7	99A5	98A1	HT_PWROK	E16	HT_PWROK_H
103D6 102B4	101A7	99A4	98A1	HT_LDTRESET_L	C18	HT_RESET_L
102A6	101A4	99A5	98A1	HT_LDTSTOP_L	E17	HT_LDTSTOP_L
103D6	HT_CLK66M_SB_C				C8	HT_REFCLK
	SB_HT_S100M66M				D8	HT_S100M66M
	SB_SELHT100				V6	SEL_HT00_H

HT_LDTREQ_L A19 HT_LDTREQ_SB_L
HT_R100P E10 SB_HT_R100_P
HT_R100N F10 SB_HT_R100_N

RA301 0 5% 1/16W MF-LF 402 — HT_LDTREQ_L 98A1 99A4 101A4 102B4

HT_PLL AGND DGND — HT_RXGND — HT_TXGND

RA350 82.5 1% 1/16W MF-LF 402
CA350 47pF 5% 50V CERM 402
CA351 47pF 5% 50V CERM 402

P4MM SM PPA302

RA355 0 5% 1/16W MF-LF 402 — 103D6 26C2 HT_CLK66M_SB
1.0V pk-pk

103D6 103D3 103C2 3B2 =PP1V2_PWRON_SB_HT

NOSTUFF RA352 4.7K 1% 1/16W MF-LF 402 — 1 = 100MHz
NOSTUFF RA354 10K 5% 1/16W MF-LF 402 — 1 = 100MHz
RA353 4.7K 1% 1/16W MF-LF 402 — 0 = 66MHz
RA351 1K 1% 1/16W MF-LF 402 — 0 = 200MHz

HT RefClk	HT I/F Speed	
1 = 100MHz	1 = 100MHz	DETERMINES THE OPERATING FREQUENCY OF HT CORE
0 = 66MHz	0 = 200MHz	1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
		0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 103 OF 154	

LAST_MODIFIED=Thu May 19 14:26:14 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
BUS	P3MM_SPACING	

PCI_AD<31..28>	120B6	121C3	121C4	122B5	122C5	125C3			
PCI_AD<27>	120B6	121C4	122C6	125C3					
PCI_AD<26..24>	120B6	121C3	121C4	122C5	125C3				
PCI_AD<23>	120B6	121C4	122C5						
PCI_AD<22>	120C6	121C3	122C5						
PCI_AD<21>	120C6	121C4	122C5						
PCI_AD<20>	120C6	121C3	122C5	125B5					
PCI_AD<19..18>	120C6	121C3	121C4	122C5	125B5				
PCI_AD<17>	120C6	121C1	121C4	122C5	125B5				
PCI_AD<16..0>	120C6	120D6	121B3	121B4	121C3	121C4	122C5	122D5	125B5	125C5
PCI_CBE_L<3..0>	120B6	121B3	121C4	122B5					
PCI_PAR	120B6	121C3	122B5						
PCI_DEVSEL_L	119B2	120B6	121C3	122B5					
PCI_FRAME_L	119B2	120B6	121C3	122B5					
PCI_IRDY_L	119B2	120B6	121C4	122B5					
PCI_TRDY_L	119A2	120B6	121C3	122B5					
PCI_STOP_L	119A2	120B6	121C3	122B5					
PCI_CLK66M_SB_INT	26A2	119C5							

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

119B8 119B1 3A7 =PP3V3_SB_PCI

PPB905 P4MM SM PP_3V3SBPCI_B9 XWB900 SM

CB910 10UF 10% 6.3V X5R 805
CB900 0.1uF 20% 10V CERM 402
CB901 0.1uF 20% 10V CERM 402
CB902 0.1uF 20% 10V CERM 402
CB903 0.1uF 20% 10V CERM 402
CB904 0.1uF 20% 10V CERM 402

NO STUFF
CB911 10UF 10% 6.3V X5R 805
CB905 0.1uF 20% 10V CERM 402
CB906 0.1uF 20% 10V CERM 402
CB907 0.1uF 20% 10V CERM 402
CB908 0.1uF 20% 10V CERM 402
CB909 0.1uF 20% 10V CERM 402

XWB901 SM PP_2V5PWRONSB_B9 P4MM SM PPB906

=PP2V5_PWRON_SB 3C1 23B2 23C2 24D5 138C6

CB920 0.1uF 20% 10V CERM 402
CB921 0.1uF 20% 10V CERM 402
CB922 0.1uF 20% 10V CERM 402
CB923 0.1uF 20% 10V CERM 402

AA22 B22 E21 B16 J21 M16 N21 R20 U21 V19 B20 J18 M20 U20
VDDOPC PCIVDDP

SEE_TABLE U2300 SHASTA V1.1 BGA-LF (4 OF 8) PCI

PPB900 P4MM SM P3MM SPACING
119D6 26A2 PCI_CLK66M_SB_INT AB9 PCIBR_CLK_H

PPB901 P4MM SM 26A1 PCI_CLK33M_SB_EXT_RR U19 PCI1CLK_H

NOSTUFF CB912 2PF ±/-0.25PF 50V COG 402-1 STUFF NEAR SHASTA

PCI1AD_0_H	L18	PCI_SB_AD<0>	6C1 120D7
PCI1AD_1_H	K19	PCI_SB_AD<1>	120D7
PCI1AD_2_H	L22	PCI_SB_AD<2>	6C1 120C7
PCI1AD_3_H	M22	PCI_SB_AD<3>	6C1 120C7
PCI1AD_4_H	M18	PCI_SB_AD<4>	6C1 120C7
PCI1AD_5_H	L20	PCI_SB_AD<5>	120C7
PCI1AD_6_H	M21	PCI_SB_AD<6>	120C7
PCI1AD_7_H	M16	PCI_SB_AD<7>	120C7
PCI1AD_8_H	M20	PCI_SB_AD<8>	120C7
PCI1AD_9_H	P22	PCI_SB_AD<9>	6C1 120C7
PCI1AD_10_H	M17	PCI_SB_AD<10>	6C1 120C7
PCI1AD_11_H	N18	PCI_SB_AD<11>	6C1 120C7
PCI1AD_12_H	M19	PCI_SB_AD<12>	120C7
PCI1AD_13_H	N19	PCI_SB_AD<13>	6C1 120C7
PCI1AD_14_H	P21	PCI_SB_AD<14>	6C1 120C7
PCI1AD_15_H	R22	PCI_SB_AD<15>	120C7
PCI1AD_16_H	P20	PCI_SB_AD<16>	120C7
PCI1AD_17_H	V21	PCI_SB_AD<17>	120C7
PCI1AD_18_H	P18	PCI_SB_AD<18>	6C1 120C7
PCI1AD_19_H	T20	PCI_SB_AD<19>	6C1 120C7
PCI1AD_20_H	R16	PCI_SB_AD<20>	120C7
PCI1AD_21_H	R17	PCI_SB_AD<21>	6C1 120C7
PCI1AD_22_H	W21	PCI_SB_AD<22>	120C7
PCI1AD_23_H	Y22	PCI_SB_AD<23>	6C1 120B7
PCI1AD_24_H	R18	PCI_SB_AD<24>	120B7
PCI1AD_25_H	T19	PCI_SB_AD<25>	6C1 120B7
PCI1AD_26_H	T18	PCI_SB_AD<26>	6C1 120B7
PCI1AD_27_H	Y21	PCI_SB_AD<27>	120B7
PCI1AD_28_H	W20	PCI_SB_AD<28>	6C1 120B7
PCI1AD_29_H	T16	PCI_SB_AD<29>	6C1 120B7
PCI1AD_30_H	AA21	PCI_SB_AD<30>	6C1 120B7
PCI1AD_31_H	T17	PCI_SB_AD<31>	6C1 120B7

"Slot A" - AD17
121C4 119B7 PCI_SLOTA_REQ_L AB18 PCI1REQ_0_L
121C3 119B7 PCI_SLOTA_GNT_L AA18 PCI1GNT_0_L

"Slot G" - AD27
122B5 119B7 PCI_SLOTG_REQ_L AB20 PCI1REQ_1_L
122B5 119B7 PCI_SLOTG_GNT_L AB19 PCI1GNT_1_L

"Slot D" - AD20
119B7 PCI_SLOTD_REQ_L V17 PCI1REQ_2_L
119A7 PCI_SLOTD_GNT_L V18 PCI1GNT_2_L

125B7 121B4 ROM_CS_L AB8 ROMCS_L
125B7 121B3 ROM_OE_L AA9 ROMOE_L
125B7 121B4 ROM_WE_L Y10 ROMRW_L

PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	6C1 120B7
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	6C1 120B7
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	6C1 120B7
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	6C1 120B7
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	120B7
PCI1FRAME_L	T21	PCI_SB_FRAME_L	6B1 120B7
PCI1IRDY_L	R21	PCI_SB_IRDY_L	6B1 120B7
PCI1TRDY_L	P19	PCI_SB_TRDY_L	6B1 120B7
PCI1STOP_L	P17	PCI_SB_STOP_L	6B1 120B7
PCI1PAR_H	N17	PCI_SB_PAR	6B1 120B7
PCI1RST_L	U18	SB_PCI_RESET_L	

NET_SPACING_TYPE=P3MM SPACING

=PP3V3_PWRON_SB 3A3 20D2 23B7 24A6 24B7 24C3 24D2 29B4 29C7 120C4 149A3 154D2

RB955 4.7K 1% 1/16W MF-LF 402
CB950 0.1uF 20% 10V CERM 402
NOSTUFF RB950 4.7K 1% 1/16W MF-LF 402

UB950 MC74VHC1G08 SOT23-5-LF

PCI_RESET_L 120B4 120C2

122A7 29D6 28D4 24B7 21C5 SYS_IO_RESET_L

Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

RB900 0 5% 1/16W MF-LF 402 NOSTUFF

=PP3V3_SB_PCI 3A7 119B1 119C7

RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTA_REQ_L 119B5 121C4
PCI_SLOTA_GNT_L 119B5 121C3
PCI_SLOTG_REQ_L 119B5 122B5
PCI_SLOTG_GNT_L 119B5 122B5
RPB901 4.7K 5% 1/16W SM-LF
PCI_SLOTD_REQ_L 119B5
PCI_SLOTD_GNT_L 119B5

119C7 119B8 3A7 =PP3V3_SB_PCI

RPB902 4.7K 5% 1/16W SM-LF
122B5 121C3 120B6 119D6 PCI_DEVSEL_L
122B5 121C3 120B6 119D6 PCI_FRAME_L
122B5 121C4 120B6 119D6 PCI_IRDY_L
122B5 121C3 120B6 119D6 PCI_TRDY_L
RPB901 4.7K 5% 1/16W SM-LF
122B5 121C3 120B6 119D6 PCI_STOP_L

Shasta PCI Interface		
SYNC_MASTER=Q63	SYNC_DATE=05/19/2005	
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863
	REV. 07	
	SCALE NONE	SHT 119 OF 154

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DRAWING

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119C3	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119D6	121B5	122D5 125C5
119B3	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119D6	121B5	122D5 125C5
119B3	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119D6	121B4	122D5 125C5
119B3	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119D6	121B5	122D5 125C5
119B3	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119D6	121B4	122C5 125C5
119B3	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119D6	121B5	122C5 125C5
119B3	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119D6	121B5	122C5 125C5
119B3	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119D6	121B5	122C5 125C5
119B3	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119D6	121B5	122C5 125C5
119B3	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119D6	121B5	122C5 125C5
119B3	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119D6	121B4	122C5 125B5
119B3	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119D6	121B4	122C5 125B5
119B3	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119D6	121B5	122C5 125B5
119B3	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119D6	121B4	122C5 125B5
119B3	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119D6	121B4	122C5 125B5
119B3	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119D6	121B4	122C5 125B5
119B3	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119D6	121B4	122C5 125B5

RC000

119B3	PCI_SB_AD<17>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<17>	119D6	121C4	121C6	122C5 125B5

119B3	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119D6	121C5	122C5	125B5
119B3	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119D6	121C5	122C5	125B5
119B3	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119D6	121C4	122C5	125B5
119B3	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119D6	121C5	122C5	
119B3	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119D6	121C5	122C5	
119B3	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119D6	121C4	122C5	
119B3	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119D6	121C4	122C5	125C3
119B3	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119D6	121C5	122C5	125C3
119B3	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119D6	121C5	122C5	125C3

RC001

119A3	PCI_SB_AD<27>		1	2	47 5% 1/16W MF-LF 402	PCI_AD<27>	119D6	121C5	122C6	125C3

119A3	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119D6	121C4	122C5	125C3
119A3	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119D6	121C5	122C5	125C3
119A3	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119D6	121C5	122B5	125C3
119A3	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119D6	121C4	122B5	125C3
119A3	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119D6	121B5	122B5	
119A3	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119D6	121B4	122B5	
119A3	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119D6	121B4	122B5	
119A3	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119D6	121C5	122B5	
119A3	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119B2	119D6	121C5	122B5
119A3	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119B2	119D6	121C4	122B5
119A3	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119B2	119D6	121C5	122B5
119A3	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119A2	119D6	121C4	122B5
119A3	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119A2	119D6	121B5	122B5
119A3	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119D6	121B5	122B5	

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

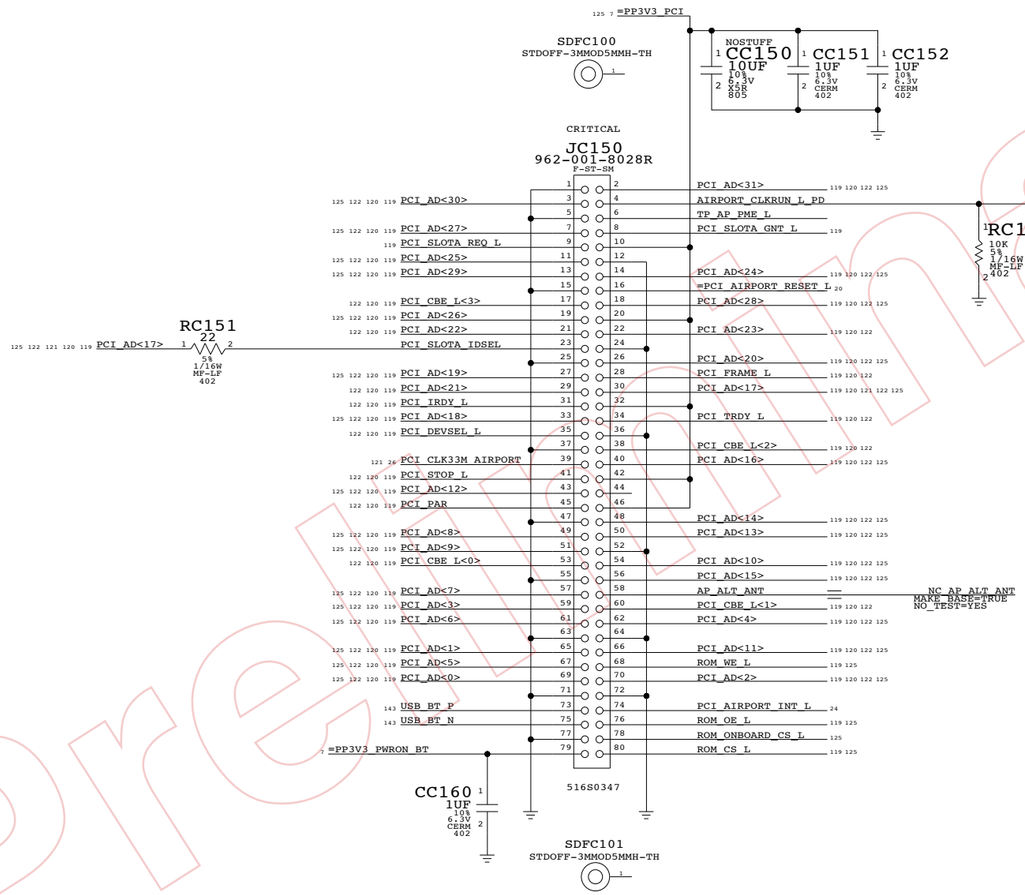
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT 121 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 120A3 122B5

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122B7 3A7 =PPVIO_PCI_USB2

CC201 0.1uF 20% 10V CERM 402
CC202 0.1uF 20% 10V CERM 402
CC203 0.1uF 20% 10V CERM 402

XWC200 SM P4MM PP_VIOPCIUSB2_C2 PPC203

VDD_PCI
R3 R4 C8

UC200
NEC_UPD720101_USB2
FBGA-LF

125C5	121B3	120D6	119D6	PCI_AD<0>	M1	AD0	
125C5	121B4	120D6	119D6	PCI_AD<1>	P1	AD1	
125C5	121B3	120C6	119D6	PCI_AD<2>	N1	AD2	
125C5	121B4	120C6	119D6	PCI_AD<3>	P2	AD3	
125C5	121B3	120C6	119D6	PCI_AD<4>	N2	AD4	
125C5	121B4	120C6	119D6	PCI_AD<5>	M3	AD5	
125C5	121B3	120C6	119D6	PCI_AD<6>	N3	AD6	
125C5	121B4	120C6	119D6	PCI_AD<7>	M4	AD7	
125C5	121B4	120C6	119D6	PCI_AD<8>	L1	AD8	
125C5	121B3	120C6	119D6	PCI_AD<9>	L2	AD9	
125B5	121C4	120C6	119D6	PCI_AD<10>	K1	AD10	
125B5	121C3	120C6	119D6	PCI_AD<11>	L3	AD11	
125B5	121C4	120C6	119D6	PCI_AD<12>	K2	AD12	
125B5	121C3	120C6	119D6	PCI_AD<13>	K3	AD13	
125B5	121C4	120C6	119D6	PCI_AD<14>	J1	AD14	
125B5	121C3	120C6	119D6	PCI_AD<15>	J2	AD15	
125B5	121C3	120C6	119D6	PCI_AD<16>	F1	AD16	
125B5	121C4	121C1	120C6	119D6	PCI_AD<17>	E1	AD17
125B5	121C3	120C6	119D6	PCI_AD<18>	E2	AD18	
125B5	121C4	120C6	119D6	PCI_AD<19>	D1	AD19	
125B5	121C3	120C6	119D6	PCI_AD<20>	D2	AD20	
	121C4	120C6	119D6	PCI_AD<21>	D3	AD21	
	121C3	120C6	119D6	PCI_AD<22>	C1	AD22	
	121C4	120B6	119D6	PCI_AD<23>	C2	AD23	
125C3	121C3	120B6	119D6	PCI_AD<24>	B1	AD24	
125C3	121C4	120B6	119D6	PCI_AD<25>	A2	AD25	
125C3	121C3	120B6	119D6	PCI_AD<26>	B2	AD26	
125C3	121C4	120C6	119D6	PCI_AD<27>	C4	AD27	(PCI_AD<27>)
125C3	121C3	120B6	119D6	PCI_AD<28>	A3	AD28	
125C3	121C4	120B6	119D6	PCI_AD<29>	C3	AD29	
125C3	121C3	120B6	119D6	PCI_AD<30>	B3	AD30	
125C3	121C4	120B6	119D6	PCI_AD<31>	A4	AD31	
	121B3	120B6	119D6	PCI_CBE_L<0>	M2	CBE0	
	121C4	120B6	119D6	PCI_CBE_L<1>	J3	CBE1	
	121C4	120B6	119D6	PCI_CBE_L<2>	F3	CBE2	
	121C4	120B6	119D6	PCI_CBE_L<3>	C5	CBE3	
	121C3	120B6	119D6	PCI_PAR	J4	PAR	
121C3	120B6	119D6	119B2	PCI_FRAME_L	F3	FRAME	
121C4	120B6	119D6	119B2	PCI_IRDY_L	F4	IRDY	
121C3	120B6	119D6	119A2	PCI_TRDY_L	G1	TRDY	
121C3	120B6	119D6	119A2	PCI_STOP_L	G3	STOP	
		PCI_SLOTG_IDSEL			B1	IDSEL	
121C3	120B6	119D6	119B2	PCI_DEVSEL_L	G2	DEVSEL	
		119B7	119B5	PCI_SLOTG_REQ_L	C6	REQ	
		119B7	119B5	PCI_SLOTG_GNT_L	D6	GNT	
		NEC_PERR_L_PU			H2	PERR	
		NEC_SERR_L_PU			H1	SERR	OD
		NEC_INTA_L			C7	INTA	OD
		NEC_INTB_L			B7	INTB	OD
		NEC_INTC_L			A7	INTC	OD
		122D6 120A3 =PCI_CLK33M_USB2			A8	PCLK	
		NEC_VBBRST_L			B8	VBBRST	(CHIP RESET)
		NEC_CRUN_L_PD			M6	CRUN	
		NEC_PME_L			D5	PME	OD
					C5	VCCRST	(PCI RESET)
		TP_NEC_SMI_L			L6	SMI	OD
		NEC_LEGC_PD			L7	LEGC	

IPD	NTEST1	M8	TP_NEC_NTEST1
IPD	SMC	M7	TP_NEC_SMC
IPD	TEB	N7	TP_NEC_TEB
IPD	AMC	P7	TP_NEC_AMC
IPD	TEST	L8	TP_NEC_TEST
	NANDTEST	M10	TP_NEC_NANDTEST
	SRCLK	M9	TP_NEC_SRCLK
	SRDTA	N9	TP_NEC_SRDATA
IPD	SRMOD	P9	TP_NEC_SRMOD

ALL NETS TO FUNCTIONAL TEST PAGE

RC214 22 5% 1/16W MF-LF 402

122D5 3A7 =PPVIO_PCI_USB2

RC216 10K 5% 1/16W MF-LF 402
RC213 10K 5% 1/16W MF-LF 402

RPC203 47 5% 1/16W SM-LF
RPC203 47 5% 1/16W SM-LF
RPC203 47 5% 1/16W SM-LF

24C6 24B3 24A7 PCI_USB2_INT_L

RC250 47 5% 1/16W MF-LF 402

119A4 29D6 28D4 24B7 21C5 SYS_IO_RESET_L

RC251 47 5% 1/16W MF-LF 402

113A6 28C3 28B1 24B5 21C1 SYS_PME_L

120A3 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

RC215 4.7K 1% 1/16W MF-LF 402
RPC203 47 5% 1/16W SM-LF

PPC200 P4MM SM
PPC201 P4MM SM

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

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LAST_MODIFIED=Thu May 19 14:26:20 2005

DRAWING

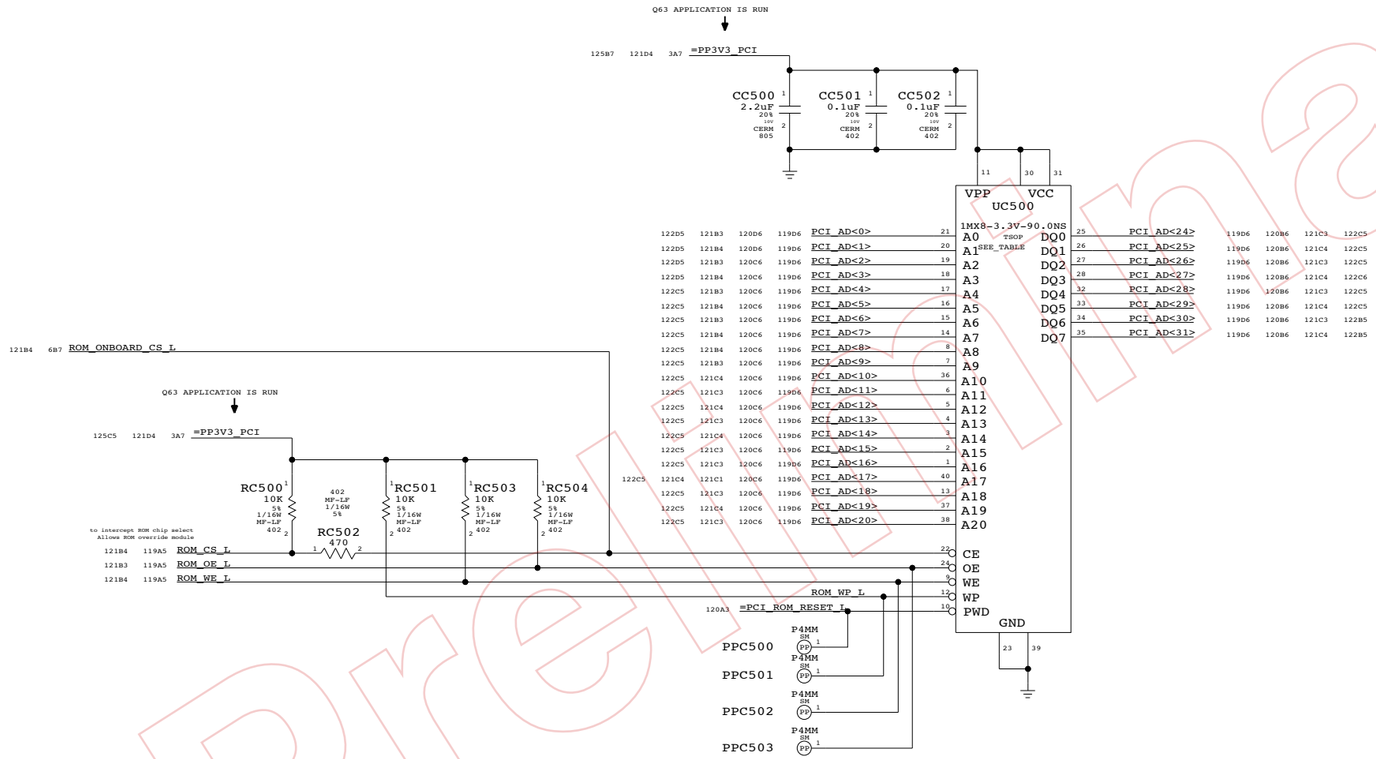
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT 125 OF 154

LAST_MODIFIED=Thu May 19 14:26:21 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
	SATA	SATA	SATA_TXD1	SATA_TXD_P1
	SATA	SATA	SATA_TXD1	SATA_TXD_N1
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
	SATA	SATA	SATA_TXD2	SATA_TXD_P2
	SATA	SATA	SATA_TXD2	SATA_TXD_N2
				UATA_DD<15..8>
				UATA_DD<7>
				UATA_DD<6..0>
				UATA_DA<2..0>
				UATA_CS0_L
				UATA_CS1_L
				UATA_HSTROBE
				UATA_STOP
				UATA_DMACK_L
	UATA_NETSPA			UATA_RESET_L
				UATA_DSTROBE
				UATA_DMARQ
				UATA_INTRQ
				UATA_DD_R<15..8>
				UATA_DD_R<7>
				UATA_DD_R<6..0>
				UATA_DA_R<2..0>
				UATA_CS0_L_R
				UATA_CS1_L_R
				UATA_DMACK_L_R
				UATA_HSTROBE_R
				UATA_STOP_R
				UATA_RESET_L_R

PLACE UATA TERMINATION RESISTORS NEAR JC901 CONNECTOR

RC706 33 5% 1/16W MF-LF 402: UATA_RESET_L_R → UATA_RESET_L
RC704 22 5% 1/16W MF-LF 402: UATA_DMACK_L_R → UATA_DMACK_L
RC702 22 5% 1/16W MF-LF 402: UATA_HSTROBE_R → UATA_HSTROBE
RC703 22 5% 1/16W MF-LF 402: UATA_STOP_R → UATA_STOP
RC700 33 5% 1/16W MF-LF 402: UATA_CS0_L_R → UATA_CS0_L
RC701 33 5% 1/16W MF-LF 402: UATA_CS1_L_R → UATA_CS1_L

DIOR- :HDMARDY- :HSTROBE >

DIOW- :STOP >

SPARE
RPC704 33 5% 1/16W SM-LF

RPC704 33 5% 1/16W SM-LF: UATA_DA_R<0> → UATA_DA<0>; UATA_DA_R<1> → UATA_DA<1>; UATA_DA_R<2> → UATA_DA<2>

RPC700 33 5% 1/16W SM-LF: UATA_DD_R<0> → UATA_DD<0>; UATA_DD_R<1> → UATA_DD<1>; UATA_DD_R<2> → UATA_DD<2>; UATA_DD_R<3> → UATA_DD<3>

RPC701 33 5% 1/16W SM-LF: UATA_DD_R<4> → UATA_DD<4>; UATA_DD_R<5> → UATA_DD<5>; UATA_DD_R<6> → UATA_DD<6>; UATA_DD_R<7> → UATA_DD<7>

RPC702 33 5% 1/16W SM-LF: UATA_DD_R<8> → UATA_DD<8>; UATA_DD_R<9> → UATA_DD<9>; UATA_DD_R<10> → UATA_DD<10>; UATA_DD_R<11> → UATA_DD<11>

RPC703 33 5% 1/16W SM-LF: UATA_DD_R<12> → UATA_DD<12>; UATA_DD_R<13> → UATA_DD<13>; UATA_DD_R<14> → UATA_DD<14>; UATA_DD_R<15> → UATA_DD<15>

RC705 10K 5% 1/16W MF-LF 402: 1 — 2

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A 0805 → PP1V2_SATA_VDD

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM

CC705 2.2UF 20% 6.3V CERM1 603
CC700 0.1UF 20% 10V CERM 402
CC701 0.1UF 20% 10V CERM 402
CC702 0.1UF 20% 10V CERM 402
CC703 0.1UF 20% 10V CERM 402
CC704 0.1UF 20% 10V CERM 402

XWCC00 (SM) → PP_1V2PWRONDISKSB_CC NO_TEST=YES → P4MM (SM, PP) PPCC00

SATA_VDD x 5

SATA_VDD: AB14, AB17, T14, W15, Y18

U2300 SHASTA V1.1 BGA-LF (5 OF 8) SEE_TABLE

UATA:
UD_IDEDD_0_H J6 UATA_DD_R<0>
UD_IDEDD_1_H H7 UATA_DD_R<1>
UD_IDEDD_2_H H6 UATA_DD_R<2>
UD_IDEDD_3_H K2 UATA_DD_R<3>
UD_IDEDD_4_H C1 UATA_DD_R<4>
UD_IDEDD_5_H C2 UATA_DD_R<5>
UD_IDEDD_6_H K3 UATA_DD_R<6>
UD_IDEDD_7_H G6 UATA_DD_R<7>
UD_IDEDD_8_H G5 UATA_DD_R<8>
UD_IDEDD_9_H D4 UATA_DD_R<9>
UD_IDEDD_10_H G7 UATA_DD_R<10>
UD_IDEDD_11_H F6 UATA_DD_R<11>
UD_IDEDD_12_H C3 UATA_DD_R<12>
UD_IDEDD_13_H F5 UATA_DD_R<13>
UD_IDEDD_14_H E5 UATA_DD_R<14>
UD_IDEDD_15_H D5 UATA_DD_R<15>
UD_IDEDA0_H E6 UATA_DA_R<0>
UD_IDEDA1_H C4 UATA_DA_R<1>
UD_IDEDA2_H D6 UATA_DA_R<2>
UD_IDECS1FX_L B3 UATA_CS0_L_R
UD_IDECS3FX_L B4 UATA_CS1_L_R
UD_IDEDMACK_L E8 UATA_DMACK_L_R
UD_IDERD_L E4 UATA_HSTROBE_R
UD_IDEWR_L D3 UATA_STOP_R
UD_IDERST_L E7 UATA_RESET_L_R

DSTROBE aka: IORDY/HDMARDY* HSTROBE aka: DIOR* STOP aka: DIOW*

129 127 UATA_DSTROBE F9 UD_IDECHRDY_H
129 127 UATA_DMARQ D7 UD_IDEDMARQ_H
129 127 UATA_INTRQ C5 UD_IDEINTRQ_H

SATA 0:
129 127 SATA_RXD_P1_C Y17 RXDP1
129 127 SATA_RXD_N1_C Y16 RXDN1
TXDP1 AA16 SATA_TXD_P1
TXDN1 AB16 SATA_TXD_N1

SATA 1:
129 127 SATA_RXD_P2_C AB15 RXDP2
129 127 SATA_RXD_N2_C AA15 RXDN2
TXDP2 Y15 SATA_TXD_P2
TXDN2 Y14 SATA_TXD_N2

SATA_GND: AA16, AA17, T15, W17

P4MM (SM, PP) PPCC01

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

4-29-05

AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
RPAK PINS WERE REMAPPED FOR BETTER ROUTING AROUND UATA CONNECTOR.

Shasta Disk

SYNC_MASTER=M33-MB SYNC_DATE=05/19/2005

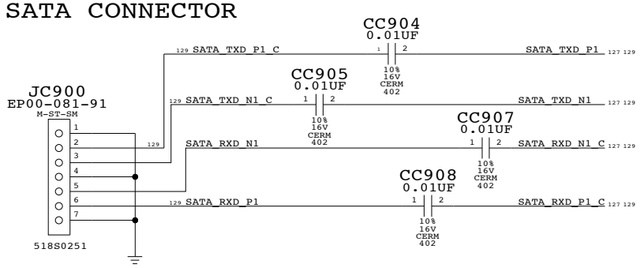
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 127 OF 154	

DRAWING

LAST_MODIFIED=Thu May 19 14:26:22 2005

SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

SATA_TXD_P2 — NC_SATA_TXD_P2 (MAKE_BASE=TRUE)
SATA_TXD_N2 — NC_SATA_TXD_N2 (MAKE_BASE=TRUE)
SATA_RXD_N2_C — NC_SATA_RXD_N2_C (MAKE_BASE=TRUE)
SATA_RXD_P2_C — NC_SATA_RXD_P2_C (MAKE_BASE=TRUE)

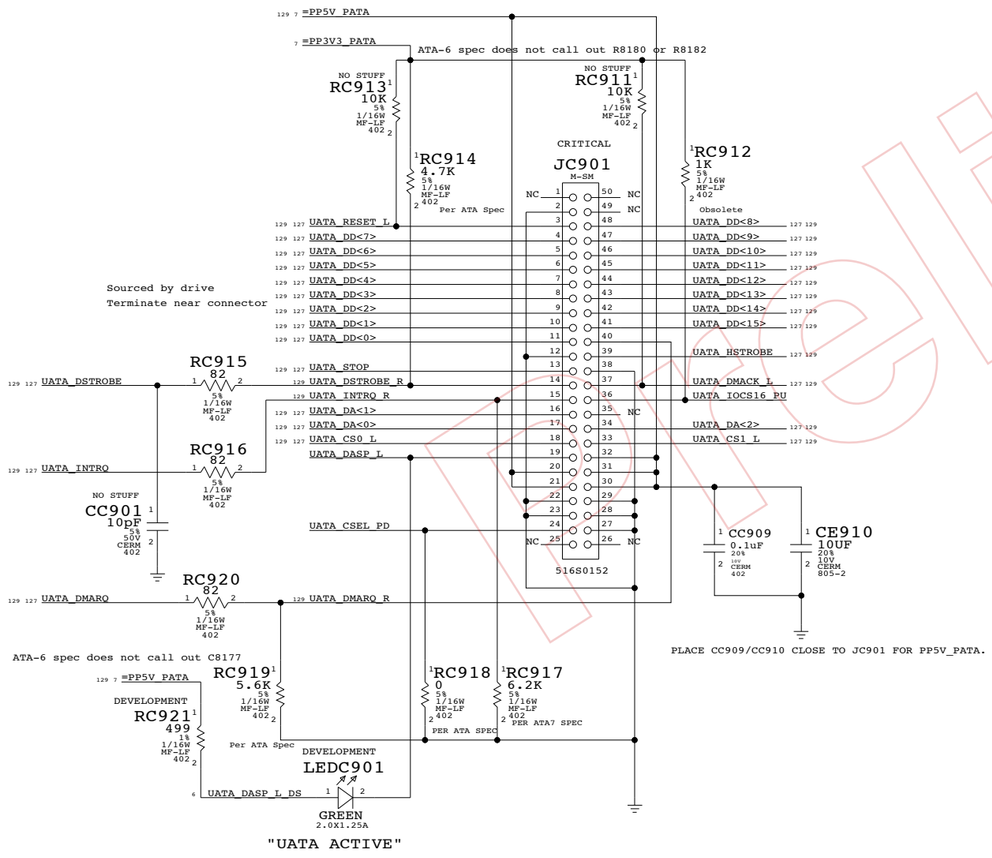
SATA & USB DIFF PAIR GND VIAS

ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA APPROXIMATELY 0.152MM AWAY FROM SIGNAL VIA.

GV901 HOLE-VIA-P5RP25
GV902 HOLE-VIA-P5RP25
GV903 HOLE-VIA-P5RP25
GV904 HOLE-VIA-P5RP25
GV905 HOLE-VIA-P5RP25
GV906 HOLE-VIA-P5RP25
GV907 HOLE-VIA-P5RP25
GV908 HOLE-VIA-P5RP25
GV909 HOLE-VIA-P5RP25
GV910 HOLE-VIA-P5RP25
GV911 HOLE-VIA-P5RP25
GV912 HOLE-VIA-P5RP25
GV913 HOLE-VIA-P5RP25
GV914 HOLE-VIA-P5RP25
GV915 HOLE-VIA-P5RP25
GV916 HOLE-VIA-P5RP25

M33 PATA CONNECTOR

4-12-05



UATA FROM RPAKS TO JC901

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM SHASTA U2300 TO RPAKS

UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA		
UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA		
UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA		
UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA		
UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA		
UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA		
UATA_STOP_R		UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA		
UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE		UATA_NETPH	UATA_NETSPA		
UATA_DMARQ		UATA_NETPH	UATA_NETSPA		
UATA_INTRQ		UATA_NETPH	UATA_NETSPA		

SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M33-MB SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 129 OF 154	

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT OF
NONE	130 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	

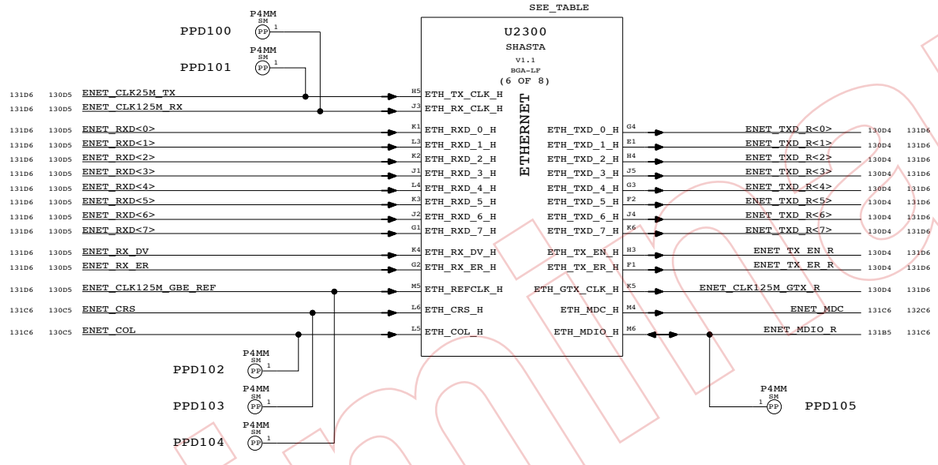
ENET_CLK25M_TX	130D5	131C6		
ENET_CLK125M_RX	130D5	131C6		
ENET_CLK125M_GBE_REF	130D5	131C6		
ENET_CLK125M_GTX	130B6	132C5		
ENET_CLK125M_GTX_R	130D4	131C3		
ENET_RXD_R<7..0>	130B4	130C4	132C3	
ENET_RX_DV_R	130B4	132C3		
ENET_RX_ER_R	130B4	132C3		
ENET_RXD<7..0>	130D5	131C6		
ENET_RX_DV	130D5	131C6		
ENET_RX_ER	130D5	131C6		
ENET_TXD_R<7..0>	130D4	131C3		
ENET_TX_EN_R	130D4	131C3		
ENET_TX_ER_R	130D4	131C3		
ENET_TXD<7..0>	130B6	130C6	132C5	
ENET_TX_EN	130B6	132C5		
ENET_TX_ER	130B6	132C5		
ENET_CRS_R	130B4	132C3		
ENET_COL_R	130B4	132C3		
ENET_CRS	130C5	131C6		
ENET_COL	130C5	131C6		
ENET_MDC	131C3	132C6		
ENET_MDIO	131B3	132C6		
ENET_MDIO_R	131B5	131C3		
R8405_1	131B4			
R8405_2	131B4			
R8407_2	131A4			

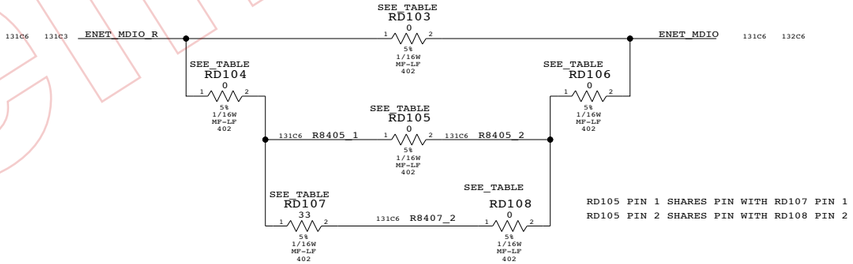
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 131 OF 154	

LAST_MODIFIED=Thu May 19 14:01:02 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
DEF	0.38mm SPACING	
DEF	0.38mm SPACING	
DEF	0.38mm SPACING	
ENET	ENET_MDI0	ENET_MDI_P<0>
ENET	ENET_MDI0	ENET_MDI_N<0>
ENET	ENET_MDI1	ENET_MDI_P<1>
ENET	ENET_MDI1	ENET_MDI_N<1>
ENET	ENET_MDI2	ENET_MDI_P<2>
ENET	ENET_MDI2	ENET_MDI_N<2>
ENET	ENET_MDI3	ENET_MDI_P<3>
ENET	ENET_MDI3	ENET_MDI_N<3>
DEF	0.38mm SPACING	
DEF	0.38mm SPACING	
DEF	0.38mm SPACING	

ENET_CLK125M_GBE_REF_R 130C4 132C3
ENET_CLK125M_RX_R 130C4 132C3
ENET_CLK25M_TX_R 130C4 132C3
ENET_MDI_P<0> 130B3 132B1
ENET_MDI_N<0> 130B3 132B1
ENET_MDI_P<1> 130B3 132B1
ENET_MDI_N<1> 130B3 132B1
ENET_MDI_P<2> 130B3 132B1
ENET_MDI_N<2> 130B3 132B1
ENET_MDI_P<3> 130B3 132B1
ENET_MDI_N<3> 130A3 132B1
VESTA_CLK25M_XTALI 132B5
VESTA_CLK25M_XTALO 132A4
VESTA_CLK25M_XTALO_R 132B5

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL
139D5 139D1 3B5 =PP2V5_ENETFW

LD200 FERR-EMI-600-OHM SM
PP2V5_VESTA_BIASVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD201 0.1uF 20% 10V CERM 402
LD201 FERR-EMI-600-OHM SM
PP2V5_VESTA_XTALVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD202 10UF 10% 6.3V X5R 805
CD203 0.001uF 20% 50V CERM 402

XWD200 SM OMIT 6B1 TP_VESTA_BIASVDD1 P4MM SM PPD239
XWD201 SM OMIT 6B1 TP_VESTA_XTALVDD1 P4MM SM PPD201
XWD202 SM OMIT 6B1 TP_VESTA_PLLVDD1 P4MM SM PPD238

PP1V2_VESTA_PLLVDD1 VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD204 0.001uF 20% 50V CERM 402
CD205 10UF 10% 6.3V X5R 805
LD202 FERR-EMI-600-OHM SM
Q63 APPLICATION IS ALL
=PP1V2_ENETFW 3B4 139C1 139D5
VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms

XTALVDD1 BIASVDD1 PLLVDD1

PPD200 P4MM SM
131D6 130B6 ENET_CLK125M_GTX → A4 GTXCLK IPD

VESTA ENET
U1701
VESTA-V1.3
FBGA-200-LF
2 OF 3

131D6 130C6	ENET_TXD<0>	B6	TXD[0] IPD
131D6 130C6	ENET_TXD<1>	C6	TXD[1] IPD
131D6 130C6	ENET_TXD<2>	C7	TXD[2] IPD
131D6 130C6	ENET_TXD<3>	D6	TXD[3] IPD
131D6 130C6	ENET_TXD<4>	E6	TXD[4] IPD
131D6 130C6	ENET_TXD<5>	C5	TXD[5] IPD
131D6 130B6	ENET_TXD<6>	B5	TXD[6] IPD
131D6 130B6	ENET_TXD<7>	A5	TXD[7] IPD
131D6 130B6	ENET_TX_EN	B4	TX_EN IPD
131D6 130B6	ENET_TX_ER	C4	TX_ER IPD
131C6 131C3	ENET_MDC	G1	MDC IPU
131C6 131B3	ENET_MDIO	G2	MDIO IPU
VESTA_ENET_LOWPWR		H5	LOWPWR IPD

IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP

TP_VESTA_PHYA<0>	L5	PHYA[0] IPD
TP_VESTA_PHYA<1>	L4	PHYA[1] IPD
TP_VESTA_PHYA<2>	L3	PHYA[2] IPD
TP_VESTA_PHYA<3>	L2	PHYA[3] IPD
TP_VESTA_PHYA<4>	L1	PHYA[4] IPD
TP_VESTA_EN_10B	K3	EN_10B IPD
TP_VESTA_RGMIIEN	B8	RGMIIEN IPD
TP_VESTA_FDX	C8	FDX IPU
TP_VESTA_F1000	K4	F1000 IPU
TP_VESTA_SPD0	K5	SPD0 IPD
TP_VESTA_MANMS	D9	MANMS IPD
TP_VESTA_HUB	A9	HUB IPD
TP_VESTA_ER	H3	ER IPD
TP_VESTA_TEST<0>	M4	TEST[0]
TP_VESTA_TEST<1>	M5	TEST[1]
TP_VESTA_TVCO	N3	TVCO
VESTA_CLK25M_XTALI	N2	XTALI
VESTA_CLK25M_XTALO_R	P2	XTALO

CLK125	D1	ENET_CLK125M_GBE_REF_R 130C4 132D6
TXC	A6	ENET_CLK25M_TX_R 130C4 132D6
RXC	C1	ENET_CLK25M_RX_R 130C4 132D6
RXD[0]	F4	ENET_RXD_R<0> 130C4 131D6
RXD[1]	F5	ENET_RXD_R<1> 130B4 131D6
RXD[2]	E5	ENET_RXD_R<2> 130B4 131D6
RXD[3]	E4	ENET_RXD_R<3> 130B4 131D6
RXD[4]	E3	ENET_RXD_R<4> 130B4 131D6
RXD[5]	D5	ENET_RXD_R<5> 130B4 131D6
RXD[6]	D4	ENET_RXD_R<6> 130B4 131D6
RXD[7]	D3	ENET_RXD_R<7> 130B4 131D6
RX_DV	D2	ENET_RX_DV_R 130B4 131D6
RX_ER	C2	ENET_RX_ER_R 130B4 131D6
COL	F3	ENET_COL_R 130B4 131C6
CRS	G3	ENET_CRS_R 130B4 131D6
RBC0	A3	TP_VESTA_RBC0
RBC1	B3	TP_VESTA_RBC1

TRD+[0]	R4	ENET_MDI_P<0> 130B3 132D6
TRD-[0]	R5	ENET_MDI_N<0> 130B3 132D6
TRD+[1]	R7	ENET_MDI_P<1> 130B3 132D6
TRD-[1]	R6	ENET_MDI_N<1> 130B3 132D6
TRD+[2]	R8	ENET_MDI_P<2> 130B3 132D6
TRD-[2]	R9	ENET_MDI_N<2> 130B3 132D6
TRD+[3]	R11	ENET_MDI_P<3> 130B3 132D6
TRD-[3]	R10	ENET_MDI_N<3> 130A3 132D6

INTR*/ENERGYDET D10 ENET_ENERGYDET 24A2 24B3
TERMINATION OFF PAGE

IPU SLAVE*/AN_EN	C10	TP_VESTA_AN_EN
QUALITY*/TXC_RXC_DELAY	A8	TP_VESTA_TXC_RXC_DELAY
IPD LINK1*	A10	TP_VESTA_LINK1_L
IPD LINK2*	B11	TP_VESTA_LINK2_L
IPD FDXLED*	B10	TP_VESTA_FDXLED_L
IPU XMTLED*	B12	TP_VESTA_XMTLED_L
IPU ACTLED*	A11	TP_VESTA_ACTLED_L
RDAC1	R1	VESTA_RDAC1_PD

Q63 APPLICATION IS ALL
140B4 139D1 139C6 139A6 139A1 17D7 17B8 17B1 17A6 3B6 =PP3V3_ENETFW
RD204 1K 1% 1/16W MF-LF 402
QD200 2N7002DW-X-F SOT-363
132C6 3A3 =PP3V3_ENET
CD206 1UF 10% 6.3V CERM 402
17A6 VESTA_RESET_H
QD200 2N7002DW-X-F SOT-363

132B7 3A3 =PP3V3_ENET
RD250 1.5K 5% 1/16W MF-LF 402
VESTA_ENET_LOWPWR

Put crystal circuit close to PHY
RD209 0 5% 1/16W MF-LF 402
CRITICAL
YD200 25.0000M SM-2
VESTA_CLK25M_XTALO 132D6
CD218 33pF 5% 50V CERM 402
CD219 33pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 20PF

XTALGND BIASGND PLLGND1
RD213 1.24K 1% 1/16W MF-LF 402

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

LAST_MODIFIED=Thu May 19 14:26:25 2005

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07
SCALE: NONE	SHT 132 OF 154	

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

P292	ENET	ENET_MDI_P<0>	132 136
P296	ENET	ENET_MDI_N<0>	132 136
P297	ENET	ENET_MDI_P<1>	132 136
P298	ENET	ENET_MDI_N<1>	132 136
P299	ENET	ENET_MDI_P<2>	132 136
P300	ENET	ENET_MDI_N<2>	132 136
P301	ENET	ENET_MDI_P<3>	132 136
P302	ENET	ENET_MDI_N<3>	132 136

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD601 330 5% 1/10W MF-LF 603
LED8700_P
DEVELOPMENT
LEDD600 GREEN 2.0X1.25A
132 TP_VESTA_XMTLED_L — VESTA_XMTLED_L MAKE_BASE=TRUE

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>
RD604 49.9 1% 1/16W MF-LF 402
RD605 49.9 1% 1/16W MF-LF 402
ENET_MDI0
136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>
CD606 0.01UF 20% 16V CERM 402
RD606 49.9 1% 1/16W MF-LF 402
RD607 49.9 1% 1/16W MF-LF 402
ENET_MDI1
136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>
RD608 49.9 1% 1/16W MF-LF 402
RD609 49.9 1% 1/16W MF-LF 402
CD607 0.01UF 20% 16V CERM 402
ENET_MDI2
136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>
CD608 0.01UF 20% 16V CERM 402
RD610 49.9 1% 1/16W MF-LF 402
RD611 49.9 1% 1/16W MF-LF 402
ENET_MDI3
CD609 0.01UF 20% 16V CERM 402

LD600
FERR-EMI-600-OHM
SM
7 =PP2V5_ENET
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.20mm
MIN_NECK_WIDTH=0.138mm
VOLTAGE=2.5V
CD600 0.1UF 20% 10V CERM 402
CD601 0.1UF 20% 10V CERM 402
7 GND_CHASSIS_RJ45
CD604 0.001UF 10% 50V CERM 402
CD605 0.001UF 10% 50V CERM 402

(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
RJ45 CHIP SIDE
1CT:1CT
75 OHM
SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45 CABLE SIDE
SHIELD
1000PF, 2000V

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD603 330 5% 1/10W MF-LF 603
LED8701_P
DEVELOPMENT
LEDD601 GREEN 2.0X1.25A
132 TP_VESTA_ACTLED_L — VESTA_ACTLED_L MAKE_BASE=TRUE

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE-VIA
ZHD691 HOLE-VIA
ZHD692 HOLE-VIA
ZHD693 HOLE-VIA

ETHERNET CONNECTOR

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	0.38mm_SPACING	
	0.38mm_SPACING	
	0.38mm_SPACING	

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

FW_DATA<7..0> 138B4 138C4 139B7 139C7
FW_CTL_S<1..0> 138B4 139D6
FW_CTL<1..0> 138B2 139A4 139A6 139B7 139D6
FW_DATA_R<7..0> 139B5 139C5
FW_CTL_R<1..0> 139B5 139D6
FW_LPS 138B4 139B5
FW_LREQ 138B4 139B5
FW_PINT 138B5 139C3
FW_CLK98M_LCLK 138B2 139C5
FW_CLK98M_PCLK 138B5 139C1
FW_CLK98M_LCLK_R 138B4

119C3 24D5 23C2 23B2 3C1 =PP2V5_PWRON_SB

CD800 0.1uF 20% 10V CERM 402
CD801 0.1uF 20% 10V CERM 402
CD802 0.1uF 20% 10V CERM 402

FIREWIRE
FWVDDP
U2300
SHASTA
V1.1
BGA-LF
SEE_TABLE
(7 OF 8)

PHY_DATA_0_H	N4	FW_DATA<0>	138D6	139C7
PHY_DATA_1_H	P5	FW_DATA<1>	138D6	139C7
PHY_DATA_2_H	N1	FW_DATA<2>	138D6	139C7
PHY_DATA_3_H	M7	FW_DATA<3>	138D6	139B7
PHY_DATA_4_H	N6	FW_DATA<4>	138D6	139B7
PHY_DATA_5_H	L1	FW_DATA<5>	138D6	139B7
PHY_DATA_6_H	M3	FW_DATA<6>	138D6	139B7
PHY_DATA_7_H	L2	FW_DATA<7>	138D6	139B7
PHY_CTL_0_H	N2	139D6 138D6 FW_CTL_S<0>		
PHY_CTL_1_H	N3	139D6 138D6 FW_CTL_S<1>		
PHY_LPS_H	P6	FW_LPS	138D6	139B5
PHY_LREQ_H	P1	FW_LREQ	138D6	139B5
PHY_SCLK_H	P2	139C1 138D6 FW_CLK98M_PCLK		
PHY_PINT_L	P3	139C3 138D6 FW_PINT		
PHY_LCLK_H	R1	138D6 FW_CLK98M_LCLK_R		
PHY_LINKON_L	N7	FW_LINKON	139C3	

RD801 0 5% 1/16W MF-LF 402: FW_CTL<0> 138D6 139A4 139A6 139B7 139D6
RD802 0 5% 1/16W MF-LF 402: FW_CTL<1> 138D6 139A4 139A6 139B7 139D6
RD800 22 5% 1/16W MF-LF 402: FW_CLK98M_LCLK 138D6 139C5

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07
SCALE: NONE	SHT 138 OF 154	

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DRAWING:

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
(PROPAGATED BY LINK PAGE)		0.38mm SPACING	
	FW	FW	FW_TPA0
	FW	FW	FW_TPA0
	FW	FW	FW_TPB0
	FW	FW	FW_TPB0
	FW	FW	FW_TPA1
	FW	FW	FW_TPA1
	FW	FW	FW_TPB1
	FW	FW	FW_TPB1
4MM/SPACING TO ROUTE ON LAYER 4	FW	FW	FW_TPA2
	FW	FW	FW_TPA2
	FW	FW	FW_TPB2
	FW	FW	FW_TPB2
		0.38mm SPACING	
		0.38mm SPACING	
		0.38mm SPACING	
5mil	FW_CTL		
5mil	FW_CTL		
5mil	FW_CTL		

FW_CLK98M_PCLK_R	139C3
FW_TPA_P<0>	139B2 140A5 140B8
FW_TPA_N<0>	139B2 140A5 140B8
FW_TPB_P<0>	139B2 140A5 140B8
FW_TPB_N<0>	139B2 140A5 140B8
FW_TPA_P<1>	139B2 140A5 140B8
FW_TPA_N<1>	139B2 140A5 140A8
FW_TPB_P<1>	139B2 140A5 140A8
FW_TPB_N<1>	139B2 140A5 140A8
FW_TPA_P<2>	139B2 140A5 140B8
FW_TPA_N<2>	139B2 140A5 140B8
FW_TPB_P<2>	139B2 140A5 140B8
FW_TPB_N<2>	139B2 140A5 140B8
VESTA_CLK24M_XTALI	139B5
VESTA_CLK24M_XTALO	139A4
VESTA_CLK24M_XTALO_R	139B5
FW_CTL_S<1..0>	138B4 138D6
FW_CTL<1..0>	138B2 138D6 139A4 139A6 139B7
FW_CTL_R<1..0>	138D6 139B5

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta.
  See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta.
  See straps table for more information.

Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

ESDET[0]
1=PORTS 1 AND 2 DS ONLY
0=PARTS 1 AND 2 BI-LINGUAL
ESDET[1]
1=PORT 1 PRESENT
0=PORT 1 NOT PRESENT
ESDET[2]
1=PORT 2 PRESENT
0=PORT 2 NOT PRESENT

CRYSTAL LOAD CAPACITANCE IS 12PF

Vesta FireWire PHY

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 139 OF 154	

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DRAWING:

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	140
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	140
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	140
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	140
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	140
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	140
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	140
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	140

7 =PP12V_ALL_FW

8 WATTS MAX
12 VOLTS

RE056 1.3 20% 1W FF 2512 — PP12V_FW (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V, MAKE_BASE=TRUE)

I443 = =PPFW_PHY 139 — TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XKG SMC

FW_VP_R (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, MAKE_BASE=TRUE, VOLTAGE=24V)

CRITICAL
RE002 1.3 20% 1W FF 2512

FW_VP (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=24V)

FE002 0.75AMP-13.2V MINISMD

PPFW_PORT0_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

FE000 1.5AMP-33V SM

PPFW_PORT1_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V) 140

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

CE009 0.1UF 10% 50V X7R 603-1

FW_VP MAX IS 24V

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
139 FW_TPBIAS<1>
139 FW_TPBIAS<0>
VOLTAGE=1.86V

CE050 1uF 10% 6.3V CERM 402
CE060 1uF 10% 6.3V CERM 402

RE050 56.2 1% 1/16W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/16W MF-LF 402

139 FW_TPA_P<0> — FW_PORT0_TPA_P 140
139 FW_TPA_N<0> — FW_PORT0_TPA_N 140
139 FW_TPB_P<0> — FW_PORT0_TPB_P 140
139 FW_TPB_N<0> — FW_PORT0_TPB_N 140
MAKE_BASE=TRUE

139 FW_TPA_P<1> — FW_PORT1_TPA_P 140
139 FW_TPA_N<1> — FW_PORT1_TPA_N 140
139 FW_TPB_P<1> — FW_PORT1_TPB_P 140
139 FW_TPB_N<1> — FW_PORT1_TPB_N 140
MAKE_BASE=TRUE

RE052 56.2 1% 1/16W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/16W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V
FW_TPA_C<1> VOLTAGE=0V

RE054 4.99K 1% 1/16W MF-LF 402
CE054 270pF 5% 25V CERM 402
CE064 270pF 5% 25V CERM 402
RE064 4.99K 1% 1/16W MF-LF 402

3rd TPA/TPB pair unused

139 FW_TPBIAS<2> — NC_FW_TPBIAS2
139 FW_TPA_P<2> — NC_FW_TPA_P2
139 FW_TPA_N<2> — NC_FW_TPA_N2
139 FW_TPB_P<2> — FW_TPB2_RD
139 FW_TPB_N<2> —
MAKE_BASE=TRUE, NO_TEST=YES

RE070 1K 5% 1/16W MF-LF 402

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

7 =PP3V3_FW — RE090 215 1% 1/16W MF-LF 402 — PP3V3_FW_ESD_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — LE090 400-OHM-EMI SM-1 — PP3V3_FW_ESD (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) 140

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD

DPE010 BAV99DW-X-F SOT-363
DPE010 BAV99DW-X-F SOT-363

CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402

140 GND_CHASSIS_FIREWIRE

FLE010 120-OHM 2012 SM_YBK-1

140 FW_PORT0_TPA_P
140 FW_PORT0_TPA_N
FLE011 120-OHM 2012 SM_YBK-1
140 FW_PORT0_TPB_P
140 FW_PORT0_TPB_N

140 PP3V3_FW_ESD

DPE011 BAV99DW-X-F SOT-363
DPE011 BAV99DW-X-F SOT-363

CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

140 GND_CHASSIS_FIREWIRE

LE010 FERR-160-OHM 1206-LF

PORT 0
1394A
OMIT

JE000 UF01613-M33-4F F-ST-TH

140 FW_PORT0_TPA_P_FL — TPO (TPA+)
140 FW_PORT0_TPA_N_FL — TPO# (TPA-)
140 FW_PORT0_TPB_P_FL — TPI (TPB+)
140 FW_PORT0_TPB_N_FL — TPI# (TPB-)
PPFW_PORT0_VP_FL — VP
VGND

VOLTAGE=24V (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm)

FW_VP MAX IS 24V
CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01uF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE 7 140

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD

DPE020 BAV99DW-X-F SOT-363
DPE020 BAV99DW-X-F SOT-363

CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

FLE020 120-OHM 2012 SM_YBK-1

140 FW_PORT1_TPA_P
140 FW_PORT1_TPA_N
FLE021 120-OHM 2012 SM_YBK-1
140 FW_PORT1_TPB_P
140 FW_PORT1_TPB_N

140 PP3V3_FW_ESD

DPE021 BAV99DW-X-F SOT-363
DPE021 BAV99DW-X-F SOT-363

CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

140 GND_CHASSIS_FIREWIRE

PPFW_PORT1_VP 140

LE020 FERR-160-OHM 1206-LF

PORT 1
1394A
OMIT

JE001 UF01613-M33-4F F-ST-TH

140 FW_PORT1_TPA_P_FL — TPO (TPA+)
140 FW_PORT1_TPA_N_FL — TPO# (TPA-)
140 FW_PORT1_TPB_P_FL — TPI (TPB+)
140 FW_PORT1_TPB_N_FL — TPI# (TPB-)
PPFW_PORT1_VP_FL — VP
VGND

MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01uF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE 7 140

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 140 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_2
	USB2	USB2	USB2_3
	USB2	USB2	USB2_3
	USB2	USB2	USB2_4
	USB2	USB2	USB2_4
	0.38mm SPACING		
	0.38mm SPACING		
	0.38mm SPACING		

USB2_P<0> 142C2 143D1 143D8
USB2_N<0> 142C2 143D1 143D8
USB2_P<1> 6B7 142C2 143C8 143D1
USB2_N<1> 6B7 142C2 143C8 143D1
USB2_P<2> 142B2 143B8 143D1
USB2_N<2> 142B2 143B8 143D1
USB2_P<3> 142B2 143A8 143D1
USB2_N<3> 142B2 143A8 143D1
USB2_P<4> 142A2 143A4 143D1
USB2_N<4> 142A2 143A4 143D1
NEC_CLK30M_XT1 142A5
NEC_CLK30M_XT2 142A5
NEC_CLK30M_XT2_R 142A5

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

142C6 142B6 3A3 =PP3V3_PWRON_USB
LE235 FERR-EMI-100-OHM SM
RE235 4.7 5% 1/10W MF-LF 603
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
CE235 10UF 10% 6.3V X5R 805
CE236 0.1uF 20% 10V CERM 402
CE237 0.1uF 20% 10V CERM 402
XWE200 OMIT SM
TP_NEC_AVDD
P4MM SM PP
PPE2000
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
GND_NEC_AVSS_R 6B1 142A2

CE220 10UF 10% 6.3V X5R 805
CE221 CE222 CE223 CE224 CE225 CE226 CE227 CE228 CE229 CE230 0.1uF 20% 10V CERM 402

P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 VDD
H10 H12 AVDD

UC200
NEC_UPD720101_USB2
FBGA-LF

RSDM1 M14 USB_NEC_N<0>
DM1 M13 (USB2_N<0>)
DP1 L14 (USB2_P<0>)
RSDP1 K13 USB_NEC_P<0>
RE200 36 1% 1/16W MF-LF 402
RE201 36 1% 1/16W MF-LF 402
USB2_N<0> 142D6 143D1 143D8
USB2_P<0> 142D6 143D1 143D8

P4MM SM PP
PPE2002
RSDM2 K14 USB_NEC_N<1>
DM2 K12 (USB2_N<1>)
DP2 J14 (USB2_P<1>)
RSDP2 J12 USB_NEC_P<1>
RE202 36 1% 1/16W MF-LF 402
RE203 36 1% 1/16W MF-LF 402
USB2_N<1> 6B7 142D6 143C8 143D1
USB2_P<1> 6B7 142D6 143C8 143D1

P4MM SM PP
PPE2001
RSDM3 H11 USB_NEC_N<2>
DM3 G11 (USB2_N<2>)
DP3 G13 (USB2_P<2>)
RSDP3 G14 USB_NEC_P<2>
RE204 36 1% 1/16W MF-LF 402
RE205 36 1% 1/16W MF-LF 402
USB2_N<2> 142D6 143B8 143D1
USB2_P<2> 142D6 143B8 143D1
40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

RSDM4 F12 USB_NEC_N<3>
DM4 F14 (USB2_N<3>)
DP4 E12 (USB2_P<3>)
RSDP4 E14 USB_NEC_P<3>
RE206 36 1% 1/16W MF-LF 402
RE207 36 1% 1/16W MF-LF 402
USB2_N<3> 142D6 143A8 143D1
USB2_P<3> 142D6 143A8 143D1

RSDM5 E13 USB_NEC_N<4>
DM5 D14 (USB2_N<4>)
DP5 C13 (USB2_P<4>)
RSDP5 C14 USB_NEC_P<4>
RE208 36 1% 1/16W MF-LF 402
RE209 36 1% 1/16W MF-LF 402
USB2_N<4> 142D6 143A4 143D1
USB2_P<4> 142D6 143A4 143D1
BLUTOOTH CONNECTOR,(PORT #4)

142D5 142B6 3A3 =PP3V3_PWRON_USB
RE210 33K 5% 1/16W MF-LF 402
RPE210 10K 5% 1/16W SM-LF

143B4 USB2_OC<0> (USB2_OC<0>) B12 OCI1
143B4 USB2_OC<1> (USB2_OC<1>) B11 OCI2
143B4 USB2_OC<2> (USB2_OC<2>) B10 OCI3
143B4 USB2_OC<3> (USB2_OC<3>) A10 OCI4
121B6 USB2_OC<4> (USB2_OC<4>) B9 OCI5

143B2 USB2_PWREN<0> C12 PPON1
143B2 USB2_PWREN<1> A11 PPON2
143B2 USB2_PWREN<2> C11 PPON3
143B2 USB2_PWREN<3> C10 PPON4
143B2 USB2_PWREN<4> A9 PPON5

142D5 142C6 3A3 =PP3V3_PWRON_USB
RE240 1.5K 5% 1/16W MF-LF 402
RE241 1.5K 5% 1/16W MF-LF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

142D6 NEC_CLK30M_XT1 L9 XT1/SCLK
142D6 NEC_CLK30M_XT2_R P8 XT2
RE245 100 1% 1/16W MF-LF 402
CRYSTAL YE245 30.0000M SM-1
NEC_CLK30M_XT2
CE245 22pF 5% 50V CERM 402
CE246 22pF 5% 50V CERM 402
SPEC SHOWS LOAD CAPACITANCE OF 16PF

142D6 VSS
B1 H1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 E8
XWE201 SM OMIT
P13 M12 AVSS AVSS(R) M11
Tie to GND at ball M11

RREF P11 NEC_RREF_PD
RE238 9.09K 1% 1/16W MF-LF 402
MINIMIZE TRACE LENGTH TO PINS
GND_NEC_AVSS_R 6B1 142D3
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

U2300
SHASTA
V1.1
BGA-LF
(8 OF 8)

NC0	P7	TP_SB<0>
NC1	P8	TP_SB<1>
NC2	R3	TP_SB<2>
NC3	R4	TP_SB<3>
NC4	R5	TP_SB<4>
NC5	R6	TP_SB<5>
NC6	R7	TP_SB<6>
NC7	R8	TP_SB<7>
NC8	T1	TP_SB<8>
NC9	T2	TP_SB<9>
NC10	T3	TP_SB<10>
NC11	T4	TP_SB<11>
NC12	T5	TP_SB<12>
NC13	T6	TP_SB<13>
NC14	T7	TP_SB<14>
NC15	T8	TP_SB<15>
NC16	U1	TP_SB<16>
NC17	U2	TP_SB<17>
NC18	U3	TP_SB<18>
NC19	U4	TP_SB<19>
NC20	U5	TP_SB<20>
NC21	U6	TP_SB<21>
NC22	V1	TP_SB<22>
NC23	V2	TP_SB<23>
NC24	V3	TP_SB<24>
NC25	V4	TP_SB<25>
NC26	W1	TP_SB<26>
NC27	W3	TP_SB<27>
NC28	Y1	TP_SB<28>
NC29	Y3	TP_SB<29>

USB Host Interfaces

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07

SCALE: NONE SHT 142 OF 154

DRAWING

LAST_MODIFIED=Thu May 19 14:26:30 2005

External USB Ports

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
142 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
142 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
142 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
142 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0247	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0250	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_P_F	USB2	USB2_PORT1_P_F 143
	USB2	USB2_PORT1_N_F	USB2	USB2_PORT1_N_F 143
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F 143
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F 143
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F 143
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F 143
E608	USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2>
E609	USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2>
E610	USB2	USB2_BNDI_F	USB2	USB2_P_L<3>
E611	USB2	USB2_BNDI_F	USB2	USB2_N_L<3>

7 =PP5V_PWRON_USB
UE300 TPS2024 SOI
IN_0 OUT_0
IN_1 OUT_1
OUT_2
EN* OC*
GND
142 USB2_OC<0> — USB_OC MAKE_BASE=TRUE
142 USB2_OC<1>
142 USB2_OC<2>

96 PP5V_USB2
LE310 FERR-250-OHM SM
NOSTUFF CE310 150UF 20% 6.3V POLY SMD2
RE336 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_USB_PORT1
CE312 0.01uF 20% 16V CERM 402
CE313 0.01uF 20% 16V CERM 402
PP5V_USB2_PORT1_F
OMIT JE310 UB01123M23-4F F-ST-TH
VDD D- D+ GND
PORT 1
514-0247
GND_CHASSIS_USB 7 143

LE312 120-OHM 2012 SYN_VSB-1
142 USB2_N<0> — USB2_PORT1_N MAKE_BASE=TRUE
142 USB2_P<0> — USB2_PORT1_P MAKE_BASE=TRUE
143 USB2_PORT1_N_F
143 USB2_PORT1_P_F
NOSTUFF RE312 0 402
NOSTUFF RE313 0 402
RE310 15K 5% 1/16W MF-LF 402
RE311 15K 5% 1/16W MF-LF 402

LE320 FERR-250-OHM SM
NOSTUFF CE320 330UF 20% 6.3V POLY SMD
RE335 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_USB_PORT2
CE322 0.01uF 20% 16V CERM 402
CE323 0.01uF 20% 16V CERM 402
PP5V_USB2_PORT2_F
OMIT JE320 UB01123M23-4F F-ST-TH
VDD D- D+ GND
PORT 2
514-0247
GND_CHASSIS_USB 7 143

LE322 120-OHM 2012 SYN_VSB-1
142 USB2_N<1> — USB2_PORT2_N MAKE_BASE=TRUE
142 USB2_P<1> — USB2_PORT2_P MAKE_BASE=TRUE
143 USB2_PORT2_N_F
143 USB2_PORT2_P_F
NOSTUFF RE322 0 402
NOSTUFF RE323 0 402
RE320 15K 5% 1/16W MF-LF 402
RE321 15K 5% 1/16W MF-LF 402

LE330 FERR-250-OHM SM
PP5V_USB2_PORT3_F
RE334 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM
GND_USB_PORT3
CE332 0.01uF 20% 16V CERM 402
CE333 0.01uF 20% 16V CERM 402
OMIT JE330 UB01123M23-4F F-ST-TH
VDD D- D+ GND
PORT 3
514-0247
GND_CHASSIS_USB 7 143

LE332 120-OHM 2012 SYN_VSB-1
142 USB2_N<2> — USB2_PORT3_N MAKE_BASE=TRUE
142 USB2_P<2> — USB2_PORT3_P MAKE_BASE=TRUE
143 USB2_PORT3_N_F
143 USB2_PORT3_P_F
NOSTUFF RE332 0 402
NOSTUFF RE333 0 402
RE330 15K 5% 1/16W MF-LF 402
RE331 15K 5% 1/16W MF-LF 402

FE301 0.75AMP-13.2V MINISMD 740S0509
7 =PP5V_PWRON_BNDI
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
PP5V_USB_BNDI_LE340
LE340 FERR-250-OHM SM
PP5V_PWRON_BNDI 143
RE346 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_BNDI 143
CE342 0.01uF 20% 16V CERM 402
CE343 0.01uF 20% 16V CERM 402
CE344 10UF 20% 10V CERM 805-2
143 7 GND_CHASSIS_BNDI

FHB CONNECTOR
518S0275
JE350 53261-1471 M-RT-SM
153 AUD_MIC_IN_P_CONN 1
153 GND_AUDIO_MIC_CONN 2
153 AUD_MIC_IN_N_CONN 3
143 7 GND_CHASSIS_BNDI 4
5
143 7 GND_CHASSIS_BNDI 6
USB2_HUB_P_L<2> 7
USB2_HUB_N_L<2> 8
9
143 GND_BNDI 10
USB2_P_L<3> 11
USB2_N_L<3> 12
24 SB_GPIO14 13
143 PP5V_PWRON_BNDI 14
15
16

USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEEDED HERE
144 USB2_HUB_P<2> — NOSTUFF RE343 0 402 — LE342 120-OHM 2012
144 USB2_HUB_N<2> — NOSTUFF RE342 0 402
NOSTUFF RE354 0 402 — LE352 120-OHM 2012
142 USB2_P<3>
142 USB2_N<3>
RE350 15K 5% 1/16W MF-LF 402
RE351 15K 5% 1/16W MF-LF 402
NOSTUFF RE355 0 402

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

RE356 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_BNDI 143
CE352 0.01uF 20% 16V CERM 402
143 7 GND_CHASSIS_BNDI

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT
142 USB2_P<4> — MAKE_BASE=TRUE — USB2_HUB_P<0> 144
142 USB2_N<4> — MAKE_BASE=TRUE — USB2_HUB_N<0> 144
RE352 15K 5% 1/16W MF-LF 402
RE353 15K 5% 1/16W MF-LF 402

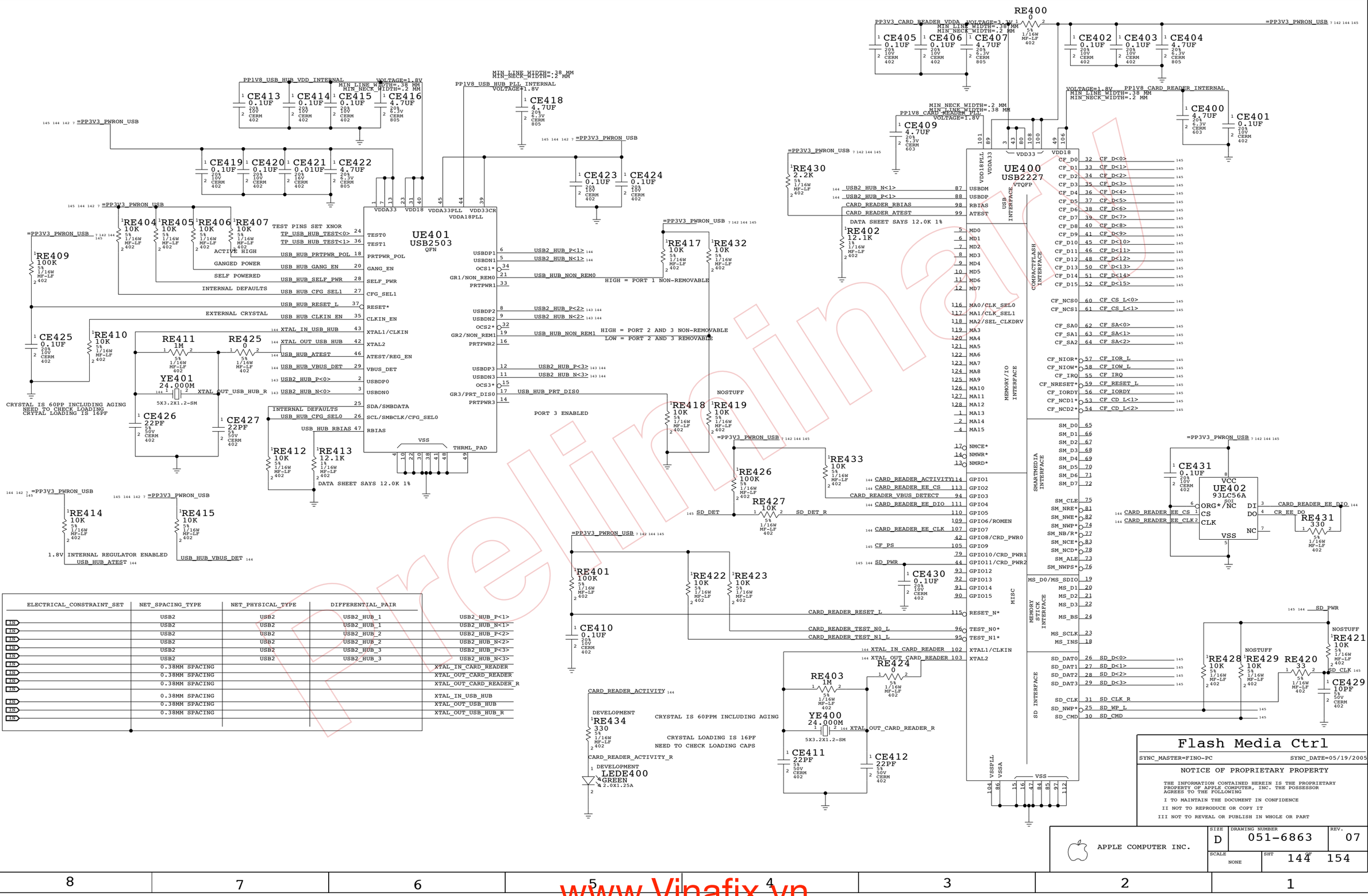
SENDS USB HUB PORT 3 TO BLUETOOTH MODULE
121 USB_BT_P — MAKE_BASE=TRUE — USB2_HUB_P<3> 144
121 USB_BT_N — MAKE_BASE=TRUE — USB2_HUB_N<3> 144
USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEED HERE

USB Device Interfaces

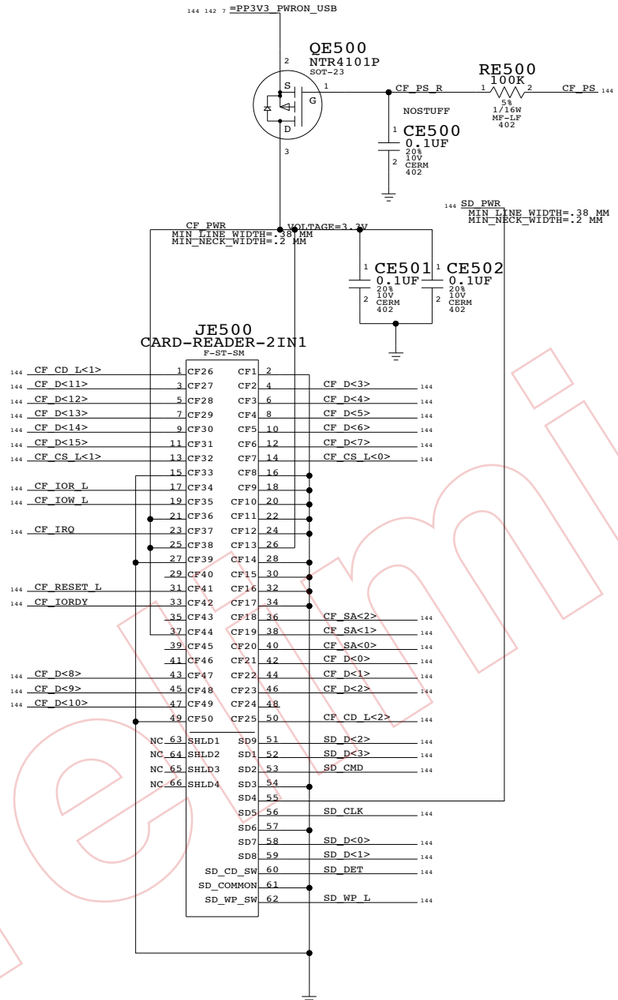
SYNC_MASTER=FINO-MB SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 143 OF 154	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
	0.38MM SPACING			XTAL_IN_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER_R
	0.38MM SPACING			XTAL_IN_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB_R



Flash Connector

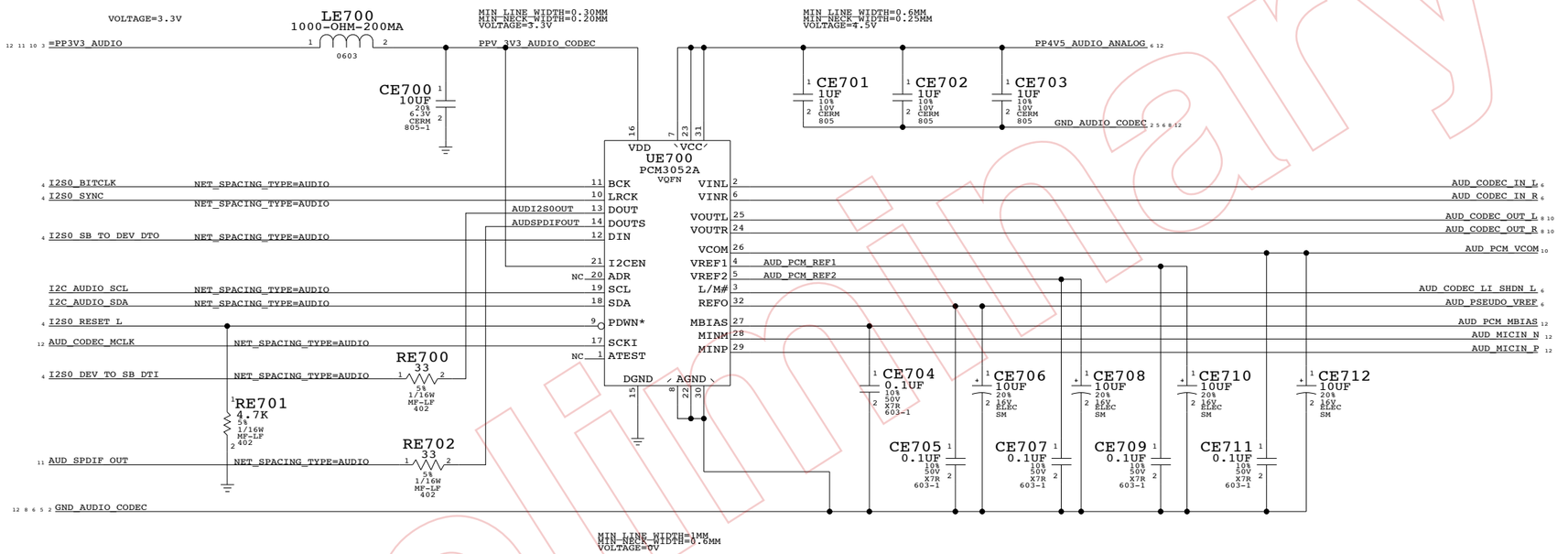
SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT
NONE	145 OF 154

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

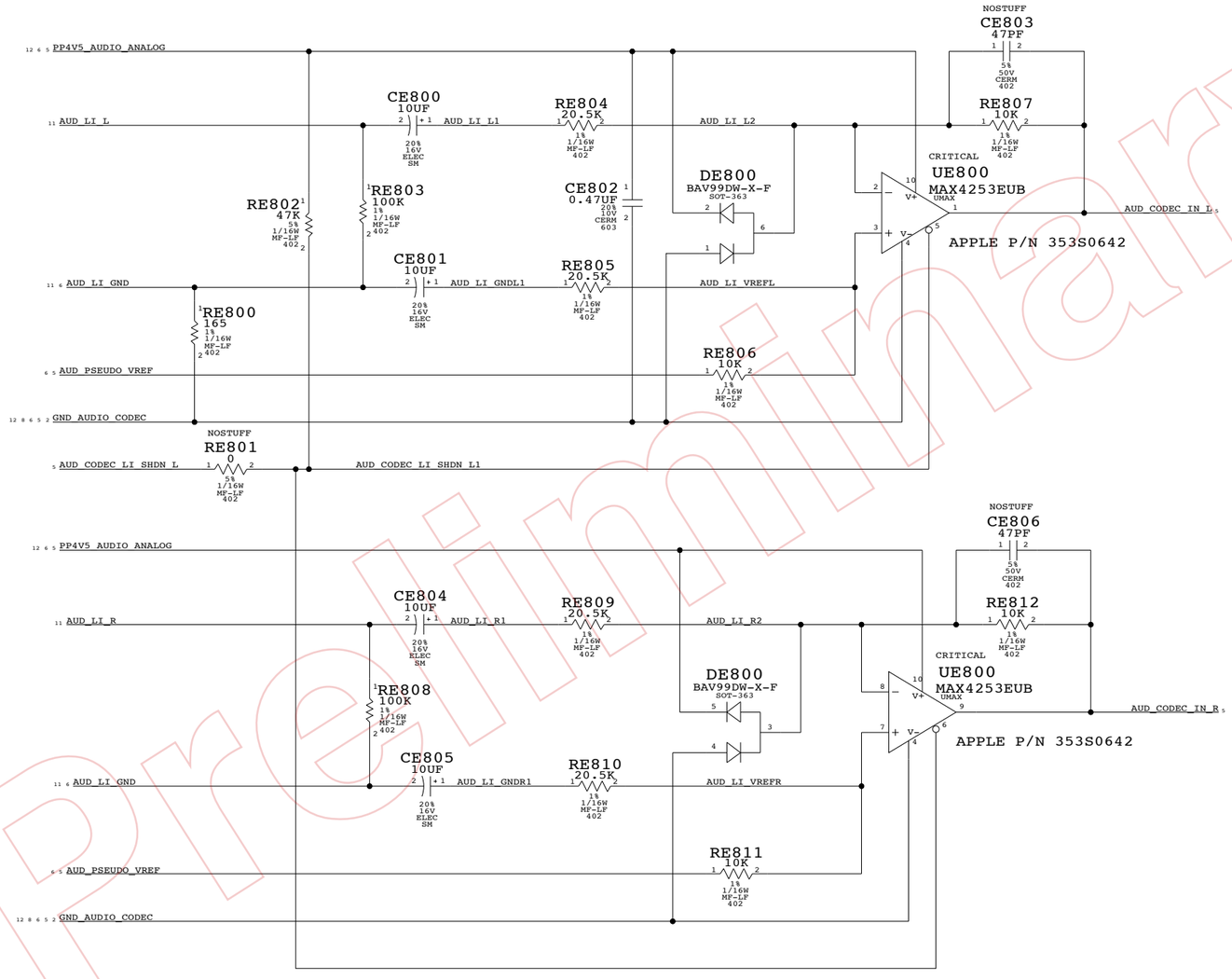
SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 147 OF 154	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

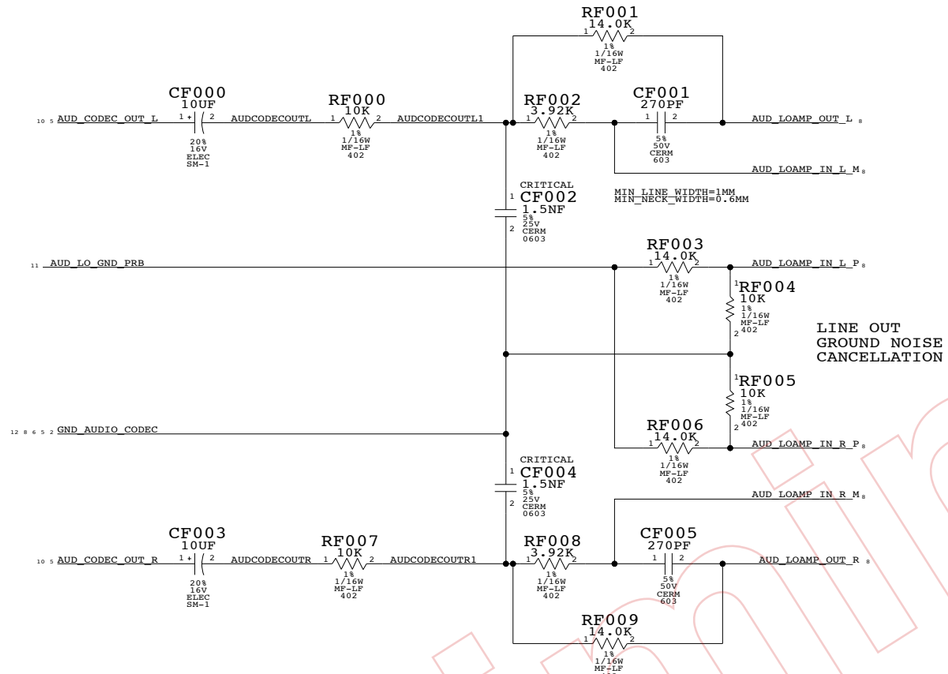
SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 148 OF 154	

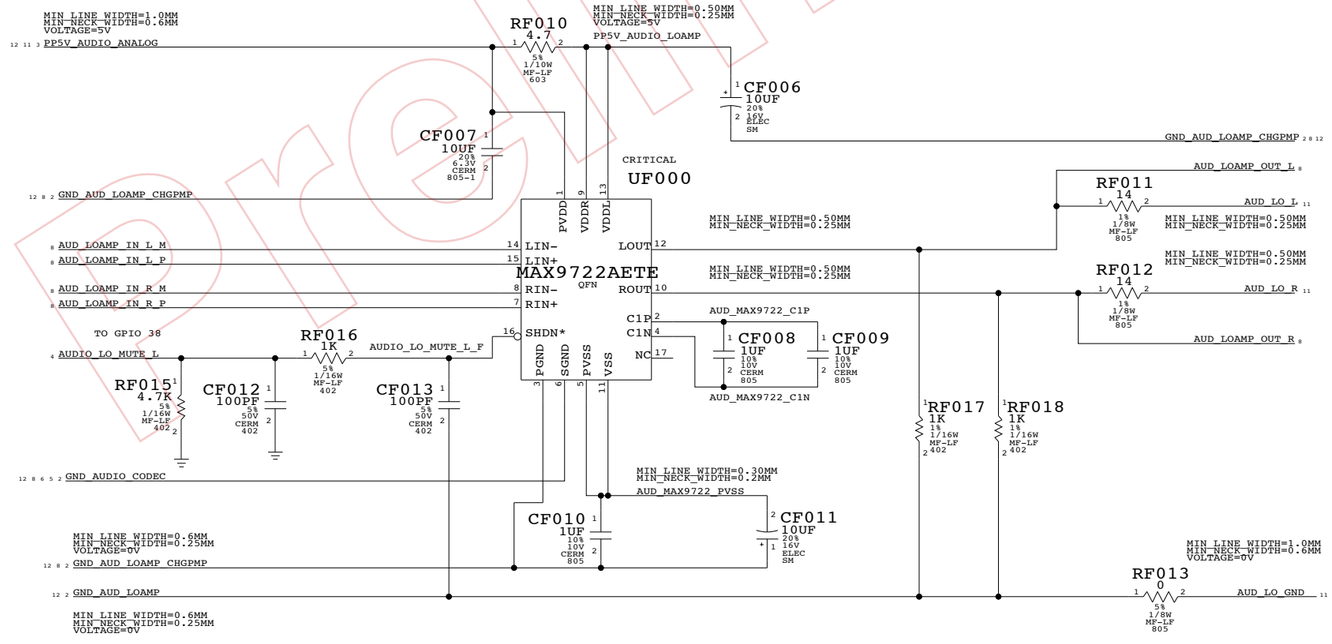
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
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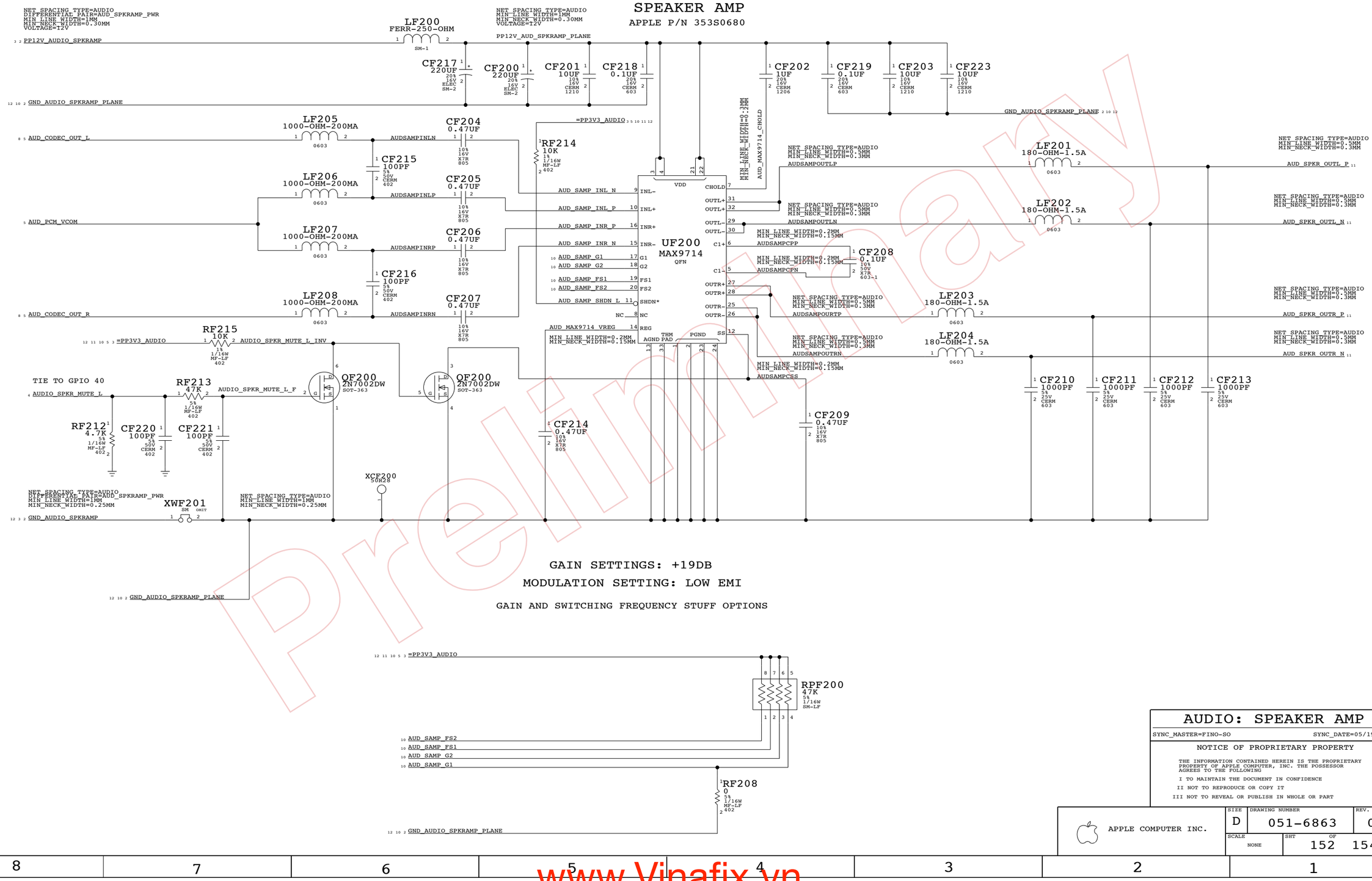
SPEAKER AMP

APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

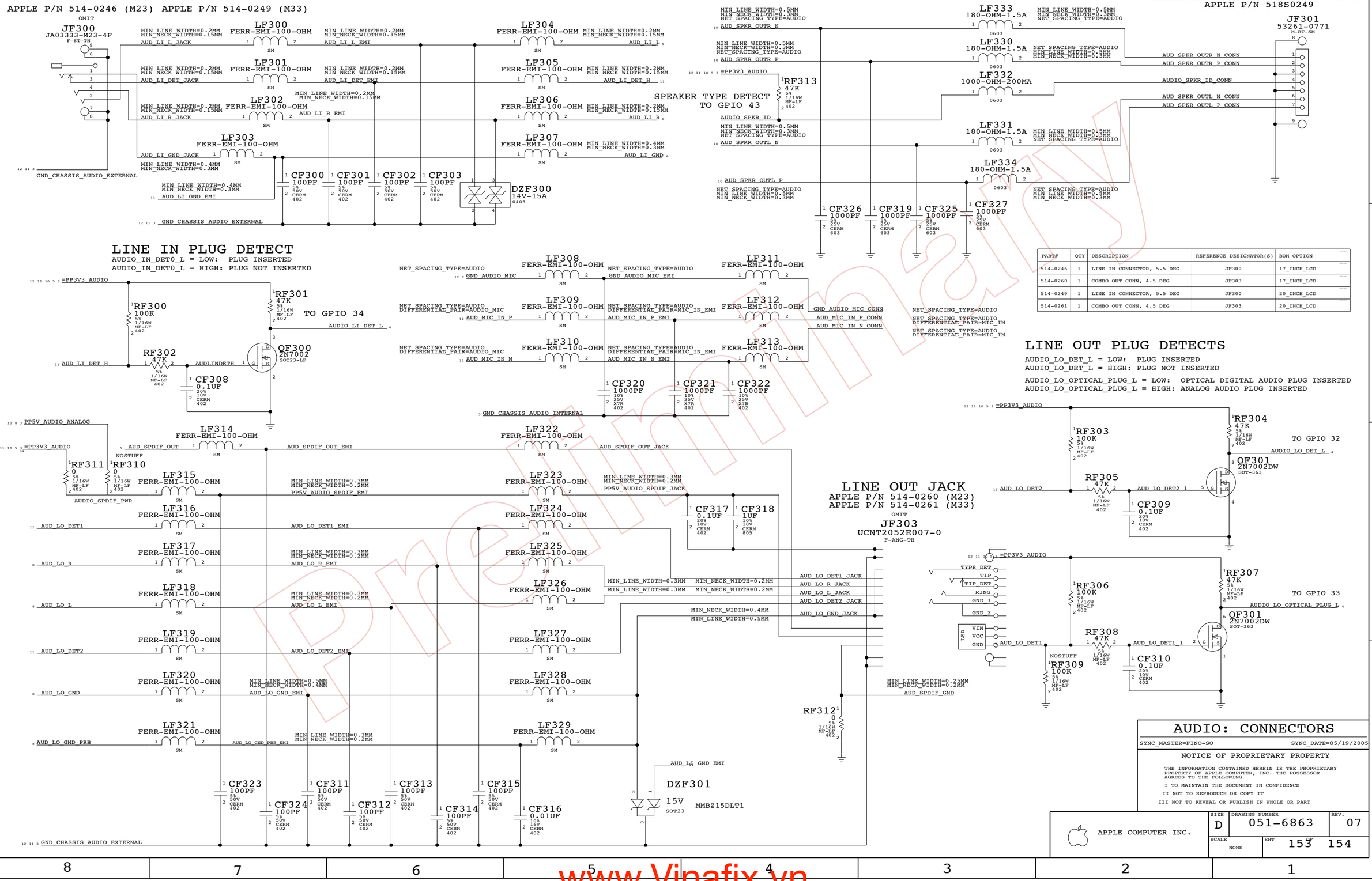
AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	152	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

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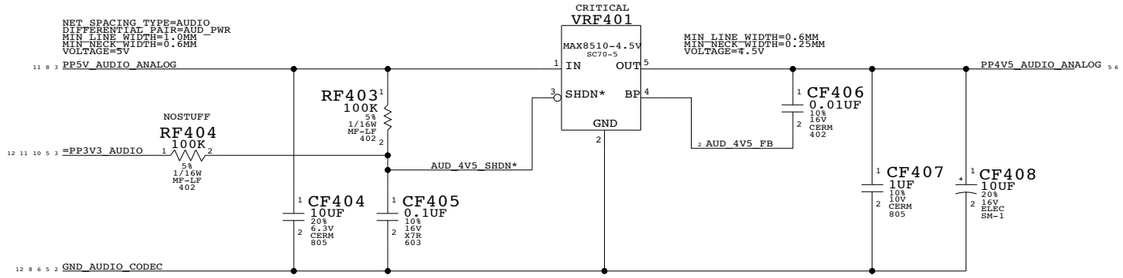
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 153 OF 154	

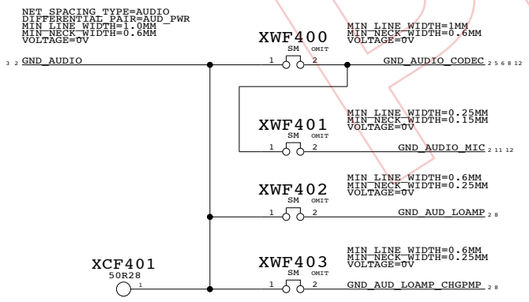
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733



AUDIO GROUND RETURNS



PLACE ACROSS GROUND SPLIT

NOSTUFF

RF416 0 5% 1/8W MF-LF 805

10 2 GND_AUDIO_SPKRAMP_PLANE — GND_AUDIO_CODEC 2 5 6 8 12

PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE

NOSTUFF

RF417 0 5% 1/8W MF-LF 805

10 3 2 GND_AUDIO_SPKRAMP

PLACE ACROSS GROUND SPLIT AT CODEC UE700

RF405 0 5% 1/8W MF-LF 805

12 8 6 5 2 GND_AUDIO_CODEC

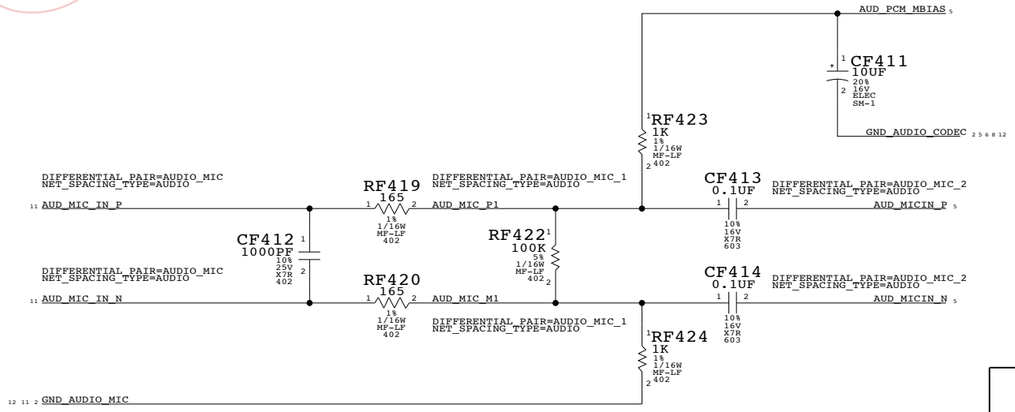
PLACE AT JF303

NOSTUFF

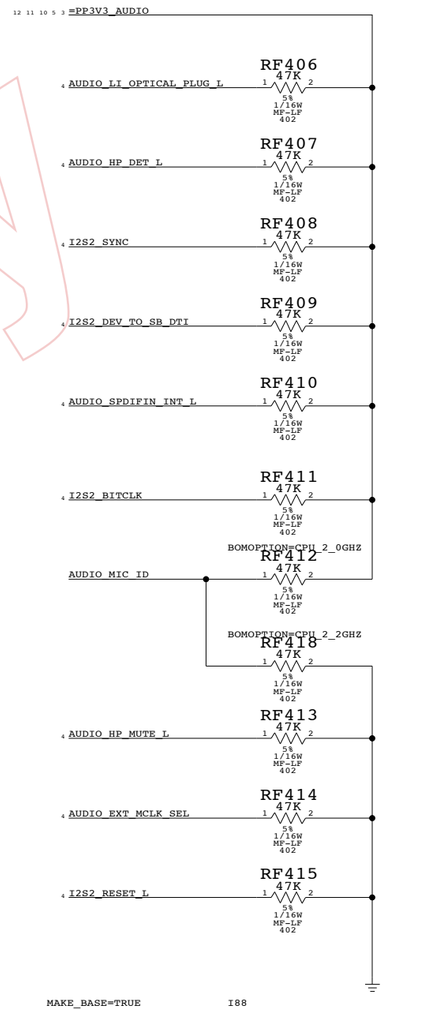
RF429 0 5% 1/8W MF-LF 805

11 3 GND_CHASSIS_AUDIO_EXTERNAL

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 154 OF 154	