1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

PRODUCTION RELEASED

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
H		468168	PRODUCTION RELEASED	10/17/06	06/22/04

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3	3	Power Block Diagram	M51_PAUL	08/04/2006
4	4	BOM Config	M51_DAVE	(MASTER)
5	5	FUNC TEST 1 OF 2	M51_HENRY	08/04/2006
6	6	POWER CONN / MISC	M51_PAUL	08/04/2006
7	7	CPU 1 OF 2-FSB	M50_HENRY	08/04/2006
8	8	CPU 2 OF 2-PWR/GND	M50_HENRY	08/04/2006
9	9	CPU DECAPS & VID<>	M51_HENRY	08/04/2006
10	10	ASIC TEMP SENSORS	M51_DAVE	(MASTER)
11	11	CPU ITP700FLEX DEBUG	M50_HENRY	08/04/2006
12	12	NB CPU Interface	M50_HENRY	08/04/2006
13	13	NB PEG / Video Interfaces	M50_HENRY	08/04/2006
14	14	NB Misc Interfaces	M50_HENRY	08/04/2006
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18	18	NB Grounds	M50_HENRY	08/04/2006
19	19	NB (GM) Decoupling	M51_DAVE	(MASTER)
20	20	NB Config Straps	M50_HENRY	08/04/2006
21	21	SB: 1 OF 4	M50_DOUG	08/04/2006
22	22	SB: 2 OF 4	M51_DOUG	08/04/2006
23	23	SB: 3 OF 4	M51_DOUG	08/04/2006
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25	25	SB:DECOUPLING	M51_DOUG	08/04/2006
26	26	SB: MISC	M50_DOUG	08/04/2006
27	27	M51 SMBus Connections	M51_DAVE	(MASTER)
28	28	DDR2 SO-DIMM Connector A	M51_HENRY	08/04/2006
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30	30	Memory Active Termination	M50_HENRY	08/04/2006
31	31	Memory Vtt Supply	M50_HENRY	08/04/2006
32	33	CLOCKS	M50_HENRY	08/04/2006
33	34	CLOCKS: TERMINATIONS	M51_HENRY	08/04/2006
34	38	Disk Connectors	M51_DOUG	08/04/2006
35	41	ETHERNET CONTROLLER	M50_DOUG	08/04/2006
36	42	ETHERNET MISC	M51_DOUG	08/04/2006
37	43	ETHERNET CONNECTOR	M51_DOUG	08/04/2006
38	44	FW: 1394B-LINK/PHY	M51_DOUG	08/04/2006
39	45	FW: 1394B MISC	M51_DOUG	08/04/2006
40	46	FIREWIRE CONNECTORS	M51_DOUG	08/04/2006
41	47	USB Device Interfaces	M51_DOUG	08/04/2006
42	53	AIRPORT CONN	M51_DOUG	08/04/2006
43	54	PCI-E CONNECTIONS	M51_DOUG	08/04/2006
44	58	SMC	M51_HENRY	08/04/2006
45	59	SMC & TPM SUPPORT	M51_HENRY	07/31/2006
46	60	LPC+ CONN	M51_HENRY	08/04/2006
47	63	SPI BOOTROM	M50_DOUG	08/04/2006
48	65	HD AND OD FAN	M51_HENRY	08/04/2006
49	66	CPU FAN, HD & OD TEMP	M51_HENRY	08/04/2006
50	67	TPM	M51_HENRY	08/04/2006
51	68	AUDIO: CODEC	AUDIO	08/04/2006
52	69	AUDIO: LINE INPUT AMP	AUDIO	08/04/2006
53	70	AUDIO: COMBO OUT AMP	AUDIO	08/04/2006
54	71	AUDIO: SPEAKER AMP_1	AUDIO	08/04/2006
55	72	AUDIO: SPEAKER AMP	AUDIO	08/04/2006
56	73	AUDIO: CONNECTORS	AUDIO	08/04/2006
57	74	AUDIO: POWER SUPPLIES	AUDIO	08/04/2006
58	75	IMVP6 CPU VCore Regulator	M51_PAUL	08/04/2006
59	76	CPU & SYSTEM SENSE	M51_DAVE	(MASTER)
60	77	PWR GOOD	M51_PAUL	08/04/2006
61	78	3V DC/DC 2.5V	M51_PAUL	08/04/2006
62	79	1.8V & 1.2V VREG	M51_PAUL	08/04/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	08/04/2006
64	82	5V DC/DC	M51_PAUL	08/04/2006
65	83	S0 AND S3 FETS	M51_PAUL	08/04/2006
66	84	MXM PCI-E & PWR	M51_DAVE	(MASTER)
67	85	MXM I/O	M51_DAVE	(MASTER)
68	94	Internal Display Conns	M51_DAVE	(MASTER)
69	97	External Display Conns	M51_DAVE	(MASTER)

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB,SCHEM,MLB,M51	SCH1		
820-1984	1	PCB,FAB,MLB,M51	MLB1		

NEW 630 BOMS AS OF 9/7
CURRENT: REV D 10/17
SCH: REV G

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

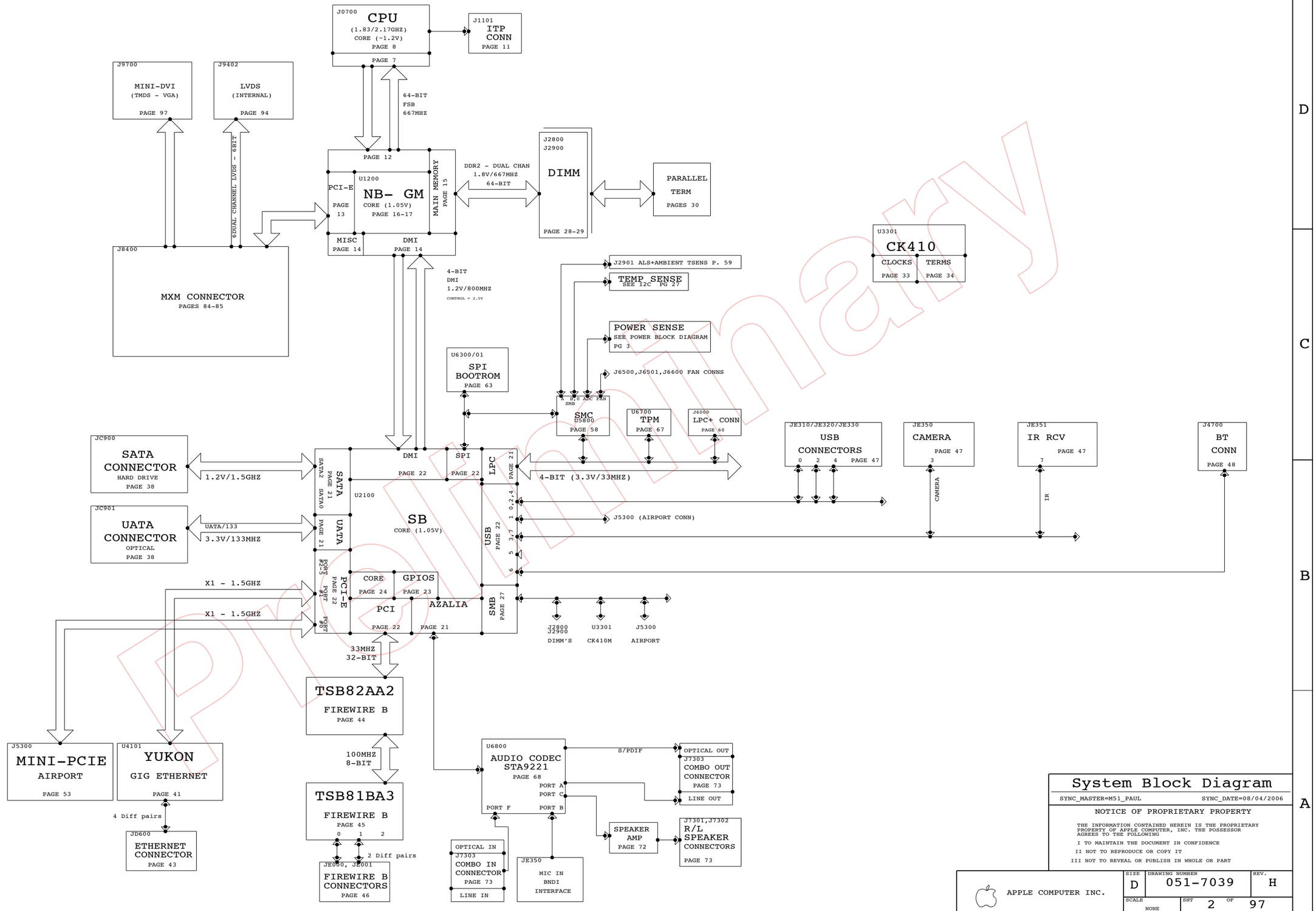
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE: SCHEM SANTANA

DRAWING NUMBER 051-7039 | REV. H

SHT 1 OF 97

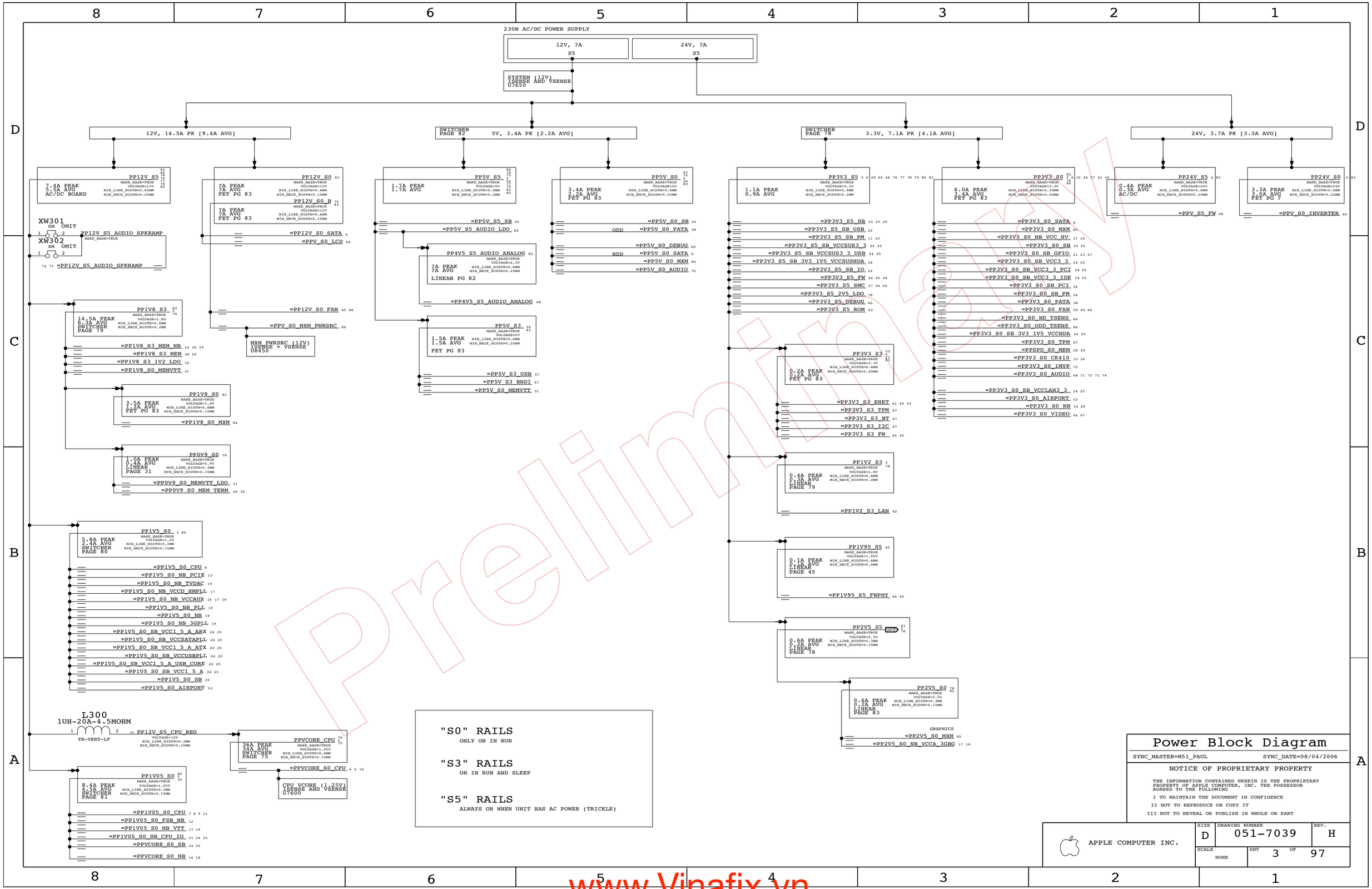


System Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 2 OF 97	



Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7899	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_WZD,PRODUCTION
630-7898	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_WZC,PRODUCTION

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSENS,CPU_PWR_SENSE
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_TSENS_INT,SYS_PWR_SENSE,MXM_PWR_SENSE

BarCode Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:WZD]	CRITICAL	EEE_WZD
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:WZC]	CRITICAL	EEE_WZC

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

CHIPSET, ROMS, ETC.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
359S0117	1	IC,SLG84435,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM
(335S0384) 341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	
(338S0274) 341T0020	1	IC,SMC,M51	U5800	CRITICAL	

PROCESSORS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3392	1	MEROM 2.33GHZ, M51	CPU	CRITICAL	M51_BEST
337S3390	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	

BATTERY IS INSTALLED AT FATP

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.
124-0361	124-0339		ALL	SANYO ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
353S1461	353S1465		U7500	CPU VREG NEW REV
740S0044	740S0028		F9710	DVI DDC (LITTLEFUSE)
138S0567	138S0516		ALL	CAP CONSOLIDATION
376S0388	376S0444		ALL	ON SEMI 2ND SRC FOR IR

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION

PULL-DOWNS FOR UNUSED PINS
WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8458	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8459	PRODUCTION

PULL-DOWNS FOR UNUSED PINS
WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K-OHM,5%,0402	C7602	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C7612	NOSTUFF

PULL-DOWNS FOR UNUSED PINS
WHEN DEVELOPMENT SENSORS ARE GONE

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H

SCALE NONE SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 OMIT P4MM

34 22 PCI_CLK_SB PP6D0 OMIT P4MM
44 34 PCI_CLK_FW PP626 OMIT P4MM
58 34 PCI_CLK_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 OMIT P4MM
38 21 IDE_PDIORDY PP6C7 OMIT P4MM
38 21 IDE_PDD<9> PP6C8 OMIT P4MM

54 22 PCIE_B_D2R_P PP600 OMIT P4MM
54 22 PCIE_B_D2R_N PP601 OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 OMIT P4MM
63 58 22 SPI_SO PP612 OMIT P4MM
63 58 22 SPI_SI PP613 OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 OMIT P4MM
27 SMBUS_SB_SDA PP605 OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 OMIT P4MM

FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 OMIT P4MM

I473
14 NB_CFG<17> — I474 — NC_NB_CFG<17> MAKE_BASE=TRUE
14 NB_CFG<15> — I475 — NC_NB_CFG<15> MAKE_BASE=TRUE
14 NB_CFG<14> — I476 — NC_NB_CFG<14> MAKE_BASE=TRUE
14 NB_CFG<13> — I477 — NC_NB_CFG<13> MAKE_BASE=TRUE
14 NB_CFG<12> — I478 — NC_NB_CFG<12> MAKE_BASE=TRUE
14 NB_CFG<11> — I479 — NC_NB_CFG<11> MAKE_BASE=TRUE
14 NB_CFG<10> — I481 — NC_NB_CFG<10> MAKE_BASE=TRUE
14 NB_CFG<8> — I480 — NC_NB_CFG<8> MAKE_BASE=TRUE
14 NB_CFG<6> — I482 — NC_NB_CFG<6> MAKE_BASE=TRUE
14 NB_CFG<4> — I483 — NC_NB_CFG<4> MAKE_BASE=TRUE
14 NB_CFG<3> — NC_NB_CFG<3> MAKE_BASE=TRUE

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 OMIT P4MM
14 NB_RST_IN_L_R PP666 OMIT P4MM

22 14 DMI_S2N_N<0> PP673 OMIT P4MM
22 14 DMI_S2N_P<0> PP674 OMIT P4MM
19 14 MEM_VREF_NB_0 PP6E1 OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 OMIT P4MM

I513
22 PCI_GNT3_L — — TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT
22 USB_F_N — TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P — TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
19 13 LVDS_BKLTEN — TP_LVDS_BKLTEN MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN PEG_R2D_C_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<15> NO_TEST=TRUE

84 13 IN PEG_R2D_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_P<15> NO_TEST=TRUE

84 13 IN PEG_D2R_N<0> NO_TEST=TRUE
84 13 IN PEG_D2R_P<0> NO_TEST=TRUE
84 13 IN PEG_D2R_N<1> NO_TEST=TRUE
84 13 IN PEG_D2R_P<1> NO_TEST=TRUE
84 13 IN PEG_D2R_N<2> NO_TEST=TRUE
84 13 IN PEG_D2R_P<2> NO_TEST=TRUE
84 13 IN PEG_D2R_N<3> NO_TEST=TRUE
84 13 IN PEG_D2R_P<3> NO_TEST=TRUE
84 13 IN PEG_D2R_N<4> NO_TEST=TRUE
84 13 IN PEG_D2R_P<4> NO_TEST=TRUE
84 13 IN PEG_D2R_N<5> NO_TEST=TRUE
84 13 IN PEG_D2R_P<5> NO_TEST=TRUE
84 13 IN PEG_D2R_N<6> NO_TEST=TRUE
84 13 IN PEG_D2R_P<6> NO_TEST=TRUE
84 13 IN PEG_D2R_N<7> NO_TEST=TRUE
84 13 IN PEG_D2R_P<7> NO_TEST=TRUE
84 13 IN PEG_D2R_N<8> NO_TEST=TRUE
84 13 IN PEG_D2R_P<8> NO_TEST=TRUE
84 13 IN PEG_D2R_N<9> NO_TEST=TRUE
84 13 IN PEG_D2R_P<9> NO_TEST=TRUE
84 13 IN PEG_D2R_N<10> NO_TEST=TRUE
84 13 IN PEG_D2R_P<10> NO_TEST=TRUE
84 13 IN PEG_D2R_N<11> NO_TEST=TRUE
84 13 IN PEG_D2R_P<11> NO_TEST=TRUE
84 13 IN PEG_D2R_N<12> NO_TEST=TRUE
84 13 IN PEG_D2R_P<12> NO_TEST=TRUE
84 13 IN PEG_D2R_N<13> NO_TEST=TRUE
84 13 IN PEG_D2R_P<13> NO_TEST=TRUE
84 13 IN PEG_D2R_N<14> NO_TEST=TRUE
84 13 IN PEG_D2R_P<14> NO_TEST=TRUE
84 13 IN PEG_D2R_N<15> NO_TEST=TRUE
84 13 IN PEG_D2R_P<15> NO_TEST=TRUE

76 75 3 IN PPVCORE_CPU FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
83 78 3 IN PP2V5_S5 FUNC_TEST=TRUE
83 79 3 IN PP1V8_S3 FUNC_TEST=TRUE
79 3 IN PP1V2_S3 FUNC_TEST=TRUE
80 3 IN PP1V5_S0 FUNC_TEST=TRUE
80 34 3 IN PP1V05_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
97 83 75 59 3 IN PP5V_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
84 83 76 45 41 27 26 10 6 3 IN PP3V3_S0 FUNC_TEST=TRUE
83 3 IN PP24V_S0 FUNC_TEST=TRUE

11 7 IN XDP_BPM_L<3> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<2> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<1> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<0> FUNC_TEST=TRUE
26 11 7 IN XDP_DBRESET_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<0> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<1> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<2> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<3> FUNC_TEST=TRUE
67 60 58 21 5 IN LPC_FRAME_L FUNC_TEST=TRUE
67 60 58 23 IN PM_CLKRUN_L FUNC_TEST=TRUE
60 58 22 IN BOOT_LPC_SPI_L FUNC_TEST=TRUE
60 6 IN DEBUG_RST_L FUNC_TEST=TRUE
60 59 21 IN FWH_INIT_L FUNC_TEST=TRUE
60 34 IN PCI_CLK_PORT80 FUNC_TEST=TRUE
67 60 58 23 IN INT_SERIRQ FUNC_TEST=TRUE
67 60 58 23 IN PM_SUS_STAT_L FUNC_TEST=TRUE
60 58 IN SMC_MD1 FUNC_TEST=TRUE
60 59 58 IN SMC_RST_L FUNC_TEST=TRUE
60 58 IN SMC_NMI FUNC_TEST=TRUE
60 23 IN SV_SET_UP FUNC_TEST=TRUE
76 58 IN ISENSE_CAL_EN FUNC_TEST=TRUE
94 85 IN INV_ENABLE_BL FUNC_TEST=TRUE
94 IN LCD_PWM FUNC_TEST=TRUE
75 8 IN CPU_VID<0> FUNC_TEST=TRUE
75 8 IN CPU_VID<1> FUNC_TEST=TRUE
75 8 IN CPU_VID<2> FUNC_TEST=TRUE
75 8 IN CPU_VID<3> FUNC_TEST=TRUE
75 8 IN CPU_VID<4> FUNC_TEST=TRUE
75 8 IN CPU_VID<5> FUNC_TEST=TRUE
75 8 IN CPU_VID<6> FUNC_TEST=TRUE
75 23 14 IN PM_DPRSLPVR FUNC_TEST=TRUE
75 21 7 IN CPU_DPRSTP_L FUNC_TEST=TRUE
75 26 14 5 IN VR_PWRGOOD_DELAY FUNC_TEST=TRUE
26 23 IN VR_PWRGD_CK410 FUNC_TEST=TRUE
84 77 58 26 IN ALL_SYS_PWRGD FUNC_TEST=TRUE
77 58 23 IN PM_SLP_S4_L FUNC_TEST=TRUE
80 79 77 58 23 IN PM_SLP_S3_L FUNC_TEST=TRUE

60 59 58 IN SMC_TCK FUNC_TEST=TRUE
60 59 58 IN SMC_TDI FUNC_TEST=TRUE
60 59 58 IN SMC_TDO FUNC_TEST=TRUE
60 59 58 IN SMC_TMS FUNC_TEST=TRUE
60 58 IN SMC_TRST_L FUNC_TEST=TRUE
60 59 58 IN SMC_TX_L FUNC_TEST=TRUE
60 59 58 IN SMC_RX_L FUNC_TEST=TRUE
59 IN SMC_MANUAL_RST_L FUNC_TEST=TRUE
11 7 IN XDP_TCK FUNC_TEST=TRUE
11 7 IN XDP_TDI FUNC_TEST=TRUE
11 7 IN XDP_TDO FUNC_TEST=TRUE
11 7 IN XDP_TMS FUNC_TEST=TRUE
11 7 IN XDP_TRST_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXP FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXN FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_N FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_P FUNC_TEST=TRUE
11 IN ITPRESET_L FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<5> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<4> FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA 1
ZH510 HOLE-VIA 1
ZH520 HOLE-VIA 1
ZH501 HOLE-VIA 1
ZH511 HOLE-VIA 1
ZH521 HOLE-VIA 1
ZH502 HOLE-VIA 1
ZH512 HOLE-VIA 1
ZH522 HOLE-VIA 1
ZH503 HOLE-VIA 1
ZH513 HOLE-VIA 1
ZH523 HOLE-VIA 1
ZH504 HOLE-VIA 1
ZH514 HOLE-VIA 1
ZH524 HOLE-VIA 1
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ZH515 HOLE-VIA 1
ZH525 HOLE-VIA 1
ZH506 HOLE-VIA 1
ZH516 HOLE-VIA 1
ZH526 HOLE-VIA 1
ZH507 HOLE-VIA 1
ZH517 HOLE-VIA 1
ZH527 HOLE-VIA 1
ZH508 HOLE-VIA 1
ZH518 HOLE-VIA 1
ZH528 HOLE-VIA 1
ZH509 HOLE-VIA 1
ZH519 HOLE-VIA 1
ZH529 HOLE-VIA 1

FUNC TEST 1 OF 2

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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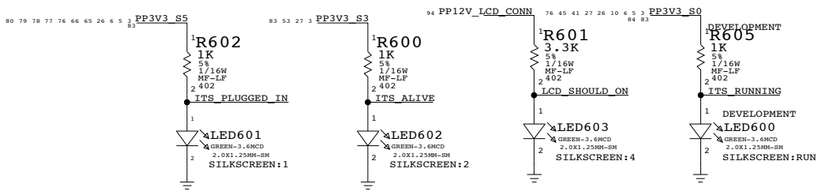
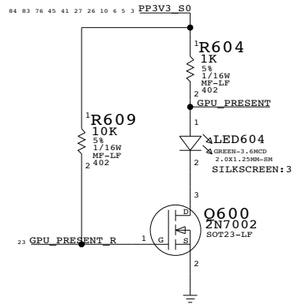
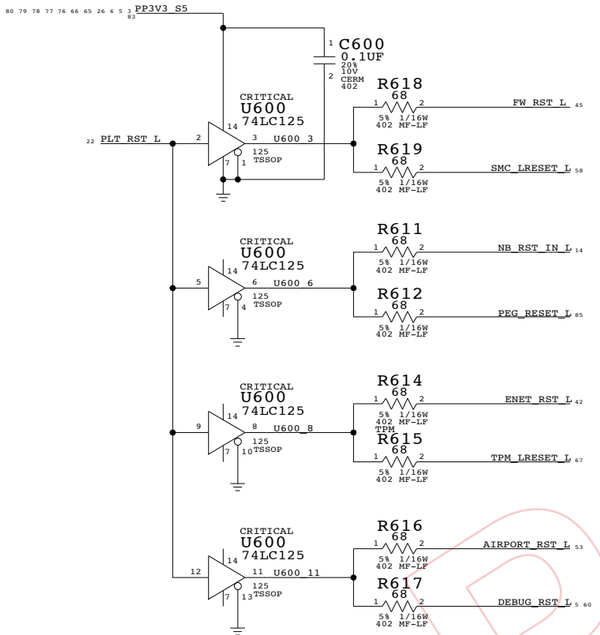
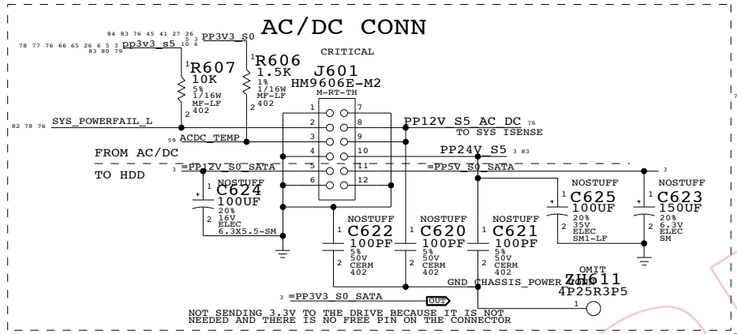
SYSTEM STATUS

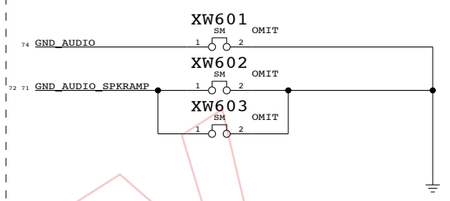




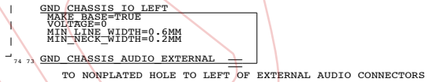




GND RAILS

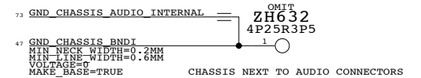


CHASSIS GND

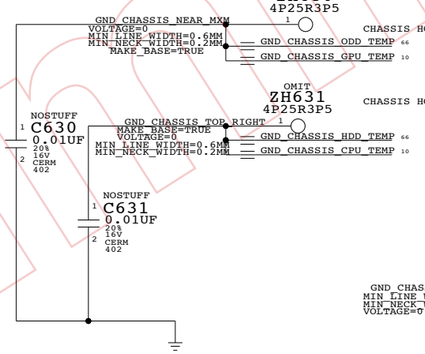


TO NONPLATED HOLE TO LEFT OF EXTERNAL AUDIO CONNECTORS

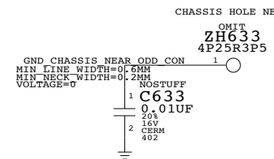
TO NONPLATED SLOT TO RIGHT OF EXTERNAL IO



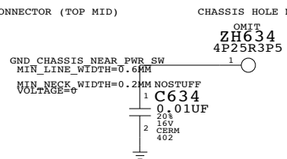
CHASSIS NEXT TO AUDIO CONNECTORS



CHASSIS HOLE NEAR ODD CONNECTOR (TOP MID)



CHASSIS HOLE NEAR POWER SWITCH CONNECTOR (BOT RIGHT)



HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU

POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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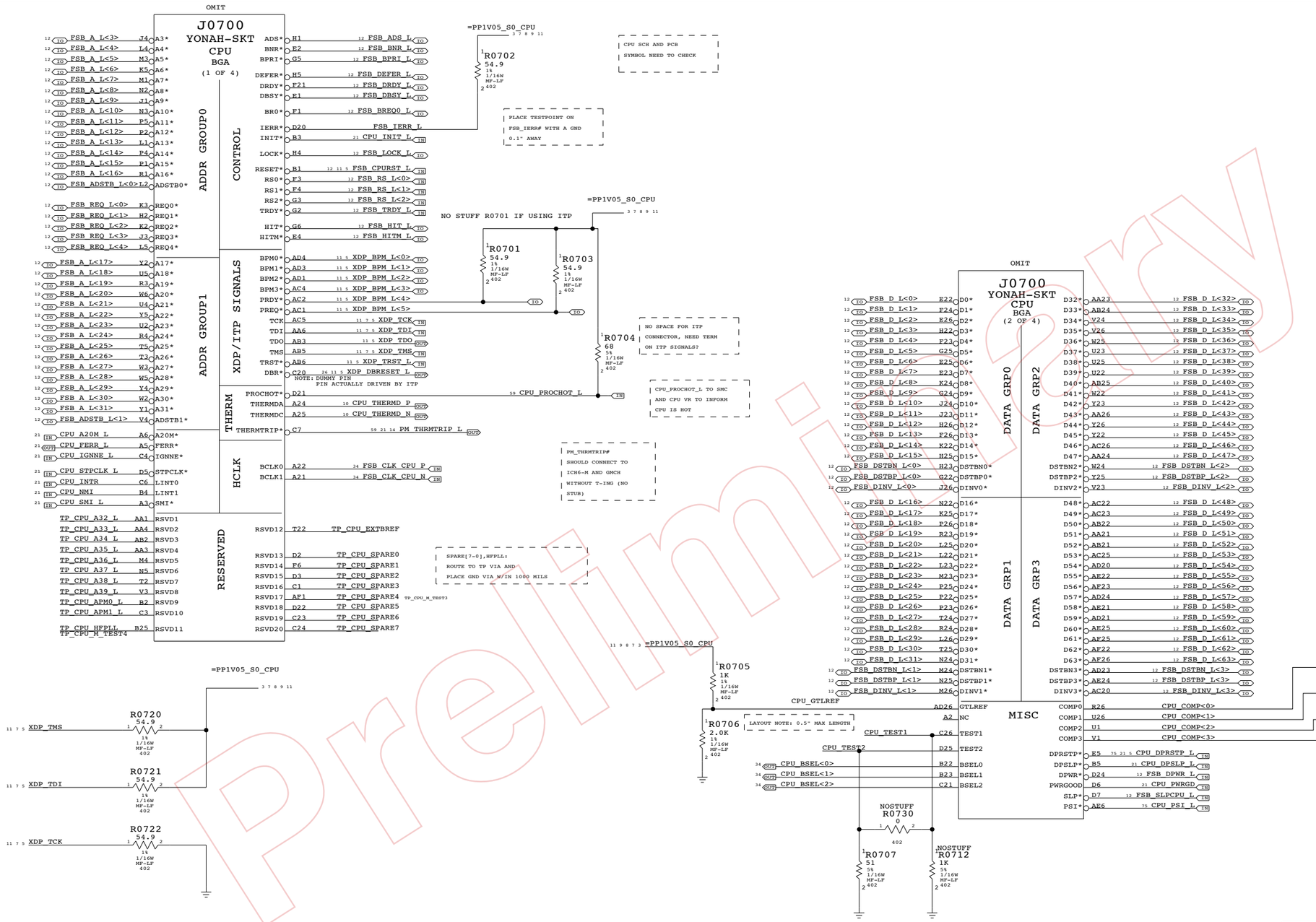
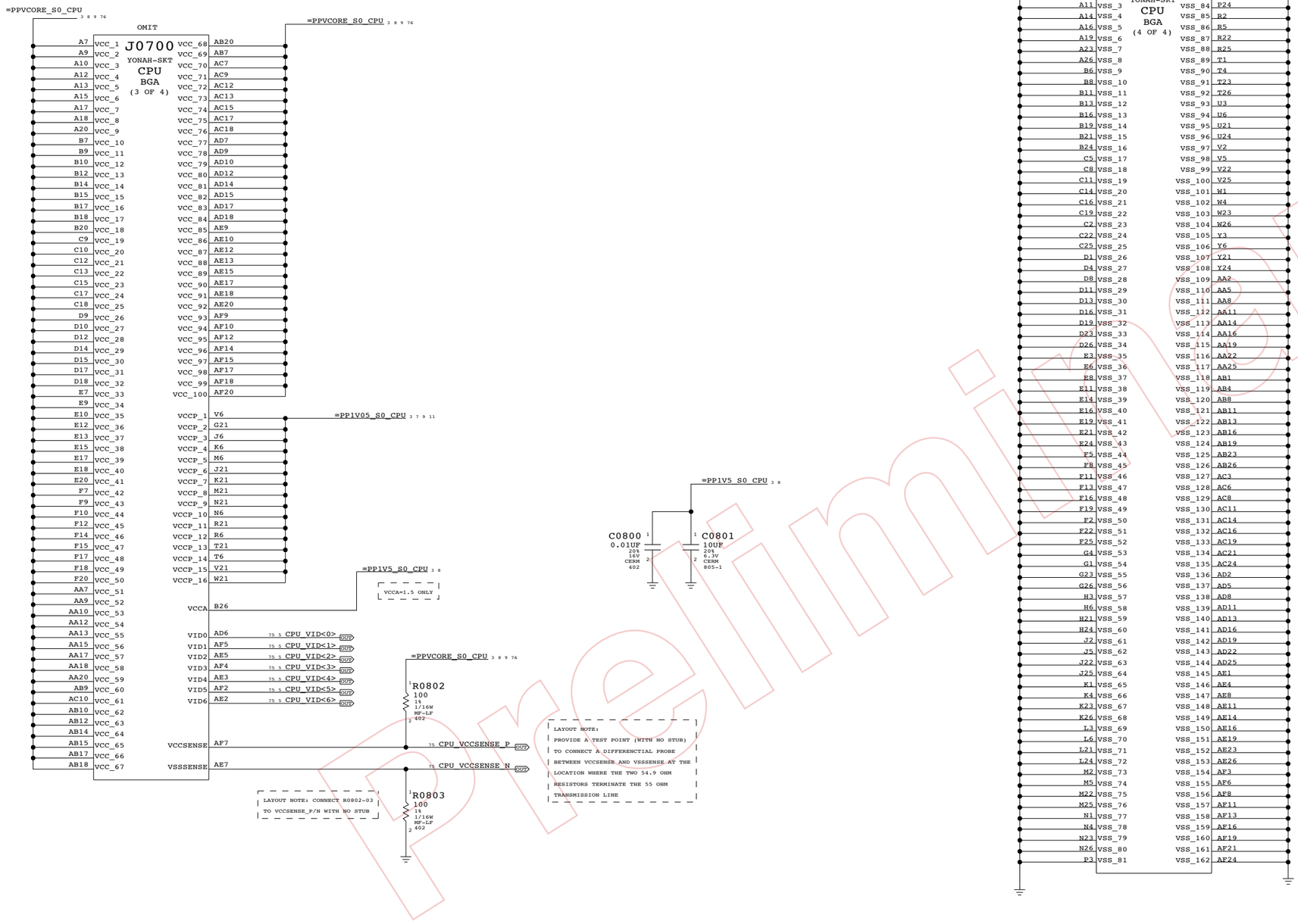


CPU 1 OF 2-FSB

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 7 OF 97	



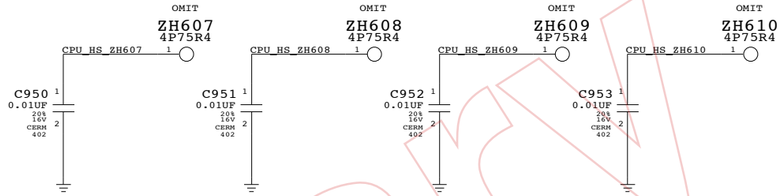
CPU 2 OF 2-PWR/GND

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 8 OF 97	

CPU HEATSINK MOUNTING HOLES



WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING

11 8 7 3 =PP1V05_S0_CPU

PLACE INSIDE SOCKET CAVITY ON L8 (NORTH SIDE SECONDARY)

C926 0.1UF 20% 10V CERM 402
C934 0.1UF 20% 10V CERM 402
C935 0.1UF 20% 10V CERM 402
C936 0.1UF 20% 10V CERM 402
C937 0.1UF 20% 10V CERM 402
C938 0.1UF 20% 10V CERM 402

NEED LARGE BULK FOR 1.05V

VCC CORE DECOUPLING

76 8 3 =PPVCORE_S0_CPU

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF

PLACE 8 INSIDE SOCKET CAVITY ON L8 (NORTH SIDE SECONDARY)

C923 C911 C910 C908 C901 C928 C900 C909 C907 C929
22UF 20% 6.3V X5R 805

PLACE 8 INSIDE SOCKET CAVITY ON L8 (SOUTH SIDE SECONDARY)

C924 C918 C913 C912 C904 C930 C902 C931 C939 C920
22UF 20% 6.3V X5R 805

PLACE 6 INSIDE SOCKET CAVITY ON L1 (NORTH SIDE PRIMARY)

C925 C919 C916 NOSTUFF C914 NOSTUFF C932 NOSTUFF C905 C999 C998 C997 C996
22UF 20% 6.3V X5R 805

PLACE 6 INSIDE SOCKET CAVITY ON L1 (SOUTH SIDE PRIMARY)

C922 C921 NOSTUFF C917 NOSTUFF C915 C906 NOSTUFF C903 C993 C994 C995 C988
22UF 20% 6.3V X5R 805

SOUTH SIDE SECONDARY

C941 C942 C943 C944 C945 C946 C989 C990 C991 C992
22UF 20% 6.3V X5R 805

NOSTUFF
C947 470UF 20% 2.5V TANT D2T

CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

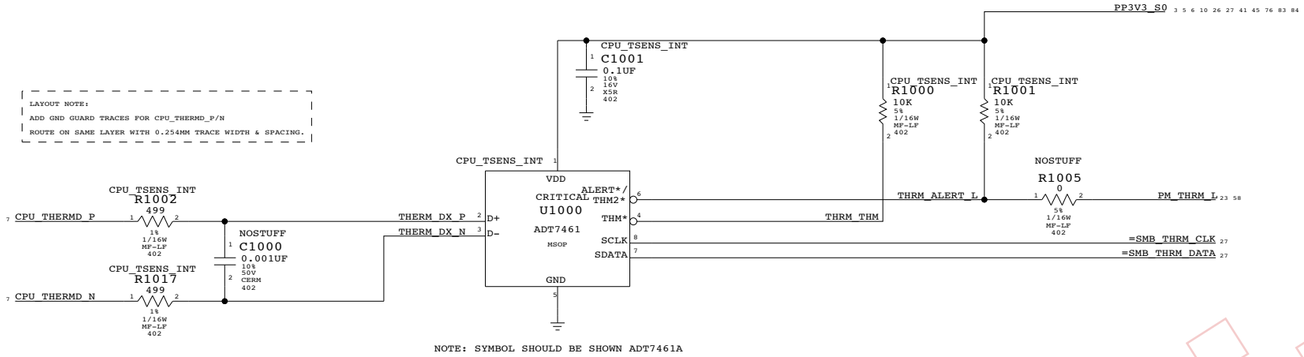
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 9 OF 97	

CPU INTERNAL DIODE THERMAL SENSOR

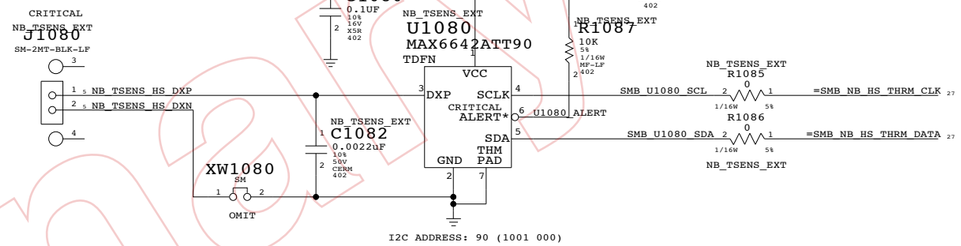
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



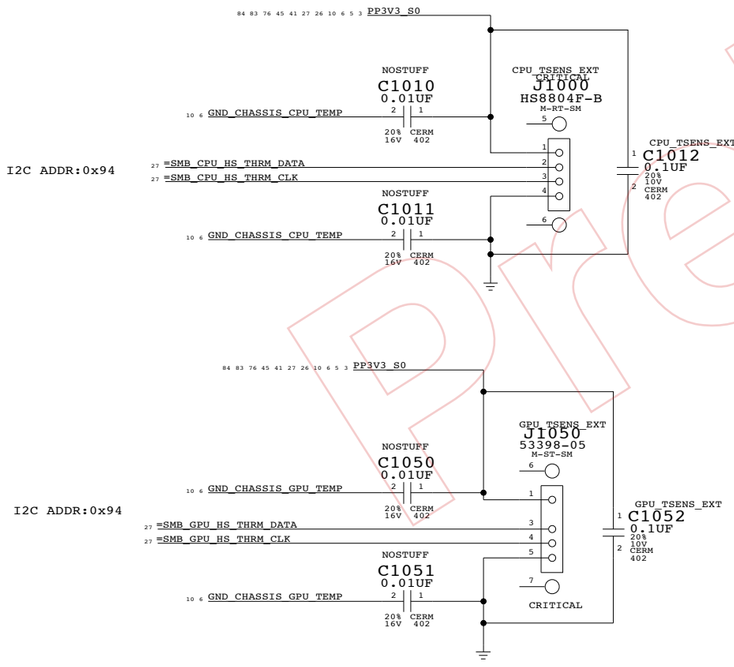
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

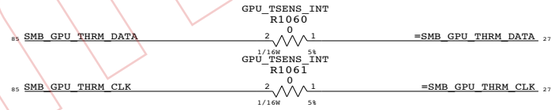


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

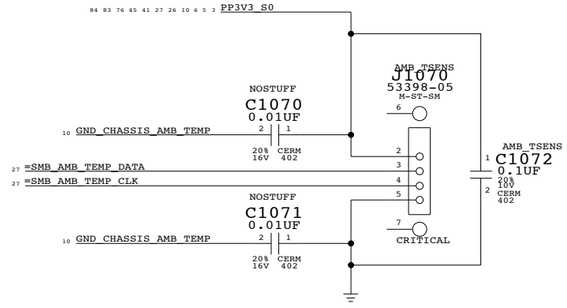


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



ASIC TEMP SENSORS			
SYNC_MASTER=M51_DAVE		SYNC_DATE=(MASTER)	
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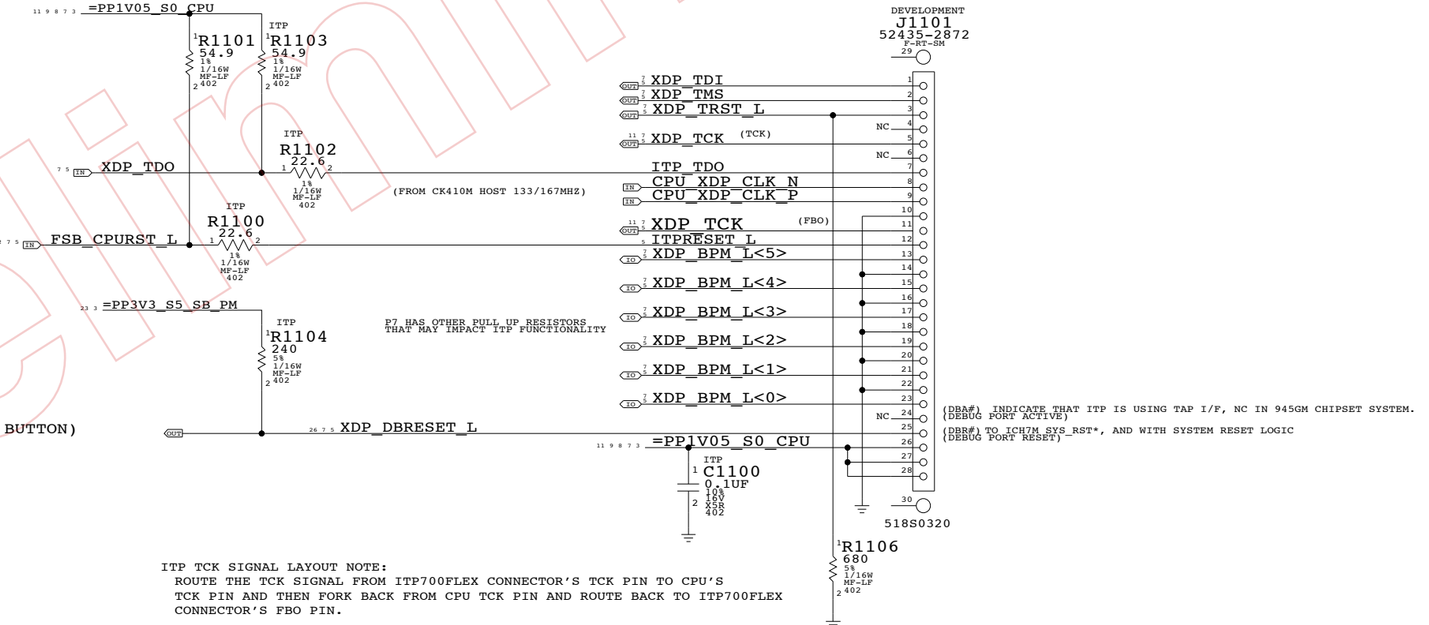
	SCALE NONE	SHT 10 OF 97	

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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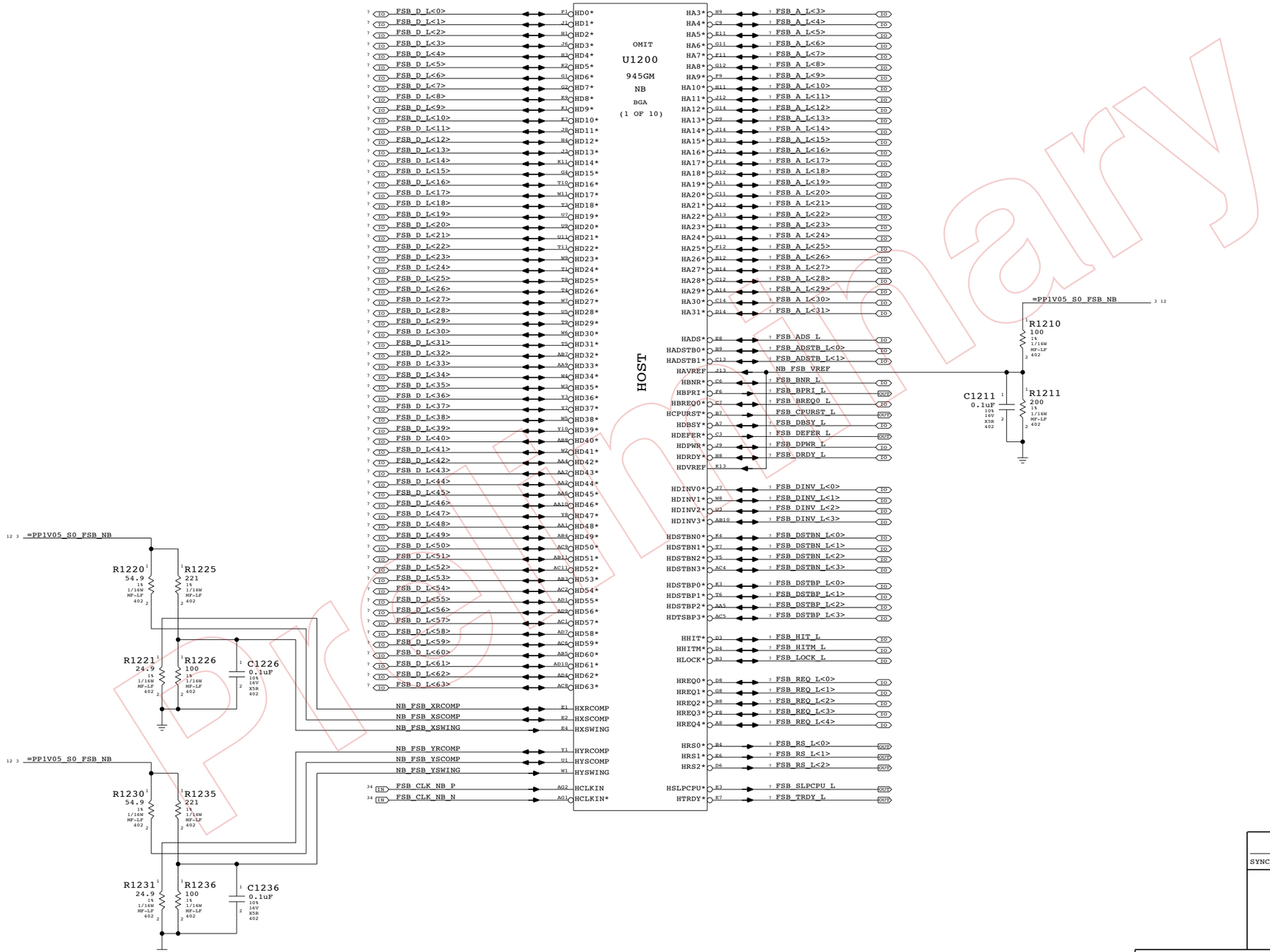
SCALE: NONE	SHT 11 OF 97	



NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

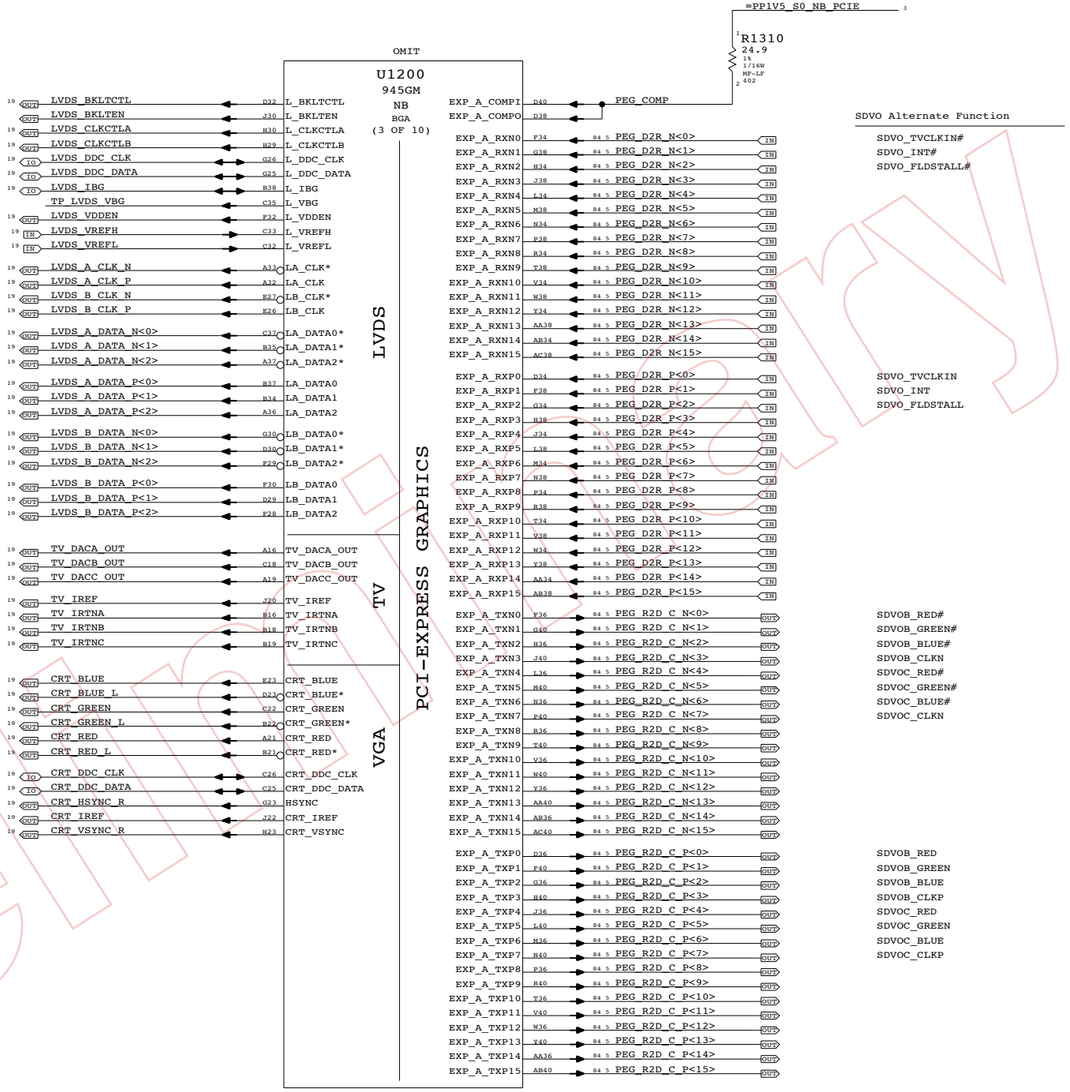
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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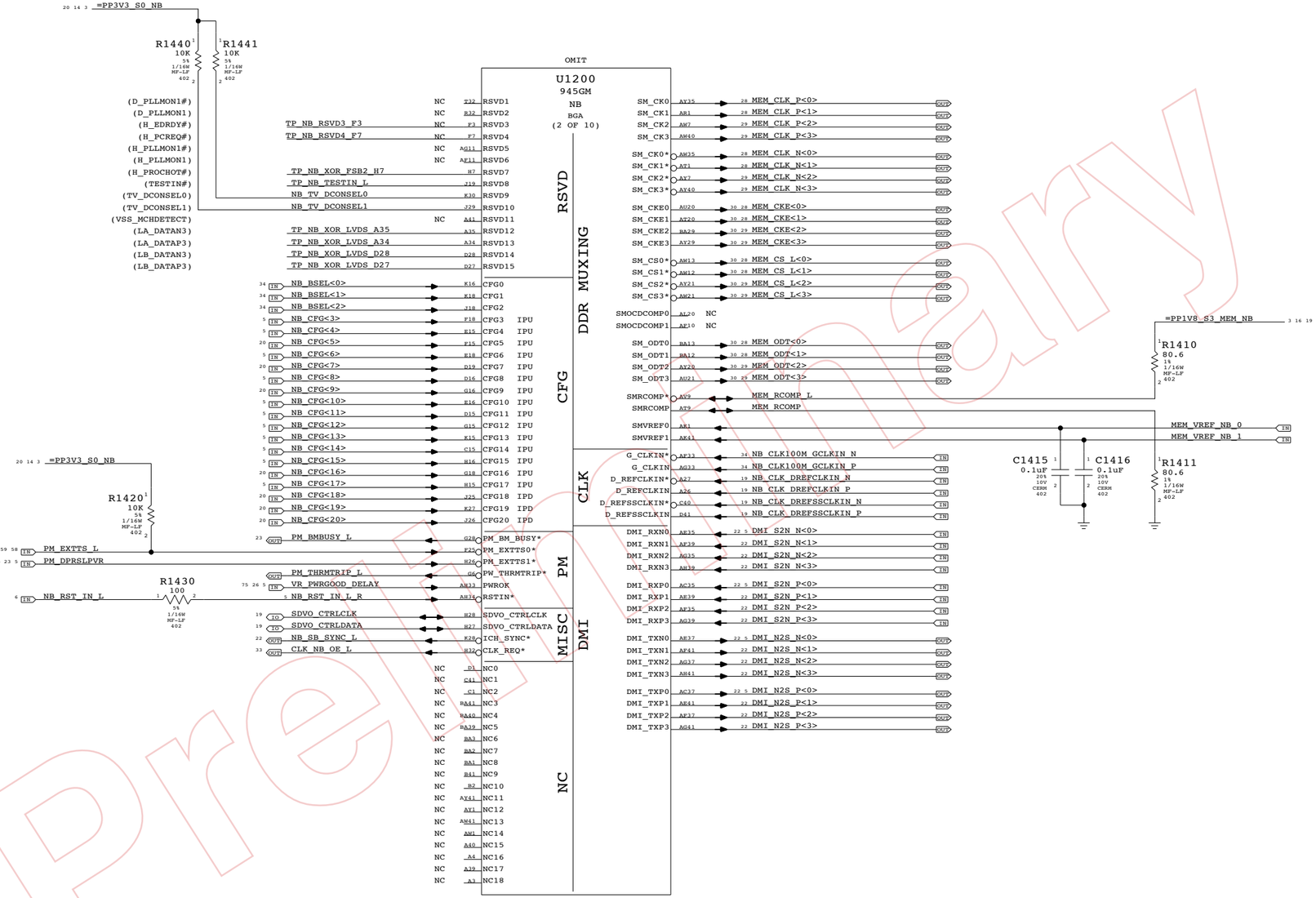

NB Misc Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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SIZE	DRAWING NUMBER	REV.
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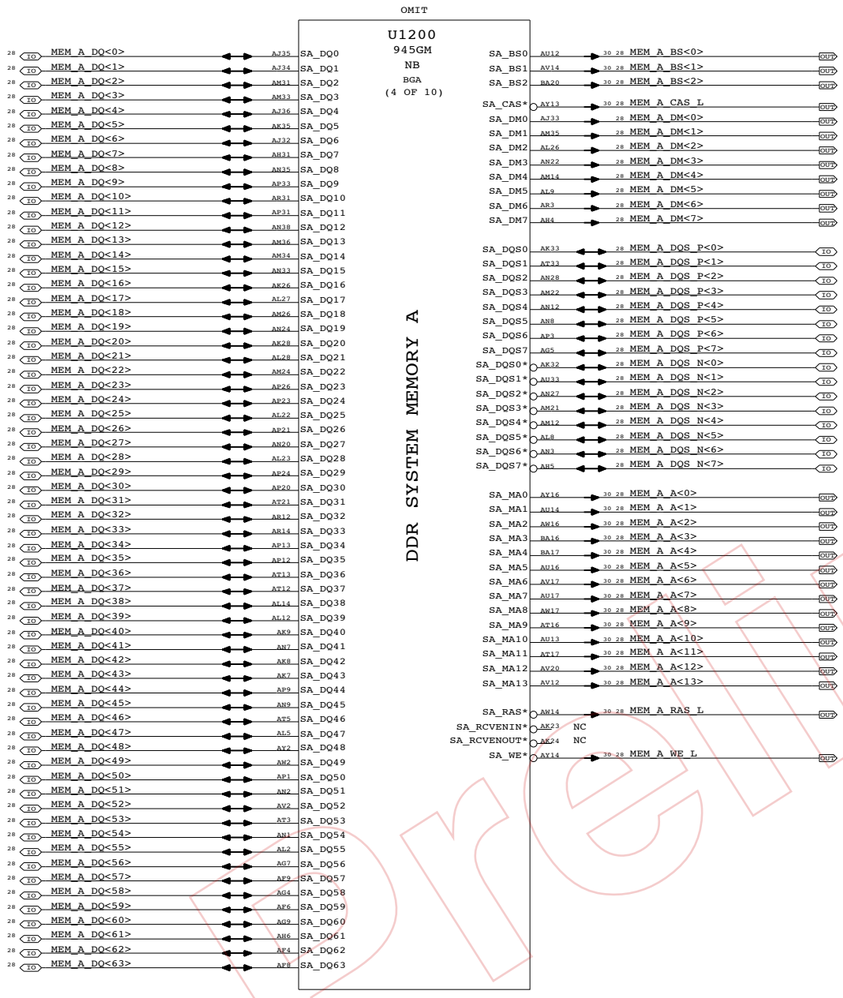
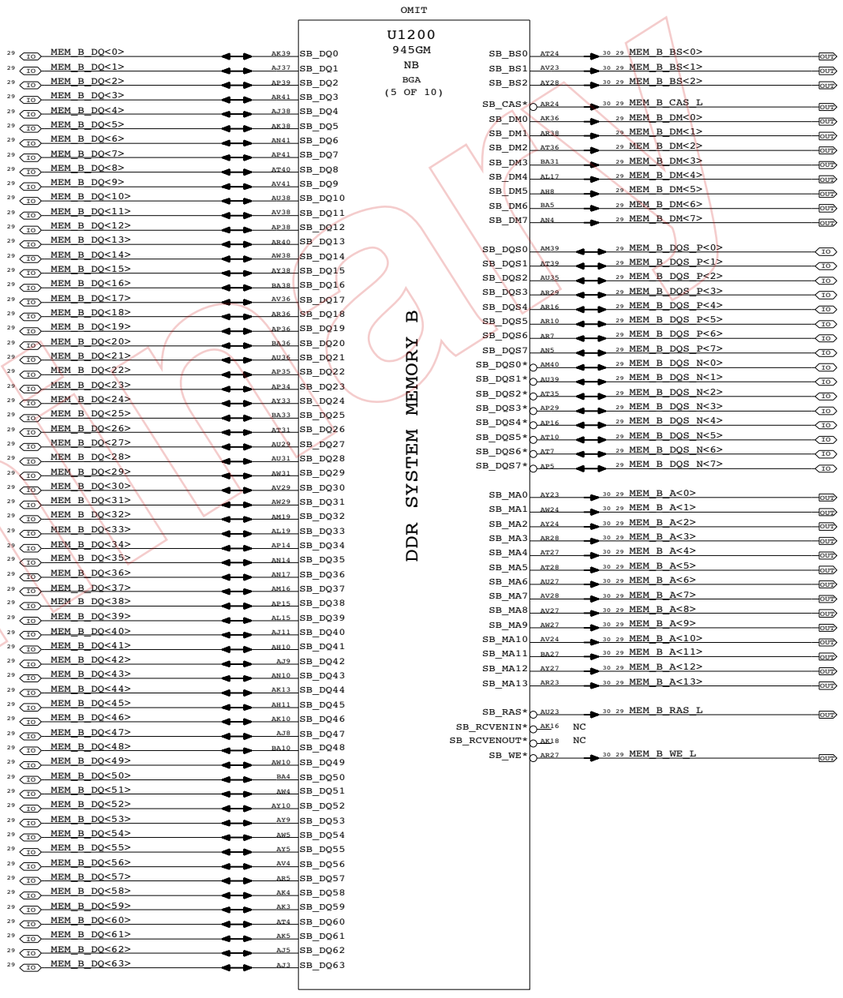
SCALE: NONE SHT 14 OF 97





NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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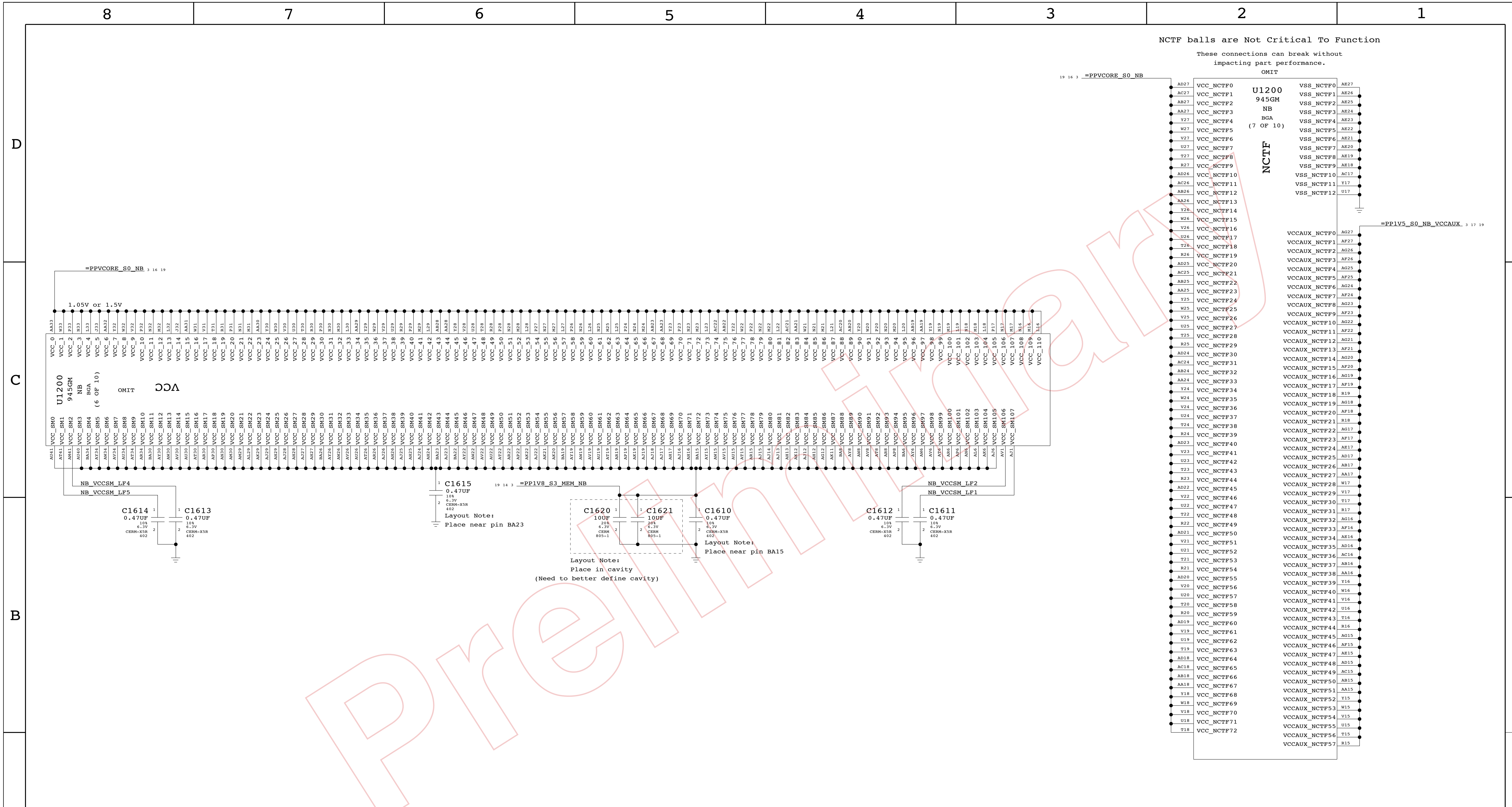

NB Power 1

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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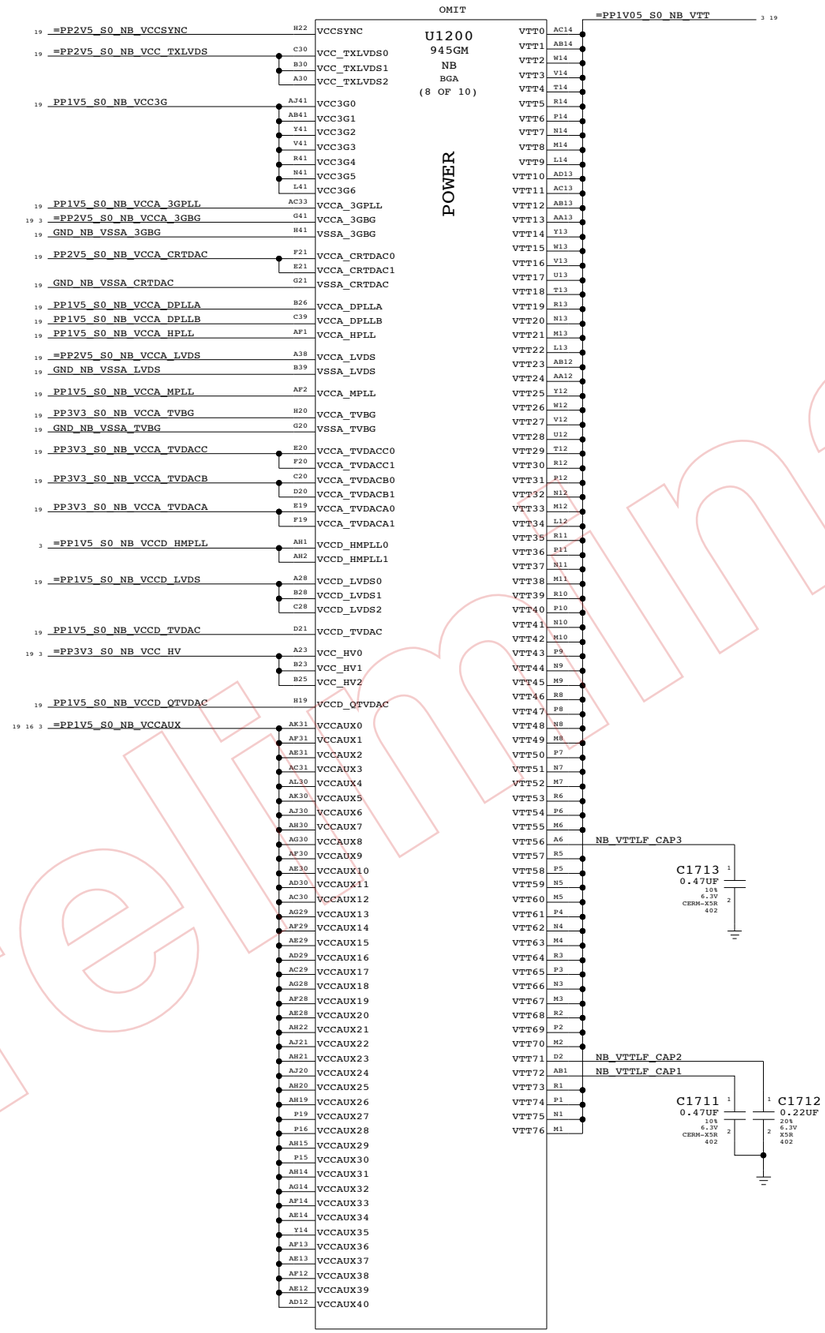
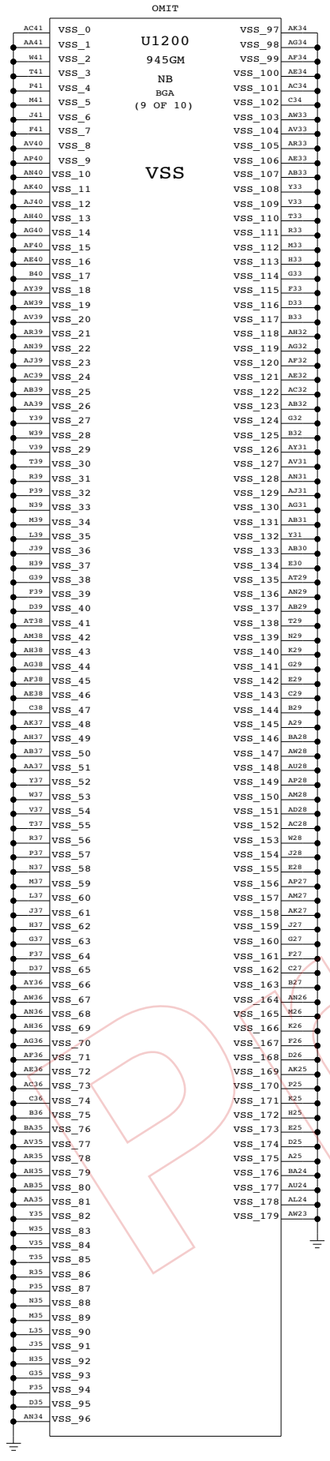


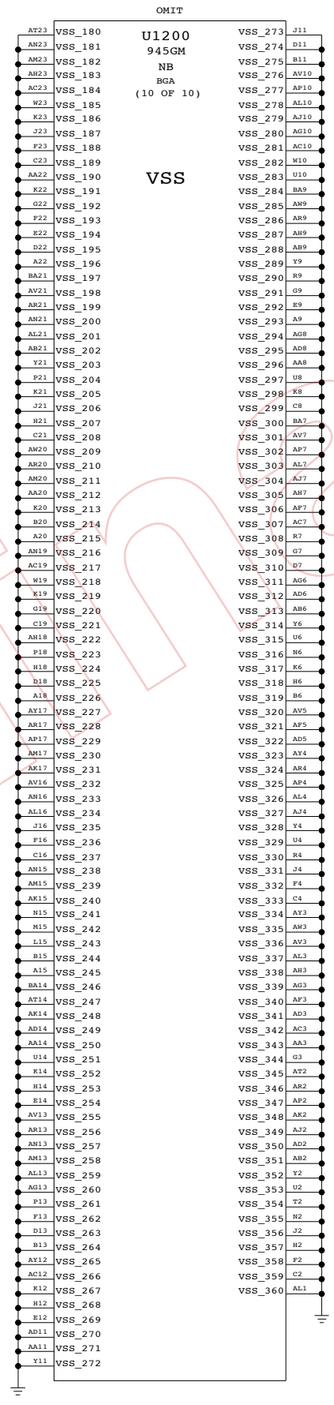
NB Power 2

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 17 OF 97	





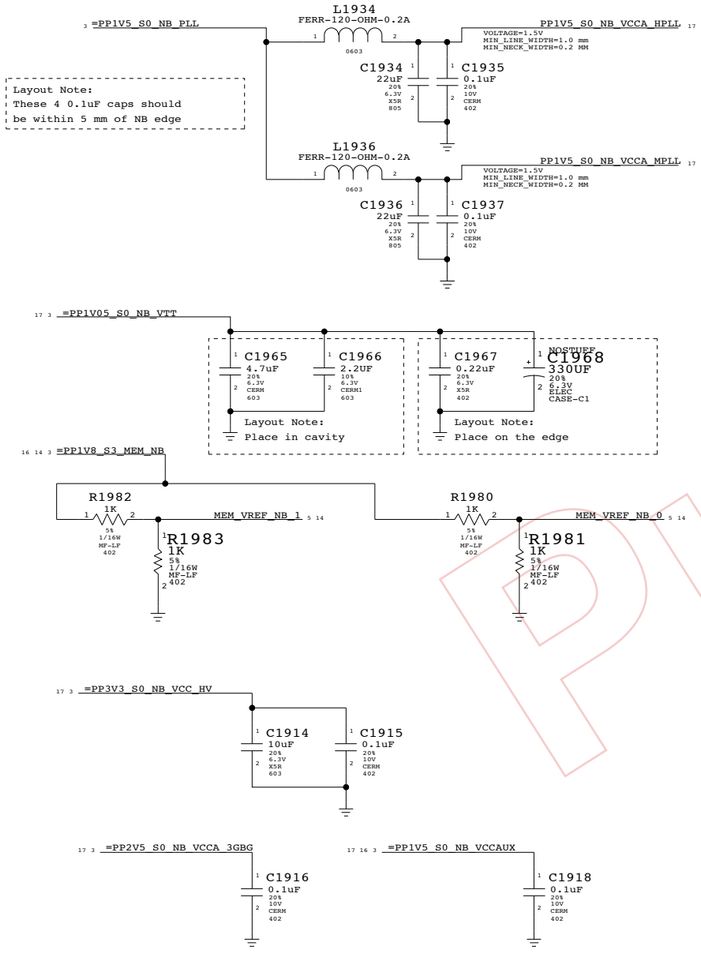
NB Grounds

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

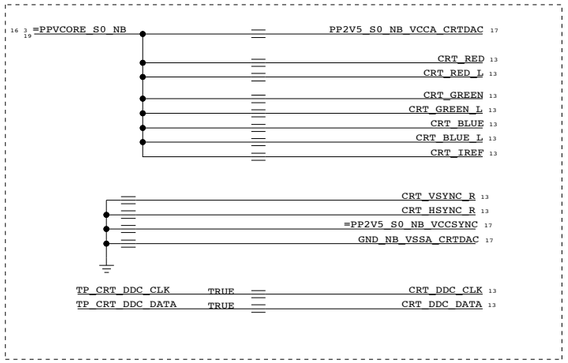
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H

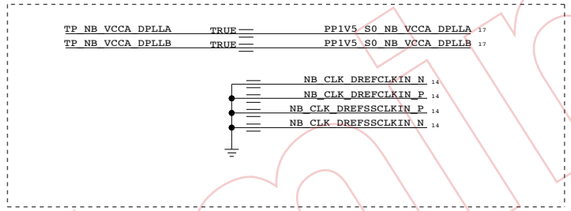
SCALE NONE SHT 18 OF 97



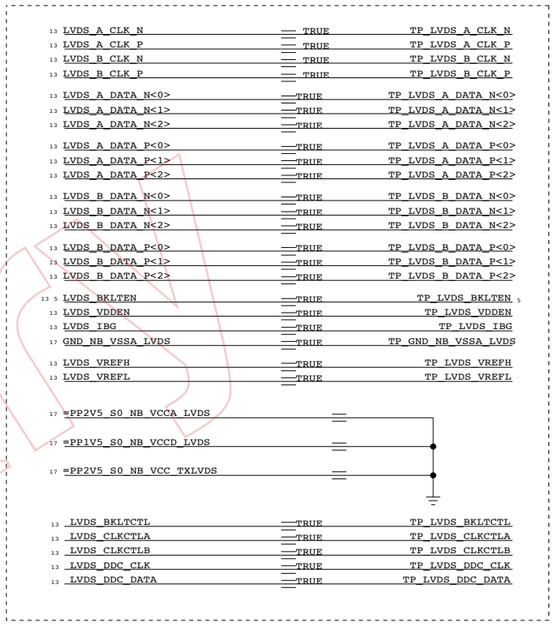
TVOUT DISABLE

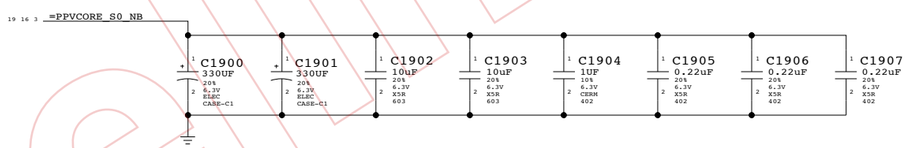


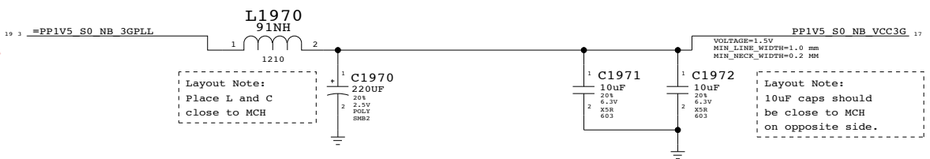
DISPLAY DISABLE

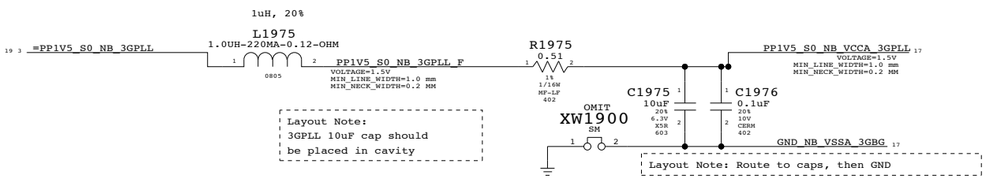


LVDS DISABLE

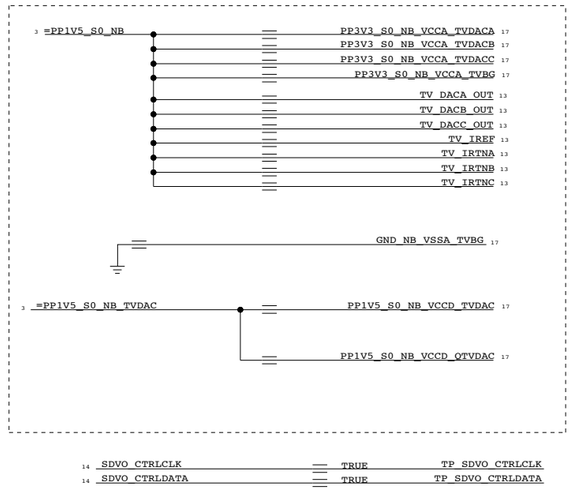








TVOUT DISABLE



NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 19 OF 97	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402
1
2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

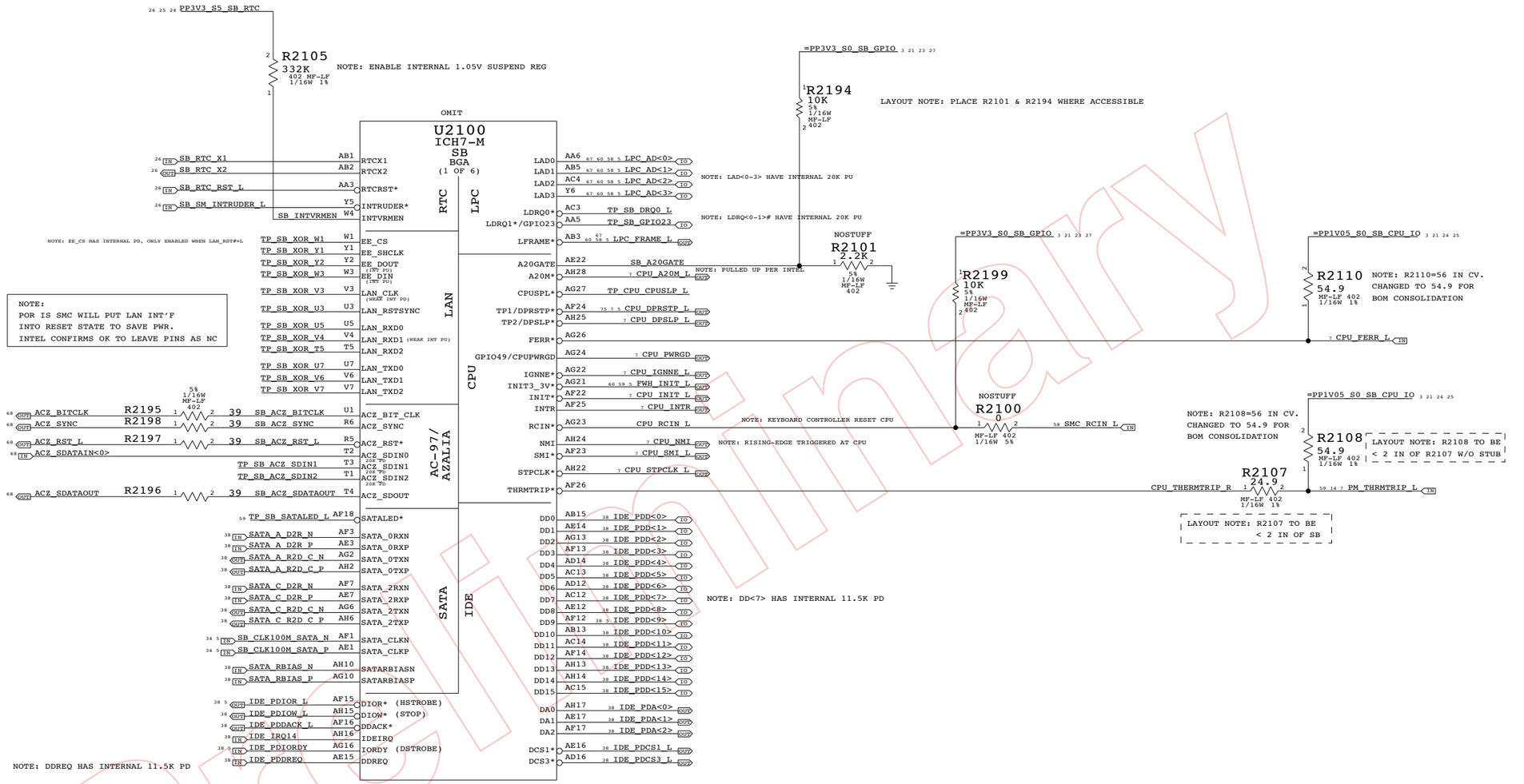
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 20 OF 97	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 21 OF 97	

=PP3V3_S5_SB_USB

R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2222 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402

USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L

SB_GPIO29
SB_GPIO30
SB_GPIO31

=PP3V3_S5_SB_IO

R2205 10K MF-LF 1/16W 402 5%
R2206 NOSTUFF 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%

SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO

OMIT

U2100
ICH7-M
SB
BGA
(3 OF 6)

PCI-EXP

PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N E28
PCIE_A_R2D_C_P E27
PCIE_B_D2R_N H26
PCIE_B_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_C_D2R_N K26
PCIE_C_D2R_P K25
PCIE_C_R2D_C_N J28
PCIE_C_R2D_C_P J27
PCIE_D_D2R_N M26
PCIE_D_D2R_P M25
PCIE_D_R2D_C_N L28
PCIE_D_R2D_C_P L27
PCIE_E_D2R_N P26
PCIE_E_D2R_P P25
PCIE_E_R2D_C_N N28
PCIE_E_R2D_C_P N27
PCIE_F_D2R_N T25
PCIE_F_D2R_P T24
PCIE_F_R2D_C_N R28
PCIE_F_R2D_C_P R27

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6

DMI

DMI0RXN V26
DMI0RXP V25
DMI0TXN U28
DMI0TXP U27
DMI1RXN Y26
DMI1RXP Y25
DMI1TXN W28
DMI1TXP W27
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA28
DMI2TXP AA27
DMI3RXN AD25
DMI3RXP AD24
DMI3TXN AC28
DMI3TXP AC27

DMI0RXN DMI_N2S_N<0>
DMI0RXP DMI_N2S_P<0>
DMI0TXN DMI_S2N_N<0>
DMI0TXP DMI_S2N_P<0>
DMI1RXN DMI_N2S_N<1>
DMI1RXP DMI_N2S_P<1>
DMI1TXN DMI_S2N_N<1>
DMI1TXP DMI_S2N_P<1>
DMI2RXN DMI_N2S_N<2>
DMI2RXP DMI_N2S_P<2>
DMI2TXN DMI_S2N_N<2>
DMI2TXP DMI_S2N_P<2>
DMI3RXN DMI_N2S_N<3>
DMI3RXP DMI_N2S_P<3>
DMI3TXN DMI_S2N_N<3>
DMI3TXP DMI_S2N_P<3>

DMI_CLKN AE28 SB_CLK100M_DMI_N
DMI_CLKP AE27 SB_CLK100M_DMI_P

DMI_ZCOMP C25
DMI_IRCOMP D25

R2203 24.9 1/16W MF-LF 1% 402
DMI_IRCOMP_R

PP1V5_S0_SB_VCC1_5_B

LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB

SPI

SPI_CLK (INT PD) R2
SPI_CS* P6
SPI_ARB (INT PD) P1
SPI_MOSI P5
SPI_MISO P2

USB

USB_A_OC_L D3
USB_B_OC_L C4
USB_C_OC_L D5
USB_D_OC_L D4
USB_E_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
SB_GPIO31 B3

OC0* OC1* OC2* OC3* OC4* OC5*/GPIO29 OC6*/GPIO30 OC7*/GPIO31

USBP0N F1 USB_A_N EXTERNAL 0
USBP0P F2 USB_A_P
USBP1N G4 USB_B_N AIRPORT (MINI-PCIE)
USBP1P G3 USB_B_P
USBP2N H1 USB_C_N EXTERNAL 1
USBP2P H2 USB_C_P
USBP3N J4 USB_D_N CAMERA
USBP3P J3 USB_D_P
USBP4N K1 USB_E_N EXTERNAL 2
USBP4P K2 USB_E_P
USBP5N L4 USB_F_N CF/SD
USBP5P L5 USB_F_P
USBP6N M1 USB_G_N BT
USBP6P M2 USB_G_P
USBP7N N4 USB_H_N IR
USBP7P N3 USB_H_P

NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD

USBRBIAS* D2
USBRBIAS D1
USB_RBIAS_PN

R2204 22.6 1% 1/16W MF-LF 402

VOLTAGE=0

LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB

OMIT

U2100
ICH7-M
SB
BGA
(2 OF 6)

PCI

PCI_AD<0> E18 AD0
PCI_AD<1> C18 AD1
PCI_AD<2> A16 AD2
PCI_AD<3> F18 AD3
PCI_AD<4> E16 AD4
PCI_AD<5> A18 AD5
PCI_AD<6> E17 AD6
PCI_AD<7> A17 AD7
PCI_AD<8> A15 AD8
PCI_AD<9> C14 AD9
PCI_AD<10> E14 AD10
PCI_AD<11> D14 AD11
PCI_AD<12> B12 AD12
PCI_AD<13> C13 AD13
PCI_AD<14> G15 AD14
PCI_AD<15> G13 AD15
PCI_AD<16> E12 AD16
PCI_AD<17> C11 AD17
PCI_AD<18> D11 AD18
PCI_AD<19> A11 AD19
PCI_AD<20> A10 AD20
PCI_AD<21> F11 AD21
PCI_AD<22> F10 AD22
PCI_AD<23> E9 AD23
PCI_AD<24> D9 AD24
PCI_AD<25> B9 AD25
PCI_AD<26> A8 AD26
PCI_AD<27> A6 AD27
PCI_AD<28> C7 AD28
PCI_AD<29> B6 AD29
PCI_AD<30> E6 AD30
PCI_AD<31> D6 AD31

PCI_FRAME_L F16 FRAME*

C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY_L
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL_L
PERR* C9 PCI_PERR_L
PLOCK* E11 PCI_LOCK_L
SERR* B10 PCI_SERR_L
STOP* F15 PCI_STOP_L
TRDY* F14 PCI_TRDY_L

INT I/F

INT_PIRQA_L A3 PIRQA*
INT_PIRQB_L B4 PIRQB*
INT_PIRQC_L C5 PIRQC*
INT_PIRQD_L B5 PIRQD*

GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 ODD_PWR_EN_L

MISC

NOTE: CHANGE SYMBOL TO RSVD[1-9]

TP_SB_XOR_AE5 AE5 RSVD0
TP_SB_XOR_AD5 AD5 RSVD1
TP_SB_XOR_AG4 AG4 RSVD2
TP_SB_XOR_AH4 AH4 RSVD3
TP_SB_XOR_AD9 AD9 RSVD4

RSVD5 AE9 TP_SB_XOR_AE9
RSVD6 AG8 TP_SB_XOR_AG8
RSVD7 AH8 TP_SB_XOR_AH8
RSVD8 F21 TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
MCH_SYNC* AH20 NB_SB_SYNC_L

NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H

REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 PCI_GNT3_L
REQ4*/GPIO22 A13 SB_CRT_TVOUT_MUX NOTE: FWH_WP_L NOT USED
GNT4*/GPIO48 A14 TP_SB_GPIO_48
GPIO1/REQ5* C8 PCI_PME_FW_L
GPIO17/GNT5* D8 BOOT_LPC_SPI_L

(INT 20K PU) PME* B19 TP_PCI_PME_L

=PP3V3_S0_SB

R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402

R2211 1K 5% 1/16W MF-LF 402

BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)

SB BOOT BIOS SELECT

STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT) 11	UNSTUFF	UNSTUFF
PCI 10	UNSTUFF	STUFF
SPI 01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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SIZE D | DRAWING NUMBER 051-7039 | REV. H
SCALE NONE | SHT 22 OF 97

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 3 21 23 27

=PP3V3_S5_SB 3 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

26 25 23 3 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 TO SMB_CLK — C22 SMBCLK
27 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
67 60 58 5 OUT PM_SUS_STAT_L — A27 SUS_STAT*
58 26 IN PM_SYSRST_L — A22 SYS_RST*
14 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

SATA GPIO

GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
38 SATA_C_DET_L IN

CLKS

CLK14 — AC1 — 34 5 SB_CLK14P3M_TIMER IN
CLK48 — B2 — 34 5 SB_CLK48M_USBCTLR IN
SUSCLK — C20 — 50 SUS_CLK_SB OUT

SYS GPIO
PWR MNGT

SLP_S3* — B24 — 79 77 80 58 5 PM_SLP_S3_L OUT
SLP_S4* — D23 — 77 58 5 PM_SLP_S4_L OUT
SLP_S5* — F22 — 58 PM_SLP_S5_L OUT
PWROK — AA4 — 26 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 — 75 14 5 PM_DPRSLPVR OUT
NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING TCN
TP0/BATLOW* — C21 — 58 PM_BATLOW_L IN
(INT 20K PU) PWRBTN* — C23 — 58 PM_PWRBTN_L IN
LAN_RST* — C19 — 58 PM_LAN_ENABLE IN
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4 — 58 PM_RSMRST_L IN

GPIO

GPIO9 — E20 — 58 26 SMS_INT_L IN
GPIO10 — A20 — 58 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 38 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 5 23 60
GPIO24 — R3 — TP_SB_GPIO24
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 23 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*

33 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
34 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23 BIOS_REC — B21 GPIO27
23 FWH_MFG_MODE — E23 GPIO28
67 60 58 5 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
53 41 IN PCIE_WAKE_L — F20 WAKE*
67 60 58 5 TO INT_SERIRQ — AH21 SERIRQ
58 10 IN PM_THRM_L — AF20 THRM*
26 5 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
6 GPU_PRESENT_R — AC21 GPIO6
58 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
58 IN SMC_EXTSMI_L — E21 GPIO8

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 350S AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 3 11

NOSTUFF R2387 10K 1/16W 402 MF-LF 5%
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

R2399 100K 5% 1/16W 402 MF-LF

26 25 23 3 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 10K 1/16W 402 MF-LF 5%

SV_SET_UP 5 23 60
EFI_OK_R

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 3 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
FWH_MFG_MODE 23
BIOS_REC 23
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

=PP3V3_S5_SB 3 23 25 26

R2390 10K 5% 1/16W MF-LF 402
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 3 21 23 27

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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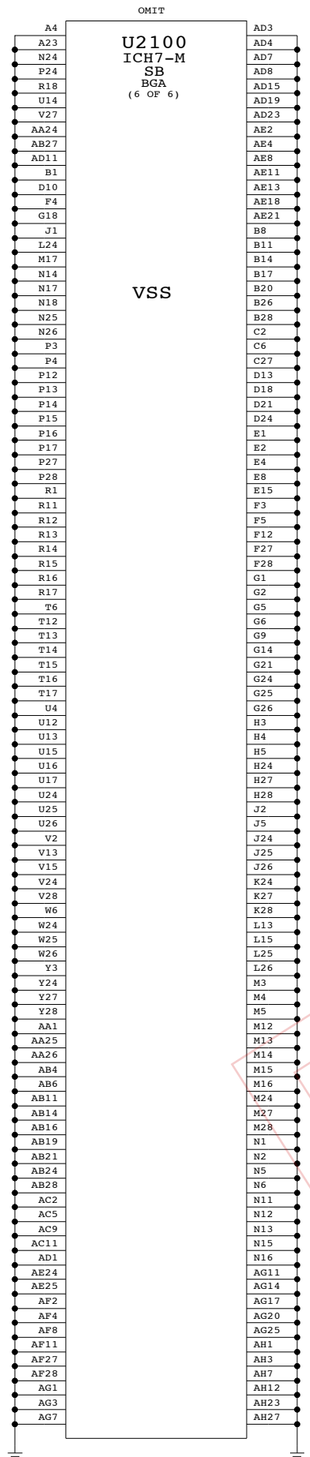
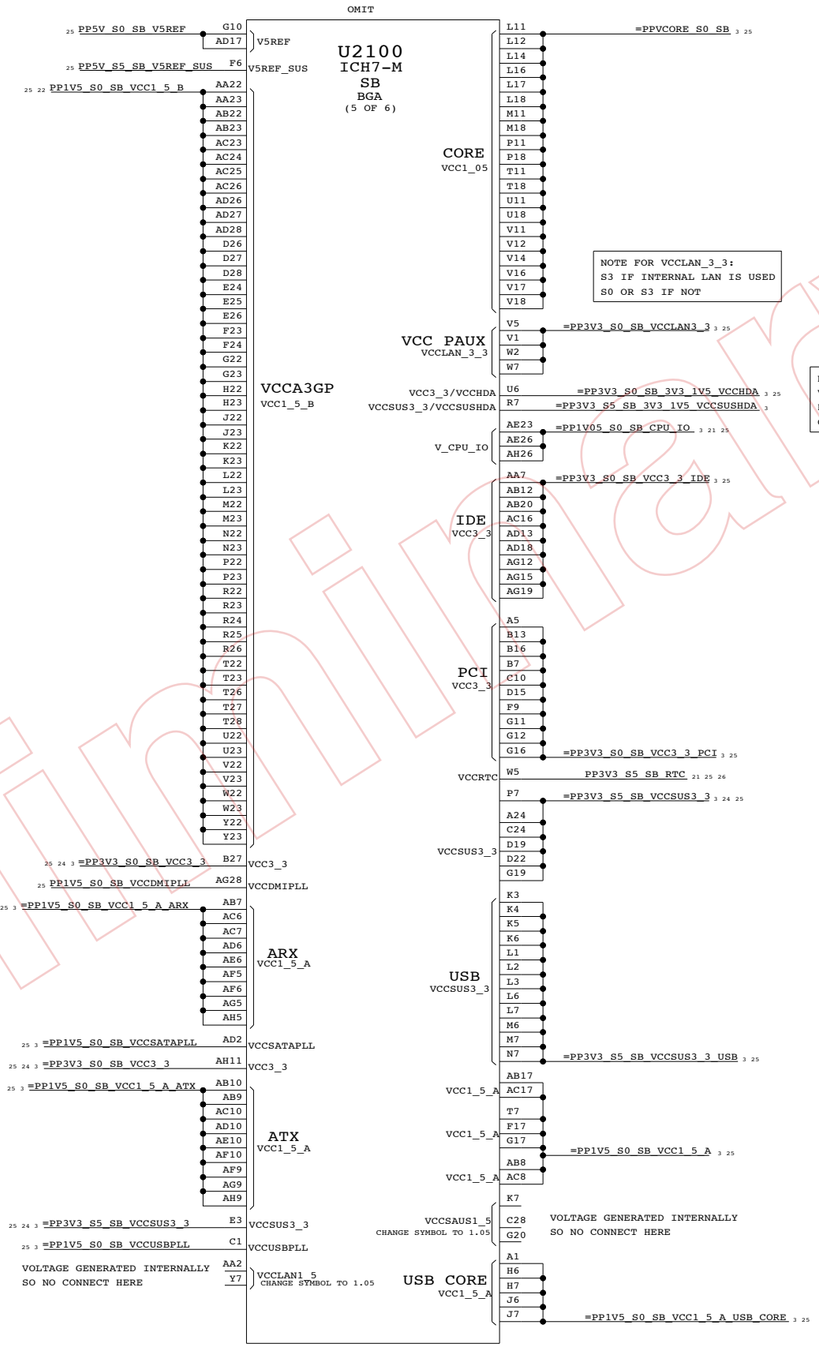
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 23 OF 97	





SB: 4 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

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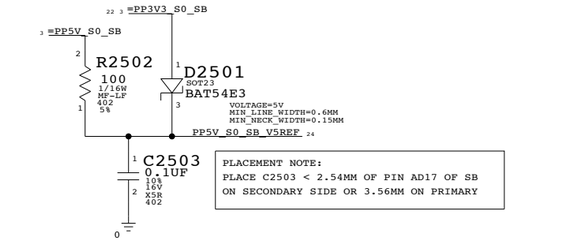
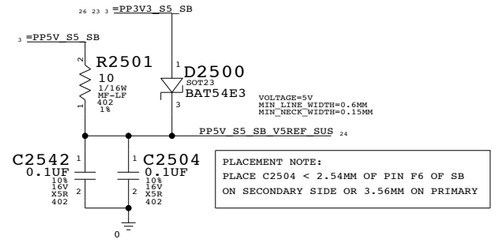
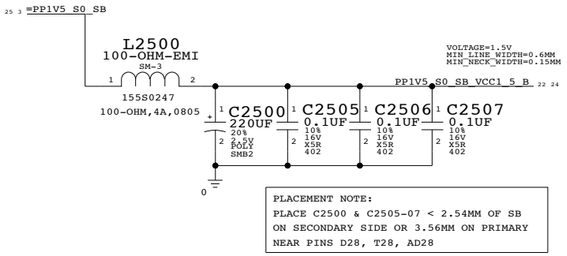
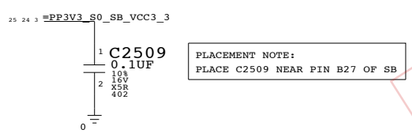
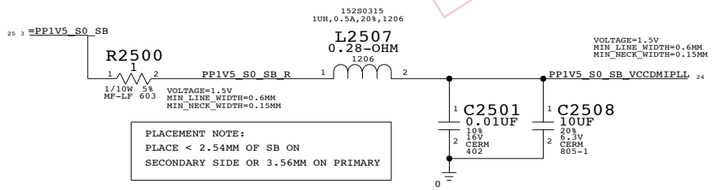
D	051-7039	H
SCALE: NONE	SHT 24 OF 97	

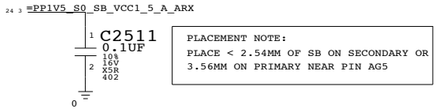


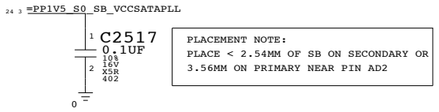


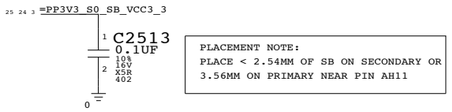


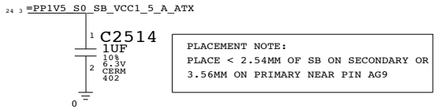


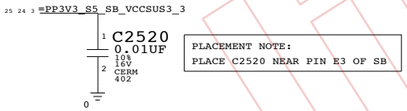


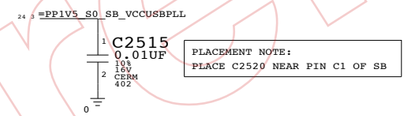


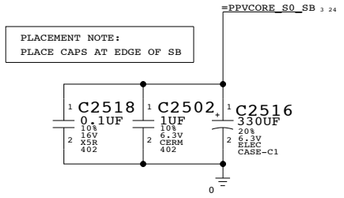


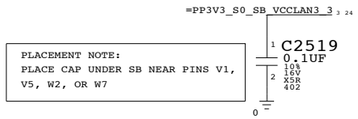


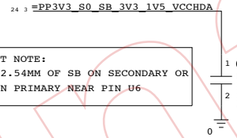


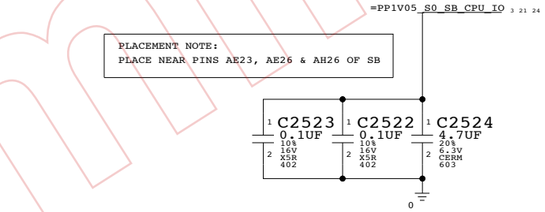


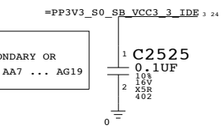


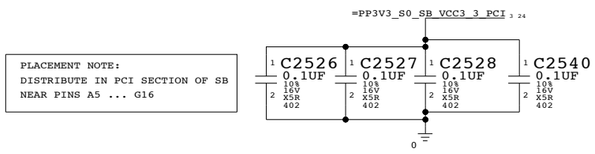


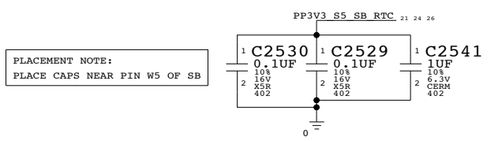


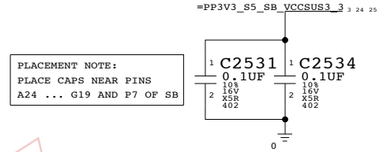


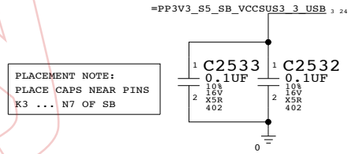


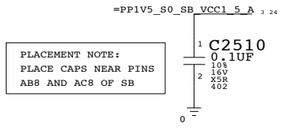


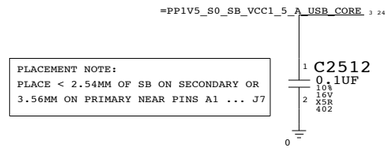












SB:DECOUPLING

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APPLE COMPUTER INC.

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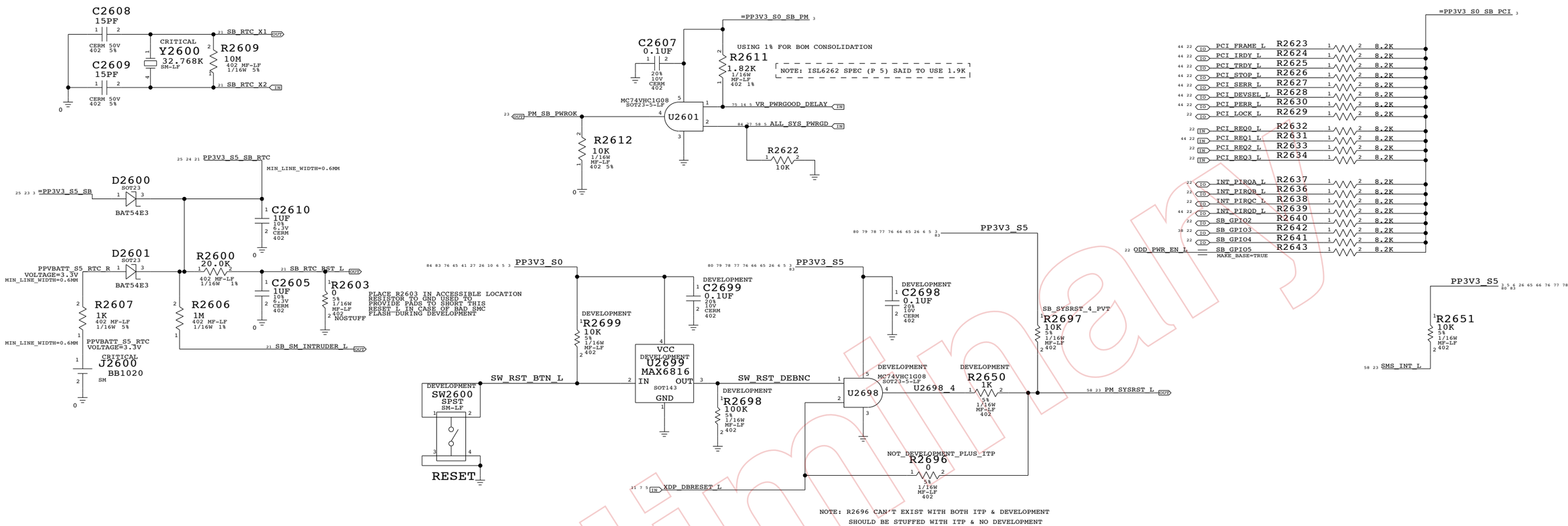

SB: MISC

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APPLE COMPUTER INC.

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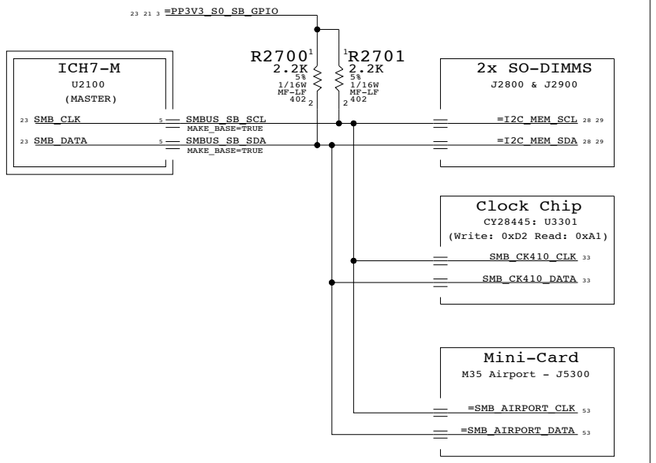
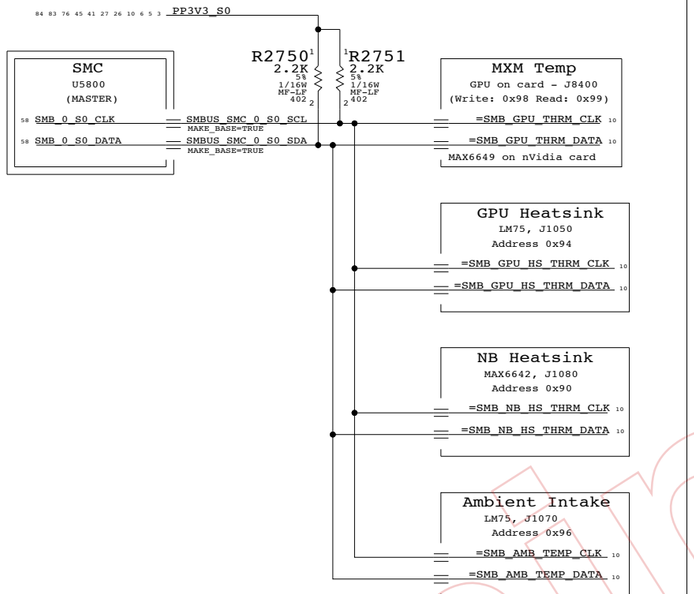
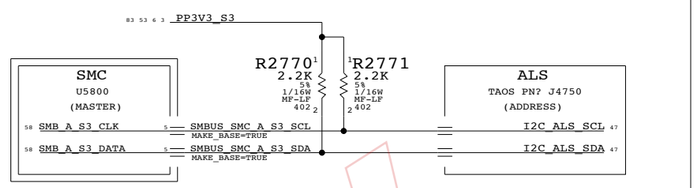
ICH7-M SMBus Connections



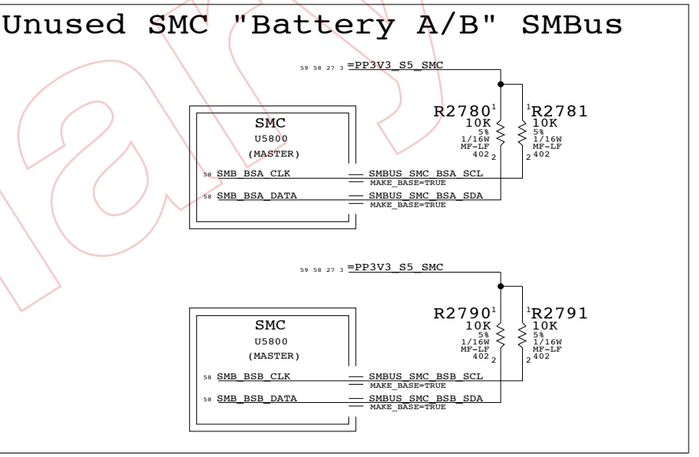
SMC "0" SMBus Connections



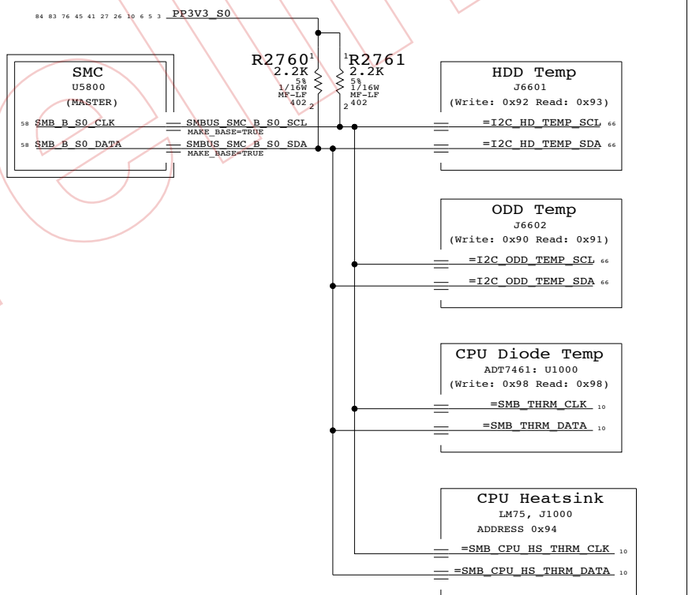
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 27 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

=PP1V8_S3_MEM
R2800 1K 1% 1/16W MF-LF 402
MEM_VREF (VOLTAGE=0.9V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)
R2801 1K 1% 1/16W MF-LF 402

MEM_VREF
C2850 2.2UF 10% 6.3V CERM1 603
C2800 0.1uF 20% 10V CERM 402

J2800

DDR2-SODIMM-STD
CRITICAL
F-RT-SM2

1	VREF		2	VSS0			
3	VSS1		4	DQ4	MEM_A_DQ<4>	15	
5	DQ0	MEM_A_DQ<0>	15	6	DQ5	MEM_A_DQ<5>	15
7	DQ1	MEM_A_DQ<1>	15	8	VSS2		
9	VSS4		10	DM0	MEM_A_DM<0>	15	
11	DQS0*	MEM_A_DQS_N<0>	15	12	VSS5		
13	DQS0	MEM_A_DQS_P<0>	15	14	DQ6	MEM_A_DQ<6>	15
15	VSS6		16	DQ7	MEM_A_DQ<7>	15	
17	DQ2	MEM_A_DQ<2>	15	18	VSS7		
19	DQ3	MEM_A_DQ<3>	15	20	DQ12	MEM_A_DQ<12>	15
21	VSS8		22	DQ13	MEM_A_DQ<13>	15	
23	DQ8	MEM_A_DQ<8>	15	24	VSS9		
25	DQ9	MEM_A_DQ<9>	15	26	DM1	MEM_A_DM<1>	15
27	VSS10		28	VSS11			
29	DQS1*	MEM_A_DQS_N<1>	15	30	CK0	MEM_CLK_P<0>	14
31	DQS1	MEM_A_DQS_P<1>	15	32	CK0*	MEM_CLK_N<0>	14
33	VSS12		34	VSS13			
35	DQ10	MEM_A_DQ<10>	15	36	DQ14	MEM_A_DQ<14>	15
37	DQ11	MEM_A_DQ<11>	15	38	DQ15	MEM_A_DQ<15>	15
39	VSS14		40	VSS15			
KEY							
41	VSS16		42	VSS17			
43	DQ16	MEM_A_DQ<16>	15	44	DQ20	MEM_A_DQ<20>	15
45	DQ17	MEM_A_DQ<17>	15	46	DQ21	MEM_A_DQ<21>	15
47	VSS18		48	VSS19			
49	DQS2*	MEM_A_DQS_N<2>	15	50	NC0	DIMM_OVERTEMP_L	29 59
51	DQS2	MEM_A_DQS_P<2>	15	52	DM2	MEM_A_DM<2>	15
53	VSS21		54	VSS22			
55	DQ18	MEM_A_DQ<18>	15	56	DQ22	MEM_A_DQ<22>	15
57	DQ19	MEM_A_DQ<19>	15	58	DQ23	MEM_A_DQ<23>	15
59	VSS23		60	VSS24			
61	DQ24	MEM_A_DQ<24>	15	62	DQ28	MEM_A_DQ<28>	15
63	DQ25	MEM_A_DQ<25>	15	64	DQ29	MEM_A_DQ<29>	15
65	VSS25		66	VSS26			
67	DM3	MEM_A_DM<3>	15	68	DQS3*	MEM_A_DQS_N<3>	15
69	NC1	NC		70	DQS3	MEM_A_DQS_P<3>	15
71	VSS27		72	VSS28			
73	DQ26	MEM_A_DQ<26>	15	74	DQ30	MEM_A_DQ<30>	15
75	DQ27	MEM_A_DQ<27>	15	76	DQ31	MEM_A_DQ<31>	15
77	VSS29		78	VSS30			
79	CKE0	MEM_CKE<0>	30 14	80	NC/CKE1	MEM_CKE<1>	14 30
81	VDD0		82	VDD1			
83	NC2	NC		84	NC/A15	TP_MEM_A_A<15>	
85	BA2	MEM_A_BS<2>	30 15	86	NC/A14	TP_MEM_A_A<14>	
87	VDD2		88	VDD3			
89	A12	MEM_A_A<12>	30 15	90	A11	MEM_A_A<11>	15 30
91	A9	MEM_A_A<9>	30 15	92	A7	MEM_A_A<7>	15 30
93	A8	MEM_A_A<8>	30 15	94	A6	MEM_A_A<6>	15 30
95	VDD4		96	VDD5			
97	A5	MEM_A_A<5>	30 15	98	A4	MEM_A_A<4>	15 30
99	A3	MEM_A_A<3>	30 15	100	A2	MEM_A_A<2>	15 30
101	A1	MEM_A_A<1>	30 15	102	A0	MEM_A_A<0>	15 30
103	VDD6		104	VDD7			
105	A10/AP	MEM_A_A<10>	30 15	106	BA1	MEM_A_BS<1>	15 30
107	BA0	MEM_A_BS<0>	30 15	108	RAS*	MEM_A_RAS_L	15 30
109	WE*	MEM_A_WE_L	30 15	110	S0*	MEM_CS_L<0>	14 30
111	VDD8		112	VDD9			
113	CAS*	MEM_A_CAS_L	30 15	114	ODT0	MEM_ODT<0>	14 30
115	NC/S1*	MEM_CS_L<1>	30 14	116	NC/A13	MEM_A_A<13>	15 30
117	VDD10		118	VDD11			
119	NC/ODT1	MEM_ODT<1>	30 14	120	NC3	NC	
121	VSS31		122	VSS32			
123	DQ32	MEM_A_DQ<32>	15	124	DQ36	MEM_A_DQ<36>	15
125	DQ33	MEM_A_DQ<33>	15	126	DQ37	MEM_A_DQ<37>	15
127	VSS33		128	VSS34			
129	DQS4*	MEM_A_DQS_N<4>	15	130	DM4	MEM_A_DM<4>	15
131	DQS4	MEM_A_DQS_P<4>	15	132	VSS35		
133	VSS36		134	DQ38	MEM_A_DQ<38>	15	
135	DQ34	MEM_A_DQ<34>	15	136	DQ39	MEM_A_DQ<39>	15
137	DQ35	MEM_A_DQ<35>	15	138	VSS37		
139	VSS38		140	DQ44	MEM_A_DQ<44>	15	
141	DQ40	MEM_A_DQ<40>	15	142	DQ45	MEM_A_DQ<45>	15
143	DQ41	MEM_A_DQ<41>	15	144	VSS39		
145	VSS40		146	DQS5*	MEM_A_DQS_N<5>	15	
147	DM5	MEM_A_DM<5>	15	148	DQS5	MEM_A_DQS_P<5>	15
149	VSS41		150	VSS42			
151	DQ42	MEM_A_DQ<42>	15	152	DQ46	MEM_A_DQ<46>	15
153	DQ43	MEM_A_DQ<43>	15	154	DQ47	MEM_A_DQ<47>	15
155	VSS43		156	VSS44			
157	DQ48	MEM_A_DQ<48>	15	158	DQ52	MEM_A_DQ<52>	15
159	DQ49	MEM_A_DQ<49>	15	160	DQ53	MEM_A_DQ<53>	15
161	VSS45		162	VSS46			
163	NC_TEST	NC		164	CK1	MEM_CLK_P<1>	14
165	VSS47		166	CK1*	MEM_CLK_N<1>	14	
167	DQS6*	MEM_A_DQS_N<6>	15	168	VSS48		
169	DQS6	MEM_A_DQS_P<6>	15	170	DM6	MEM_A_DM<6>	15
171	VSS49		172	VSS50			
173	DQ50	MEM_A_DQ<50>	15	174	DQ54	MEM_A_DQ<54>	15
175	DQ51	MEM_A_DQ<51>	15	176	DQ55	MEM_A_DQ<55>	15
177	VSS51		178	VSS52			
179	DQ56	MEM_A_DQ<56>	15	180	DQ60	MEM_A_DQ<60>	15
181	DQ57	MEM_A_DQ<57>	15	182	DQ61	MEM_A_DQ<61>	15
183	VSS53		184	VSS54			
185	DM7	MEM_A_DM<7>	15	186	DQS7*	MEM_A_DQS_N<7>	15
187	VSS55		188	DQS7	MEM_A_DQS_P<7>	15	
189	DQ58	MEM_A_DQ<58>	15	190	VSS56		
191	DQ59	MEM_A_DQ<59>	15	192	DQ62	MEM_A_DQ<62>	15
193	VSS57		194	DQ63	MEM_A_DQ<63>	15	
195	SDA	=I2C_MEM_SDA	29 27	196	VSS58		
197	SCL	=I2C_MEM_SCL	29 27	198	SA0	ADDR=0xA0(WR)/0xA1(RD)	
199	VDDSPD	=PPSPD_S0_MEM	29 3	200	SA1		
201	GND						
202	GND						
203	GND						
204	GND						
205	GND						

516S0403

SOME ANCHOR PINS CONNECTED TO NETS TO IMPROVE PLANE FOUR

=PPSPD_S0_MEM
C2851 2.2UF 10% 6.3V CERM1 603
C2852 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM
C2853 10UF 20% 6.3V X5R 603

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM
C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603
C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402
C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402
C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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SCALE: NONE	SHT 28 OF 97	

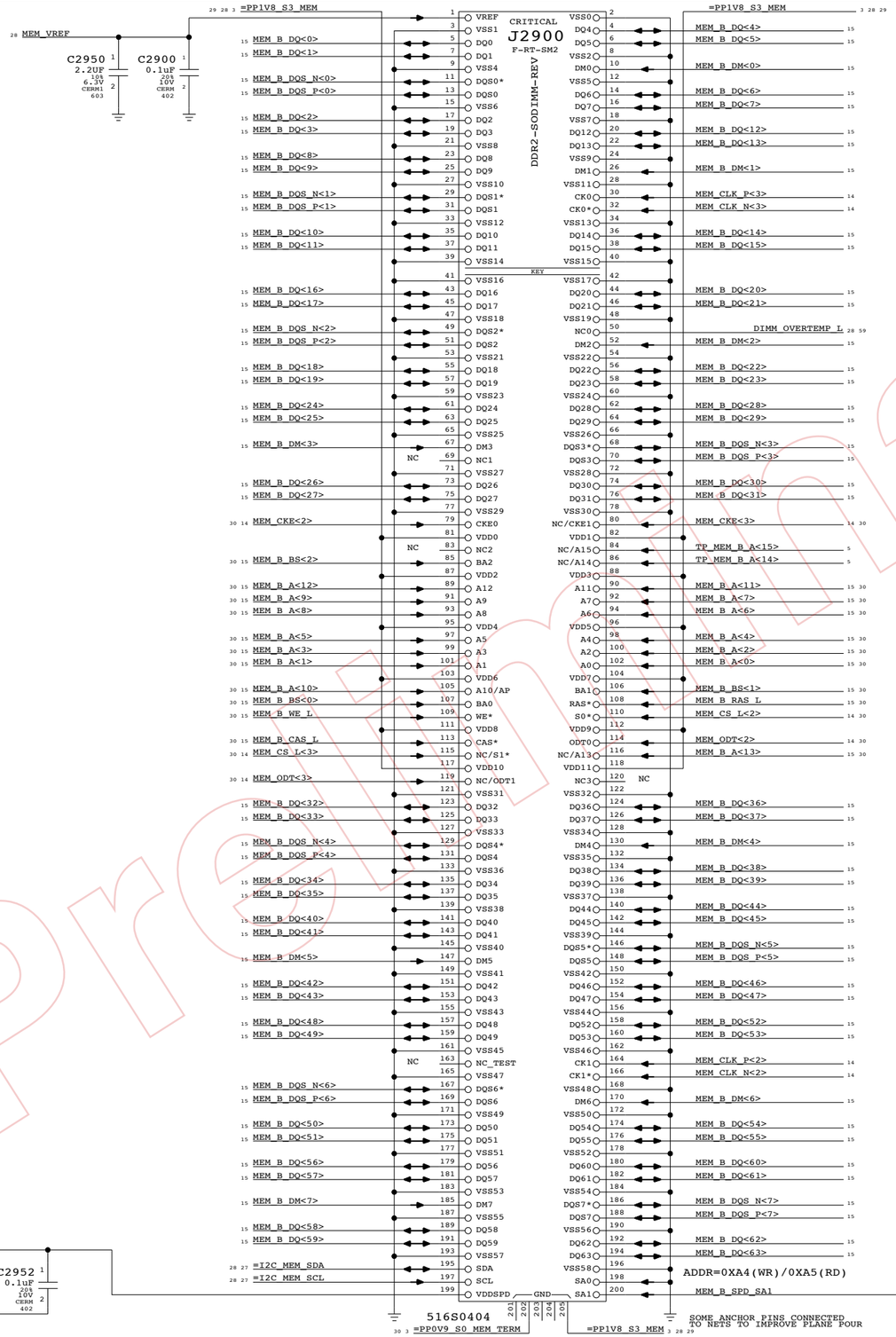
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

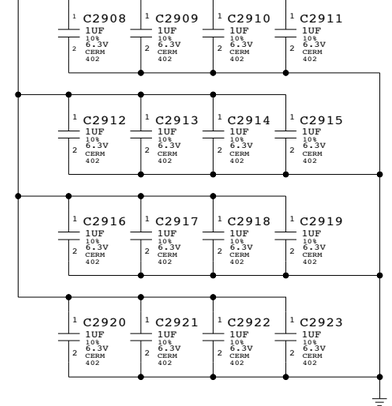
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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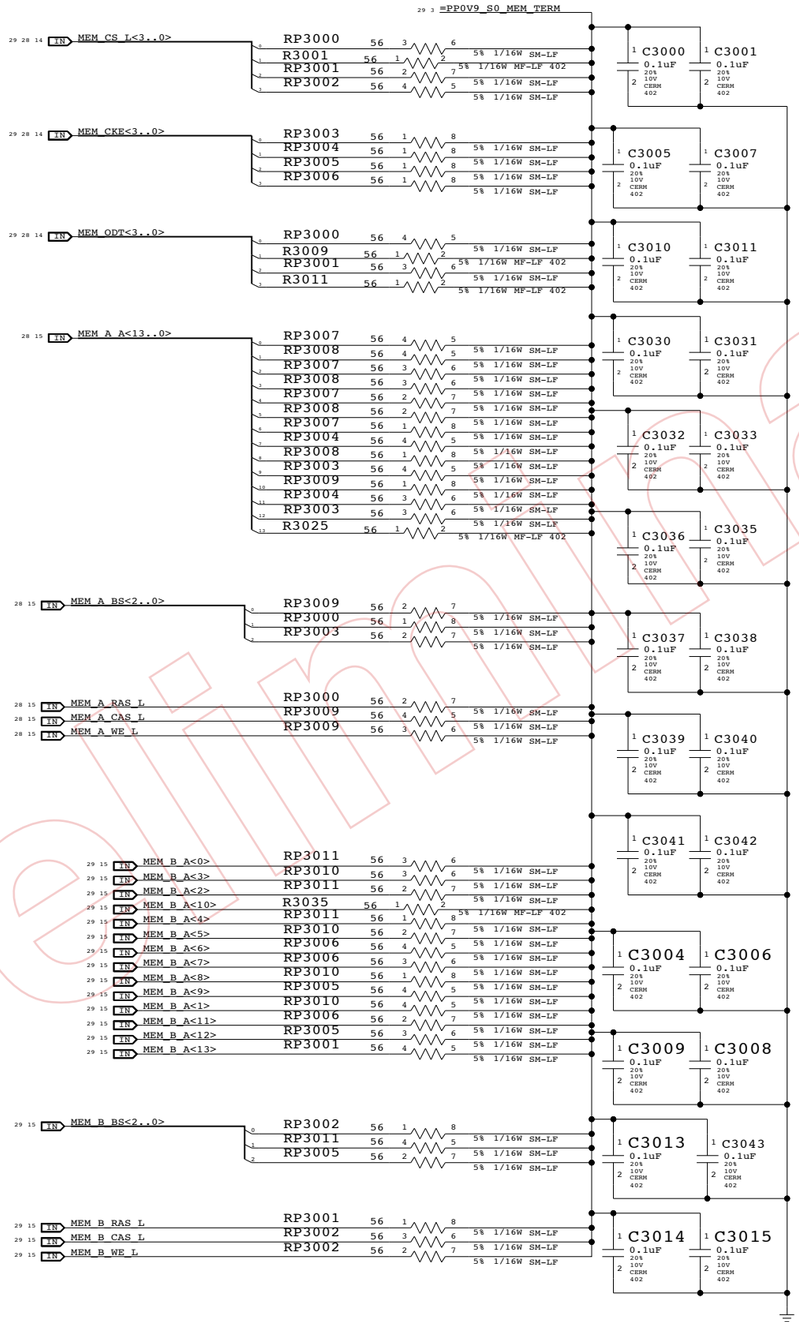
SCALE: NONE	SHT 29 OF 97	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 30 OF 97	

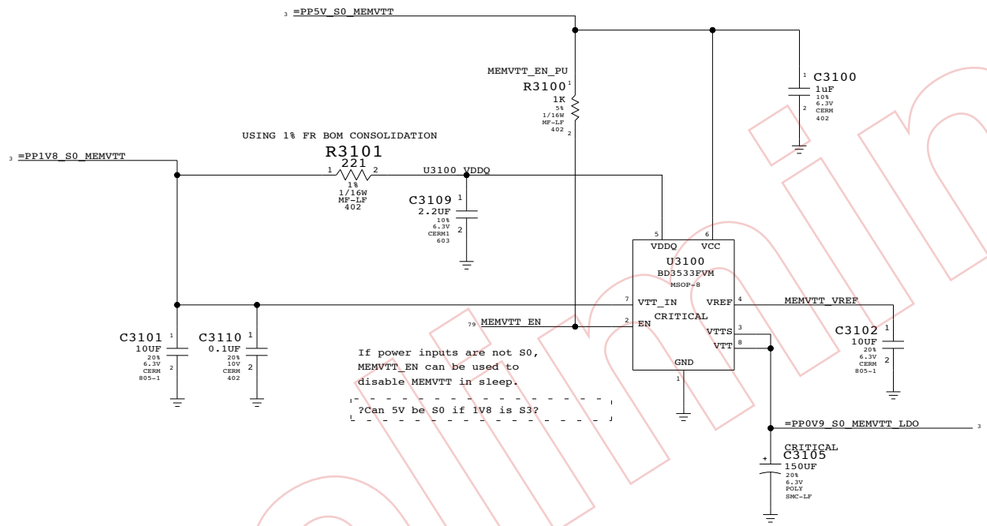
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator

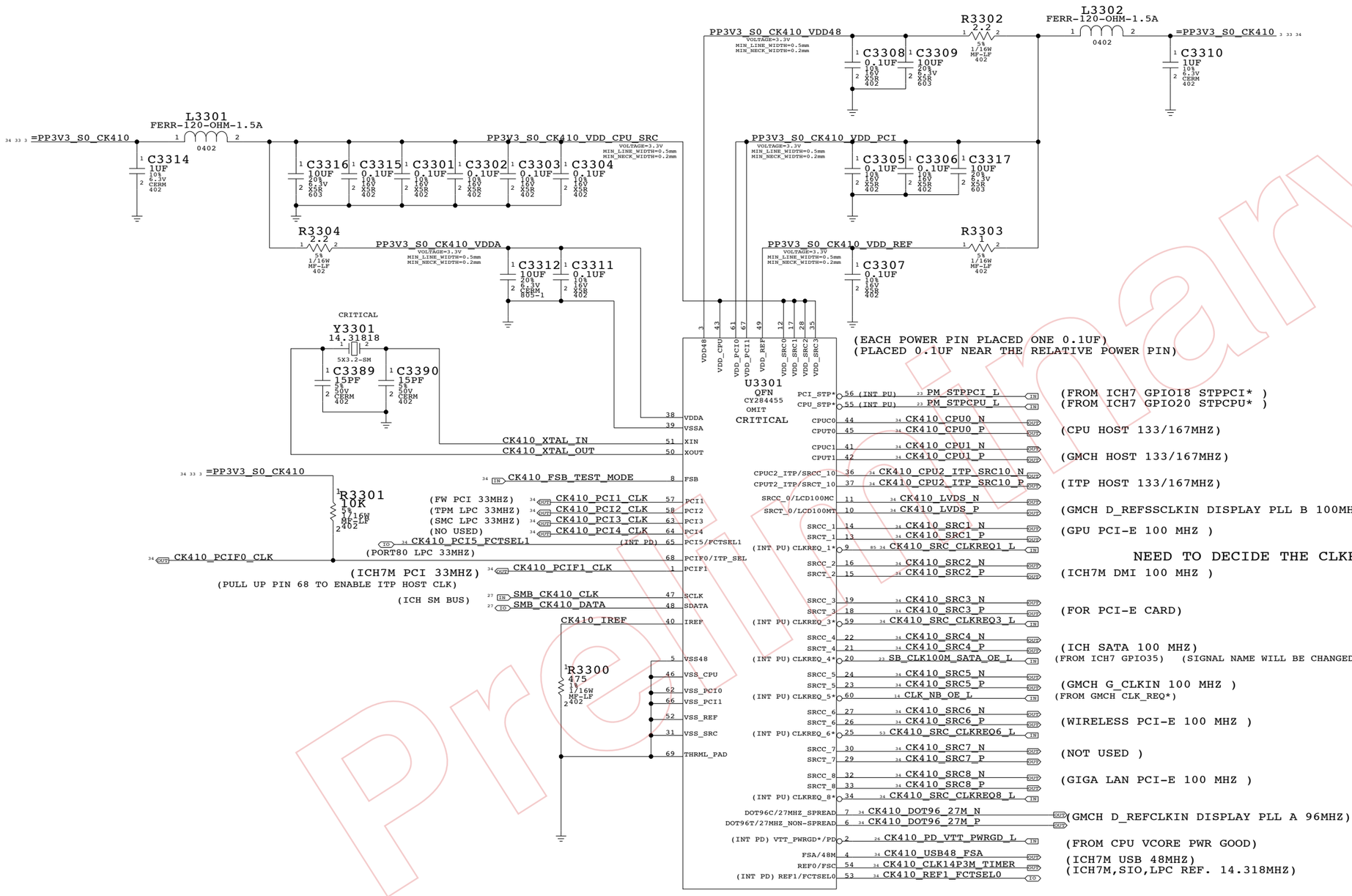


Memory Vtt Supply

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 31 OF 97	



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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D	051-7039	H
SCALE: NONE	SHT 33 OF 97	

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

80 34 5 3 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<0>

34 CK410_FSA

R3454 0 5% 1/16W MF-LF 402 — NOSTUFF R3452 56 5% 1/16W MF-LF 402

R3455 1K 1/16W 5% MF-LF 402

7 CPU_BSEL<0>

80 34 5 3 PP1V05_S0

R3456 1K 5% 1/16W MF-LF 402

R3458 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<1>

33 CK410_FSB_TEST_MODE

R3459 0 5% 1/16W MF-LF 402 — NOSTUFF R3457 0 5% 1/16W MF-LF 402

7 CPU_BSEL<1>

80 34 5 3 PP1V05_S0

R3460 1K 5% 1/16W MF-LF 402

R3462 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<2>

34 CK410_FSC

R3463 0 5% 1/16W MF-LF 402 — NOSTUFF R3461 0 5% 1/16W MF-LF 402

7 CPU_BSEL<2>

=PP3V3_S0_CK410 3 33

33 CK410_PCI5_FCTSEL1 — R3499 1K 1/16W 5% MF-LF 402

R3497 2.2K 5% 1/16W MF-LF 402 — CK410_FSC 34

33 CK410_CLK14P3M_TIMER — R3498 33 1/16W 5% MF-LF 402 — SB_CLK14P3M_TIMER 5 23

33 CK410_REF1_FCTSEL0 — R3496 33 — TP_CLK14P3M_SPARE

R3451 2.2K 5% 1/16W MF-LF 402 — CK410_FSA 34

33 CK410_USB48_FSA — R3400 33 1/16W 5% MF-LF 402 — SB_CLK48M_USBCTLR 5 23

33 CK410_PCI4_CLK — R3406 33 — TP_PCI_CLK_SPARE

33 CK410_PCI3_CLK — R3405 33 — PCI_CLK_SMC 5 58

33 CK410_PCI2_CLK — R3404 33 NOSTUFF — PCI_CLK_TPM 47

33 CK410_PCI1_CLK — R3403 33 — PCI_CLK_FW 5 44

33 CK410_PCIF1_CLK — R3401 33 — PCI_CLK_SB 5 22

33 CK410_PCIF0_CLK — R3402 33 — PCI_CLK_PORT80 5 60

TPM CLOCK IS TURNED OFF IN SW AND RESISTOR NOSTUFF

33 CK410_SRC3_P — 33 — R3492 — SPARE_SRC3_P — R3488 49.9

33 CK410_SRC3_N — 33 — R3491 — SPARE_SRC3_N — R3487 49.9

33 CK410_SRC7_P — 33 — R3490 — SPARE_SRC7_P — R3486 49.9

33 CK410_SRC7_N — 33 — R3489 — SPARE_SRC7_N — R3485 49.9

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

85 33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) — R3495 NOSTUFF 1K

33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) — R3494 1K

33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) — R3493 1K

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

33 CK410_CPU1_P — 33 — R3407 — 12 FSB_CLK_NB_P — R3429 1% 402 1/16W MF-LF 49.9

33 CK410_CPU1_N — 33 — R3408 — 12 FSB_CLK_NB_N — R3430 1% 402 1/16W MF-LF 49.9

33 CK410_CPU0_P — 33 — R3409 — 7 FSB_CLK_CPU_P — R3431 1% 402 1/16W MF-LF 49.9

33 CK410_CPU0_N — 33 — R3410 — 7 FSB_CLK_CPU_N — R3432 1% 402 1/16W MF-LF 49.9

33 CK410_CPU2_ITP_SRC10_P — 33 — R3411 — 11 5 CPU_XDP_CLK_P — MAKE_BASE=TRUE FSB_CLK_XDP_P — R3433 1% 402 1/16W MF-LF 49.9

33 CK410_CPU2_ITP_SRC10_N — 33 — R3412 — 11 5 CPU_XDP_CLK_N — FSB_CLK_XDP_N MAKE_BASE=TRUE — R3434 1% 402 1/16W MF-LF 49.9

33 CK410_SRC6_P — 33 — R3413 — 53 AIRPORT_CLK100M_PCIE_P — R3435 1% 402 1/16W MF-LF 49.9

33 CK410_SRC6_N — 33 — R3414 — 53 AIRPORT_CLK100M_PCIE_N — R3436 1% 402 1/16W MF-LF 49.9

33 CK410_SRC5_P — 33 — R3415 — 14 NB_CLK100M_GCLKIN_P — R3438 1% 402 1/16W MF-LF 49.9

33 CK410_SRC5_N — 33 — R3416 — 14 NB_CLK100M_GCLKIN_N — R3437 1% 402 1/16W MF-LF 49.9

33 CK410_SRC4_P — 33 — R3417 — 21 5 SB_CLK100M_SATA_P — R3439 1% 402 1/16W MF-LF 49.9

33 CK410_SRC4_N — 33 — R3418 — 21 5 SB_CLK100M_SATA_N — R3440 1% 402 1/16W MF-LF 49.9

33 CK410_SRC2_P — 33 — R3419 — 22 SB_CLK100M_DMI_P — R3442 1% 402 1/16W MF-LF 49.9

33 CK410_SRC2_N — 33 — R3420 — 22 SB_CLK100M_DMI_N — R3441 1% 402 1/16W MF-LF 49.9

33 CK410_SRC8_P — 33 — R3421 — 41 ENET_CLK100M_PCIE_P — R3443 1% 402 1/16W MF-LF 49.9

33 CK410_SRC8_N — 33 — R3422 — 41 ENET_CLK100M_PCIE_N — R3444 1% 402 1/16W MF-LF 49.9

33 CK410_SRC1_P — 33 — R3423 — 85 GPU_CLK100M_PCIE_P — R3446 1% 402 1/16W MF-LF 49.9

33 CK410_SRC1_N — 33 — R3424 — 85 GPU_CLK100M_PCIE_N — R3445 1% 402 1/16W MF-LF 49.9

33 CK410_LVDS_P = MAKE_BASE=TRUE TP_CK410_LVDS_P

33 CK410_LVDS_N = MAKE_BASE=TRUE TP_CK410_LVDS_N

33 CK410_DOT96_27M_N = MAKE_BASE=TRUE TP_CK410_27M_SPREAD

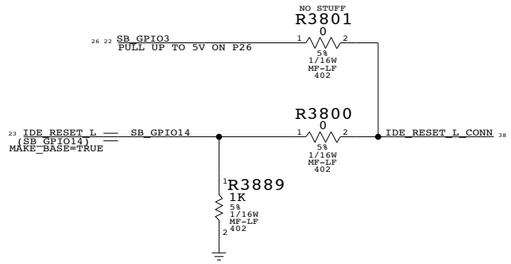
33 CK410_DOT96_27M_P = MAKE_BASE=TRUE TP_CK410_27M_NONSPREAD

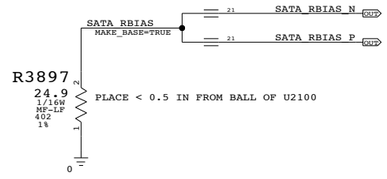
CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

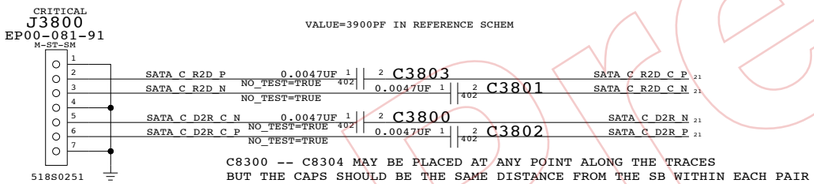
APPLE COMPUTER INC.

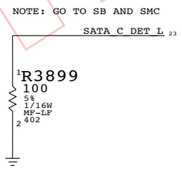
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 34 OF 97	

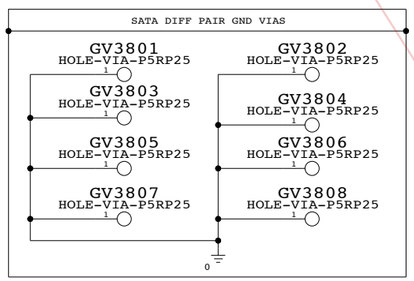




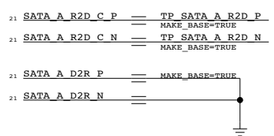
SATA CONNECTOR



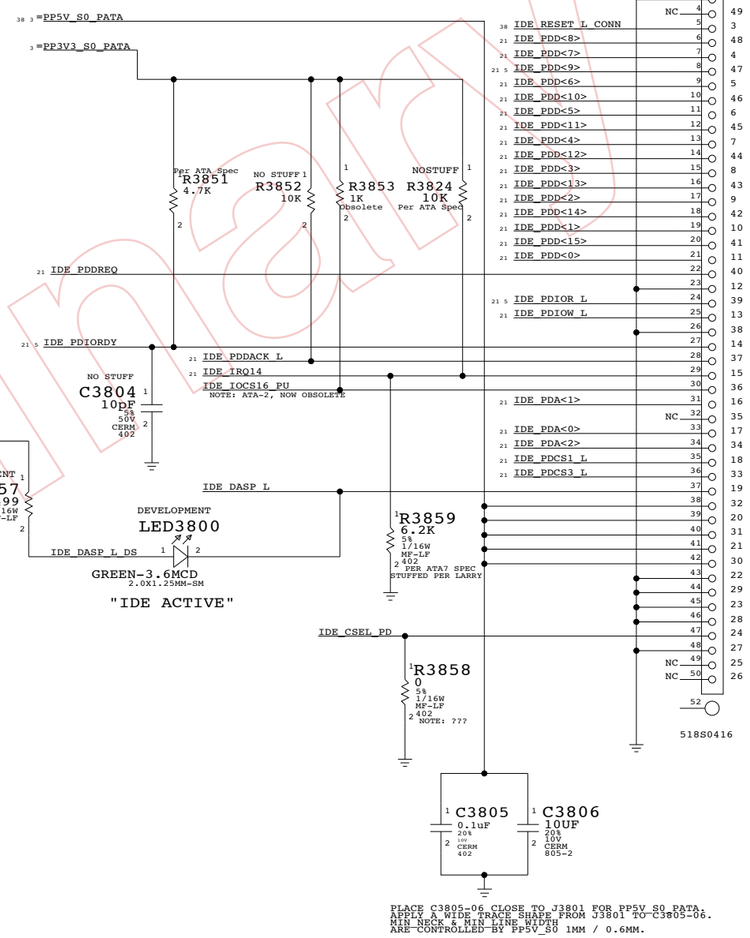




SATA PORT 0 IS NOT USED



PATA (ODD) CONNECTOR



Disk Connectors

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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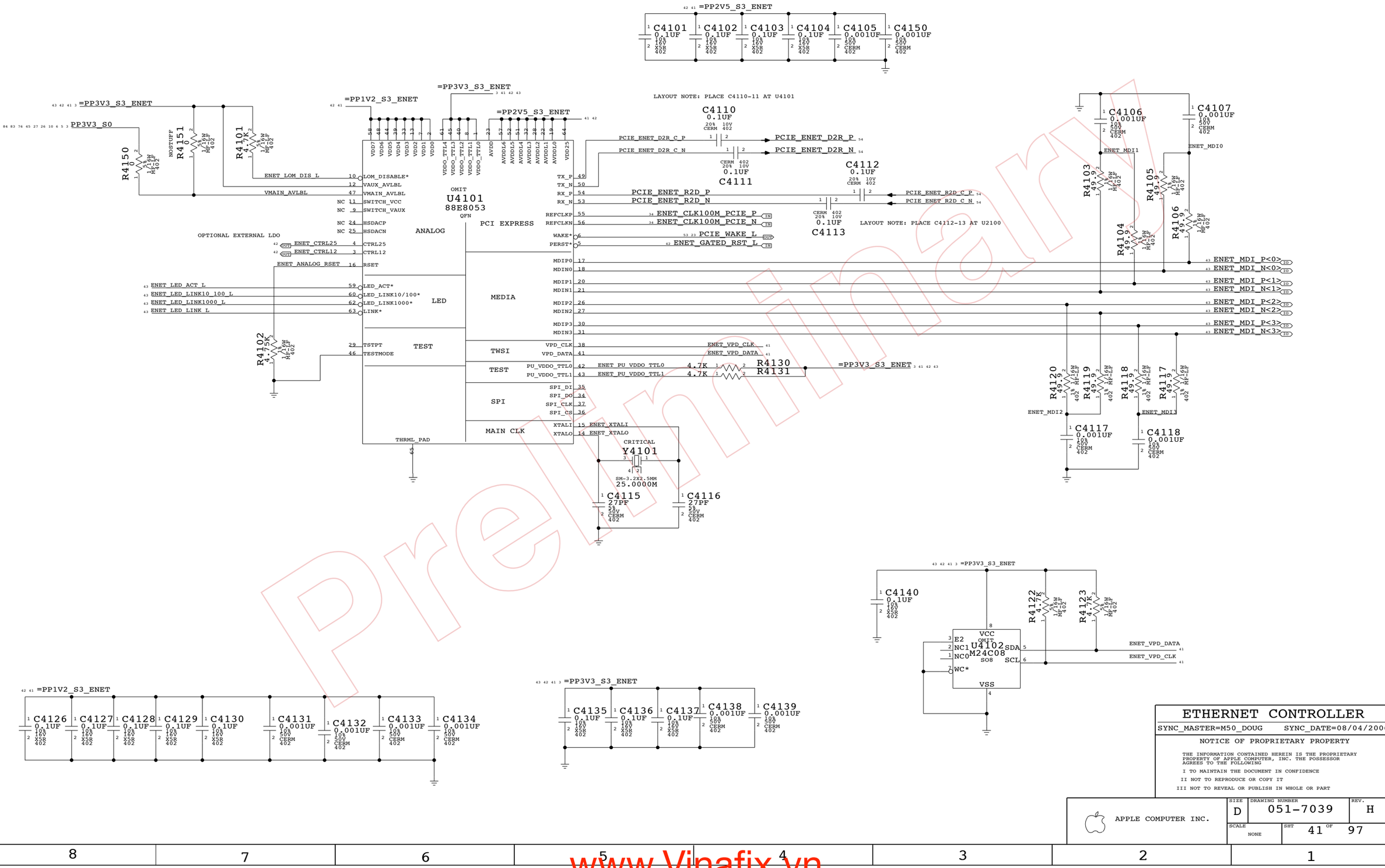
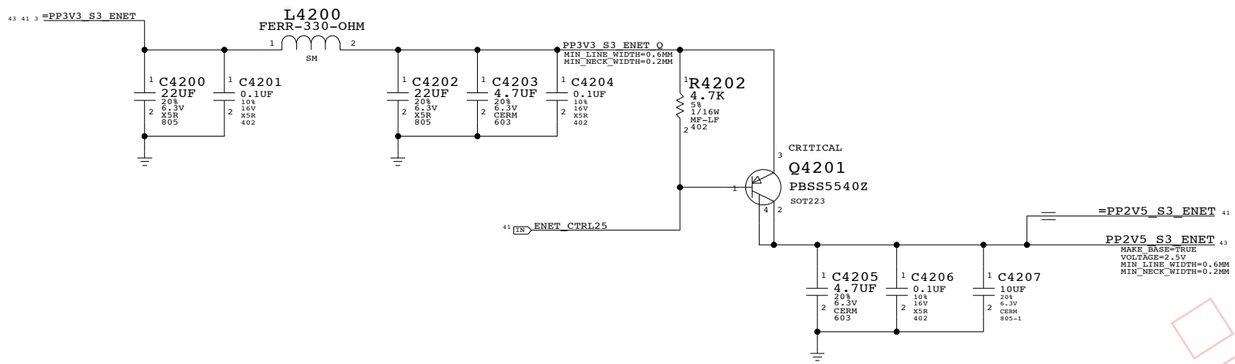
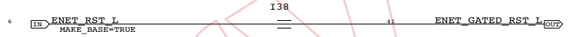
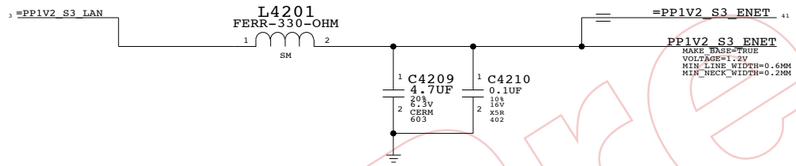
D	051-7039	H
SCALE: NONE	SHT 38 OF 97	









ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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D	051-7039	H
SCALE: NONE	SHT 42 OF 97	

RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED

42 PP2V5_S3_ENET — R4300 0 5% 1/8W MF-LF 805 — PP2V5_ENET_CTAP

MIN_LINE_WIDTH=0.30mm
MIN_NECK_WIDTH=0.10mm
VOLTAGE=2.5V

C4300 0.1UF 20% 10V CERM 402

C4301 0.001UF 10% 50V CERM 402

6 GND_CHASSIS_RJ45

C4304 0.001UF 10% 50V CERM 402

CRITICAL
(514-0331)
J4300
RJ45-M51
F-ANG-TH

PRIMARY

13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12

1CT:1CT — 75 OHM (x4)

SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8

RJ45
CABLE SIDE

RJ45
CHIP SIDE

SHIELD 1000PF, 2000V

41 10 ENET_MDI_P<0>
41 10 ENET_MDI_N<0>
41 10 ENET_MDI_P<1>
41 10 ENET_MDI_N<1>
41 10 ENET_MDI_P<2>
41 10 ENET_MDI_N<2>
41 10 ENET_MDI_P<3>
41 10 ENET_MDI_N<3>

MARVELL DOES NOT REQUIRE/RECOMMEND ANY SERIES TERMINATIONS HERE

C4305 0.001UF 10% 50V CERM 402

42 41 3 =PP3V3_S3_ENET

DEVELOPMENT R4301 330 5% 1/10W MF-LF 603 — LED4300_1
DEVELOPMENT R4302 330 5% 1/10W MF-LF 603 — LED4301_1
DEVELOPMENT R4303 330 5% 1/10W MF-LF 603 — LED4302_1
DEVELOPMENT R4304 330 5% 1/10W MF-LF 603 — LED4303_1

DEVELOPMENT LED4300 GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT LED4301 GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT LED4302 GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT LED4303 GREEN-3.6MCD 2.0X1.25MM-SM

41 ENET_LED_ACT_L MAKE_BASE=TRUE
41 ENET_LED_LINK10_100_L MAKE_BASE=TRUE
41 ENET_LED_LINK1000_L MAKE_BASE=TRUE
41 ENET_LED_LINK_L MAKE_BASE=TRUE

ETHERNET CONNECTOR

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

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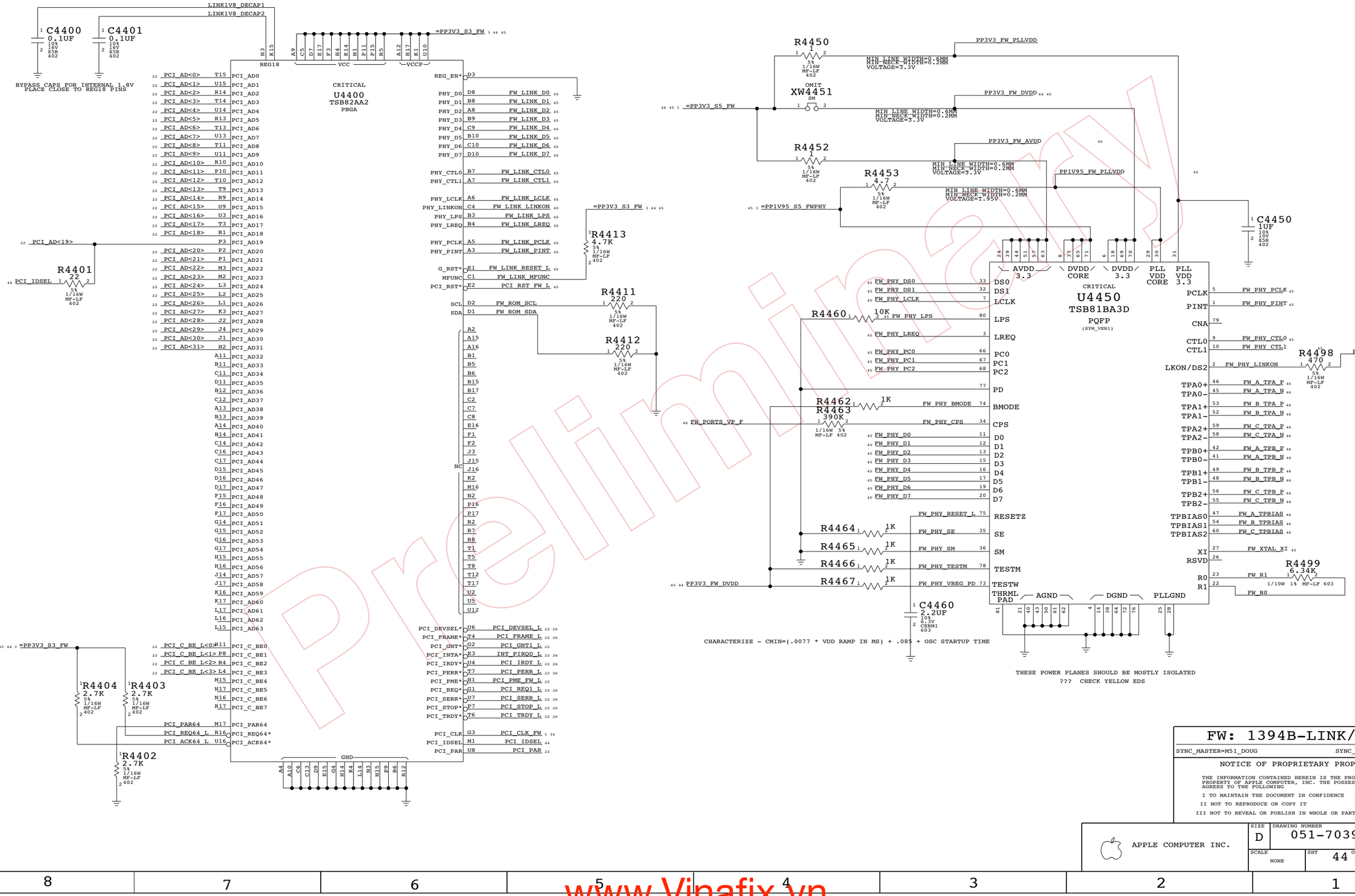
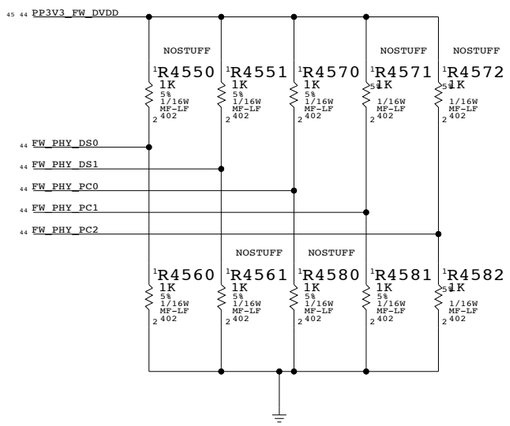
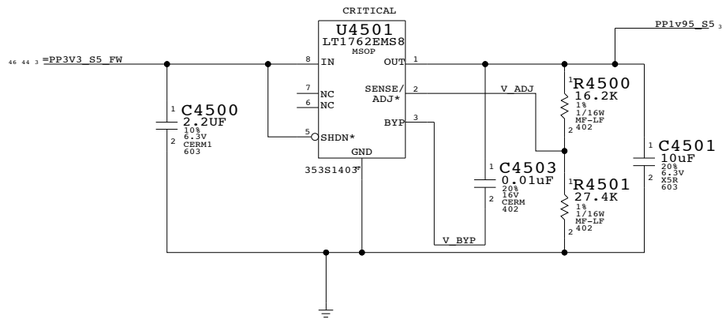
D	051-7039	H
SCALE: NONE	SHT 43 OF 97	



1394 PHY DATA/STROBE AND POWER CLASS OPTIONS



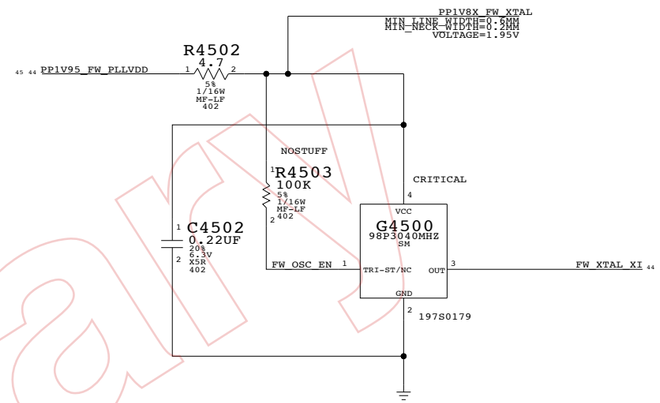
1394 PHY 1.95V REGULATOR



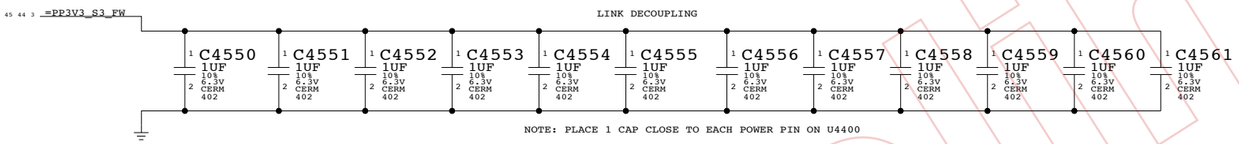
VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V

1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION

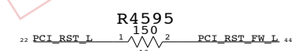


LINK DECOUPLING

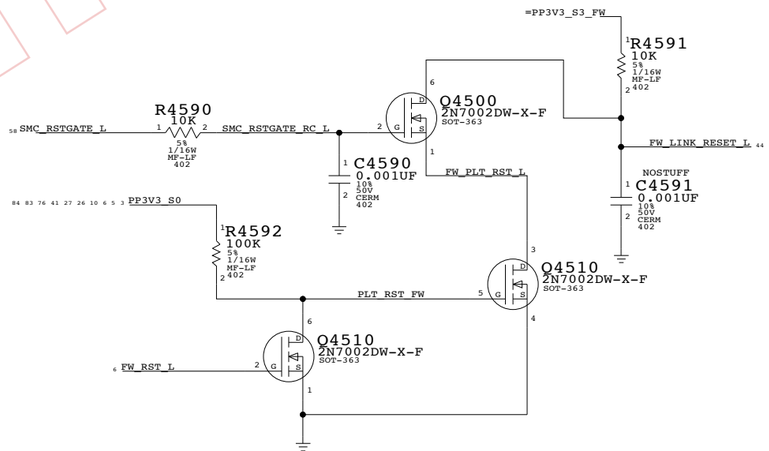


NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

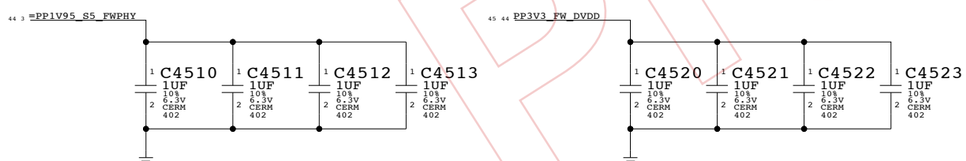
1394 LINK POWER ON RESET AND PCI RESET

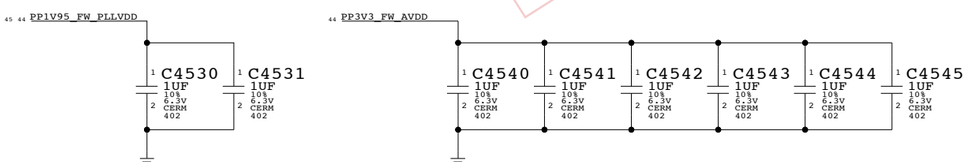


NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT



PHY DECOUPLING





NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2

NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

FW: 1394B MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 45 OF 97	

=PPV_S5_FW

DE4600
MURS320XXG
SMC

FW_PORTS_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

CRITICAL
R4600
2.7
10%
1W
FF-LF
2512

CRITICAL
R4601
2.7
10%
1W
FF-LF
2512

FW_PORTS_VP_R
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

CRITICAL
F4600
0.75AMP-30V
SM

FW_PORTS_VP_F
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

24 VOLTS
15 WATTS MAX

L4600
FERR-250-OHM
SM

SHOULD BE DONE AS A POWER STRIP(SUBPLANE)

FW_PORT0_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

C4600
0.01UF
10%
50V
X7R
603-1

GND_CHASSIS_FIREWIRE

Termination
Place close to FireWire PHY

VOLTAGE=1.86V
FW_B_TPBIAS
FW_A_TPBIAS
VOLTAGE=1.86V

C4650
1UF
10%
6.3V
CERM
402

C4660
1UF
10%
6.3V
CERM
402

NOTE: TI PHY REQUIRES 1uF EVEN THOUGH SPEC CALLS OUT .33uF

L4650
18NH-250MA
0402

L4651
18NH-250MA
0402

FW_A_TPA_P_RL
NO_TEST=TRUE
VOLTAGE=1.86V

FW_A_TPA_N_RL
NO_TEST=TRUE
VOLTAGE=1.86V

R4650 56.2 1% 1/16W MF-LF 402
R4651 56.2 1% 1/16W MF-LF 402
R4660 56.2 1% 1/16W MF-LF 402
R4661 56.2 1% 1/16W MF-LF 402

FW_A_TPA_P
FW_A_TPA_N
FW_A_TPB_P
FW_A_TPB_N

MAKE_BASE=TRUE

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

FW_B_TPA_P
FW_B_TPA_N
FW_B_TPB_P
FW_B_TPB_N

FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N

R4652 56.2 1% 1/16W MF-LF 402
R4653 56.2 1% 1/16W MF-LF 402
R4662 56.2 1% 1/16W MF-LF 402
R4663 56.2 1% 1/16W MF-LF 402

FW_A_TPB_N_RL
NO_TEST=TRUE
VOLTAGE=0V

FW_A_TPB_P_RL
NO_TEST=TRUE
VOLTAGE=0V

L4652
18NH-250MA
0402

L4653
18NH-250MA
0402

FW_TPA_C0
VOLTAGE=0V

FW_TPA_C1
VOLTAGE=0V

C4654
270PF
5%
25V
CERM
402

R4654
4.99K
1%
1/16W
MF-LF
402

C4664
270PF
5%
25V
CERM
402

R4664
4.99K
1%
1/16W
MF-LF
402

3rd TPA/TPB pair unused

FW_C_TPBIAS = NC_FW_C_TPBIAS
FW_C_TPA_P = NC_FW_C_TPA_P
FW_C_TPA_N = NC_FW_C_TPA_N
FW_C_TPB_P
FW_C_TPB_N

MAKE_BASE=TRUE
NO_TEST=TRUE

NOTE: TI RECOMMENDS THIS FOR UNCONNECTED PORTS

ESD Rail

=PP3V3_S5_FW
R4690
332
1%
1/16W
MF-LF
402

PP3V3_FW_ESD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

L4690
400-OHM-EMI
SM-1

PP3V3_FW_ESD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

CRITICAL
D4690
SOT23
MMBZ5227B

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD

DP4610
BAV99DW-X-F
SOT-363

C4610 0.01UF 10% 50V X7R 402
C4611 0.01UF 10% 50V X7R 402

FW_PORT0_TPB_N
FW_PORT0_TPB_P
FW_PORT0_TPA_N
FW_PORT0_TPA_P

DP4611
BAV99DW-X-F
SOT-363

C4612 0.01UF 10% 50V X7R 402
C4613 0.01UF 10% 50V X7R 402

PORT 0
1394B
CRITICAL
J4600
1394B-M51
F-ST-TH

TPB-
TPB<R>
TPB+
VP
NC
VG
TPA-
TPA<R>
TPA+

514-0325

FW_PORT0_TPA_R

NOSTUFF
C4630 0.001UF 10% 50V CERM 402
C4631 0.001UF 10% 50V CERM 402
C4632 0.001UF 10% 50V CERM 402

R4635 1M 1% 1/16W MF-LF 402
C4635 0.1UF 10% 50V X7R 603-1

GND_CHASSIS_FIREWIRE

L4601
FERR-250-OHM
SM

SHOULD BE DONE AS A POWER STRIP(SUBPLANE)

FW_PORT1_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

C4601
0.01UF
10%
50V
X7R
603-1

GND_CHASSIS_FIREWIRE

PP3V3_FW_ESD

DP4620
BAV99DW-X-F
SOT-363

C4620 0.01UF 10% 50V X7R 402
C4621 0.01UF 10% 50V X7R 402

CRITICAL
FL4600
120-OHM
DLW21H-SM1

CRITICAL
FL4610
120-OHM
DLW21H-SM1

FW_PORT1_TPA_FL_P
FW_PORT1_TPA_FL_N
FW_PORT1_TPB_FL_P
FW_PORT1_TPB_FL_N

FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N

PP3V3_FW_ESD

DP4621
BAV99DW-X-F
SOT-363

C4622 0.01UF 10% 50V X7R 402
C4623 0.01UF 10% 50V X7R 402

PORT 1
1394A
CRITICAL
J4601
1394A-M51
F-ST-TH

TPO
TPO#
TPI
TPI#
VP
VGND

514-0342

NOSTUFF
C4642 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

"Snapback" & "Late VG" Protection

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

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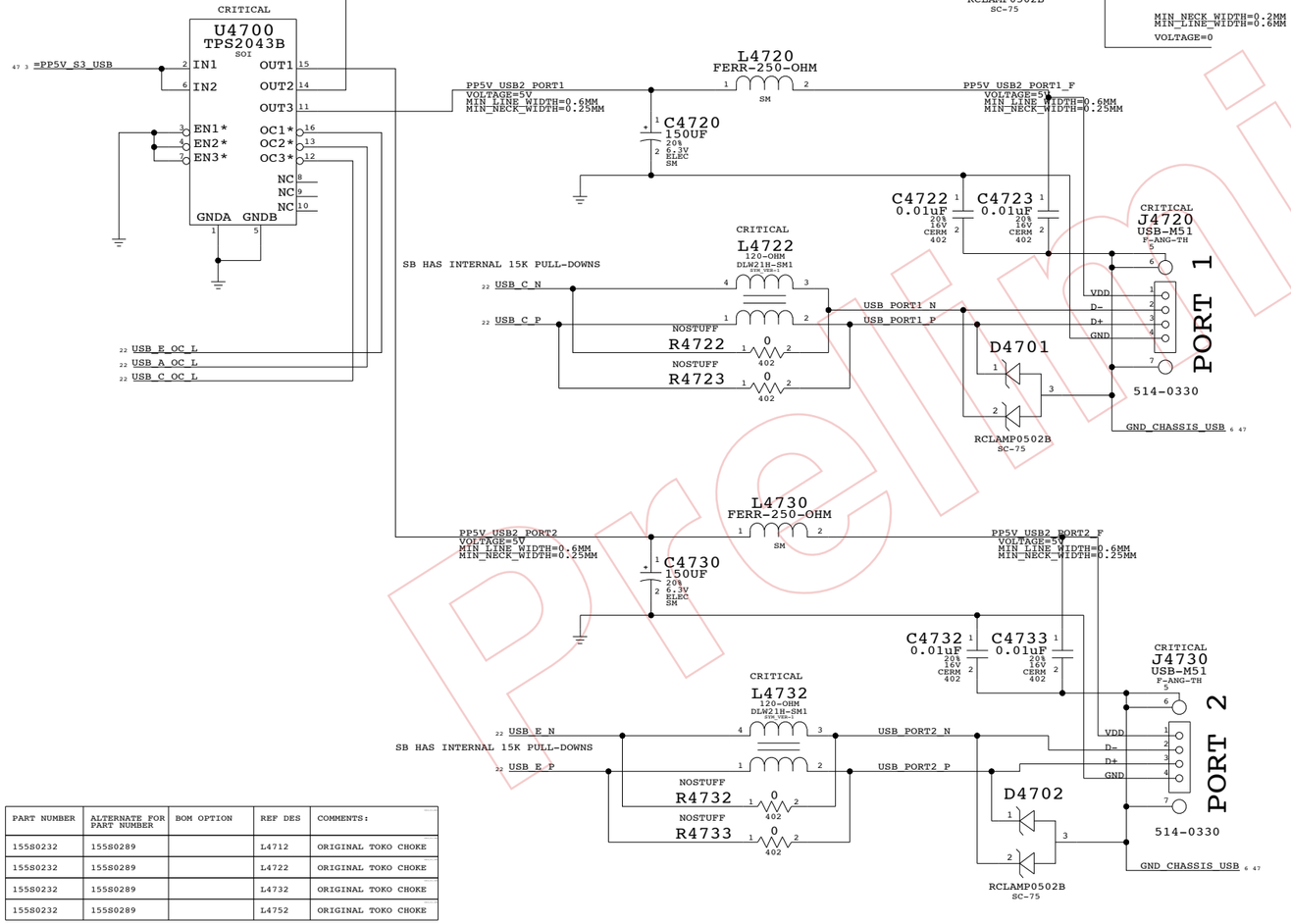
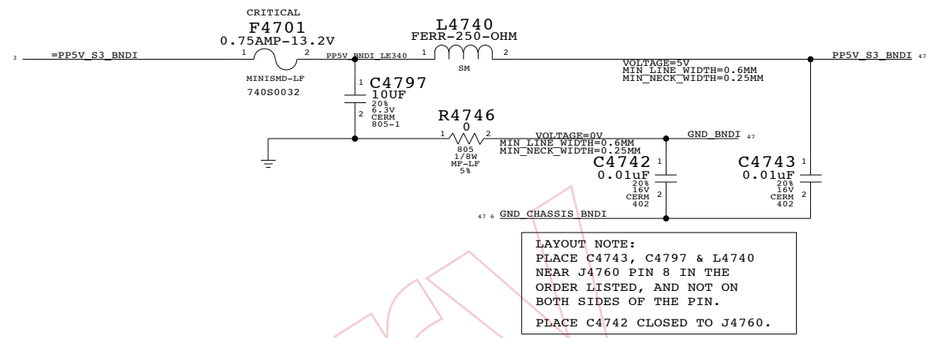
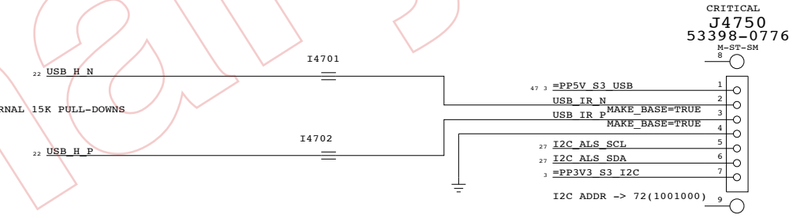
External USB Ports



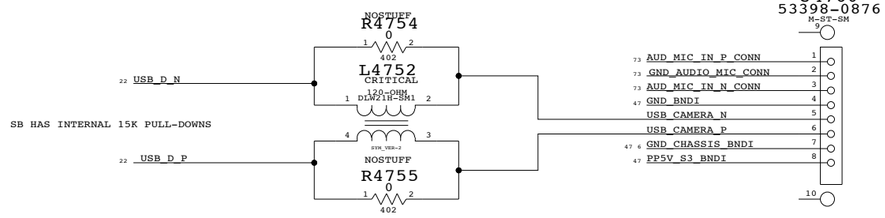
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



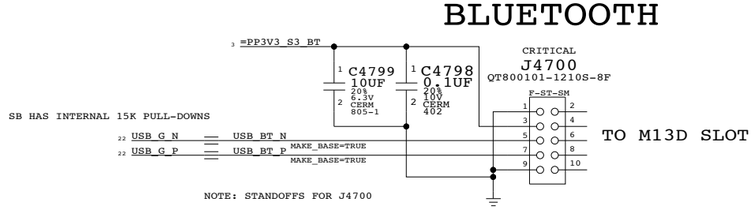
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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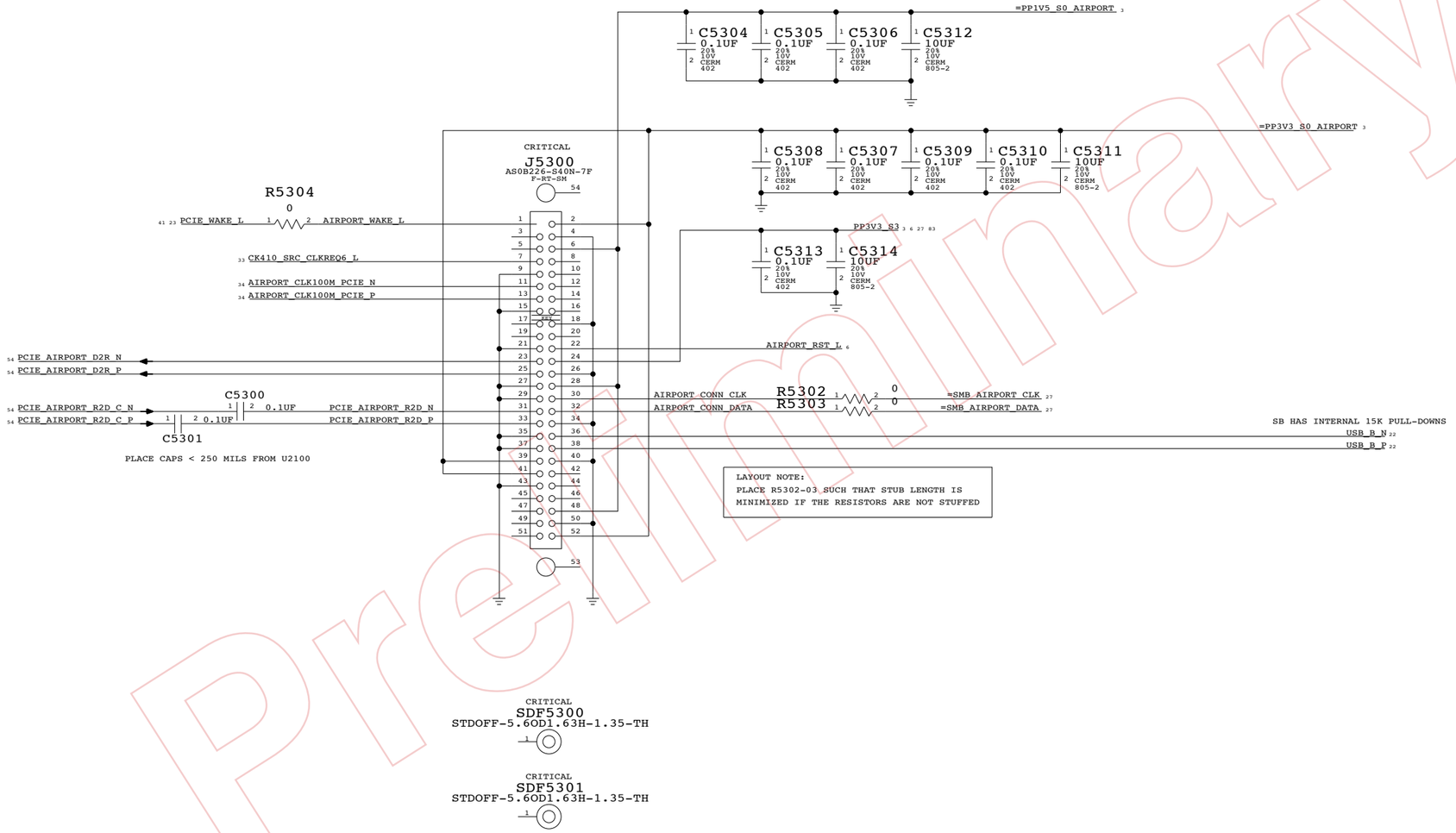

AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
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PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13		SMC_PM_G2_EN
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14		SMC_ADAPTER_EN
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22	SPI_SCLK
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22	SPI_SI
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22	SPI_SO
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	59	SMC_PROCHOT_3_3_L
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	59	SMC_CPU_INIT_3_3_L
SMC_P20	D13	P20	P70/AN0	N12	76	SMC_CPU_ISENSE
SMC_P21	D14	P21	P71/AN1	R13	76	SMC_CPU_VSENSE
SMC_P22	D15	P22	P72/AN2	P13	84	SMC_GPU_ISENSE
SMC_P23	E12	P23	P73/AN3	R14	84	SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	76	SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	76	SMC_PBUS_VSENSE
SMC_P26	E13	P26	P76/AN6	N13	59	SMC_BATT_ISENSE
SMC_P27	F14	P27	P77/AN7	P15	59	SMC_FWIRE_ISENSE
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	59	SMC_TPM_GPIO
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 23 5	PM_CLKRUN_L
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23 5	PM_SUS_STAT_L
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	59	SC_TX_L
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	59	SC_RX_L
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27	SMB_BSB_CLK
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	59	SMC_ONOFF_L
SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	59	SMC_BC_ACOK
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	59	SMC_BS_ALRT_L
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	80 79 77 23 5	PM_SLP_S3_L
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23 5	PM_SLP_S4_L
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	59	SMC_SUS_CLK
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27	SMB_0_S0_DATA
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
SMC_TX_L	G1	P50				
SMC_RX_L	G4	P51				
SMB_0_S0_CLK	F2	P52/SCL0				

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U5800
SMC_H8S2116
BGA
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SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5 SMC_TCK
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5 SMC_TDI
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5 SMC_TDO
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5 SMC_TMS
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59 SMC_LID
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59 SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59 SMC_BATT_ISET
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59 SMC_BATT_VSET
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59 SMC_SYS_ISET
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59 SMC_SYS_VSET
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22 SPI_CE_L
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59 SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	27 SMB_BSA_DATA
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	27 SMB_BSA_CLK
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	27 SMB_A_S3_DATA
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	27 SMB_A_S3_CLK
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	27 SMB_B_S0_DATA
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	27 SMB_B_S0_CLK
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59 SMC_PROCHOT
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59 SMC_THRMTRIP
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59 SMC_FWE
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59 ALS_GAIN
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23 SMS_INT_L
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59 SMS_ONOFF_L
SMC_ANALOG_ID	N11	PD3/AN11			
SMC_NB_ISENSE	P10	PD4/AN12			
SMC_MEM_ISENSE	R10	PD5/AN13			
ALS_LEFT	N10	PD6/AN14			
ALS_RIGHT	M10	PD7/AN15			

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U5800
SMC_H8S2116
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G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 27 3 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 27 3 =PP3V3_S5_SMC
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
84 76 59 58 GND_SMC_AVSS

PP3V3_AVREF_SMC 59
59 58 27 3 =PP3V3_S5_SMC

OMIT
U5800
SMC_H8S2116
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AVCC N14, N15
VCC P2, P1, J15, A1, F1
AVREF M14, M15
VSS D1, F4, F12, B13, A13, A4, B4, D2
AVSS P12, R12

60 59 5 IN SMC_RST_L → RES* E3
59 SMC_XTAL → XTAL A2
59 SMC_EXTAL → EXTAL B2
ETRST* L1

MD1 E2 → SMC_MD1 5 60
MD2 K1 → KBC_MDE
NMI F4 → SMC_NMI IN
SMC_TRST_L IN

R5809 10K 5% 1/16W MF-LF 2402
R5801 10K 5% 1/16W MF-LF 2402
R5898 10K 5% 1/16W MF-LF 2402
NOSTUFF
R5803 0 5% 1/16W MF-LF 2402
R5802 10K 5% 1/16W MF-LF 2402

OMIT
XW5800
SM
GND_SMC_AVSS 58 59 76 84

SMC

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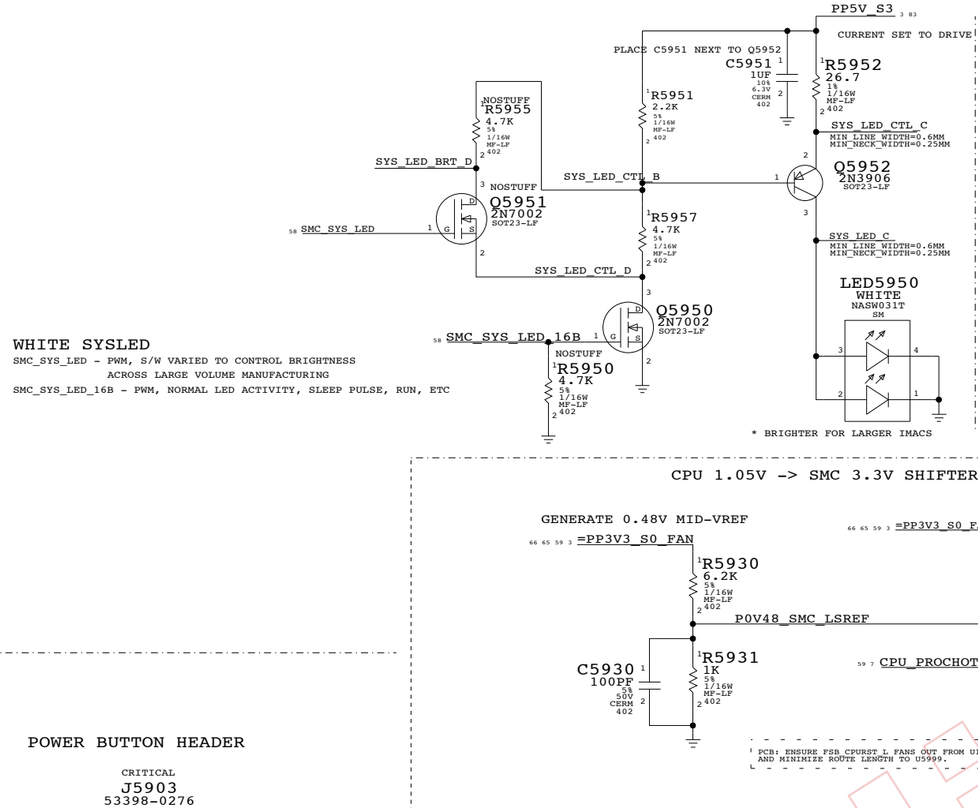
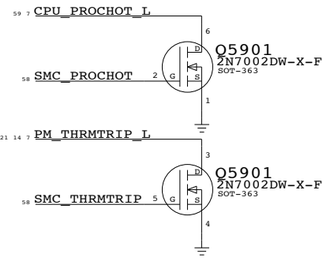


WHITE SYSLED

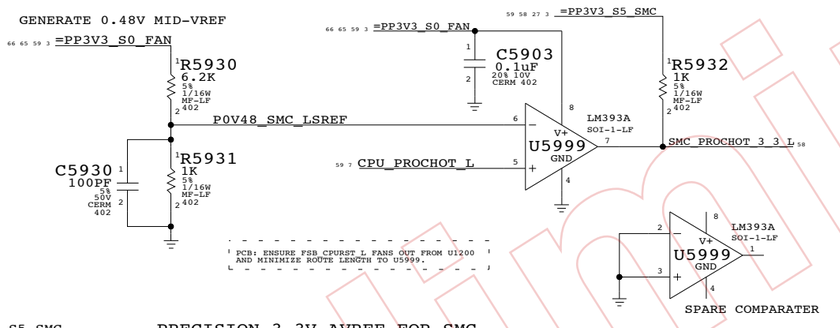
SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS ACROSS LARGE VOLUME MANUFACTURING

SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

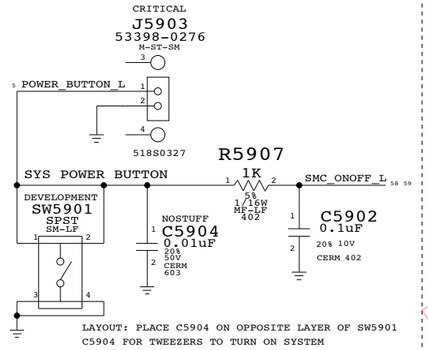
SMC 3.3V -> CPU 1.05V SHIFTER



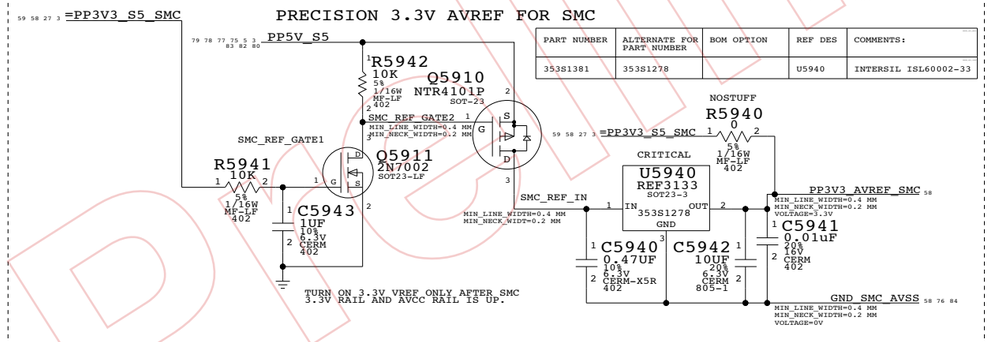
CPU 1.05V -> SMC 3.3V SHIFTER



POWER BUTTON HEADER

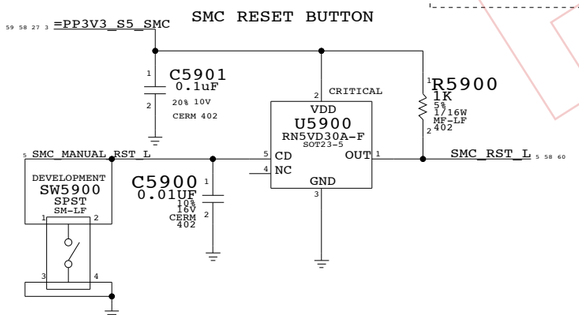


PRECISION 3.3V AVREF FOR SMC

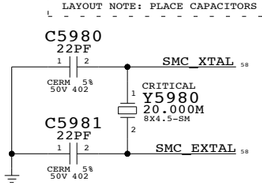


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	INTERSIL ISL60002-33

SMC RESET BUTTON

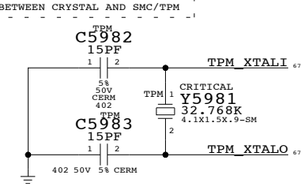


SMC CRYSTAL



TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20	MAKE_BASE=TRUE
SMC_P21	NC_SMC_P21	MAKE_BASE=TRUE
SMC_P22	NC_SMC_P22	MAKE_BASE=TRUE
SMC_P23	NC_SMC_P23	MAKE_BASE=TRUE
SMC_P26	NC_SMC_P26	MAKE_BASE=TRUE
SMC_P27	NC_SMC_P27	MAKE_BASE=TRUE
SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE; FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE; FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE
SMC_XDP_TCK	TP_SMC_XDP_TCK	MAKE_BASE=TRUE
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L	MAKE_BASE=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE; FUNC_TEST=TRUE

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE
SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE
SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE
SMC_NB_ISENSE	NC_SMC_NB_ISENSE	MAKE_BASE=TRUE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE

UNUSED_SMC_SENSE — R5924 10K 5% 1/16W MF-LF

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE; FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE; FUNC_TEST=TRUE

TPM RESET PULLUP

SMC_TPM_RESET_L — R5827 10K — PP3V3_TPM_3VSB

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE
SC_RX_L — R5922 0 — SMC_RX_L		
SC_TX_L — R5923 0 — SMC_TX_L		

SMC PULL-UPS & PULL-DOWNS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K
SMC_LID	R5916	10K
SMC_EXCARD_OC_L	R5831	10K
SMC_XDP_TCK_3_3	R5934	1K
SMC_CPU_RESET_3_3_L	R5933	1K
SMC_EXCARD_CP	R5830	10K
SMC_CASE_OPEN	R5917	10K

POWER SUPPLY TEMP SENSE

SMC_ANALOG_ID — ACDC_TEMP

SELECT TPM GPIO

SMC_TPM_GPIO — R5920 0 — TPM_GPIO1; R5921 0 — TPM_GPIO2

HDD ACTIVITY MONITOR

PP5V_S0 — R5960 10K — PU_HDD_ACTIVITY_LED

TP_SB_SATALED_L

M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM — GND_NEXT_TO_SMC — OMIT

M51 SPECIFIC: GPU MONITORING SIGNALS

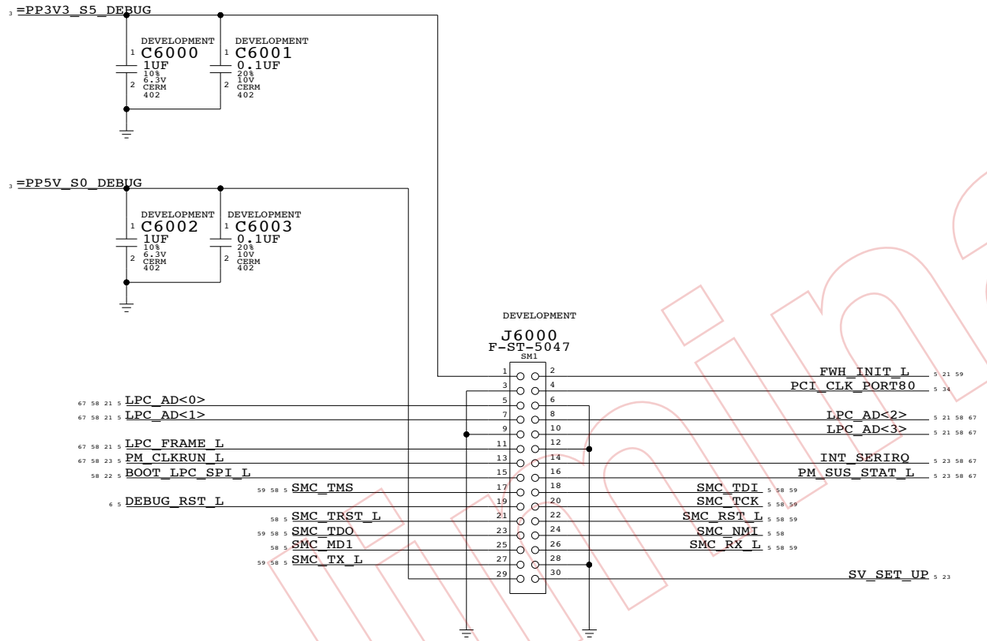
SMC_XDP_TMS	I327	MXM_AC_BATT_L
SMC_XDP_TDO_3_3	I328	GPU_OVERTEMP_L

SMC & TPM SUPPORT

SYNC_MASTER=M51_HENRY SYNC_DATE=07/31/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 59 OF 97	

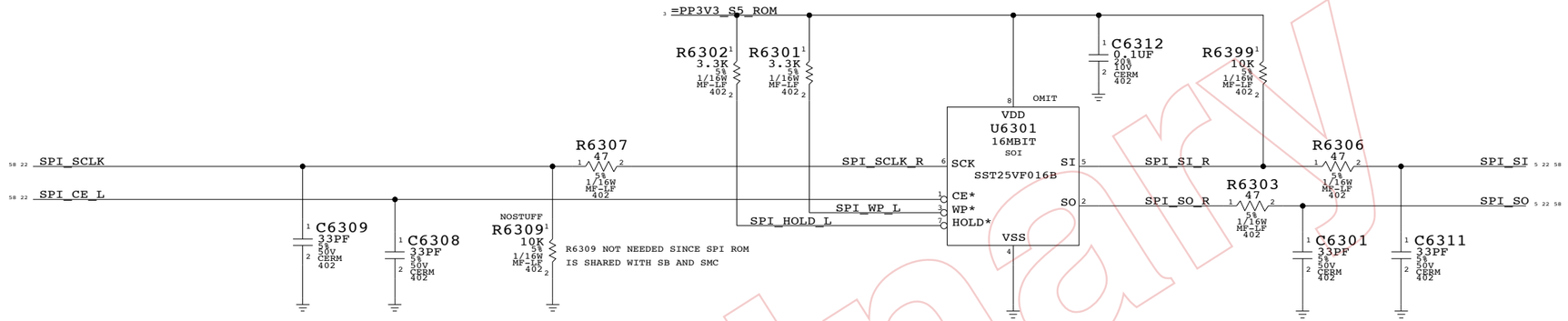


LPC+ CONN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 60 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

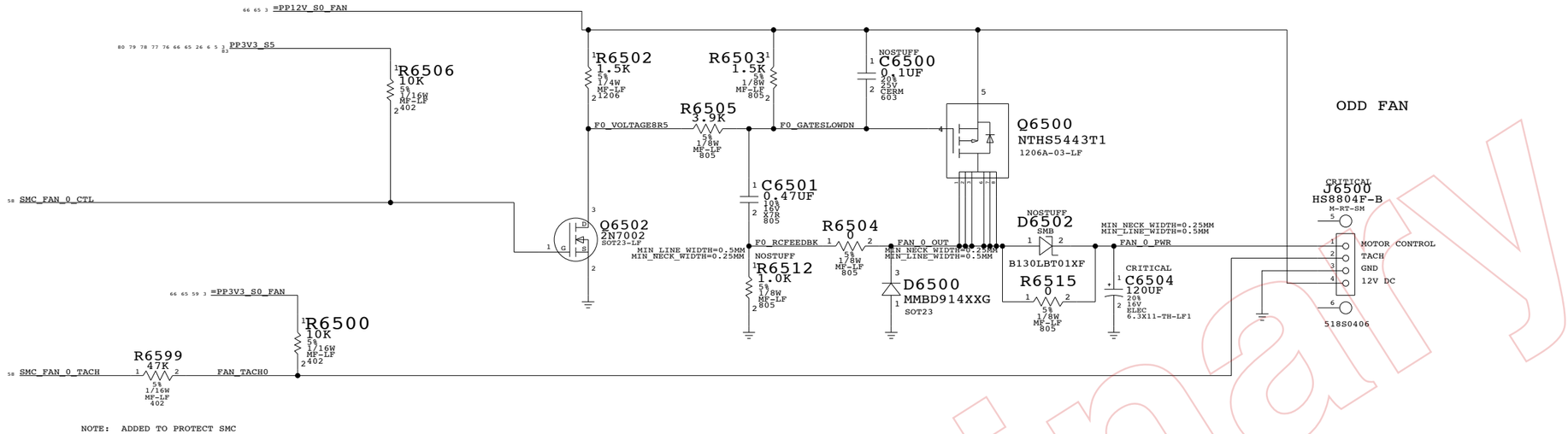
SPI BOOTROM

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

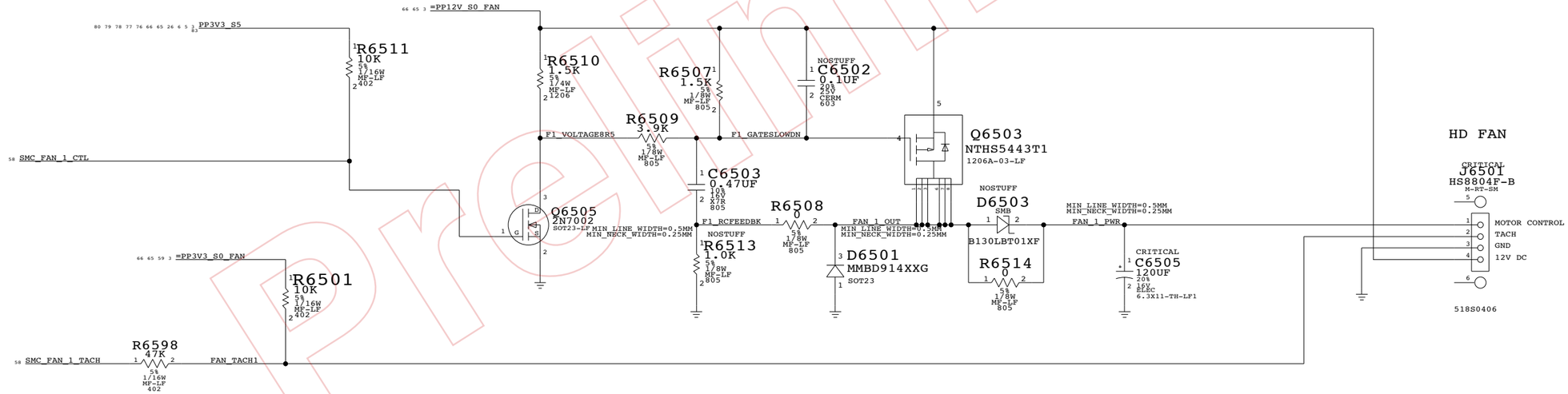
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 63 OF 97	

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



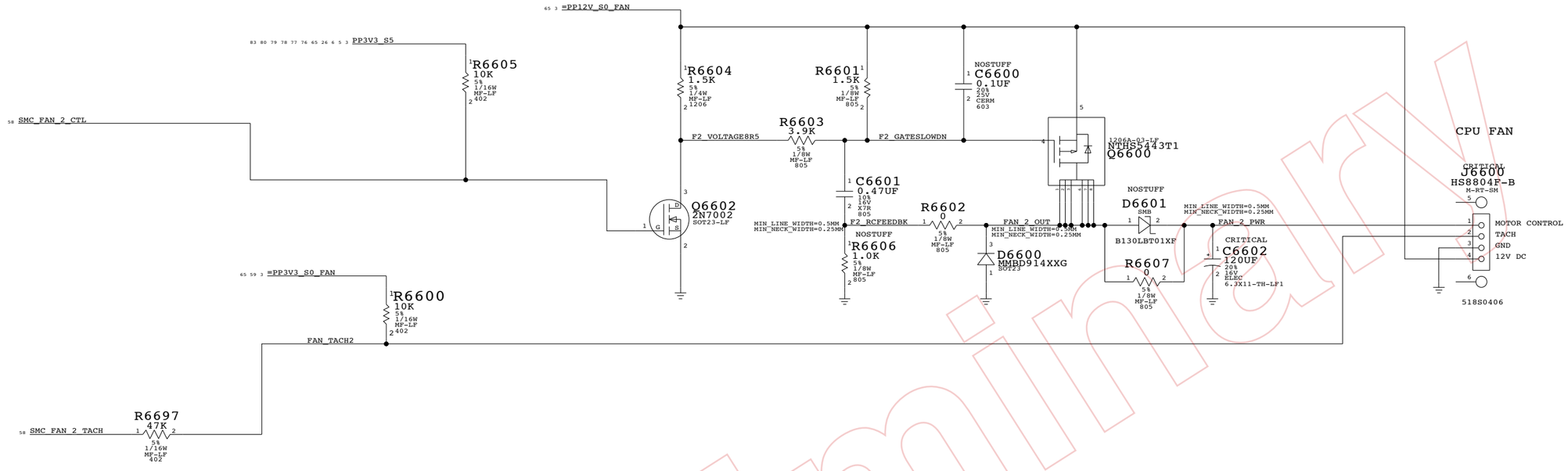
HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

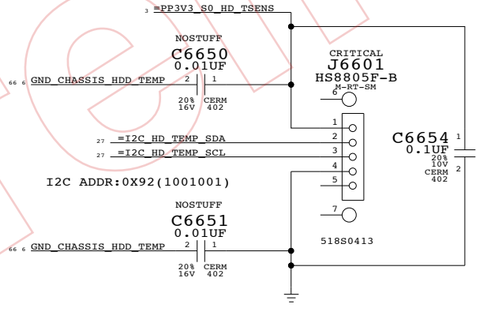
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 65 OF 97	

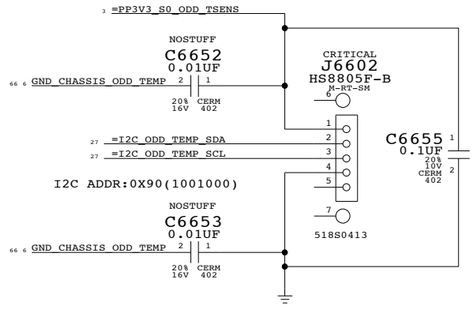
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR

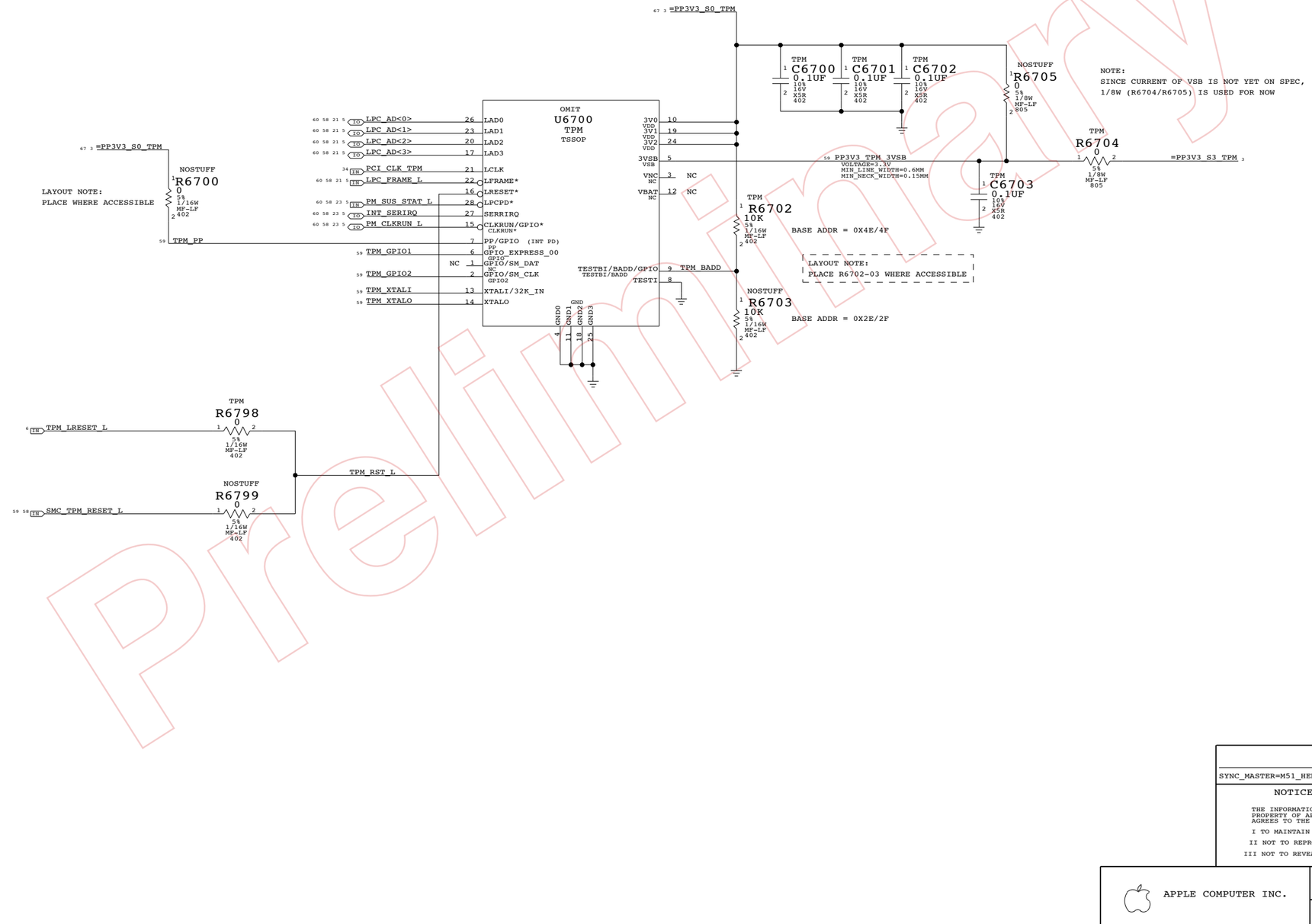


CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 66 OF 97	



TPM

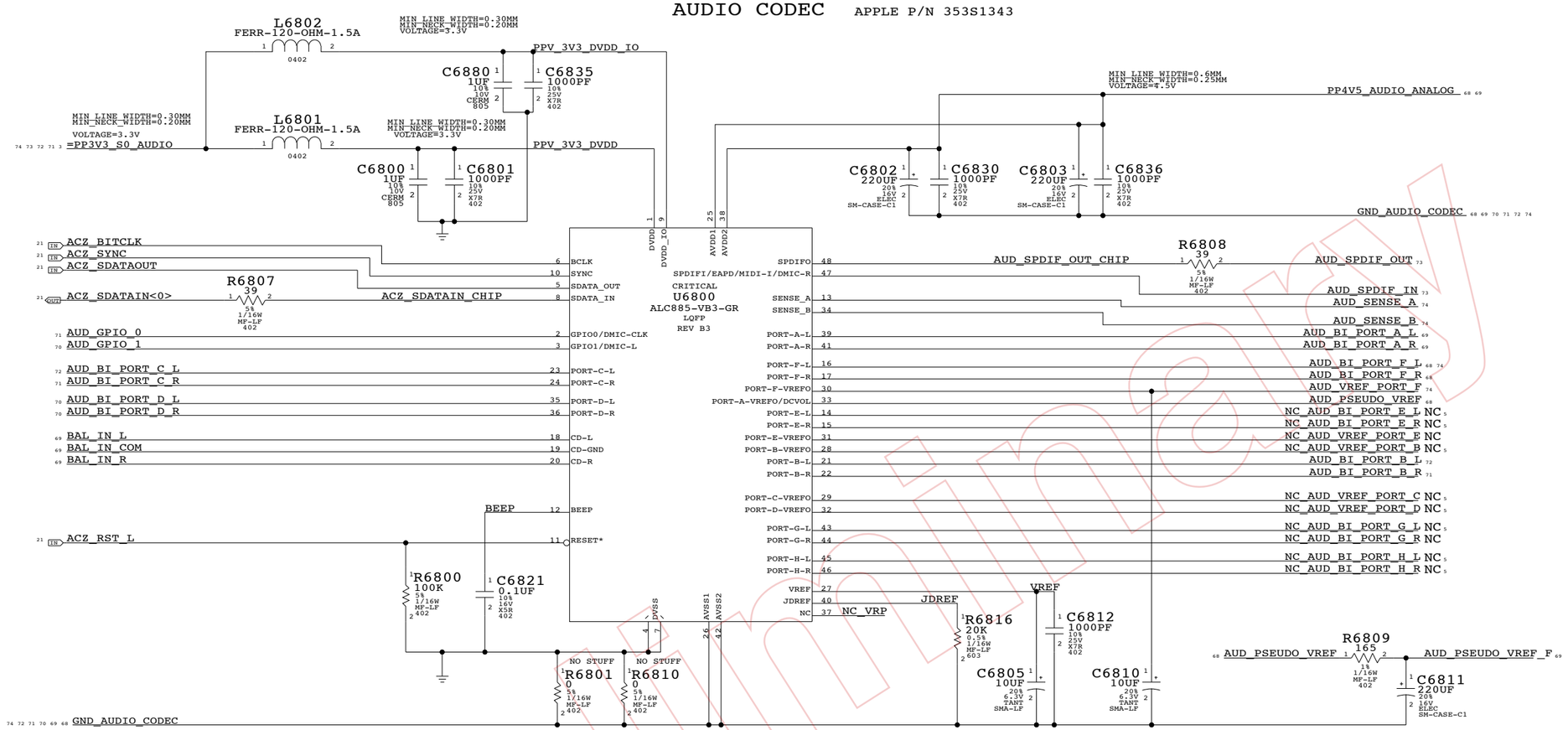
SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

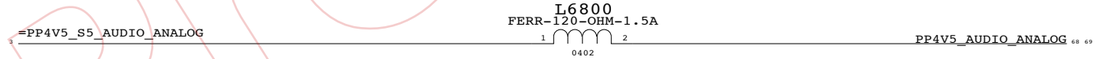
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 67 OF 97	

AUDIO CODEC

APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

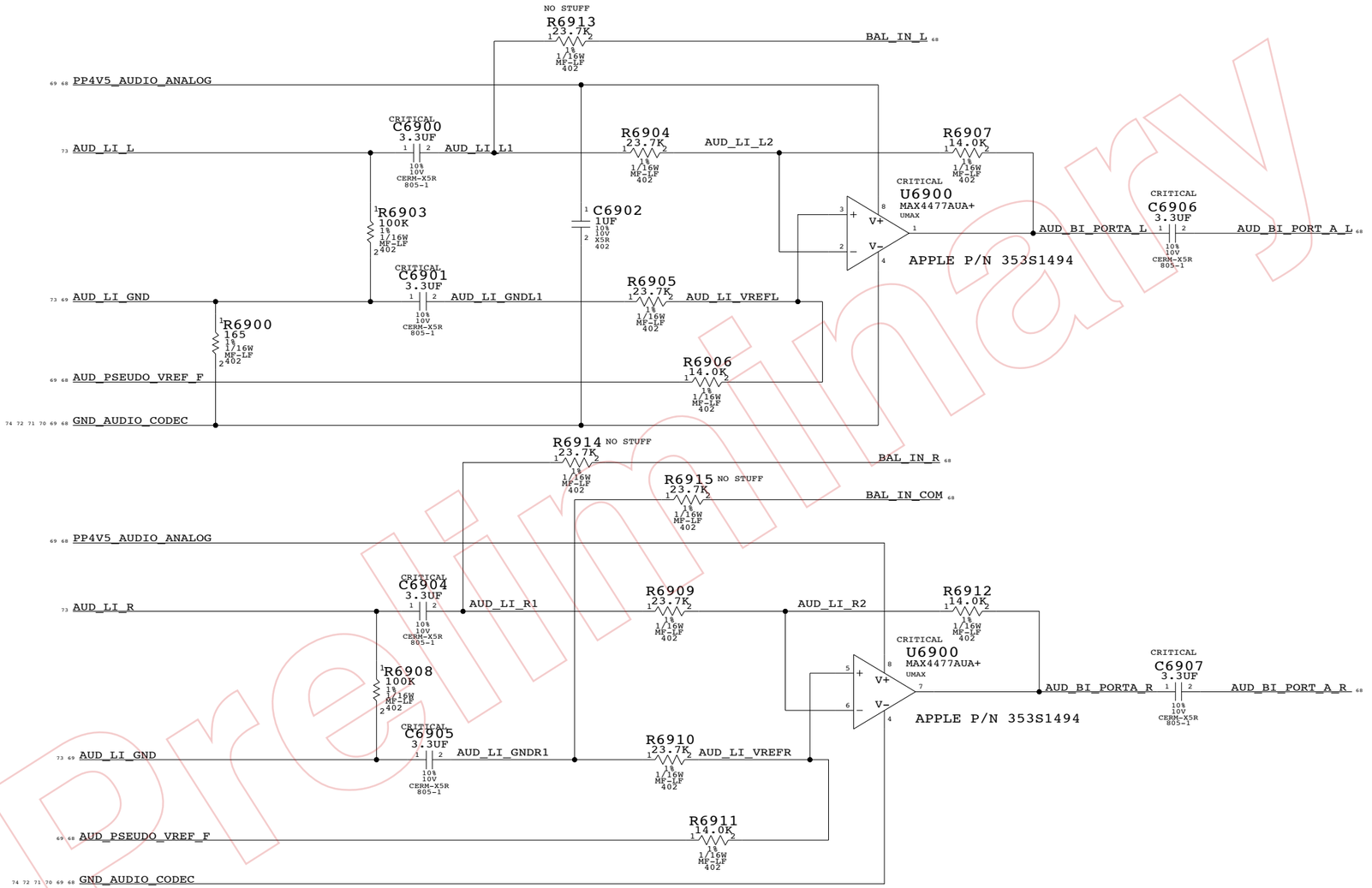


MIC INPUT TO BOTH L&R

AUDIO: CODEC		
SYNC_MASTER=AUDIO	SYNC_DATE=08/04/2006	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE COMPUTER INC.	SIZE D / DRAWING NUMBER 051-7039 / REV. H	
	SCALE NONE	SHT 68 OF 97

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59



AUDIO: LINE INPUT AMP

APPLE COMPUTER INC.

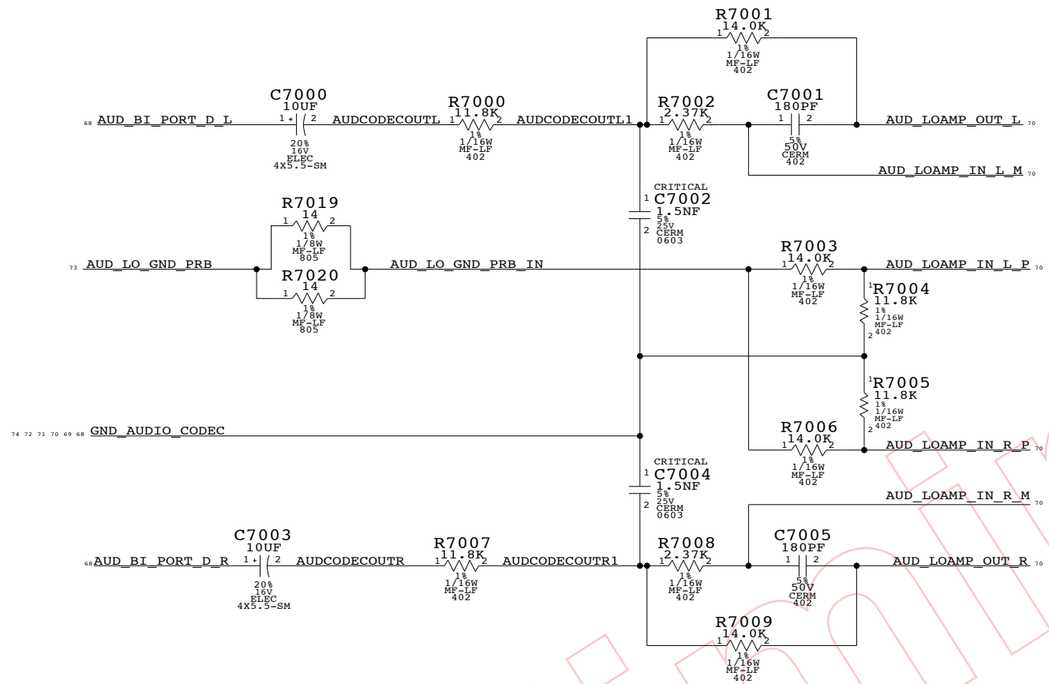
SIZE	DRAWING NUMBER	REV.
D	051-7039	H

SCALE: NONE

SHT 69 OF 97

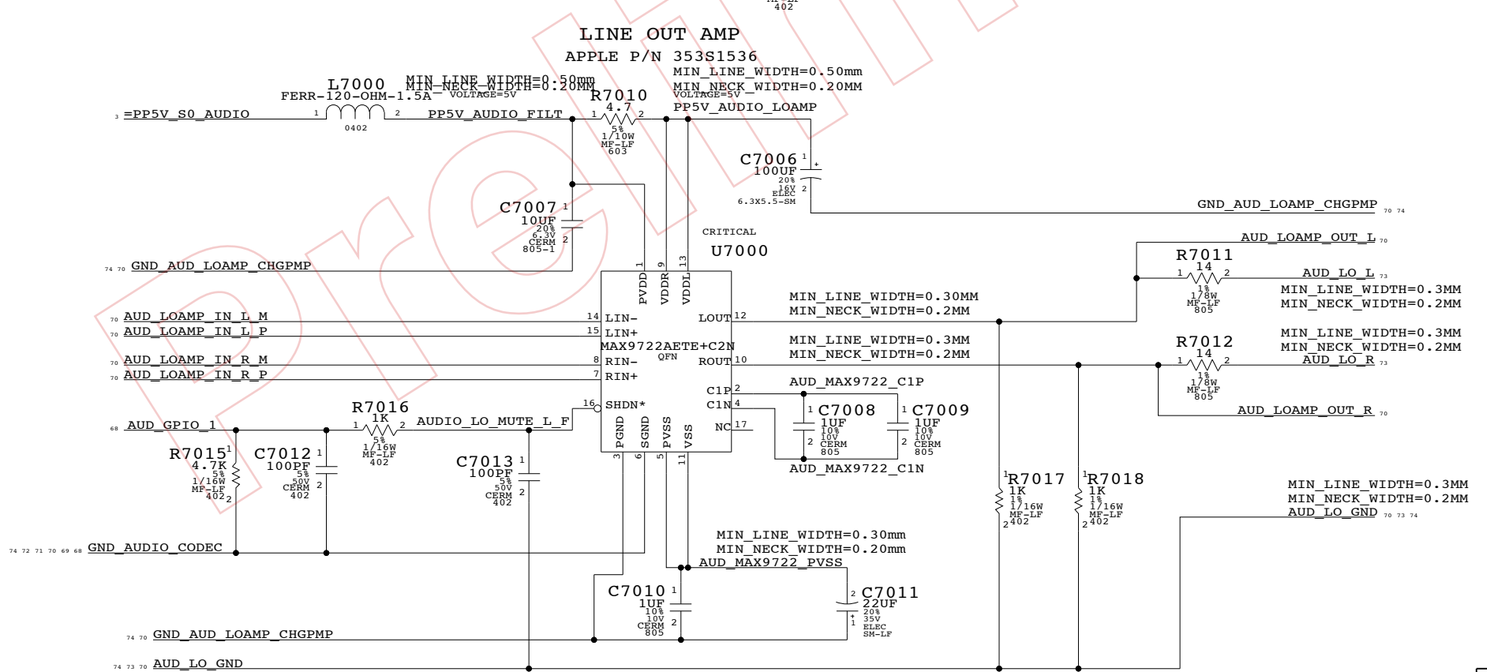
LINE OUT LOW-PASS FILTER

Fc = 37 KHZ, Av = -1.18



LINE OUT AMP

APPLE P/N 353S1536



AUDIO: COMBO OUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 70 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
PP12V_AUD_SPKRAMP_PLANE

L7122 FERR-250-OHM SM-1
L7100 FERR-250-OHM SM-1
R7170 0.005 1% 1/4W MF-LF 1206
=PP12V_S5_AUDIO_SPKRAMP
12V_S5_SPKRAMP
C7117 470UF 20% 25V ELEC 10X10-SM
C7100 470UF 20% 25V ELEC 10X10-SM
C7101 10UF 10% 16V X5R-CERM 1210
C7118 0.1UF 20% 16V CERM 603
GND_AUDIO_SPKRAMP_PLANE

C7102 1UF 10% 35V X7R 805
C7119 0.1UF 20% 16V CERM 603
C7103 10UF 10% 16V X5R-CERM 1210
GND_AUDIO_SPKRAMP_PLANE

L7105 1000-OHM-200MA 0603
C7104 0.47UF 10% 16V X7R 805
AUD_BI_PORT_C_R
AUDSAMPINLN
C7115 100PF 5% 50V CERM 402
L7106 1000-OHM-200MA 0603
C7105 0.47UF 10% 16V X7R 805
AUDSAMPINLP
GND_AUDIO_CODEC
L7107 1000-OHM-200MA 0603
C7106 0.47UF 10% 16V X7R 805
AUDSAMPINRP
C7116 100PF 5% 50V CERM 402
L7108 1000-OHM-200MA 0603
C7107 0.47UF 10% 16V X7R 805
AUD_BI_PORT_B_R
AUDSAMPINRN

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD

CRITICAL
U7100
MAX9714
QFN-LF

AUD_SAMP_INL_N	9	INL-
AUD_SAMP_INL_P	10	INL+
AUD_SAMP_INR_P	16	INR+
AUD_SAMP_INR_N	15	INR-
AUD_SAMP_G1	17	G1
AUD_SAMP_G2	18	G2
AUD_SAMP_FS1	19	FS1
AUD_SAMP_FS2	20	FS2
AUD_SAMP_SHDN_L	11	SHDN*
	8	NC
AUD_MAX9714_VREG	14	REG
	7	CHOLD
	31,32	OUTL+
	29,30	OUTL-
	6	C1+
	5	C1-
	27,28	OUTR+
	25,26	OUTR-
	12	SS
	13	THM
	33	AGND PAD
	1,2,23,24	PGND
	3,4,21,22	VDD

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
SPKRAMP_SS
C7114 1UF 10% 25V X5R 603
C7109 0.47UF 10% 16V X7R 805

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPOUTRP
AUDSAMPOUTRN

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP
AUDSAMPCPN
C7108 0.1UF 10% 50V X7R 603-1

L7101 180-OHM-1.5A 0603-LF
L7102 180-OHM-1.5A 0603-LF
L7103 180-OHM-1.5A 0603-LF
L7104 180-OHM-1.5A 0603-LF

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUD_SPKR_OUTCR_P
AUD_SPKR_OUTCR_N
AUD_SPKR_OUTBR_P
AUD_SPKR_OUTBR_N

C7110 1000PF 10% 25V X7R 402
C7111 1000PF 10% 25V X7R 402
C7112 1000PF 10% 25V X7R 402
C7113 1000PF 10% 25V X7R 402

XW7102 SM OMIT
XW7101 SM OMIT
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP_PLANE

R7114 47K 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
AUD_SAMP_SHDN_L
AUD_SPKRAMP_MUTE
R7115 47K 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
R7113 47K 5% 1/16W MF-LF 402
AUD_GPIO_0
AUD_SPKRAMP_MUTE_L
Q7100 2N7002DW-X-F SOT-363
Q7100 2N7002DW-X-F SOT-363
R7112 4.7K 5% 1/16W MF-LF 402
C7120 100PF 5% 50V CERM 402
C7121 100PF 5% 50V CERM 402
C7190 100PF 5% 50V CERM 402
GND_AUDIO_CODEC
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC

NOSTUFF
R7119 0 5% 1/16W MF-LF 402

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO
RP7100 47K 5% 1/16W SM-LF
AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1
NOSTUFF R7118 0 5% 1/16W MF-LF 402
NOSTUFF R7108 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 71 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

=PP12V_S5_AUDIO_SPKRAMP — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=3.0MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=12V
R7270 0.005 1% 1/4W MF-LF 1206
12V_S5_SPKRAMP1 — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=3.0MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=12V
L7222 FERR-250-OHM SM-1
L7200 FERR-250-OHM SM-1
PP12V_AUD_SPKRAMP1_PLANE — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V
C7217 470UF 20% 25V ELEC 10X10-SM
C7200 470UF 20% 25V ELEC 10X10-SM
C7201 10UF 10% 16V X5R-CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 35V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V X5R-CERM 1210
GND_AUDIO_SPKRAMP1_PLANE
GND_AUDIO_CODEC
AUD_BI_PORT_C_L
AUD_BI_PORT_B_L
L7205 1000-OHM-200MA 0603
L7206 1000-OHM-200MA 0603
L7207 1000-OHM-200MA 0603
L7208 1000-OHM-200MA 0603
C7204 0.47UF 10% 16V X7R 805
C7205 0.47UF 10% 16V X7R 805
C7206 0.47UF 10% 16V X7R 805
C7207 0.47UF 10% 16V X7R 805
C7215 100PF 5% 50V CERM 402
C7216 100PF 5% 50V CERM 402
C7290 100PF 5% 50V CERM 402
AUDSAMPINLN1
AUDSAMPINLP1
AUDSAMPINRP1
AUDSAMPINRN1
R7214 47K 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
SPKRAMP1_SS
AUD_SPKRAMP_MUTE
Q7200 2N7002 SOT23-LF
C7214 1UF 10% 25V X5R 603
C7209 0.47UF 10% 16V X7R 805
R7219 0 5% 1/16W MF-LF 402 NOSTUFF

CRITICAL
U7200
MAX9714
QFN-LF

VDD
INL- AUD_SAMP1_INL_N
INL+ AUD_SAMP1_INL_P
INR+ AUD_SAMP1_INR_P
INR- AUD_SAMP1_INR_N
G1 AUD_SAMP1_G1
G2 AUD_SAMP1_G2
FS1 AUD_SAMP1_FS1
FS2 AUD_SAMP1_FS2
SHDN* AUD_SAMP1_SHDN_L
NC
REG AUD_MAX9714_VREG1
THM AGND PAD PGND SS
CHOLD AUD_MAX9714_CHOLD1 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.2MM
OUTL+ AUDSAMPOUTLP1 — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM
OUTL+ AUDSAMPOUTLN1 — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM
OUTL- AUDSAMPOUTLN1 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM
C1+ AUDSAMPCPP1
C1- AUDSAMPCPN1
C7208 0.1UF 10% 50V X7R 603-1 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM
OUTR+ AUDSAMPOURTP1 — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM
OUTR+ AUDSAMPOUTRN1 — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM
OUTR- AUDSAMPOURTP1
OUTR- AUDSAMPOUTRN1

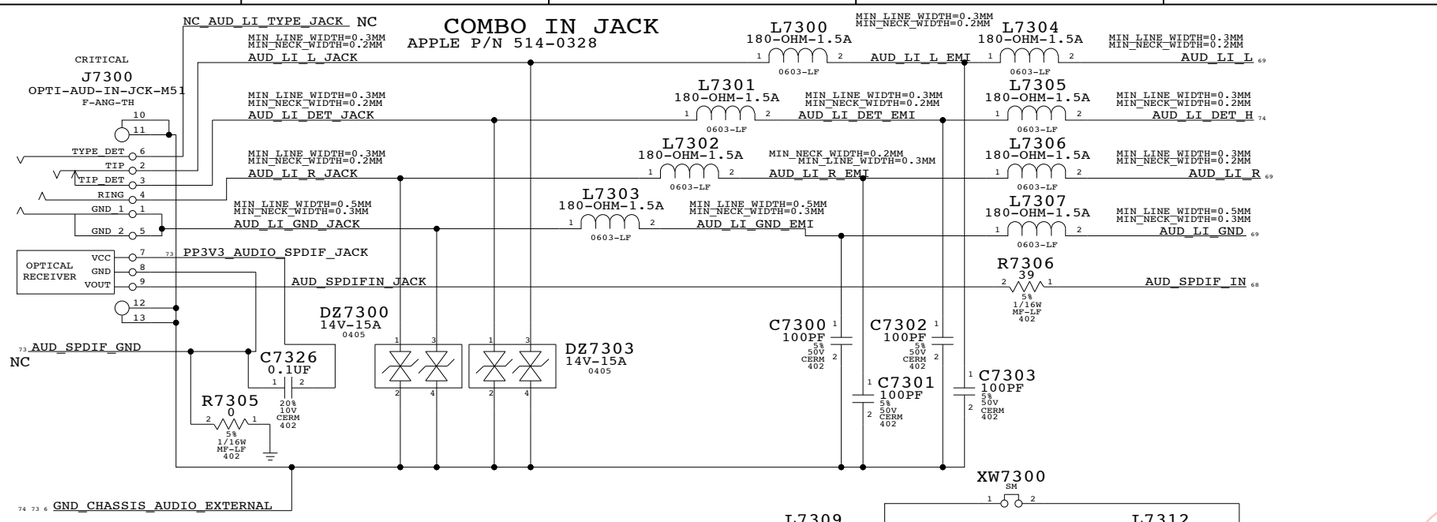
L7201 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTCL_P
L7202 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTCL_N
L7203 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTBL_P
L7204 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTBL_N
NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM
C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402
XW7202 SM OMIT
XW7201 SM OMIT
AUD_SPKR_OUTBL_N
GND_AUDIO_SPKRAMP — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=3.0MM, MIN_NECK_WIDTH=0.2MM
NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
GND_AUDIO_SPKRAMP1_PLANE

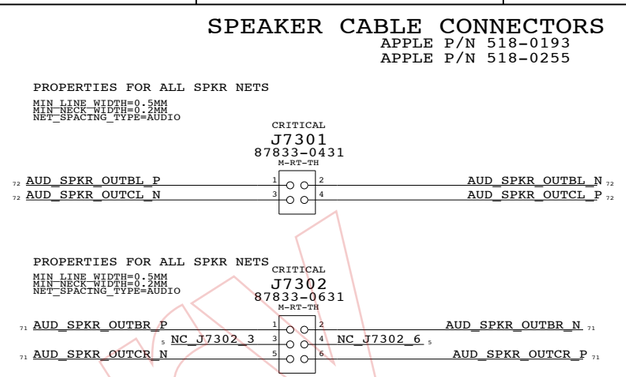
GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

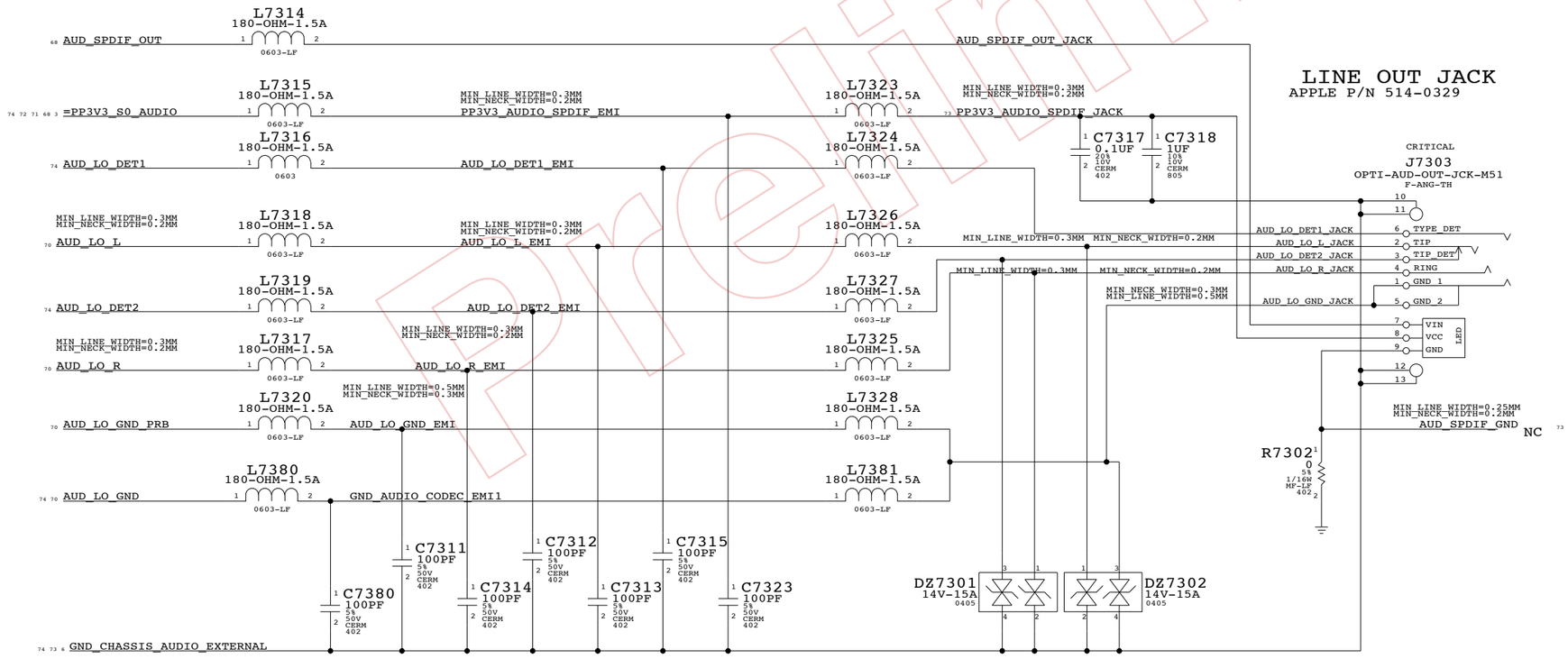
=PP3V3_S0_AUDIO
RP7200 47K 5% 1/16W SM-LF
AUD_SAMP1_FS2
AUD_SAMP1_FS1
AUD_SAMP1_G2
AUD_SAMP1_G1
R7218 0 5% 1/16W MF-LF 402 NOSTUFF
R7208 0 5% 1/16W MF-LF 402 NOSTUFF
GND_AUDIO_SPKRAMP1_PLANE

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-7039 | REV. H
SCALE NONE | SHT 72 OF 97







AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H

SCALE: NONE SHT 73 OF 97

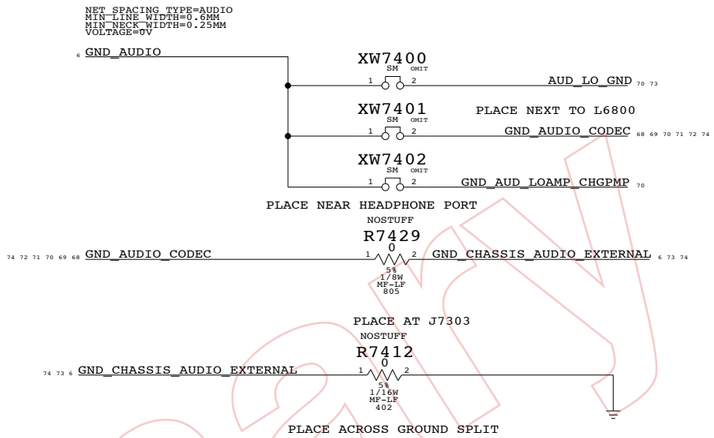
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14(D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18(B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A(C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN 0X16H		

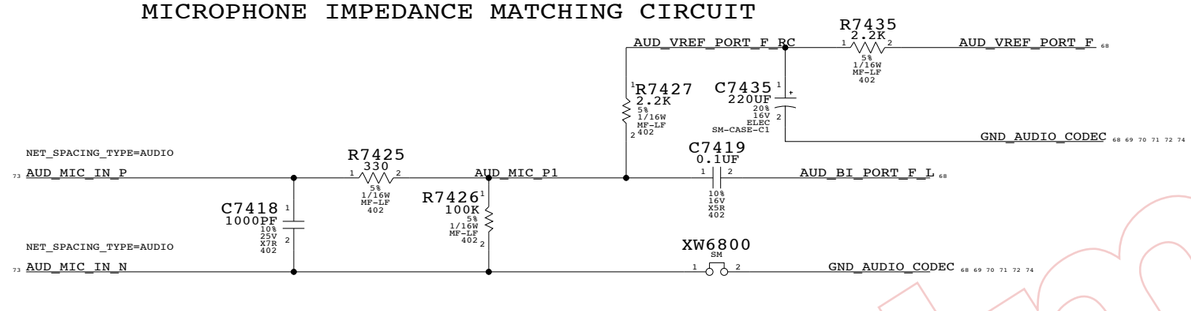
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19(F)	80%
LINE INPUT	0X08	0X23	0X15(A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

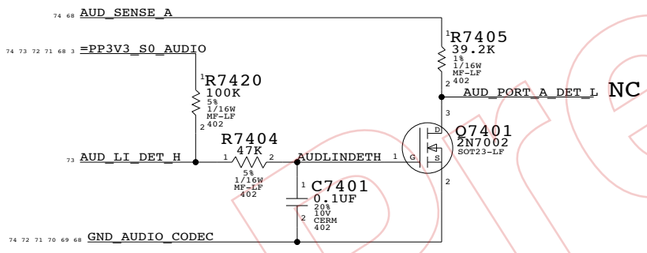
AUDIO GROUND RETURNS



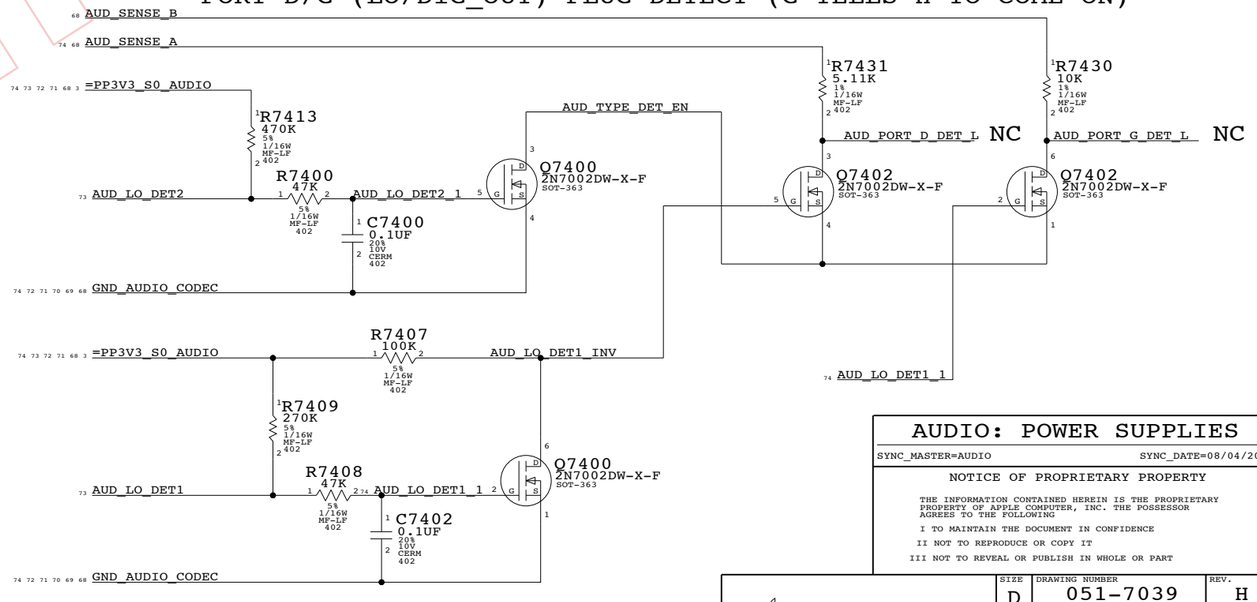
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)

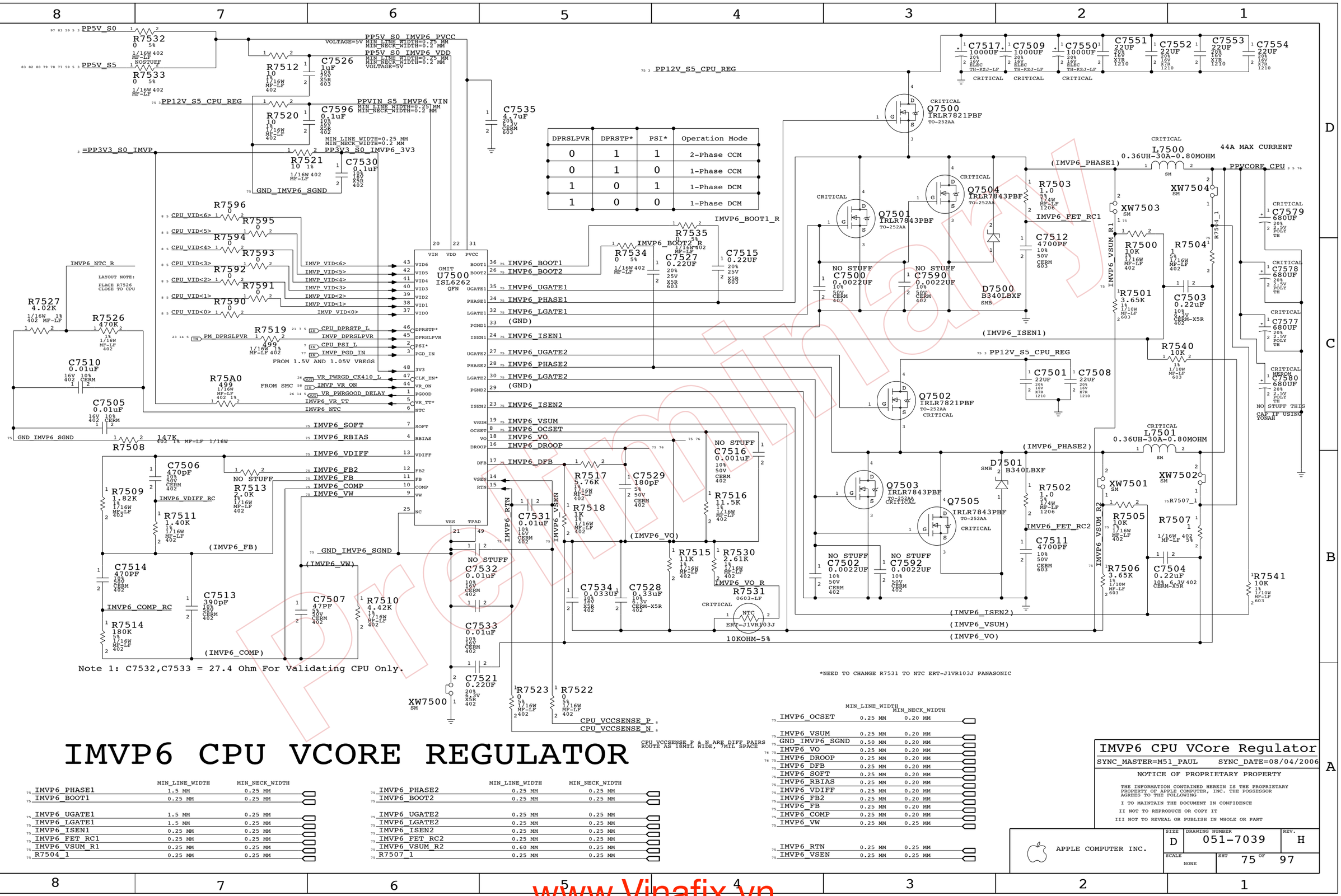


AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 74 OF 97	



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC_MASTER=M51_PAUL	SYNC_DATE=08/04/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 75 OF 97	

PROCESSOR VCORE SENSE

PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)

75 5 3 PPVCORE_CPU — R7612 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_VSENSE 58

C7612 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

C7600 470PF 10% 50V CERM 402 — CPU_ISENSE_OUT_R

R7600 1M 1% 1/16W MF-LF 402

75 IMVP6_VO — R7659 0 5% 1/16W MF-LF 402 — IMVP6_VO_R_OA

84 83 76 45 41 27 26 10 6 5 3 PP3V3_S0 — C7601 0.1UF CERM 20% 10V CRITICAL

U7600 LMV2011MF SOT23-5 — GND_CPU_ISENSE_OPAMP

R7605 40.2K 1% 1/16W MF-LF 402 — CPU_ISENSE_R_POS

75 IMVP6_DROOP — R7669 0 5% 1/16W MF-LF 402 — IMVP6_DROOP_R

R7606 40.2K 1% 1/16W MF-LF 402 — CPU_ISENSE_R_NEG

PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)

R7602 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_ISENSE 58

C7602 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

MIN_LINE_WIDTH=0.20 MM

NOSTUFF R7604 0 5% 1/16W MF-LF 402

C7603 470PF 10% 50V CERM 402 — R7603 1M 1% 1/16W MF-LF 402

R7607 0 5% 1/16W MF-LF 402 — GND_NEXT_TO_SMC 59

CPU CURRENT SENSE CALIBRATION CIRCUIT
Switches in fixed load on power supplies to calibrate current sense circuits

83 3 PP12V_S0_B

R7639 10K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_L — MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.20 MM

Q7640 NTR4101P SOT-23

R7641 10K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_L_R

Q7639 2N7002 SOT23-LF

58 5 ISENSE_CAL_EN — R7640 100K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_LS12V

R7642 470K 5% 1/16W MF-LF 402

9 8 3 =PPVCORE_S0_CPU

R7643 1.00 1% 1/4W MF-LF 1206

CPUVCORE_ISENSE_CAL — MIN_LINE_WIDTH=0.50 mm, MIN_NECK_WIDTH=0.20 mm

CRITICAL Q7641 FDC796N SUPERSOT-6 CPU_PWR_SENSE

SYSTEM CURRENT SENSE

PP12V_S5_AC_DC — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

CRITICAL R7650 0.005 1% MF 2010 — SYS_PWR_SENSE

PP12V_S5 3 76 77 78 79 80 82 83

PCB:KEEP SHORTS NEXT TO U7602
PCB:PLACE D7650,R7652,C7650 BY SMC

SYS_PWR_SENSE

CRITICAL U7602 ZXCT1010 SOT23-5 — 4 VIN, IOUT 3, 1 NC, LOAD 5, GND 2

OMIT XW7650 SM — SYSTEM_DCIN_SENSE 1, 2 SYSTEM_SENSE_I_R

PP3V3_S0 3 5 6 10 26 27 41 45 76 83 84

NOSTUFF D7650 BAS16-75V-0.25A SOT23-LF → TO SMC

R7652 4.53K 1% 1/16W MF-LF 402 — SMC_DCIN_ISENSE 58

C7650 0.22UF 20% 6.3V X5R 402 — 1 MS TIME CONSTANT, SO SMC ADC SAMPLING WORKS WELL.

GND_SMC_AVSS 58 59 76 84

R7651 5.90K 1% 1/16W MF-LF 402

R7656 100 1% 1/16W MF-LF 402 — SYSTEM_SENSE_SET

SCALE	COUNT
3.33333 A/V	.010753 A/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)

SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

83 82 80 79 78 77 76 3 PP12V_S5

R7653 6.04K 1% 1/16W MF-LF 402

R7654 2.0K 1% 1/16W MF-LF 402

SMC_SYSTEM_VSENSE_R

R7655 4.53K 1% 1/16W MF-LF 402 — SMC_PBUS_VSENSE 58

C7651 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)

SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

SMC PWRGD PULLUP

83 80 79 78 77 66 65 26 6 5 3 PP3V3_S5

R7623 10K 1% 1/16W MF-LF 402

NOSTUFF R7620 0 5% 1/16W MF-LF 402

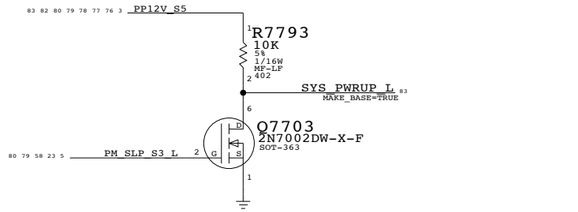
82 78 6 SYS_POWERFAIL_L — RSMRST_PWRGD 58

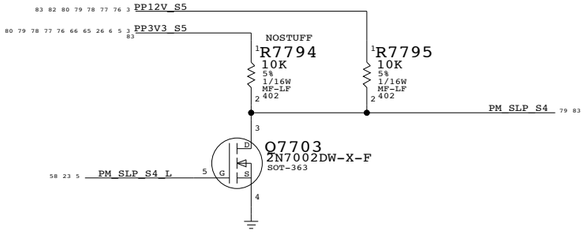
CPU & SYSTEM SENSE

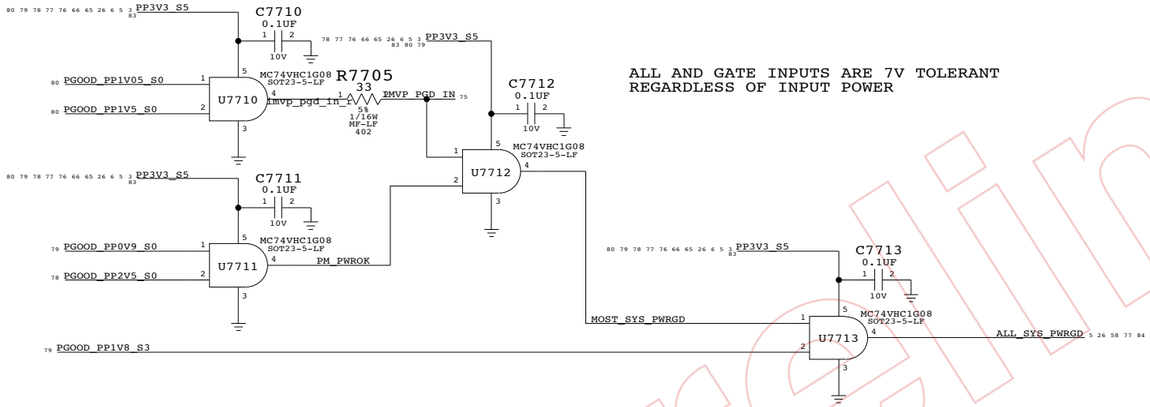
SYNC_MASTER=M51_DAVE — SYNC_DATE=(MASTER)

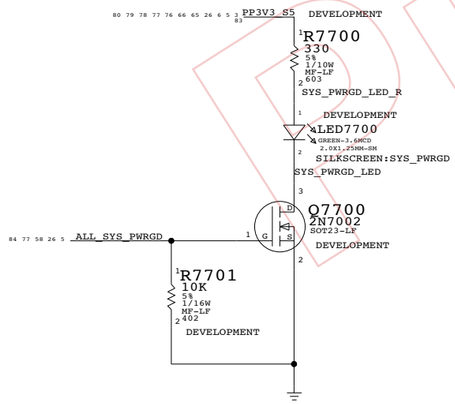
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 76 OF 97	



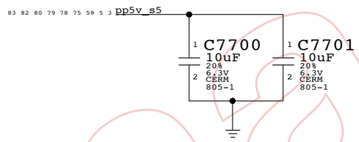






ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 bh page 82



PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 77 OF 97	

3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

3.3V S5
POWER BUDGET
MISC=1.500A
SB=0.500A
AIRPORT=1.000A
PANEL=1.000A
TOTAL=4.000A

=PP3V3_S5_2V5_LDO
C7820 22UF 20% 6.3V X5R 805
Q7803 IRF1902PBF SO-8 CRITICAL

PP12V_S5
C7892 1UF 10% 25V X5R 603
C7800 1UF 10% 6.3V CERM 402

3V3REG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7805 10 1% 1/16W MF-LF 402
3V3REG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7823 1000PF 10% 25V X7R 402
2V5_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7821 2.7K 5% 1/16W MF-LF 402
C7824 1000PF 10% 25V X7R 402
3V3REG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP2V5_S5 2.50V NOMINAL
C7825 10UF 20% 6.3V CERM 805-1
C7822 10UF 20% 6.3V CERM 805-1
C7821 10UF 20% 6.3V CERM 805-1
C7826 10UF 20% 6.3V CERM 805-1
R7820 1K 1% 1/16W MF-LF 402
R7822 470 1% 1/16W MF-LF 402

U7800 ISL6549 QFN
VCC12 CRITICAL
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND AGND PGND
UGATE
BOOT
PHASE
LGATE
FB
COMP

3V3REG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7840 2.2 5% 1/16W MF-LF 402
3V3REG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7801 0.1UF 20% 25V CERM 603
3V3REG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7804 8.06K 1% 1/16W MF-LF 402
C7808 0.047UF 10% 16V CERM 402
3V3REG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7806 560PF 10% 50V CERM 402

Q7800 IRLR7807Z TO-252AA CRITICAL
Q7801 IRLR7807Z TO-252AA CRITICAL
C7853 1000UF 20% 16V ELEC TH-KZJ-LF CRITICAL
C7811 10UF 10% 16V X5R-CERM 1210
L7803 3.0UH TH1 CRITICAL
C7802 1000PF 10% 25V X7R 402
D7800 CDLSH3-30M833 TLM833
nostuff
R7802 5.11 1% 1/4W MF-LF 1206
3V3REG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7809 1000PF 5% 50V CERM 1206
C7815 1800UF 20% 6.3V ELEC TH-KZJ-LF CRITICAL
C7814 10UF 20% 6.3V CERM 805-1
C7813 10UF 20% 6.3V CERM 805-1
PP3V3_S5 3.35V NOMINAL

R7899 22 5% 1/16W MF-LF 402
3V3REG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7807 0.01UF 10% 16V CERM 402
R7803 1.24K 1% 1/16W MF-LF 402 (R2)
R7801 392 1% 1/16W MF-LF 402 (R1)

5% OK ON R7801?
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN / 0.800V TYP / 0.816V MAX

XW7800 SM

3V3REG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7892 100K 5% 1/16W MF-LF 402
NOSTUFF
Q7802 2N7002 SOT23-LF
SYS_POWERFAIL_L
C7803 4.7UF 20% 6.3V CERM 603
3V3REG_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP5V_S5
PP3V3_S5
C7880 0.1UF 20% 10V CERM 402
R7811 2.49K 1% 1/16W MF-LF 402
R7810 10K 1% 1/16W MF-LF 402
2V2_REF 2.219V
U7810 LM339A SOI-LF V+ GND
PP2V5_S0
PGOOD_PP2V5_S0
R7812 5.11K 1% 1/16W MF-LF 402

SPARE COMPARATOR

3V DC/DC 2.5V

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H

SCALE: NONE SHT 78 OF 97

1.8V AND 1.2V S3 REGULATOR

1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A

=PP1V8_S3_1V2_LDO
C7920 22UF 20% 6.3V X5R 805
CRITICAL
Q7903 IRF1902PBF SO-8
C7992 1UF 10% 25V X5R 603
PP12V_S5
1V8REG_DDR_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7905 10 1% 1/16W MF-LF 402
C7900 1UF 10% 6.3V CERM 402
1V8REG_DDR_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7923 1000PF 10% 25V X7R 402
1V2_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7921 2.7K 5% 1/16W MF-LF 402
C7924 1000PF 10% 25V X7R 402
PP1V2_S3 1.21V NOMINAL
R7920 1K 1% 1/16W MF-LF 402
C7925 10UF 20% 6.3V CERM 805-1
C7922 10UF 20% 6.3V CERM 805-1
C7921 10UF 20% 6.3V CERM 805-1
C7926 10UF 20% 6.3V CERM 805-1
R7922 1.96K 1% 1/16W MF-LF 402
1V8REG_DDR_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7992 100K 5% 1/16W MF-LF 402
Q7902 2N7002 SOT23-LF
PM_SLP_S4
C7903 4.7UF 20% 6.3V CERM 603
1V8REG_DDR_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
PM_SLP_S3_L
MEMVTT_EN

VCC12
U7900 ISL6549 QFN
CRITICAL
VCC5 PVCC5 LDO_DR LDO_FB FS_DIS THRML_PAD DGND AGND PGND
UGATE BOOT PHASE LGATE FB COMP

1V8REG_DDR_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7940 2.2 5% 1/16W MF-LF 402
1V8REG_DDR_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7901 0.1UF 20% 25V CERM 603
1V8REG_DDR_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7904 8.06K 1% 1/16W MF-LF 402
C7908 0.047UF 10% 16V CERM 402
1V8REG_DDR_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7906 560PF 10% 50V CERM 402
XW7900 SM

Q7900 IRLR7807Z TO-252AA
Q7901 IRLR7807Z TO-252AA
C7902 1000PF 10% 25V X7R 402
D7900 CTLSH3-30M833 TLM833
nostuff
L7903 1.53UH TH-LF CRITICAL
R7902 5.11 1% 1/4W MF-LF 1206
1V8REG_DDR_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7909 1000PF 5% 50V CERM 1206

CRITICAL C7953 680UF 20% 16V ELEC TH-MCZ
CRITICAL C7954 680UF 20% 16V ELEC TH-MCZ
C7911 10UF 10% 16V X5R-CERM 1210
C7912 10UF 10% 16V X5R-CERM 1210
1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A
CRITICAL C7956 1500UF 20% 6.3V ELEC TH-MCZ
CRITICAL C7957 1500UF 20% 6.3V ELEC TH-MCZ
C7913 10UF 10% 6.3V CERM 805-1
C7958 1UF 10% 6.3V CERM 402
C7959 1UF 10% 6.3V CERM 402
C7960 1UF 10% 6.3V CERM 402
PP1V8_S3 1.81V NOMINAL
R7999 22 5% 1/16W MF-LF 402
R7903 1.24K 1% 1/16W MF-LF 402 (R2)
1V8REG_DDR_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7907 0.01UF 10% 16V CERM 402
R7901 953 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN / 0.800V TYP / 0.816V MAX

PP5V_S5
PP3V3_S5
R7911 5.49K 1% 1/16W MF-LF 402
R7910 10K 1% 1/16W MF-LF 402
1V2_REF 1.21V
U7810 LM339A SOI-LF GND V+
PGOOD_PP1V8_S3
PP1V8_S3
R7912 2.7K 5% 1/16W MF-LF 402

PP5V_S5
PP3V3_S5
R7914 8.45K 1% 1/16W MF-LF 402
R7913 10K 1% 1/16W MF-LF 402
0V7_REF 0.723V
U7810 LM339A SOI-LF GND V+
PGOOD_PP0V9_S0
PP0V9_S0
R7915 2.37K 1% 1/16W MF-LF 402

PP3V3_S5
DEVELOPMENT
R7906 330 5% 1/16W MF-LF 402
LED_PP1V8_S3_P
DEVELOPMENT
LED7900 GREEN-3.6MCD 2.0X1.25MM-SM
PLACE_LED NEAR VREG
PP1V8_S3
U7901 DEVELOPMENT LM339A SOI-LF GND V+
1V0_REF
LED_PP1V8_S3_N

1.8V & 1.2V VREG
SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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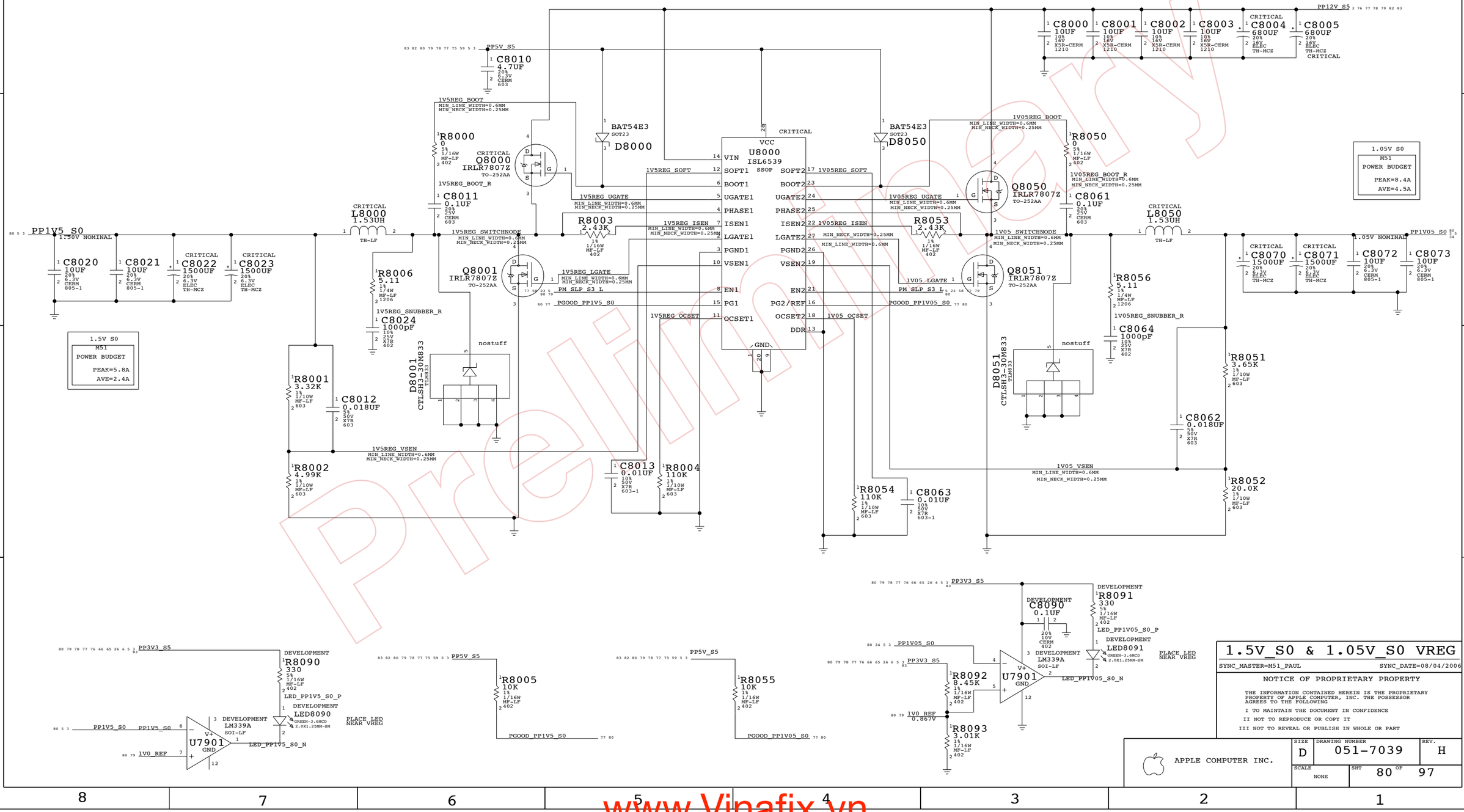
APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-7039 | REV. H
SCALE NONE | SHT 79 OF 97

1.5V S0 AND 1.05V S0 RAILS



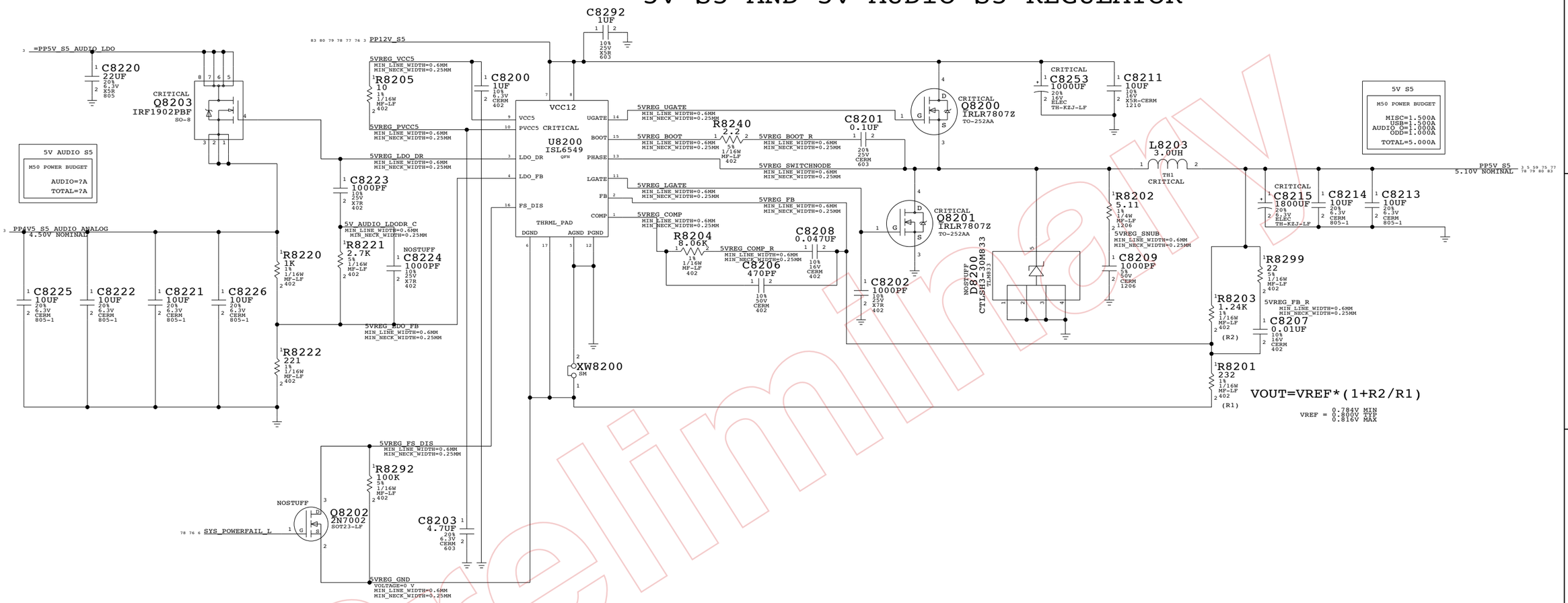
1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 80 OF 97	

5V S5 AND 5V AUDIO S5 REGULATOR



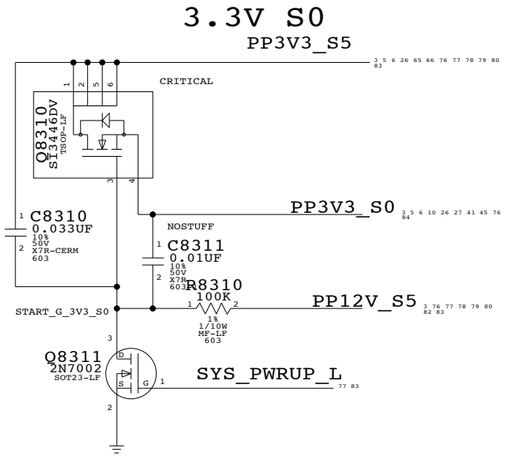
POWER SUPPLY 3.3V/5V MAIN SWITCH

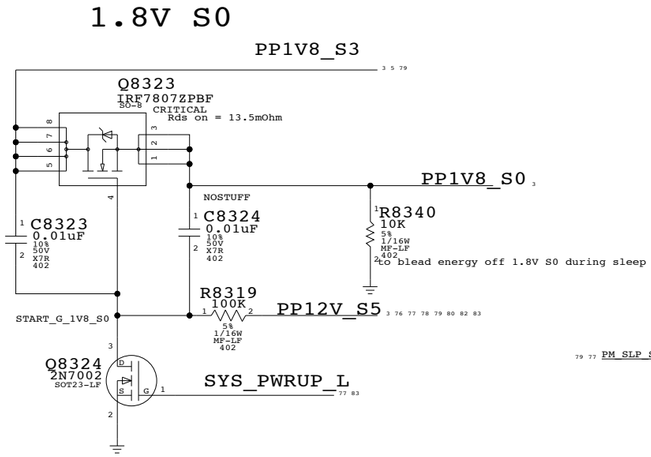
5V DC/DC

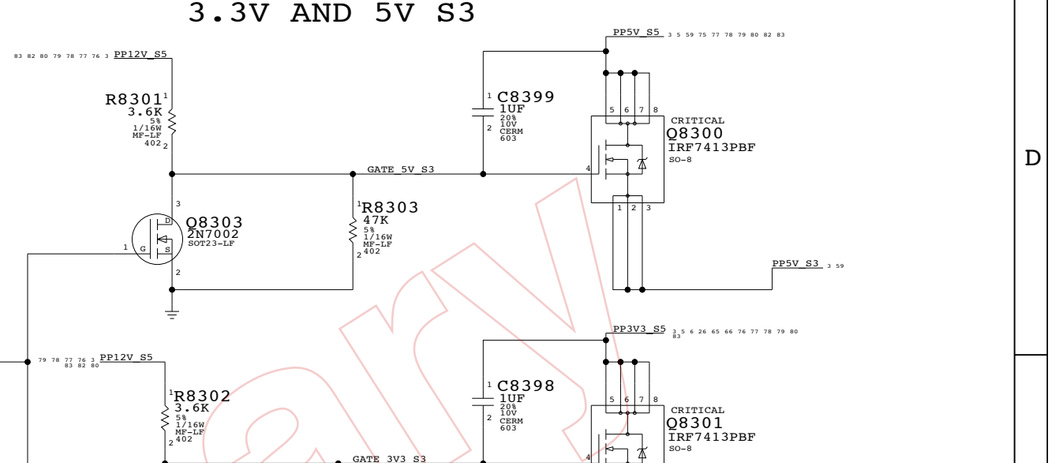
SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

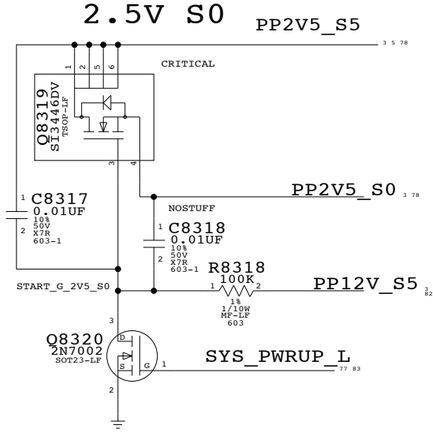
APPLE COMPUTER INC.

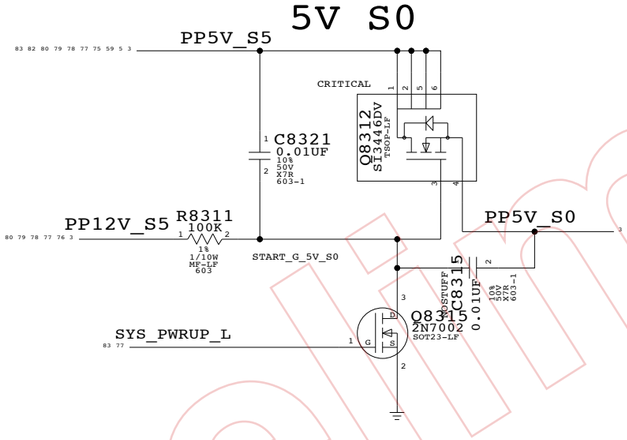
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 82 OF 97	

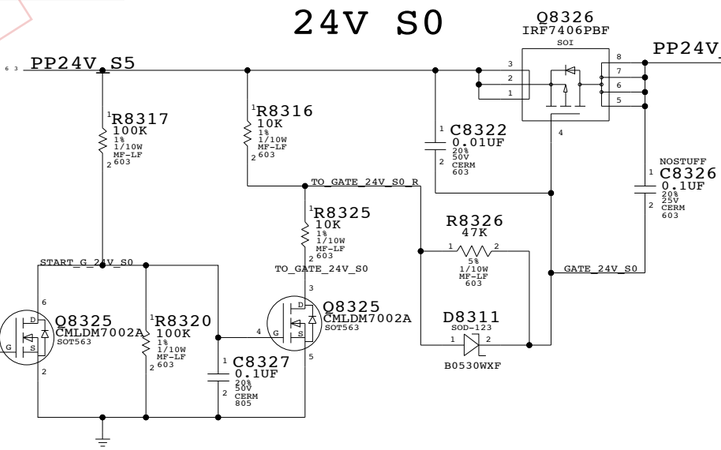


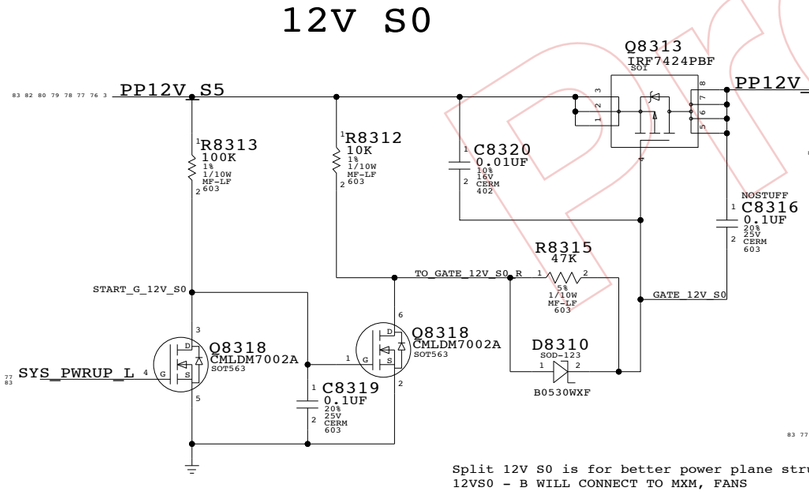




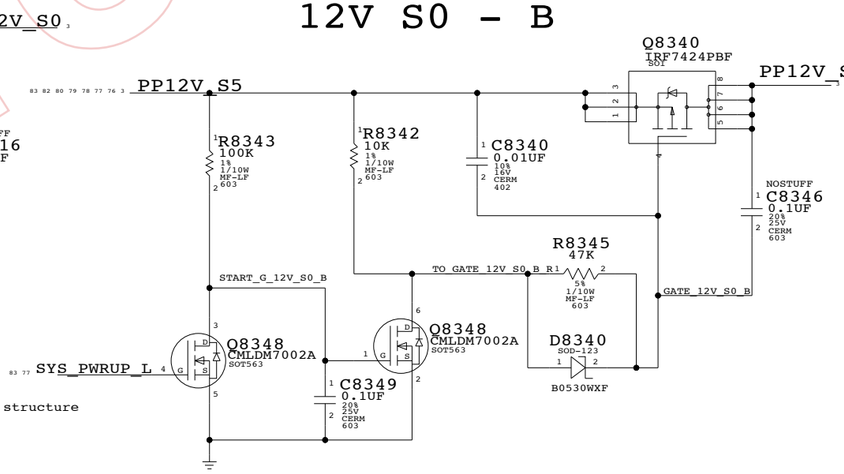








Split 12V S0 is for better power plane structure
12VS0 - B WILL CONNECT TO MXM, FANS



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 83 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

=PP1V8_S0_MXM
C8401 22UF 20% 6.3V X5R 805
C8402 22UF 20% 6.3V X5R 805 NOSTUFF
C8403 22UF 20% 6.3V X5R 805 NOSTUFF
=PP5V_S0_MXM
ALL_SYS_PWRGD

CRITICAL
J8400 B33@102-0123 F-RT-SM (1 OF 2)

2	1V8RUN0	PWR_SRC0	1
4	1V8RUN1	PWR_SRC1	3
6	1V8RUN2	PWR_SRC2	5
8	1V8RUN3	PWR_SRC3	7
10	1V8RUN4	PWR_SRC4	9
12	1V8RUN5	PWR_SRC5	11
14	1V8RUN6	PWR_SRC6	13
16	RUNPWROK	PWR_SRC7	15
18	5VRUN	GND0	17
20	GND20	GND1	19
22	GND21	GND2	21
24	GND22	GND3	23
	KEY		
38	PRSNT2_L	PEX_RX15_L	37
40	PEX_TX15_L	PEX_RX15	39
42	PEX_TX15	GND4	41
44	GND23	PEX_RX14_L	43
46	PEX_TX14_L	PEX_RX14	45
48	PEX_TX14	GND5	47
50	GND24	PEX_RX13_L	49
52	PEX_TX13_L	PEX_RX13	51
54	PEX_TX13	GND6	53
56	GND25	PEX_RX12_L	55
58	PEX_TX12_L	PEX_RX12	57
60	PEX_TX12	GND7	59
62	GND26	PEX_RX11_L	61
64	PEX_TX11_L	PEX_RX11	63
66	PEX_TX11	GND8	65
68	GND27	PEX_RX10_L	67
70	PEX_TX10_L	PEX_RX10	69
72	PEX_TX10	GND9	71
74	GND28	PEX_RX9_L	73
76	PEX_TX9_L	PEX_RX9	75
78	PEX_TX9	GND10	77
80	GND29	PEX_RX8_L	79
82	PEX_TX8_L	PEX_RX8	81
84	PEX_TX8	GND11	83
86	GND30	PEX_RX7_L	85
88	PEX_TX7_L	PEX_RX7	87
90	PEX_TX7	GND12	89
92	GND31	PEX_RX6_L	91
94	PEX_TX6_L	PEX_RX6	93
96	PEX_TX6	GND13	95
98	GND32	PEX_RX5_L	97
100	PEX_TX5_L	PEX_RX5	99
102	PEX_TX5	GND14	101
104	GND33	PEX_RX4_L	103
106	PEX_TX4_L	PEX_RX4	105
108	PEX_TX4	GND15	107
110	GND34	PEX_RX3_L	109
112	PEX_TX3_L	PEX_RX3	111
114	PEX_TX3	GND16	113
116	GND35	PEX_RX2_L	115
118	PEX_TX2_L	PEX_RX2	117
120	PEX_TX2	GND17	119
122	GND36	PEX_RX1_L	121
124	PEX_TX1_L	PEX_RX1	123
126	PEX_TX1	GND18	125
128	GND37	PEX_RX0_L	127
130	PEX_TX0_L	PEX_RX0	129
132	PEX_TX0	GND19	131

PRSNT2_L: RESERVED FOR FUTURE USE

PPV_S0_MXM_PWRSRC (VOLTAGE=12V MIN_LINE_WIDTH=0.404MM MIN_NECK_WIDTH=0.254MM)
C8400 22UF 20% 35V ELEC SM-LF

PLACE CAPS NEAR NB

PEG_R2D_C_P<0>	C8420	PEG_R2D_P<15>	PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8421	PEG_R2D_N<15>	PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8422	PEG_R2D_P<14>	PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8423	PEG_R2D_N<14>	PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8424	PEG_R2D_P<13>	PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8425	PEG_R2D_N<13>	PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8426	PEG_R2D_P<12>	PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8427	PEG_R2D_N<12>	PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8428	PEG_R2D_P<11>	PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8429	PEG_R2D_N<11>	PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8430	PEG_R2D_P<10>	PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8431	PEG_R2D_N<10>	PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8432	PEG_R2D_P<9>	PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8433	PEG_R2D_N<9>	PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8434	PEG_R2D_P<8>	PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8435	PEG_R2D_N<8>	PEG_D2R_N<7>
PEG_R2D_C_P<8>	C8436	PEG_R2D_P<7>	PEG_D2R_P<8>
PEG_R2D_C_N<8>	C8437	PEG_R2D_N<7>	PEG_D2R_N<8>
PEG_R2D_C_P<9>	C8438	PEG_R2D_P<6>	PEG_D2R_P<9>
PEG_R2D_C_N<9>	C8439	PEG_R2D_N<6>	PEG_D2R_N<9>
PEG_R2D_C_P<10>	C8440	PEG_R2D_P<5>	PEG_D2R_P<10>
PEG_R2D_C_N<10>	C8441	PEG_R2D_N<5>	PEG_D2R_N<10>
PEG_R2D_C_P<11>	C8442	PEG_R2D_P<4>	PEG_D2R_P<11>
PEG_R2D_C_N<11>	C8443	PEG_R2D_N<4>	PEG_D2R_N<11>
PEG_R2D_C_P<12>	C8444	PEG_R2D_P<3>	PEG_D2R_P<12>
PEG_R2D_C_N<12>	C8445	PEG_R2D_N<3>	PEG_D2R_N<12>
PEG_R2D_C_P<13>	C8446	PEG_R2D_P<2>	PEG_D2R_P<13>
PEG_R2D_C_N<13>	C8447	PEG_R2D_N<2>	PEG_D2R_N<13>
PEG_R2D_C_P<14>	C8448	PEG_R2D_P<1>	PEG_D2R_P<14>
PEG_R2D_C_N<14>	C8449	PEG_R2D_N<1>	PEG_D2R_N<14>
PEG_R2D_C_P<15>	C8450	PEG_R2D_P<0>	PEG_D2R_P<15>
PEG_R2D_C_N<15>	C8451	PEG_R2D_N<0>	PEG_D2R_N<15>

All 0.1uF 10% 16V X5R 402

MXM PWRSRC (GPU CORE) CURRENT SENSE

=PPV_S0_MXM_PWRSRC
CRITICAL R8450 0.025 1% 1/2W MF 2512-1 MXM_PWR_SENSE
PPV_S0_MXM_PWRSRC
PCB:KEEP SHORTS NEXT TO U8450
PCB:PLACE D8450,R8452,C8458 BY SMC
CRITICAL U8450 ZXCT1010 SOT23-5 MXM_PWR_SENSE
VIN IOUT NC LOAD GND
PP3V3_S0
NOSTUFF D8450 BAS16-75V-0.25A SOT23-LF → TO SMC
OMIT XW8450 SM MXM_PWRSRC_SENSE MXM_SENSE_I_R
MXM_PWR_SENSE R8452 4.53K 1% 1/16W MF-LF 402
SMC_GPU_ISENSE
MXM_PWR_SENSE R8451 3.01K 1% 1/16W MF-LF 402
MXM_PWR_SENSE C8458 0.22UF 20% 6.3V X5R 402 1MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.
GND_SMC_AVSS

SCALE COUNT
1.33333 A/V .004296875 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

MXM PWRSRC VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

PPV_S0_MXM_PWRSRC
MXM_PWR_SENSE R8453 6.04K 1% 1/16W MF-LF 402
SMC_MXM_VSENSE_R
MXM_PWR_SENSE R8454 2.0K 1% 1/16W MF-LF 402
MXM_PWR_SENSE R8455 4.53K 1% 1/16W MF-LF 402
PCB: PLACE R8455, C8459 WITHIN 1" OF SMC (U5800)
SMC_GPU_VSENSE
MXM_PWR_SENSE C8459 0.22UF 20% 6.3V X5R 402
GND_SMC_AVSS

SCALE COUNT
4 V/V .0129 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 84 OF 97	

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)

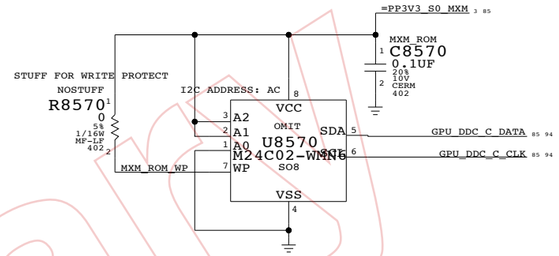
MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

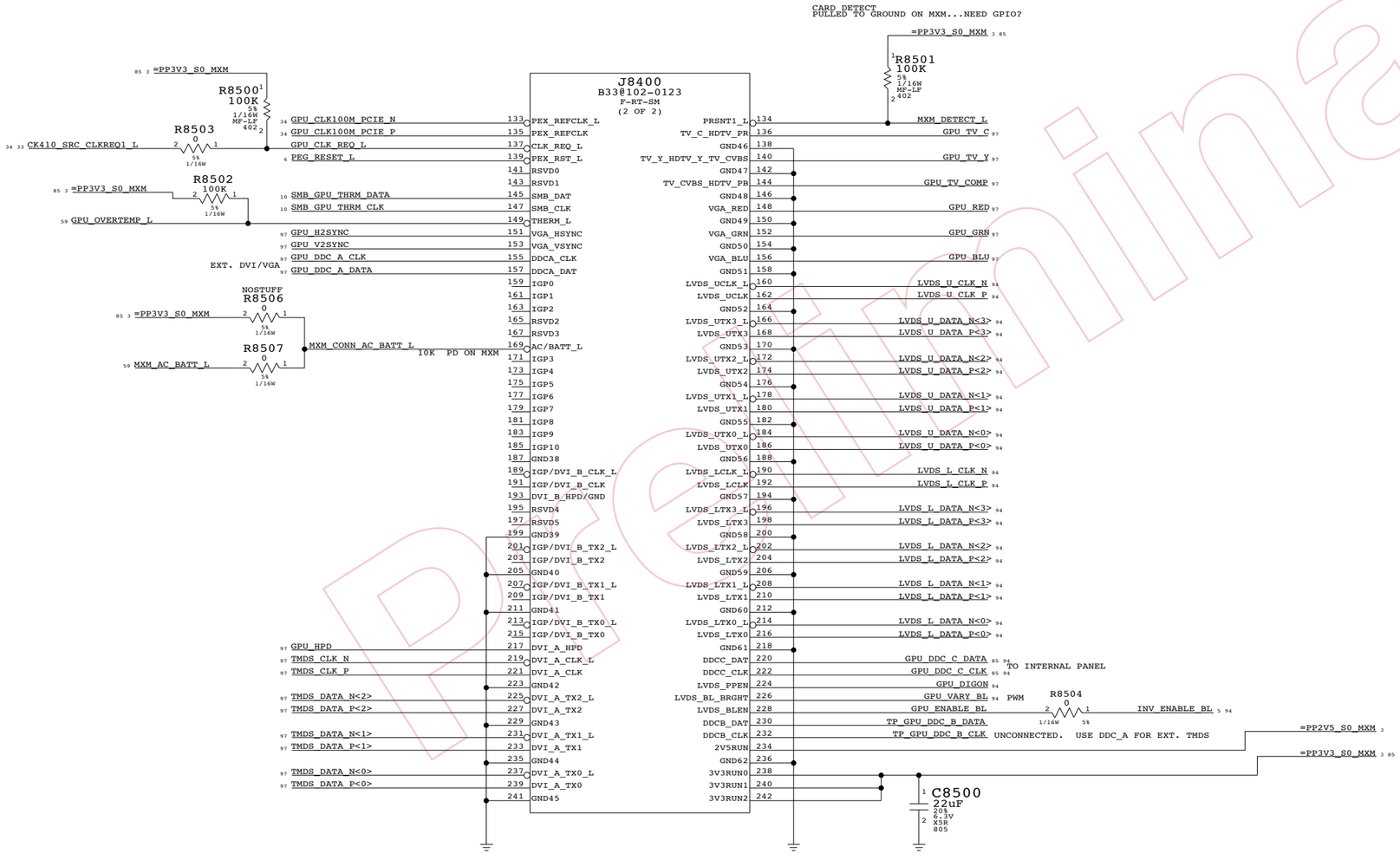
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



CARD DETECT
PULLED TO GROUND ON MXM...NEED GPIO?



MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 85 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

3 =PPV_S0_LCD

NOSTUFF R9490 0 5% 1/8W MF-LF 805

R9400 100K 5% 1/16W MF-LF 402

C9400 0.1UF 10% 50V X7R 603-1

PLACE NEAR J9402

R9401 29.4K 1% 1/16W MF-LF 402

LCD_PWREN_DIV

LCD_PWREN_L_RC

Q9400 SI3443DV TSOP-LF

PP12V_LCD_SW

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

L9400 FERR-250-OHM SM

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

PP12V_LCD_CONN 6 94

C9420 10UF 10% 16V X5R-CERM 1210

C9401 0.001uF 20% 50V CERM 402

R9499 100K 5% 1/16W MF-LF 402

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

85 GPU_DIGON

R9470 100K 5% 1/16W MF-LF 402

CRITICAL
SDF9400
STDOFF-3MMOD4.6MMH-1.35-TH

CRITICAL
J9402
53307-3072
F-ST-SM

85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0> 85
85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1> 85
85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2> 85
	7	8	LVDS_U_CLK_N 85
85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3> 85
85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0> 85
85 LVDS_L_DATA_P<0>	13	14	
85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1> 85
	17	18	LVDS_L_DATA_N<2> 85
85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N 85
85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3> 85
85 LVDS_L_DATA_P<3>	23	24	
85 GPU_DDC_C_CLK	25	26	GPU_DDC_C_DATA 85
	27	28	
	29	30	

94 =PP3V3_DDC_LCD

94 6 PP12V_LCD_CONN

PP12V_LCD_CONN 6 94

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9410 0.001uF 20% 50V CERM 402

CRITICAL
SDF9401
STDOFF-3MMOD4.6MMH-1.35-TH

INVERTER INTERFACE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS

CRITICAL
J9400
88290-14XG
M-ST-SM

3 =PPV_S0_INVERTER

C9440 2.2UF 10% 50V X7R 1206

97 94 3 =PP3V3_S0_VIDEO

NOSTUFF R9440 10K 5% 1/16W MF-LF 402

85 INV_ENABLE_BL

94 5 LCD_PWM

85 GPU_VARY_BL

R9475 47 5% 1/16W MF-LF 402

LCD_PWM 5 94

NOSTUFF R9474 10K 5% 1/16W MF-LF 402

Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

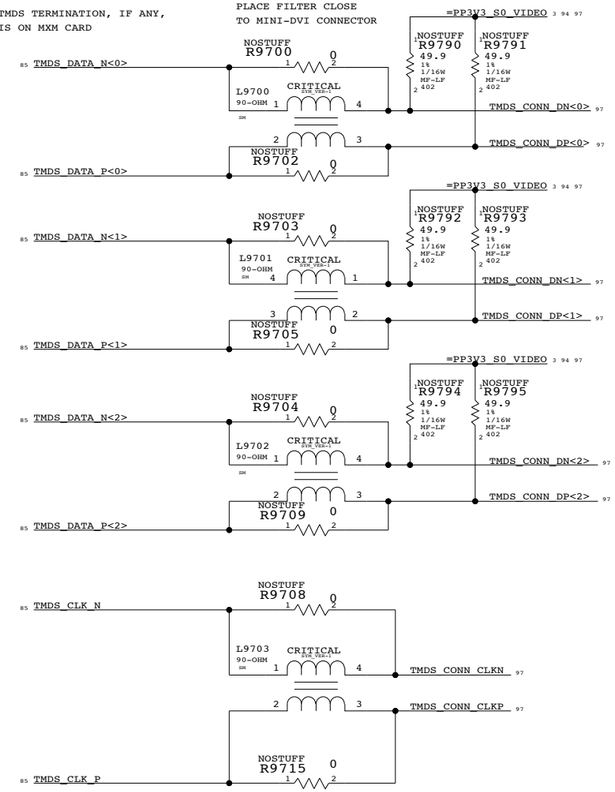
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE: NONE	SHT 94 OF 97	

DVI INTERFACE

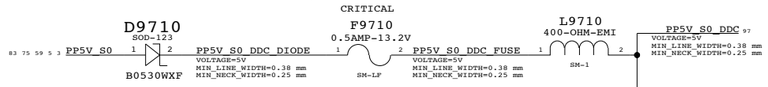
TMDS TERMINATION, IF ANY, IS ON MXM CARD

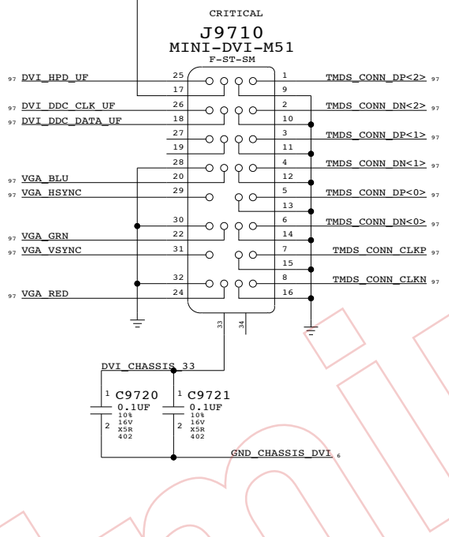
PLACE FILTER CLOSE TO MINI-DVI CONNECTOR



DVI DDC CURRENT LIMIT

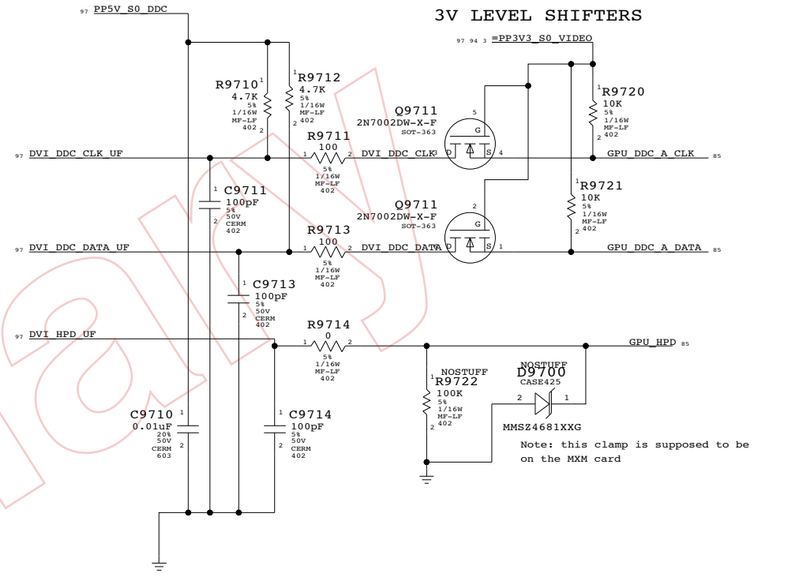
(55mA requirement per DVI spec)





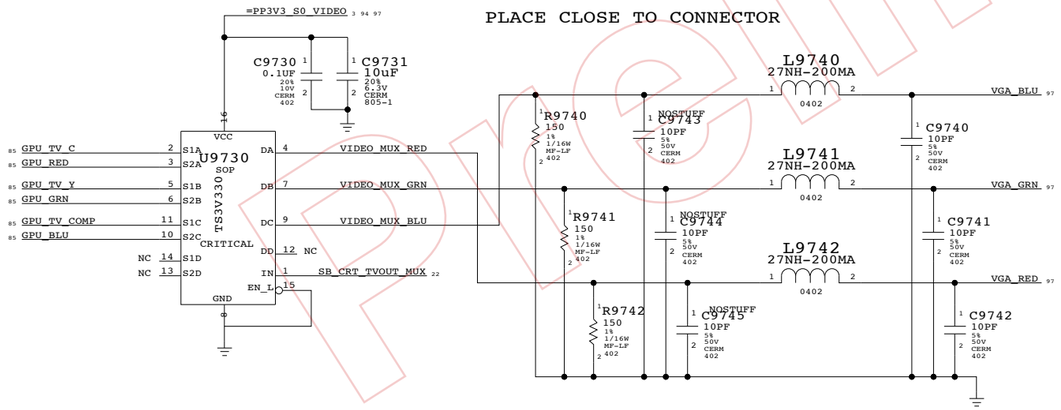
PLACE CLOSE TO MINI-DVI CONNECTOR

3V LEVEL SHIFTERS

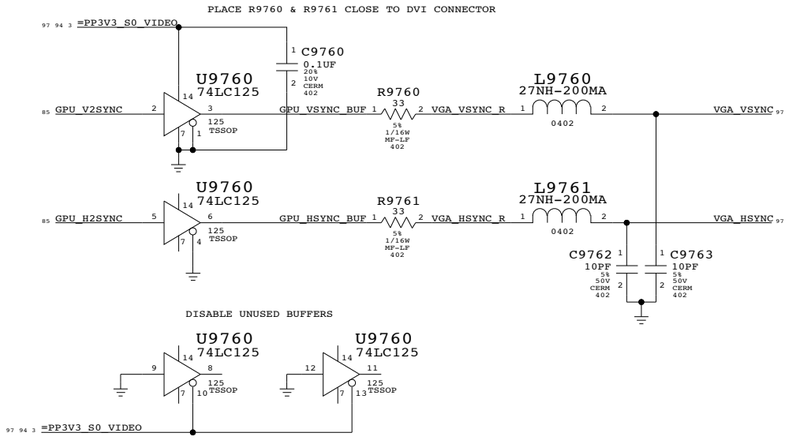


ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR



External Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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	SCALE: NONE	SHT 97 OF 97	