1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# SANTANA - M51 MLB

## DVT -- 06/29/06

| REV | ZONE | ECN | DESCRIPTION OF CHANGE | CK APPD DATE | ENG APPD DATE |
|---|---|---|---|---|---|
| 21 | | 446951 | ENGINEERING RELEASED | 06/29/06 | 06/22/04 |



### Schematic / PCB #'s

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 051-7039 | 1 | PCB,SCHEM,MLB,M51 | SCH1 | | |
| 820-1984 | 1 | PCB,FAB,MLB,M51 | MLB1 | | |



DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

| | | | |
|---|---|---|---|
| DRAFTER | | DESIGN CK | |
| ENG APPD | | MFG APPD | |
| QA APPD | | DESIGNER | |
| RELEASE | | SCALE | NONE |

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

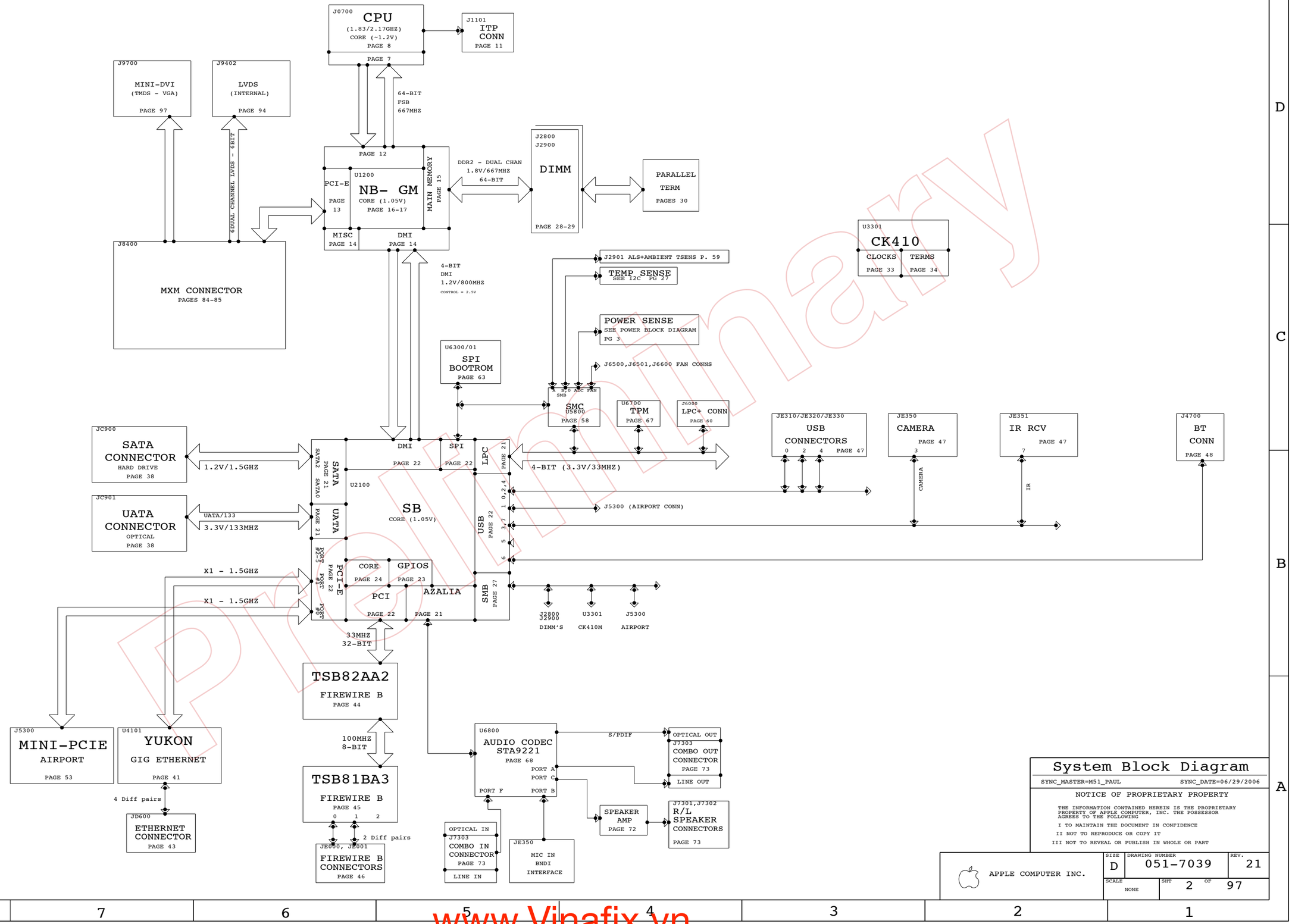
Apple Computer Inc.



TITLE
SCHEM SANTANA

DRAWING NUMBER 051-7039 REV. 21

SHT 1 OF 97



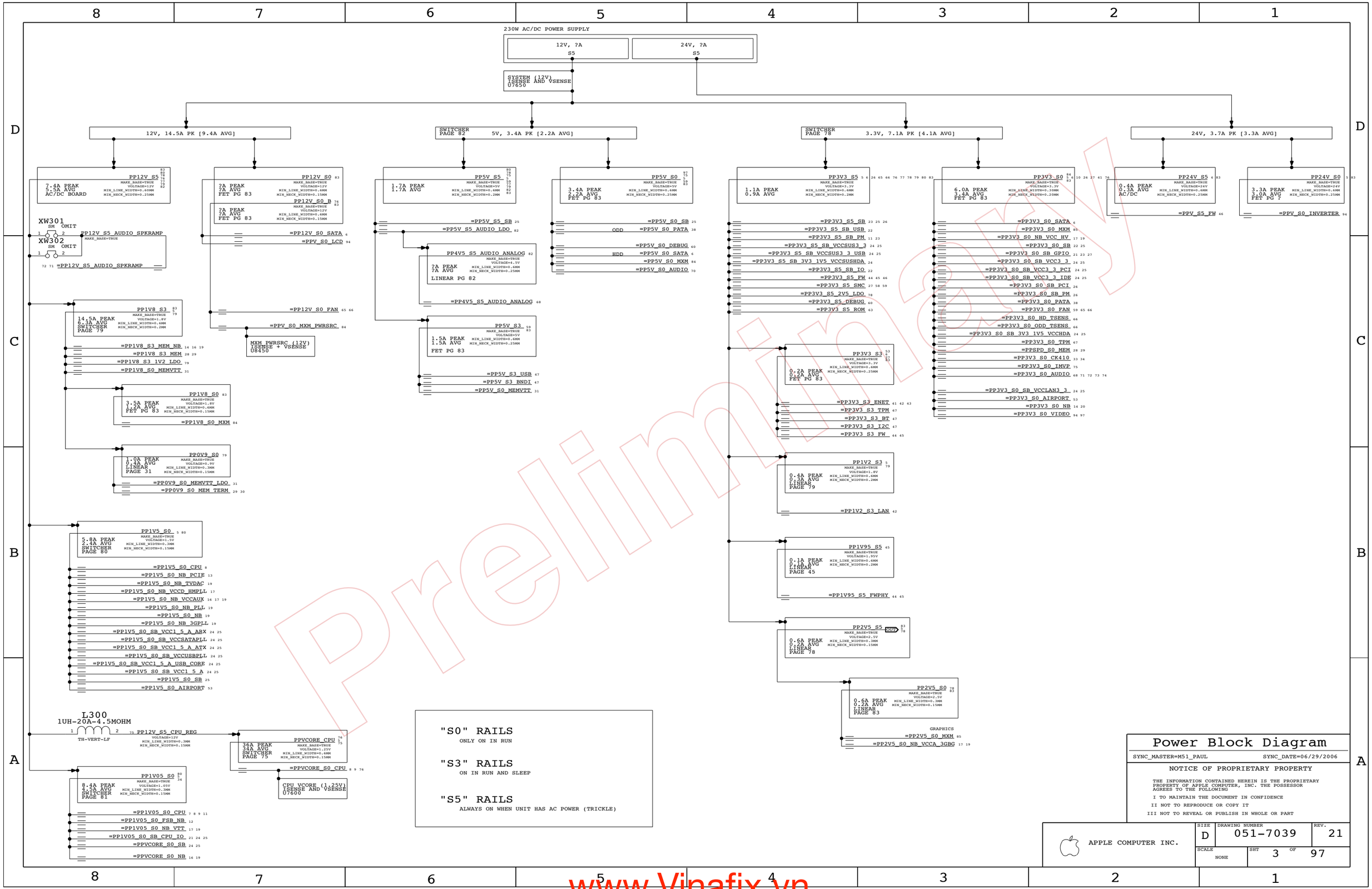

# System Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 2 OF 97 | |



## Production BOM

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 630-7512 | PCBA,MLB,2.33GHz,M51 | M51_COMMON,M51_BEST,EEE_V4K |
| 630-7595 | PCBA,MLB,2.16GHz,M51 | M51_COMMON,M51_BETTER,EEE_VMD,PRODUCTION |

## Development BOM

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 603-8960 | PCBA,DEVBOM,M51 | M51_DEVELOPMENT |

## BOMOPTION Groups

| BOM GROUP | BOM OPTIONS |
|---|---|
| M51_COMMON | COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE |
| M51_COMMON1 | CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE |
| M51_COMMON2 | SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSENS,CPU_PWR_SENSE,MXM_PWR_SENSE |
| M51_DEVELOPMENT | DEVELOPMENT,M51_DEV1 |
| M51_DEV1 | CPU_TSENS_INT,SYS_PWR_SENSE |

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

## BarCode Label / EEE #'s

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 825-6447 | 1 | BAR CODE LABLE, MLB, M51 | [EEE:VMD] | CRITICAL | EEE_VMD |
| 825-6447 | 1 | BAR CODE LABLE, MLB, M51 | [EEE:V4K] | CRITICAL | EEE_V4K |

## Module Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 511S0025 | 1 | IC,CPU-SKT,479BGA | J0700 | CRITICAL | |
| 338S0328 | 1 | IC,945PM,NORTHBRIDGE | U1200 | CRITICAL | |
| 343S0385 | 1 | IC,SB,652BGA | U2100 | CRITICAL | |
| 359S0101 | 1 | IC,CY28445-5,CLK GEN,68PIN QFN | U3301 | CRITICAL | |
| 338S0270 | 1 | IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO | U4101 | CRITICAL | |
| (335S0382) 341S1797 | 1 | IC,ENET LAN ROM | U4102 | CRITICAL | |
| 341S1789 | 1 | IC,TPM,TSSOP,28P | U6700 | CRITICAL | TPM |
| 353S1465 | 1 | IC,CPU VREG,IMVP,TWO PHASE,SCREENED | U7500 | CRITICAL | |
| 341S1892 | 1 | IC,2K I2C EEPROM,MXM,M51 | U8570 | CRITICAL | MXM_ROM |

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| (335S0384) 341T0019 | 1 | IC,EFI BOOT ROM,M51 | U6301 | CRITICAL | |
| (338S0274) 341T0020 | 1 | IC,SMC,M51 | U5800 | CRITICAL | |
| 337S3292 | 1 | MEROM 2.3GHZ, M51 | CPU | CRITICAL | M51_BEST |
| 337S3293 | 1 | MEROM 2.16GHZ, M51 | CPU | CRITICAL | M51_BETTER |

## Misc. Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 742-0048 | 1 | BAT,COIN,3V,220MAH,CR2032 | BT2600 | CRITICAL | NOSTUFF |
| 820-2038 | 1 | IO ALIGNMENT BOARD, M51 | PCB2 | CRITICAL | |
| 946-0743 | 1 | IO ALIGNMENT BOARD ADHESIVE | ADH1 | CRITICAL | |

BATTERY IS INSTALLED AT FATP

FOR DVT, TRYING AN EVEN BRIGHTER LED ON 2.16GHZ CONFIG

| | | | | | |
|---|---|---|---|---|---|
| 378S0199 | 1 | LED,WHITE,DUAL,2500MCD,SMD | LED5950 | CRITICAL | M51_BETTER |
| 378S0193 | 1 | LED,WHITE,740MCD,LF,3X2MM | LED5950 | CRITICAL | M51_BEST |

## Alternate Parts

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 126S0086 | 126S0078 | | ALL | Sanyo alt for Nich. |
| 126S0099 | 126S0073 | | ALL | Sanyo alt for Nich. |
| 126S0068 | 126S0088 | | ALL | Sanyo alt for Nich. |
| 124-0361 | 124-0339 | | ALL | SANYO ALT |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 378S0141 | 378S0140 | | ALL | GREEN LED ALT. |
| 359S0117 | 359S0101 | | U3301 | SILEGO CK410 CLOCK |
| 353S1461 | 353S1465 | | U7500 | CPU VREG NEW REV |
| 740S0044 | 740S0028 | | F9710 | DVI DDC (LITTLEFUSE) |
| 516S0511 | 516S0460 | | J8400 | MXM CONN SPEEDTECH |

## SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 102S0699 | 1 | RES,0-OHM,2010 | R7650 | PRODUCTION |
| 116S0090 | 1 | RES,10K-OHM,5%,0402 | C7650 | PRODUCTION |
| 116S0090 | 1 | RES,10K-OHM,5%,0402 | C7650 | PRODUCTION |

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 107S0070 | 1 | RES,0-OHM,2512 | R8450 | NOSTUFF |
| 116S0090 | 1 | RES,10K-OHM,5%,0402 | C8458 | NOSTUFF |
| 116S0090 | 1 | RES,10K-OHM,5%,0402 | C8459 | NOSTUFF |

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 116S0090 | 1 | RES,10K-OHM,5%,0402 | C7602 | NOSTUFF |
| 116S0090 | 1 | RES,10K-OHM,5%,0402 | C7612 | NOSTUFF |

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

## BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE NONE SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 OMIT P4MM

34 22 PCI_CLK_SB PP6D0 OMIT P4MM
44 34 PCI_CLK_FW PP626 OMIT P4MM
58 34 PCI_CLK_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 OMIT P4MM
38 21 IDE_PDIORDY PP6C7 OMIT P4MM
38 21 IDE_PDD<9> PP6C8 OMIT P4MM

54 22 PCIE_B_D2R_P PP600 OMIT P4MM
54 22 PCIE_B_D2R_N PP601 OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 OMIT P4MM
63 58 22 SPI_SO PP612 OMIT P4MM
63 58 22 SPI_SI PP613 OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 OMIT P4MM
27 SMBUS_SB_SDA PP605 OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 OMIT P4MM

## FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 OMIT P4MM

I473
14 NB_CFG<17> — NC_NB_CFG<17> MAKE_BASE=TRUE
I474
14 NB_CFG<15> — NC_NB_CFG<15> MAKE_BASE=TRUE
I475
14 NB_CFG<14> — NC_NB_CFG<14> MAKE_BASE=TRUE
I476
14 NB_CFG<13> — NC_NB_CFG<13> MAKE_BASE=TRUE
I477
14 NB_CFG<12> — NC_NB_CFG<12> MAKE_BASE=TRUE
I478
14 NB_CFG<11> — NC_NB_CFG<11> MAKE_BASE=TRUE
I479
14 NB_CFG<10> — NC_NB_CFG<10> MAKE_BASE=TRUE
I481
14 NB_CFG<8> — NC_NB_CFG<8> MAKE_BASE=TRUE
I480
14 NB_CFG<6> — NC_NB_CFG<6> MAKE_BASE=TRUE
I482
14 NB_CFG<4> — NC_NB_CFG<4> MAKE_BASE=TRUE
I483
14 NB_CFG<3> — NC_NB_CFG<3> MAKE_BASE=TRUE

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 OMIT P4MM
14 NB_RST_IN_L_R PP666 OMIT P4MM

22 14 DMI_S2N_N<0> PP673 OMIT P4MM
22 14 DMI_S2N_P<0> PP674 OMIT P4MM
19 14 MEM_VREF_NB_0 PP6E1 OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 OMIT P4MM

I513
22 PCI_GNT3_L — TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT
22 USB_F_N — TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P — TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
19 13 LVDS_BKLTEN — TP_LVDS_BKLTEN MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN PEG_R2D_C_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<15> NO_TEST=TRUE

84 13 IN PEG_R2D_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_P<15> NO_TEST=TRUE

84 13 IN PEG_D2R_N<0> NO_TEST=TRUE
84 13 IN PEG_D2R_P<0> NO_TEST=TRUE
84 13 IN PEG_D2R_N<1> NO_TEST=TRUE
84 13 IN PEG_D2R_P<1> NO_TEST=TRUE
84 13 IN PEG_D2R_N<2> NO_TEST=TRUE
84 13 IN PEG_D2R_P<2> NO_TEST=TRUE
84 13 IN PEG_D2R_N<3> NO_TEST=TRUE
84 13 IN PEG_D2R_P<3> NO_TEST=TRUE
84 13 IN PEG_D2R_N<4> NO_TEST=TRUE
84 13 IN PEG_D2R_P<4> NO_TEST=TRUE
84 13 IN PEG_D2R_N<5> NO_TEST=TRUE
84 13 IN PEG_D2R_P<5> NO_TEST=TRUE
84 13 IN PEG_D2R_N<6> NO_TEST=TRUE
84 13 IN PEG_D2R_P<6> NO_TEST=TRUE
84 13 IN PEG_D2R_N<7> NO_TEST=TRUE
84 13 IN PEG_D2R_P<7> NO_TEST=TRUE
84 13 IN PEG_D2R_N<8> NO_TEST=TRUE
84 13 IN PEG_D2R_P<8> NO_TEST=TRUE
84 13 IN PEG_D2R_N<9> NO_TEST=TRUE
84 13 IN PEG_D2R_P<9> NO_TEST=TRUE
84 13 IN PEG_D2R_N<10> NO_TEST=TRUE
84 13 IN PEG_D2R_P<10> NO_TEST=TRUE
84 13 IN PEG_D2R_N<11> NO_TEST=TRUE
84 13 IN PEG_D2R_P<11> NO_TEST=TRUE
84 13 IN PEG_D2R_N<12> NO_TEST=TRUE
84 13 IN PEG_D2R_P<12> NO_TEST=TRUE
84 13 IN PEG_D2R_N<13> NO_TEST=TRUE
84 13 IN PEG_D2R_P<13> NO_TEST=TRUE
84 13 IN PEG_D2R_N<14> NO_TEST=TRUE
84 13 IN PEG_D2R_P<14> NO_TEST=TRUE
84 13 IN PEG_D2R_N<15> NO_TEST=TRUE
84 13 IN PEG_D2R_P<15> NO_TEST=TRUE

76 75 3 IN PPVCORE_CPU FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
83 78 3 IN PP2V5_S5 FUNC_TEST=TRUE
83 79 3 IN PP1V8_S3 FUNC_TEST=TRUE
79 3 IN PP1V2_S3 FUNC_TEST=TRUE
80 3 IN PP1V5_S0 FUNC_TEST=TRUE
80 34 3 IN PP1V05_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
97 83 75 59 3 IN PP5V_S0 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S5 FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 3 IN PP3V3_S5 FUNC_TEST=TRUE
84 83 76 41 27 26 10 6 3 IN PP3V3_S0 FUNC_TEST=TRUE
83 3 IN PP24V_S0 FUNC_TEST=TRUE

11 7 IN XDP_BPM_L<3> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<2> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<1> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<0> FUNC_TEST=TRUE
26 11 7 IN XDP_DBRESET_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<0> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<1> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<2> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<3> FUNC_TEST=TRUE
67 60 58 21 5 IN LPC_FRAME_L FUNC_TEST=TRUE
67 60 58 23 IN PM_CLKRUN_L FUNC_TEST=TRUE
60 58 22 IN BOOT_LPC_SPI_L FUNC_TEST=TRUE
60 6 IN DEBUG_RST_L FUNC_TEST=TRUE
60 59 21 IN FWH_INIT_L FUNC_TEST=TRUE
60 34 IN PCI_CLK_PORT80 FUNC_TEST=TRUE
67 60 58 23 IN INT_SERIRQ FUNC_TEST=TRUE
67 60 58 23 IN PM_SUS_STAT_L FUNC_TEST=TRUE
60 58 IN SMC_MD1 FUNC_TEST=TRUE
60 59 58 IN SMC_RST_L FUNC_TEST=TRUE
60 58 IN SMC_NMI FUNC_TEST=TRUE
60 23 IN SV_SET_UP FUNC_TEST=TRUE
76 58 IN ISENSE_CAL_EN FUNC_TEST=TRUE
94 85 IN INV_ENABLE_BL FUNC_TEST=TRUE
94 IN LCD_PWM FUNC_TEST=TRUE
75 8 IN CPU_VID<0> FUNC_TEST=TRUE
75 8 IN CPU_VID<1> FUNC_TEST=TRUE
75 8 IN CPU_VID<2> FUNC_TEST=TRUE
75 8 IN CPU_VID<3> FUNC_TEST=TRUE
75 8 IN CPU_VID<4> FUNC_TEST=TRUE
75 8 IN CPU_VID<5> FUNC_TEST=TRUE
75 8 IN CPU_VID<6> FUNC_TEST=TRUE
75 23 14 IN PM_DPRSLPVR FUNC_TEST=TRUE
75 21 7 IN CPU_DPRSTP_L FUNC_TEST=TRUE
75 26 14 5 IN VR_PWRGOOD_DELAY FUNC_TEST=TRUE
26 23 IN VR_PWRGD_CK410 FUNC_TEST=TRUE
84 77 58 26 IN ALL_SYS_PWRGD FUNC_TEST=TRUE
77 58 23 IN PM_SLP_S4_L FUNC_TEST=TRUE
80 79 77 58 23 IN PM_SLP_S3_L FUNC_TEST=TRUE

60 59 58 IN SMC_TCK FUNC_TEST=TRUE
60 59 58 IN SMC_TDI FUNC_TEST=TRUE
60 59 58 IN SMC_TDO FUNC_TEST=TRUE
60 59 58 IN SMC_TMS FUNC_TEST=TRUE
60 58 IN SMC_TRST_L FUNC_TEST=TRUE
60 59 58 IN SMC_TX_L FUNC_TEST=TRUE
60 59 58 IN SMC_RX_L FUNC_TEST=TRUE
59 IN SMC_MANUAL_RST_L FUNC_TEST=TRUE
11 7 IN XDP_TCK FUNC_TEST=TRUE
11 7 IN XDP_TDI FUNC_TEST=TRUE
11 7 IN XDP_TDO FUNC_TEST=TRUE
11 7 IN XDP_TMS FUNC_TEST=TRUE
11 7 IN XDP_TRST_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXP FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXN FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_N FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_P FUNC_TEST=TRUE
11 IN ITPRESET_L FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<5> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<4> FUNC_TEST=TRUE

## MISC GROUND VIAS

ZH500 HOLE-VIA 1
ZH510 HOLE-VIA 1
ZH520 HOLE-VIA 1
ZH501 HOLE-VIA 1
ZH511 HOLE-VIA 1
ZH521 HOLE-VIA 1
ZH502 HOLE-VIA 1
ZH512 HOLE-VIA 1
ZH522 HOLE-VIA 1
ZH503 HOLE-VIA 1
ZH513 HOLE-VIA 1
ZH523 HOLE-VIA 1
ZH504 HOLE-VIA 1
ZH514 HOLE-VIA 1
ZH524 HOLE-VIA 1
ZH505 HOLE-VIA 1
ZH515 HOLE-VIA 1
ZH525 HOLE-VIA 1
ZH506 HOLE-VIA 1
ZH516 HOLE-VIA 1
ZH526 HOLE-VIA 1
ZH507 HOLE-VIA 1
ZH517 HOLE-VIA 1
ZH527 HOLE-VIA 1
ZH508 HOLE-VIA 1
ZH518 HOLE-VIA 1
ZH528 HOLE-VIA 1
ZH509 HOLE-VIA 1
ZH519 HOLE-VIA 1
ZH529 HOLE-VIA 1

# FUNC TEST 1 OF 2

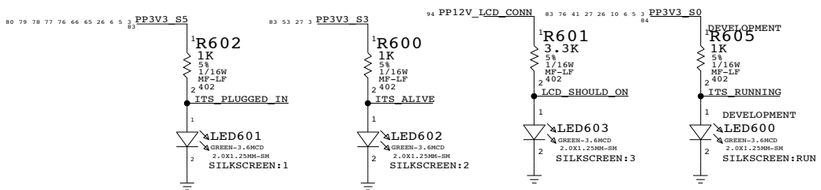
SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

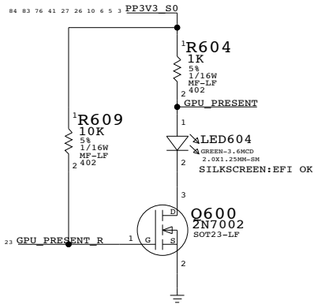


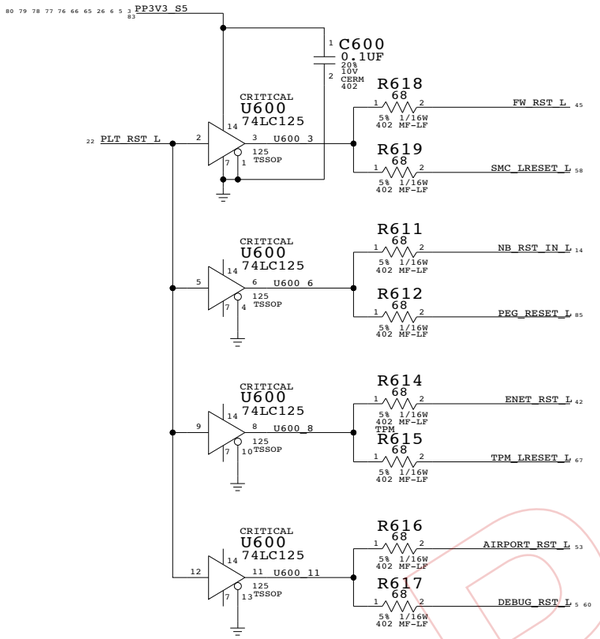
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 5 OF 97 | |

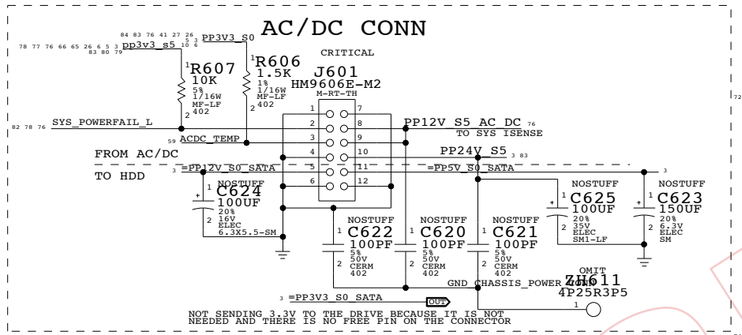
## SYSTEM STATUS



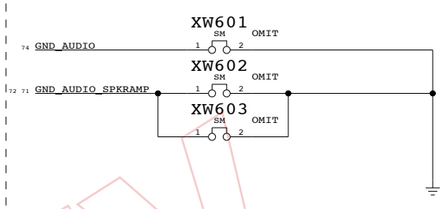



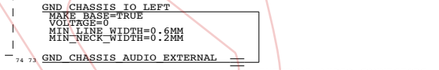

## AC/DC CONN

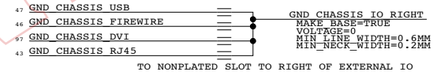


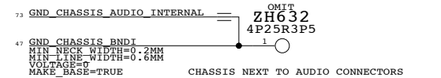

## GND RAILS

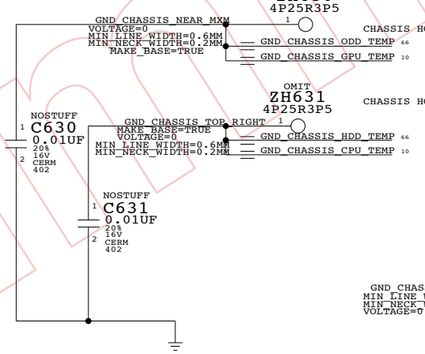


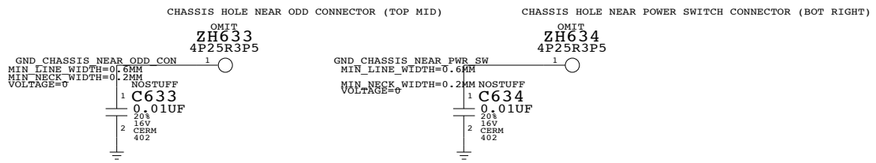

## CHASSIS GND



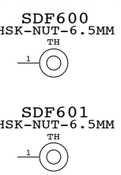




## HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU




## POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006



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|---|---|---|
| D | 051-7039 | 21 |
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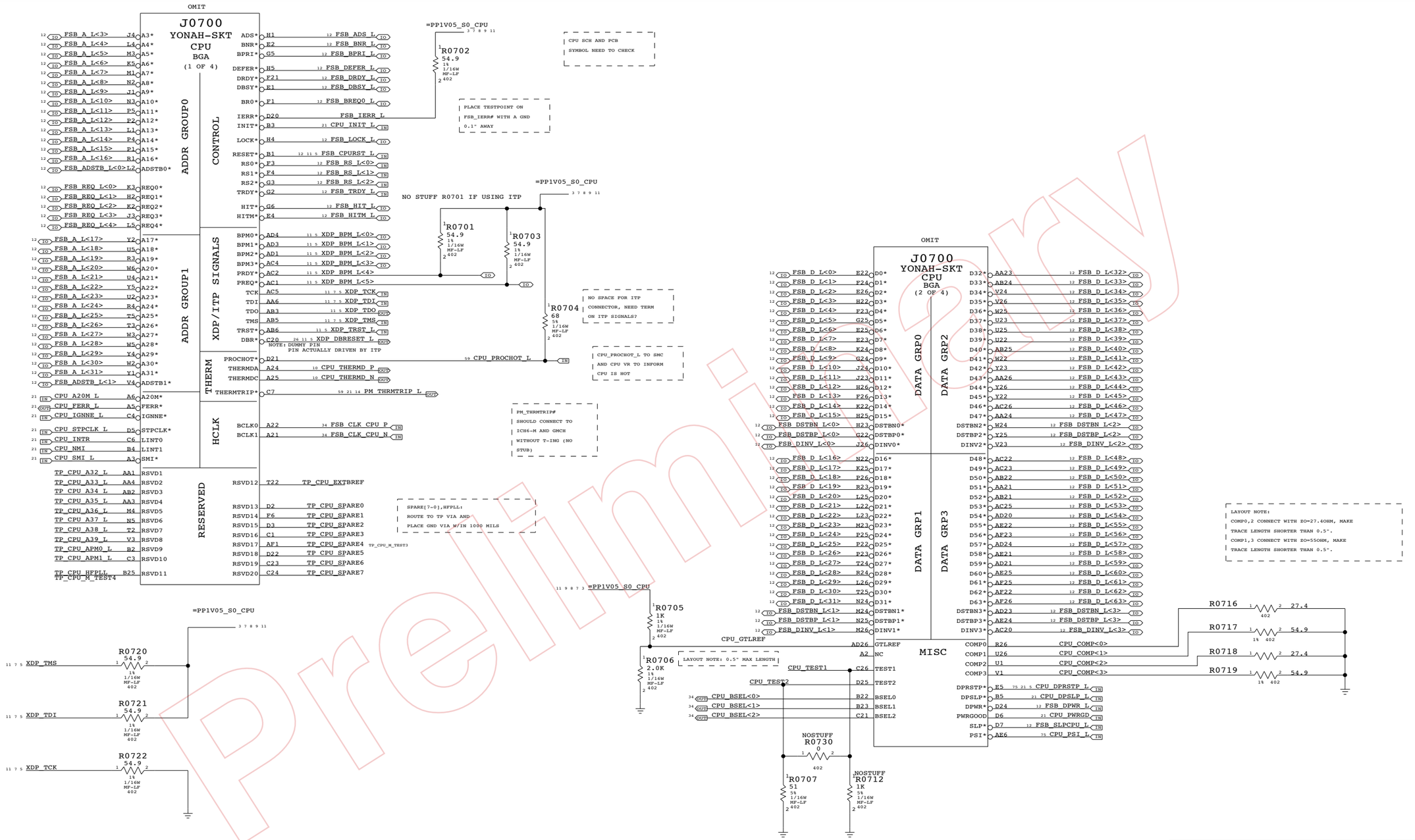




CPU 1 OF 2-FSB

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 7 OF 97 | |

=PPVCORE_S0_CPU 3 8 9 76

OMIT

J0700 YONAH-SKT CPU BGA (3 OF 4)

| | | | |
|---|---|---|---|
| A7 | VCC_1 | VCC_68 | AB20 |
| A9 | VCC_2 | VCC_69 | AB7 |
| A10 | VCC_3 | VCC_70 | AC7 |
| A12 | VCC_4 | VCC_71 | AC9 |
| A13 | VCC_5 | VCC_72 | AC12 |
| A15 | VCC_6 | VCC_73 | AC13 |
| A17 | VCC_7 | VCC_74 | AC15 |
| A18 | VCC_8 | VCC_75 | AC17 |
| A20 | VCC_9 | VCC_76 | AC18 |
| B7 | VCC_10 | VCC_77 | AD7 |
| B9 | VCC_11 | VCC_78 | AD9 |
| B10 | VCC_12 | VCC_79 | AD10 |
| B12 | VCC_13 | VCC_80 | AD12 |
| B14 | VCC_14 | VCC_81 | AD14 |
| B15 | VCC_15 | VCC_82 | AD15 |
| B17 | VCC_16 | VCC_83 | AD17 |
| B18 | VCC_17 | VCC_84 | AD18 |
| B20 | VCC_18 | VCC_85 | AE9 |
| C9 | VCC_19 | VCC_86 | AE10 |
| C10 | VCC_20 | VCC_87 | AE12 |
| C12 | VCC_21 | VCC_88 | AE13 |
| C13 | VCC_22 | VCC_89 | AE15 |
| C15 | VCC_23 | VCC_90 | AE17 |
| C17 | VCC_24 | VCC_91 | AE18 |
| C18 | VCC_25 | VCC_92 | AE20 |
| D9 | VCC_26 | VCC_93 | AF9 |
| D10 | VCC_27 | VCC_94 | AF10 |
| D12 | VCC_28 | VCC_95 | AF12 |
| D14 | VCC_29 | VCC_96 | AF14 |
| D15 | VCC_30 | VCC_97 | AF15 |
| D17 | VCC_31 | VCC_98 | AF17 |
| D18 | VCC_32 | VCC_99 | AF18 |
| E7 | VCC_33 | VCC_100 | AF20 |
| E9 | VCC_34 | | |
| E10 | VCC_35 | VCCP_1 | V6 |
| E12 | VCC_36 | VCCP_2 | G21 |
| E13 | VCC_37 | VCCP_3 | J6 |
| E15 | VCC_38 | VCCP_4 | K6 |
| E17 | VCC_39 | VCCP_5 | M6 |
| E18 | VCC_40 | VCCP_6 | J21 |
| E20 | VCC_41 | VCCP_7 | K21 |
| F7 | VCC_42 | VCCP_8 | M21 |
| F9 | VCC_43 | VCCP_9 | N21 |
| F10 | VCC_44 | VCCP_10 | N6 |
| F12 | VCC_45 | VCCP_11 | R21 |
| F14 | VCC_46 | VCCP_12 | R6 |
| F15 | VCC_47 | VCCP_13 | T21 |
| F17 | VCC_48 | VCCP_14 | T6 |
| F18 | VCC_49 | VCCP_15 | V21 |
| F20 | VCC_50 | VCCP_16 | W21 |
| AA7 | VCC_51 | | |
| AA9 | VCC_52 | | |
| AA10 | VCC_53 | | |
| AA12 | VCC_54 | | |
| AA13 | VCC_55 | | |
| AA15 | VCC_56 | | |
| AA17 | VCC_57 | | |
| AA18 | VCC_58 | | |
| AA20 | VCC_59 | | |
| AB9 | VCC_60 | | |
| AC10 | VCC_61 | | |
| AB10 | VCC_62 | | |
| AB12 | VCC_63 | | |
| AB14 | VCC_64 | | |
| AB15 | VCC_65 | | |
| AB17 | VCC_66 | | |
| AB18 | VCC_67 | | |

=PPVCORE_S0_CPU 3 8 9 76

=PP1V05_S0_CPU 3 7 9 11

=PP1V5_S0_CPU 3 8

VCCA=1.5 ONLY

| | | |
|---|---|---|
| VCCA | B26 | |
| VID0 | AD6 | 75 5 CPU_VID<0> OUT |
| VID1 | AF5 | 75 5 CPU_VID<1> OUT |
| VID2 | AE5 | 75 5 CPU_VID<2> OUT |
| VID3 | AF4 | 75 5 CPU_VID<3> OUT |
| VID4 | AE3 | 75 5 CPU_VID<4> OUT |
| VID5 | AF2 | 75 5 CPU_VID<5> OUT |
| VID6 | AE2 | 75 5 CPU_VID<6> OUT |
| VCCSENSE | AF7 | 75 CPU_VCCSENSE_P OUT |
| VSSSENSE | AE7 | 75 CPU_VCCSENSE_N OUT |

=PP1V5_S0_CPU 3 8

C0800 1 0.01UF 20% 16V CERM 402 2

C0801 1 10UF 20% 6.3V CERM 805-1 2

=PPVCORE_S0_CPU 3 8 9 76

R0802 1 100 1% 1/16W MF-LF 402 2

R0803 1 100 1% 1/16W MF-LF 402 2

LAYOUT NOTE: CONNECT R0802-03 TO VCCSENSE_P/N WITH NO STUB

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB) TO CONNECT A DIFFERENCTIAL PROBE BETWEEN VCCSENSE AND VSSSENSE AT THE LOCATION WHERE THE TWO 54.9 OHM RESISTORS TERMINATE THE 55 OHM TRANSMISSION LINE

OMIT

J0700 YONAH-SKT CPU BGA (4 OF 4)

| | | | |
|---|---|---|---|
| A4 | VSS_1 | VSS_82 | P6 |
| A8 | VSS_2 | VSS_83 | P21 |
| A11 | VSS_3 | VSS_84 | P24 |
| A14 | VSS_4 | VSS_85 | R2 |
| A16 | VSS_5 | VSS_86 | R5 |
| A19 | VSS_6 | VSS_87 | R22 |
| A23 | VSS_7 | VSS_88 | R25 |
| A26 | VSS_8 | VSS_89 | T1 |
| B6 | VSS_9 | VSS_90 | T4 |
| B8 | VSS_10 | VSS_91 | T23 |
| B11 | VSS_11 | VSS_92 | T26 |
| B13 | VSS_12 | VSS_93 | U3 |
| B16 | VSS_13 | VSS_94 | U6 |
| B19 | VSS_14 | VSS_95 | U21 |
| B21 | VSS_15 | VSS_96 | U24 |
| B24 | VSS_16 | VSS_97 | V2 |
| C5 | VSS_17 | VSS_98 | V5 |
| C8 | VSS_18 | VSS_99 | V22 |
| C11 | VSS_19 | VSS_100 | V25 |
| C14 | VSS_20 | VSS_101 | W1 |
| C16 | VSS_21 | VSS_102 | W4 |
| C19 | VSS_22 | VSS_103 | W23 |
| C2 | VSS_23 | VSS_104 | W26 |
| C22 | VSS_24 | VSS_105 | Y3 |
| C25 | VSS_25 | VSS_106 | Y6 |
| D1 | VSS_26 | VSS_107 | Y21 |
| D4 | VSS_27 | VSS_108 | Y24 |
| D8 | VSS_28 | VSS_109 | AA2 |
| D11 | VSS_29 | VSS_110 | AA5 |
| D13 | VSS_30 | VSS_111 | AA8 |
| D16 | VSS_31 | VSS_112 | AA11 |
| D19 | VSS_32 | VSS_113 | AA14 |
| D23 | VSS_33 | VSS_114 | AA16 |
| D26 | VSS_34 | VSS_115 | AA19 |
| E3 | VSS_35 | VSS_116 | AA22 |
| E6 | VSS_36 | VSS_117 | AA25 |
| E8 | VSS_37 | VSS_118 | AB1 |
| E11 | VSS_38 | VSS_119 | AB4 |
| E14 | VSS_39 | VSS_120 | AB8 |
| E16 | VSS_40 | VSS_121 | AB11 |
| E19 | VSS_41 | VSS_122 | AB13 |
| E21 | VSS_42 | VSS_123 | AB16 |
| E24 | VSS_43 | VSS_124 | AB19 |
| F5 | VSS_44 | VSS_125 | AB23 |
| F8 | VSS_45 | VSS_126 | AB26 |
| F11 | VSS_46 | VSS_127 | AC3 |
| F13 | VSS_47 | VSS_128 | AC6 |
| F16 | VSS_48 | VSS_129 | AC8 |
| F19 | VSS_49 | VSS_130 | AC11 |
| F2 | VSS_50 | VSS_131 | AC14 |
| F22 | VSS_51 | VSS_132 | AC16 |
| F25 | VSS_52 | VSS_133 | AC19 |
| G4 | VSS_53 | VSS_134 | AC21 |
| G1 | VSS_54 | VSS_135 | AC24 |
| G23 | VSS_55 | VSS_136 | AD2 |
| G26 | VSS_56 | VSS_137 | AD5 |
| H3 | VSS_57 | VSS_138 | AD8 |
| H6 | VSS_58 | VSS_139 | AD11 |
| H21 | VSS_59 | VSS_140 | AD13 |
| H24 | VSS_60 | VSS_141 | AD16 |
| J2 | VSS_61 | VSS_142 | AD19 |
| J5 | VSS_62 | VSS_143 | AD22 |
| J22 | VSS_63 | VSS_144 | AD25 |
| J25 | VSS_64 | VSS_145 | AE1 |
| K1 | VSS_65 | VSS_146 | AE4 |
| K4 | VSS_66 | VSS_147 | AE8 |
| K23 | VSS_67 | VSS_148 | AE11 |
| K26 | VSS_68 | VSS_149 | AE14 |
| L3 | VSS_69 | VSS_150 | AE16 |
| L6 | VSS_70 | VSS_151 | AE19 |
| L21 | VSS_71 | VSS_152 | AE23 |
| L24 | VSS_72 | VSS_153 | AE26 |
| M2 | VSS_73 | VSS_154 | AF3 |
| M5 | VSS_74 | VSS_155 | AF6 |
| M22 | VSS_75 | VSS_156 | AF8 |
| M25 | VSS_76 | VSS_157 | AF11 |
| N1 | VSS_77 | VSS_158 | AF13 |
| N4 | VSS_78 | VSS_159 | AF16 |
| N23 | VSS_79 | VSS_160 | AF19 |
| N26 | VSS_80 | VSS_161 | AF21 |
| P3 | VSS_81 | VSS_162 | AF24 |

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



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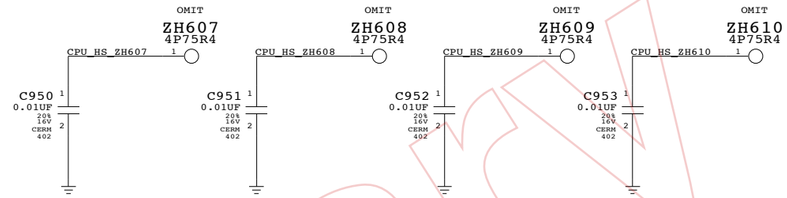
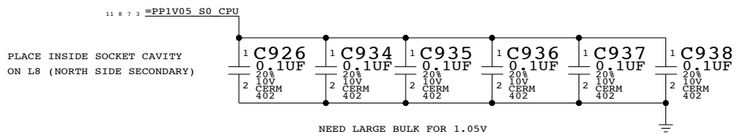
## CPU HEATSINK MOUNTING HOLES

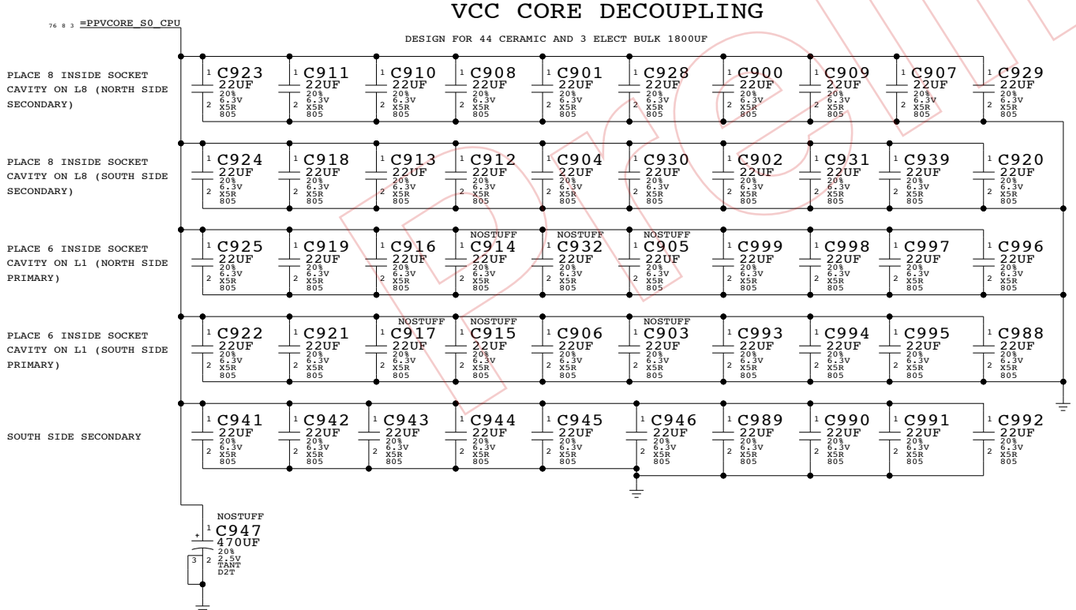



WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

## VCCP CORE DECOUPLING




## VCC CORE DECOUPLING




CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
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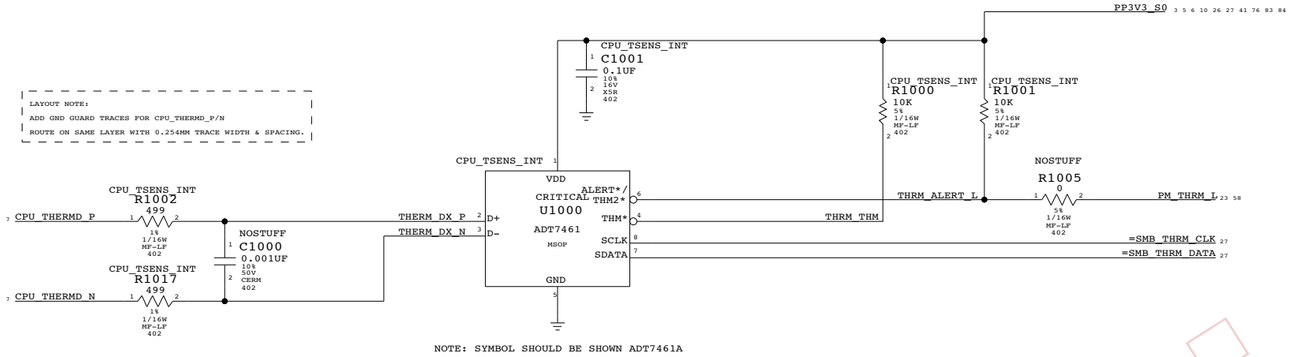
## CPU INTERNAL DIODE THERMAL SENSOR

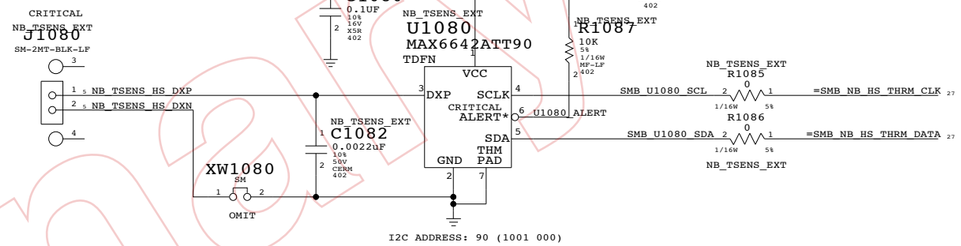
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



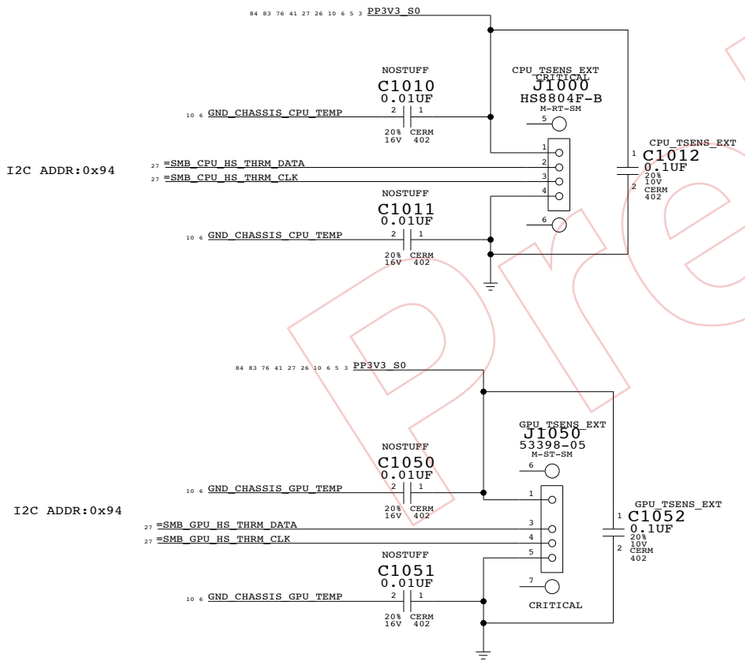

NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

## NB HEATSINK TEMPERATURE SENSE




I2C ADDRESS: 90 (1001 000)

## CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

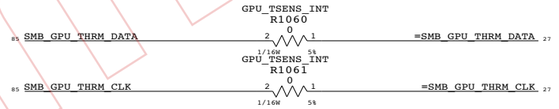



I2C ADDR:0x94



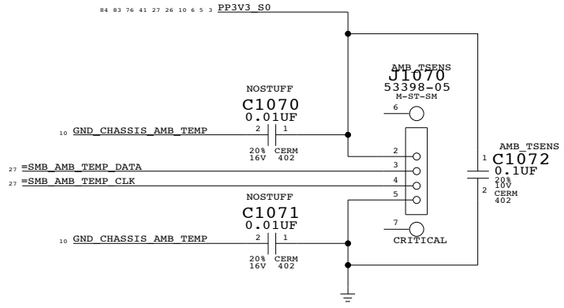

I2C ADDR:0x94

## MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)




NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

## AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR




I2C ADDR:0x96

## ASIC TEMP SENSORS

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)



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| D | 051-7039 | 21 |
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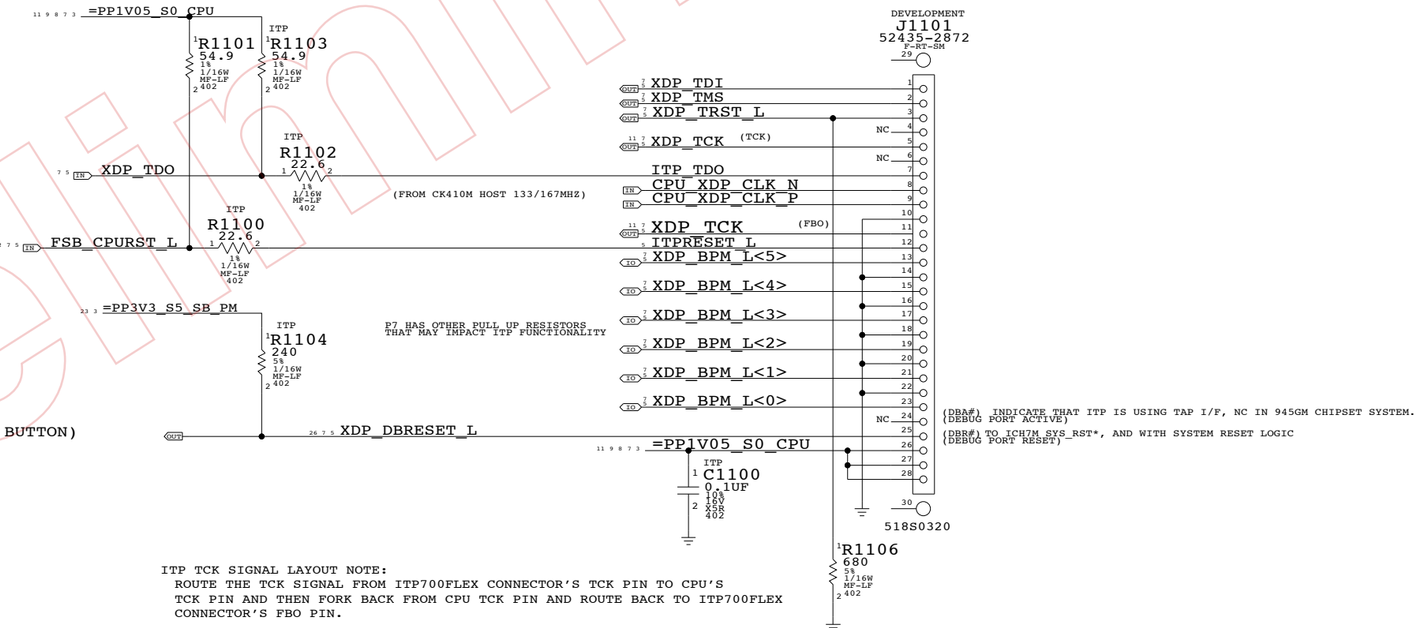
# CPU ITP700FLEX DEBUG SUPPORT




(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM. (DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

## CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



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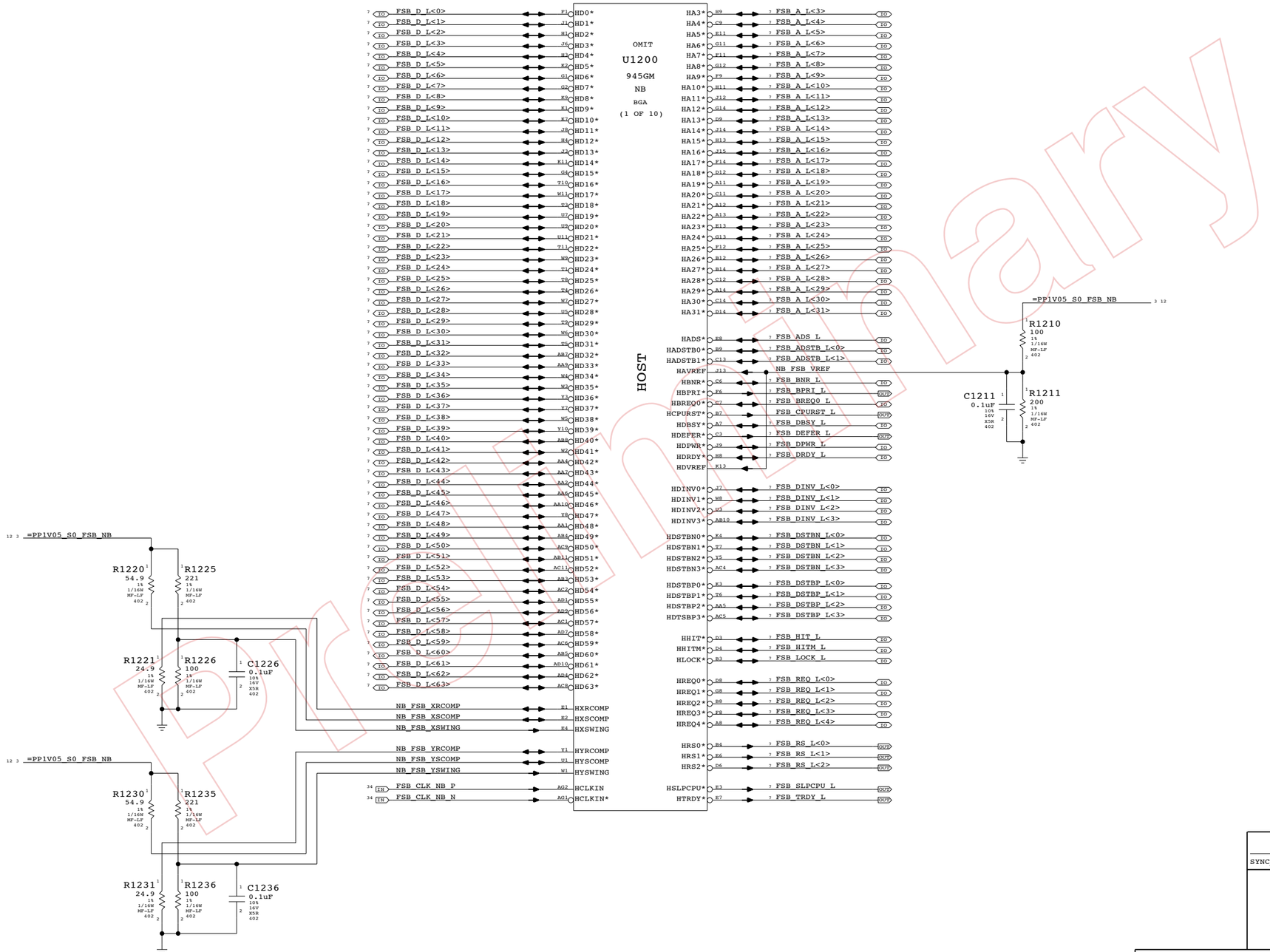
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 11 OF 97 | |




## NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 12 OF 97

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

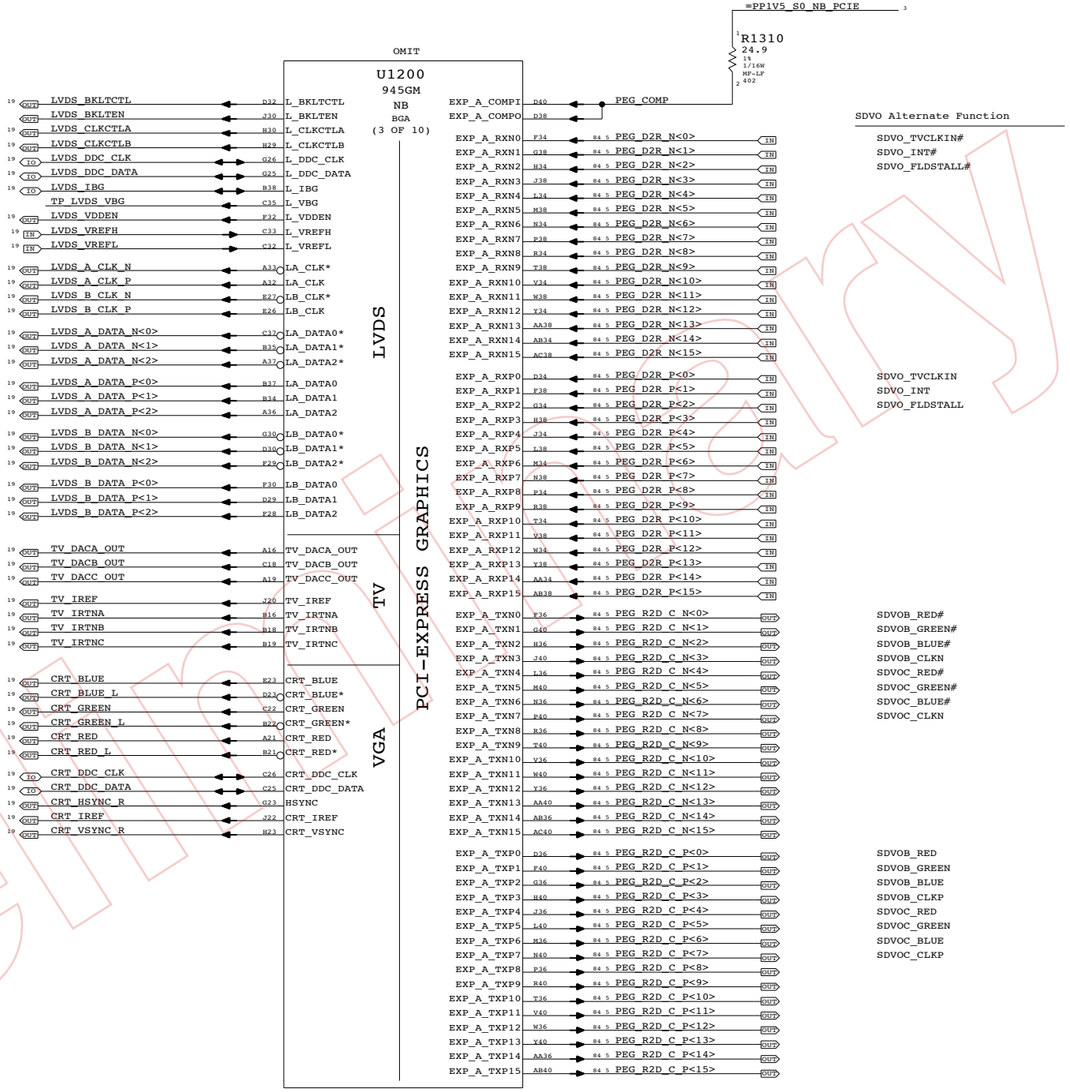
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



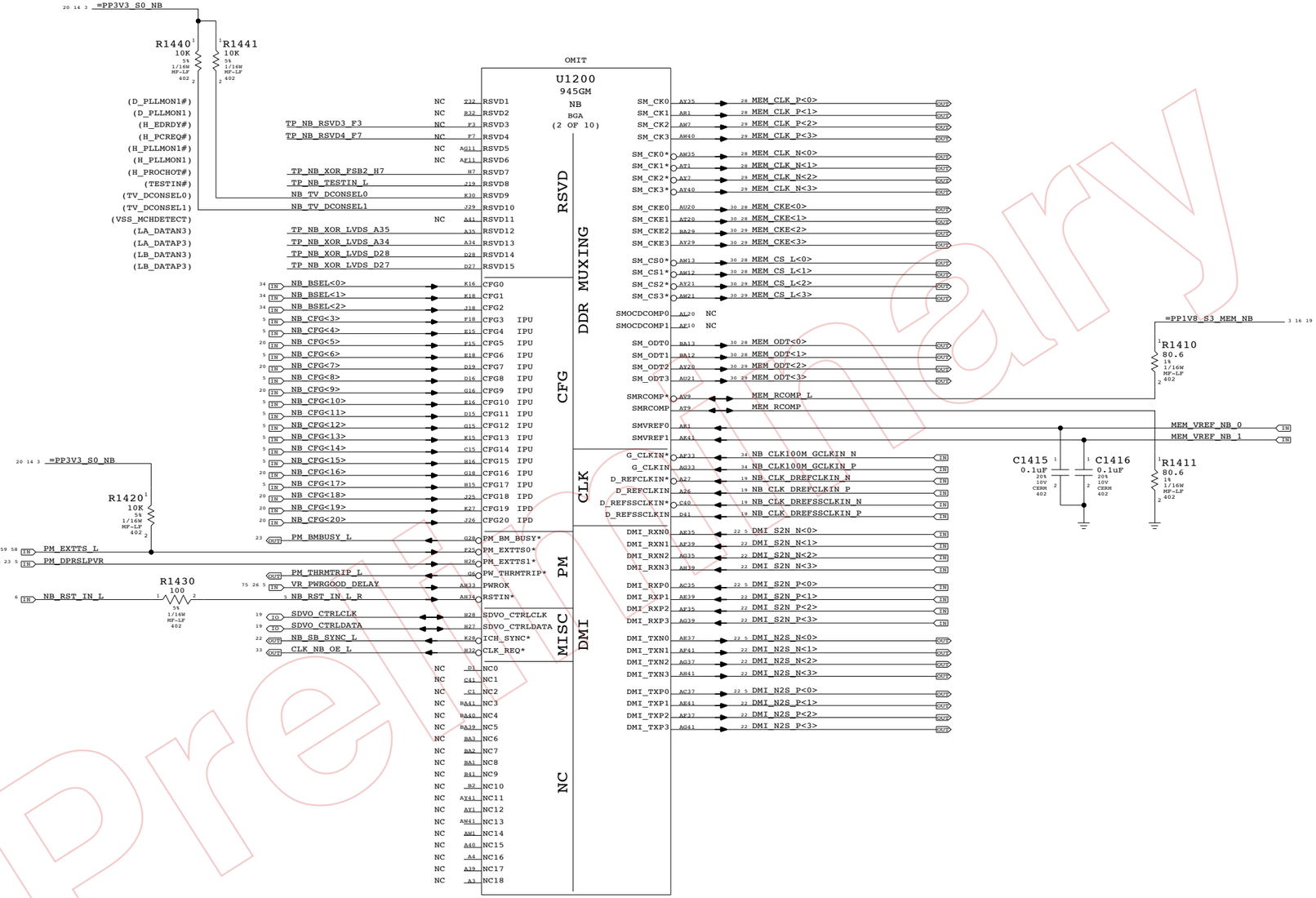

NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 13 OF 97 | |






## NB Misc Interfaces

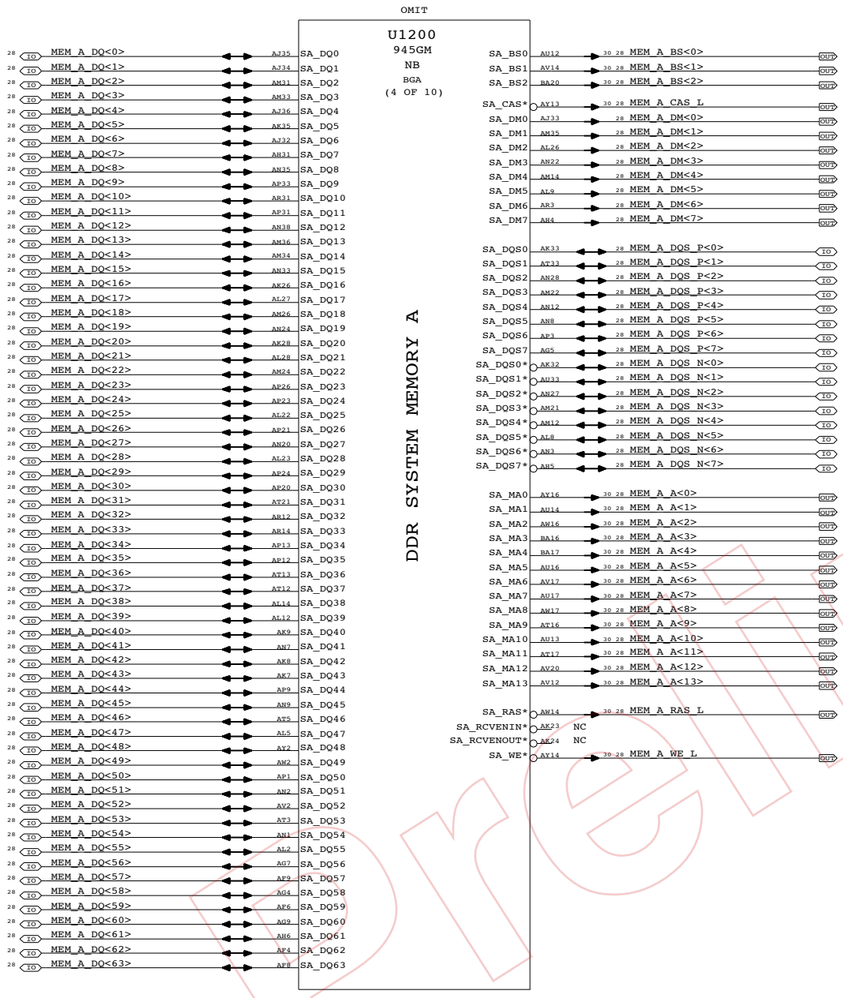
SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

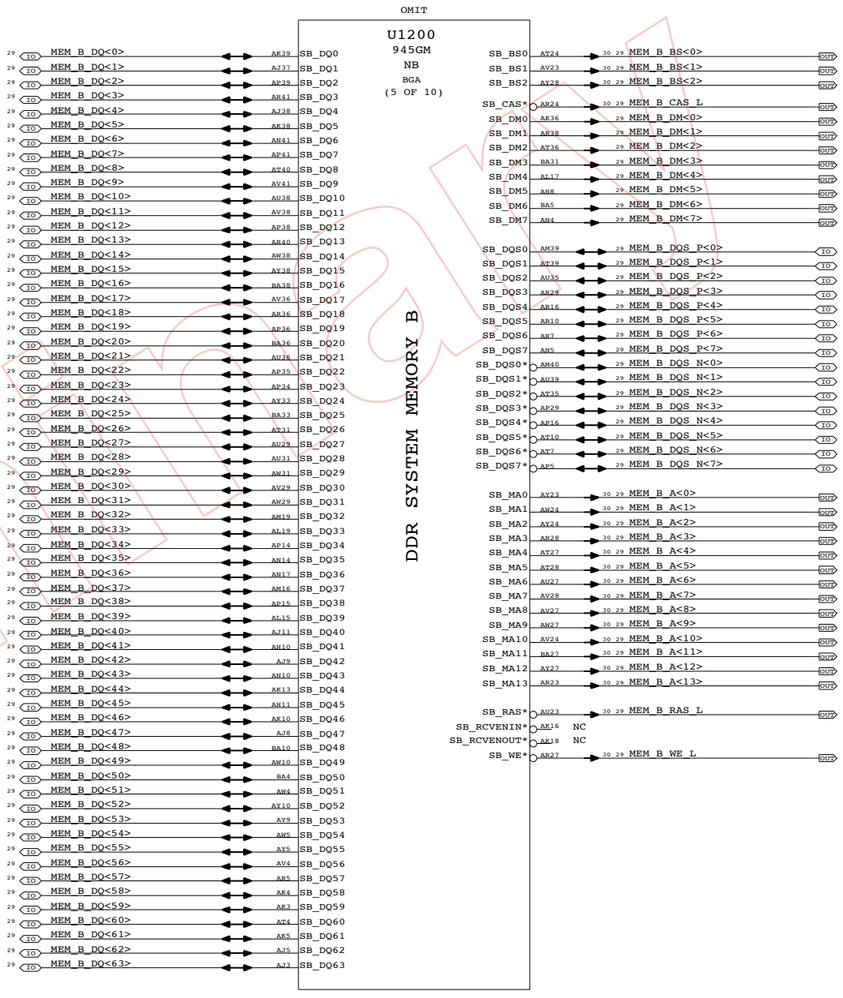


APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 14 OF 97




NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 15 OF 97

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT

=PPVCORE_S0_NB 3 16 19

1.05V or 1.5V

U1200
945GM
NB
BGA
(6 OF 10)

VCC

OMIT

VCC_0 AA33
VCC_1 R33
VCC_2 P33
VCC_3 L33
VCC_4 J33
VCC_5 J32
VCC_6 AA32
VCC_7 Y32
VCC_8 W32
VCC_9 V32
VCC_10 U32
VCC_11 R32
VCC_12 N32
VCC_13 L32
VCC_14 J32
VCC_15 AA31
VCC_16 W31
VCC_17 V31
VCC_18 T31
VCC_19 R31
VCC_20 P31
VCC_21 N31
VCC_22 L31
VCC_23 AA30
VCC_24 Y30
VCC_25 W30
VCC_26 V30
VCC_27 U30
VCC_28 T30
VCC_29 R30
VCC_30 P30
VCC_31 N30
VCC_32 L30
VCC_33 AA29
VCC_34 Y29
VCC_35 W29
VCC_36 V29
VCC_37 U29
VCC_38 T29
VCC_39 R29
VCC_40 P29
VCC_41 N29
VCC_42 L29
VCC_43 AA28
VCC_44 Y28
VCC_45 W28
VCC_46 V28
VCC_47 U28
VCC_48 T28
VCC_49 R28
VCC_50 P28
VCC_51 N28
VCC_52 L28
VCC_53 P27
VCC_54 N27
VCC_55 M27
VCC_56 L27
VCC_57 P26
VCC_58 N26
VCC_59 M26
VCC_60 L26
VCC_61 M25
VCC_62 L25
VCC_63 P24
VCC_64 N24
VCC_65 M24
VCC_66 L24
VCC_67 AA23
VCC_68 Y23
VCC_69 W23
VCC_70 V23
VCC_71 N23
VCC_72 M23
VCC_73 L23
VCC_74 AC22
VCC_75 AA22
VCC_76 Y22
VCC_77 W22
VCC_78 V22
VCC_79 N22
VCC_80 M22
VCC_81 L22
VCC_82 AC21
VCC_83 AA21
VCC_84 Y21
VCC_85 W21
VCC_86 L21
VCC_87 AC20
VCC_88 AA20
VCC_89 Y20
VCC_90 W20
VCC_91 V20
VCC_92 P20
VCC_93 N20
VCC_94 L20
VCC_95 AB19
VCC_96 AA19
VCC_97 Y19
VCC_98 W19
VCC_99 V19
VCC_100 U19
VCC_101 L19
VCC_102 R18
VCC_103 N18
VCC_104 L18
VCC_105 P17
VCC_106 N17
VCC_107 M17
VCC_108 N16
VCC_109 M16
VCC_110 L16

VCC_SM0 AU41
VCC_SM1 AT41
VCC_SM2 AM41
VCC_SM3 AU40
VCC_SM4 BA34
VCC_SM5 AT34
VCC_SM6 AM34
VCC_SM7 AV34
VCC_SM8 AU34
VCC_SM9 AT34
VCC_SM10 AM34
VCC_SM11 BA30
VCC_SM12 AV30
VCC_SM13 AM30
VCC_SM14 AV30
VCC_SM15 AU30
VCC_SM16 AT30
VCC_SM17 AM30
VCC_SM18 AP30
VCC_SM19 AN30
VCC_SM20 AM30
VCC_SM21 AM29
VCC_SM22 AL29
VCC_SM23 AK29
VCC_SM24 AJ29
VCC_SM25 AM29
VCC_SM26 AJ28
VCC_SM27 AM28
VCC_SM28 AJ27
VCC_SM29 AM27
VCC_SM30 AJ26
VCC_SM31 BA26
VCC_SM32 AV26
VCC_SM33 AM26
VCC_SM34 AU26
VCC_SM35 AT26
VCC_SM36 AM26
VCC_SM37 AJ26
VCC_SM38 AM26
VCC_SM39 AJ25
VCC_SM40 AM25
VCC_SM41 AJ24
VCC_SM42 AM24
VCC_SM43 AJ23
VCC_SM44 BA23
VCC_SM45 AV22
VCC_SM46 AM22
VCC_SM47 AM22
VCC_SM48 AV22
VCC_SM49 AU22
VCC_SM50 AT22
VCC_SM51 AM22
VCC_SM52 AK22
VCC_SM53 AJ22
VCC_SM54 AJ22
VCC_SM55 AM21
VCC_SM56 AK20
VCC_SM57 BA19
VCC_SM58 AV19
VCC_SM59 AM19
VCC_SM60 AU19
VCC_SM61 AT19
VCC_SM62 AM19
VCC_SM63 AK19
VCC_SM64 AJ19
VCC_SM65 AM19
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VCC_SM67 AJ18
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VCC_SM71 BA15
VCC_SM72 AV15
VCC_SM73 AM15
VCC_SM74 AM15
VCC_SM75 AU15
VCC_SM76 AT15
VCC_SM77 AM15
VCC_SM78 BA15
VCC_SM79 AJ15
VCC_SM80 AJ14
VCC_SM81 AJ13
VCC_SM82 AM13
VCC_SM83 AK12
VCC_SM84 AJ12
VCC_SM85 AM12
VCC_SM86 AG12
VCC_SM87 AK11
VCC_SM88 BA8
VCC_SM89 AV8
VCC_SM90 AM8
VCC_SM91 AU8
VCC_SM92 AT8
VCC_SM93 AM8
VCC_SM94 AK8
VCC_SM95 AJ8
VCC_SM96 AK6
VCC_SM97 AJ6
VCC_SM98 AM6
VCC_SM99 AK6
VCC_SM100 AM6
VCC_SM101 AK6
VCC_SM102 AM6
VCC_SM103 AK6
VCC_SM104 AM6
VCC_SM105 AV1
VCC_SM106 AM1
VCC_SM107 AJ1

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 1 2 0.47UF 10% 6.3V CERM-X5R 402
C1613 1 2 0.47UF 10% 6.3V CERM-X5R 402

C1615 1 2 0.47UF 10% 6.3V CERM-X5R 402
19 14 3 =PP1V8_S3_MEM_NB
Layout Note:
Place near pin BA23

C1620 1 2 10UF 20% 6.3V CERM 805-1
C1621 1 2 10UF 20% 6.3V CERM 805-1
Layout Note:
Place in cavity
(Need to better define cavity)

C1610 1 2 0.47UF 10% 6.3V CERM-X5R 402
Layout Note:
Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 1 2 0.47UF 10% 6.3V CERM-X5R 402
C1611 1 2 0.47UF 10% 6.3V CERM-X5R 402

19 16 3 =PPVCORE_S0_NB

U1200
945GM
NB
BGA
(7 OF 10)

NCTF

VCC_NCTF0 AD27
VCC_NCTF1 AC27
VCC_NCTF2 AB27
VCC_NCTF3 AA27
VCC_NCTF4 Y27
VCC_NCTF5 W27
VCC_NCTF6 V27
VCC_NCTF7 U27
VCC_NCTF8 T27
VCC_NCTF9 R27
VCC_NCTF10 AD26
VCC_NCTF11 AC26
VCC_NCTF12 AB26
VCC_NCTF13 AA26
VCC_NCTF14 Y26
VCC_NCTF15 W26
VCC_NCTF16 V26
VCC_NCTF17 U26
VCC_NCTF18 T26
VCC_NCTF19 R26
VCC_NCTF20 AD25
VCC_NCTF21 AC25
VCC_NCTF22 AB25
VCC_NCTF23 AA25
VCC_NCTF24 Y25
VCC_NCTF25 W25
VCC_NCTF26 V25
VCC_NCTF27 U25
VCC_NCTF28 T25
VCC_NCTF29 R25
VCC_NCTF30 AD24
VCC_NCTF31 AC24
VCC_NCTF32 AB24
VCC_NCTF33 AA24
VCC_NCTF34 Y24
VCC_NCTF35 W24
VCC_NCTF36 V24
VCC_NCTF37 U24
VCC_NCTF38 T24
VCC_NCTF39 R24
VCC_NCTF40 AD23
VCC_NCTF41 V23
VCC_NCTF42 U23
VCC_NCTF43 T23
VCC_NCTF44 R23
VCC_NCTF45 AD22
VCC_NCTF46 V22
VCC_NCTF47 U22
VCC_NCTF48 T22
VCC_NCTF49 R22
VCC_NCTF50 AD21
VCC_NCTF51 V21
VCC_NCTF52 U21
VCC_NCTF53 T21
VCC_NCTF54 R21
VCC_NCTF55 AD20
VCC_NCTF56 V20
VCC_NCTF57 U20
VCC_NCTF58 T20
VCC_NCTF59 R20
VCC_NCTF60 AD19
VCC_NCTF61 V19
VCC_NCTF62 U19
VCC_NCTF63 T19
VCC_NCTF64 AD18
VCC_NCTF65 AC18
VCC_NCTF66 AB18
VCC_NCTF67 AA18
VCC_NCTF68 Y18
VCC_NCTF69 W18
VCC_NCTF70 V18
VCC_NCTF71 U18
VCC_NCTF72 T18

VSS_NCTF0 AE27
VSS_NCTF1 AE26
VSS_NCTF2 AE25
VSS_NCTF3 AE24
VSS_NCTF4 AE23
VSS_NCTF5 AE22
VSS_NCTF6 AE21
VSS_NCTF7 AE20
VSS_NCTF8 AE19
VSS_NCTF9 AE18
VSS_NCTF10 AC17
VSS_NCTF11 Y17
VSS_NCTF12 U17

=PP1V5_S0_NB_VCCAUX 3 17 19

VCCAUX_NCTF0 AG27
VCCAUX_NCTF1 AF27
VCCAUX_NCTF2 AG26
VCCAUX_NCTF3 AF26
VCCAUX_NCTF4 AG25
VCCAUX_NCTF5 AF25
VCCAUX_NCTF6 AG24
VCCAUX_NCTF7 AF24
VCCAUX_NCTF8 AG23
VCCAUX_NCTF9 AF23
VCCAUX_NCTF10 AG22
VCCAUX_NCTF11 AF22
VCCAUX_NCTF12 AG21
VCCAUX_NCTF13 AF21
VCCAUX_NCTF14 AG20
VCCAUX_NCTF15 AF20
VCCAUX_NCTF16 AG19
VCCAUX_NCTF17 AF19
VCCAUX_NCTF18 R19
VCCAUX_NCTF19 AG18
VCCAUX_NCTF20 AF18
VCCAUX_NCTF21 R18
VCCAUX_NCTF22 AG17
VCCAUX_NCTF23 AF17
VCCAUX_NCTF24 AE17
VCCAUX_NCTF25 AD17
VCCAUX_NCTF26 AB17
VCCAUX_NCTF27 AA17
VCCAUX_NCTF28 W17
VCCAUX_NCTF29 V17
VCCAUX_NCTF30 T17
VCCAUX_NCTF31 R17
VCCAUX_NCTF32 AG16
VCCAUX_NCTF33 AF16
VCCAUX_NCTF34 AE16
VCCAUX_NCTF35 AD16
VCCAUX_NCTF36 AC16
VCCAUX_NCTF37 AB16
VCCAUX_NCTF38 AA16
VCCAUX_NCTF39 Y16
VCCAUX_NCTF40 W16
VCCAUX_NCTF41 V16
VCCAUX_NCTF42 U16
VCCAUX_NCTF43 T16
VCCAUX_NCTF44 R16
VCCAUX_NCTF45 AG15
VCCAUX_NCTF46 AF15
VCCAUX_NCTF47 AE15
VCCAUX_NCTF48 AD15
VCCAUX_NCTF49 AC15
VCCAUX_NCTF50 AB15
VCCAUX_NCTF51 AA15
VCCAUX_NCTF52 Y15
VCCAUX_NCTF53 W15
VCCAUX_NCTF54 V15
VCCAUX_NCTF55 U15
VCCAUX_NCTF56 T15
VCCAUX_NCTF57 R15

NB Power 1

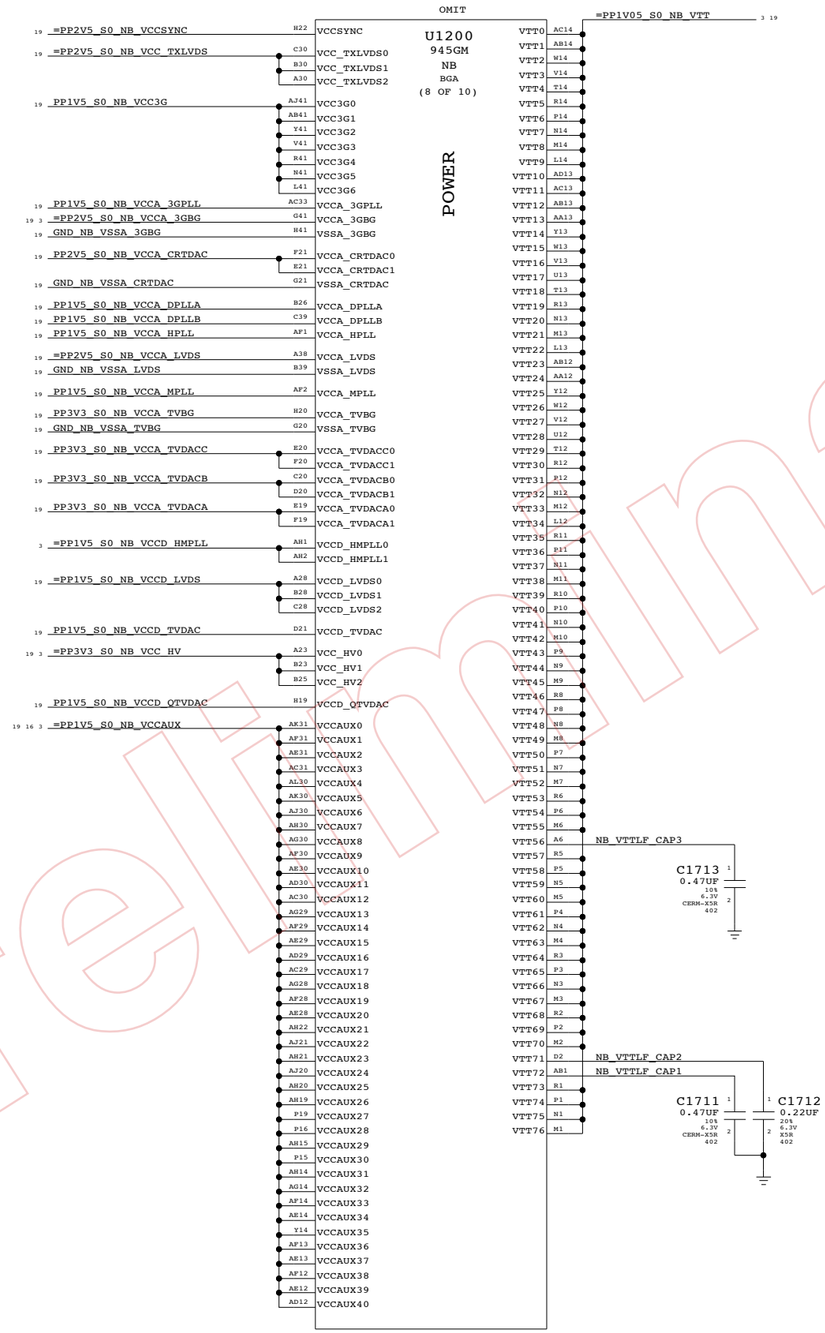
SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7039 | REV. 21

SCALE NONE | SHT 16 OF 97






NB Power 2

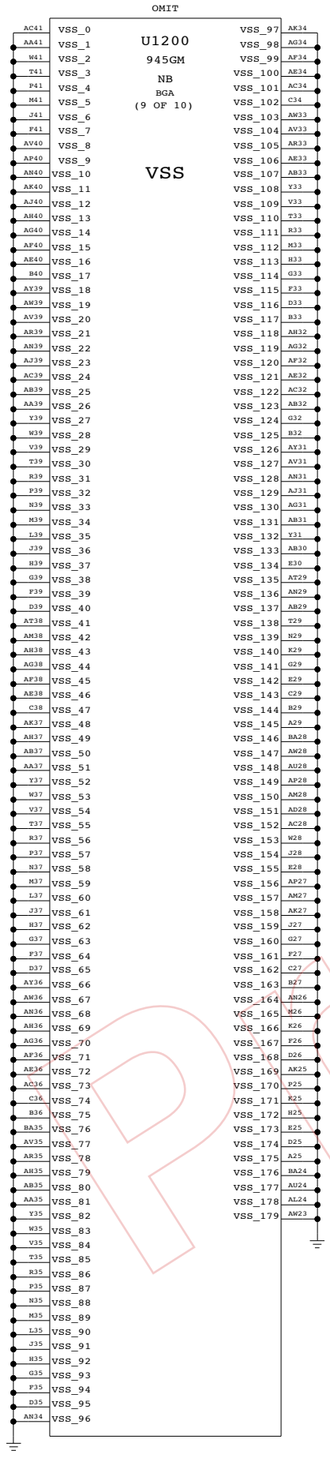
SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

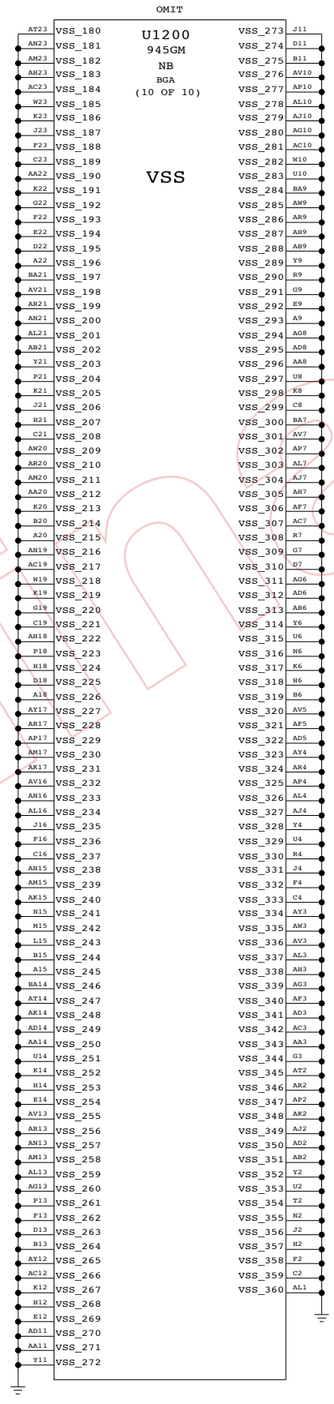


APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 17 OF 97






NB Grounds

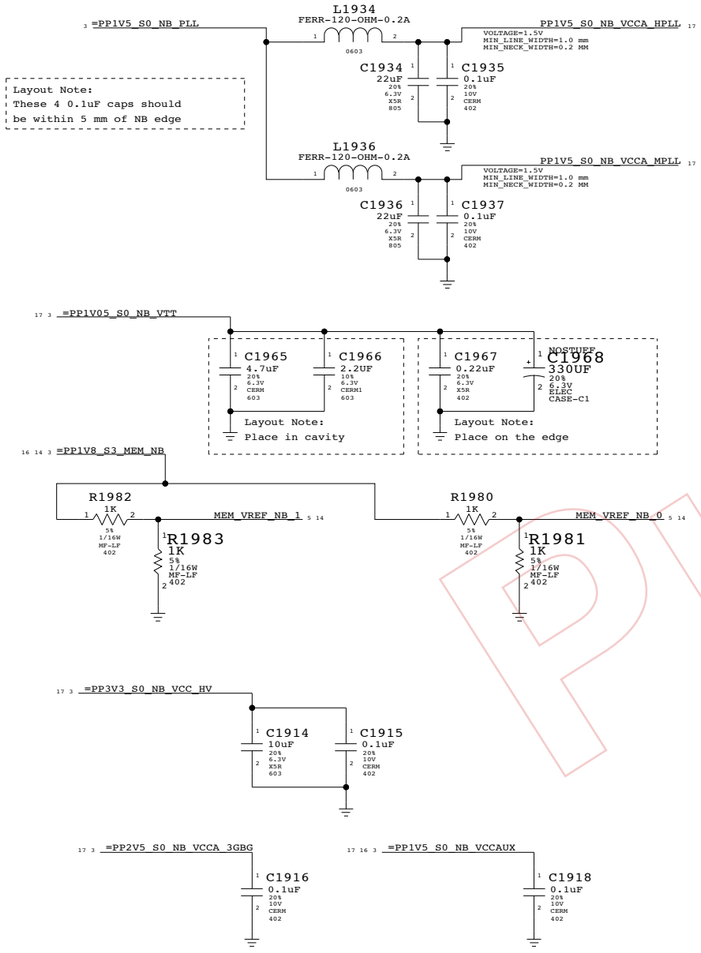
SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



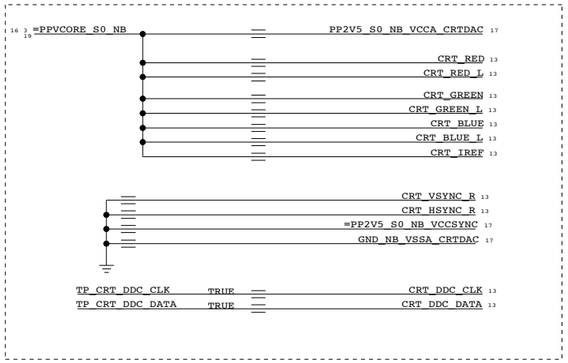
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

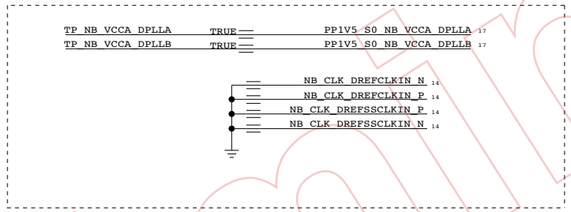
SCALE NONE SHT 18 OF 97



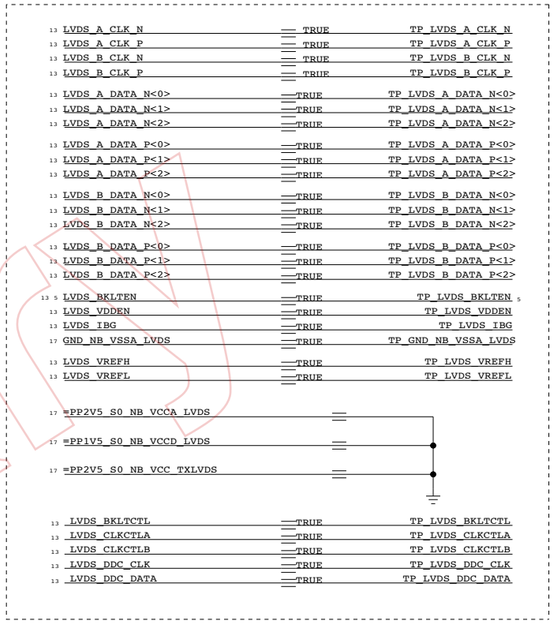

## TVOUT DISABLE



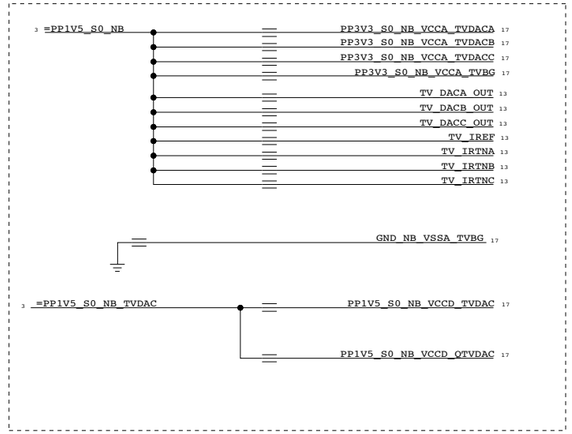

## DISPLAY DISABLE

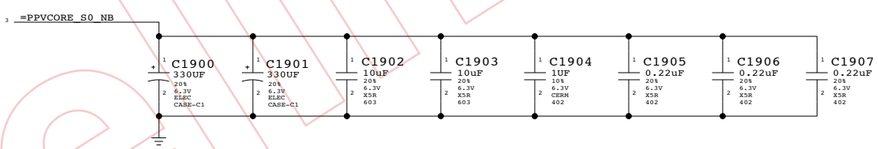


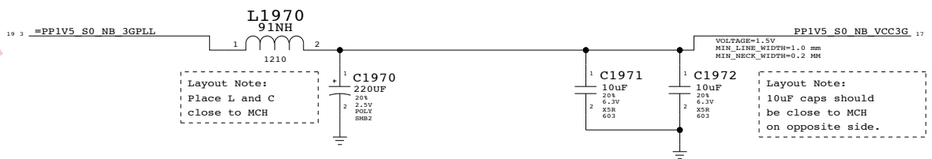

## LVDS DISABLE

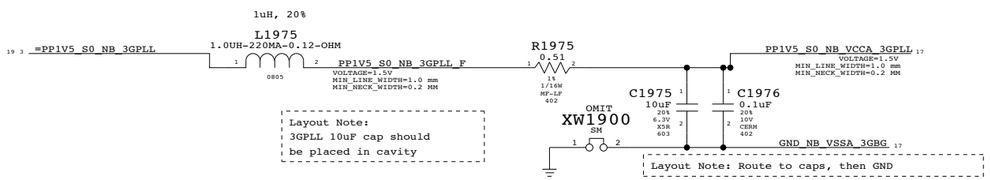



## TVOUT DISABLE






NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 19 OF 97 | |

| NB_CFG<3> | RESERVED |
|---|---|

| NB_CFG<4> | RESERVED |
|---|---|

14 NB_CFG<5>
Internal pull-up

| NB_CFG<5><br>DMI x2 Select | High = DMIx4<br>Low = DMIx2 |
|---|---|

NBCFG_DMI_X2
R2075
2.2K
5% 1/16W MF-LF 402

PROBABLY NOT NEEDED

| NB_CFG<6> | RESERVED |
|---|---|

14 NB_CFG<7>
Internal pull-up

| NB_CFG<7><br>CPU Strap | High = Mobile CPU<br>Low = RESERVED |
|---|---|

NO STUFF
R2077
2.2K
5% 1/16W MF-LF 402

| NB_CFG<8> | RESERVED |
|---|---|

14 NB_CFG<9>
Internal pull-up

| NB_CFG<9><br>PCIE Graphics<br>Lane Reversal | High = Normal<br>Low = Reversed |
|---|---|

NBCFG_PEG_REVERSE
R2079
2.2K
5% 1/16W MF-LF 402

| NB_CFG<10> | RESERVED |
|---|---|

| NB_CFG<11> | RESERVED |
|---|---|

Internal pull-ups

| NB_CFG<13:12> | 00 = Partial Clock Gating Disable<br>01 = XOR Mode Enabled<br>10 = All-Z Mode Enabled<br>11 = Normal Operation |
|---|---|

| NB_CFG<14> | RESERVED |
|---|---|

| NB_CFG<15> | RESERVED |
|---|---|

14 NB_CFG<16>
Internal pull-up

| NB_CFG<16><br>FSB Dynamic<br>ODT | High = Enabled<br>Low = Disabled |
|---|---|

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5% 1/16W MF-LF 402

| NB_CFG<17> | RESERVED |
|---|---|

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058
2.2K
5% 1/16W MF-LF 402

| NB_CFG<18><br>VCC Select | High = 1.5V<br>Low = 1.05V |
|---|---|

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059
2.2K
5% 1/16W MF-LF 402

| NB_CFG<19><br>DMI Lane<br>Reversal | High = Reversed<br>Low = Normal |
|---|---|

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5% 1/16W MF-LF 402

| NB_CFG<20><br>PCIe Backward<br>Interop. Mode | High = Both active<br>Low = Only SDVO or PCIe x1 |
|---|---|

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED



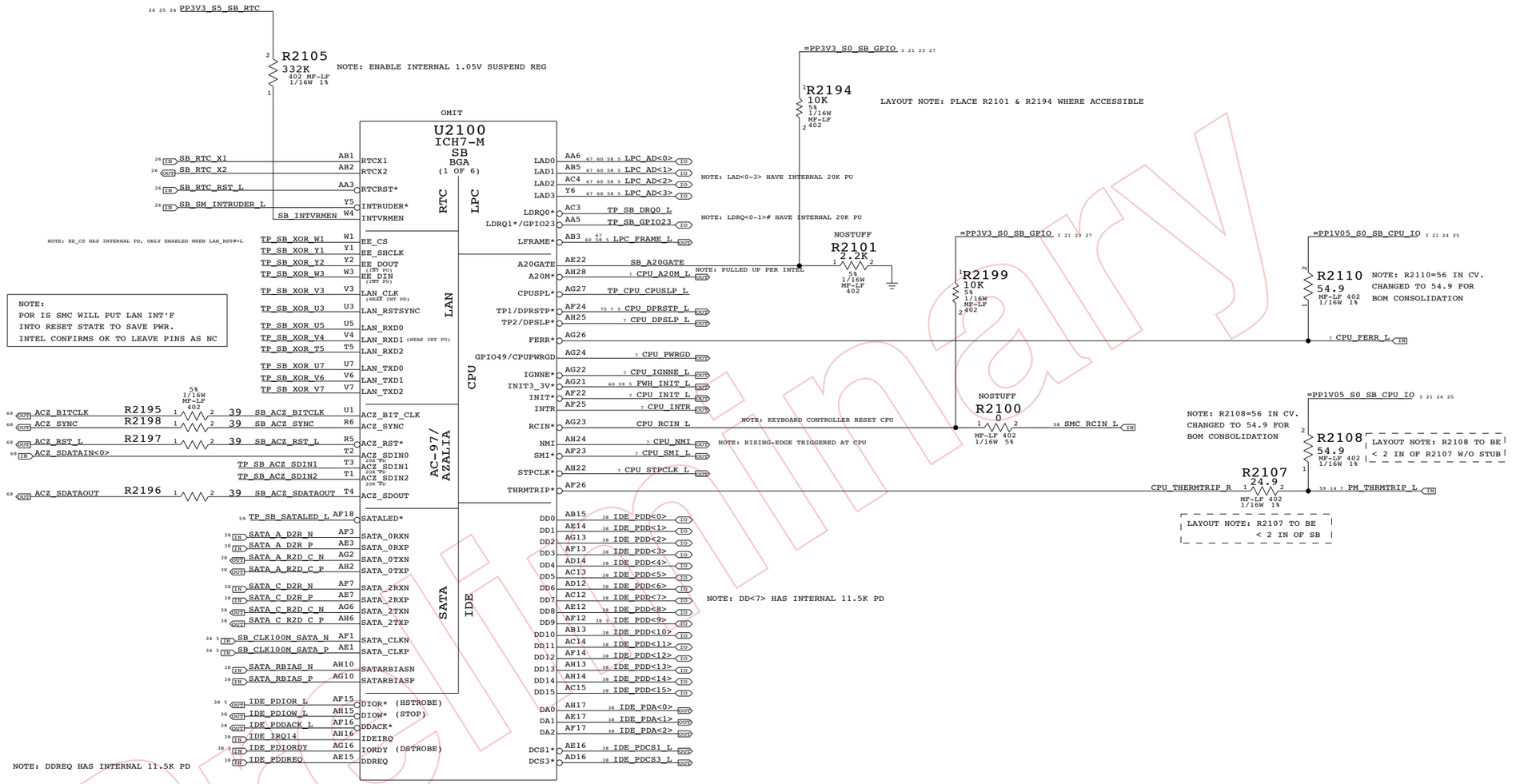
# NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 20 OF 97 | |




| | AC '07 | INTEL HIGH DEFINITION AUDIO |
|---|---|---|
| ACZ_BIT_CLK | INTERNAL 20K PD ENABLED WHEN | INTERNAL 20K PD ONLY ENABLED IN S3COLD |
| ACZ_RST# | - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR<br>- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED | NONE |
| ACZ_SDIN[0-2] | INTERNAL 20K PD | INTERNAL 20K PD |
| ACZ_SDOUT | INTERNAL 20K PD ENABLED DURING RESET AND WHEN<br>- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR<br>- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED | INTERNAL 20K PD ENABLED WHEN<br>- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR<br>- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED |
| ACZ_SYNC | | INTERNAL 20K PD |

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

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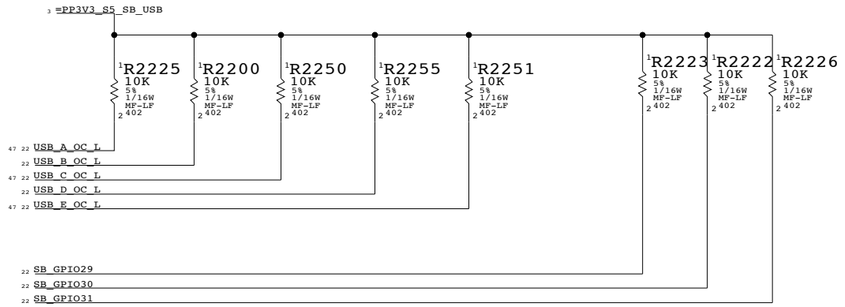
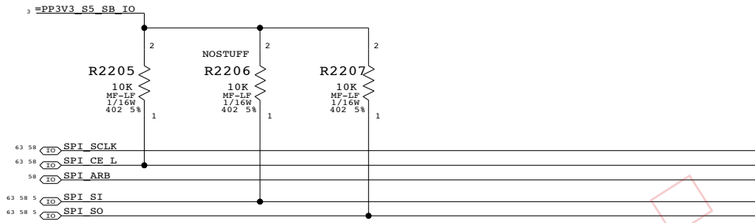
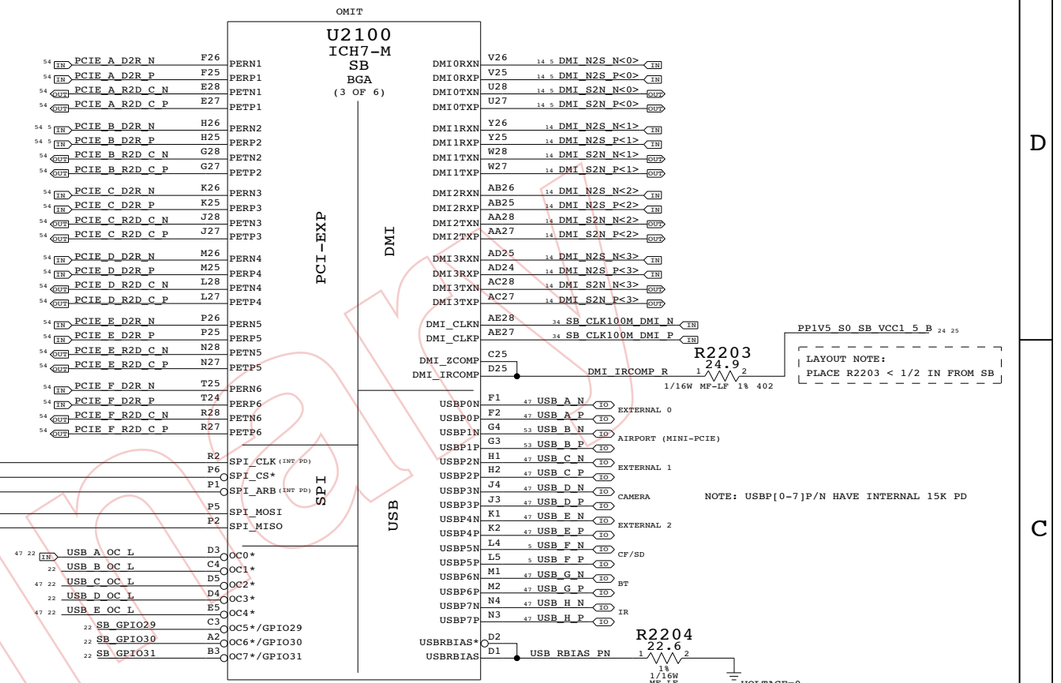
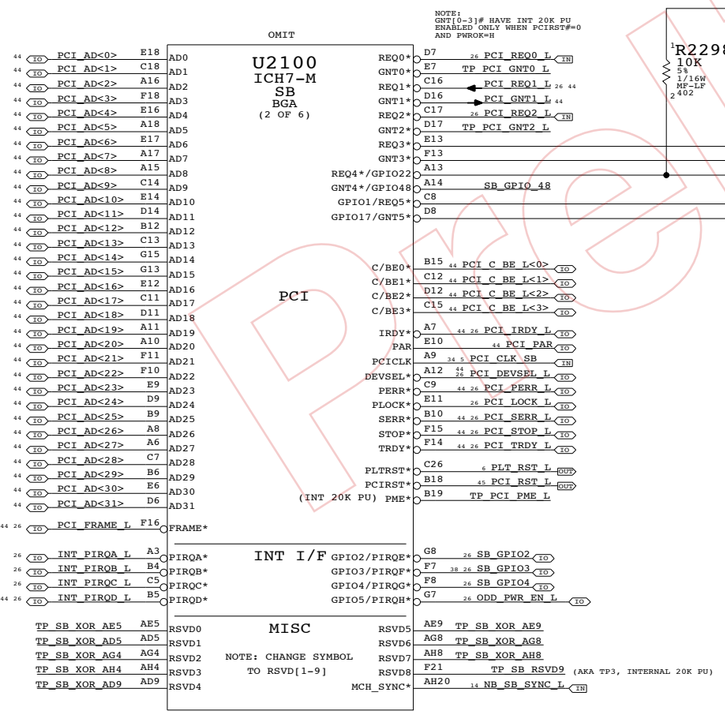
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 21 OF 97 | |

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|




SB: 2 OF 4

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 3 21 23 27

=PP3V3_S5_SB 3 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

=PP3V3_S5_SB 26 25 23 3

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

| | | |
|---|---|---|
| 27 TO SMB_CLK | C22 | SMBCLK |
| 27 TO SMB_DATA | B22 | SMBDATA |
| SMB_LINK_ALERT_L | A26 | LINKALERT* |
| SMLINK<0> | B25 | SMLINK0 |
| NOT USED SMLINK<1> | A25 | SMLINK1 |
| PM_RI_L | A28 | RI* |
| SB_SPKR | A19 | SPKR (INT WEAK PD) |
| 67 60 58 5 OUT PM_SUS_STAT_L | A27 | SUS_STAT* |
| 58 26 IN PM_SYSRST_L | A22 | SYS_RST* |
| 14 IN PM_BMBUSY_L | AB18 | GPIO0/BM_BUSY* |
| SMB_ALERT_L NOTE: RESERVED FOR FUTURE | B23 | GPIO11/SMBALERT* |
| 33 OUT PM_STPPCI_L | AC20 | GPIO18/STPPCI* |
| 34 OUT PM_STPCPU_L | AF21 | GPIO20/STPCPU* |
| SB_GPIO26 | A21 | GPIO26 |
| 23 BIOS_REC | B21 | GPIO27 |
| 23 FWH_MFG_MODE | E23 | GPIO28 |
| 67 60 58 5 TO PM_CLKRUN_L | AG18 | GPIO32/CLKRUN* |
| RESERVED FOR MOBILE AZALIA DOCKING INT'F: TP_AZ_DOCK_EN_L | AC19 | GPIO33/AZ_DOCK_EN* |
| TP_AZ_DOCK_RST_L | U2 | GPIO34/AZ_DOCK_RST* |
| 53 41 IN PCIE_WAKE_L | F20 | WAKE* |
| 67 60 58 5 TO INT_SERIRQ | AH21 | SERIRQ |
| 58 10 IN PM_THRM_L | AF20 | THRM* |
| 26 5 IN VR_PWRGD_CK410 | AD22 | VRMPWRGD |
| 6 GPU_PRESENT_R | AC21 | GPIO6 |
| 58 IN SMC_RUNTIME_SCI_L | AC18 | GPIO7 |
| 58 IN SMC_EXTSMI_L | E21 | GPIO8 |

SATA GPIO

| | | |
|---|---|---|
| GPIO21/SATA0GP | AF19 | SB_GPIO21 100 R2302 |
| GPIO19/SATA1GP | AH18 | SB_GPIO19 100 R2303 |
| GPIO36/SATA2GP | AH19 | 38 SATA_C_DET_L IN |
| GPIO37/SATA3GP | AE19 | SB_GPIO37 100 R2305 |

CLKS

| | | |
|---|---|---|
| CLK14 | AC1 | 34 5 SB_CLK14P3M_TIMER IN |
| CLK48 | B2 | 34 5 SB_CLK48M_USBCTLR IN |
| SUSCLK | C20 | 58 SUS_CLK_SB OUT |

SYS GPIO / PWR MNGT

| | | |
|---|---|---|
| SLP_S3* | B24 | 79 77 80 58 5 PM_SLP_S3_L OUT |
| SLP_S4* | D23 | 77 58 5 PM_SLP_S4_L OUT |
| SLP_S5* | F22 | 58 PM_SLP_S5_L OUT |
| PWROK | AA4 | 26 PM_SB_PWROK IN |
| GPIO16/DPRSLPVR | AC22 | 75 14 5 PM_DPRSLPVR OUT |
| TP0/BATLOW* | C21 | NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN |
| (INT 20K PU) PWRBTN* | C23 | 58 PM_PWRBTN_L IN |
| LAN_RST* | C19 | 58 PM_LAN_ENABLE IN NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR |
| RSMRST* | Y4 | |

GPIO

| | | |
|---|---|---|
| GPIO9 | E20 | 58 26 SMS_INT_L IN |
| GPIO10 | A20 | 58 SMC_SB_NMI IN |
| DEF=GPI GPIO12 | F19 | 23 PATA_PWR_EN_L OUT |
| GPIO13 | E19 | |
| DEF=GPI GPIO14 | R4 | 38 IDE_RESET_L OUT |
| GPIO15 | E22 | SV_SET_UP 5 23 60 |
| GPIO24 | R3 | TP_SB_GPIO24 |
| GPIO25 | D20 | TP_SB_GPIO25_DO_NOT_USE |
| OD GPIO35 | AD21 | 23 SB_CLK100M_SATA_OE_L OUT |
| GPIO38 | AD20 | TP_SB_GPIO38 TO |
| DEF=GPI GPIO39 | AE20 | 23 SATA_C_PWR_EN_L OUT |

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 350S AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 3 11

R2387 10K 1/16W 402 MF-LF 5% NOSTUFF
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L IN
58 PM_RSMRST_L IN
58 SMC_WAKE_SCI_L IN

R2399 100K 5% 1/16W 402 MF-LF

=PP3V3_S5_SB 26 25 23 3

R2306 10K 1/16W 402 MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 MF-LF 5% NOSTUFF
R2307 10K 1/16W 402 MF-LF 5%
R2309 10K 1/16W 402 MF-LF 5%

SV_SET_UP 5 23 60
EFI_OK_R

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

=PP3V3_S5_SB 26 25 23 3

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 0 1/16W 402 MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 MF-LF 5% NOSTUFF

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 3 23 25 26

R2390 10K 5% 1/16W MF-LF 402
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 3 21 23 27

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L



SB: 3 OF 4

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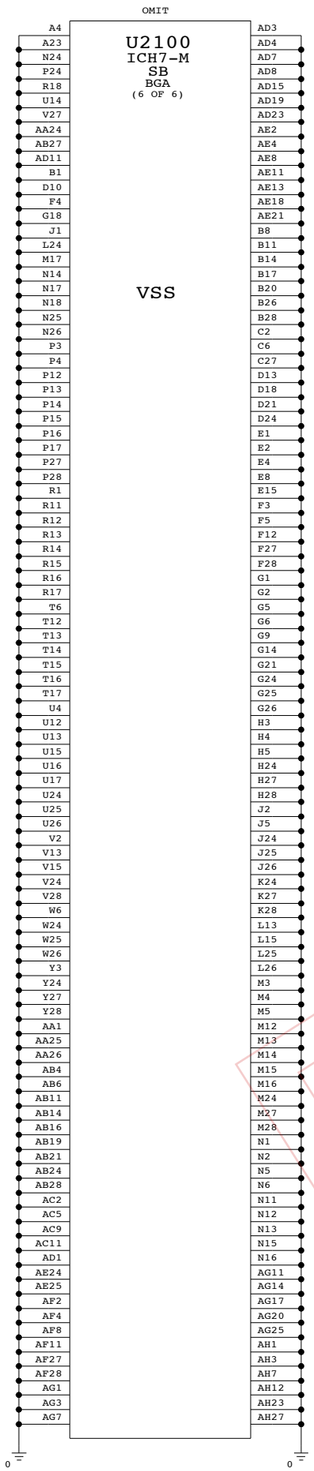


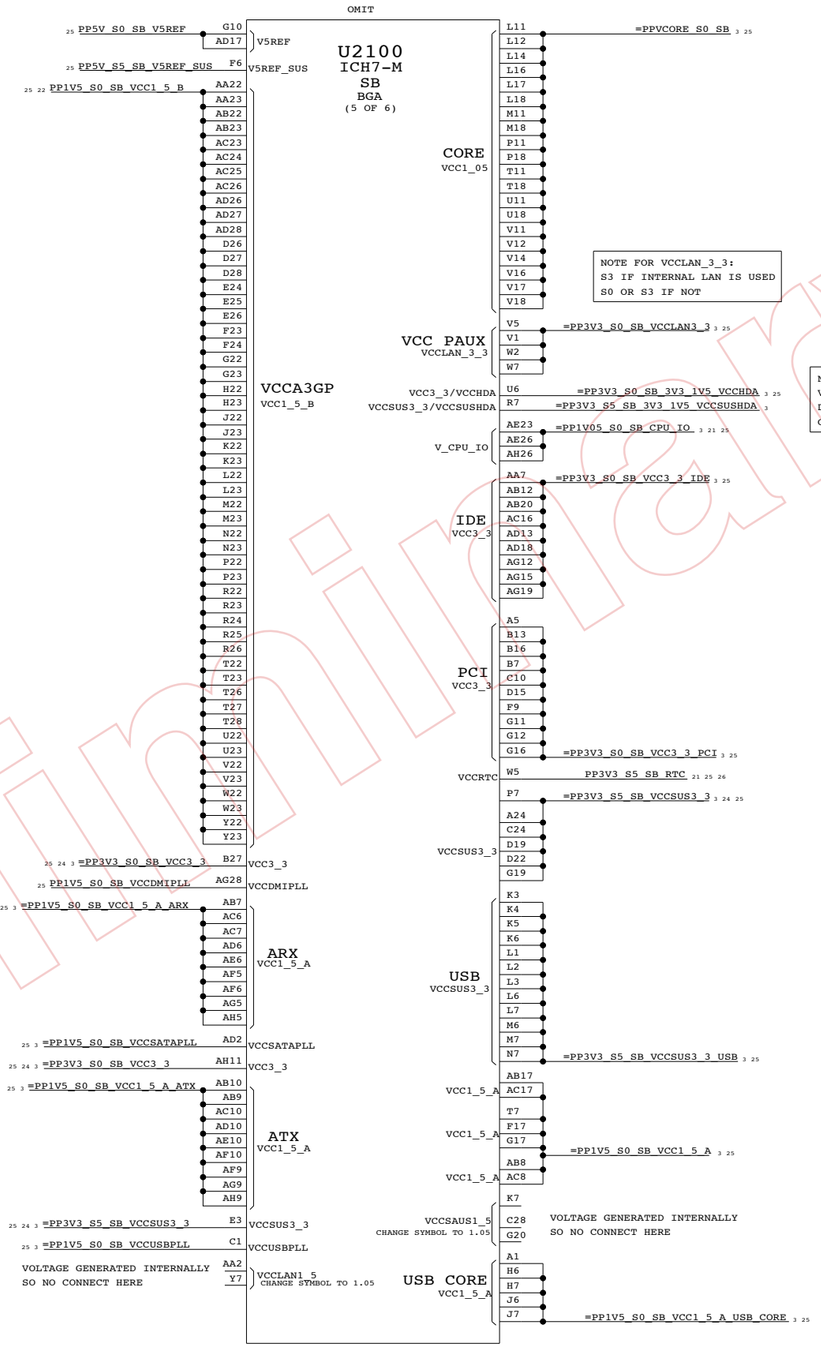




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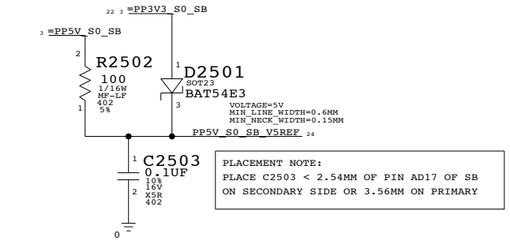


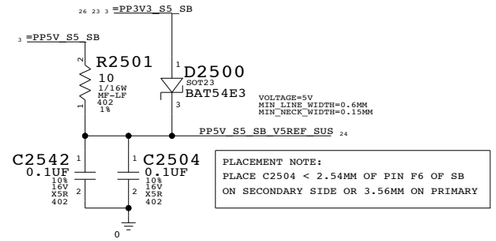


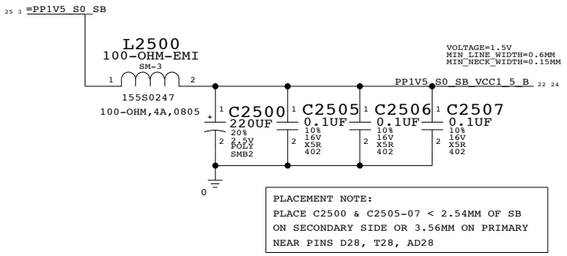


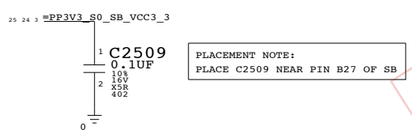


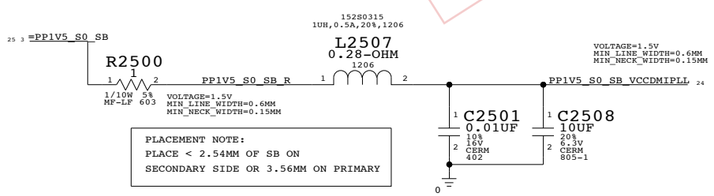


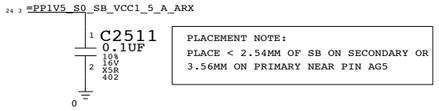


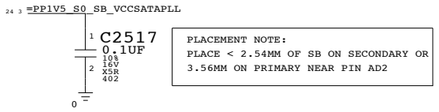


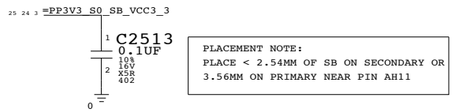


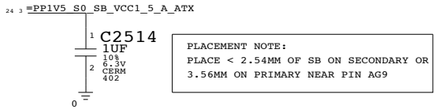


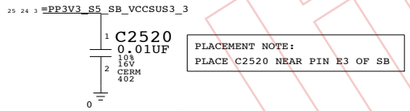


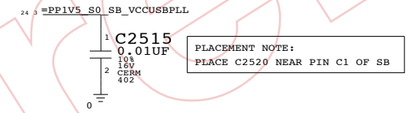


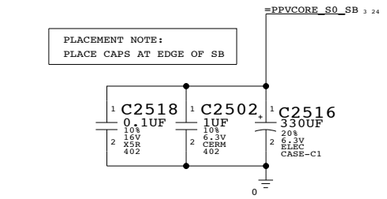


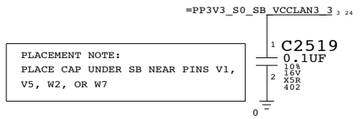


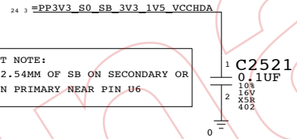


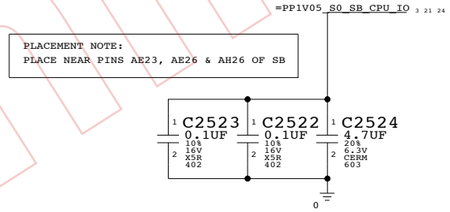


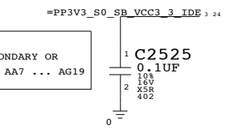


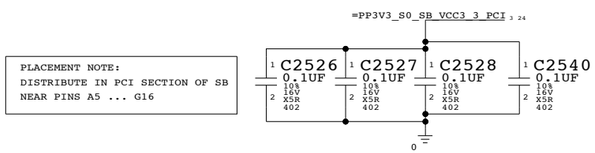


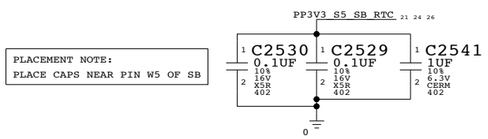


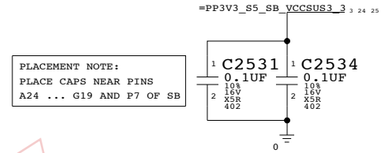


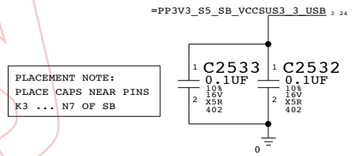


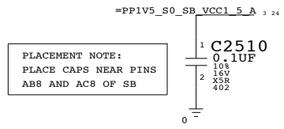


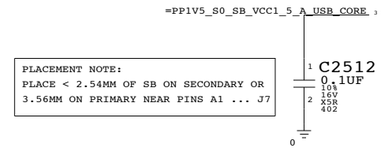




# SB:DECOUPLING

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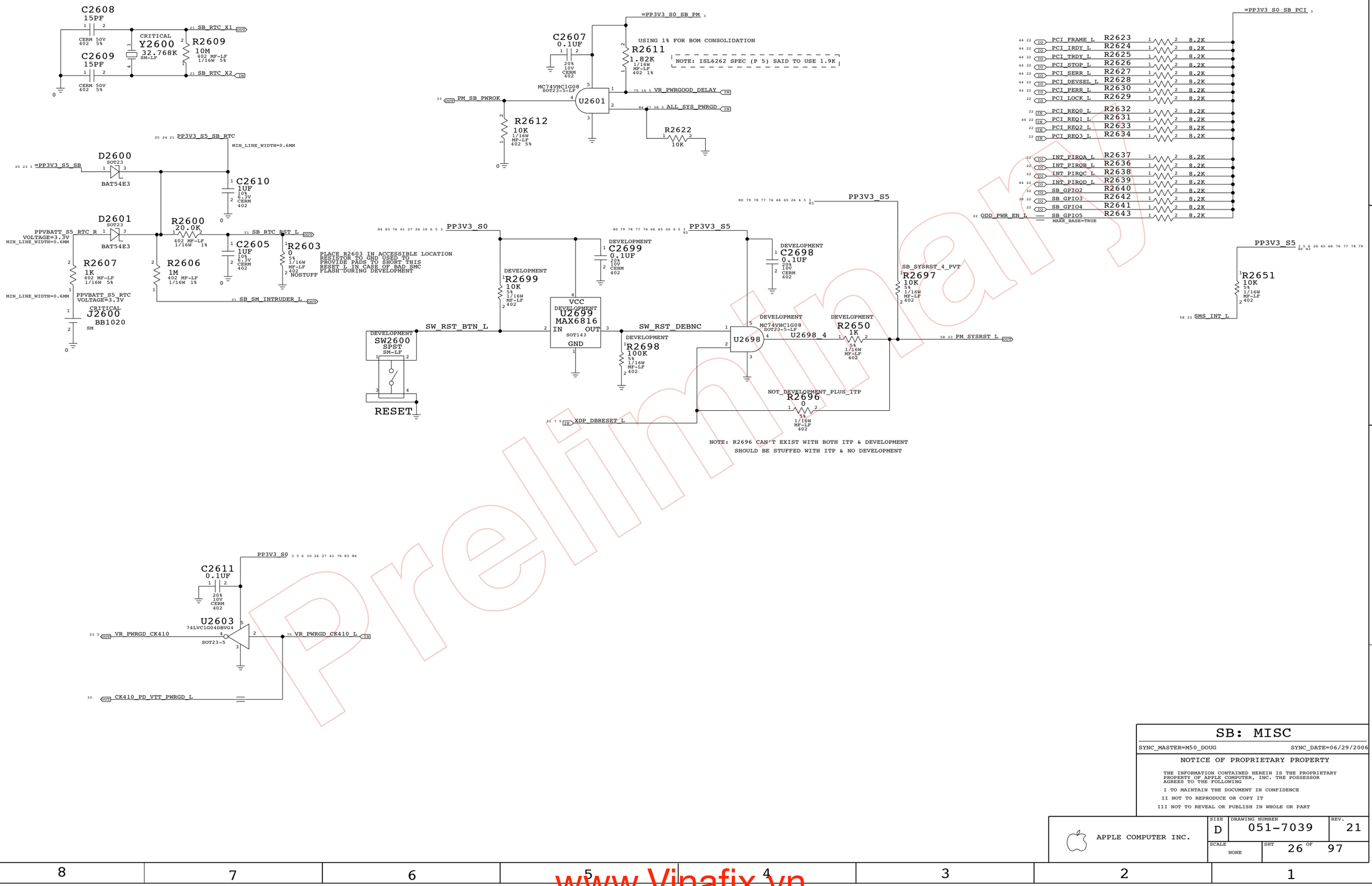




## SB: MISC

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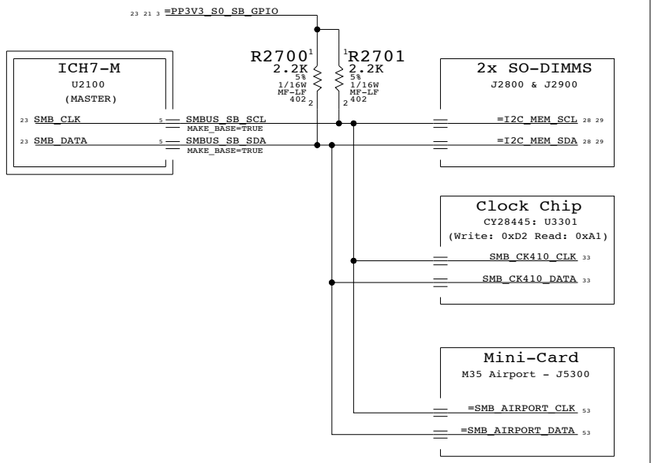
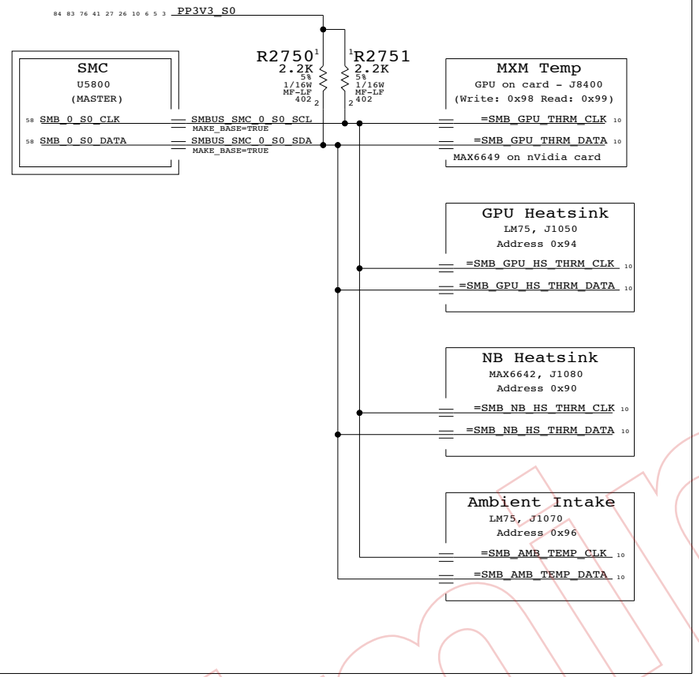
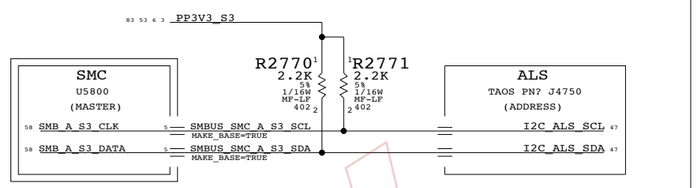
## ICH7-M SMBus Connections



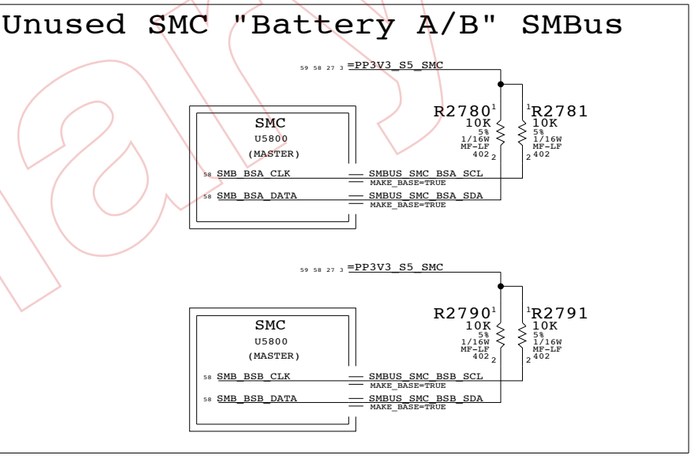

## SMC "0" SMBus Connections




## SMC "A" SMBus Connections




## Unused SMC "Battery A/B" SMBus

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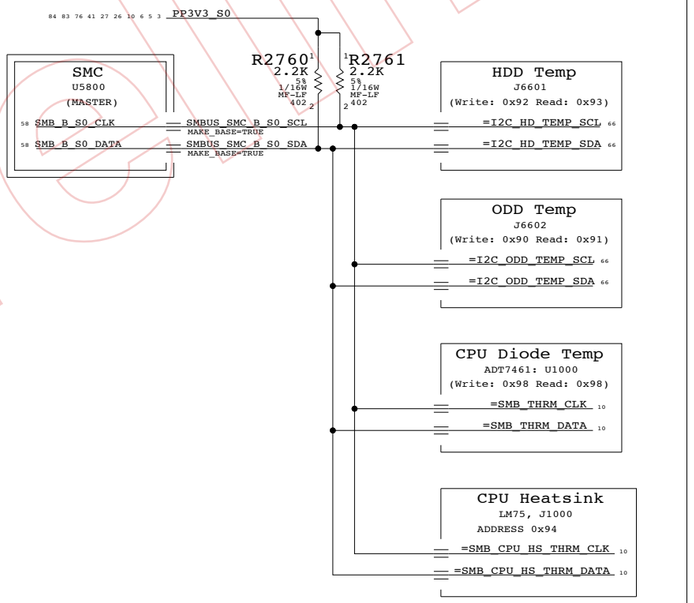


# M51 SMBus Connections

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# Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

## DDR2 VRef

One 0.1uF per connector

=PP1V8_S3_MEM (29 28 3)

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF (28 29) VOLTAGE=0.9V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

MEM_VREF (29 28)

C2850 2.2UF 10% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM (29 28 3)

## J2800

CRITICAL

DDR2-SODIMM-STD

F-RT-SM2

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | VREF | 1 | 2 | VSS0 | | |
| | | VSS1 | 3 | 4 | DQ4 | MEM_A_DQ<4> | 15 |
| 15 | MEM_A_DQ<0> | DQ0 | 5 | 6 | DQ5 | MEM_A_DQ<5> | 15 |
| 15 | MEM_A_DQ<1> | DQ1 | 7 | 8 | VSS2 | | |
| | | VSS4 | 9 | 10 | DM0 | MEM_A_DM<0> | 15 |
| 15 | MEM_A_DQS_N<0> | DQS0* | 11 | 12 | VSS5 | | |
| 15 | MEM_A_DQS_P<0> | DQS0 | 13 | 14 | DQ6 | MEM_A_DQ<6> | 15 |
| | | VSS6 | 15 | 16 | DQ7 | MEM_A_DQ<7> | 15 |
| 15 | MEM_A_DQ<2> | DQ2 | 17 | 18 | VSS7 | | |
| 15 | MEM_A_DQ<3> | DQ3 | 19 | 20 | DQ12 | MEM_A_DQ<12> | 15 |
| | | VSS8 | 21 | 22 | DQ13 | MEM_A_DQ<13> | 15 |
| 15 | MEM_A_DQ<8> | DQ8 | 23 | 24 | VSS9 | | |
| 15 | MEM_A_DQ<9> | DQ9 | 25 | 26 | DM1 | MEM_A_DM<1> | 15 |
| | | VSS10 | 27 | 28 | VSS11 | | |
| 15 | MEM_A_DQS_N<1> | DQS1* | 29 | 30 | CK0 | MEM_CLK_P<0> | 14 |
| 15 | MEM_A_DQS_P<1> | DQS1 | 31 | 32 | CK0* | MEM_CLK_N<0> | 14 |
| | | VSS12 | 33 | 34 | VSS13 | | |
| 15 | MEM_A_DQ<10> | DQ10 | 35 | 36 | DQ14 | MEM_A_DQ<14> | 15 |
| 15 | MEM_A_DQ<11> | DQ11 | 37 | 38 | DQ15 | MEM_A_DQ<15> | 15 |
| | | VSS14 | 39 | 40 | VSS15 | | |
| | | | | KEY | | | |
| | | VSS16 | 41 | 42 | VSS17 | | |
| 15 | MEM_A_DQ<16> | DQ16 | 43 | 44 | DQ20 | MEM_A_DQ<20> | 15 |
| 15 | MEM_A_DQ<17> | DQ17 | 45 | 46 | DQ21 | MEM_A_DQ<21> | 15 |
| | | VSS18 | 47 | 48 | VSS19 | | |
| 15 | MEM_A_DQS_N<2> | DQS2* | 49 | 50 | NC0 | DIMM_OVERTEMP_L | 29 59 |
| 15 | MEM_A_DQS_P<2> | DQS2 | 51 | 52 | DM2 | MEM_A_DM<2> | 15 |
| | | VSS21 | 53 | 54 | VSS22 | | |
| 15 | MEM_A_DQ<18> | DQ18 | 55 | 56 | DQ22 | MEM_A_DQ<22> | 15 |
| 15 | MEM_A_DQ<19> | DQ19 | 57 | 58 | DQ23 | MEM_A_DQ<23> | 15 |
| | | VSS23 | 59 | 60 | VSS24 | | |
| 15 | MEM_A_DQ<24> | DQ24 | 61 | 62 | DQ28 | MEM_A_DQ<28> | 15 |
| 15 | MEM_A_DQ<25> | DQ25 | 63 | 64 | DQ29 | MEM_A_DQ<29> | 15 |
| | | VSS25 | 65 | 66 | VSS26 | | |
| 15 | MEM_A_DM<3> | DM3 | 67 | 68 | DQS3* | MEM_A_DQS_N<3> | 15 |
| | NC | NC1 | 69 | 70 | DQS3 | MEM_A_DQS_P<3> | 15 |
| | | VSS27 | 71 | 72 | VSS28 | | |
| 15 | MEM_A_DQ<26> | DQ26 | 73 | 74 | DQ30 | MEM_A_DQ<30> | 15 |
| 15 | MEM_A_DQ<27> | DQ27 | 75 | 76 | DQ31 | MEM_A_DQ<31> | 15 |
| | | VSS29 | 77 | 78 | VSS30 | | |
| 30 14 | MEM_CKE<0> | CKE0 | 79 | 80 | NC/CKE1 | MEM_CKE<1> | 14 30 |
| | | VDD0 | 81 | 82 | VDD1 | | |
| | NC | NC2 | 83 | 84 | NC/A15 | TP_MEM_A_A<15> | |
| 30 15 | MEM_A_BS<2> | BA2 | 85 | 86 | NC/A14 | TP_MEM_A_A<14> | |
| | | VDD2 | 87 | 88 | VDD3 | | |
| 30 15 | MEM_A_A<12> | A12 | 89 | 90 | A11 | MEM_A_A<11> | 15 30 |
| 30 15 | MEM_A_A<9> | A9 | 91 | 92 | A7 | MEM_A_A<7> | 15 30 |
| 30 15 | MEM_A_A<8> | A8 | 93 | 94 | A6 | MEM_A_A<6> | 15 30 |
| | | VDD4 | 95 | 96 | VDD5 | | |
| 30 15 | MEM_A_A<5> | A5 | 97 | 98 | A4 | MEM_A_A<4> | 15 30 |
| 30 15 | MEM_A_A<3> | A3 | 99 | 100 | A2 | MEM_A_A<2> | 15 30 |
| 30 15 | MEM_A_A<1> | A1 | 101 | 102 | A0 | MEM_A_A<0> | 15 30 |
| | | VDD6 | 103 | 104 | VDD7 | | |
| 30 15 | MEM_A_A<10> | A10/AP | 105 | 106 | BA1 | MEM_A_BS<1> | 15 30 |
| 30 15 | MEM_A_BS<0> | BA0 | 107 | 108 | RAS* | MEM_A_RAS_L | 15 30 |
| 30 15 | MEM_A_WE_L | WE* | 109 | 110 | S0* | MEM_CS_L<0> | 14 30 |
| | | VDD8 | 111 | 112 | VDD9 | | |
| 30 15 | MEM_A_CAS_L | CAS* | 113 | 114 | ODT0 | MEM_ODT<0> | 14 30 |
| 30 14 | MEM_CS_L<1> | NC/S1* | 115 | 116 | NC/A13 | MEM_A_A<13> | 15 30 |
| | | VDD10 | 117 | 118 | VDD11 | | |
| 30 14 | MEM_ODT<1> | NC/ODT1 | 119 | 120 | NC3 | NC | |
| | | VSS31 | 121 | 122 | VSS32 | | |
| 15 | MEM_A_DQ<32> | DQ32 | 123 | 124 | DQ36 | MEM_A_DQ<36> | 15 |
| 15 | MEM_A_DQ<33> | DQ33 | 125 | 126 | DQ37 | MEM_A_DQ<37> | 15 |
| | | VSS33 | 127 | 128 | VSS34 | | |
| 15 | MEM_A_DQS_N<4> | DQS4* | 129 | 130 | DM4 | MEM_A_DM<4> | 15 |
| 15 | MEM_A_DQS_P<4> | DQS4 | 131 | 132 | VSS35 | | |
| | | VSS36 | 133 | 134 | DQ38 | MEM_A_DQ<38> | 15 |
| 15 | MEM_A_DQ<34> | DQ34 | 135 | 136 | DQ39 | MEM_A_DQ<39> | 15 |
| 15 | MEM_A_DQ<35> | DQ35 | 137 | 138 | VSS37 | | |
| | | VSS38 | 139 | 140 | DQ44 | MEM_A_DQ<44> | 15 |
| 15 | MEM_A_DQ<40> | DQ40 | 141 | 142 | DQ45 | MEM_A_DQ<45> | 15 |
| 15 | MEM_A_DQ<41> | DQ41 | 143 | 144 | VSS39 | | |
| | | VSS40 | 145 | 146 | DQS5* | MEM_A_DQS_N<5> | 15 |
| 15 | MEM_A_DM<5> | DM5 | 147 | 148 | DQS5 | MEM_A_DQS_P<5> | 15 |
| | | VSS41 | 149 | 150 | VSS42 | | |
| 15 | MEM_A_DQ<42> | DQ42 | 151 | 152 | DQ46 | MEM_A_DQ<46> | 15 |
| 15 | MEM_A_DQ<43> | DQ43 | 153 | 154 | DQ47 | MEM_A_DQ<47> | 15 |
| | | VSS43 | 155 | 156 | VSS44 | | |
| 15 | MEM_A_DQ<48> | DQ48 | 157 | 158 | DQ52 | MEM_A_DQ<52> | 15 |
| 15 | MEM_A_DQ<49> | DQ49 | 159 | 160 | DQ53 | MEM_A_DQ<53> | 15 |
| | | VSS45 | 161 | 162 | VSS46 | | |
| | NC | NC_TEST | 163 | 164 | CK1 | MEM_CLK_P<1> | 14 |
| | | VSS47 | 165 | 166 | CK1* | MEM_CLK_N<1> | 14 |
| 15 | MEM_A_DQS_N<6> | DQS6* | 167 | 168 | VSS48 | | |
| 15 | MEM_A_DQS_P<6> | DQS6 | 169 | 170 | DM6 | MEM_A_DM<6> | 15 |
| | | VSS49 | 171 | 172 | VSS50 | | |
| 15 | MEM_A_DQ<50> | DQ50 | 173 | 174 | DQ54 | MEM_A_DQ<54> | 15 |
| 15 | MEM_A_DQ<51> | DQ51 | 175 | 176 | DQ55 | MEM_A_DQ<55> | 15 |
| | | VSS51 | 177 | 178 | VSS52 | | |
| 15 | MEM_A_DQ<56> | DQ56 | 179 | 180 | DQ60 | MEM_A_DQ<60> | 15 |
| 15 | MEM_A_DQ<57> | DQ57 | 181 | 182 | DQ61 | MEM_A_DQ<61> | 15 |
| | | VSS53 | 183 | 184 | VSS54 | | |
| 15 | MEM_A_DM<7> | DM7 | 185 | 186 | DQS7* | MEM_A_DQS_N<7> | 15 |
| | | VSS55 | 187 | 188 | DQS7 | MEM_A_DQS_P<7> | 15 |
| 15 | MEM_A_DQ<58> | DQ58 | 189 | 190 | VSS56 | | |
| 15 | MEM_A_DQ<59> | DQ59 | 191 | 192 | DQ62 | MEM_A_DQ<62> | 15 |
| | | VSS57 | 193 | 194 | DQ63 | MEM_A_DQ<63> | 15 |
| 29 27 | =I2C_MEM_SDA | SDA | 195 | 196 | VSS58 | | |
| 29 27 | =I2C_MEM_SCL | SCL | 197 | 198 | SA0 | | |
| | | VDDSPD | 199 | 200 | SA1 | ADDR=0xA0(WR)/0xA1(RD) | |
| | | GND | 201 202 203 204 205 | | | | |

516S0403

SOME ANCHOR PINS CONNECTED TO NETS TO IMPROVE PLANE FOUR

=PP1V8_S3_MEM (3 28 29)

=PPSPD_S0_MEM (29 3)

C2851 2.2UF 10% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

## DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM (29 28 3)

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

## DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

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|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 28 OF 97 | |

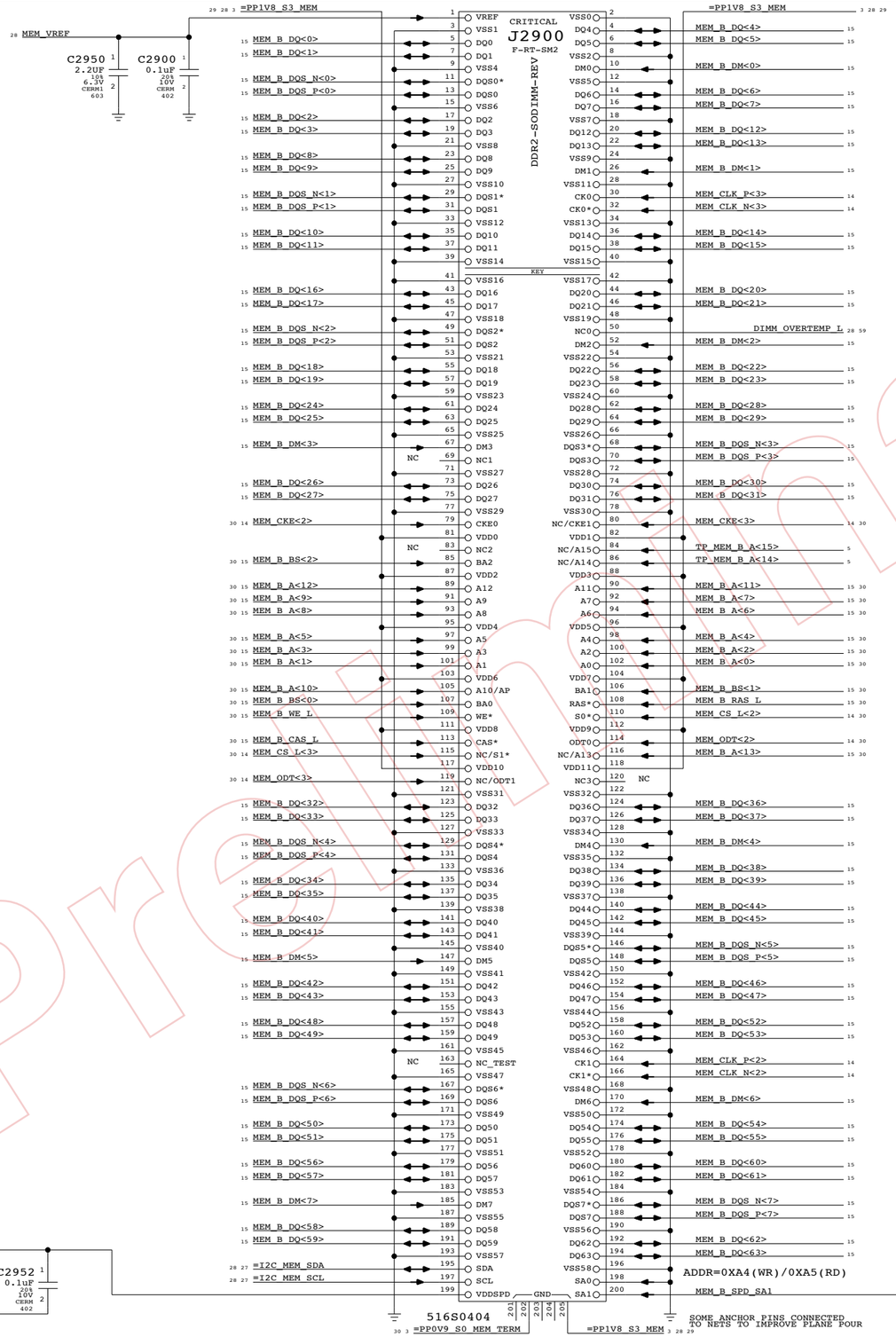
# Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

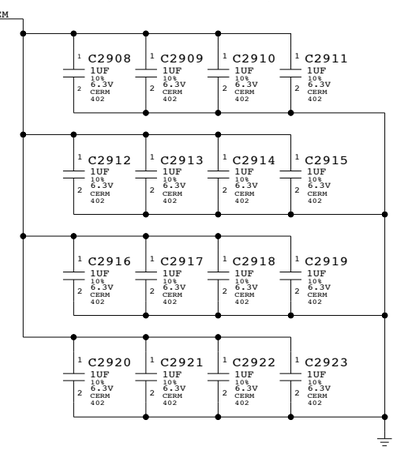
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.




## DDR2 Bypass Caps

(For return current)




## DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



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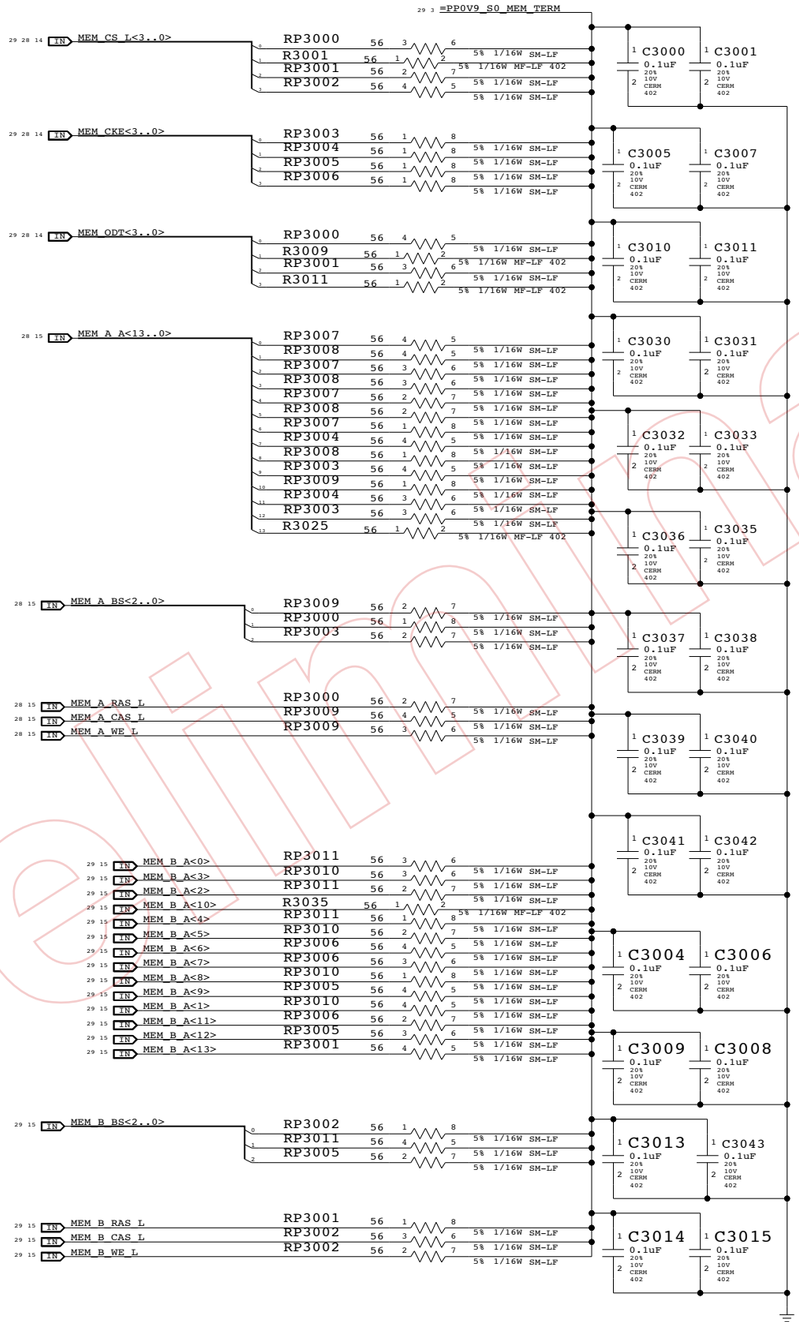
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 29 OF 97 | |

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it






Memory Active Termination



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|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 30 OF 97 | |

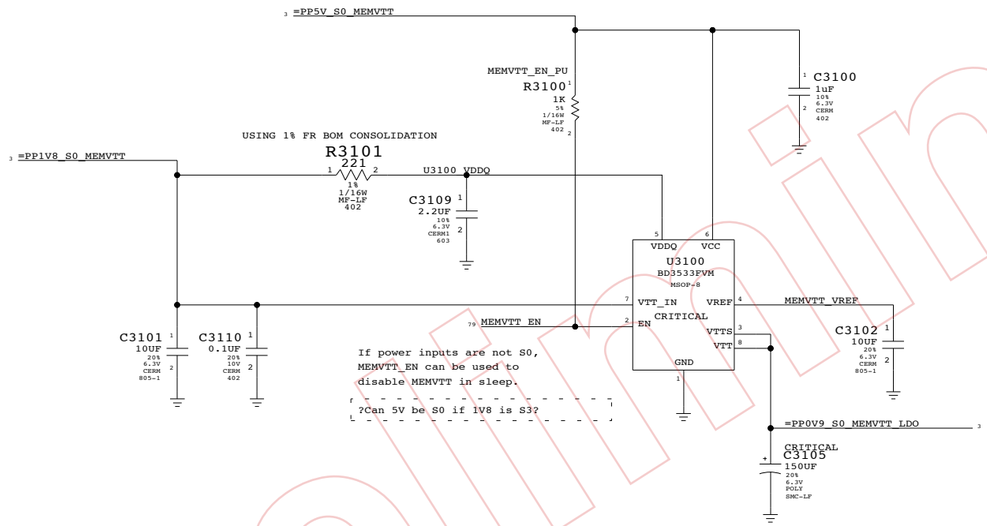
## Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

# DDR2 Vtt Regulator






## Memory Vtt Supply

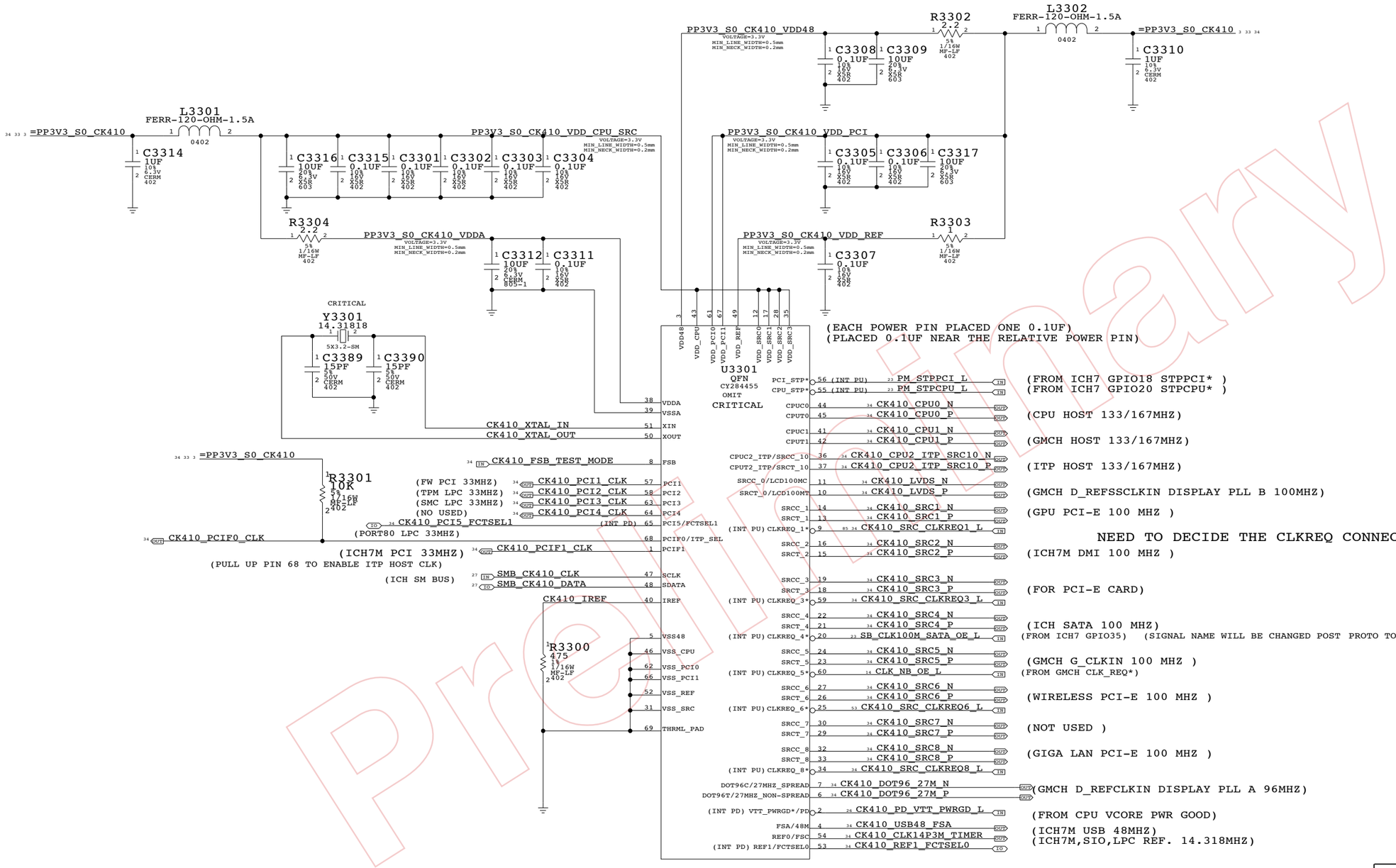
SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 31 OF 97




| FCTSEL1 | FCTSEL0 | PIN 6 | PIN 7 | PIN 10 | PIN 11 | |
|---|---|---|---|---|---|---|
| 0 | 0 | DOT96T | DOT96C | 100MT_SST | 100MC_SST | * FOR INT. GRAPHIC SYSTEM |
| 0 | 1 | DOT96T | DOT96C | SRCT0 | SRCC0 | |
| 1 | 0 | 27M NON SPREAD | 27M SPREAD | SRCT0 | SRCC0 | * FOR EXT. GRAPHIC SYSTEM |
| 1 | 1 | OFF LOW | TBD | SRCT0 | SRCC0 | |

## CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 33 OF 97 | |

FSB FREQUENCY SELECT:

| | STUFF | NO STUFF |
|---|---|---|
| CPU DRIVEN | R3454<br>R3459<br>R3463 | R3452<br>R3457<br>R3461 |
| 533MHZ (133MHZ CPU CLK) | R3452<br>R3457<br>R3461 | R3454<br>R3459<br>R3463 |
| 667MHZ (166MHZ CPU CLK) | R3452<br>R3461 | R3454<br>R3459<br>R3463<br>R3457 |

80 34 5 3 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402
14 NB_BSEL<0>
34 CK410_FSA
R3455 1K 1/16W 5% MF-LF 402
7 CPU_BSEL<0>

NOSTUFF R3452 56 5% 1/16W MF-LF 402
R3454 0 5% 1/16W MF-LF 402

80 34 5 3 PP1V05_S0

R3458 1K 1/16W 5% MF-LF 402
14 NB_BSEL<1>
33 CK410_FSB_TEST_MODE
7 CPU_BSEL<1>

R3456 1K 5% 1/16W MF-LF 402
NOSTUFF R3457 0 5% 1/16W MF-LF 402
R3459 0 5% 1/16W MF-LF 402

80 34 5 3 PP1V05_S0

R3462 1K 1/16W 5% MF-LF 402
14 NB_BSEL<2>
34 CK410_FSC
7 CPU_BSEL<2>

R3460 1K 5% 1/16W MF-LF 402
NOSTUFF R3461 0 5% 1/16W MF-LF 402
R3463 0 5% 1/16W MF-LF 402

33 CK410_PCI5_FCTSEL1 R3499 1K 1/16W 5% MF-LF 402 =PP3V3_S0_CK410 3 33

R3497 2.2K 5% 1/16W MF-LF 402 CK410_FSC 34
33 CK410_CLK14P3M_TIMER R3498 33 1/16W 5% MF-LF 402 SB_CLK14P3M_TIMER 5 23
33 CK410_REF1_FCTSEL0 R3496 33 TP_CLK14P3M_SPARE

R3451 2.2K 5% 1/16W MF-LF 402 CK410_FSA 34
33 CK410_USB48_FSA R3400 33 1/16W 5% MF-LF 402 SB_CLK48M_USBCTLR 5 23
33 CK410_PCI4_CLK R3406 33 TP_PCI_CLK_SPARE
33 CK410_PCI3_CLK R3405 33 PCI_CLK_SMC 5 58
33 CK410_PCI2_CLK R3404 33 NOSTUFF PCI_CLK_TPM 47
33 CK410_PCI1_CLK R3403 33 PCI_CLK_FW 5 44

33 CK410_PCIF1_CLK R3401 33 PCI_CLK_SB 5 22
33 CK410_PCIF0_CLK R3402 33 PCI_CLK_PORT80 5 60

33 CK410_SRC3_P 33 R3492 SPARE_SRC3_P R3488 49.9
33 CK410_SRC3_N 33 R3491 SPARE_SRC3_N R3487 49.9
33 CK410_SRC7_P 33 R3490 SPARE_SRC7_P R3486 49.9
33 CK410_SRC7_N 33 R3489 SPARE_SRC7_N R3485 49.9

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

85 33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) R3495 NOSTUFF 1K
33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) R3494 1K
33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) R3493 1K

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

TPM CLOCK IS TURNED OFF IN SW AND RESISTOR NOSTUFF

| | | | | | |
|---|---|---|---|---|---|
| 33 CK410_CPU1_P | 33 | R3407 | 12 FSB_CLK_NB_P | R3429 | 49.9 |
| 33 CK410_CPU1_N | 33 | R3408 | 12 FSB_CLK_NB_N | R3430 | 49.9 |
| 33 CK410_CPU0_P | 33 | R3409 | 7 FSB_CLK_CPU_P | R3431 | 49.9 |
| 33 CK410_CPU0_N | 33 | R3410 | 7 FSB_CLK_CPU_N | R3432 | 49.9 |
| 33 CK410_CPU2_ITP_SRC10_P | 33 | R3411 | 11 5 CPU_XDP_CLK_P (MAKE_BASE=TRUE FSB_CLK_XDP_P) | R3433 | 49.9 |
| 33 CK410_CPU2_ITP_SRC10_N | 33 | R3412 | 11 5 CPU_XDP_CLK_N (FSB_CLK_XDP_N MAKE_BASE=TRUE) | R3434 | 49.9 |
| 33 CK410_SRC6_P | 33 | R3413 | 53 AIRPORT_CLK100M_PCIE_P | R3435 | 49.9 |
| 33 CK410_SRC6_N | 33 | R3414 | 53 AIRPORT_CLK100M_PCIE_N | R3436 | 49.9 |
| 33 CK410_SRC5_P | 33 | R3415 | 14 NB_CLK100M_GCLKIN_P | R3438 | 49.9 |
| 33 CK410_SRC5_N | 33 | R3416 | 14 NB_CLK100M_GCLKIN_N | R3437 | 49.9 |
| 33 CK410_SRC4_P | 33 | R3417 | 21 5 SB_CLK100M_SATA_P | R3439 | 49.9 |
| 33 CK410_SRC4_N | 33 | R3418 | 21 5 SB_CLK100M_SATA_N | R3440 | 49.9 |
| 33 CK410_SRC2_P | 33 | R3419 | 22 SB_CLK100M_DMI_P | R3442 | 49.9 |
| 33 CK410_SRC2_N | 33 | R3420 | 22 SB_CLK100M_DMI_N | R3441 | 49.9 |
| 33 CK410_SRC8_P | 33 | R3421 | 41 ENET_CLK100M_PCIE_P | R3443 | 49.9 |
| 33 CK410_SRC8_N | 33 | R3422 | 41 ENET_CLK100M_PCIE_N | R3444 | 49.9 |
| 33 CK410_SRC1_P | 33 | R3423 | 85 GPU_CLK100M_PCIE_P | R3446 | 49.9 |
| 33 CK410_SRC1_N | 33 | R3424 | 85 GPU_CLK100M_PCIE_N | R3445 | 49.9 |

All: 1% 402 1/16W MF-LF

33 CK410_LVDS_P (MAKE_BASE=TRUE) TP_CK410_LVDS_P
33 CK410_LVDS_N (MAKE_BASE=TRUE) TP_CK410_LVDS_N

33 CK410_DOT96_27M_N (MAKE_BASE=TRUE) TP_CK410_27M_SPREAD
33 CK410_DOT96_27M_P (MAKE_BASE=TRUE) TP_CK410_27M_NONSPREAD

# CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



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| D | 051-7039 | 21 |
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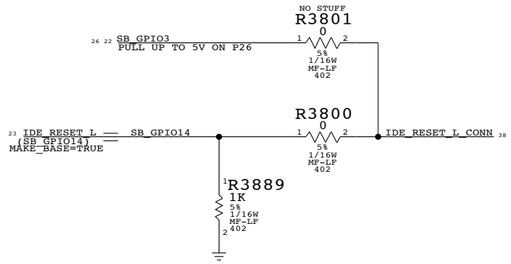
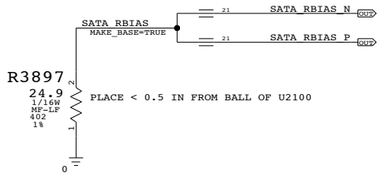
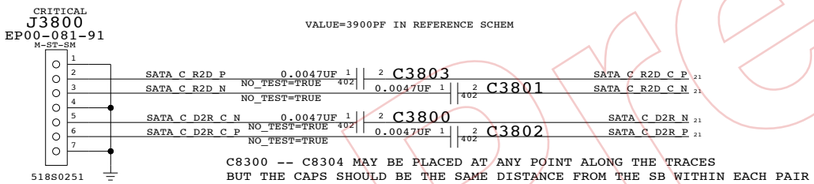
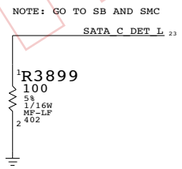
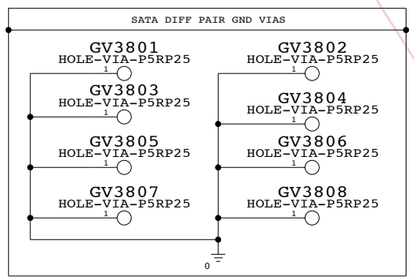


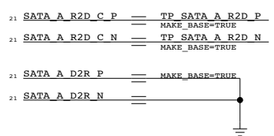

## SATA CONNECTOR



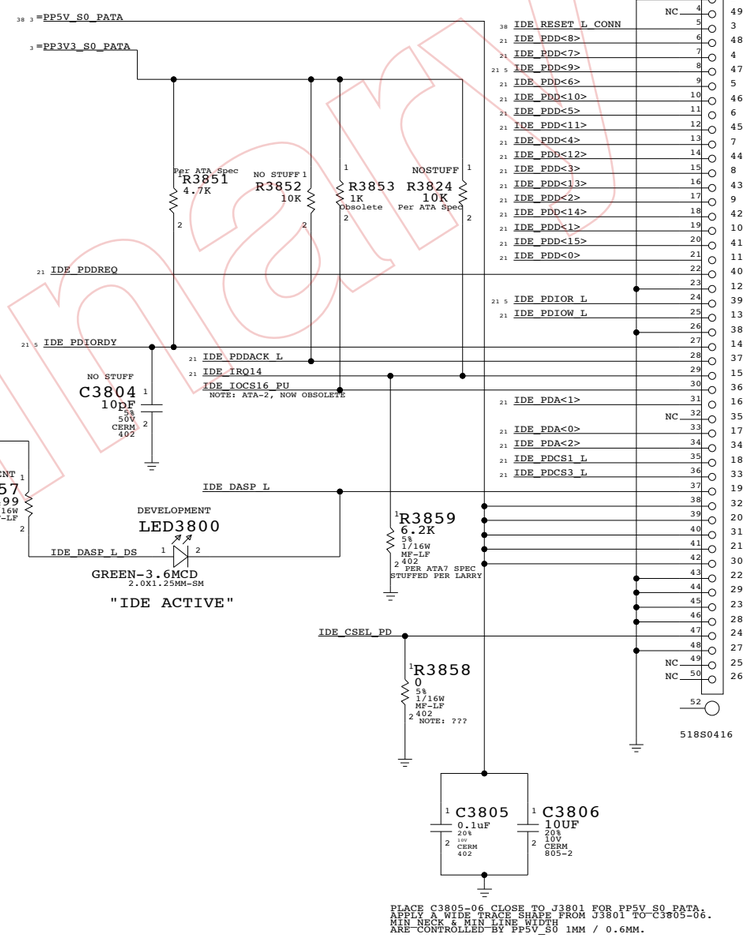




SATA PORT 0 IS NOT USED




## PATA (ODD) CONNECTOR




# Disk Connectors

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006



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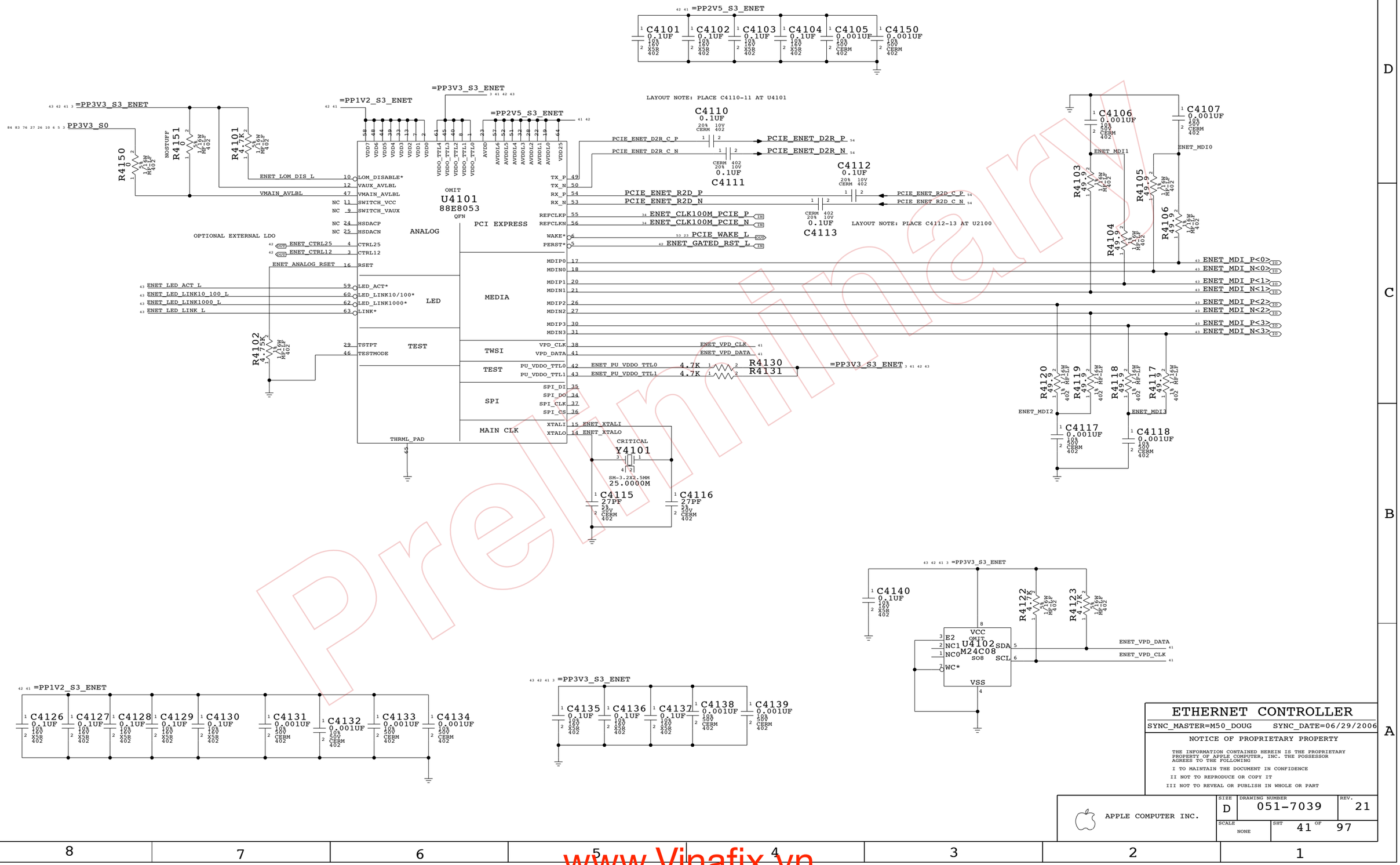
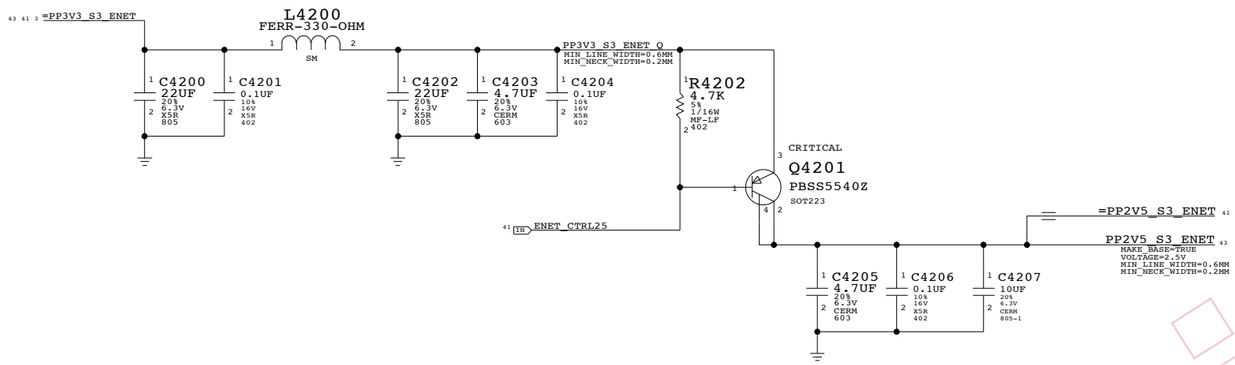
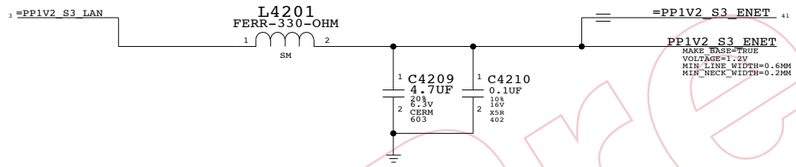
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 38 OF 97 | |










ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006



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|---|---|---|
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RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED

42 PP2V5_S3_ENET — R4300 0 5% 1/8W MF-LF 805 — PP2V5_ENET_CTAP

MIN_LINE_WIDTH=0.30mm
MIN_NECK_WIDTH=0.10mm
VOLTAGE=2.5V

C4300 0.1UF 20% 10V CERM 402

C4301 0.001UF 10% 50V CERM 402

6 GND_CHASSIS_RJ45

C4304 0.001UF 10% 50V CERM 402

CRITICAL
(514-0331)
J4300
RJ45-M51
F-ANG-TH

PRIMARY

13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12

1CT:1CT — 75 OHM (x4)

SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8

RJ45
CABLE SIDE

RJ45
CHIP SIDE

SHIELD 1000PF, 2000V

41 ENET_MDI_P<0>
41 ENET_MDI_N<0>
41 ENET_MDI_P<1>
41 ENET_MDI_N<1>
41 ENET_MDI_P<2>
41 ENET_MDI_N<2>
41 ENET_MDI_P<3>
41 ENET_MDI_N<3>

MARVELL DOES NOT REQUIRE/RECOMMEND ANY SERIES TERMINATIONS HERE

C4305 0.001UF 10% 50V CERM 402

42 41 3 =PP3V3_S3_ENET

R4301 330 5% 1/10W MF-LF 603 — LED4300_1
R4302 330 5% 1/10W MF-LF 603 — LED4301_1
R4303 330 5% 1/10W MF-LF 603 — LED4302_1
R4304 330 5% 1/10W MF-LF 603 — LED4303_1

DEVELOPMENT

LED4300 GREEN-3.6MCD 2.0X1.25MM-SM
LED4301 GREEN-3.6MCD 2.0X1.25MM-SM
LED4302 GREEN-3.6MCD 2.0X1.25MM-SM
LED4303 GREEN-3.6MCD 2.0X1.25MM-SM

41 ENET_LED_ACT_L MAKE_BASE=TRUE
41 ENET_LED_LINK10_100_L MAKE_BASE=TRUE
41 ENET_LED_LINK1000_L MAKE_BASE=TRUE
41 ENET_LED_LINK_L MAKE_BASE=TRUE

# ETHERNET CONNECTOR

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

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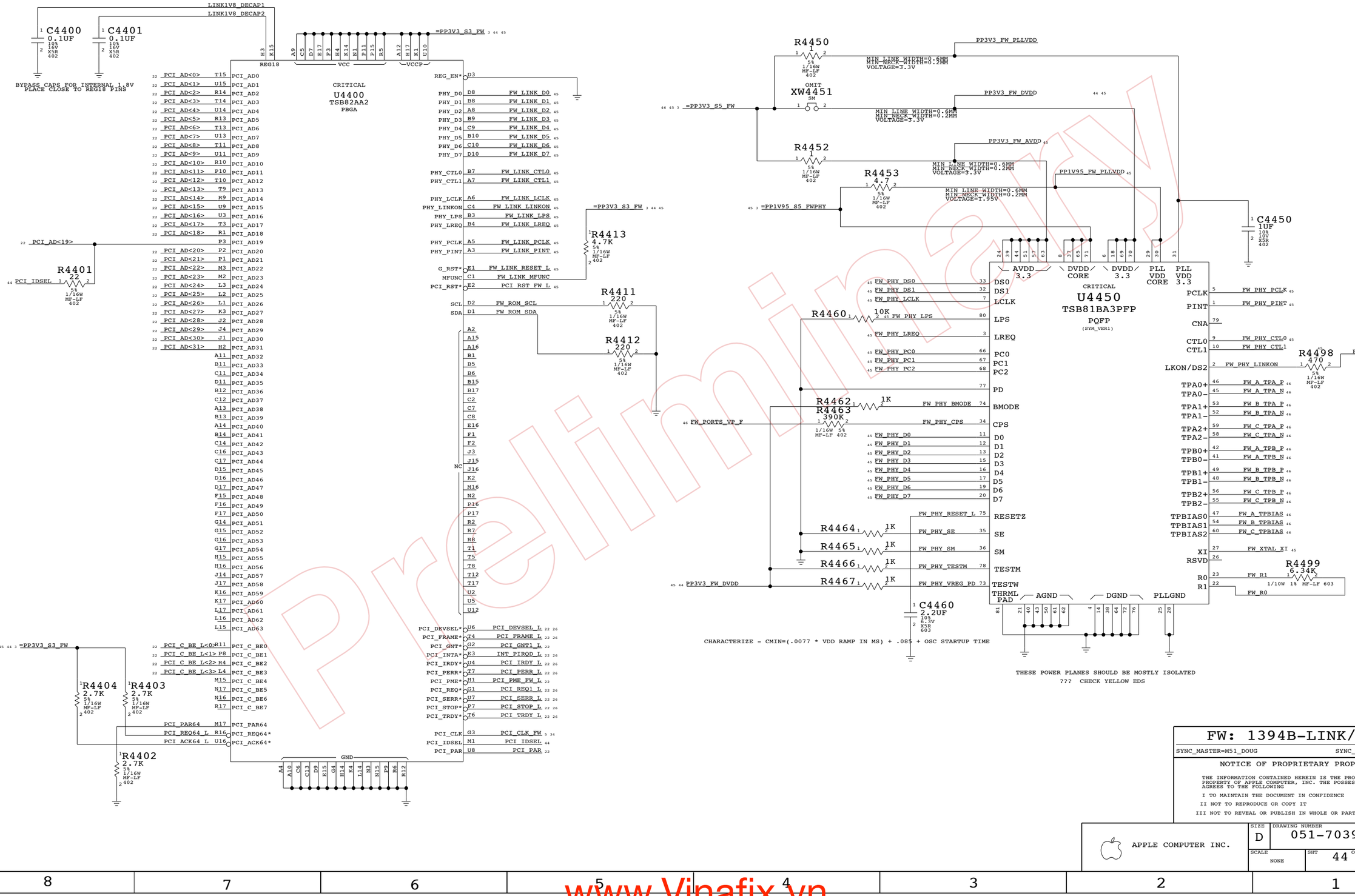
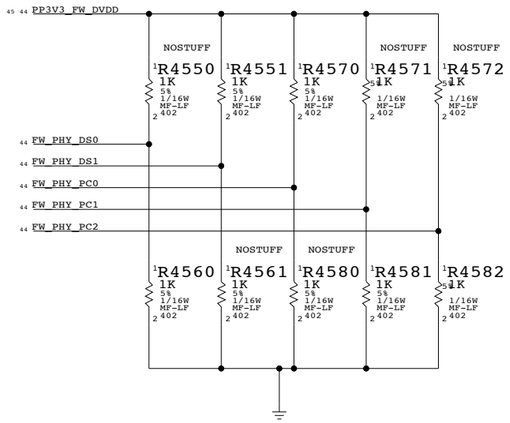
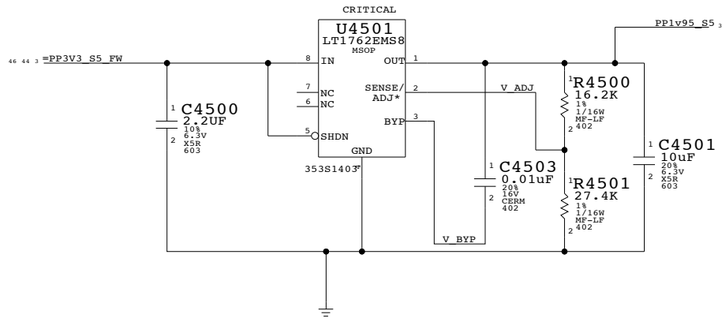
SCALE: NONE SHT 43 OF 97



## 1394 PHY DATA/STROBE AND POWER CLASS OPTIONS



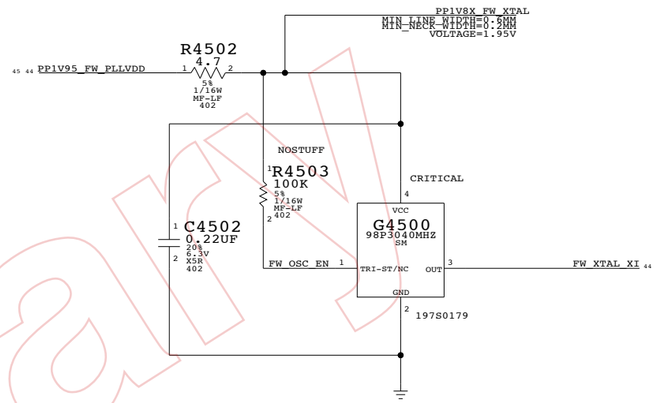

## 1394 PHY 1.95V REGULATOR



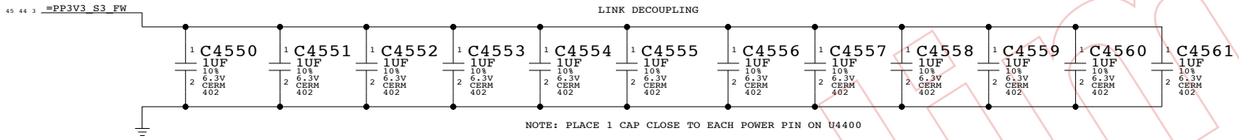

VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V

## 1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION

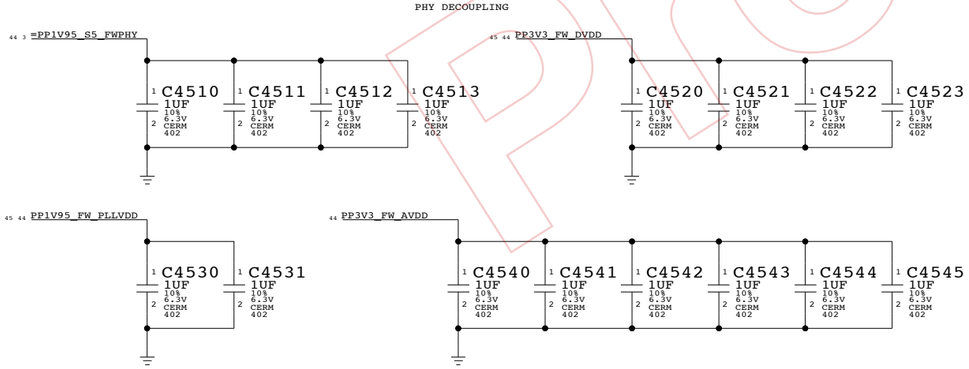



## LINK DECOUPLING



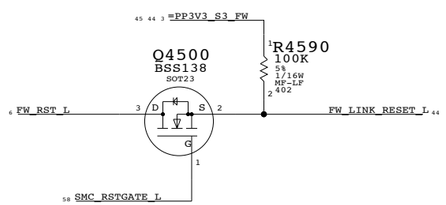

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

## PHY DECOUPLING

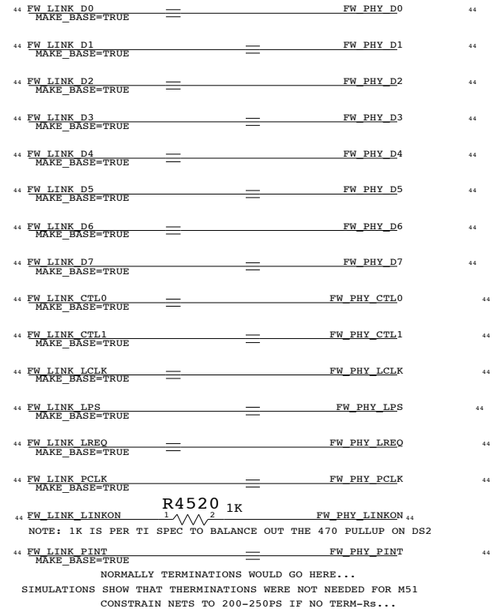



NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

## 1394 LINK POWER ON RESET AND PCI RESET




NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT




NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2
NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

# FW: 1394B MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006



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=PPV_S5_FW

DE4600
MURS320XXG
SMC

FW_PORTS_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

CRITICAL
R4600
2.7
10%
1W
FF-LF
2512

CRITICAL
R4601
2.7
10%
1W
FF-LF
2512

FW_PORTS_VP_R
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

CRITICAL
F4600
0.75AMP-30V
SM

FW_PORTS_VP_F
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

24 VOLTS
15 WATTS MAX

L4600
FERR-250-OHM
SM

SHOULD BE DONE AS A POWER STRIP(SUBPLANE)

FW_PORT0_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

C4600
0.01UF
10%
50V
X7R
603-1

GND_CHASSIS_FIREWIRE

## Termination
Place close to FireWire PHY

VOLTAGE=1.86V
FW_B_TPBIAS
FW_A_TPBIAS
VOLTAGE=1.86V

C4650
1UF
10%
6.3V
CERM
402

C4660
1UF
10%
6.3V
CERM
402

NOTE: TI PHY REQUIRES 1uF EVEN THOUGH SPEC CALLS OUT .33uF

L4650
18nH-15mA
0402

L4651
18nH-15mA
0402

FW_A_TPA_P_RL
NO_TEST=TRUE
VOLTAGE=1.86V

FW_A_TPA_N_RL
NO_TEST=TRUE
VOLTAGE=1.86V

R4650 56.2 1% 1/16W MF-LF 402
R4651 56.2 1% 1/16W MF-LF 402
R4660 56.2 1% 1/16W MF-LF 402
R4661 56.2 1% 1/16W MF-LF 402

FW_A_TPA_P
FW_A_TPA_N
FW_A_TPB_P
FW_A_TPB_N

MAKE_BASE=TRUE

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

FW_B_TPA_P
FW_B_TPA_N
FW_B_TPB_P
FW_B_TPB_N

FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N

R4652 56.2 1% 1/16W MF-LF 402
R4653 56.2 1% 1/16W MF-LF 402
R4662 56.2 1% 1/16W MF-LF 402
R4663 56.2 1% 1/16W MF-LF 402

FW_A_TPB_N_RL
NO_TEST=TRUE
VOLTAGE=0V

FW_A_TPB_P_RL
NO_TEST=TRUE
VOLTAGE=0V

L4652
18nH-15mA
0402

L4653
18nH-15mA
0402

FW_TPA_C0
VOLTAGE=0V

FW_TPA_C1
VOLTAGE=0V

C4654
270PF
5%
25V
CERM
402

R4654
4.99K
1%
1/16W
MF-LF
402

C4664
270PF
5%
25V
CERM
402

R4664
4.99K
1%
1/16W
MF-LF
402

### 3rd TPA/TPB pair unused

FW_C_TPBIAS = NC_FW_C_TPBIAS (MAKE_BASE=TRUE)
FW_C_TPA_P = NC_FW_C_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)
FW_C_TPA_N = NC_FW_C_TPA_N (MAKE_BASE=TRUE)
FW_C_TPB_P =
FW_C_TPB_N =

NOTE: TI RECOMMENDS THIS FOR UNCONNECTED PORTS

### ESD Rail

=PP3V3_S5_FW
R4690
332
1%
1/16W
MF-LF
402

PP3V3_FW_ESD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

L4690
400-OHM-EMI
SM-1

PP3V3_FW_ESD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

CRITICAL
D4690
SOT23
MMBZ5227B

[ LATE VG NOTES ]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

## "Snapback" & "Late VG" Protection

PP3V3_FW_ESD

DP4610 BAV99DW-X-F SOT-363
C4610 0.01UF 10% 50V X7R 402
C4611 0.01UF 10% 50V X7R 402

FW_PORT0_TPB_N
FW_PORT0_TPB_P
FW_PORT0_TPA_N
FW_PORT0_TPA_P

DP4611 BAV99DW-X-F SOT-363
C4612 0.01UF 10% 50V X7R 402
C4613 0.01UF 10% 50V X7R 402

PORT 0
1394B
CRITICAL
J4600
1394B-M51
F-ST-TH

TPB-
TPB<R>
TPB+
VP
NC
VG
TPA-
TPA<R>
TPA+

514-0325

FW_PORT0_TPA_R

NOSTUFF
C4630 0.001UF 10% 50V CERM 402
C4631 0.001UF 10% 50V CERM 402
C4632 0.001UF 10% 50V CERM 402

R4635 1M 1% 1/16W MF-LF 402
C4635 0.1UF 10% 50V X7R 603-1

GND_CHASSIS_FIREWIRE

L4601
FERR-250-OHM
SM

SHOULD BE DONE AS A POWER STRIP(SUBPLANE)

FW_PORT1_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V

C4601
0.01UF
10%
50V
X7R
603-1

GND_CHASSIS_FIREWIRE

PP3V3_FW_ESD

DP4620 BAV99DW-X-F SOT-363
C4620 0.01UF 10% 50V X7R 402
C4621 0.01UF 10% 50V X7R 402

CRITICAL
FL4600
120-OHM
DLW21H-SM1

FW_PORT1_TPA_FL_P
FW_PORT1_TPA_FL_N

CRITICAL
FL4610
120-OHM
DLW21H-SM1

FW_PORT1_TPB_FL_P
FW_PORT1_TPB_FL_N

FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N

PP3V3_FW_ESD

DP4621 BAV99DW-X-F SOT-363
C4622 0.01UF 10% 50V X7R 402
C4623 0.01UF 10% 50V X7R 402

PORT 1
1394A
CRITICAL
J4601
1394A-M51
F-ST-TH

TPO
TPO#
TPI
TPI#
VP
VGND

514-0342

NOSTUFF
C4642 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

"Snapback" & "Late VG" Protection

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 155S0232 | 155S0289 | | FL4600 | ORIGINAL TOKO CHOKE |
| 155S0232 | 155S0289 | | FL4610 | ORIGINAL TOKO CHOKE |

# FIREWIRE CONNECTORS



APPLE COMPUTER INC.

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| D | 051-7039 | 21 |
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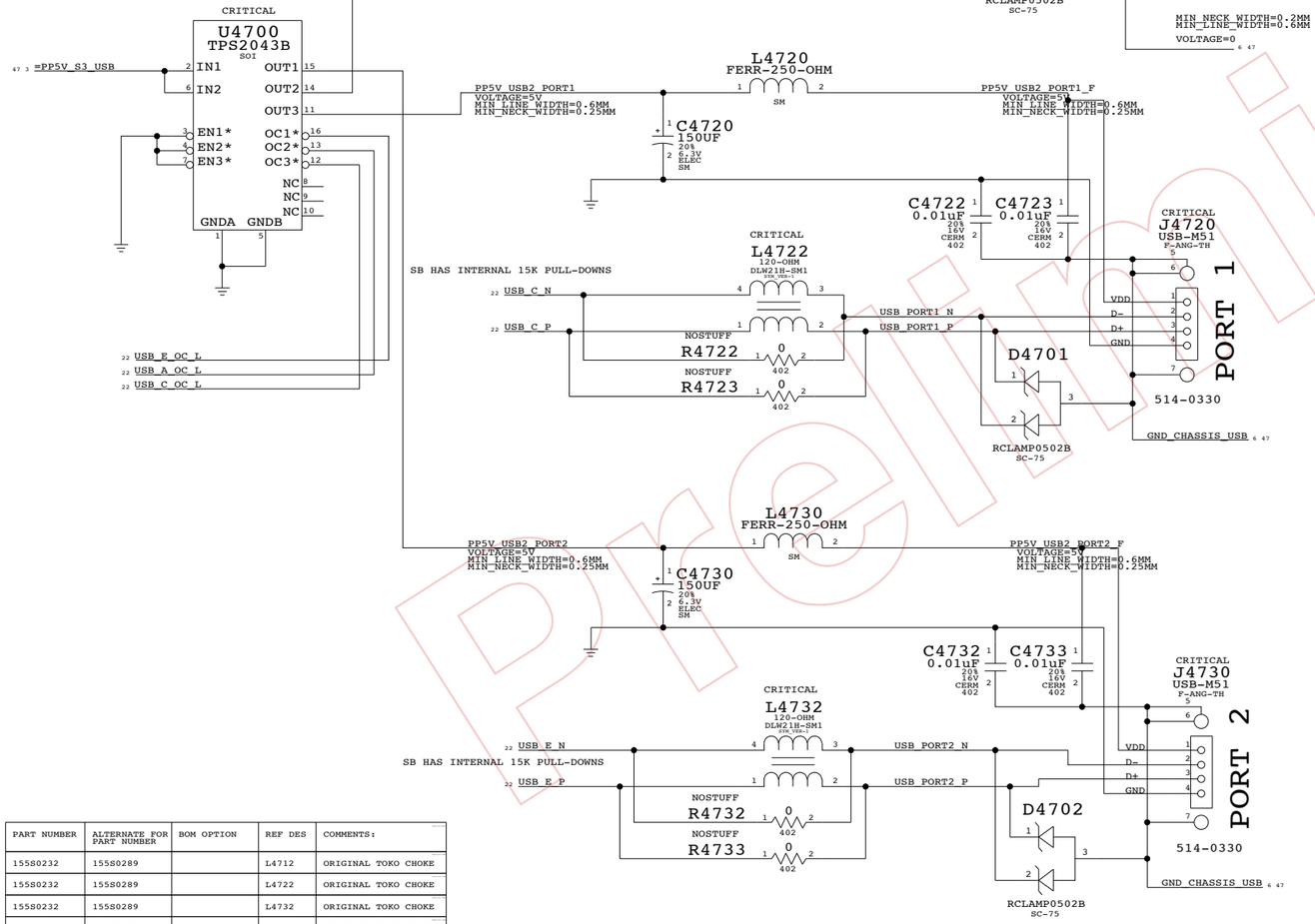
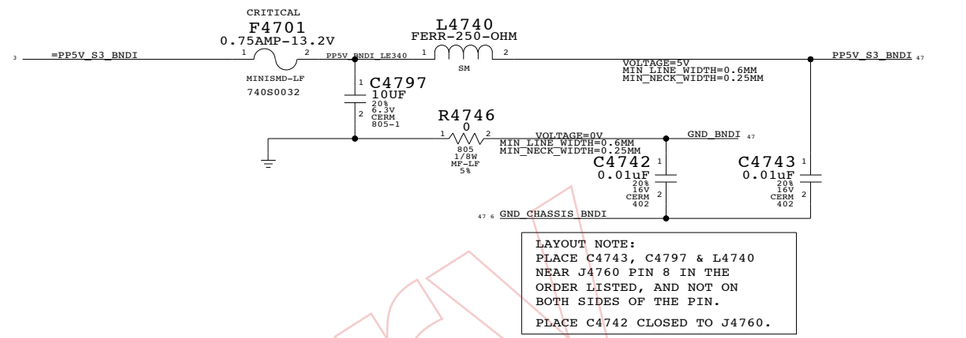
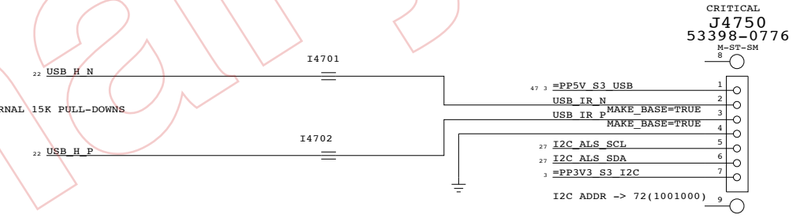
# External USB Ports



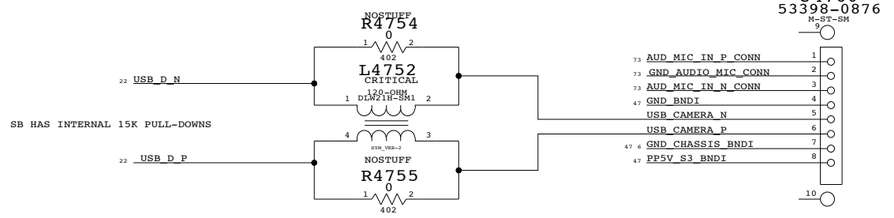

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 155S0232 | 155S0289 | | L4712 | ORIGINAL TOKO CHOKE |
| 155S0232 | 155S0289 | | L4722 | ORIGINAL TOKO CHOKE |
| 155S0232 | 155S0289 | | L4732 | ORIGINAL TOKO CHOKE |
| 155S0232 | 155S0289 | | L4752 | ORIGINAL TOKO CHOKE |



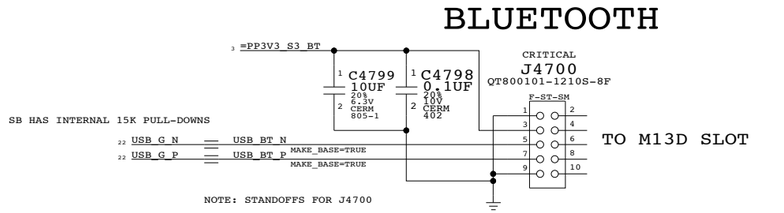

## IR RECEIVER & ALS




## CAMERA & MIC




## BLUETOOTH




# USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006



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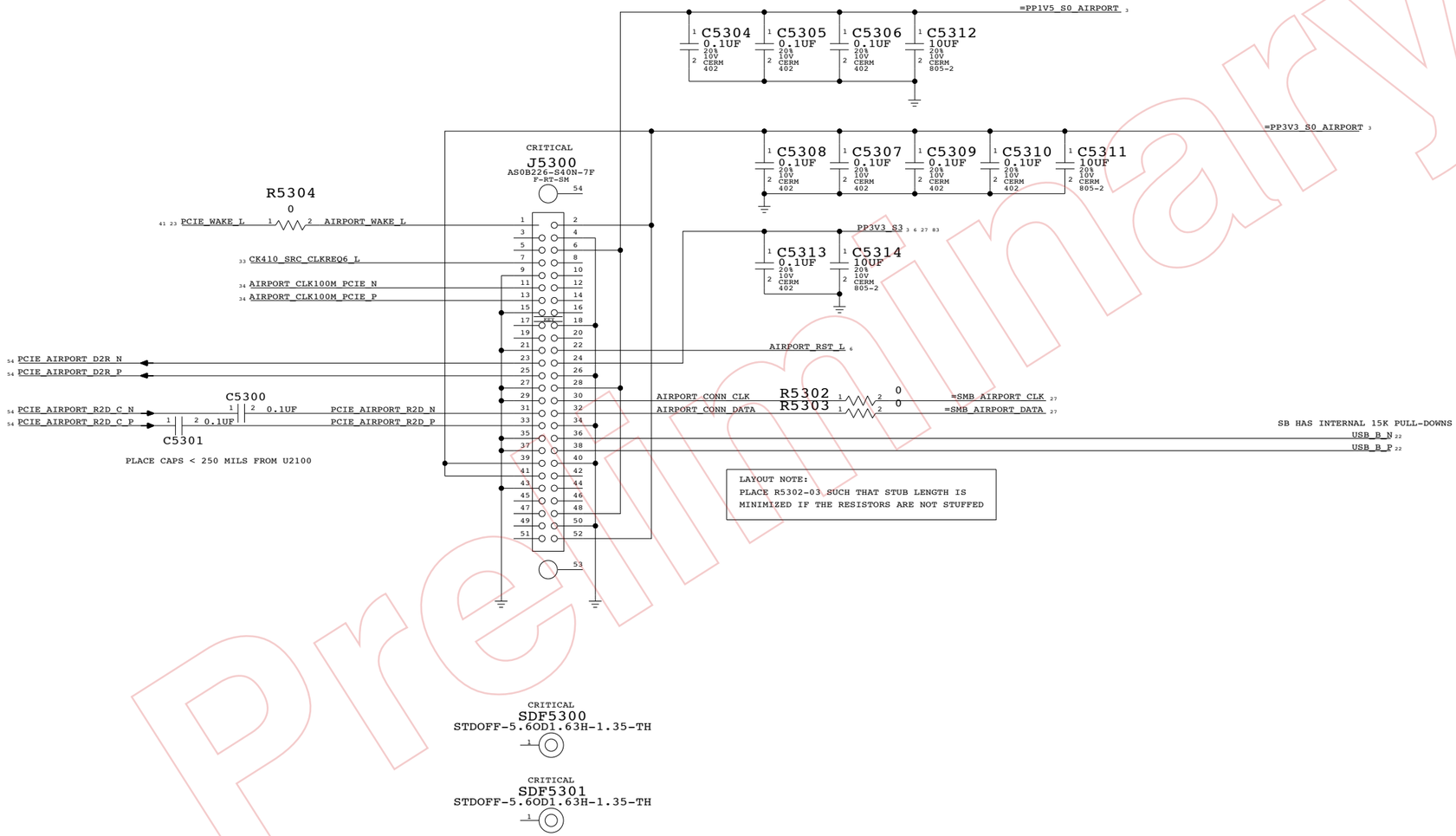


# AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

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## PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

## PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

## PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE



# PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006



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UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PM_LAN_ENABLE | B12 | P10 | P60/KIN0* | L13 | | SMC_PM_G2_EN | |
| SMC_RSTGATE_L | C13 | P11 | P61/KIN1* | L14 | | SMC_ADAPTER_EN | |
| ALL_SYS_PWRGD | A15 | P12 | P62/KIN2* | L15 | | SPI_ARB | |
| RSMRST_PWRGD | B14 | P13 | P63/KIN3* | K12 | | SPI_SCLK | |
| SMC_SB_NMI | B15 | P14 | P64/KIN4* | K13 | | SPI_SI | |
| PM_RSMRST_L | C14 | P15 | P65/KIN5* | K14 | | SPI_SO | |
| IMVP_VR_ON | D12 | P16 | P66/IRQ6*/KIN6* | J12 | | SMC_PROCHOT_3_3_L | |
| PM_PWRBTN_L | C15 | P17 | P67/IRQ7*/KIN7* | J13 | | SMC_CPU_INIT_3_3_L | |
| SMC_P20 | D13 | P20 | P70/AN0 | N12 | | SMC_CPU_ISENSE | |
| SMC_P21 | D14 | P21 | P71/AN1 | R13 | | SMC_CPU_VSENSE | |
| SMC_P22 | D15 | P22 | P72/AN2 | P13 | | SMC_GPU_ISENSE | |
| SMC_P23 | E12 | P23 | P73/AN3 | R14 | | SMC_GPU_VSENSE | |
| SMC_BATT_TRICKLE_EN_L | E14 | P24 | P74/AN4 | P14 | | SMC_DCIN_ISENSE | |
| SMC_BATT_CHG_EN | E15 | P25 | P75/AN5 | R15 | | SMC_PBUS_VSENSE | |
| SMC_P26 | E13 | P26 | P76/AN6 | N13 | | SMC_BATT_ISENSE | |
| SMC_P27 | F14 | P27 | P77/AN7 | P15 | | SMC_FWIRE_ISENSE | |
| LPC_AD<0> | D9 | P30/LAD0 | P80/PME* | C7 | | SMC_WAKE_SCI_L | |
| LPC_AD<1> | C9 | P31/LAD1 | P81/GA20 | A7 | | SMC_TPM_GPIO | |
| LPC_AD<2> | A9 | P32/LAD2 | P82/CLKRUN* | B7 | | PM_CLKRUN_L | |
| LPC_AD<3> | B9 | P33/LAD3 | P83/LPCPD* | D6 | | PM_SUS_STAT_L | |
| LPC_FRAME_L | D8 | P34/LFRAME* | P84/IRQ3*/TXD1 | C6 | | SC_TX_L | |
| SMC_LRESET_L | C8 | P35/LRESET* | P85/IRQ4*/RXD1 | A6 | | SC_RX_L | |
| PCI_CLK_SMC | A8 | P36/LCLK | P86/IRQ5*/SCK1/SCL1 | B6 | | SMB_BSB_CLK | |
| INT_SERIRQ | D7 | P37/SERIRQ | P90/IRQ2* | K4 | | SMC_ONOFF_L | |
| SMC_XDP_TMS | A5 | P40/TMIO | P91/IRQ1* | J2 | | SMC_BC_ACOK | |
| SMC_SYS_LED_16B | B5 | P41/TMO0 | P92/IRQ0* | J1 | | SMC_BS_ALRT_L | |
| SMB_BSB_DATA | D5 | P42/SDA1 | P93/IRQ12* | J3 | | PM_SLP_S3_L | |
| SMC_TPM_PP | C3 | P43/TMI1/EXSCK1 | P94/IRQ13* | J4 | | PM_SLP_S4_L | |
| SMC_XDP_TRST_L | B1 | P44/TMO1 | P95/IRQ14* | H2 | | PM_SLP_S5_L | |
| SMC_XDP_TCK | C2 | P45 | P96/EXCL | H1 | | SMC_SUS_CLK | |
| SMC_SYS_LED | D3 | P46/PWX0/PWM0 | P97/IRQ15*/SDA0 | G2 | | SMB_0_S0_DATA | |
| SMC_SYS_KBDLED | C1 | P47/PWX1/PWM1 | | | | | |
| SMC_TX_L | G1 | P50 | | | | | |
| SMC_RX_L | G4 | P51 | | | | | |
| SMB_0_S0_CLK | F2 | P52/SCL0 | | | | | |

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U5800
SMC_H8S2116
BGA
(2 OF 4)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SMC_RCIN_L | R3 | PA0/KIN8*/PA2DC | PE0 | M3 | | SMC_CASE_OPEN | |
| BOOT_LPC_SPI_L | P3 | PA1/KIN9*/PA2DD | PE1*/ETCK | M2 | | SMC_TCK | |
| PM_SYSRST_L | R2 | PA2/KIN10*/PS2AC | PE2*/ETDI | M1 | | SMC_TDI | |
| SMC_TPM_RESET_L | N3 | PA3/KIN11*/PS2AD | PE3*/ETDO | L4 | | SMC_TDO | |
| PM_EXTTS_L | R1 | PA4/KIN12*/PS2BC | PE4*/ETMS | L2 | | SMC_TMS | |
| PM_THRM_L | N2 | PA5/KIN13*/PS2BD | PF0/IRQ8*/PWM2 | M7 | | SMC_PF0 | |
| SYS_ONEWIRE | M4 | PA6/KIN14*/PS2CC | PF1/IRQ9*/PWM3 | P6 | | SMC_PF1 | |
| PM_BATLOW_L | N1 | PA7/KIN15*/PS2CD | PF2/IRQ10*/TMOY | R6 | | SMC_LID | |
| SMC_EXTSMI_L | B10 | PB0/LSMI* | PF3/IRQ11*/TMOX | N6 | | SMC_CPU_RESET_3_3_L | |
| SMC_RUNTIME_SCI_L | A10 | PB1/LSCI | PF4/PWM4 | M6 | | SMC_BATT_ISET | |
| SMC_ODD_DETECT | D10 | PB2 | PF5/PWM5 | R5 | | SMC_BATT_VSET | |
| ISENSE_CAL_EN | A11 | PB3 | PF6/PWM6 | P5 | | SMC_SYS_ISET | |
| SMC_EXCARD_CP | B11 | PB4 | PF7/PWM7 | N5 | | SMC_SYS_VSET | |
| SMC_EXCARD_PWR_EN | C11 | PB5 | PG0/EXIRQ8*/TMIX | P9 | | SPI_CE_L | |
| SMC_EXCARD_OC_L | A12 | PB6 | PG1/EXIRQ9*/TMIY | R9 | | SMC_XDP_TCK_3_3 | |
| SMC_XDP_TDO_3_3 | D11 | PB7 | PG2/EXIRQ10*/SDA2 | N9 | | SMB_BSA_DATA | |
| SMC_FAN_0_CTL | G14 | PC0/TIOCA0/WUE8* | PG3/EXIRQ11*/SCL2 | P8 | | SMB_BSA_CLK | |
| SMC_FAN_1_CTL | G15 | PC1/TIOCB0/WUE9* | PG4/EXIRQ12*/EXSDAA | R8 | | SMB_A_S3_DATA | |
| SMC_FAN_2_CTL | G13 | PC2/TIOCC0/TCLKA/WUE10* | PG5/EXIRQ13*/EXSCLA | M8 | | SMB_A_S3_CLK | |
| SMC_FAN_3_CTL | G12 | PC3/TIOCD0/TCLKB/WUE11* | PG6/EXIRQ14*/EXSDAB | P7 | | SMB_B_S0_DATA | |
| SMC_FAN_0_TACH | H14 | PC4/TIOCA1/WUE12* | PG7/EXIRQ15*/EXSCLB | R7 | | SMB_B_S0_CLK | |
| SMC_FAN_1_TACH | H15 | PC5/TIOCB1/TCLKC/WUE13* | PH0/EXIRQ6* | E1 | | SMC_PROCHOT | |
| SMC_FAN_2_TACH | H13 | PC6/TIOCA2/WUE14* | PH1/EXIRQ7* | F3 | | SMC_THRMTRIP | |
| SMC_FAN_3_TACH | H12 | PC7/TIOCB2/TCLKD/WUE15* | PH2/FWE | K2 | | SMC_FWE | |
| SMS_X_AXIS | M11 | PD0/AN8 | PH3/EXEXCL | C4 | | ALS_GAIN | |
| SMS_Y_AXIS | P11 | PD1/AN9 | PH4 | D4 | | SMS_INT_L | |
| SMS_Z_AXIS | R11 | PD2/AN10 | PH5 | B3 | | SMS_ONOFF_L | |
| SMC_ANALOG_ID | N11 | PD3/AN11 | | | | | |
| SMC_NB_ISENSE | P10 | PD4/AN12 | | | | | |
| SMC_MEM_ISENSE | R10 | PD5/AN13 | | | | | |
| ALS_LEFT | N10 | PD6/AN14 | | | | | |
| ALS_RIGHT | M10 | PD7/AN15 | | | | | |

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| | | | |
|---|---|---|---|
| G3 | NC0 | NC12 | F15 |
| H3 | NC1 | NC13 | A14 |
| K3 | NC2 | NC14 | C12 |
| L3 | NC3 | NC15 | C10 |
| N4 | NC4 | NC16 | C5 |
| M5 | NC5 | NC17 | A3 |
| N7 | NC6 | NC18 | B8 |
| M12 | NC7 | NC19 | E4 |
| M13 | NC8 | NC20 | H4 |
| L12 | NC9 | NC21 | M9 |
| K15 | NC10 | NC22 | N8 |
| J14 | NC11 | | |

=PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

=PP3V3_S5_SMC
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 10% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
=PP3V3_S5_SMC

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SMC_H8S2116
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SMC_RST_L
SMC_XTAL
SMC_EXTAL

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
KBC_MDE
SMC_MD1
SMC_NMI
SMC_TRST_L

NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

OMIT
XW5800
SM
GND_SMC_AVSS

SMC

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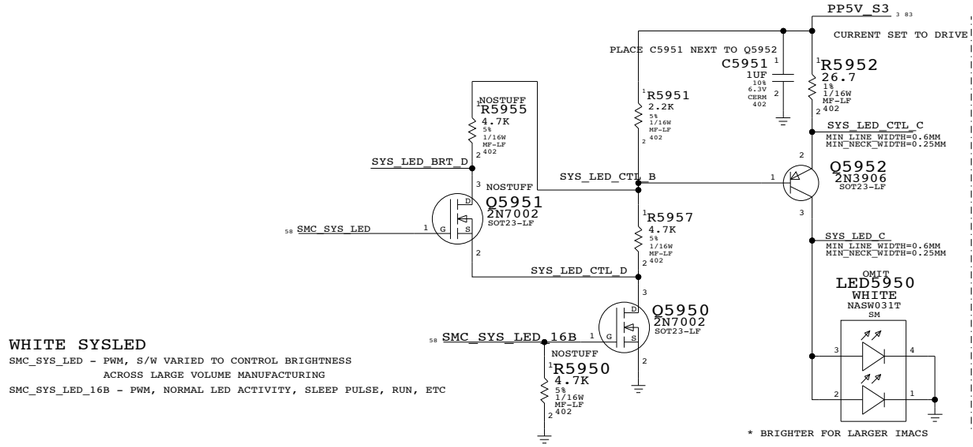
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 58 OF 97 | |

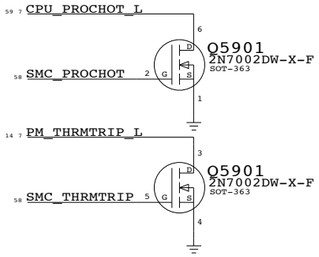



## WHITE SYSLED

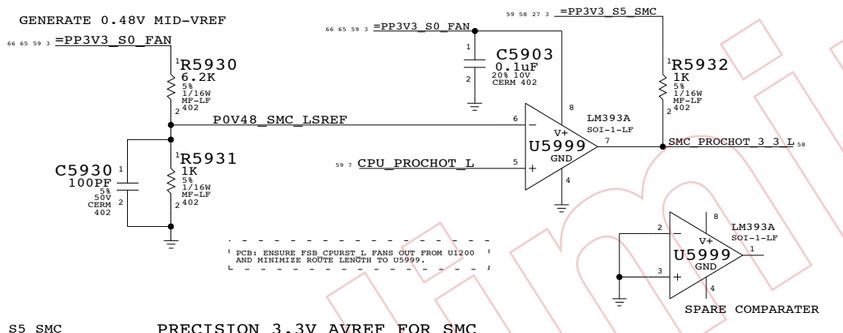
SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS ACROSS LARGE VOLUME MANUFACTURING

SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

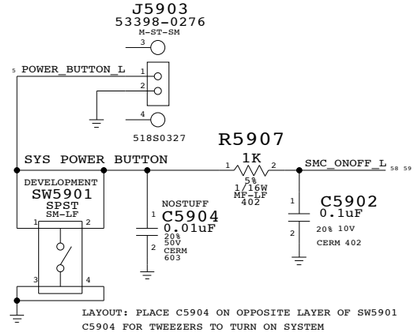
## SMC 3.3V -> CPU 1.05V SHIFTER



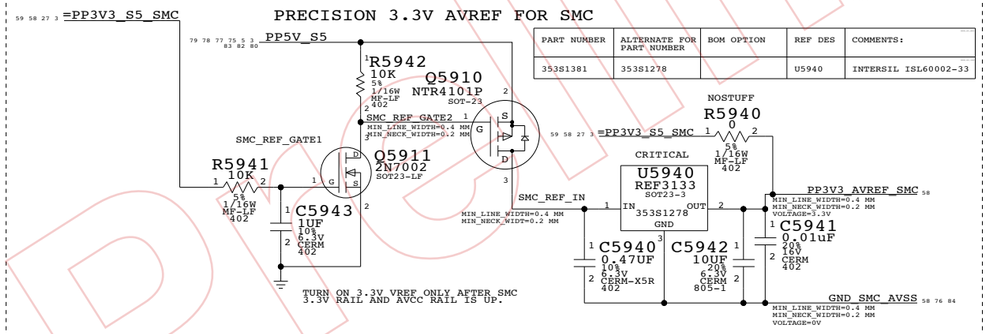

## CPU 1.05V -> SMC 3.3V SHIFTER




## POWER BUTTON HEADER

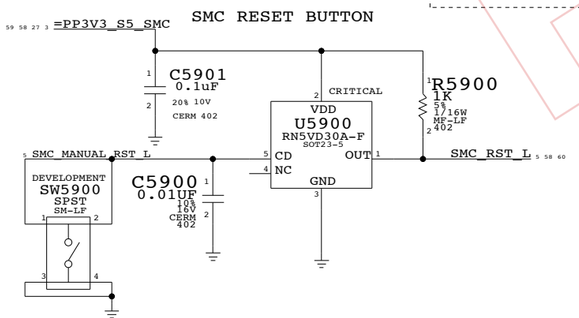



## PRECISION 3.3V AVREF FOR SMC

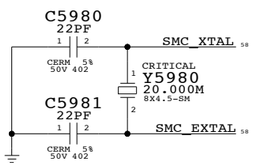



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 353S1381 | 353S1278 | | U5940 | INTERSIL ISL60002-33 |

## SMC RESET BUTTON

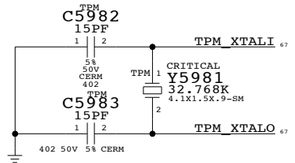



## SMC CRYSTAL




## TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM




## SMC ALIASES, PULLUPS, AND TESTPOINTS

### NO-CONNECT UNUSED PINS

| | | |
|---|---|---|
| SMC_P20 | NC_SMC_P20 | MAKE_BASE=TRUE |
| SMC_P21 | NC_SMC_P21 | MAKE_BASE=TRUE |
| SMC_P22 | NC_SMC_P22 | MAKE_BASE=TRUE |
| SMC_P23 | NC_SMC_P23 | MAKE_BASE=TRUE |
| SMC_P26 | NC_SMC_P26 | MAKE_BASE=TRUE |
| SMC_P27 | NC_SMC_P27 | MAKE_BASE=TRUE |
| SMC_BATT_ISET | NC_SMC_BATT_ISET | MAKE_BASE=TRUE |
| SMC_BATT_VSET | NC_SMC_BATT_VSET | MAKE_BASE=TRUE |
| SMC_SYS_ISET | NC_SMC_SYS_ISET | MAKE_BASE=TRUE |
| SMC_SYS_VSET | NC_SMC_SYS_VSET | MAKE_BASE=TRUE |
| SMC_BATT_TRICKLE_EN_L | NC_SMC_BATT_TRICKLE_EN_L | MAKE_BASE=TRUE |
| SMC_BATT_CHG_EN | NC_SMC_BATT_CHG_EN | MAKE_BASE=TRUE |
| ALS_GAIN | NC_ALS_GAIN | MAKE_BASE=TRUE |

### DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

| | | |
|---|---|---|
| SMC_SYS_KBDLED | TP_SMC_SYS_KBDLED | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| SMC_PF0 | TP_SMC_PF0 | MAKE_BASE=TRUE |
| SMC_PM_G2_EN | TP_SMC_PM_G2_EN | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| SMC_ADAPTER_EN | TP_SMC_ADAPTER_EN | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| ALS_LEFT | TP_ALS_LEFT | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| ALS_RIGHT | TP_ALS_RIGHT | MAKE_BASE=TRUE |
| SMC_PF1 | TP_SMC_PF1 | MAKE_BASE=TRUE |
| SMC_XDP_TCK | TP_SMC_XDP_TCK | MAKE_BASE=TRUE |
| SMC_XDP_TRST_L | TP_SMC_XDP_TRST_L | MAKE_BASE=TRUE |
| SMC_PB7 | TP_SMC_PB7 | MAKE_BASE=TRUE; FUNC_TEST=TRUE |

### NC OR PULLDOWN UNUSED ANALOG SENSE PINS

| | | |
|---|---|---|
| SMS_X_AXIS | NC_SMS_X_AXIS | MAKE_BASE=TRUE |
| SMS_Y_AXIS | NC_SMS_Y_AXIS | MAKE_BASE=TRUE |
| SMS_Z_AXIS | NC_SMS_Z_AXIS | MAKE_BASE=TRUE |
| SMC_NB_ISENSE | NC_SMC_NB_ISENSE | MAKE_BASE=TRUE |
| SMC_MEM_ISENSE | NC_SMC_MEM_ISENSE | MAKE_BASE=TRUE |
| SMC_FWIRE_ISENSE | UNUSED_SMC_SENSE | MAKE_BASE=TRUE |
| SMC_BATT_ISENSE | UNUSED_SMC_SENSE | MAKE_BASE=TRUE |

UNUSED_SMC_SENSE — R5924 10K 5% 1/16W MF-LF

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

| | | |
|---|---|---|
| SMC_EXCARD_PWR_EN | TP_SMC_EXCARD_PWR_EN | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| SMC_PB7 | TP_SMC_PB7 | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| SMC_FAN_3_TACH | TP_SMC_FAN_3_TACH | MAKE_BASE=TRUE; FUNC_TEST=TRUE |
| SMC_FAN_3_CTL | TP_SMC_FAN_3_CTL | MAKE_BASE=TRUE; FUNC_TEST=TRUE |

### SMC PULL-UPS & PULL-DOWNS

=PP3V3_S5_SMC — 5% 1/16W MF-LF 402

| | | |
|---|---|---|
| SMC_ONOFF_L | R5808 | 10K |
| SMC_ODD_DETECT | R5829 | 10K |
| SC_RX_L | R5832 | 10K |
| SC_TX_L | R5833 | 10K |
| SMS_ONOFF_L | R5815 | 10K |
| SMC_TX_L | R5817 | 10K |
| SMC_RX_L | R5818 | 100K |
| SYS_ONEWIRE | R5819 | 10K |
| SMC_BS_ALRT_L | R5821 | 10K |
| SMC_TMS | R5822 | 10K |
| SMC_TDO | R5823 | 10K |
| SMC_TDI | R5824 | 10K |
| SMC_TCK | R5825 | 10K |
| SMC_BC_ACOK | R5826 | 10K |
| SMC_FWE | R5828 | 10K |
| SMC_LID | R5916 | 10K |
| SMC_EXCARD_OC_L | R5831 | 10K |
| SMC_XDP_TCK_3_3 | R5934 | 1K |
| SMC_CPU_RESET_3_3_L | R5933 | 1K |
| SMC_EXCARD_CP | R5830 | 10K |
| SMC_CASE_OPEN | R5917 | 10K |

TPM_RESET_PULLUP: SMC_TPM_RESET_L — R5827 10K — PP3V3_TPM_3VSB

WIRE-OR_DIMM_OVERTEMP_TO_SMC: DIMM_OVERTEMP_L — PM_EXTTS_L

WIRE SMC TO SB PINS

| | | |
|---|---|---|
| SMC_CPU_INIT_3_3_L | FWH_INIT_L | MAKE_BASE=TRUE |
| SMC_SUS_CLK | SUS_CLK_SB | MAKE_BASE=TRUE |
| SC_RX_L — R5922 0 — | SMC_RX_L | |
| SC_TX_L — R5923 0 — | SMC_TX_L | |

### POWER SUPPLY TEMP SENSE

SMC_ANALOG_ID — ACDC_TEMP (MAKE_BASE=TRUE)

### SELECT TPM GPIO

SMC_TPM_GPIO — SMC_TPM_GPIO1 R5920 0 TPM_GPIO1; SMC_TPM_GPIO2 R5921 0 TPM_GPIO2 — 5% 1/16W MF-LF 402

### HDD ACTIVITY MONITOR

PP5V_S0

SMC_TPM_PP — R5995 0 5% 1/16W MF-LF 402 — TPM_PP

M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING

TP_SB_SATALED_L — PU_HDD_ACTIVITY_LED — R5960 10K (MAKE_BASE=TRUE)

### TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM — GND_NEXT_TO_SMC — OMIT

### M51 SPECIFIC: GPU MONITORING SIGNALS

| | | |
|---|---|---|
| I327 SMC_XDP_TMS | | MXM_AC_BATT_L |
| I328 SMC_XDP_TDO_3_3 | | GPU_OVERTEMP_L |

## SMC & TPM SUPPORT

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



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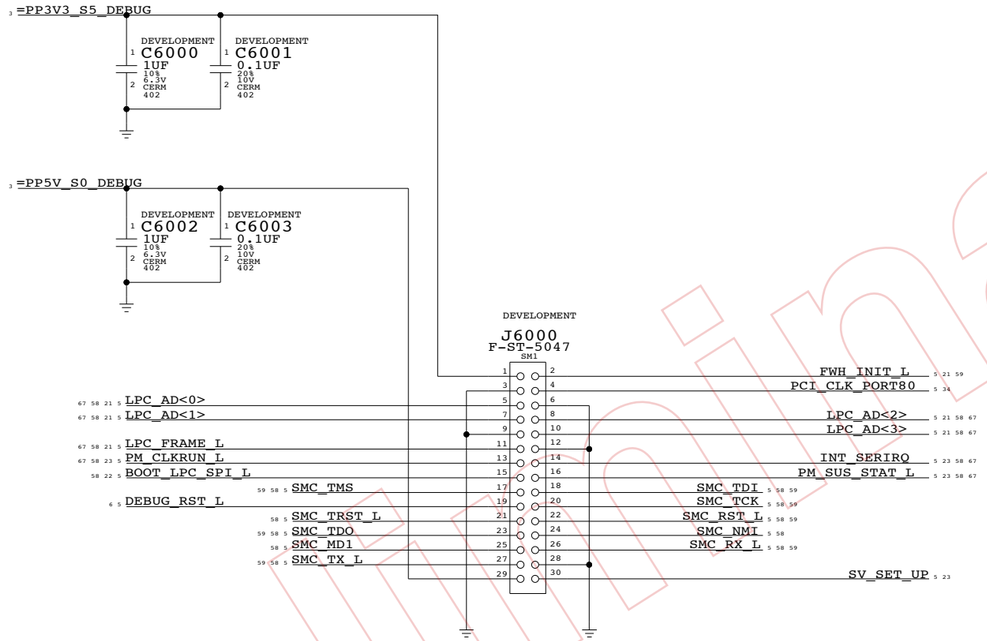
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 59 OF 97 | |






# LPC+ CONN

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
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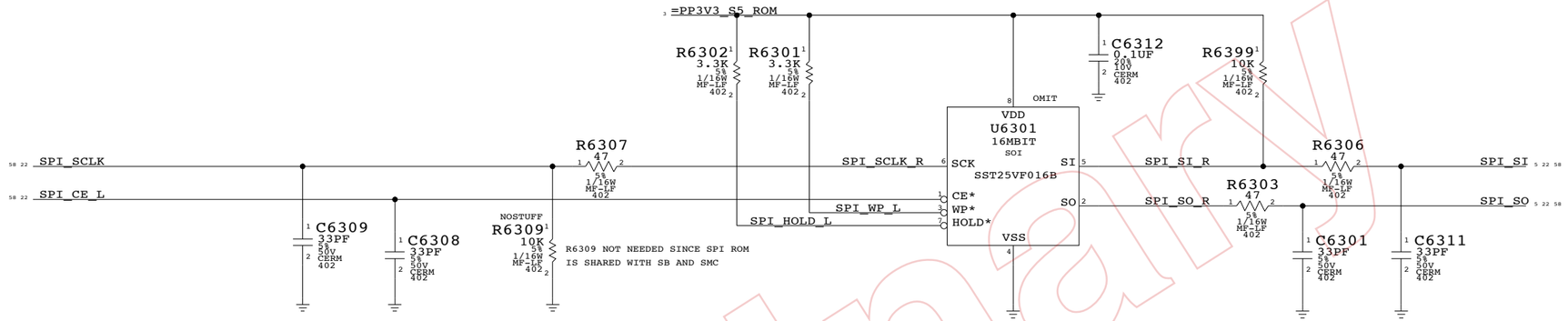



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301



# SPI BOOTROM

SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006



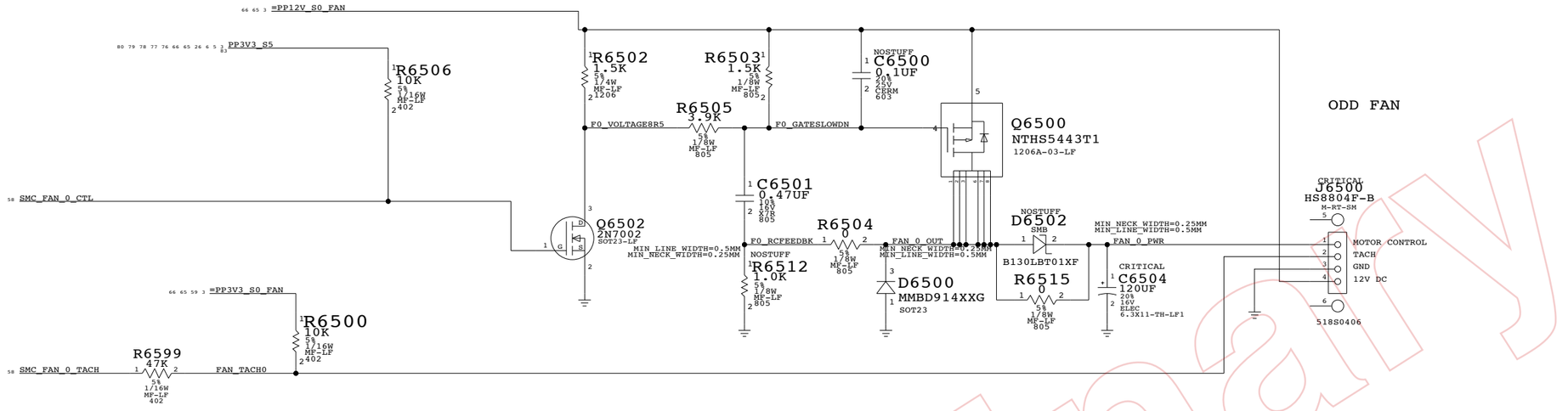
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE

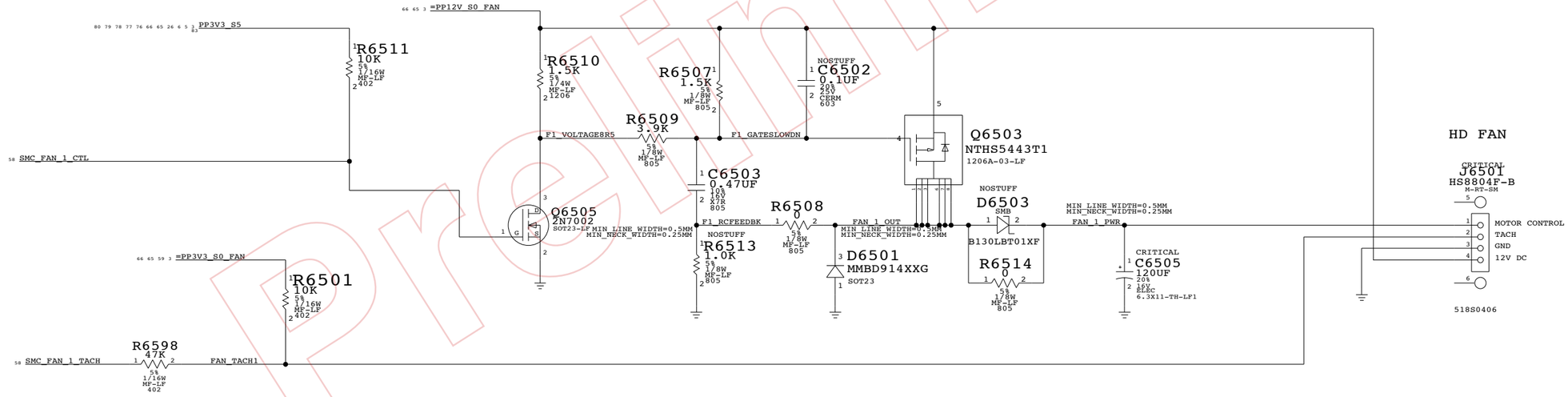
SHT 63 OF 97

# FAN 0




NOTE: ADDED TO PROTECT SMC

# FAN 1




## HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

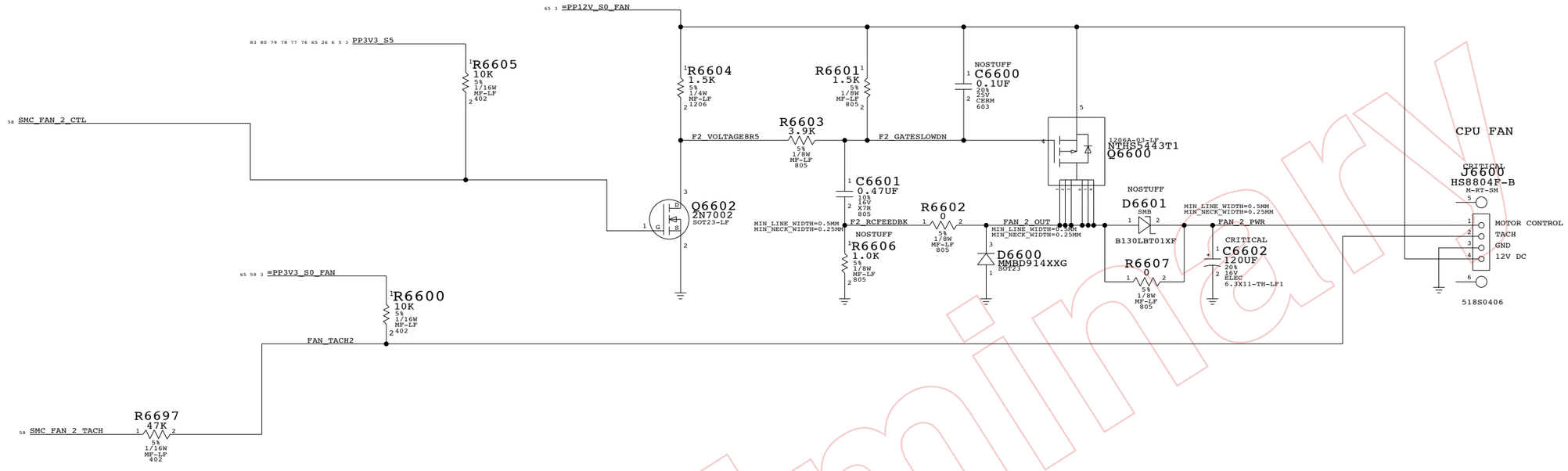


APPLE COMPUTER INC.

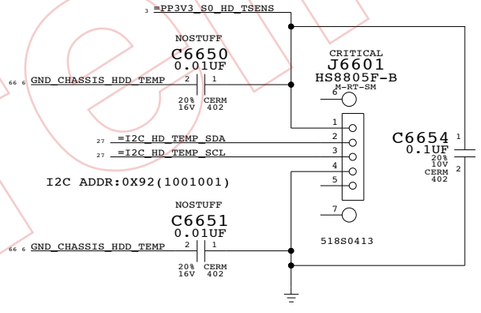
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 65 OF 97

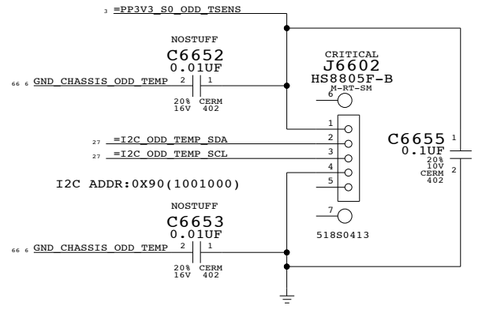
# FAN 2




## HD TEMP SENSOR




## ODD TEMP SENSOR






## CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006



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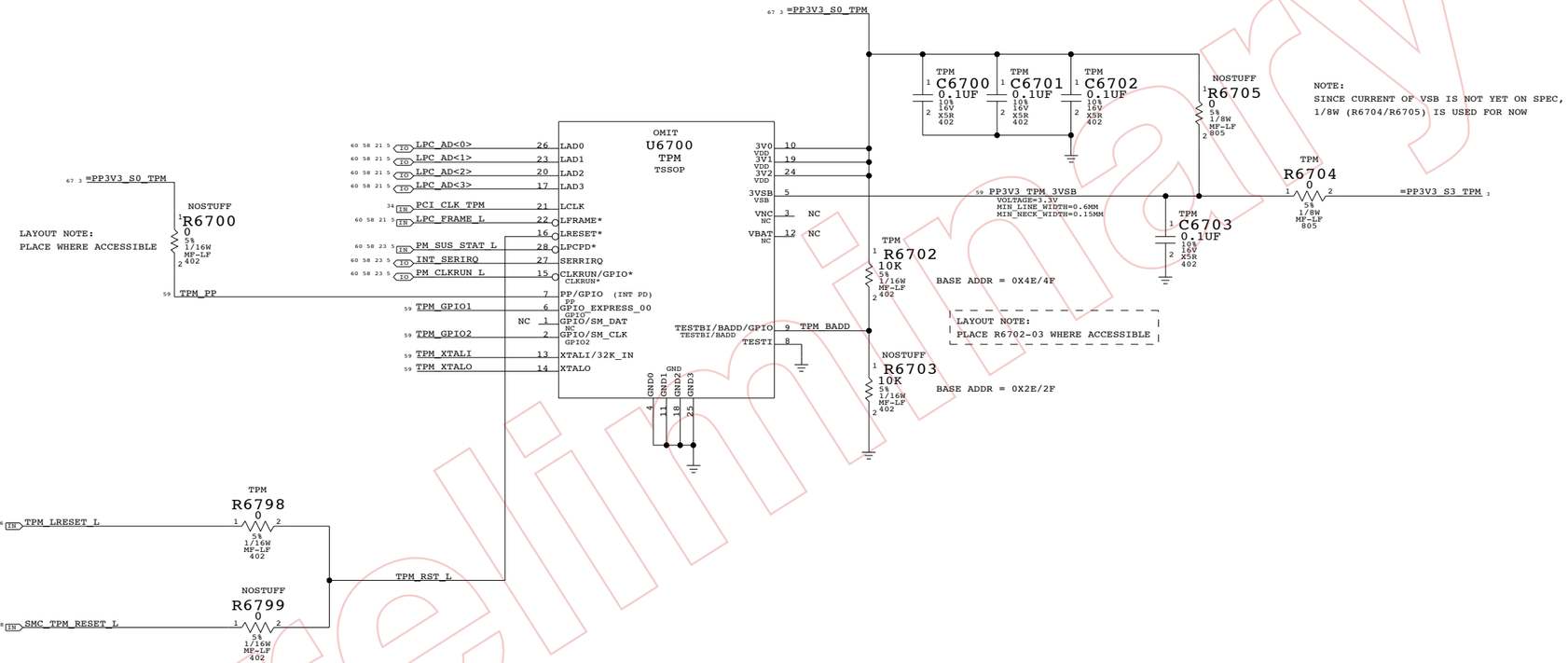
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 66 OF 97 | |






# TPM

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

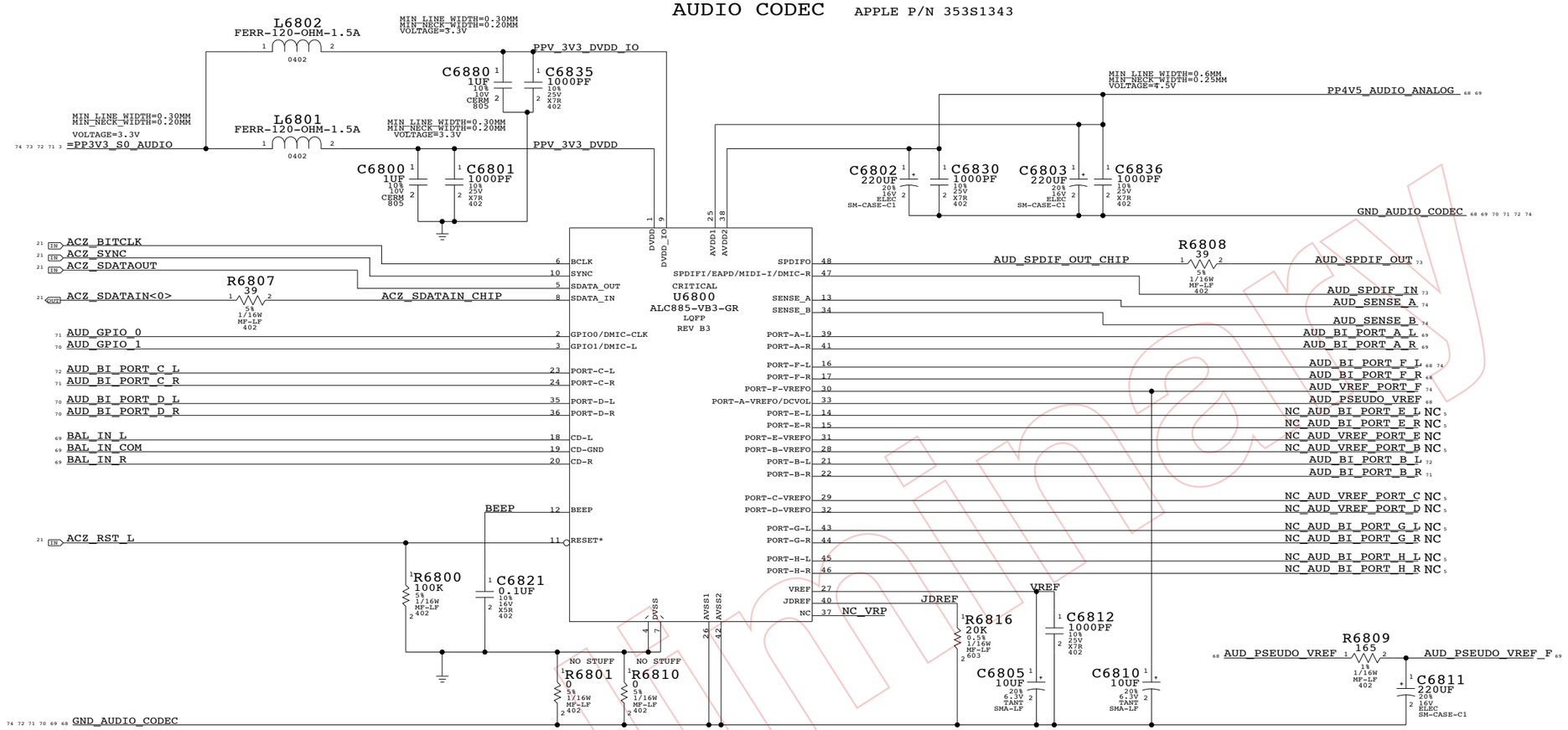


APPLE COMPUTER INC.

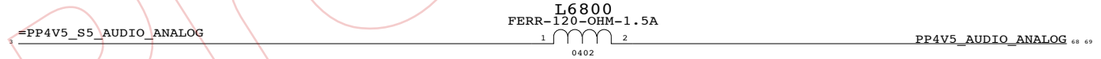
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 67 OF 97 | |

# AUDIO CODEC

APPLE P/N 353S1343




## 4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP




## MIC INPUT TO BOTH L&R

AUD_BI_PORT_F_L — AUD_BI_PORT_F_R



## AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006



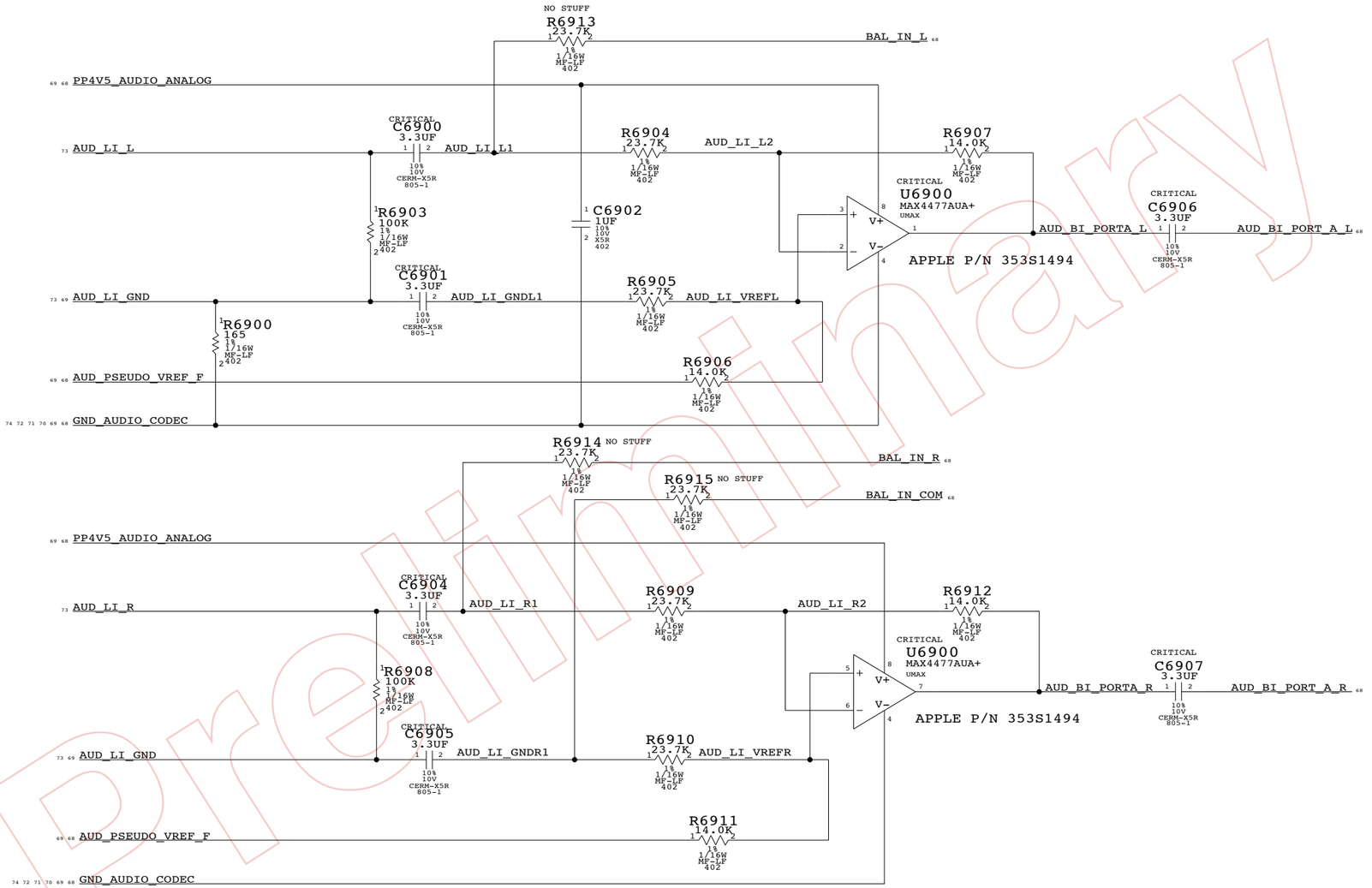
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE SHT 68 OF 97

# LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59






## AUDIO: LINE INPUT AMP



APPLE COMPUTER INC.

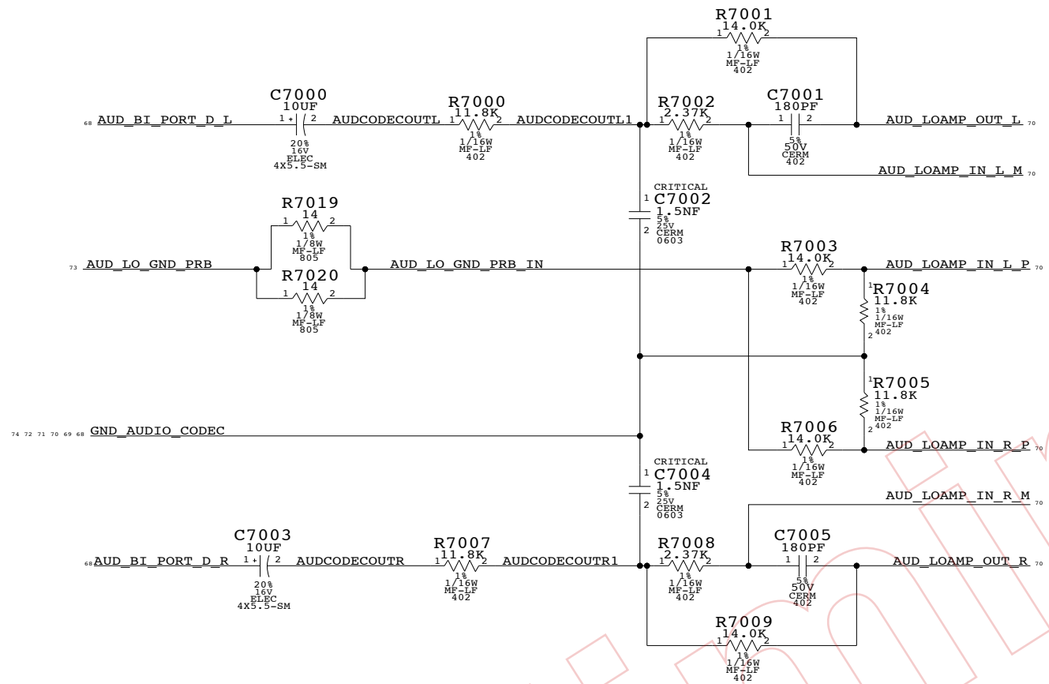
| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE: NONE

SHT 69 OF 97

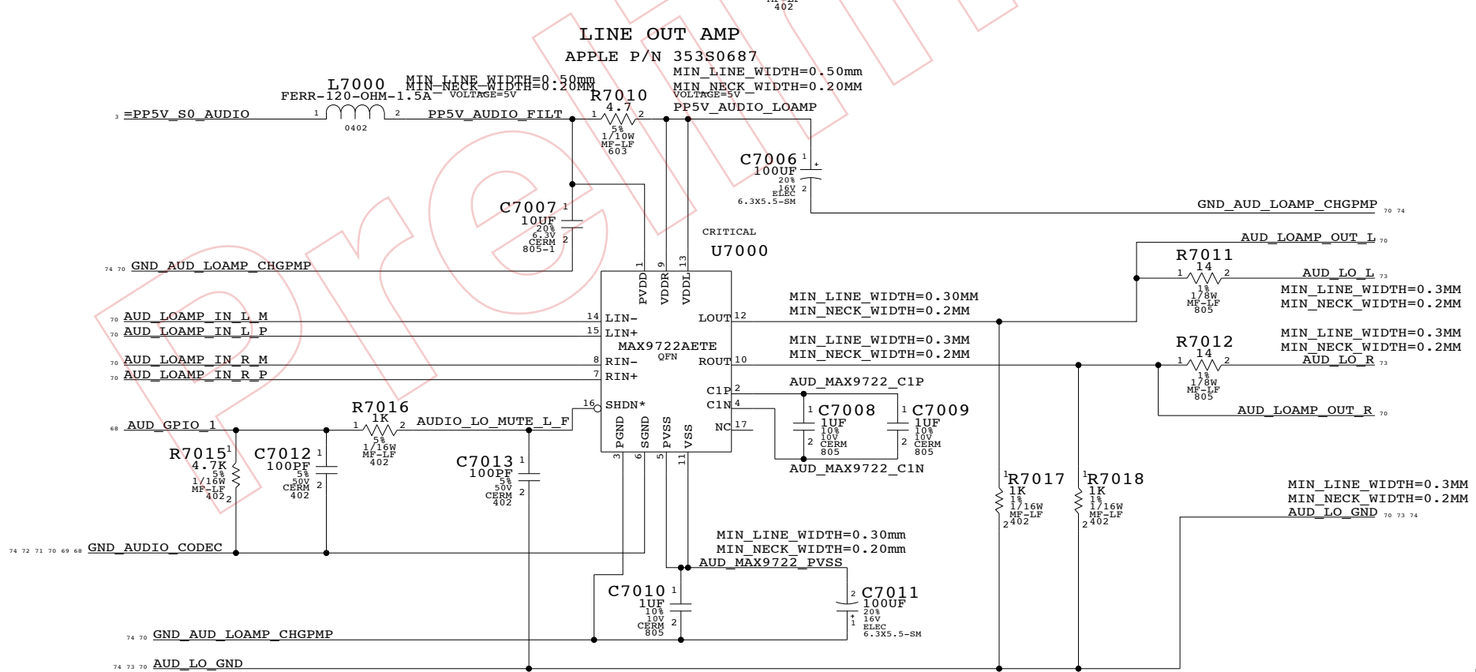
## LINE OUT LOW-PASS FILTER

Fc = 37 KHZ, Av = -1.18




## LINE OUT AMP

APPLE P/N 353S0687




## AUDIO: COMBO OUT AMP



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 70 OF 97 | |

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

# SPEAKER AMP
APPLE P/N 353S1156

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
PP12V_AUD_SPKRAMP_PLANE

L7122 FERR-250-OHM SM-1
L7100 FERR-250-OHM SM-1
R7170 0.005 1% 1/4W MF-LF 1206
=PP12V_S5_AUDIO_SPKRAMP
12V_S5_SPKRAMP
C7117 470UF 20% 25V ELEC 10X10-SM
C7100 470UF 20% 25V ELEC 10X10-SM
C7101 10UF 10% 16V CERM 1210
C7118 0.1UF 20% 16V CERM 603
GND_AUDIO_SPKRAMP_PLANE

C7102 1UF 10% 35V X7R 805
C7119 0.1UF 20% 16V CERM 603
C7103 10UF 10% 16V CERM 1210
GND_AUDIO_SPKRAMP_PLANE

L7105 1000-OHM-200MA 0603
AUD_BI_PORT_C_R
AUDSAMPINLN
C7104 0.47UF 10% 16V X7R 805
C7115 100PF 5% 50V CERM 402
L7106 1000-OHM-200MA 0603
AUDSAMPINLP
C7105 0.47UF 10% 16V X7R 805
GND_AUDIO_CODEC
L7107 1000-OHM-200MA 0603
AUDSAMPINRP
C7106 0.47UF 10% 16V X7R 805
C7116 100PF 5% 50V CERM 402
L7108 1000-OHM-200MA 0603
AUD_BI_PORT_B_R
AUDSAMPINRN
C7107 0.47UF 10% 16V X7R 805

R7114 47K 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO
AUD_SAMP_SHDN_L
AUD_SPKRAMP_MUTE
R7115 47K 5% 1/16W MF-LF 402
=PP3V3_S0_AUDIO

R7113 47K 5% 1/16W MF-LF 402
AUD_GPIO_0
AUD_SPKRAMP_MUTE_L
Q7100 2N7002DW-X-F SOT-363
R7112 4.7K 5% 1/16W MF-LF 402
C7120 100PF 5% 50V CERM 402
C7121 100PF 5% 50V CERM 402
GND_AUDIO_CODEC
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
SPKRAMP_SS
Q7100 2N7002DW-X-F SOT-363
C7190 100PF 5% 50V CERM 402
C7114 1UF 10% 25V X5R 603
C7109 0.47UF 10% 16V X7R 805

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD

CRITICAL
U7100
MAX9714
QFN-LF

VDD
CHOLD
INL- INL+ INR+ INR-
AUD_SAMP_INL_N
AUD_SAMP_INL_P
AUD_SAMP_INR_P
AUD_SAMP_INR_N
AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2
SHDN*
NC
REG
AUD_MAX9714_VREG
AGND PAD
PGND
SS
OUTL+ OUTL+ OUTL- OUTL-
OUTR+ OUTR+ OUTR- OUTR-
C1+ C1-

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP
AUDSAMPCPN
C7108 0.1UF 10% 50V X7R 603-1

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPOURTP
AUDSAMPOUTRN

L7101 180-OHM-1.5A 0603-LF
L7102 180-OHM-1.5A 0603-LF
L7103 180-OHM-1.5A 0603-LF
L7104 180-OHM-1.5A 0603-LF
AUD_SPKR_OUTCR_P
AUD_SPKR_OUTCR_N
AUD_SPKR_OUTBR_P
AUD_SPKR_OUTBR_N

C7110 1000PF 10% 25V X7R 402
C7111 1000PF 10% 25V X7R 402
C7112 1000PF 10% 25V X7R 402
C7113 1000PF 10% 25V X7R 402

XW7102 SM OMIT
XW7101 SM OMIT
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP_PLANE

NOSTUFF
R7119 0 5% 1/16W MF-LF 402

## GAIN SETTINGS: +16DB
## MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO
RP7100 47K 5% 1/16W SM-LF
AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1
NOSTUFF R7118 0 5% 1/16W MF-LF 402
NOSTUFF R7108 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP_PLANE



AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE NONE SHT 71 OF 97

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

# SPEAKER AMP
APPLE P/N 353S1156

=PP12V_S5_AUDIO_SPKRAMP
R7270 0.005 1% 1/4W MF-LF 1206
12V_S5_SPKRAMP1
L7222 FERR-250-OHM SM-1
L7200 FERR-250-OHM SM-1
PP12V_AUD_SPKRAMP1_PLANE
C7217 470UF 20% 25V ELEC 10X10-SM
C7200 470UF 20% 25V ELEC 10X10-SM
C7201 10UF 10% 16V CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 35V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V CERM 1210
GND_AUDIO_SPKRAMP1_PLANE

AUD_BI_PORT_C_L
L7205 1000-OHM-200MA 0603
C7204 0.47UF 10% 16V X7R 805
C7215 100PF 5% 50V CERM 402
AUDSAMPINLN1
AUD_SAMP1_INL_N

GND_AUDIO_CODEC

L7206 1000-OHM-200MA 0603
C7205 0.47UF 10% 16V X7R 805
AUDSAMPINLP1
AUD_SAMP1_INL_P

L7207 1000-OHM-200MA 0603
C7206 0.47UF 10% 16V X7R 805
C7216 100PF 5% 50V CERM 402
AUDSAMPINRP1
AUD_SAMP1_INR_P

AUD_BI_PORT_B_L
L7208 1000-OHM-200MA 0603
C7207 0.47UF 10% 16V X7R 805
AUDSAMPINRN1
AUD_SAMP1_INR_N

=PP3V3_S0_AUDIO
R7214 47K 5% 1/16W MF-LF 402
C7290 100PF 5% 50V CERM 402
GND_AUDIO_SPKRAMP1_PLANE

SPKRAMP1_SS
AUD_SPKRAMP_MUTE
Q7200 2N7002 SOT23-LF
GND_AUDIO_SPKRAMP1_PLANE

GND_AUDIO_CODEC

C7214 1UF 10% 25V X5R 603
C7209 0.47UF 10% 16V X7R 805

CRITICAL
U7200 MAX9714 QFN-LF
VDD
CHOLD
INL-
INL+
INR+
INR-
G1
G2
FS1
FS2
SHDN*
NC
REG
THM
AGND PAD
PGND
SS
OUTL+
OUTL-
C1+
C1-
OUTR+
OUTR-
AUD_SAMP1_G1
AUD_SAMP1_G2
AUD_SAMP1_FS1
AUD_SAMP1_FS2
AUD_SAMP1_SHDN_L
AUD_MAX9714_VREG1
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM
AUD_MAX9714_CHOLD1
AUDSAMPOUTLP1
AUDSAMPOUTLN1
AUDSAMPCPP1
AUDSAMPCPN1
C7208 0.1UF 10% 50V X7R 603-1
AUDSAMPOURTP1
AUDSAMPOUTRN1
NOSTUFF R7219 0 5% 1/16W MF-LF 402

L7201 180-OHM-1.5A 0603-LF
L7202 180-OHM-1.5A 0603-LF
L7203 180-OHM-1.5A 0603-LF
L7204 180-OHM-1.5A 0603-LF
AUD_SPKR_OUTCL_P
AUD_SPKR_OUTCL_N
AUD_SPKR_OUTBL_P
AUD_SPKR_OUTBL_N

C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402

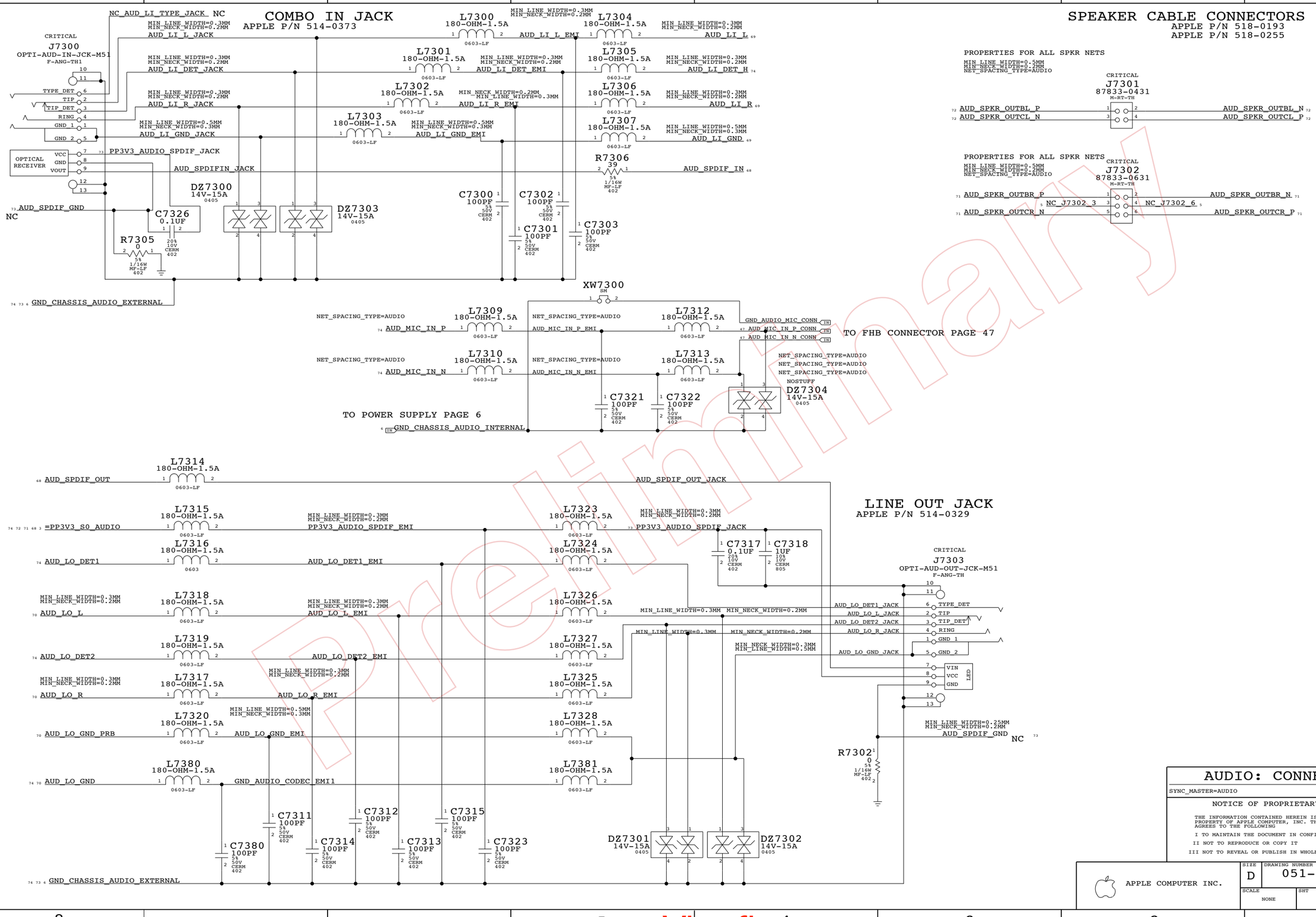
XW7202 SM OMIT
XW7201 SM OMIT
GND_AUDIO_SPKRAMP

GND_AUDIO_SPKRAMP1_PLANE

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO
RP7200 47K 5% 1/16W SM-LF
AUD_SAMP1_FS2
AUD_SAMP1_FS1
AUD_SAMP1_G2
AUD_SAMP1_G1
NOSTUFF R7218 0 5% 1/16W MF-LF 402
NOSTUFF R7208 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP1_PLANE

| AUDIO: SPEAKER AMP | | |
|---|---|---|
| SYNC_MASTER=AUDIO | SYNC_DATE=06/29/2006 | |
| NOTICE OF PROPRIETARY PROPERTY | | |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING<br>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE<br>II NOT TO REPRODUCE OR COPY IT<br>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART | | |
| APPLE COMPUTER INC. | SIZE D / DRAWING NUMBER 051-7039 / REV. 21 | |
| | SCALE NONE / SHT 72 OF 97 | |



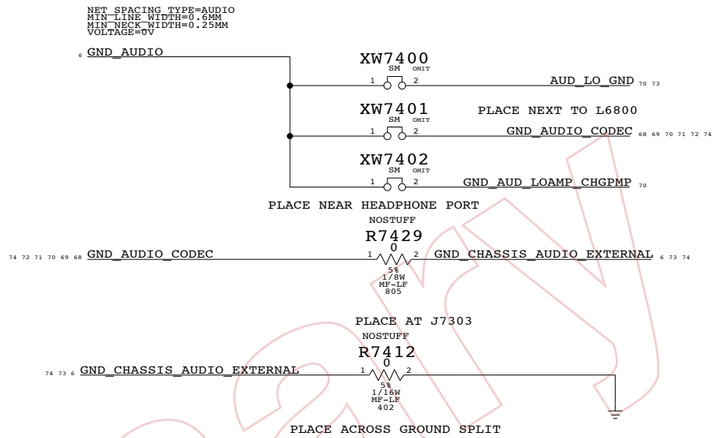
## CODEC OUTPUT SIGNAL PATHS

| FUNCTION | VOLUME | DAC | PIN COMPLEX | MUTE CONTROL |
|---|---|---|---|---|
| LINE OUT | 0X0C | 0X02 | 0X14(D) | GPIO 1 |
| SPKR AMP | 0X0D | 0X03 | 0X18(B) | GPIO 0 |
| SPKR AMP1 | 0X0F | 0X05 | 0X1A(C) | GPIO 0 |
| SPDIFOUT | | CONVERTER=0X06 | PIN=0X1E | |
| | | DETECT DELEGATE PIN 0X16H | | |

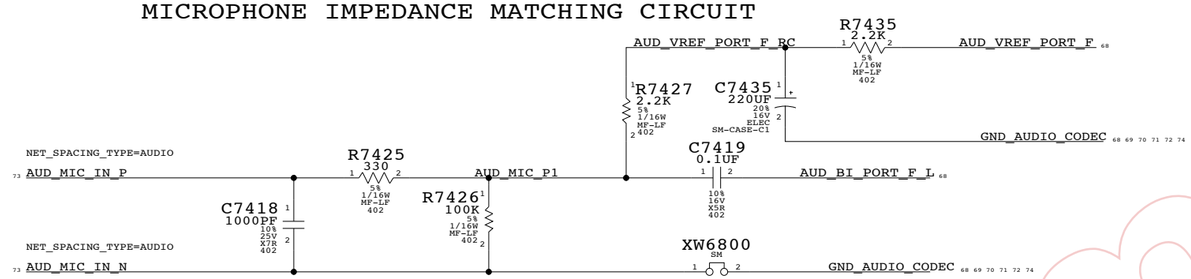
## CODEC INPUT SIGNAL PATHS

| FUNCTION | ADC | MIXER | PORT | VREF |
|---|---|---|---|---|
| MIC INPUT | 0X07 | 0X24 | 0X19(F) | 80% |
| LINE INPUT | 0X08 | 0X23 | 0X15(A) | 50% |
| SPDIFIN | CONVERTER=0X0A | | PIN=0X1F | |

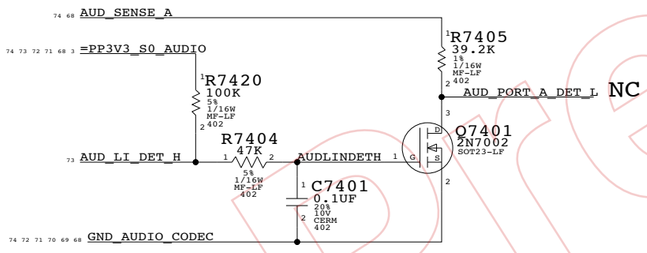
## AUDIO GROUND RETURNS



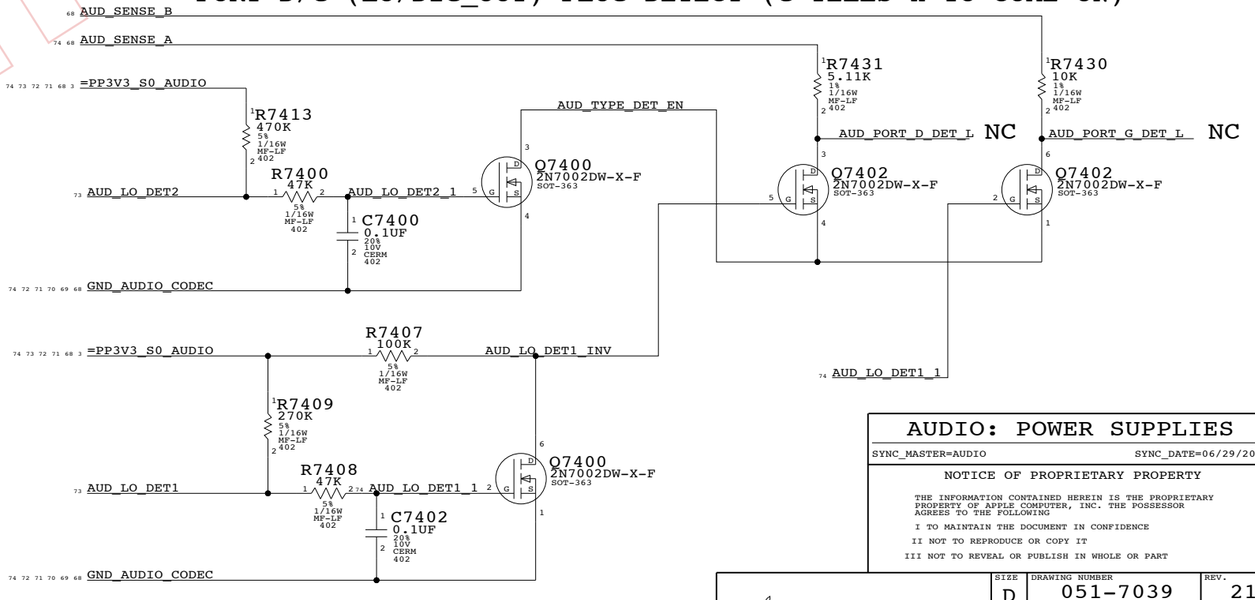

## MICROPHONE IMPEDANCE MATCHING CIRCUIT




## PORT A (LI) PLUG DETECT




## PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



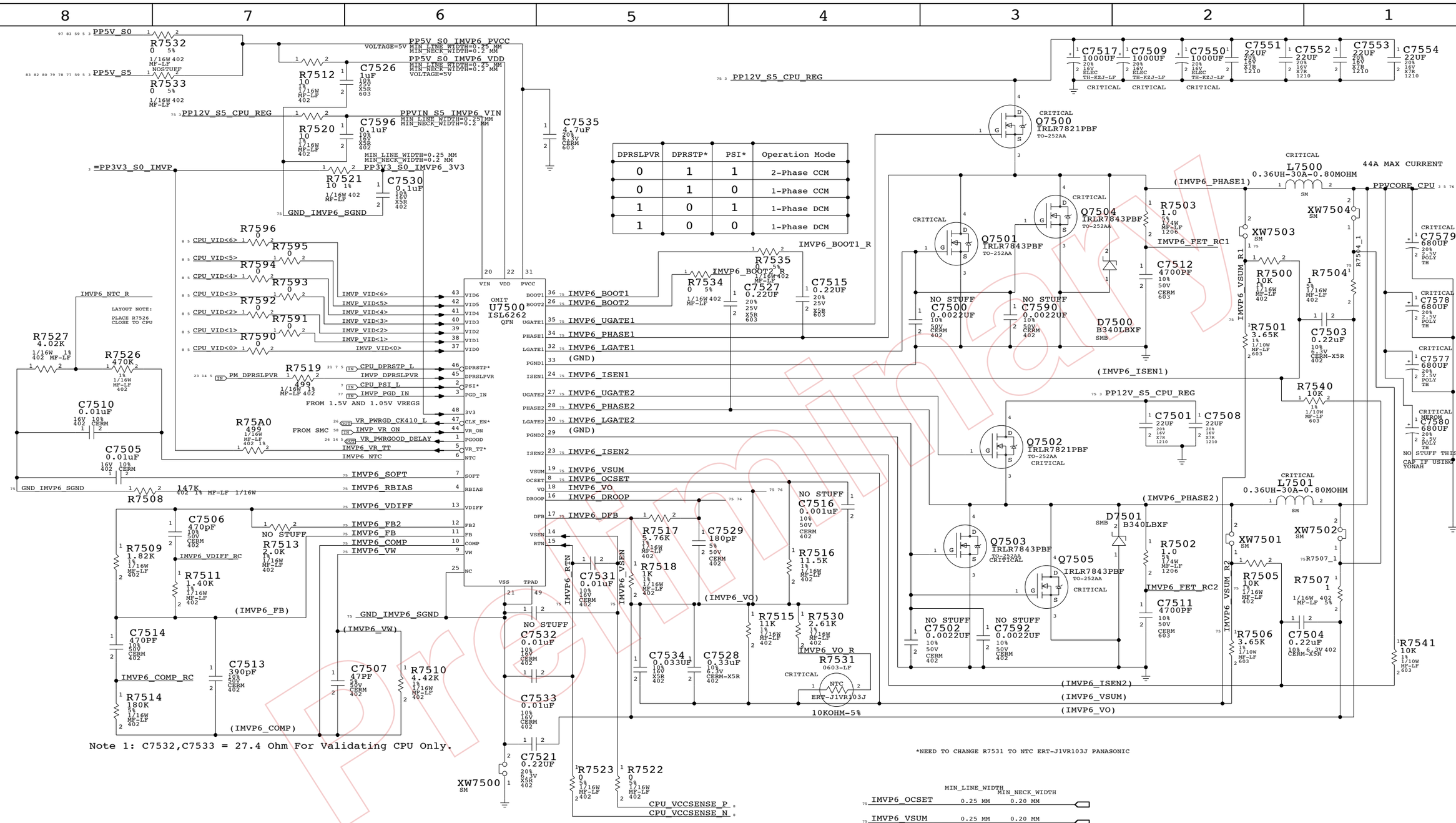

## AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 74 OF 97 | |




| DPRSLPVR | DPRSTP* | PSI* | Operation Mode |
|---|---|---|---|
| 0 | 1 | 1 | 2-Phase CCM |
| 0 | 1 | 0 | 1-Phase CCM |
| 1 | 0 | 1 | 1-Phase DCM |
| 1 | 0 | 0 | 1-Phase DCM |

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

CPU_VCCSENSE_P & N ARE DIFF PAIRS ROUTE AS 18MIL WIDE, 7MIL SPACE

# IMVP6 CPU VCORE REGULATOR

| | MIN_LINE_WIDTH | MIN_NECK_WIDTH |
|---|---|---|
| IMVP6_PHASE1 | 1.5 MM | 0.25 MM |
| IMVP6_BOOT1 | 0.25 MM | 0.25 MM |
| IMVP6_UGATE1 | 1.5 MM | 0.25 MM |
| IMVP6_LGATE1 | 1.5 MM | 0.25 MM |
| IMVP6_ISEN1 | 0.25 MM | 0.25 MM |
| IMVP6_FET_RC1 | 0.25 MM | 0.25 MM |
| IMVP6_VSUM_R1 | 0.25 MM | 0.25 MM |
| R7504_1 | 0.25 MM | 0.25 MM |

| | MIN_LINE_WIDTH | MIN_NECK_WIDTH |
|---|---|---|
| IMVP6_PHASE2 | 0.25 MM | 0.25 MM |
| IMVP6_BOOT2 | 0.25 MM | 0.25 MM |
| IMVP6_UGATE2 | 0.25 MM | 0.25 MM |
| IMVP6_LGATE2 | 0.25 MM | 0.25 MM |
| IMVP6_ISEN2 | 0.25 MM | 0.25 MM |
| IMVP6_FET_RC2 | 0.25 MM | 0.25 MM |
| IMVP6_VSUM_R2 | 0.60 MM | 0.25 MM |
| R7507_1 | 0.25 MM | 0.25 MM |

| | MIN_LINE_WIDTH | MIN_NECK_WIDTH |
|---|---|---|
| IMVP6_OCSET | 0.25 MM | 0.20 MM |
| IMVP6_VSUM | 0.25 MM | 0.20 MM |
| GND_IMVP6_SGND | 0.50 MM | 0.20 MM |
| IMVP6_VO | 0.25 MM | 0.20 MM |
| IMVP6_DROOP | 0.25 MM | 0.20 MM |
| IMVP6_DFB | 0.25 MM | 0.20 MM |
| IMVP6_SOFT | 0.25 MM | 0.20 MM |
| IMVP6_RBIAS | 0.25 MM | 0.20 MM |
| IMVP6_VDIFF | 0.25 MM | 0.20 MM |
| IMVP6_FB2 | 0.25 MM | 0.20 MM |
| IMVP6_FB | 0.25 MM | 0.20 MM |
| IMVP6_COMP | 0.25 MM | 0.20 MM |
| IMVP6_VW | 0.25 MM | 0.25 MM |
| IMVP6_RTN | 0.25 MM | 0.25 MM |
| IMVP6_VSEN | 0.25 MM | 0.25 MM |

IMVP6 CPU VCore Regulator

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 75 OF 97 | |

## PROCESSOR VCORE SENSE

PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)

75 5 3 PPVCORE_CPU — R7612 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_VSENSE 58

C7612 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

## PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

C7600 470PF 10% 50V CERM 402 — CPU_ISENSE_OUT_R

R7600 1M 1% 1/16W MF-LF 402

C7601 0.1UF CERM 20% 402 10V CRITICAL

75 IMVP6_VO — R7659 0 5% 1/16W MF-LF 402 — IMVP6_VO_R_OA

R7605 40.2K 1% 1/16W MF-LF 402 — CPU_ISENSE_R_POS

84 83 76 41 27 26 10 6 5 3 PP3V3_S0

U7600 LMV2011MF SOT23-5 — GND_CPU_ISENSE_OPAMP

75 IMVP6_DROOP — R7669 0 5% 1/16W MF-LF 402 — IMVP6_DROOP_R

R7606 40.2K 1% 1/16W MF-LF 402 — CPU_ISENSE_R_NEG

MIN_LINE_WIDTH=0.20 MM

PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)

R7602 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_ISENSE 58

C7602 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

NOSTUFF R7604 0 5% 1/16W MF-LF 402

C7603 470PF 10% 50V CERM 402 — R7603 1M 1% 1/16W MF-LF 402

R7607 0 5% 1/16W MF-LF 402 — GND_NEXT_TO_SMC 59

# CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

83 3 PP12V_S0_B

R7639 10K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_L — MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.20 MM

Q7640 NTR4101P SOT-23

R7641 10K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_L_R

ISENSE_CAL_EN_LS12V

R7642 470K 5% 1/16W MF-LF 402

58 5 ISENSE_CAL_EN

Q7639 2N7002 SOT23-LF

R7640 100K 5% 1/16W MF-LF 402

9 8 3 =PPVCORE_S0_CPU

R7643 1.00 1% 1/4W MF-LF 1206

CPUVCORE_ISENSE_CAL — MIN_LINE_WIDTH=0.50 MM, MIN_NECK_WIDTH=0.20 MM

CRITICAL Q7641 FDC796N SUPERSOT-6

## SMC PWRGD PULLUP

83 80 79 78 77 66 65 26 6 5 3 PP3V3_S5

R7623 10K 1% 1/16W MF-LF 402

NOSTUFF R7620 0 5% 1/16W MF-LF 402

82 78 6 SYS_POWERFAIL_L — RSMRST_PWRGD 58

## SYSTEM CURRENT SENSE

PP12V_S5_AC_DC — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

CRITICAL R7650 0.005 1% 2W MF 2010 — SYS_PWR_SENSE

PP12V_S5 3 76 77 78 79 80 82 83

PCB:KEEP SHORTS NEXT TO U7602

PCB:PLACE D7650,R7652,C7650 BY SMC

SYS_PWR_SENSE

CRITICAL U7602 ZXCT1010 SOT23-5 — VIN, IOUT, NC, LOAD, GND

OMIT XW7650 SM — SYSTEM_DCIN_SENSE — SYSTEM_SENSE_I_R

PP3V3_S0 3 5 6 10 26 27 41 76 83 84

NOSTUFF D7650 BAS16-75V-0.25A SOT23-LF → TO SMC

R7652 4.53K 1% 1/16W MF-LF 402 — SMC_DCIN_ISENSE 58

R7651 5.90K 1% 1/16W MF-LF 402

C7650 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

1 MS TIME CONSTANT — SO SMC ADC SAMPLING WORKS WELL.

R7656 100 1% 1/16W MF-LF 402 — SYSTEM_SENSE_SET

| SCALE | COUNT |
|---|---|
| 3.33333 A/V | .010753 A/COUNT |
| ADC IS 10BIT | 0 TO 1023 |
| | 0 TO 3.3V |

PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)

## SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

83 82 80 79 78 77 76 3 PP12V_S5

R7653 6.04K 1% 1/16W MF-LF 402

R7655 4.53K 1% 1/16W MF-LF 402 — SMC_SYSTEM_VSENSE_R — SMC_PBUS_VSENSE 58

R7654 2.0K 1% 1/16W MF-LF 402

C7651 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 58 59 76 84

| SCALE | COUNT |
|---|---|
| 4 V/V | .0129 V/COUNT |
| ADC IS 10BIT | 0 TO 1023 |
| | 0 TO 3.3V |

PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)

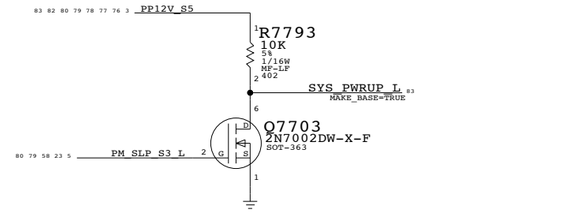
## CPU & SYSTEM SENSE

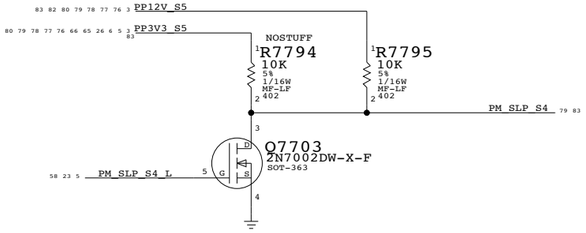
SYNC_MASTER=M51_DAVE — SYNC_DATE=(MASTER)

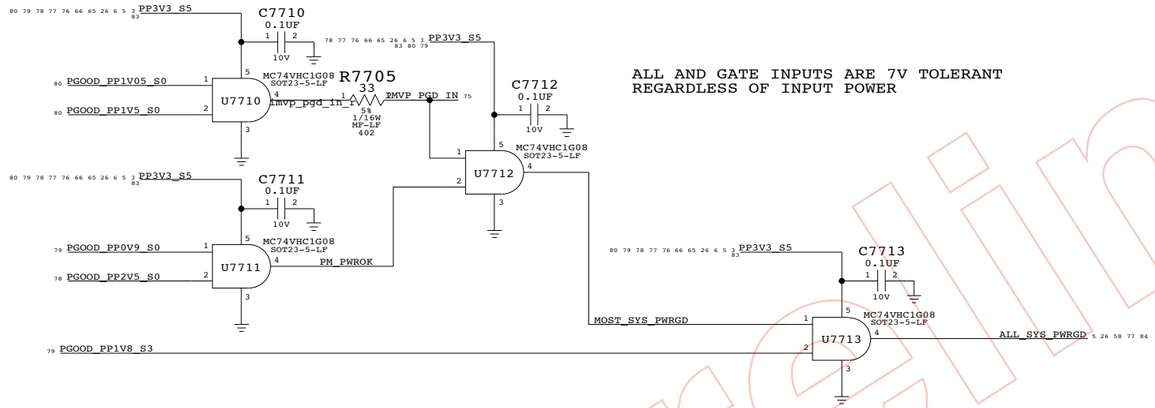


APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 76 OF 97 | |

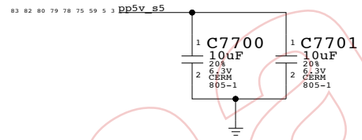


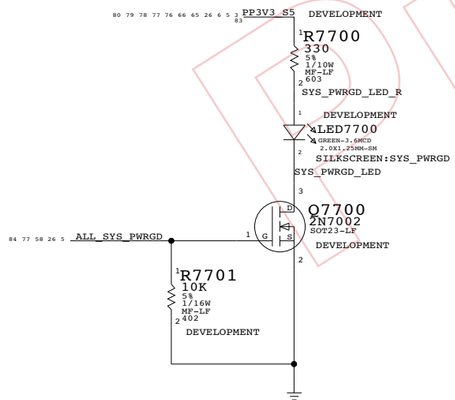




ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 bh page 82




PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

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APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 77 OF 97 | |

# 3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

3.3V S5
POWER BUDGET
MISC=1.500A
SB=0.500A
AIRPORT=1.000A
PANEL=1.000A
TOTAL=4.000A

PP12V_S5
PP3V3_S5 2V5_LDO
PP2V5_S5 2.50V NOMINAL
PP3V3_S5 3.35V NOMINAL
PP5V_S5
2V5_LDODR_C nostuff
3V3REG_LDO_FB
3V3REG_LDO_DR
3V3REG_VCC5
3V3REG_PVCC5
3V3REG_UGATE
3V3REG_BOOT
3V3REG_BOOT_R
3V3REG_SWITCHNODE
3V3REG_LGATE
3V3REG_FB
3V3REG_COMP
3V3REG_COMP_R
3V3REG_SNUB
3V3REG_FB_R
3V3REG_FS_DIS
3V3REG_GND
SYS_POWERFAIL_L
2V2_REF 2.219V
PGOOD_PP2V5_S0

C7892 1UF 10% 25V X5R 603
C7820 22UF 20% 6.3V X5R 805
Q7803 IRF1902PBF SO-8 CRITICAL
C7823 1000PF 10% 25V X7R 402
C7824 1000PF 10% 25V X7R 402
C7825 10UF 20% 6.3V CERM 805-1
C7822 10UF 20% 6.3V CERM 805-1
C7821 10UF 20% 6.3V CERM 805-1
C7826 10UF 20% 6.3V CERM 805-1
R7820 1K 1% 1/16W MF-LF 402
R7821 2.7K 5% 1/16W MF-LF 402
R7822 470 1% 1/16W MF-LF 402
C7800 1UF 10% 6.3V CERM 402
R7805 10 1% 1/16W MF-LF 402
U7800 ISL6549 QFN
VCC12 CRITICAL
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND AGND PGND
UGATE
BOOT
PHASE
LGATE
FB
COMP
R7840 2.2 5% 1/16W MF-LF 402
C7801 0.1UF 20% 25V CERM 603
Q7800 IRLR7807Z TO-252AA CRITICAL
C7853 680UF 20% 16V ELEC TH-MCZ CRITICAL
C7811 10UF 10% 16V CERM 1210
L7803 3.0UH TH1 CRITICAL
Q7801 IRLR7807Z TO-252AA CRITICAL
D7800 CMLSH3-30M833 TLM833
nostuff
C7802 1000PF 10% 25V X7R 402
R7804 8.06K 1% 1/16W MF-LF 402
C7806 560PF 10% 50V CERM 402
C7808 0.047UF 10% 16V CERM 402
XW7800 SM
R7802 5.11 1% 1/4W MF-LF 1206
C7809 1000PF 5% 50V CERM 1206
C7815 1800UF 20% 6.3V ELEC TH-KZJ-LF CRITICAL
C7814 10UF 20% 6.3V CERM 805-1
C7813 10UF 20% 6.3V CERM 805-1
R7899 22 5% 1/16W MF-LF 402
R7803 1.24K 1% 1/16W MF-LF 402 (R2)
C7807 0.01UF 10% 16V CERM 402
R7801 392 1% 1/16W MF-LF 402 (R1)

5% OK ON R7801?
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

R7892 100K 5% 1/16W MF-LF 402
Q7802 2N7002 SOT23-LF NOSTUFF
C7803 4.7UF 20% 6.3V CERM 603

C7880 0.1UF 20% 10V CERM 402
R7811 2.49K 1% 1/16W MF-LF 402
R7812 5.11K 1% 1/16W MF-LF 402
R7810 10K 1% 1/16W MF-LF 402
U7810 LM339A SOI-LF
SPARE COMPARATOR

3V DC/DC 2.5V

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |

SCALE NONE

SHT 78 OF 97

# 1.8V AND 1.2V S3 REGULATOR

1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A

=PP1V8_S3_1V2_LDO
C7920 22UF 20% 6.3V X5R 805
CRITICAL Q7903 IRF1902PBF SO-8
PP12V_S5
C7992 1UF 10% 25V X5R 603
C7900 1UF 10% 6.3V CERM 402
1V8REG_DDR_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7905 10 1% 1/16W MF-LF 402
1V8REG_DDR_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7923 1000PF 10% 25V X7R 402
1V2_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7921 2.7K 5% 1/16W MF-LF 402
C7924 1000PF 10% 25V X7R 402
1V8REG_DDR_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
PP1V2_S3 1.21V NOMINAL
C7925 10UF 20% 6.3V CERM 805-1
C7922 10UF 20% 6.3V CERM 805-1
C7921 10UF 20% 6.3V CERM 805-1
C7926 10UF 20% 6.3V CERM 805-1
R7920 1K 1% 1/16W MF-LF 402
R7922 1.96K 1% 1/16W MF-LF 402
1V8REG_DDR_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7992 100K 5% 1/16W MF-LF 402
Q7902 2N7002 SOT23-LF
PM_SLP_S4
C7903 4.7UF 20% 6.3V CERM 603
1V8REG_DDR_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
PM_SLP_S3_L
MEMVTT_EN

VCC12
U7900 ISL6549 QFN
CRITICAL
VCC5 PVCC5 LDO_DR LDO_FB FS_DIS THRML_PAD DGND AGND PGND
UGATE BOOT PHASE LGATE FB COMP
1V8REG_DDR_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7940 2.2 5% 1/16W MF-LF 402
1V8REG_DDR_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7901 0.1UF 20% 25V CERM 603
1V8REG_DDR_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
1V8REG_DDR_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7904 8.06K 1% 1/16W MF-LF 402
C7908 0.047UF 10% 16V CERM 402
1V8REG_DDR_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7906 560PF 10% 50V CERM 402
XW7900 SM

Q7900 IRLR7807Z TO-252AA
Q7901 IRLR7807Z TO-252AA
D7900 CTLSH3-30M833 TLM833
C7902 1000PF 10% 25V X7R 402

CRITICAL C7953 680UF 20% 16V ELEC TH-MCZ
CRITICAL C7954 680UF 20% 16V ELEC TH-MCZ
C7911 10UF 10% 16V CERM 1210
C7912 10UF 10% 16V CERM 1210
1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A
L7903 1.53UH TH-LF CRITICAL
CRITICAL C7956 1500UF 20% 6.3V ELEC TH-MCZ
CRITICAL C7957 1500UF 20% 6.3V ELEC TH-MCZ
C7913 10UF 10% 6.3V CERM 805-1
C7958 1UF 10% 6.3V CERM 402
C7959 1UF 10% 6.3V CERM 402
C7960 1UF 10% 6.3V CERM 402
PP1V8_S3 1.81V NOMINAL
R7902 5.11 1% 1/4W MF-LF 1206
1V8REG_DDR_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7909 1000PF 5% 50V CERM 1206
R7999 22 5% 1/16W MF-LF 402
R7903 1.24K 1% 1/16W MF-LF 402 (R2)
1V8REG_DDR_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7907 0.01UF 10% 16V CERM 402
R7901 953 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN / 0.800V TYP / 0.816V MAX

PP5V_S5
PP3V3_S5
R7911 5.49K 1% 1/16W MF-LF 402
R7910 10K 1% 1/16W MF-LF 402
1V2_REF 1.21V
U7810 LM339A SOI-LF
PGOOD_PP1V8_S3
R7912 2.7K 5% 1/16W MF-LF 402
R7914 8.45K 1% 1/16W MF-LF 402
R7913 10K 1% 1/16W MF-LF 402
0V7_REF 0.723V
PP0V9_S0
PGOOD_PP0V9_S0
R7915 2.37K 1% 1/16W MF-LF 402

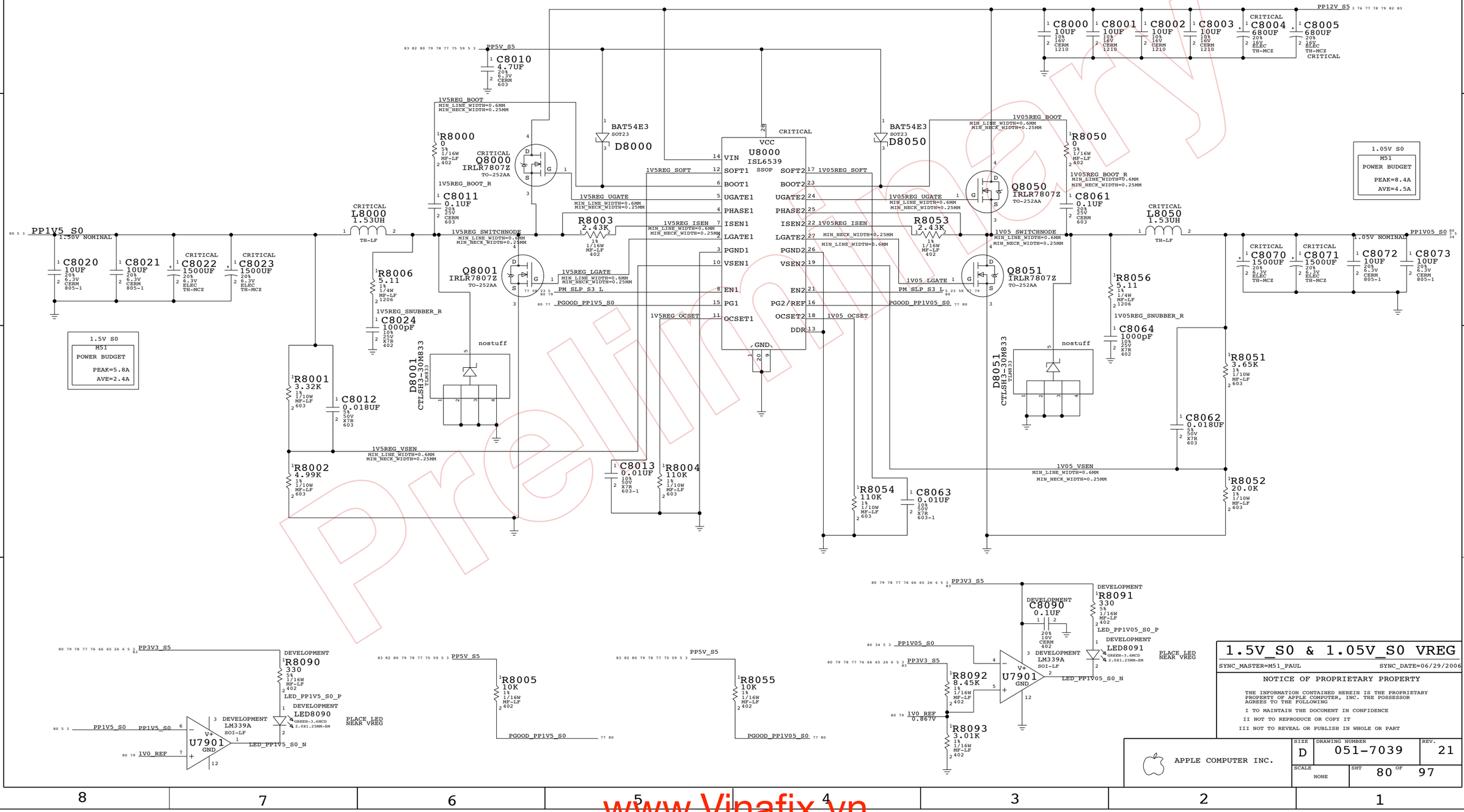
DEVELOPMENT
R7906 330 5% 1/16W MF-LF 402
LED_PP1V8_S3_P
LED7900 GREEN-3.6MCD 2.0X1.25MM-SM
PLACE_LED NEAR VREG
U7901 LM339A SOI-LF
1V0_REF
LED_PP1V8_S3_N

1.8V & 1.2V VREG
SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006



APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-7039 | REV. 21
SCALE NONE | SHT 79 OF 97

# 1.5V S0 AND 1.05V S0 RAILS

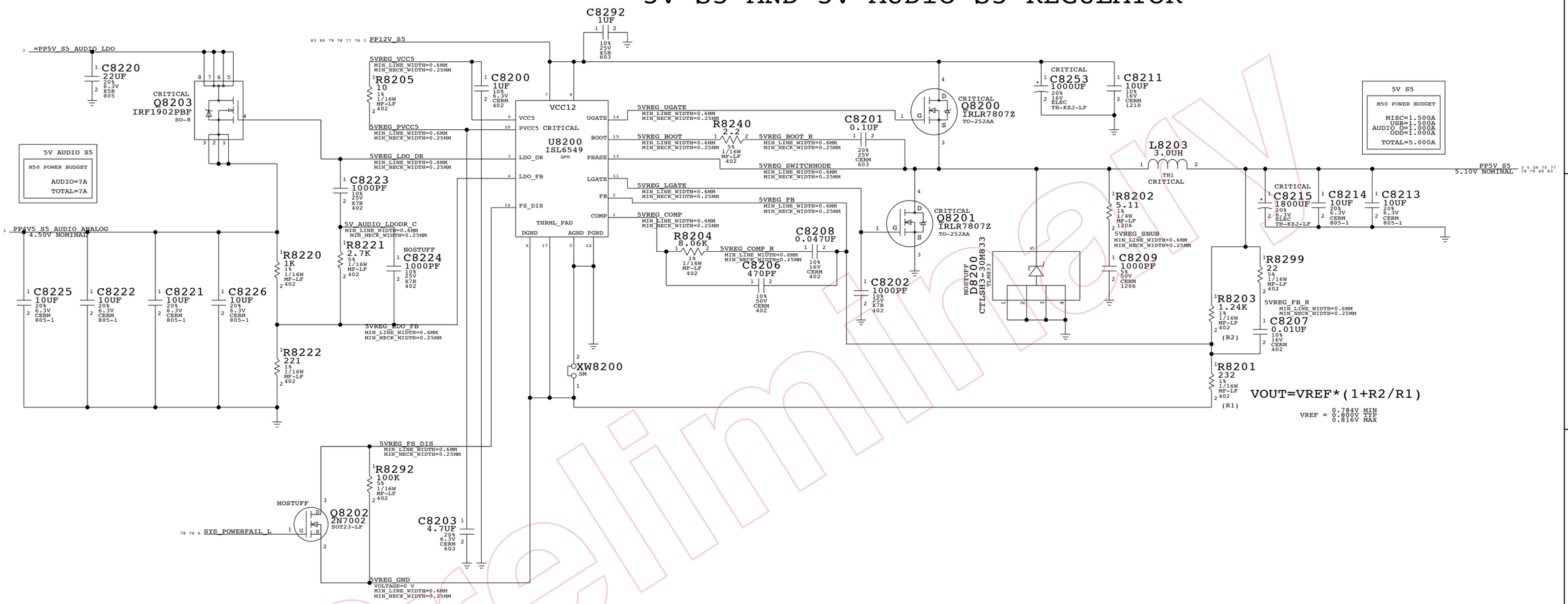



| | |
|---|---|
| 1.5V_S0 & 1.05V_S0 VREG | |
| SYNC_MASTER=M51_PAUL | SYNC_DATE=06/29/2006 |



| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|---|---|---|---|
| | D | 051-7039 | 21 |
| | SCALE: NONE | SHT 80 OF 97 | |

# 5V S5 AND 5V AUDIO S5 REGULATOR




POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

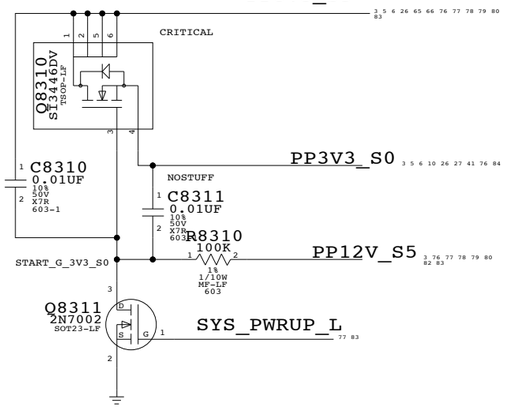
SYNC_MASTER=M50_PAUL SYNC_DATE=06/29/2006



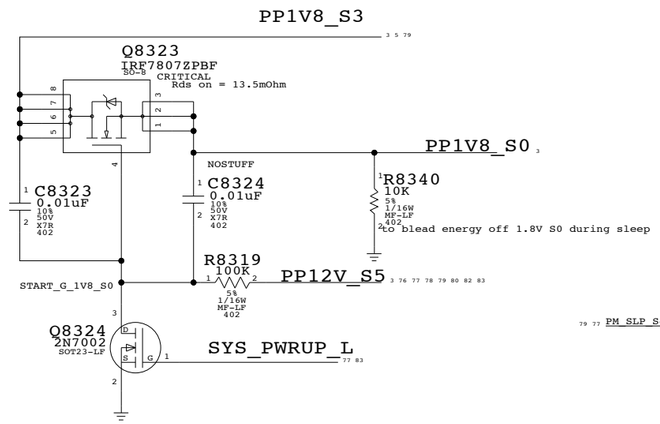
APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 82 OF 97 | |

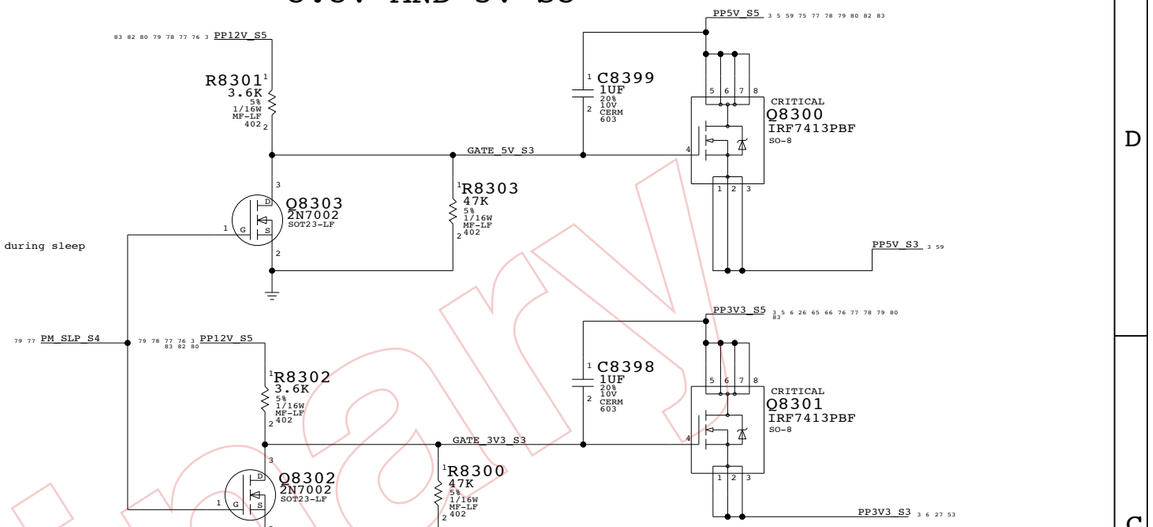
## 3.3V S0



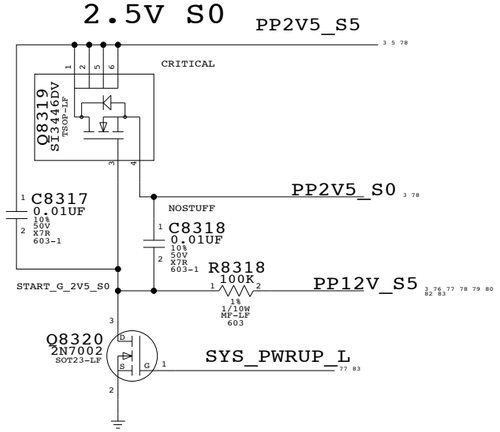

## 1.8V S0



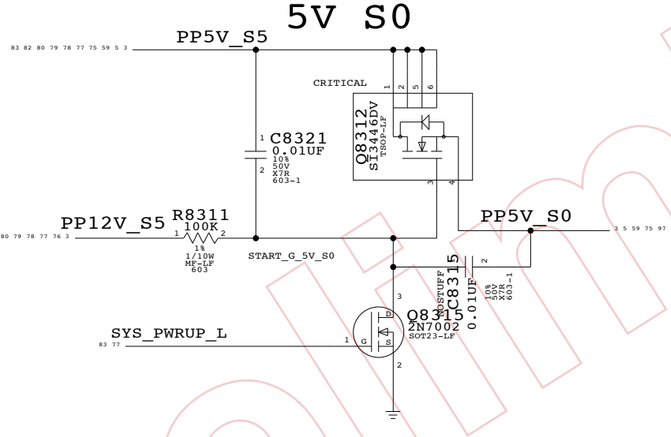

## 3.3V AND 5V S3



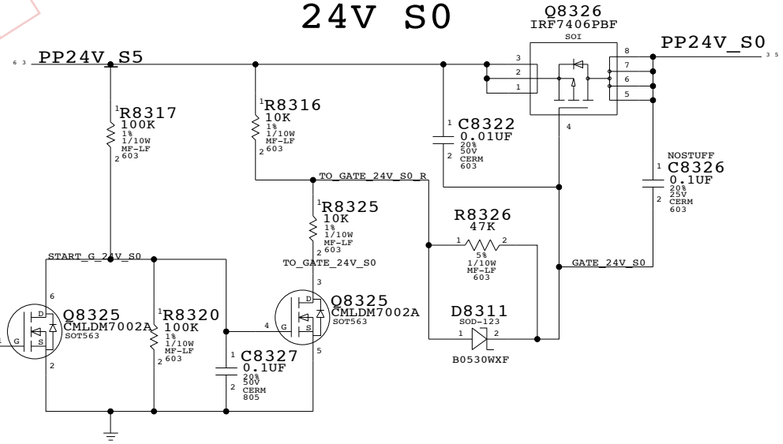

## 2.5V S0




## 5V S0

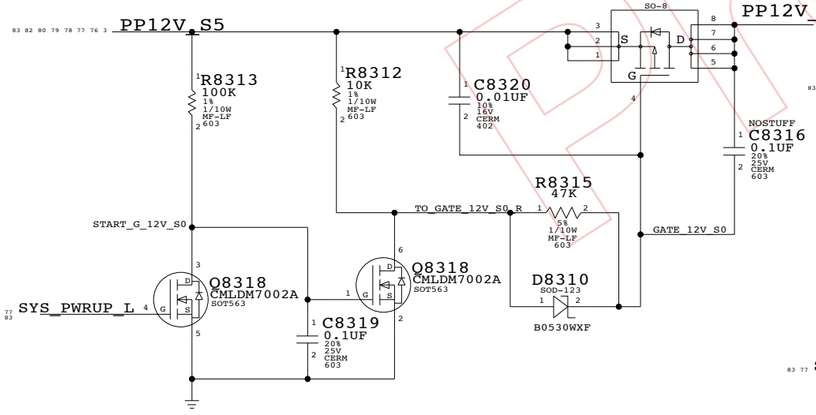



## 24V S0

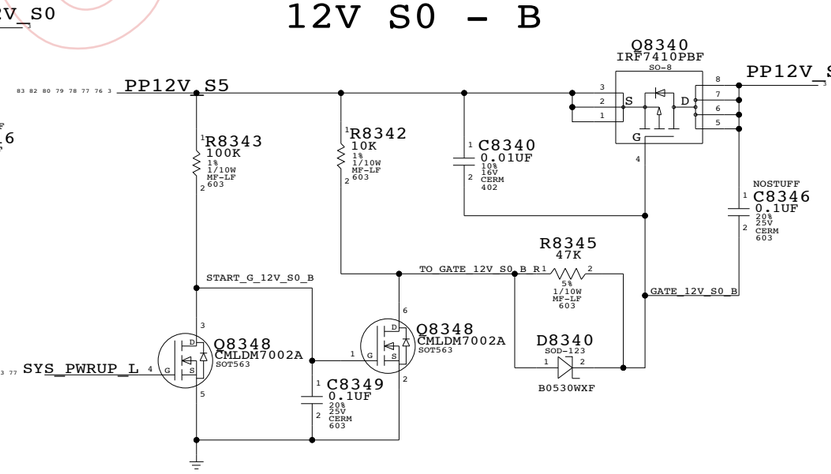



## 12V S0

Split 12V S0 is for better power plane structure
12VS0 - B will connect to MXM, Audio, Fans




## 12V S0 - B




## S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

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APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 83 OF 97 | |

# Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

| VOLTAGE | CURRENT | POWER |
|---|---|---|
| 3V3 | 1.5 A | 4.95 W |
| 5V | 0.5 A | 2.5 W |
| 2V5 | 0.5 A | 1.25 W |
| 1V8 | 3.5 A | 6.3 W |
| PWR (12V) | UP TO 4 A | PLATFORM DEPENDENT |

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

=PP1V8_S0_MXM
C8401 22UF 20% 6.3V X5R 805
C8402 22UF 20% 6.3V X5R 805 NOSTUFF
C8403 22UF 20% 6.3V X5R 805 NOSTUFF
=PP5V_S0_MXM
ALL_SYS_PWRGD

CRITICAL
J8400
AS0B326-S55N-7F
F-RT-SM
(1 OF 2)

| | | | |
|---|---|---|---|
| 2 | 1V8RUN0 | PWR_SRC0 | 1 |
| 4 | 1V8RUN1 | PWR_SRC1 | 3 |
| 6 | 1V8RUN2 | PWR_SRC2 | 5 |
| 8 | 1V8RUN3 | PWR_SRC3 | 7 |
| 10 | 1V8RUN4 | PWR_SRC4 | 9 |
| 12 | 1V8RUN5 | PWR_SRC5 | 11 |
| 14 | 1V8RUN6 | PWR_SRC6 | 13 |
| 16 | RUNPWROK | PWR_SRC7 | 15 |
| 18 | 5VRUN | GND0 | 17 |
| 20 | GND20 | GND1 | 19 |
| 22 | GND21 | GND2 | 21 |
| 24 | GND22 | GND3 | 23 |
| | KEY | | |
| 38 | PRSNT2_L | PEX_RX15_L | 37 |
| 40 | PEX_TX15_L | PEX_RX15 | 39 |
| 42 | PEX_TX15 | GND4 | 41 |
| 44 | GND23 | PEX_RX14_L | 43 |
| 46 | PEX_TX14_L | PEX_RX14 | 45 |
| 48 | PEX_TX14 | GND5 | 47 |
| 50 | GND24 | PEX_RX13_L | 49 |
| 52 | PEX_TX13_L | PEX_RX13 | 51 |
| 54 | PEX_TX13 | GND6 | 53 |
| 56 | GND25 | PEX_RX12_L | 55 |
| 58 | PEX_TX12_L | PEX_RX12 | 57 |
| 60 | PEX_TX12 | GND7 | 59 |
| 62 | GND26 | PEX_RX11_L | 61 |
| 64 | PEX_TX11_L | PEX_RX11 | 63 |
| 66 | PEX_TX11 | GND8 | 65 |
| 68 | GND27 | PEX_RX10_L | 67 |
| 70 | PEX_TX10_L | PEX_RX10 | 69 |
| 72 | PEX_TX10 | GND9 | 71 |
| 74 | GND28 | PEX_RX9_L | 73 |
| 76 | PEX_TX9_L | PEX_RX9 | 75 |
| 78 | PEX_TX9 | GND10 | 77 |
| 80 | GND29 | PEX_RX8_L | 79 |
| 82 | PEX_TX8_L | PEX_RX8 | 81 |
| 84 | PEX_TX8 | GND11 | 83 |
| 86 | GND30 | PEX_RX7_L | 85 |
| 88 | PEX_TX7_L | PEX_RX7 | 87 |
| 90 | PEX_TX7 | GND12 | 89 |
| 92 | GND31 | PEX_RX6_L | 91 |
| 94 | PEX_TX6_L | PEX_RX6 | 93 |
| 96 | PEX_TX6 | GND13 | 95 |
| 98 | GND32 | PEX_RX5_L | 97 |
| 100 | PEX_TX5_L | PEX_RX5 | 99 |
| 102 | PEX_TX5 | GND14 | 101 |
| 104 | GND33 | PEX_RX4_L | 103 |
| 106 | PEX_TX4_L | PEX_RX4 | 105 |
| 108 | PEX_TX4 | GND15 | 107 |
| 110 | GND34 | PEX_RX3_L | 109 |
| 112 | PEX_TX3_L | PEX_RX3 | 111 |
| 114 | PEX_TX3 | GND16 | 113 |
| 116 | GND35 | PEX_RX2_L | 115 |
| 118 | PEX_TX2_L | PEX_RX2 | 117 |
| 120 | PEX_TX2 | GND17 | 119 |
| 122 | GND36 | PEX_RX1_L | 121 |
| 124 | PEX_TX1_L | PEX_RX1 | 123 |
| 126 | PEX_TX1 | GND18 | 125 |
| 128 | GND37 | PEX_RX0_L | 127 |
| 130 | PEX_TX0_L | PEX_RX0 | 129 |
| 132 | PEX_TX0 | GND19 | 131 |

PRSNT2_L: RESERVED FOR FUTURE USE

PPV_S0_MXM_PWRSRC (VOLTAGE=12V, MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.25MM)
C8400 22UF 20% 35V ELEC SM-LF

PLACE CAPS NEAR NB

| | | | |
|---|---|---|---|
| PEG_R2D_C_P<0> | C8420 0.1uF | PEG_R2D_P<15> | PEG_D2R_P<0> |
| PEG_R2D_C_N<0> | C8421 0.1uF | PEG_R2D_N<15> | PEG_D2R_N<0> |
| PEG_R2D_C_P<1> | C8422 0.1uF | PEG_R2D_P<14> | PEG_D2R_P<1> |
| PEG_R2D_C_N<1> | C8423 0.1uF | PEG_R2D_N<14> | PEG_D2R_N<1> |
| PEG_R2D_C_P<2> | C8424 0.1uF | PEG_R2D_P<13> | PEG_D2R_P<2> |
| PEG_R2D_C_N<2> | C8425 0.1uF | PEG_R2D_N<13> | PEG_D2R_N<2> |
| PEG_R2D_C_P<3> | C8426 0.1uF | PEG_R2D_P<12> | PEG_D2R_P<3> |
| PEG_R2D_C_N<3> | C8427 0.1uF | PEG_R2D_N<12> | PEG_D2R_N<3> |
| PEG_R2D_C_P<4> | C8428 0.1uF | PEG_R2D_P<11> | PEG_D2R_P<4> |
| PEG_R2D_C_N<4> | C8429 0.1uF | PEG_R2D_N<11> | PEG_D2R_N<4> |
| PEG_R2D_C_P<5> | C8430 0.1uF | PEG_R2D_P<10> | PEG_D2R_P<5> |
| PEG_R2D_C_N<5> | C8431 0.1uF | PEG_R2D_N<10> | PEG_D2R_N<5> |
| PEG_R2D_C_P<6> | C8432 0.1uF | PEG_R2D_P<9> | PEG_D2R_P<6> |
| PEG_R2D_C_N<6> | C8433 0.1uF | PEG_R2D_N<9> | PEG_D2R_N<6> |
| PEG_R2D_C_P<7> | C8434 0.1uF | PEG_R2D_P<8> | PEG_D2R_P<7> |
| PEG_R2D_C_N<7> | C8435 0.1uF | PEG_R2D_N<8> | PEG_D2R_N<7> |
| PEG_R2D_C_P<8> | C8436 0.1uF | PEG_R2D_P<7> | PEG_D2R_P<8> |
| PEG_R2D_C_N<8> | C8437 0.1uF | PEG_R2D_N<7> | PEG_D2R_N<8> |
| PEG_R2D_C_P<9> | C8438 0.1uF | PEG_R2D_P<6> | PEG_D2R_P<9> |
| PEG_R2D_C_N<9> | C8439 0.1uF | PEG_R2D_N<6> | PEG_D2R_N<9> |
| PEG_R2D_C_P<10> | C8440 0.1uF | PEG_R2D_P<5> | PEG_D2R_P<10> |
| PEG_R2D_C_N<10> | C8441 0.1uF | PEG_R2D_N<5> | PEG_D2R_N<10> |
| PEG_R2D_C_P<11> | C8442 0.1uF | PEG_R2D_P<4> | PEG_D2R_P<11> |
| PEG_R2D_C_N<11> | C8443 0.1uF | PEG_R2D_N<4> | PEG_D2R_N<11> |
| PEG_R2D_C_P<12> | C8444 0.1uF | PEG_R2D_P<3> | PEG_D2R_P<12> |
| PEG_R2D_C_N<12> | C8445 0.1uF | PEG_R2D_N<3> | PEG_D2R_N<12> |
| PEG_R2D_C_P<13> | C8446 0.1uF | PEG_R2D_P<2> | PEG_D2R_P<13> |
| PEG_R2D_C_N<13> | C8447 0.1uF | PEG_R2D_N<2> | PEG_D2R_N<13> |
| PEG_R2D_C_P<14> | C8448 0.1uF | PEG_R2D_P<1> | PEG_D2R_P<14> |
| PEG_R2D_C_N<14> | C8449 0.1uF | PEG_R2D_N<1> | PEG_D2R_N<14> |
| PEG_R2D_C_P<15> | C8450 0.1uF | PEG_R2D_P<0> | PEG_D2R_P<15> |
| PEG_R2D_C_N<15> | C8451 0.1uF | PEG_R2D_N<0> | PEG_D2R_N<15> |

## MXM PWRSRC (GPU CORE) CURRENT SENSE

=PPV_S0_MXM_PWRSRC
CRITICAL R8450 0.025 1% 1/2W MF 2512-1
PPV_S0_MXM_PWRSRC
PCB:KEEP SHORTS NEXT TO U8450
PCB:PLACE D8450,R8452,C8458 BY SMC
MXM_PWR_SENSE
CRITICAL U8450 ZXCT1010 SOT23-5 (VIN, IOUT, NC, LOAD, GND)
PP3V3_S0
NOSTUFF D8450 BAS16-75V-0.25A SOT23-LF → TO SMC
OMIT XW8450 SM
MXM_PWRSRC_SENSE
MXM_SENSE_I_R
MXM_PWR_SENSE R8452 4.53K 1% 1/16W MF-LF 402
SMC_GPU_ISENSE
MXM_PWR_SENSE R8451 3.01K 1% 1/16W MF-LF 402
MXM_PWR_SENSE C8458 0.22UF 20% 6.3V X5R 402
1MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.
GND_SMC_AVSS

| SCALE | COUNT |
|---|---|
| 1.33333 A/V | .004296875 A/COUNT |

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

## MXM PWRSRC VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

PPV_S0_MXM_PWRSRC
MXM_PWR_SENSE R8453 6.04K 1% 1/16W MF-LF 402
MXM_PWR_SENSE R8455 4.53K 1% 1/16W MF-LF 402
PCB: PLACE R8455, C8459 WITHIN 1" OF SMC (U5800)
SMC_MXM_VSENSE_R
SMC_GPU_VSENSE
MXM_PWR_SENSE R8454 2.0K 1% 1/16W MF-LF 402
MXM_PWR_SENSE C8459 0.22UF 20% 6.3V X5R 402
GND_SMC_AVSS

| SCALE | COUNT |
|---|---|
| 4 V/V | .0129 V/COUNT |

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)



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SCALE: NONE SHT 84 OF 97

# Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)

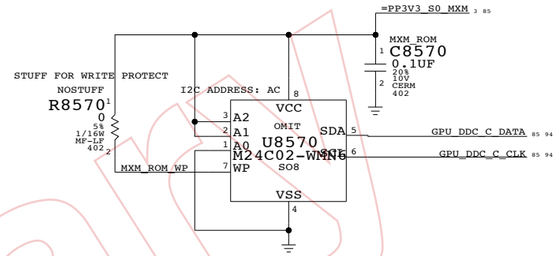
## MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

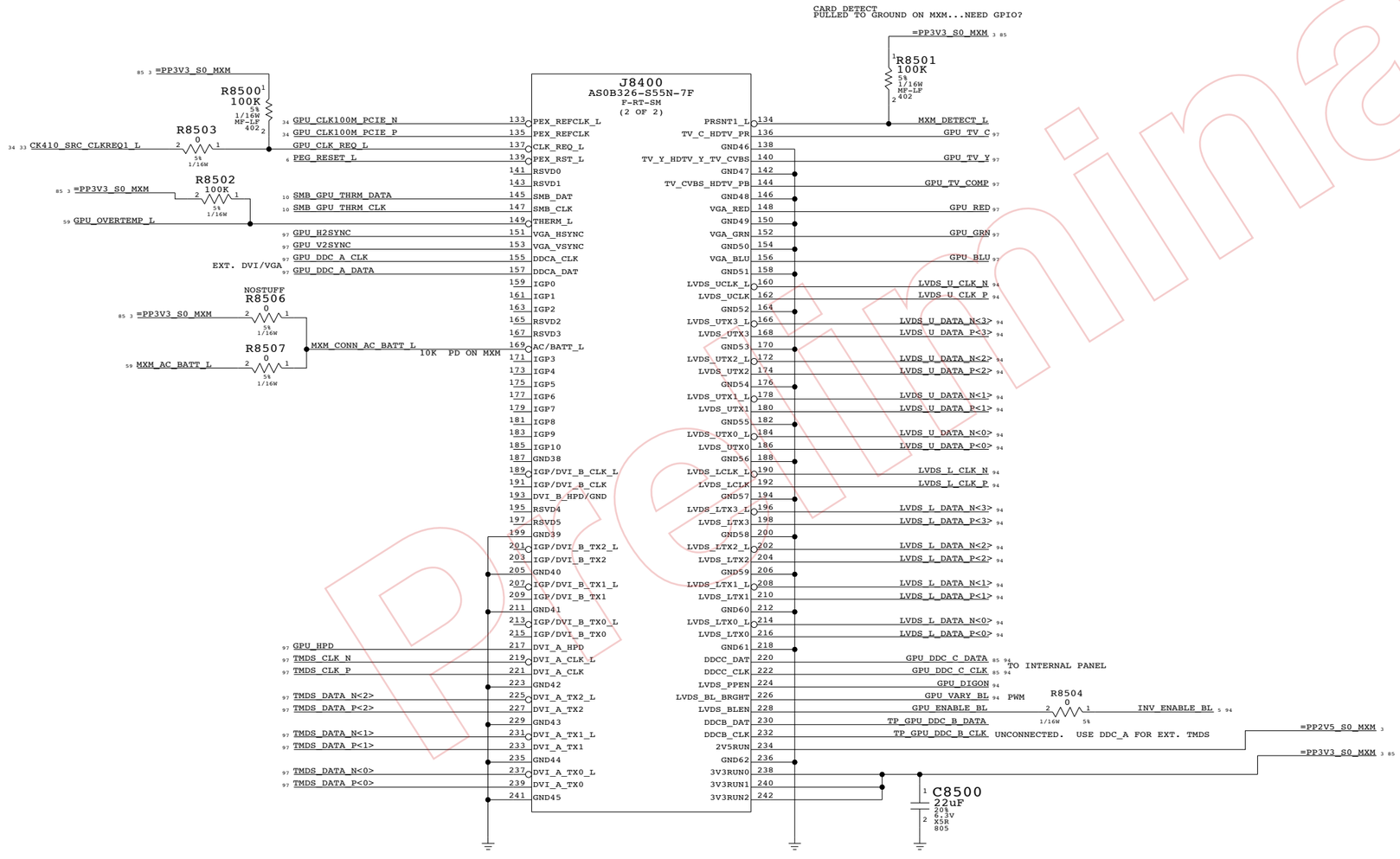
| VOLTAGE | CURRENT | POWER |
|---|---|---|
| 3V3 | 1.5 A | 4.95 W |
| 5V | 0.5 A | 2.5 W |
| 2V5 | 0.5 A | 1.25 W |
| 1V8 | 3.5 A | 6.3 W |
| PWR (12V) | UP TO 4 A | PLATFORM DEPENDENT |

## MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400




CARD DETECT
PULLED TO GROUND ON MXM...NEED GPIO?




## MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)



APPLE COMPUTER INC.

| SIZE | DRAWING NUMBER | REV. |
|---|---|---|
| D | 051-7039 | 21 |
| SCALE: NONE | SHT 85 OF 97 | |

# Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

## LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

3 =PPV_S0_LCD

NOSTUFF R9490 0 5% 1/8W MF-LF 805

R9400[1] 100K 5% 1/16W MF-LF 402

C9400 0.1UF 10% 50V X7R 603-1

PLACE NEAR J9402

R9401 29.4K 1% 1/16W MF-LF 402

LCD_PWREN_DIV

LCD_PWREN_L_RC

R9499[1] 100K 5% 1/16W MF-LF 402

Q9400 SI3443DV TSOP-LF

PP12V_LCD_SW

VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9400 FERR-250-OHM SM

VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

PP12V_LCD_CONN 6 94

C9420 10UF 10% 16V CERM 1210

C9401 0.001uF 20% 50V CERM 402

LCD_PWREN_L

85 GPU_DIGON

Q9401 2N7002 SOT23-LF

R9470[1] 100K 5% 1/16W MF-LF 402

CRITICAL
SDF9400
STDOFF-3MMOD4.6MMH-1.35-TH

CRITICAL
J9402
53307-3072
F-ST-SM

| | | | |
|---|---|---|---|
| 85 LVDS_U_DATA_N<0> | 1 | 2 | LVDS_U_DATA_P<0> 85 |
| 85 LVDS_U_DATA_N<1> | 3 | 4 | LVDS_U_DATA_P<1> 85 |
| 85 LVDS_U_DATA_N<2> | 5 | 6 | LVDS_U_DATA_P<2> 85 |
| | 7 | 8 | LVDS_U_CLK_N 85 |
| 85 LVDS_U_CLK_P | 9 | 10 | LVDS_U_DATA_N<3> 85 |
| 85 LVDS_U_DATA_P<3> | 11 | 12 | LVDS_L_DATA_N<0> 85 |
| 85 LVDS_L_DATA_P<0> | 13 | 14 | |
| 85 LVDS_L_DATA_N<1> | 15 | 16 | LVDS_L_DATA_P<1> 85 |
| | 17 | 18 | LVDS_L_DATA_N<2> 85 |
| 85 LVDS_L_DATA_P<2> | 19 | 20 | LVDS_L_CLK_N 85 |
| 85 LVDS_L_CLK_P | 21 | 22 | LVDS_L_DATA_N<3> 85 |
| 85 LVDS_L_DATA_P<3> | 23 | 24 | |
| 85 GPU_DDC_C_CLK | 25 | 26 | GPU_DDC_C_DATA 85 |
| | 27 | 28 | |
| | 29 | 30 | |

94 =PP3V3_DDC_LCD

94 6 PP12V_LCD_CONN

PP12V_LCD_CONN 6 94

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9410 0.001uF 20% 50V CERM 402

CRITICAL
SDF9401
STDOFF-3MMOD4.6MMH-1.35-TH

## INVERTER INTERFACE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS

CRITICAL
J9400
88290-14XG
M-ST-SM

3 =PPV_S0_INVERTER

C9440 2.2UF 10% 50V X7R 1206

97 94 3 =PP3V3_S0_VIDEO

NOSTUFF R9440[1] 10K 5% 1/16W MF-LF 402

85 5 INV_ENABLE_BL

94 5 LCD_PWM

85 GPU_VARY_BL

R9475 47 5% 1/16W MF-LF 402

LCD_PWM 5 94

NOSTUFF R9474[1] 10K 5% 1/16W MF-LF 402

Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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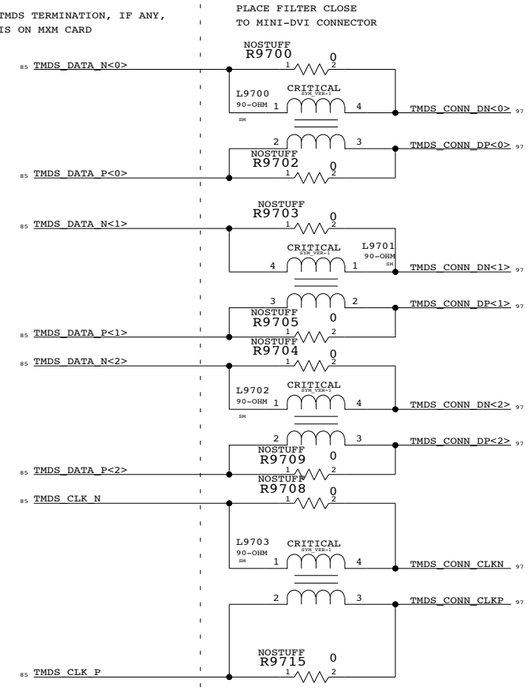
| SCALE: NONE | SHT 94 OF 97 | |

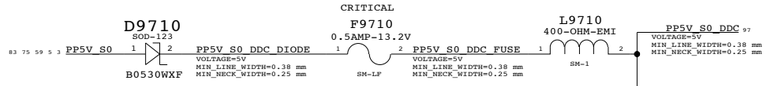
# DVI INTERFACE

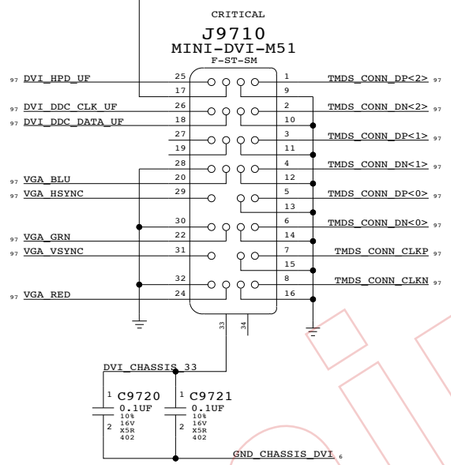
TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

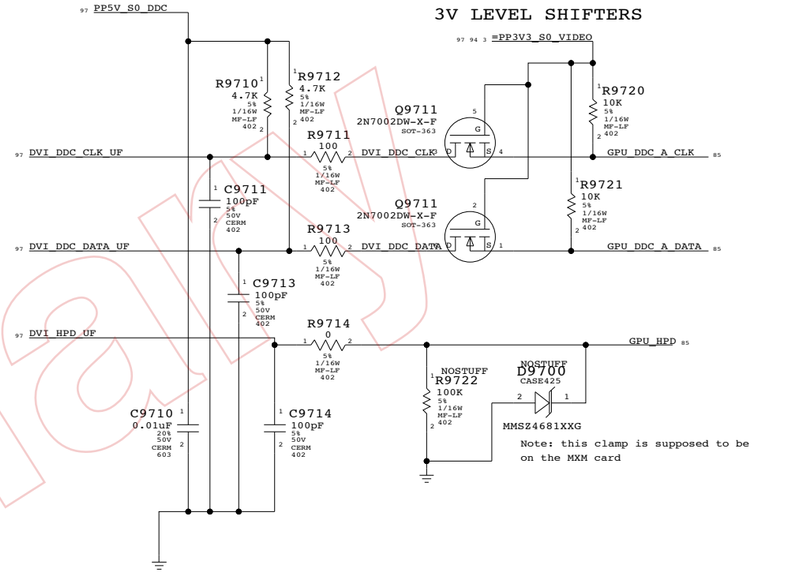


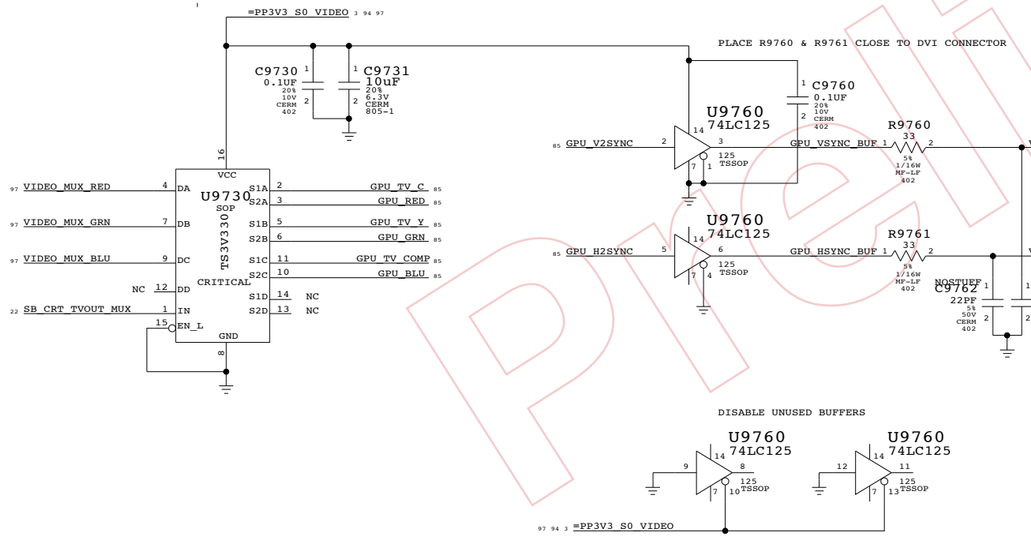

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)




PLACE CLOSE TO MINI-DVI CONNECTOR
3V LEVEL SHIFTERS



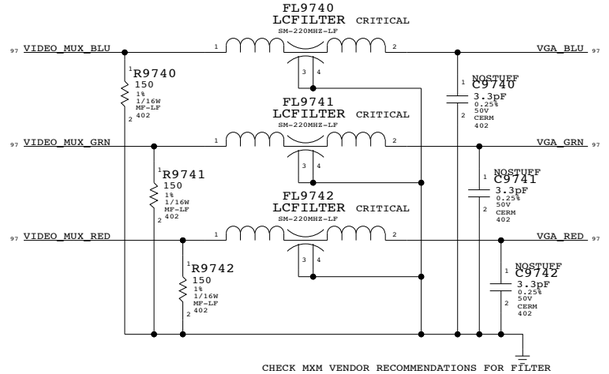

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR




DISABLE UNUSED BUFFERS




ANALOG FILTERING
PLACE CLOSE TO CONNECTOR




| | |
|---|---|
| | External Display Conns |
| SYNC_MASTER=M51_DAVE | SYNC_DATE=(MASTER) |



| | | | |
|---|---|---|---|
| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-7039 | REV. 21 |
| | SCALE NONE | SHT 97 OF 97 | |