1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

OROYA

01/23/2007 - EVT

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7225	1	SCHEM,MLB,M75	SCH	CRITICAL	
820-2101	1	PCBF,MLB,M75	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Jan 23 15:38:53 2007

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,OROYA,M75

DRAWING NUMBER 051-7225
REV 10.0.0
SHT 1 OF 88

T9 Diagram -- Needs to be updated to M75

U1000
CPU
2.? GHz
Core ~1.2V
Pg 10
Pg 9

J1300/JD000
ITP/XDP CONN
Pg 12/103

U2900
CK 505
Clocks Pg 28 | TERMS Pg 29

UC500
ReGen
Clocks Pg 98 | TERMS Pg 98

FSB
64-Bit
800/1066? MHz

J8000
PEG Connector
Pg 77

x16 PCI-E
SDVO

Pg 13
U1400
NB-GMCH
Core
1.05 - 1.25V
Pg 17,18,19

PCI-E Pg 14
TV Out RGB LVDS Pg 14
Main Memory Pg 15/16
Misc Pg 15
DMI Pg 15
CLnk 0 Pg 15

DDR2 - Dual Channel
1.8V - 64 Bits
533/667/800? MHz

J3100
J3200
DIMM
Pg30,31

Parallel Term
Pg 32

J6900/50
DC/Batt Conn
Pg 66

Power Supply
Pg 68-76

J5810/20/90 ALS SENS Pg 55

Temp Sense
CPU U5572 Pg 51
GPU U5500 Pg 52
Right Side U5550 Pg 52
Charger U??? Pg ??

U5920 Sudden Motion Detect Pg 56

Power Sense Pg 51, 115-120

J5600/10/50/60, J5720/30/50
Fan Conn Pg 53, 54

J9400
GPIO
DVI-I
MUX
U9120
Pg 79,81

J9000/10
Int Disp Conn
Pg 78

U9250/60 GPIO Pg 80
MUX
J9200

J9200 Source is the LVDS from the PEG based GPU.

x4 DMI
2.5 GHz

U6100/50
SPI Boot ROM
Pg 58

A B,0 BSA BSB ADC Fan Ser Prt
SMC
U4900 Pg 46

U6000
TPM
Pg 57

J5100
LPC Conn
Pg 48

Linda Fnc
Prt 80, Comm 1, SMC, FWH
Pg 124-130

J4510/20/30
SATA Conn
Pg 43

1.2 V / 1.5 GHz

SATA-0 SATA-1 SATA-2
SATA Pg 22
UATA Pg 22
PCI-E Pg 23
DMI Pg 23
CLnk 0 Pg 24
SPI Pg 23
LPC Pg 22
GPIOs Pg 24
USB Pg 23 1 2 3 4 5 6 7 8 9
SMB Pg 24
Core Pg 25
E-NET Pg 22
CLnk 1 Pg 24
PCI Pg 23
AZALIA Pg 22

U2300
SB-ICH8
Core 1.05V

J4400
UATA Conn
Pg 42

3.3 V
100 MHz

6 - x1
2.5 GHz

JB200 JB300 JB400
PCI-E Conns
Pg 93/4/5

UB100
PCI-E MUX
Pg 92

Ln1 Ln2 Ln3 Ln4 Ln5 Ln6

J4630 J4600
USB Connectors
Pg 44

J4710
Camera/IR
Pg 45

J4720
Bluetooth
Pg 45

J4700
Geyser
Trackpad/Keyboard
Pg 45

DIMM's J3100 J3200
Clk Gen U2900 UC500

33 MHz
32-Bit

U4000
TSB82AA2
FW-Link
Pg 38

100 MHz
8-Bit

U4100
TSB81BA3
FW-PHY
Pg 39

U3700
NINEVEH
E-NET
Pg 35

U6200
Audio Codec
Pg 59

U????
MDC
Pg ??

U6300/1
Line In Amp
Pg 60

U6400
Line Out Amp 1
Pg 61

U6500
Line Out Amp 2
Pg 62

U6600/10/20
Speaker Amps
Pg 63

J6800/1/2/3
Audio Conns
Pg 65

J3400
Mini PCI-E AirPort
Pg 33

JB500
PCI-E Conn
Pg 96

J4630
E-NET Conn
Pg 37

J4320 J4330
FireWire Conn
Pg 41

JB000
PCI Conn
Pg 91

System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	2	88

Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	3	88

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	4	88

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7931	PCBA,OROYA1,M75	M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG
630-7932	PCBA,OROYA2,M75	M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG
630-8659	PCBA,OROYA1,VRAM-HY,M75	M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX
630-8662	PCBA,OROYA2,VRAM-HY,M75	M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_YES,GPU_TMP401,HDCP,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU
M75_COMMON2	P1V8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS
M75_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128,VRAM_SAMSUNG,VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128,VRAM_HYNIX,VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5D]	CRITICAL	EEE_X5D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5E]	CRITICAL	EEE_X5E
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXS]	CRITICAL	EEE_XXS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3427	1	IC,MDC,SR,E0,ES2,2.0G,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3428	1	IC,MDC,SR,E0,ES2,2.2G,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3429	1	IC,MDC,SR,E0,ES2,2.4G,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0381	1	IC,NB,CRESTLINE,965PM,B0,ES2	U1400	CRITICAL	
338S0335	1	IC,SB,ICH8M,B0,ES1,ES2,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,LW PWR CLCK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2004	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BI-Tech magnetics
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 5 OF 88	

PROTO

See Perforce change notes for updates before Proto Release
12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0:
01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0:
01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0:
01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0:
01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0:
01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMOPTIONs and values for ISL9504B
01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0:
01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path
9.4.0:
01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787)
9.5.0:
01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMOPTIONs for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3_1V825 BOMOPTION to lift voltage at FB memories
10.0.0:
01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMOPTIONs to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	10.0.0
	SCALE NONE	SHT 6 OF 88	

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	PP5V_S0	7 8 27 42 47 52 57 58 59 65 76 78
TRUE	FAN_LT_PWM	52
TRUE	FAN_LT_TACH	52
TRUE	FAN_RT_PWM	52
TRUE	FAN_RT_TACH	52

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	45 46 56
TRUE	SMBUS_SMC_BSA_SCL	45 48 56 84
TRUE	SMBUS_SMC_BSA_SDA	45 48 56 84
TRUE	GND_BATT	56

LPC+ Debug Connector

FUNC_TEST

TRUE	PP3V42_G3H	6 20 34 43 45 46 47 56 58 78
TRUE	PP5V_S0	7 8 27 42 47 52 57 58 59 65 76 78
TRUE	LPC_AD<0>	23 45 47
TRUE	LPC_AD<1>	23 45 47
TRUE	LPC_FRAME_L	23 45 47
TRUE	PM_CLKRUN_L	25 45 47
TRUE	PCI_FW_GNT_L	24 38 47 83
TRUE	SMC_TMS	45 46 47
TRUE	DEBUG_RESET_L	28 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_MD1	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	FWH_INIT_L	47
TRUE	PCI_CLK33M_LPCPLUS	30 47 84
TRUE	LPC_AD<2>	23 45 47
TRUE	LPC_AD<3>	23 45 47
TRUE	INT_SERIRQ	25 45 47
TRUE	PM_SUS_STAT_L	25 45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_RESET_L	45 46 47
TRUE	SMC_NMI	45 47
TRUE	SMC_RX_L	43 45 46 47
TRUE	LINDACARD_GPIO	25 47

Left I/O Power Connector

FUNC_TEST

TRUE	PPBUS_G3H	8 40 49 56 57 58 59 60 61 62 63 74
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3_RTC	28
TRUE	GND	

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	45 49
TRUE	PP5V_S3	7 8 44 46 49 53 57 78
TRUE	PPVCORE_S0_NB_GFX	8 18 22 59
TRUE	PPVCORE_S0_CPU	8 11 12 49 58
TRUE	PPVCORE_GPU	8 49 67 74
TRUE	GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

Left ALS Connector

FUNC_TEST

TRUE	PP3V3_S3	8 36 38 48 50 53 54 57 78
TRUE	ALS_GAIN	45 53 78
TRUE	LTALS_OUT	53 78
TRUE	GND	

Left Clutch Barrel Connector

FUNC_TEST

TRUE	PP5V_S3	7 8 44 46 49 53 57 78
TRUE	USB_CAMERA_N	24 44 82
TRUE	USB_CAMERA_P	24 44 82
TRUE	PP5V_S3	7 8 44 46 49 53 57 78
TRUE	USB_WWAN_N	24 44 82
TRUE	USB_WWAN_P	24 44 82

Thermal Diode Connectors

FUNC_TEST

TRUE	REMTHMSNS_DX_P	51 87
TRUE	REMTHMSNS_DX_N	51
TRUE	CPUTHMSNS_D2_P	51 87
TRUE	CPUTHMSNS_D2_N	51

Other Func Test Points

FUNC_TEST

TRUE	PM_SYSRST_L	25 28 45
TRUE	SMC_ONOFF_L	45 46 78

System Validation TPs

FUNC_TEST

TRUE	CPU_PWRGD	10 13 23 79
TRUE	CPU_DPSLP_L	7 10 23 79
TRUE	PM_DPRSLPVR	16 25 58 79
TRUE	CPU_DPSLP_L	7 10 23 79
TRUE	PM_LAN_ENABLE	25 45
TRUE	PCI_RST_L	24 28
TRUE	PM_RSMRST_L	25 45
TRUE	PM_SB_PWROK	9 25 28
TRUE	SB_RTC_RST_L	23 28
TRUE	PM_STPCPU_L	25 29 30
TRUE	PM_STPPCI_L	25 29 30
TRUE	VR_PWRGD_CLKEN	25 28
TRUE	VR_PWRGOOD_DELAY	9 16 28 58
TRUE	FSB_CPURST_L	10 13 14 79
TRUE	FSB_CPUSLP_L	10 14 79
TRUE	FSB_DPWR_L	10 14 79
TRUE	NB_SB_SYNC_L	16 25

FUNC_TEST

TRUE	IMVP_VR_ON	45 58
TRUE	IMVP_DPRSLPVR	58 79
TRUE	PM_SLP_S3_L	25 35 36 40 45 49 57 62 65
TRUE	PM_S4_STATE_L	25 34 43 45 57 65
TRUE	PM_SLP_S5_L	25 45 46
TRUE	PM_ENET_EN	36 61 65
TRUE	P1V5P1V05S0_PGOOD	61 63 65
TRUE	CPU_DPRSTP_L	10 16 23 58 79
TRUE	IMVP6_VID<6..0>	12 58 79
TRUE	PLT_RST_L	24 28 77
	NB_RESET_L	16 28
TRUE	GPU_RESET_L	28 66
TRUE	SMC_LRESET_L	28 45
TRUE	CPU_STPCLK_L	10 23 79
TRUE	FSB_CLK_NB_P	14 29 30 84
TRUE	FSB_CLK_NB_N	14 29 30 84
TRUE	NB_CLKREQ_L	16 29
TRUE	NB_CLK100M_PCIE_P	16 29 30 84
TRUE	NB_CLK100M_PCIE_N	16 29 30 84
TRUE	NB_CLK96M_DOT_P	84
TRUE	NB_CLK96M_DOT_N	84
TRUE	NB_CLK100M_DPLLSS_P	16 22 29 30 84
TRUE	NB_CLK100M_DPLLSS_N	16 22 29 30 84
TRUE	CPU_THERMTRIP_R	23

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 79
TRUE	FSB_ADS_L	10 14 79
TRUE	FSB_ADSTB_L<1..0>	10 14 79
TRUE	FSB_BNR_L	10 14 79
TRUE	FSB_BREQ0_L	10 14 79
TRUE	FSB_D_L<63..0>	10 14 79
TRUE	FSB_DBSY_L	10 14 79
TRUE	FSB_DINV_L<3..0>	10 14 79
TRUE	FSB_DRDY_L	10 14 79
TRUE	FSB_DSTB_L_N<3..0>	10 14 79
TRUE	FSB_DSTB_L_P<3..0>	10 14 79
TRUE	FSB_HIT_L	10 14 79
TRUE	FSB_HITM_L	10 14 79
TRUE	FSB_LOCK_L	10 14 79
TRUE	FSB_REQ_L<4..0>	10 14 79

NB NO_TESTs

NO_TEST

TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16>	16

GPU NO_TESTs

NO_TEST

TRUE	LVDS_L_DATA_N<1>	73 77 86
TRUE	LVDS_L_DATA_N<2>	73 77 86
TRUE	LVDS_L_DATA_P<2>	73 77 86

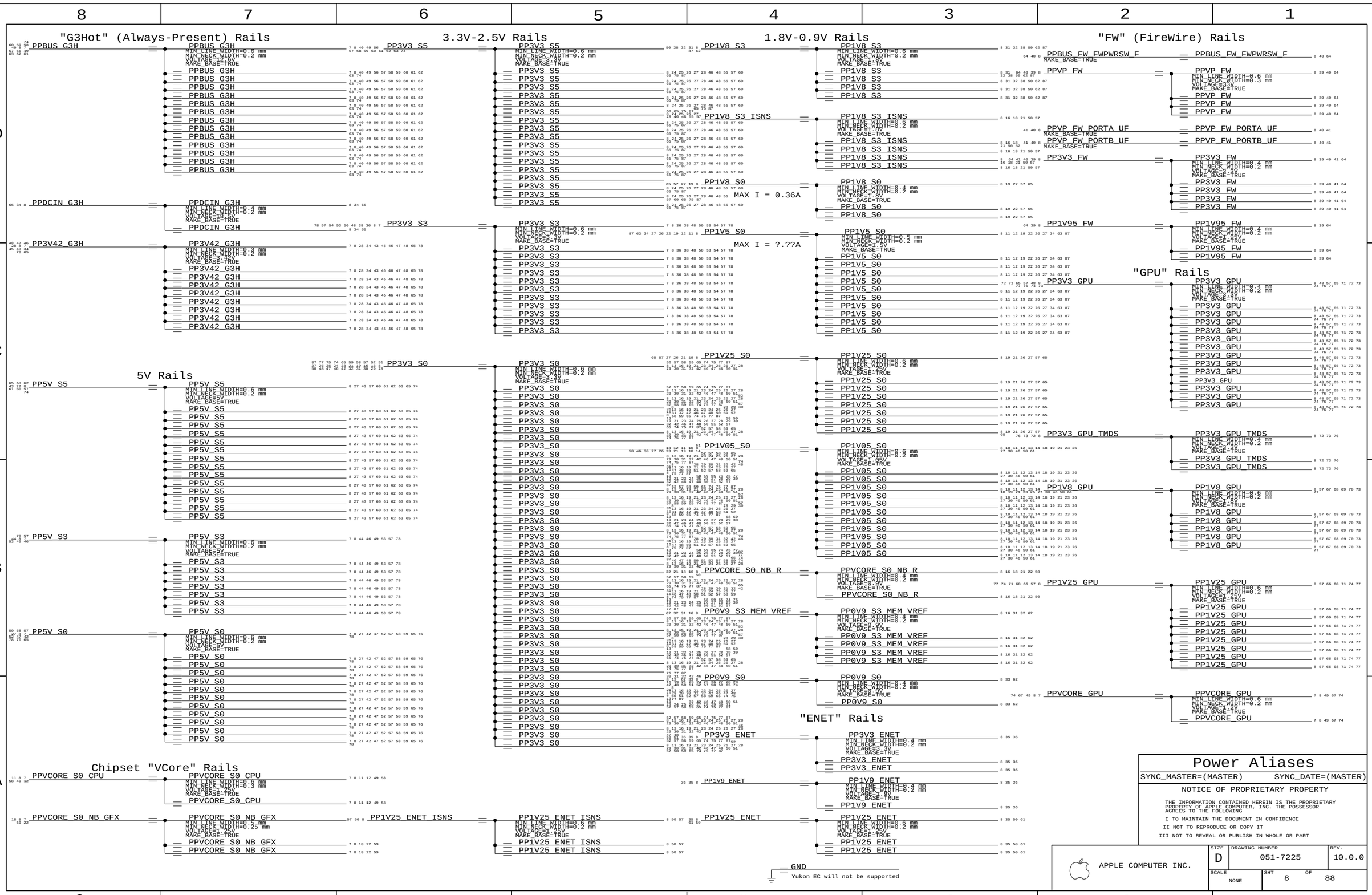
Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

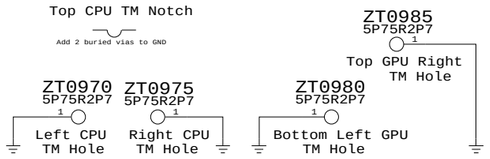
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	7	88



Thermal Module Holes



RAM Door (Torx) Holes

ZT0930 3P7R3P2 — GND

ZT0935 3P7R3P2 — GND

Frame Holes

ZT0920 3P2R2P7 — GND

ZT0940 3P7R3P2 — GND

Board Edge Notches (Can't be PTH)

ZT0945 HOLE-VIA-P5RP25 — GND

ZT0950 HOLE-VIA-P5RP25 — GND

ZT0955 3P2R2P7 — GND

ZT0965 3P2R2P7 — GND

Tooling Holes (Can't be PTH)

ZT0960 HOLE-VIA-P5RP25 — GND

ZT0990 HOLE-VIA-P5RP25 — GND_CHASSIS_DVI_TOP

Chassis GNDs

GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ GND_CHASSIS_DVI_TOP (9 76)

GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ GND_CHASSIS_DVI_BOT (9 76)

OMIT R0910 SHORT (NONE, NONE, NONE, 402)

GND_CHASSIS_ENET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ GND_CHASSIS_ENET (9 37 41)
→ GND_CHASSIS_ENET (9 37 41)
→ GND_CHASSIS_ENET (9 37 41)

GND_CHASSIS_RTUSB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ GND_CHASSIS_RTUSB (9 41 43)
→ GND_CHASSIS_RTUSB (9 41 43)

SH0925 0G-503040 SHLD-SM-LF

GND_CHASSIS_LEFTCLUTCH
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
→ GND_CHASSIS_LEFTCLUTCH (9 44)

PM_SB_PWROK (28 25 9 7) = PM_SB_PWROK (7 9 25 28) MAKE_BASE=TRUE

VR_PWRGOOD_DELAY (58 28 16 9 7) = VR_PWRGOOD_DELAY (7 9 16 28 58) MAKE_BASE=TRUE

SMC_SMS_INT (54 45 9) = SMC_SMS_INT (9 45 54) MAKE_BASE=TRUE

PEG_CLK100M_GPU_P (84 66 30 29 9) = PEG_CLK100M_GPU_P (9 29 30 66 84) MAKE_BASE=TRUE

PEG_CLK100M_GPU_N (84 66 30 29 9) = PEG_CLK100M_GPU_N (9 29 30 66 84) MAKE_BASE=TRUE

PM_ALL_NBGFX_PGOOD (77 59 9) = PM_ALL_NBGFX_PGOOD (9 59 77) MAKE_BASE=TRUE

GFX_VR_EN (59 16 9) = GFX_VR_EN (9 16 59) MAKE_BASE=TRUE

GFXIMVP6_VID<4..0> (59) = GFX_VID<4..0> (16) MAKE_BASE=TRUE

TP_MEM_A_A<15> (31 9) = TP_MEM_A_A<15> (9 31) MAKE_BASE=TRUE

TP_MEM_B_A<15> (32 9) = TP_MEM_B_A<15> (9 32) MAKE_BASE=TRUE

TP_USB_EXTCP (82 24 9) = TP_USB_EXTCP (9 24 82) MAKE_BASE=TRUE

TP_USB_EXTCN (82 24 9) = TP_USB_EXTCN (9 24 82) MAKE_BASE=TRUE

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	10.0.0
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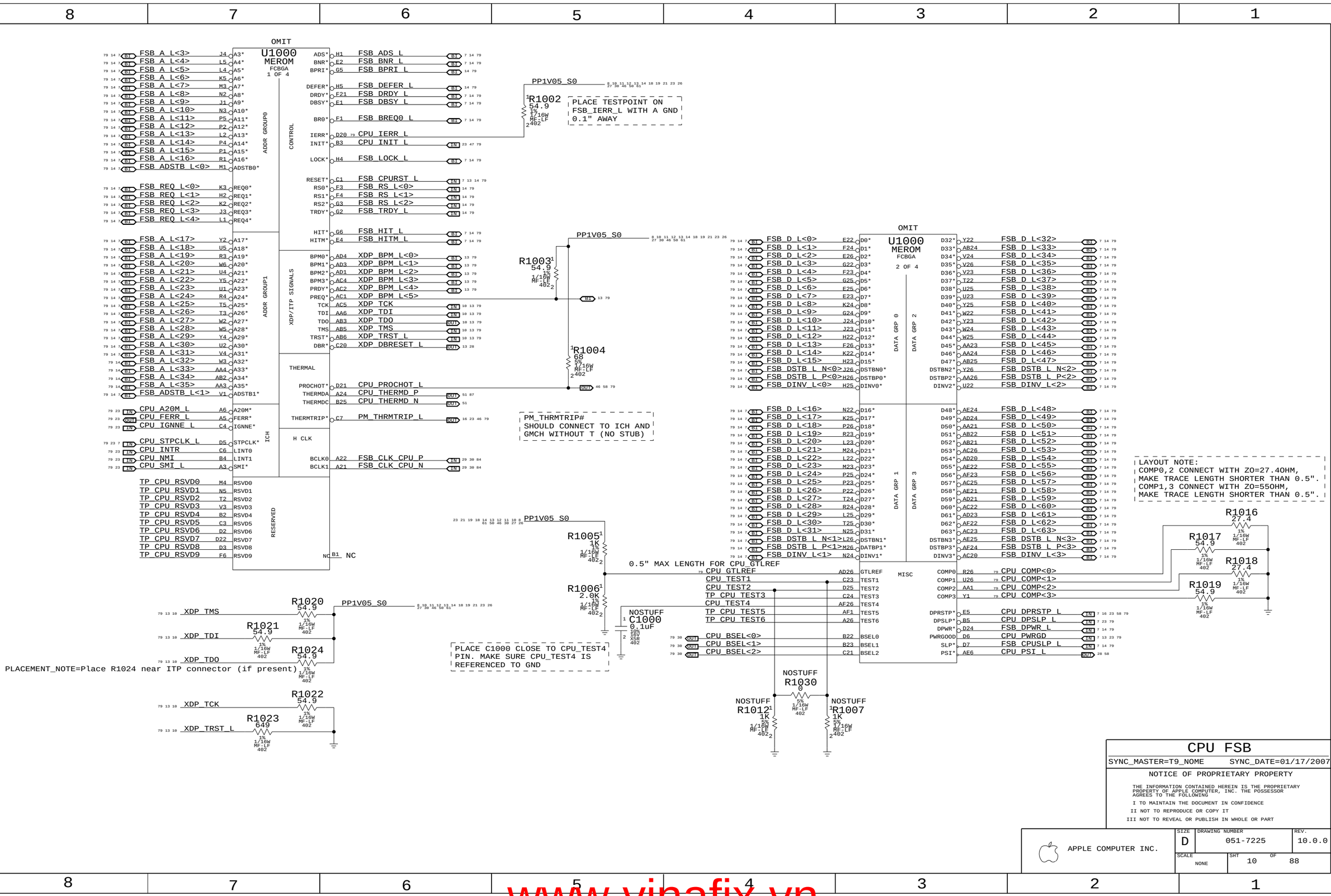
	NONE		



(CPU CORE POWER)

PPVCORE_S0_CPU 7 8 11 12 49 58

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

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U1000
MEROM
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VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AE20

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU IO POWER 1.05V)

PP1V05_S0 6 10 12 13 14 18 19 21 23 26 27 30 45 50 81

4500 mA (before VCC stable)
2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

PP1V5_S0 8 12 19 22 26 27 34 63 87

VCCA: B26 C26

130 mA

VID0	AD6	CPU_VID<0>	OUT 12 79
VID1	AF5	CPU_VID<1>	OUT 12 79
VID2	AE5	CPU_VID<2>	OUT 12 79
VID3	AF4	CPU_VID<3>	OUT 12 79
VID4	AE3	CPU_VID<4>	OUT 12 79
VID5	AF3	CPU_VID<5>	OUT 12 79
VID6	AE2	CPU_VID<6>	OUT 12 79
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 58 79
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 58 79

PPVCORE_S0_CPU 7 8 11 12 49 58

R1100 100 1% 1/16W MF-LF 402

PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101 100 1% 1/16W MF-LF 402

PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

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VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

CPU Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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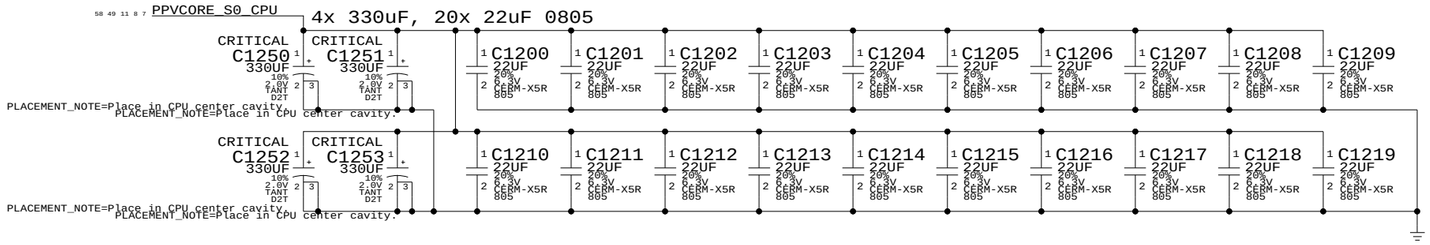
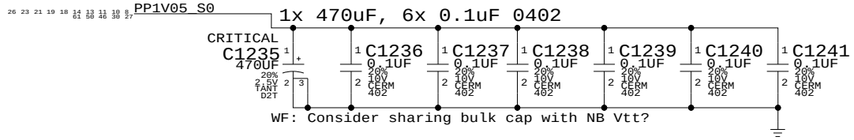
Current numbers from Merom for Santa Rosa EMTS, doc #22221.

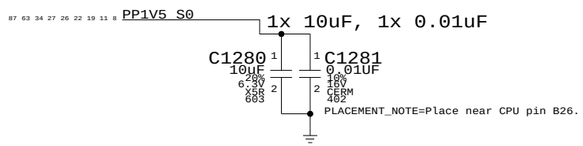
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU VCORE VID CONNECTIONS

79 11 CPU_VID<0..6> = IMVP6_VID<0..6> 7 58 79
MAKE_BASE=TRUE

CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

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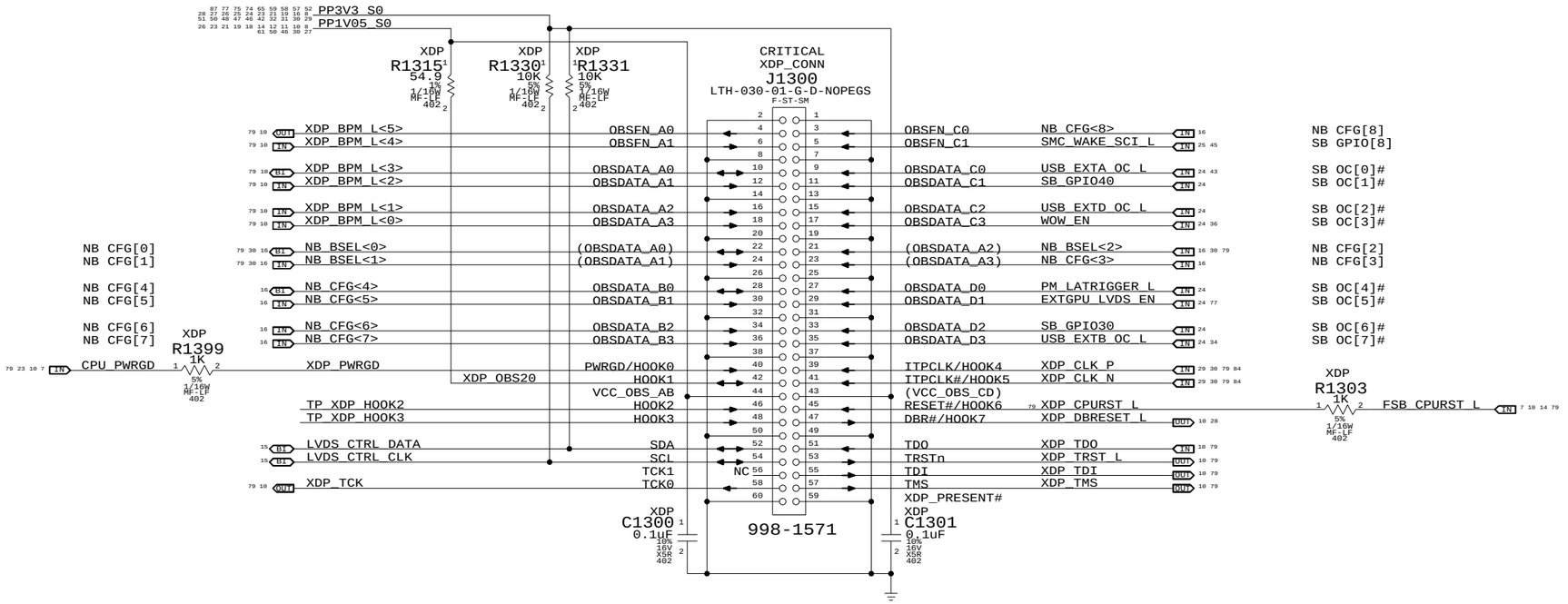
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE

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U1400
CRESTLINE
FCBGA
(1 OF 10)
HOST

FSB_D_L<0>	E2	H_D0*	H_A3*	J13	FSB_A_L<3>		
FSB_D_L<1>	G2	H_D1*	H_A4*	B11	FSB_A_L<4>		
FSB_D_L<2>	G7	H_D2*	H_A5*	C11	FSB_A_L<5>		
FSB_D_L<3>	M6	H_D3*	H_A6*	M11	FSB_A_L<6>		
FSB_D_L<4>	H7	H_D4*	H_A7*	C15	FSB_A_L<7>		
FSB_D_L<5>	H3	H_D5*	H_A8*	F16	FSB_A_L<8>		
FSB_D_L<6>	G4	H_D6*	H_A9*	L13	FSB_A_L<9>		
FSB_D_L<7>	F3	H_D7*	H_A10*	G17	FSB_A_L<10>		
FSB_D_L<8>	N8	H_D8*	H_A11*	C14	FSB_A_L<11>		
FSB_D_L<9>	H2	H_D9*	H_A12*	K16	FSB_A_L<12>		
FSB_D_L<10>	M10	H_D10*	H_A13*	B13	FSB_A_L<13>		
FSB_D_L<11>	N12	H_D11*	H_A14*	L16	FSB_A_L<14>		
FSB_D_L<12>	N9	H_D12*	H_A15*	J17	FSB_A_L<15>		
FSB_D_L<13>	H5	H_D13*	H_A16*	B14	FSB_A_L<16>		
FSB_D_L<14>	P13	H_D14*	H_A17*	K19	FSB_A_L<17>		
FSB_D_L<15>	K9	H_D15*	H_A18*	P15	FSB_A_L<18>		
FSB_D_L<16>	M2	H_D16*	H_A19*	R17	FSB_A_L<19>		
FSB_D_L<17>	W10	H_D17*	H_A20*	B16	FSB_A_L<20>		
FSB_D_L<18>	Y8	H_D18*	H_A21*	H20	FSB_A_L<21>		
FSB_D_L<19>	V4	H_D19*	H_A22*	L19	FSB_A_L<22>		
FSB_D_L<20>	M3	H_D20*	H_A23*	D17	FSB_A_L<23>		
FSB_D_L<21>	J1	H_D21*	H_A24*	M17	FSB_A_L<24>		
FSB_D_L<22>	N5	H_D22*	H_A25*	N16	FSB_A_L<25>		
FSB_D_L<23>	N3	H_D23*	H_A26*	J19	FSB_A_L<26>		
FSB_D_L<24>	W6	H_D24*	H_A27*	B18	FSB_A_L<27>		
FSB_D_L<25>	W9	H_D25*	H_A28*	E19	FSB_A_L<28>		
FSB_D_L<26>	N2	H_D26*	H_A29*	B17	FSB_A_L<29>		
FSB_D_L<27>	Y7	H_D27*	H_A30*	B15	FSB_A_L<30>		
FSB_D_L<28>	Y9	H_D28*	H_A31*	E17	FSB_A_L<31>		
FSB_D_L<29>	P4	H_D29*	H_A32*	C18	FSB_A_L<32>		
FSB_D_L<30>	W3	H_D30*	H_A33*	A19	FSB_A_L<33>		
FSB_D_L<31>	N1	H_D31*	H_A34*	B19	FSB_A_L<34>		
FSB_D_L<32>	AD12	H_D32*	H_A35*	N19	FSB_A_L<35>		
FSB_D_L<33>	AE3	H_D33*					
FSB_D_L<34>	AD9	H_D34*	H_ADS*	G12	FSB_ADS_L		
FSB_D_L<35>	AC9	H_D35*	H_ADSTB0*	H17	FSB_ADSTB_L<0>		
FSB_D_L<36>	AC7	H_D36*	H_ADSTB1*	G20	FSB_ADSTB_L<1>		
FSB_D_L<37>	AC14	H_D37*	H_BNR*	C8	FSB_BNR_L		
FSB_D_L<38>	AD11	H_D38*	H_BPRI*	E8	FSB_BPRI_L	OUT	
FSB_D_L<39>	AC11	H_D39*	H_BREQ*	F12	FSB_BREQ0_L		
FSB_D_L<40>	AB2	H_D40*	H_DEFER*	D6	FSB_DEFER_L	OUT	
FSB_D_L<41>	AD7	H_D41*	H_DBSY*	C10	FSB_DBSY_L		
FSB_D_L<42>	AB1	H_D42*	HPLL_CLK	AM5	FSB_CLK_NB_P	IN	
FSB_D_L<43>	Y3	H_D43*	HPLL_CLK*	AM7	FSB_CLK_NB_N	IN	
FSB_D_L<44>	AC6	H_D44*	H_DPWR*	H8	FSB_DPWR_L		
FSB_D_L<45>	AE2	H_D45*	H_DRDY*	K7	FSB_DRDY_L		
FSB_D_L<46>	AC5	H_D46*	H_HIT*	E4	FSB_HIT_L		
FSB_D_L<47>	AG3	H_D47*	H_HITM*	C6	FSB_HITM_L		
FSB_D_L<48>	AJ9	H_D48*	H_LOCK*	G10	FSB_LOCK_L		
FSB_D_L<49>	AH8	H_D49*	H_TRDY*	B7	FSB_TRDY_L	OUT	
FSB_D_L<50>	AJ14	H_D50*					
FSB_D_L<51>	AE9	H_D51*					
FSB_D_L<52>	AE11	H_D52*	H_DINV0*	K5	FSB_DINV_L<0>		
FSB_D_L<53>	AH12	H_D53*	H_DINV1*	L2	FSB_DINV_L<1>		
FSB_D_L<54>	AJ5	H_D54*	H_DINV2*	AD13	FSB_DINV_L<2>		
FSB_D_L<55>	AH5	H_D55*	H_DINV3*	AE13	FSB_DINV_L<3>		
FSB_D_L<56>	AJ6	H_D56*					
FSB_D_L<57>	AE7	H_D57*	H_DSTBN0*	M7	FSB_DSTB_L_N<0>		
FSB_D_L<58>	AJ7	H_D58*	H_DSTBN1*	K3	FSB_DSTB_L_N<1>		
FSB_D_L<59>	AJ2	H_D59*	H_DSTBN2*	AD2	FSB_DSTB_L_N<2>		
FSB_D_L<60>	AE5	H_D60*	H_DSTBN3*	AH11	FSB_DSTB_L_N<3>		
FSB_D_L<61>	AJ3	H_D61*	H_DSTBP0*	L7	FSB_DSTB_L_P<0>		
FSB_D_L<62>	AH2	H_D62*	H_DSTBP1*	K2	FSB_DSTB_L_P<1>		
FSB_D_L<63>	AH13	H_D63*	H_DSTBP2*	AC2	FSB_DSTB_L_P<2>		
			H_DSTBP3*	AJ10	FSB_DSTB_L_P<3>		
NB_FSB_SWING	B3	H_SWING					
NB_FSB_RCOMP	C2	H_RCOMP	H_REQ0*	M14	FSB_REQ_L<0>		
NB_FSB_SCOMP	W1	H_SCOMP	H_REQ1*	E13	FSB_REQ_L<1>		
NB_FSB_SCOMP_L	W2	H_SCOMP*	H_REQ2*	A11	FSB_REQ_L<2>		
FSB_CPURST_L	B6	H_CPURST*	H_REQ3*	H13	FSB_REQ_L<3>		
FSB_CPUSLP_L	E5	H_CPUSLP*	H_REQ4*	B12	FSB_REQ_L<4>		
NB_FSB_VREF	B9	H_AVREF					
	A9	H_DVREF	H_RS0*	E12	FSB_RS_L<0>	OUT	
			H_RS1*	D7	FSB_RS_L<1>	OUT	
			H_RS2*	D8	FSB_RS_L<2>	OUT	

PP1V05_S0

R1421 54.9 1% 1/16W MF-LF 402
R1420 54.9 1% 1/16W MF-LF 402
R1410 221 1% 1/16W MF-LF 402
R1425 1K 1% 1/16W MF-LF 402
R1426 2.0K 1% 1/16W MF-LF 402
C1425 0.1uF 10% 10V X5R 402
R1415 24.9 1% 1/16W MF-LF 402
R1411 100 1% 1/16W MF-LF 402
C1410 0.1uF 10% 10V X5R 402

NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

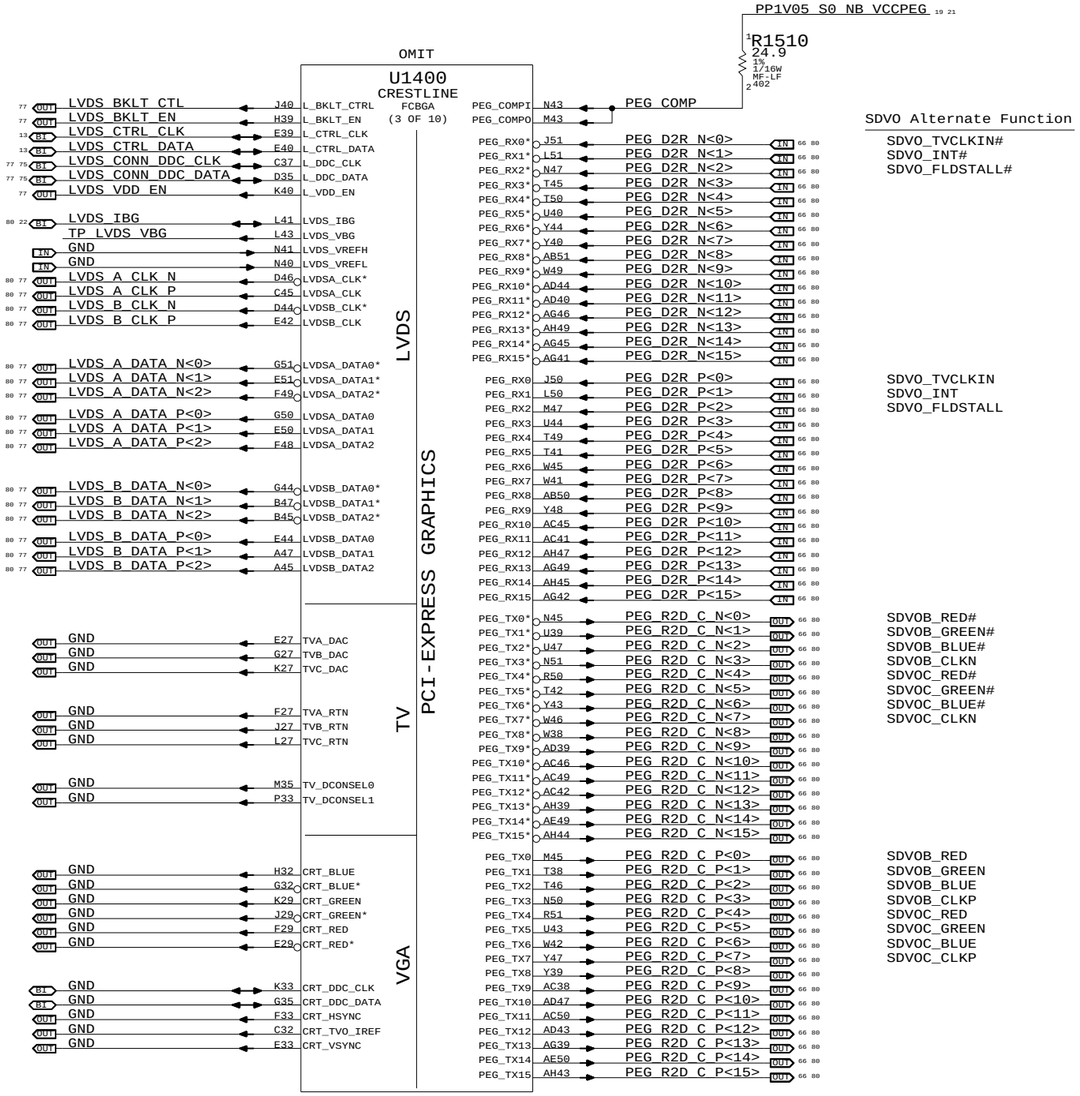
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 15 OF 88	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

PP3V3_S0 52 57 58 59 65 74 75 77 87 8 13 16 19 21 23 24 25 26 27 28 29 30 31 32 42 46 47 48 50 51
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

PP3V3_S0 52 57 58 59 65 74 75 77 87 8 13 16 19 21 23 24 25 26 27 28 29 30 31 32 42 46 47 48 50 51
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

PP3V3_S0 97 77 76 74 65 59 58 57 55 31 56 48 47 46 42 32 31 30 29 28
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402
PM_EXTTS_L<0> 45 31 IN
PM_EXTTS_L<1> 45 32 IN

OMIT

U1400
CRESTLINE
FCBGA
(2 OF 10)

TP_NB_RSVD<1>	P36	RSVD1		
TP_NB_RSVD<2>	P37	RSVD2		
TP_NB_RSVD<3>	R35	RSVD3		
TP_NB_RSVD<4>	N35	RSVD4		
TP_NB_RSVD<5>	AR12	RSVD5		
TP_NB_RSVD<6>	AR13	RSVD6		
TP_NB_RSVD<7>	AM12	RSVD7		
TP_NB_RSVD<8>	AN13	RSVD8		
TP_NB_RSVD<9>	J12	RSVD9		
TP_NB_RSVD<10>	AR37	RSVD10	RSVD	
TP_NB_RSVD<11>	AM36	RSVD11		
TP_NB_RSVD<12>	AL36	RSVD12		
TP_NB_RSVD<13>	AM37	RSVD13		
TP_NB_RSVD<14>	D20	RSVD14		
TP_NB_RSVD<20>	H10	RSVD20		
TP_NB_RSVD<21>	B51	RSVD21		
TP_NB_RSVD<22>	BJ20	RSVD22		
TP_NB_RSVD<23>	BK22	RSVD23		
TP_NB_RSVD<24>	BF19	RSVD24		
TP_NB_RSVD<25>	BH20	RSVD25		
TP_NB_RSVD<26>	BK18	RSVD26		
TP_NB_RSVD<27>	BJ18	RSVD27		
TP_MEM_CLKP2	BF23	SM_CK2	DDR MUXING	
TP_MEM_CLKN2	BG23	SM_CK2*		
TP_MEM_CLKP5	BC23	SM_CK5		
TP_MEM_CLKN5	BD24	SM_CK5*		
MEM_A_A<14> 81 33 31 OUT	BJ29	SA_MA14		
MEM_B_A<14> 81 33 32 OUT	BE24	SB_MA14		
TP_NB_RSVD<34>	BH39	RSVD34		
TP_NB_RSVD<35>	AW20	RSVD35		
TP_NB_RSVD<36>	BK20	RSVD36		
TP_LVDS_A_DATAN3	C48	RSVD37		
TP_LVDS_A_DATAP3	D47	RSVD38		
TP_LVDS_B_DATAN3	B44	RSVD39		
TP_LVDS_B_DATAP3	C44	RSVD40		
TP_NB_RSVD<41>	A35	RSVD41		
TP_NB_RSVD<42>	B37	RSVD42		
TP_NB_RSVD<43>	B36	RSVD43		
TP_NB_RSVD<44>	B34	RSVD44		
TP_NB_RSVD<45>	C34	RSVD45		
NB_BSEL<0> 79 30 13 IN	P27	CFG0	CFG	
NB_BSEL<1> 79 30 13 IN	N27	CFG1		
NB_BSEL<2> 79 30 13 IN	N24	CFG2		
NB_CFG<3> 13 OUT	C21	CFG3	IPU	
NB_CFG<4> 13 B1	C23	CFG4	IPU	
NB_CFG<5> 16 13 B1	F23	CFG5	IPU	
NB_CFG<6> 13 OUT	N23	CFG6	IPU	
NB_CFG<7> 13 OUT	G23	CFG7	IPU	
NB_CFG<8> 13 OUT	J20	CFG8	IPU	
NB_CFG<9> 16	C20	CFG9	IPU	
TP_NB_CFG<10>	R24	CFG10	IPU	
TP_NB_CFG<11>	L23	CFG11	IPU	
TP_NB_CFG<12>	J23	CFG12	IPU	
TP_NB_CFG<13>	E23	CFG13	IPU	
TP_NB_CFG<14>	E20	CFG14	IPU	
TP_NB_CFG<15>	K23	CFG15	IPU	
NB_CFG<16> 16	M20	CFG16	IPU	
TP_NB_CFG<17>	M24	CFG17	IPU	
TP_NB_CFG<18>	L32	CFG18	IPD	
NB_CFG<19> 16	N33	CFG19	IPD	
NB_CFG<20> 16	L35	CFG20	IPD	
PM_BMBUSY_L 25 OUT	G41	PM_BM_BUSY*	PM	
CPU_DPRSTP_L 79 58 23 10 7 IN	L39	PM_DPRSTP*		
	L36	PM_EXT_TS0*		
	J36	PM_EXT_TS1*		
VR_PWRGOOD_DELAY 58 28 16 9 7 IN	AW49	PWROK		
NB_RESET_L 28 7 IN	AV20	RSTIN*		
PM_THRMTRIP_L 79 46 23 10 OUT	N20	THERMTRIP*		
PM_DPRSLPVR 79 58 25 7 IN	G36	DPRSLPVR		
TP_NB_NC<1> 7	BJ51	NC1	NC	
TP_NB_NC<2> 7	BK51	NC2		
TP_NB_NC<3> 7	BK50	NC3		
TP_NB_NC<4> 7	BL50	NC4		
TP_NB_NC<5> 7	BL49	NC5		
TP_NB_NC<6> 7	BL3	NC6		
TP_NB_NC<7> 7	BL2	NC7		
TP_NB_NC<8> 7	BK1	NC8		
TP_NB_NC<9> 7	BJ1	NC9		
TP_NB_NC<10> 7	E1	NC10		
TP_NB_NC<11> 7	A5	NC11		
TP_NB_NC<12> 7	C51	NC12		
TP_NB_NC<13> 7	B50	NC13		
TP_NB_NC<14> 7	A50	NC14		
TP_NB_NC<15> 7	A49	NC15		
TP_NB_NC<16> 7	BK2	NC16		

SM_CK0	AV29	MEM_CLK_P<0>	OUT 31 81	
SM_CK1	BB23	MEM_CLK_P<1>	OUT 31 81	
SM_CK3	BA25	MEM_CLK_P<3>	OUT 32 81	
SM_CK4	AV23	MEM_CLK_P<4>	OUT 32 81	
SM_CK0*	AW30	MEM_CLK_N<0>	OUT 31 81	
SM_CK1*	BA23	MEM_CLK_N<1>	OUT 31 81	
SM_CK3*	AW25	MEM_CLK_N<3>	OUT 32 81	
SM_CK4*	AW23	MEM_CLK_N<4>	OUT 32 81	
SM_CKE0	BE29	MEM_CKE<0>	OUT 31 33 81	
SM_CKE1	AY32	MEM_CKE<1>	OUT 31 33 81	
SM_CKE3	BD39	MEM_CKE<3>	OUT 32 33 81	
SM_CKE4	BG37	MEM_CKE<4>	OUT 32 33 81	
SM_CS0*	BG20	MEM_CS_L<0>	OUT 31 33 81	
SM_CS1*	BK16	MEM_CS_L<1>	OUT 31 33 81	
SM_CS2*	BG16	MEM_CS_L<2>	OUT 32 33 81	
SM_CS3*	BE13	MEM_CS_L<3>	OUT 32 33 81	
SM_ODT0	BH18	MEM_ODT<0>	OUT 31 33 81	
SM_ODT1	BJ15	MEM_ODT<1>	OUT 31 33 81	
SM_ODT2	BJ14	MEM_ODT<2>	OUT 32 33 81	
SM_ODT3	BE16	MEM_ODT<3>	OUT 32 33 81	
SM_RCOMP	BL15	MEM_RCOMP		
SM_RCOMP*	BK14	MEM_RCOMP_L		
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH		
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL		
SM_VREF0	AR49	PP0V9_S3_MEM_VREF	IN 8 16 31 32 62	
SM_VREF1	AW4	PP0V9_S3_MEM_VREF	IN 8 16 31 32 62	
DPLL_REF_CLK	B42	GND		
DPLL_REF_CLK*	C42	PPVCORE_S0_NB_R	IN 8 18 21 22 50	
DPLL_REF_SSCLK	H48	NB_CLK100M_DPLLSS_P	IN 7 22 29 30 84	
DPLL_REF_SSCLK*	H47	NB_CLK100M_DPLLSS_N	IN 7 22 29 30 84	
PEG_CLK	K44	NB_CLK100M_PCIE_P	IN 7 29 30 84	
PEG_CLK*	K45	NB_CLK100M_PCIE_N	IN 7 29 30 84	
DMI_RXN0	AN47	DMI_S2N_N<0>	IN 24 80	
DMI_RXN1	AJ38	DMI_S2N_N<1>	IN 24 80	
DMI_RXN2	AN42	DMI_S2N_N<2>	IN 24 80	
DMI_RXN3	AN46	DMI_S2N_N<3>	IN 24 80	
DMI_RXP0	AM47	DMI_S2N_P<0>	IN 24 80	
DMI_RXP1	AJ39	DMI_S2N_P<1>	IN 24 80	
DMI_RXP2	AN41	DMI_S2N_P<2>	IN 24 80	
DMI_RXP3	AN45	DMI_S2N_P<3>	IN 24 80	
DMI_TXN0	AJ46	DMI_N2S_N<0>	OUT 24 80	
DMI_TXN1	AJ41	DMI_N2S_N<1>	OUT 24 80	
DMI_TXN2	AM40	DMI_N2S_N<2>	OUT 24 80	
DMI_TXN3	AM44	DMI_N2S_N<3>	OUT 24 80	
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 24 80	
DMI_TXP1	AJ42	DMI_N2S_P<1>	OUT 24 80	
DMI_TXP2	AM39	DMI_N2S_P<2>	OUT 24 80	
DMI_TXP3	AM43	DMI_N2S_P<3>	OUT 24 80	
		GND	OUT	
GFX_VID0	E35	GFX_VID<1>	OUT 9	
GFX_VID1	A39	GFX_VID<2>	OUT 9	
GFX_VID2	C38	GFX_VID<3>	OUT 9	
GFX_VID3	B39	GFX_VID<4>	OUT 9	
GFX_VR_EN	E36	GFX_VR_EN	OUT 9 59	
CL_CLK	AM49	CLINK_NB_CLK	B1 25 83	
CL_DATA	AK50	CLINK_NB_DATA	B1 25 83	
CL_PWROK	AT43	VR_PWRGOOD_DELAY	IN 7 9 16 28 58	
CL_RST*	AN49	CLINK_NB_RESET_L	OUT 25 83	
CL_VREF	AM50	NB_CLINK_VREF	83	
SDVO_CTRL_CLK	H35	GND	B1	
SDVO_CTRL_DATA	K36	GND	B1	
CLKREQ*	G39	NB_CLKREQ_L	OUT 7 29	
ICH_SYNC*	G40	NB_SB_SYNC_L	OUT 7 25	
TEST1	A37	NB_TEST1		
TEST2	R32	NB_TEST2		

Clk used for PEG and DMI

C1615 0.1uF 20% 10V CERM 402
C1616 0.1uF 20% 10V CERM 402

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

PP1V8_S3_ISNS 57 50 21 18 8
R1610 20 1% 1/16W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/16W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/16W MF-LF 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

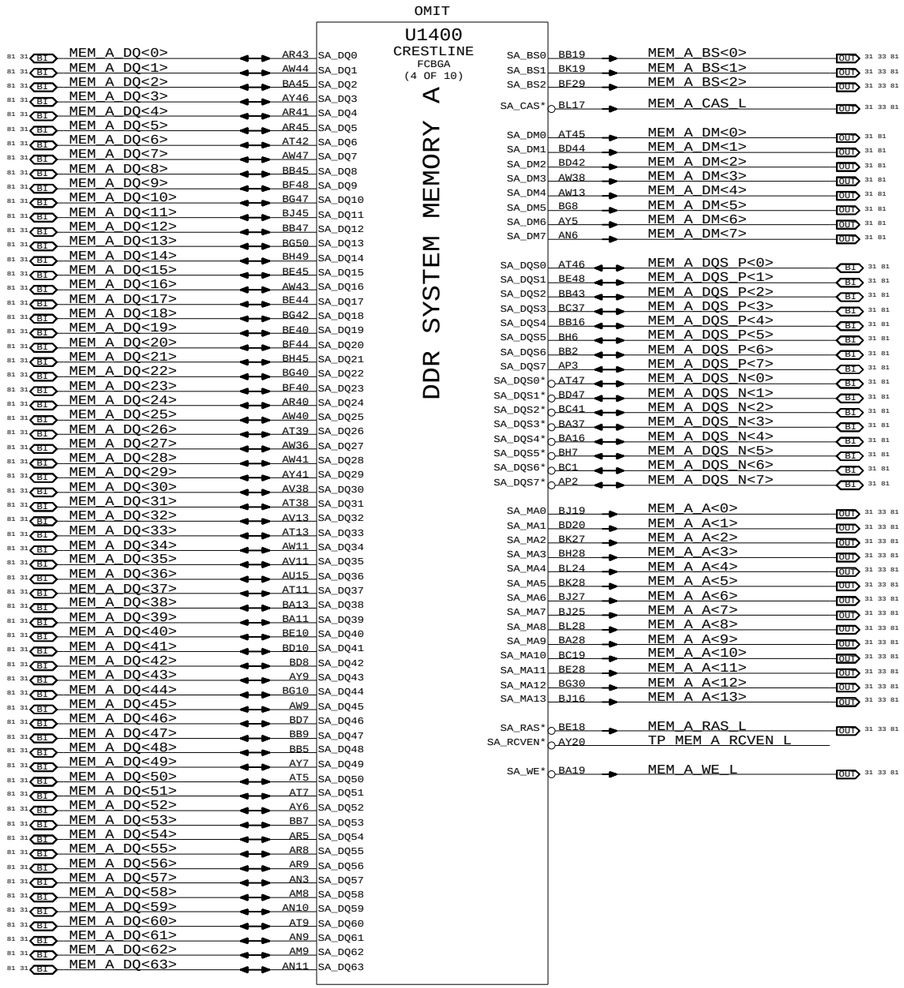
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

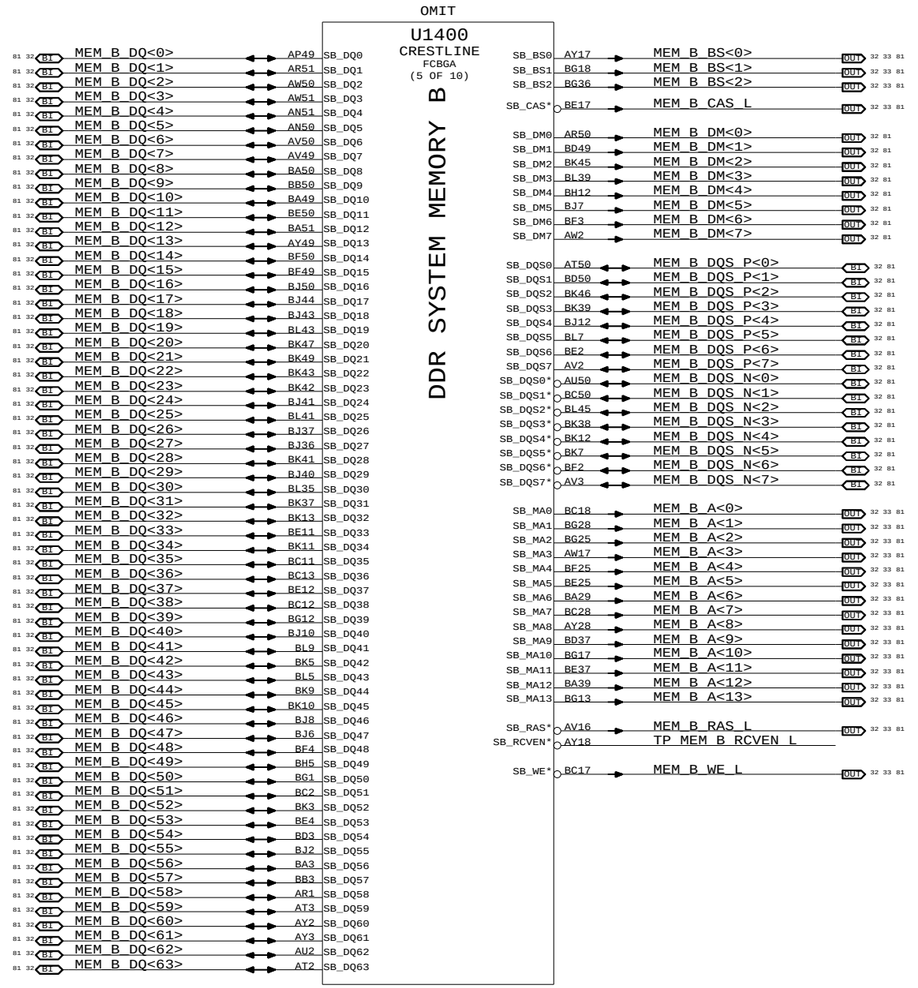
NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 16 OF 88	





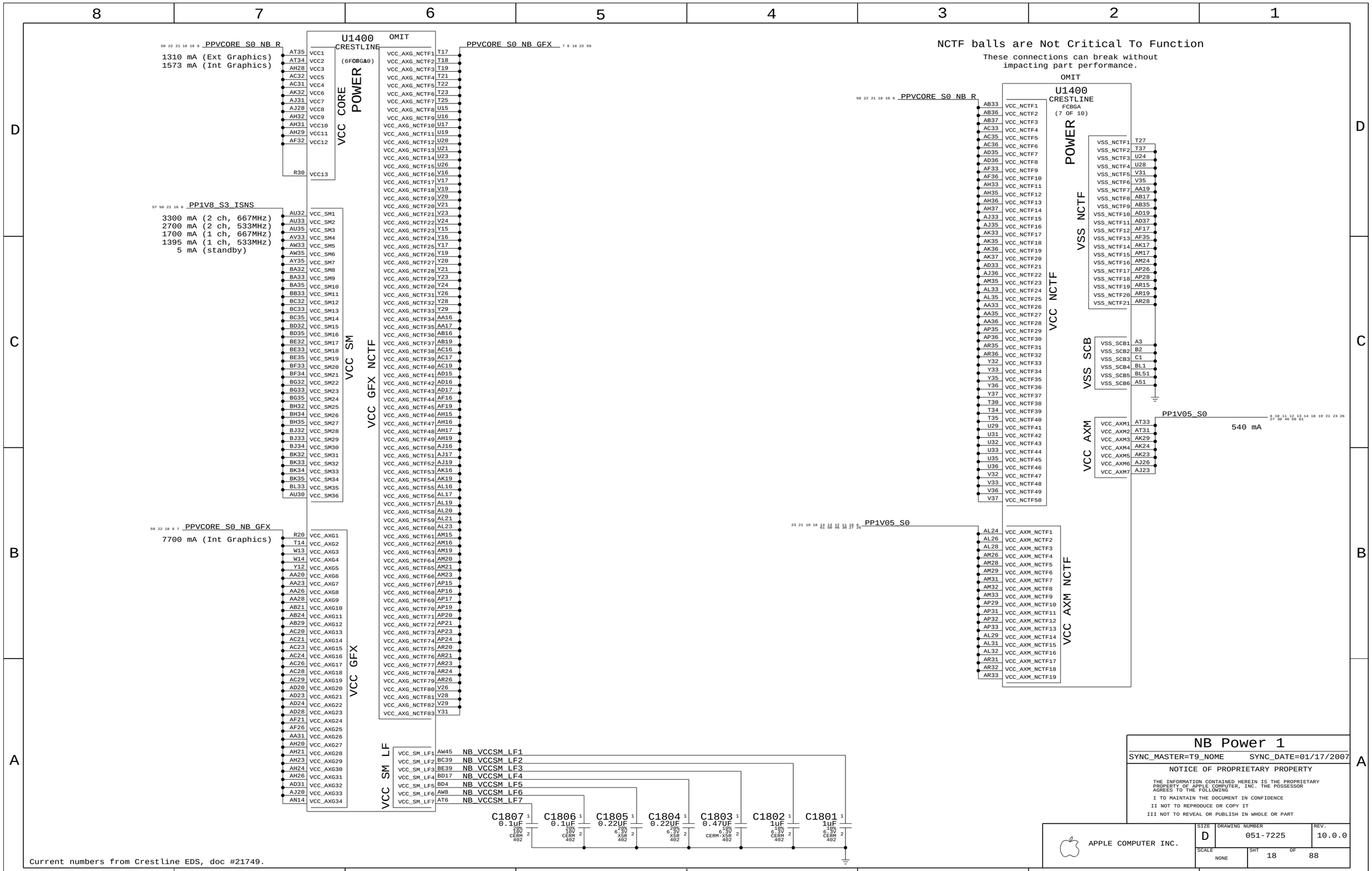
NB DDR2 Interfaces

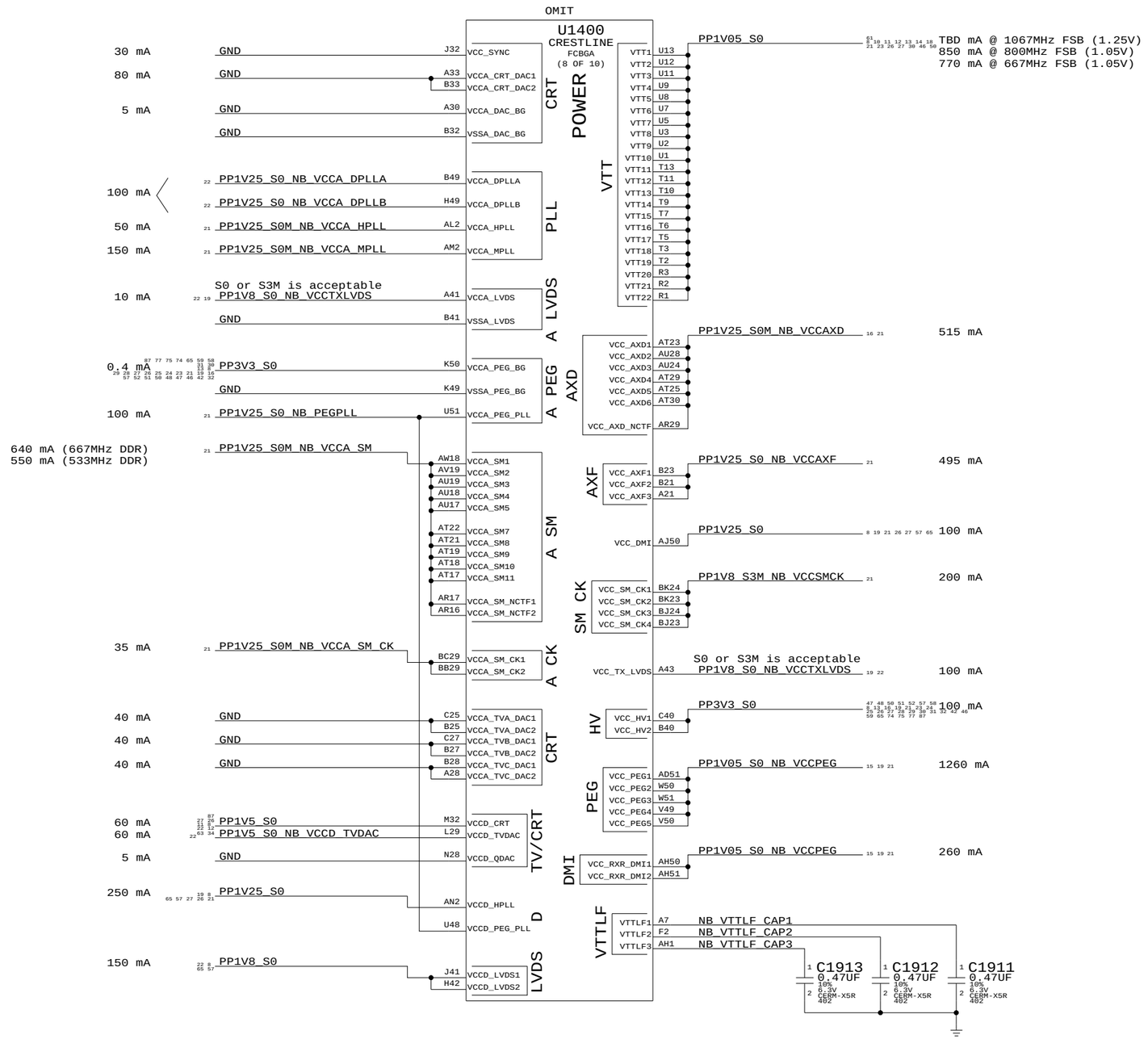
SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	17	88





Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	19	88

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218	TDE_FORCE VSS303	T31
F50	VSS219		
G1	VSS220	TDB_FORCE VSS304	T33
G13	VSS221		
G16	VSS222	TDB_SENSE VSS305	R28
G19	VSS223		
G24	VSS224		
G28	VSS225	VSS306	AA32
G29	VSS226	VSS307	AB32
G33	VSS227	VSS308	AD32
G42	VSS228	VSS309	AF28
G45	VSS229	VSS310	AF29
G48	VSS230	VSS311	AT27
G8	VSS231	VSS312	AV25
H24	VSS232	VSS313	H50
H28	VSS233		
H4	VSS234		
H45	VSS235		
J11	VSS236		
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 — GND

NOTE: TDE = _P

TDE_FORCE T31 — GND

TDB_FORCE T33 — GND

NOTE: TDB = _N

TDB_SENSE R28 — GND

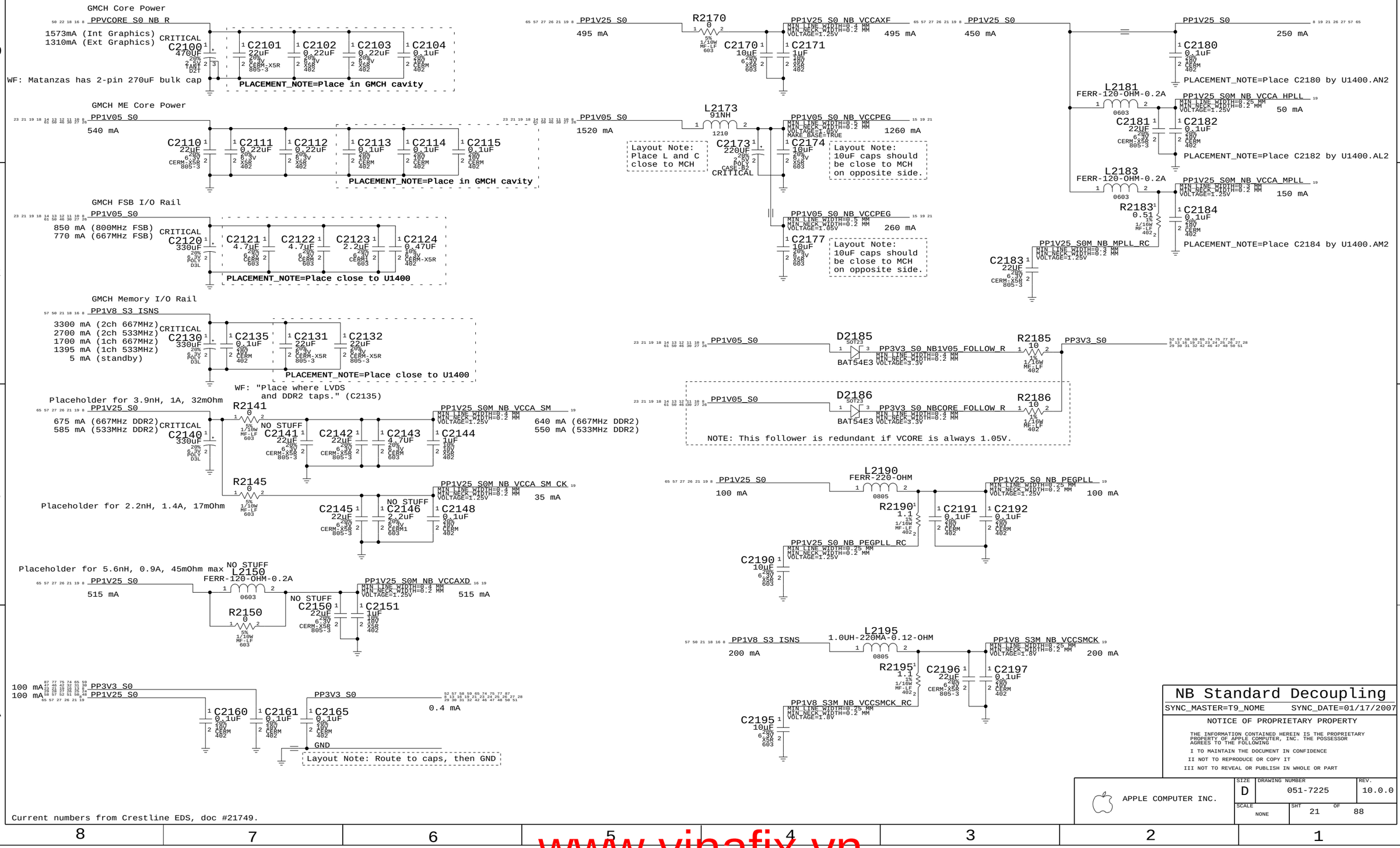
NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	20	88



NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.

87 PP1V5_S0
19 12 11 8 7 63 34 27 26
65 mA

C2201
22000pF-1000mA
10V
NFM18
1 3 2

C2200
0.1uF
20%
10V
2 CERM
402

PP1V5_S0_NB_VCCD_TVDAC 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
60 mA

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND

Crestline LVDS Support

80 15 LVDS_IBG

R2299 1
2.37K
1%
1/10W
MF-LF
402 2

GND
GND

GND
GND
GND
GND
GND
GND
GND
GND

50 22 21 18 16 8 PPVCORE_S0_NB_R
GND
PPVCORE_S0_NB_R 8 16 18 21 22 50

84 30 29 22 16 7 NB_CLK100M_DPLLSS_P — NB_CLK100M_DPLLSS_P 7 16 22 29 30 84
84 30 29 22 16 7 NB_CLK100M_DPLLSS_N — NB_CLK100M_DPLLSS_N 7 16 22 29 30 84

GMCH Graphics Core Power

59 18 8 7 PPVCORE_S0_NB_GFX
7700 mA

CRITICAL
C2210 1
470UF
20%
2.5V 2
TANT 3
D2T

CRITICAL
C2211 1
470UF
20%
2.5V 2
TANT 3
D2T

CRITICAL
C2212 1
22UF
20%
6.3V 2
CERM-X5R
805-3

C2213 1
10UF
20%
6.3V 2
X5R
603

C2214 1
1UF
10%
6.3V 2
CERM
402

C2215 1
0.47UF
10%
6.3V 2
CERM-X5R
402

C2216 1
0.1UF
20%
16V 2
CERM
402

C2217 1
0.1UF
20%
16V 2
CERM
402

PLACEMENT_NOTE=Place in GMCH cavity

65 57 22 19 8 PP1V8_S0
260 mA

L2220
1.0UH-0.5A
1 2
1210

C2220 1
220UF
20%
6.3V 2
POLY
CASE-D3L
CRITICAL

C2221 1
0.001UF
10%
50V 2
CERM
402

PP1V8_S0_NB_VCCTXLVDS 19
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
110 mA

C2223 1
0.001UF
10%
50V 2
CERM
402

GND

Layout Note: Route to cap, then GND

PP1V8_S0 8 19 22 57 65
150 mA

C2226 1
1UF
10%
6.3V 2
CERM
402

CRITICAL
U2265
TPS731125
SOT23-5
1 IN
3 EN
5 OUT
4 NR/FB
2 GND

65 57 22 19 8 PP1V8_S0
(1.7V - 5.5V)
100 mA

Vout = 1.25V (Factory Programmed)

PP1V25_S0_NB_DPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
P1V25S0NBDPLL_NR

C2265 1
1UF
10%
6.3V 2
CERM
402

C2266 1
0.01UF
10%
16V 2
CERM
402

100 mA

NO STUFF
R2261
4.7
5%
1/16W
MF-LF
402

PP1V25_S0_NB_VCCA_DPLLA 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2261 1
0.1UF
20%
16V 2
CERM
402
NO STUFF

R2262
4.7
5%
1/16W
MF-LF
402

PP1V25_S0_NB_VCCA_DPLLB 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2260 1
10UF
20%
6.3V 2
X5R
603

C2262 1
0.1UF
20%
16V 2
CERM
402

100 mA

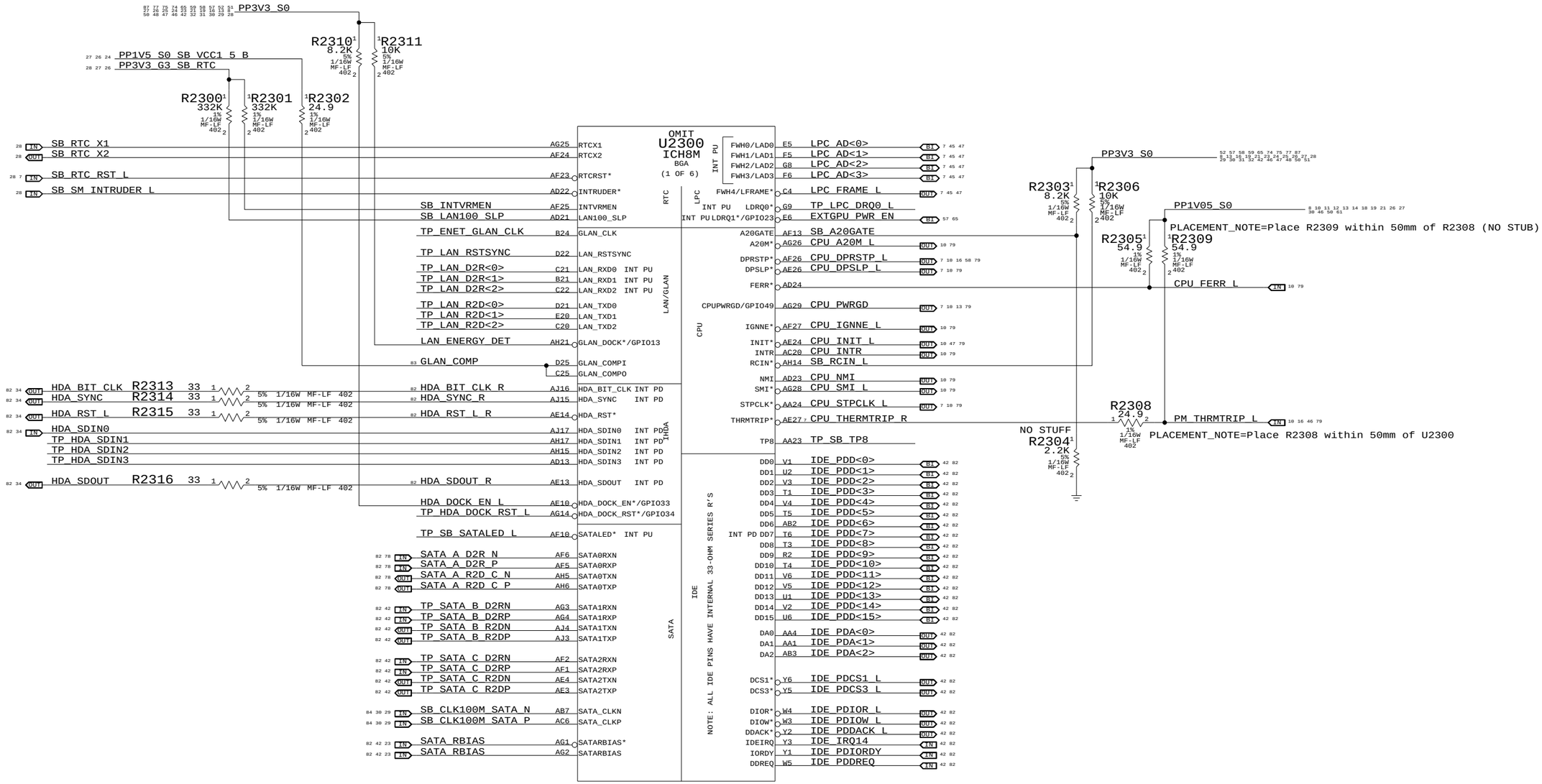
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 22 OF 88	



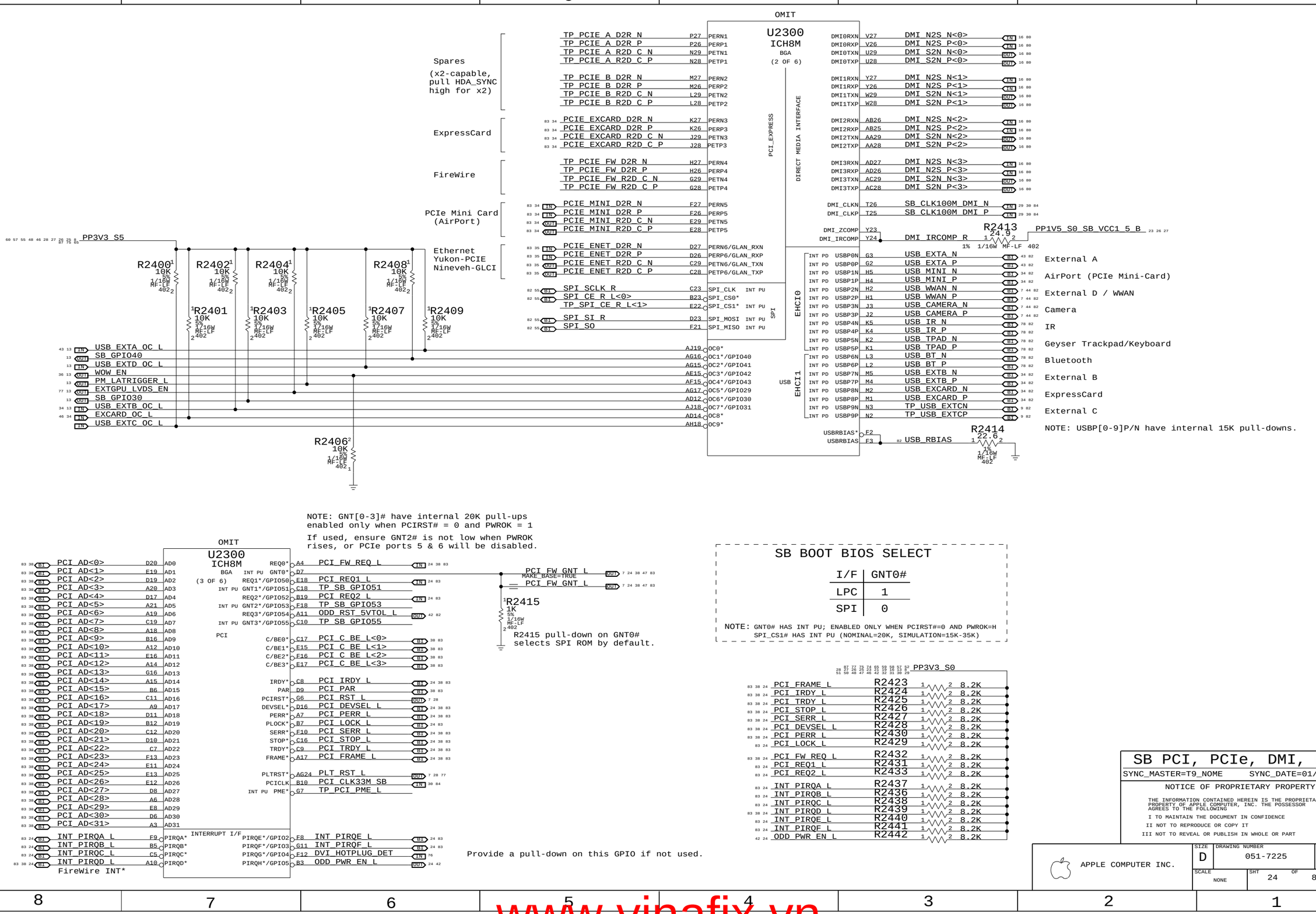
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

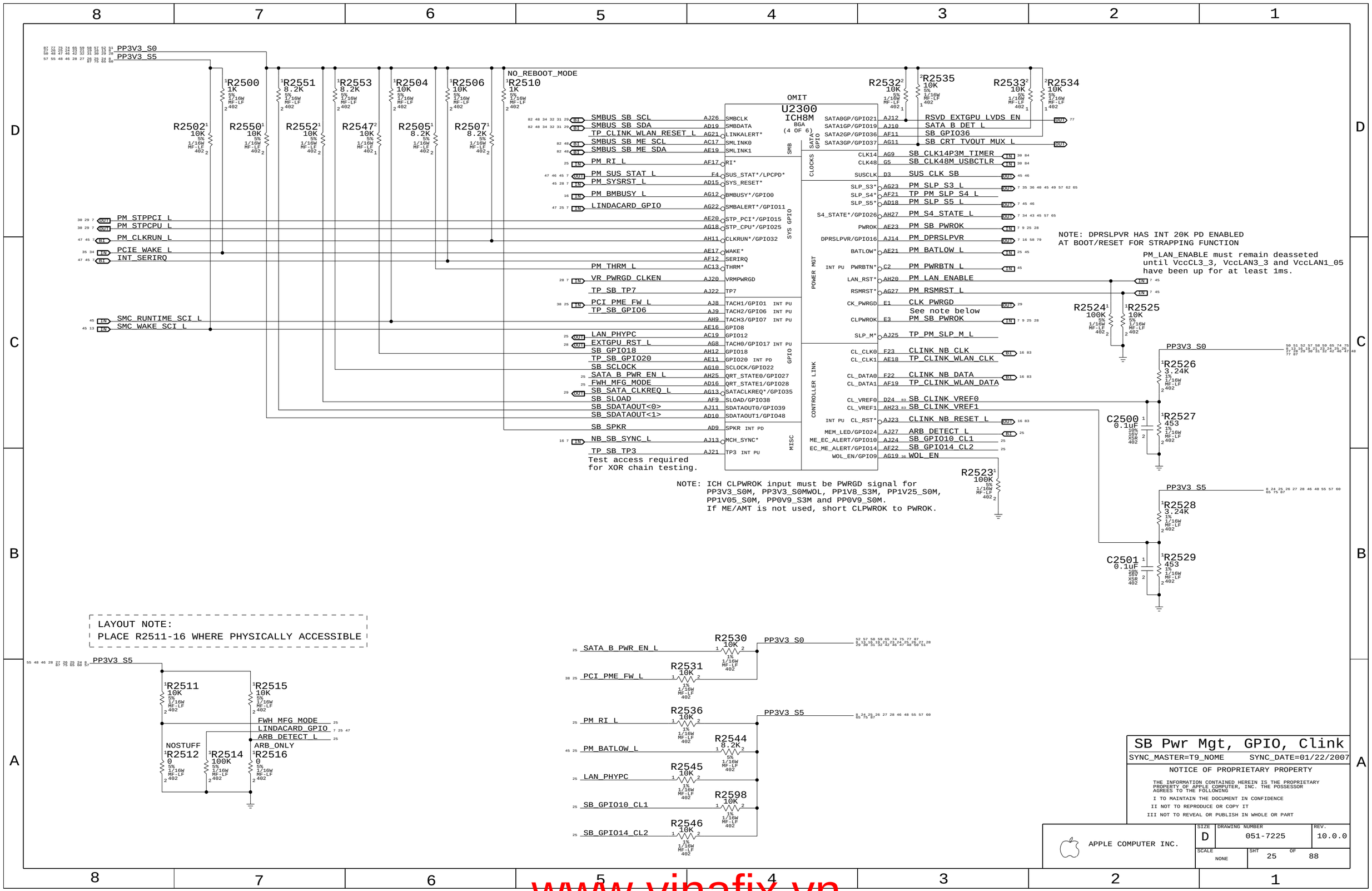
SB Enet, Disk, FSB, LPC

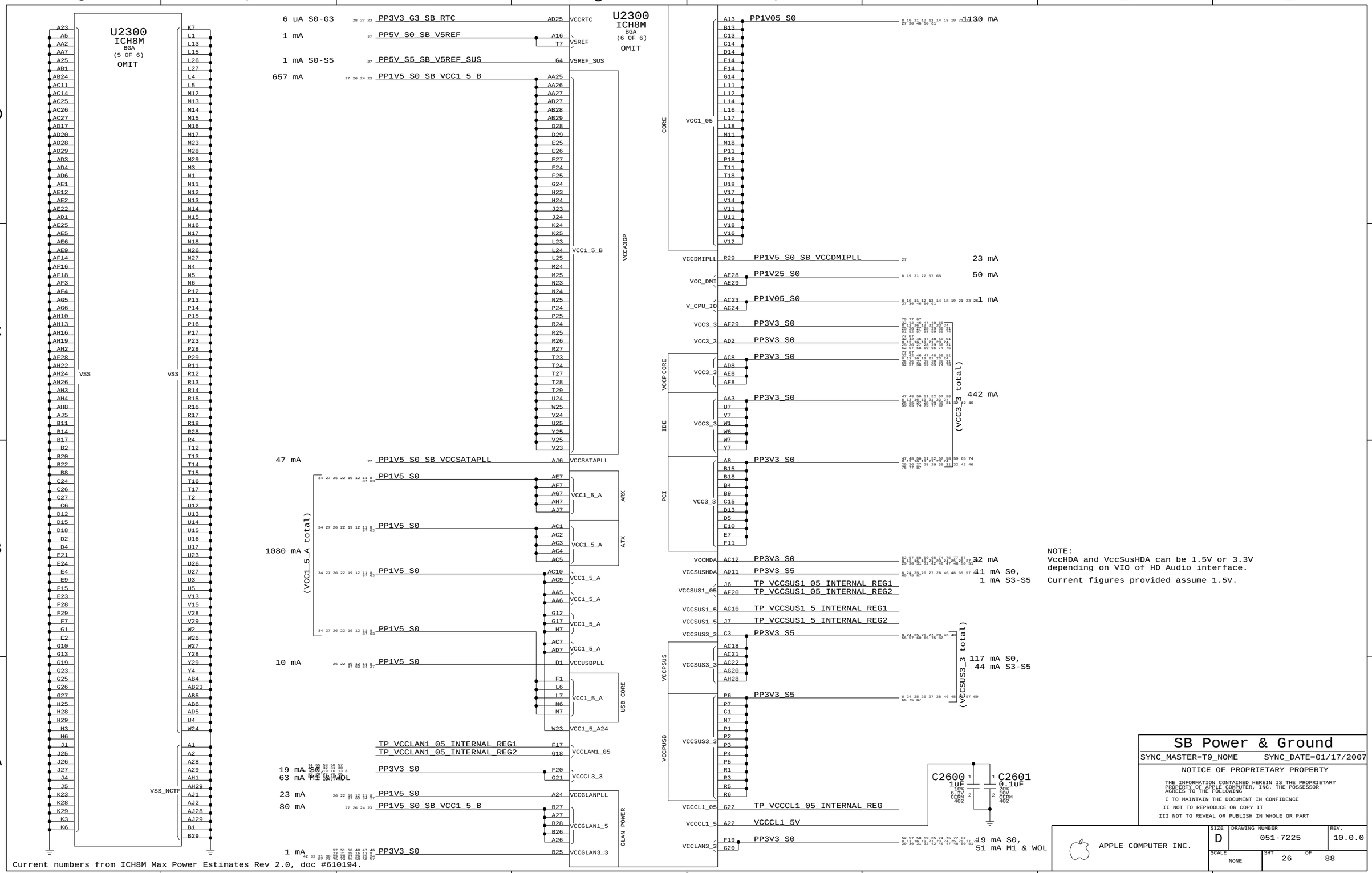
SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

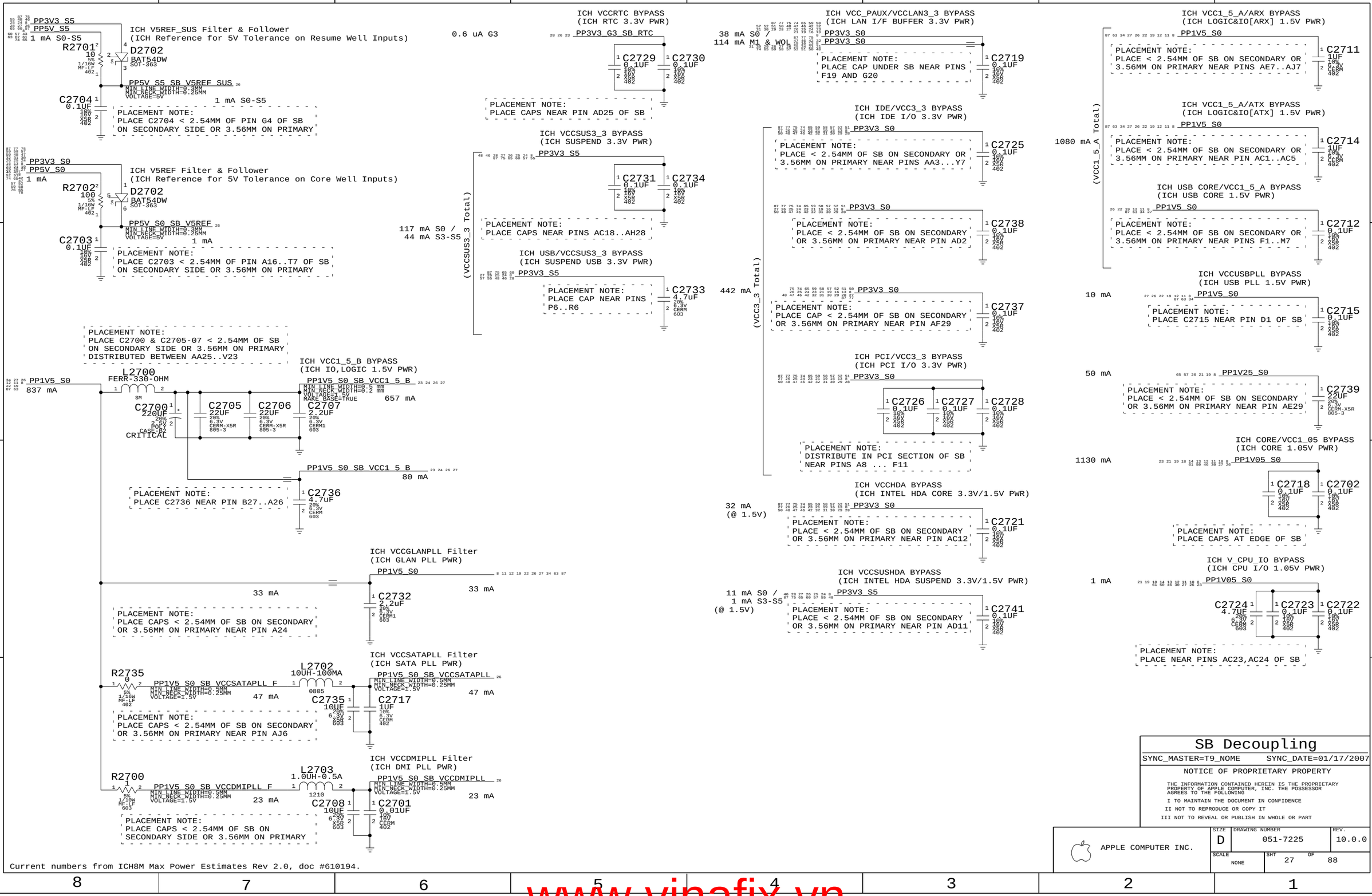
APPLE COMPUTER INC.

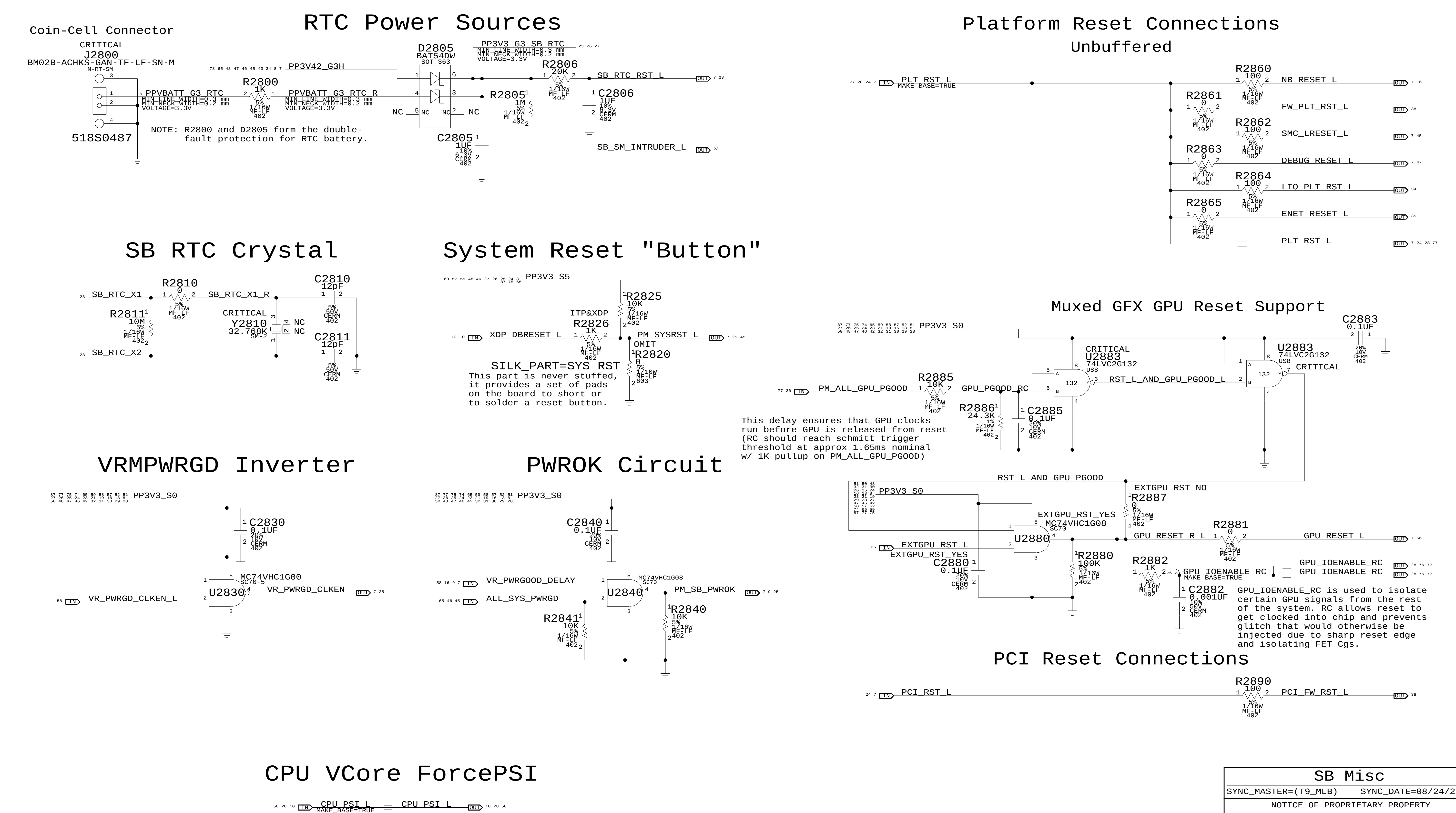
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 23 OF 88	









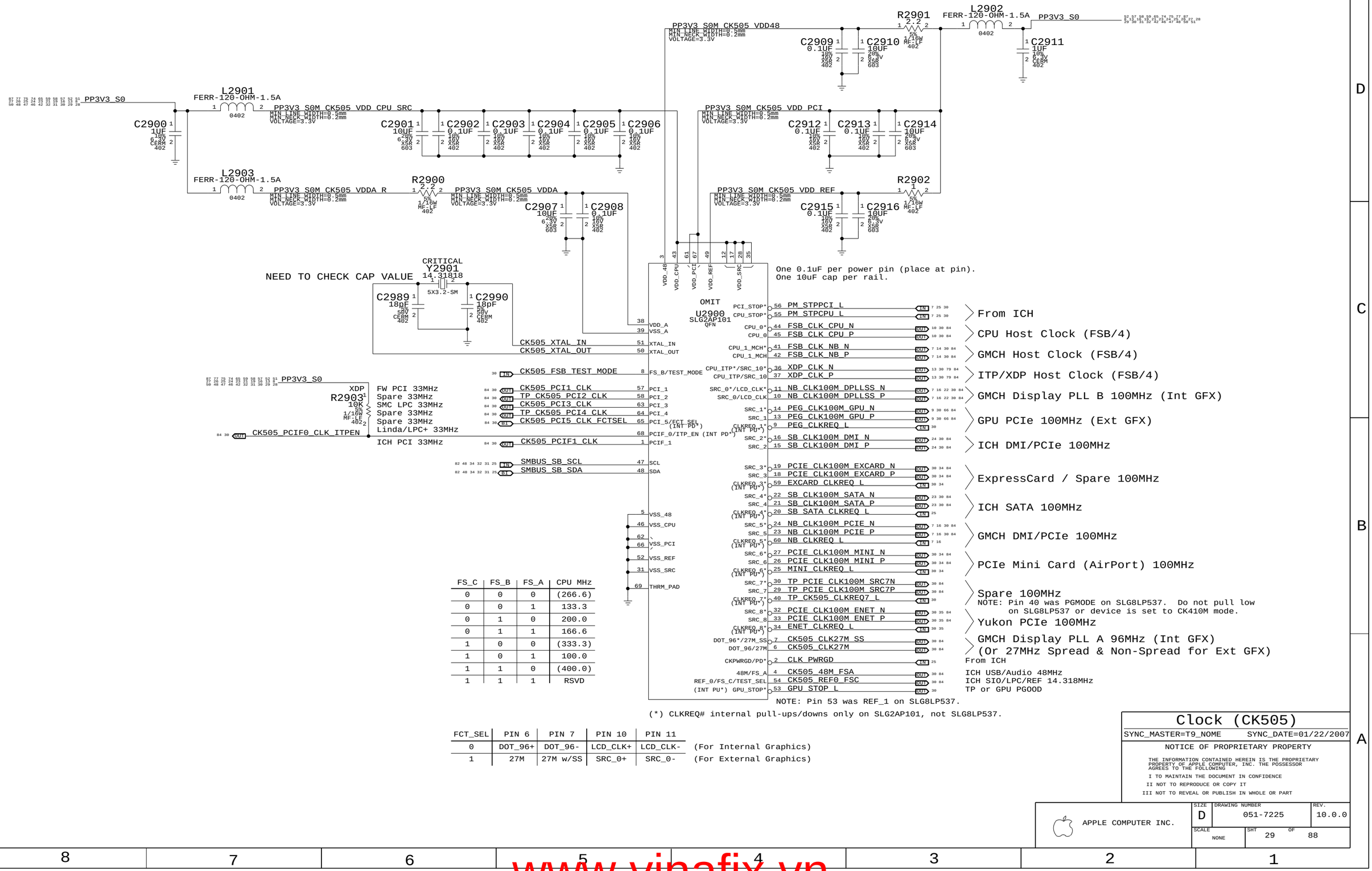

RTC Power Sources
Coin-Cell Connector
CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
518S0487
PPVBATT_G3_RTC
PPVBATT_G3_RTC_R
PP3V42_G3H
PP3V3_G3_SB_RTC
D2805
BAT54DW
SOT-363
R2800
1K
R2805
1M
R2806
20K
C2805
1UF
C2806
1UF
SB_RTC_RST_L
SB_SM_INTRUDER_L
NOTE: R2800 and D2805 form the double-
fault protection for RTC battery.
SB RTC Crystal
SB_RTC_X1
SB_RTC_X1_R
SB_RTC_X2
R2810
R2811
10M
CRITICAL
Y2810
32.768K
C2810
12pF
C2811
12pF
System Reset "Button"
PP3V3_S5
R2825
10K
ITP&XDP
R2826
1K
XDP_DBRESET_L
PM_SYSRST_L
OMIT
R2820
SILK_PART=SYS RST
This part is never stuffed,
it provides a set of pads
on the board to short or
to solder a reset button.
VRMPWRGD Inverter
PP3V3_S0
C2830
0.1UF
MC74VHC1G00
U2830
VR_PWRGD_CLKEN_L
VR_PWRGD_CLKEN
PWROK Circuit
C2840
0.1UF
MC74VHC1G08
U2840
VR_PWRGOOD_DELAY
ALL_SYS_PWRGD
PM_SB_PWROK
R2840
10K
R2841
10K
CPU VCore ForcePSI
CPU_PSI_L
CPU_PSI_L
Platform Reset Connections
Unbuffered
PLT_RST_L
R2860
NB_RESET_L
R2861
FW_PLT_RST_L
R2862
SMC_LRESET_L
R2863
DEBUG_RESET_L
R2864
LIO_PLT_RST_L
R2865
ENET_RESET_L
PLT_RST_L
Muxed GFX GPU Reset Support
C2883
0.1UF
CRITICAL
U2883
74LVC2G132
R2885
10K
PM_ALL_GPU_PGOOD
GPU_PGOOD_RC
RST_L_AND_GPU_PGOOD_L
R2886
24.3K
C2885
0.1UF
This delay ensures that GPU clocks
run before GPU is released from reset
(RC should reach schmitt trigger
threshold at approx 1.65ms nominal
w/ 1K pullup on PM_ALL_GPU_PGOOD)
RST_L_AND_GPU_PGOOD
EXTGPU_RST_NO
R2887
EXTGPU_RST_YES
MC74VHC1G08
U2880
EXTGPU_RST_L
C2880
0.1UF
R2880
100K
GPU_RESET_R_L
R2881
GPU_RESET_L
R2882
1K
GPU_IOENABLE_RC
C2882
0.001UF
GPU_IOENABLE_RC is used to isolate
certain GPU signals from the rest
of the system. RC allows reset to
get clocked into chip and prevents
glitch that would otherwise be
injected due to sharp reset edge
and isolating FET Cgs.
PCI Reset Connections
PCI_RST_L
R2890
100
PCI_FW_RST_L

SB Misc

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/24/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE NONE	SHT 28	OF 88



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

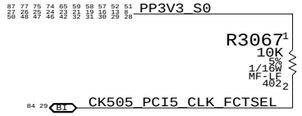
SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

APPLE COMPUTER INC.

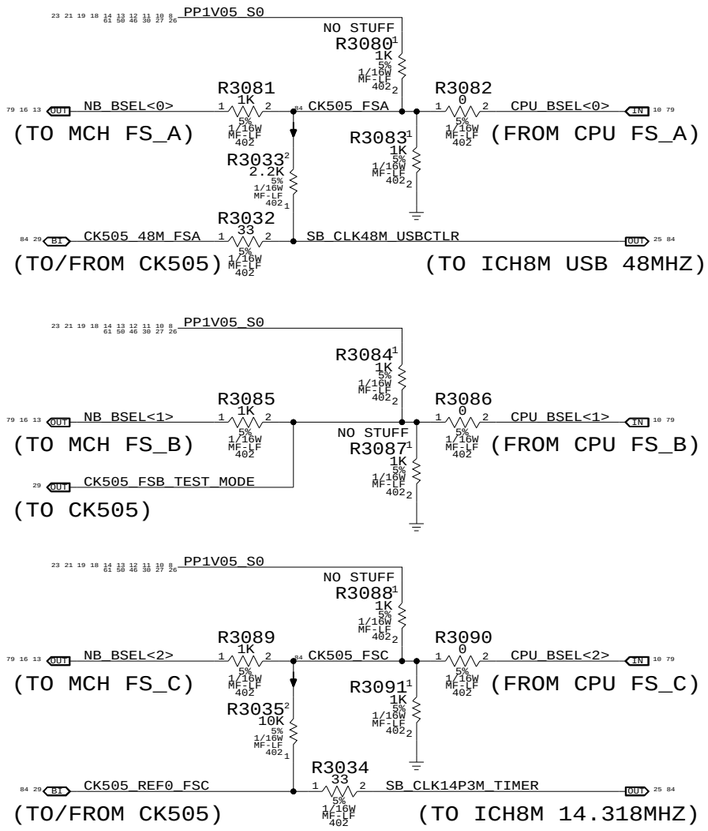
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 29 OF 88	

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)



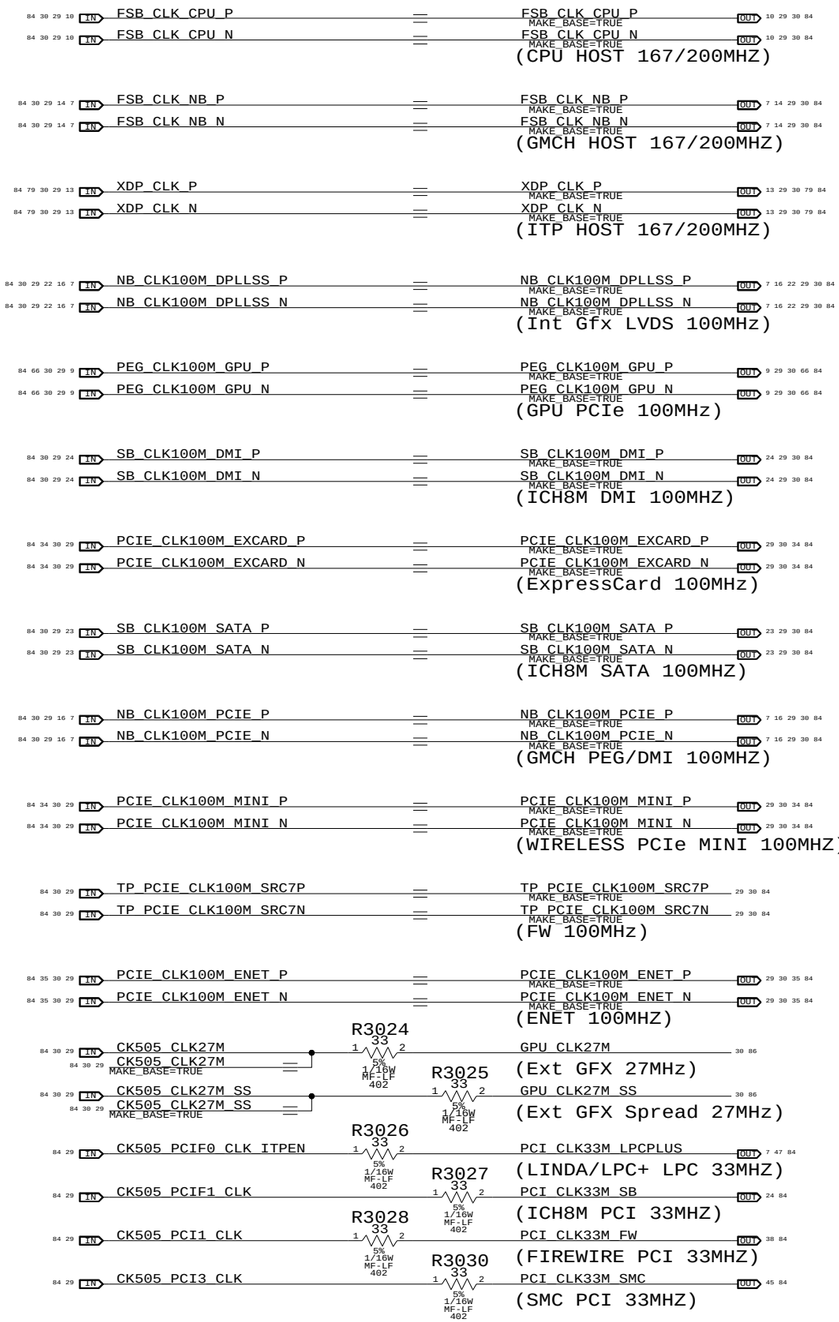
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

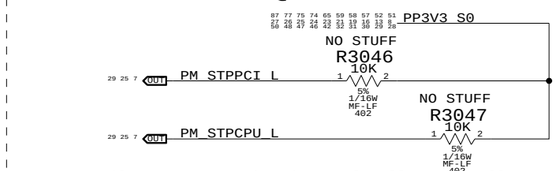
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)



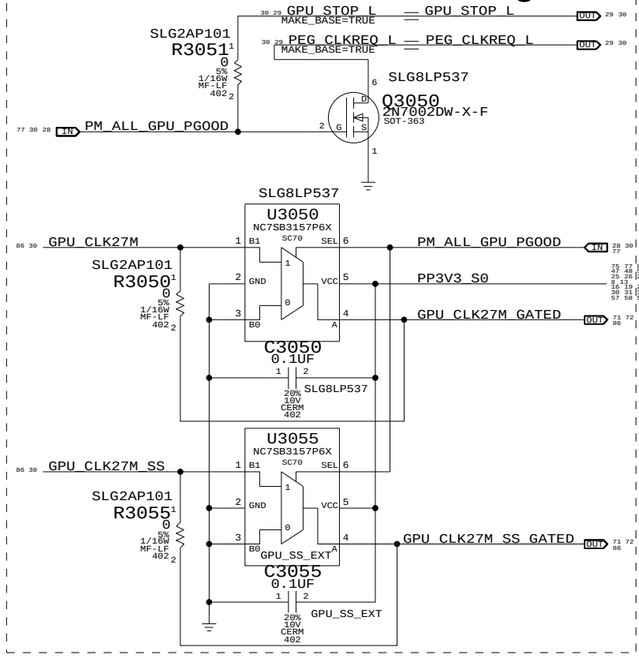
CLKREQ Controls



Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

EXCARD_CLKREQ_L
MINI_CLKREQ_L
ENET_CLKREQ_L
TP_CK505_CLKREQ7_L

GPU Clock Gating



Unused Clocks

TP_CK505_PCI2_CLK
(Reserved for TPM PCI 33MHZ)
TP_CK505_PCI4_CLK
(Spare 33MHZ)

Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 30 OF 88	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

62 32 16 8 PP0V9_S3_MEM_VREF

C3101 2.2uF 20% 6.3V CERM 603

C3100 0.1uF 20% 10V CERM 402

87 62 50 38 32 31 8 PP1V8_S3

CRITICAL J3100 F-RT-TH1

DDR2-SODIMM-DUAL

	1B	VREF		201	VSS0	2B	
	3B	VSS1			DQ4	4B	MEM_A_DQ<9> 17 81
81 17	5B	DQ0	MEM_A_DQ<14>		DQ5	6B	MEM_A_DQ<15> 17 81
81 17	7B	DQ1	MEM_A_DQ<13>		VSS2	8B	
	9B	VSS4			DM0	10B	MEM_A_DM<1> 17 81
81 17	11B	DQS0*	MEM_A_DQS_N<1>		VSS5	12B	
81 17	13B	DQS0	MEM_A_DQS_P<1>		DQ6	14B	MEM_A_DQ<8> 17 81
	15B	VSS6			DQ7	16B	MEM_A_DQ<12> 17 81
81 17	17B	DQ2	MEM_A_DQ<10>		VSS7	18B	
81 17	19B	DQ3	MEM_A_DQ<11>		DQ12	20B	MEM_A_DQ<2> 17 81
	21B	VSS8			DQ13	22B	MEM_A_DQ<3> 17 81
81 17	23B	DQ8	MEM_A_DQ<7>		VSS9	24B	
81 17	25B	DQ9	MEM_A_DQ<0>		DM1	26B	MEM_A_DM<0> 17 81
	27B	VSS10			VSS11	28B	
81 17	29B	DQS1*	MEM_A_DQS_N<0>		CK0	30B	MEM_CLK_P<0> 16 81
81 17	31B	DQS1	MEM_A_DQS_P<0>		CK0*	32B	MEM_CLK_N<0> 16 81
	33B	VSS12			VSS13	34B	
81 17	35B	DQ10	MEM_A_DQ<6>		DQ14	36B	MEM_A_DQ<1> 17 81
81 17	37B	DQ11	MEM_A_DQ<4>		DQ15	38B	MEM_A_DQ<5> 17 81
	39B	VSS14			VSS15	40B	
		KEY					
	41B	VSS16			VSS17	42B	
81 17	43B	DQ16	MEM_A_DQ<17>		DQ20	44B	MEM_A_DQ<18> 17 81
81 17	45B	DQ17	MEM_A_DQ<21>		DQ21	46B	MEM_A_DQ<20> 17 81
	47B	VSS18			VSS19	48B	
81 17	49B	DQS2*	MEM_A_DQS_N<2>		NC0	50B	PM_EXTTS_L<0> 16 45
81 17	51B	DQS2	MEM_A_DQS_P<2>		DM2	52B	MEM_A_DM<2> 17 81
	53B	VSS21			VSS22	54B	
81 17	55B	DQ18	MEM_A_DQ<23>		DQ22	56B	MEM_A_DQ<22> 17 81
81 17	57B	DQ19	MEM_A_DQ<16>		DQ23	58B	MEM_A_DQ<19> 17 81
	59B	VSS23			VSS24	60B	
81 17	61B	DQ24	MEM_A_DQ<31>		DQ28	62B	MEM_A_DQ<26> 17 81
81 17	63B	DQ25	MEM_A_DQ<27>		DQ29	64B	MEM_A_DQ<24> 17 81
	65B	VSS25			VSS26	66B	
81 17	67B	DM3	MEM_A_DM<3>		DQS3*	68B	MEM_A_DQS_N<3> 17 81
	69B	NC1	NC		DQS3	70B	MEM_A_DQS_P<3> 17 81
	71B	VSS27			VSS28	72B	
81 17	73B	DQ26	MEM_A_DQ<30>		DQ30	74B	MEM_A_DQ<25> 17 81
81 17	75B	DQ27	MEM_A_DQ<28>		DQ31	76B	MEM_A_DQ<29> 17 81
	77B	VSS29			VSS30	78B	
81 33 16	79B	CKE0	MEM_CKE<0>		NC/CKE1	80B	MEM_CKE<1> 16 33 81
	81B	VDD0			VDD1	82B	
	83B	NC2	NC		NC/A15	84B	TP_MEM_A_A<15> 9
81 33 17	85B	BA2	MEM_A_BS<2>		NC/A14	86B	MEM_A_A<14> 16 33 81
	87B	VDD2			VDD3	88B	
81 33 17	89B	A12	MEM_A_A<12>		A11	90B	MEM_A_A<11> 17 33 81
81 33 17	91B	A9	MEM_A_A<9>		A7	92B	MEM_A_A<7> 17 33 81
81 33 17	93B	A8	MEM_A_A<8>		A6	94B	MEM_A_A<6> 17 33 81
	95B	VDD4			VDD5	96B	
81 33 17	97B	A5	MEM_A_A<5>		A4	98B	MEM_A_A<4> 17 33 81
81 33 17	99B	A3	MEM_A_A<3>		A2	100B	MEM_A_A<2> 17 33 81
81 33 17	101B	A1	MEM_A_A<1>		A0	102B	MEM_A_A<0> 17 33 81
	103B	VDD6			VDD7	104B	
81 33 17	105B	A10/AP	MEM_A_A<10>		BA1	106B	MEM_A_BS<1> 17 33 81
81 33 17	107B	BA0	MEM_A_BS<0>		RAS*	108B	MEM_A_RAS_L 17 33 81
81 33 17	109B	WE*	MEM_A_WE_L		S0*	110B	MEM_CS_L<0> 16 33 81
	111B	VDD8			VDD9	112B	
81 33 17	113B	CAS*	MEM_A_CAS_L		ODT0	114B	MEM_ODT<0> 16 33 81
81 33 16	115B	NC/S1*	MEM_CS_L<1>		NC/A13	116B	MEM_A_A<13> 17 33 81
	117B	VDD10			VDD11	118B	
81 33 16	119B	NC/ODT1	MEM_ODT<1>		NC3	120B	NC
	121B	VSS31			VSS32	122B	
81 17	123B	DQ32	MEM_A_DQ<36>		DQ36	124B	MEM_A_DQ<35> 17 81
81 17	125B	DQ33	MEM_A_DQ<38>		DQ37	126B	MEM_A_DQ<39> 17 81
	127B	VSS33			VSS34	128B	
81 17	129B	DQS4*	MEM_A_DQS_N<4>		DM4	130B	MEM_A_DM<4> 17 81
81 17	131B	DQS4	MEM_A_DQS_P<4>		VSS35	132B	
	133B	VSS36			DQ38	134B	MEM_A_DQ<33> 17 81
81 17	135B	DQ34	MEM_A_DQ<37>		DQ39	136B	MEM_A_DQ<32> 17 81
81 17	137B	DQ35	MEM_A_DQ<34>		VSS37	138B	
	139B	VSS38			DQ44	140B	MEM_A_DQ<63> 17 81
81 17	141B	DQ40	MEM_A_DQ<56>		DQ45	142B	MEM_A_DQ<62> 17 81
81 17	143B	DQ41	MEM_A_DQ<59>		VSS39	144B	
	145B	VSS40			DQS5*	146B	MEM_A_DQS_N<7> 17 81
81 17	147B	DM5	MEM_A_DM<7>		DQS5	148B	MEM_A_DQS_P<7> 17 81
	149B	VSS41			VSS42	150B	
81 17	151B	DQ42	MEM_A_DQ<58>		DQ46	152B	MEM_A_DQ<57> 17 81
81 17	153B	DQ43	MEM_A_DQ<60>		DQ47	154B	MEM_A_DQ<61> 17 81
	155B	VSS43			VSS44	156B	
81 17	157B	DQ48	MEM_A_DQ<51>		DQ52	158B	MEM_A_DQ<55> 17 81
81 17	159B	DQ49	MEM_A_DQ<54>		DQ53	160B	MEM_A_DQ<50> 17 81
	161B	VSS45			VSS46	162B	
	163B	NC_TEST	NC		CK1	164B	MEM_CLK_P<1> 16 81
	165B	VSS47			CK1*	166B	MEM_CLK_N<1> 16 81
81 17	167B	DQS6*	MEM_A_DQS_N<6>		VSS48	168B	
81 17	169B	DQS6	MEM_A_DQS_P<6>		DM6	170B	MEM_A_DM<6> 17 81
	171B	VSS49			VSS50	172B	
81 17	173B	DQ50	MEM_A_DQ<48>		DQ54	174B	MEM_A_DQ<49> 17 81
81 17	175B	DQ51	MEM_A_DQ<53>		DQ55	176B	MEM_A_DQ<52> 17 81
	177B	VSS51			VSS52	178B	
81 17	179B	DQ56	MEM_A_DQ<43>		DQ60	180B	MEM_A_DQ<45> 17 81
81 17	181B	DQ57	MEM_A_DQ<42>		DQ61	182B	MEM_A_DQ<40> 17 81
	183B	VSS53			VSS54	184B	
81 17	185B	DM7	MEM_A_DM<5>		DQS7*	186B	MEM_A_DQS_N<5> 17 81
	187B	VSS55			DQS7	188B	MEM_A_DQS_P<5> 17 81
81 17	189B	DQ58	MEM_A_DQ<46>		VSS56	190B	
81 17	191B	DQ59	MEM_A_DQ<41>		DQ62	192B	MEM_A_DQ<44> 17 81
	193B	VSS57			DQ63	194B	MEM_A_DQ<47> 17 81
82 48 34 32 29 25	195B	SDA	SMBUS_SB_SDA		VSS58	196B	
82 48 34 32 29 25	197B	SCL	SMBUS_SB_SCL		SA0	198B	
	199B	VDDSPD			SA1	200B	ADDR=0xA0(WR)/0xA1(RD)

87 77 75 74 65 59 58 57 52 27 26 25 24 23 22 21 8 51 50 48 47 44 43 33 30 29 28 PP3V3_S0

516-0140 202

PP1V8_S3 8 31 32 38 50 62 87

DDR2 Bypass Caps

(For return current)

87 62 50 38 32 31 8 PP1V8_S3

C3108 10UF 20% 6.3V X5R 603

C3109 10UF 20% 6.3V X5R 603

C3110 1UF 10% 6.3V CERM 402

C3111 1UF 10% 6.3V CERM 402

C3112 1UF 10% 6.3V CERM 402

C3113 1UF 10% 6.3V CERM 402

C3114 1UF 10% 6.3V CERM 402

C3115 1UF 10% 6.3V CERM 402

C3116 1UF 10% 6.3V CERM 402

C3117 1UF 10% 6.3V CERM 402

C3118 1UF 10% 6.3V CERM 402

C3119 1UF 10% 6.3V CERM 402

C3120 1UF 10% 6.3V CERM 402

C3121 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 31 OF 88	

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

"Expansion" (surface-mount) slot

PP0V9_S3_MEM_VREF

C3201 2.2uF 20% 6.3V CERM 603

C3200 0.1uF 20% 10V CERM 402

PP1V8_S3

DDR2-SODIMM-DUAL CRITICAL J3200 F-RT-SM-M9

	1A	VREF			2A	VSS0	
	3A	VSS1			4A	DQ4	MEM_B_DQ<9>
MEM_B_DQ<15>	5A	DQ0			6A	DQ5	MEM_B_DQ<11>
MEM_B_DQ<14>	7A	DQ1			8A	VSS2	
	9A	VSS4			10A	DM0	MEM_B_DM<1>
MEM_B_DQS_N<1>	11A	DQS0*			12A	VSS5	
MEM_B_DQS_P<1>	13A	DQS0			14A	DQ6	MEM_B_DQ<12>
	15A	VSS6			16A	DQ7	MEM_B_DQ<8>
MEM_B_DQ<10>	17A	DQ2			18A	VSS7	
MEM_B_DQ<13>	19A	DQ3			20A	DQ12	MEM_B_DQ<3>
	21A	VSS8			22A	DQ13	MEM_B_DQ<6>
MEM_B_DQ<7>	23A	DQ8			24A	VSS9	
MEM_B_DQ<2>	25A	DQ9			26A	DM1	MEM_B_DM<0>
	27A	VSS10			28A	VSS11	
MEM_B_DQS_N<0>	29A	DQS1*			30A	CK0	MEM_CLK_P<4>
MEM_B_DQS_P<0>	31A	DQS1			32A	CK0*	MEM_CLK_N<4>
	33A	VSS12			34A	VSS13	
MEM_B_DQ<1>	35A	DQ10			36A	DQ14	MEM_B_DQ<0>
MEM_B_DQ<4>	37A	DQ11			38A	DQ15	MEM_B_DQ<5>
	39A	VSS14	KEY		40A	VSS15	
	41A	VSS16			42A	VSS17	
MEM_B_DQ<21>	43A	DQ16			44A	DQ20	MEM_B_DQ<22>
MEM_B_DQ<19>	45A	DQ17			46A	DQ21	MEM_B_DQ<18>
	47A	VSS18			48A	VSS19	
MEM_B_DQS_N<2>	49A	DQS2*			50A	NC0	PM_EXTTS_L<1>
MEM_B_DQS_P<2>	51A	DQS2			52A	DM2	MEM_B_DM<2>
	53A	VSS21			54A	VSS22	
MEM_B_DQ<20>	55A	DQ18			56A	DQ22	MEM_B_DQ<17>
MEM_B_DQ<23>	57A	DQ19			58A	DQ23	MEM_B_DQ<16>
	59A	VSS23			60A	VSS24	
MEM_B_DQ<29>	61A	DQ24			62A	DQ28	MEM_B_DQ<26>
MEM_B_DQ<24>	63A	DQ25			64A	DQ29	MEM_B_DQ<28>
	65A	VSS25			66A	VSS26	
MEM_B_DM<3>	67A	DM3			68A	DQS3*	MEM_B_DQS_N<3>
NC	69A	NC1			70A	DQS3	MEM_B_DQS_P<3>
	71A	VSS27			72A	VSS28	
MEM_B_DQ<27>	73A	DQ26			74A	DQ30	MEM_B_DQ<31>
MEM_B_DQ<25>	75A	DQ27			76A	DQ31	MEM_B_DQ<30>
	77A	VSS29			78A	VSS30	
MEM_CKE<3>	79A	CKE0			80A	NC/CKE1	MEM_CKE<4>
	81A	VDD0			82A	VDD1	
NC	83A	NC2			84A	NC/A15	TP_MEM_B_A<15>
MEM_B_BS<2>	85A	BA2			86A	NC/A14	MEM_B_A<14>
	87A	VDD2			88A	VDD3	
MEM_B_A<12>	89A	A12			90A	A11	MEM_B_A<11>
MEM_B_A<9>	91A	A9			92A	A7	MEM_B_A<7>
MEM_B_A<8>	93A	A8			94A	A6	MEM_B_A<6>
	95A	VDD4			96A	VDD5	
MEM_B_A<5>	97A	A5			98A	A4	MEM_B_A<4>
MEM_B_A<3>	99A	A3			100A	A2	MEM_B_A<2>
MEM_B_A<1>	101A	A1			102A	A0	MEM_B_A<0>
	103A	VDD6			104A	VDD7	
MEM_B_A<10>	105A	A10/AP			106A	BA1	MEM_B_BS<1>
MEM_B_BS<0>	107A	BA0			108A	RAS*	MEM_B_RAS_L
MEM_B_WE_L	109A	WE*			110A	S0*	MEM_CS_L<2>
	111A	VDD8			112A	VDD9	
MEM_B_CAS_L	113A	CAS*			114A	ODT0	MEM_ODT<2>
MEM_CS_L<3>	115A	NC/S1*			116A	NC/A13	MEM_B_A<13>
	117A	VDD10			118A	VDD11	
MEM_ODT<3>	119A	NC/ODT1			120A	NC3	NC
	121A	VSS31			122A	VSS32	
MEM_B_DQ<36>	123A	DQ32			124A	DQ36	MEM_B_DQ<32>
MEM_B_DQ<33>	125A	DQ33			126A	DQ37	MEM_B_DQ<37>
	127A	VSS33			128A	VSS34	
MEM_B_DQS_N<4>	129A	DQS4*			130A	DM4	MEM_B_DM<4>
MEM_B_DQS_P<4>	131A	DQS4			132A	VSS35	
	133A	VSS36			134A	DQ38	MEM_B_DQ<38>
MEM_B_DQ<34>	135A	DQ34			136A	DQ39	MEM_B_DQ<39>
MEM_B_DQ<35>	137A	DQ35			138A	VSS37	
	139A	VSS38			140A	DQ44	MEM_B_DQ<56>
MEM_B_DQ<57>	141A	DQ40			142A	DQ45	MEM_B_DQ<59>
MEM_B_DQ<60>	143A	DQ41			144A	VSS39	
	145A	VSS40			146A	DQS5*	MEM_B_DQS_N<7>
MEM_B_DM<7>	147A	DM5			148A	DQS5	MEM_B_DQS_P<7>
	149A	VSS41			150A	VSS42	
MEM_B_DQ<61>	151A	DQ42			152A	DQ46	MEM_B_DQ<63>
MEM_B_DQ<62>	153A	DQ43			154A	DQ47	MEM_B_DQ<58>
	155A	VSS43			156A	VSS44	
MEM_B_DQ<48>	157A	DQ48			158A	DQ52	MEM_B_DQ<54>
MEM_B_DQ<51>	159A	DQ49			160A	DQ53	MEM_B_DQ<53>
	161A	VSS45			162A	VSS46	
NC	163A	NC_TEST			164A	CK1	MEM_CLK_P<3>
	165A	VSS47			166A	CK1*	MEM_CLK_N<3>
MEM_B_DQS_N<6>	167A	DQS6*			168A	VSS48	
MEM_B_DQS_P<6>	169A	DQS6			170A	DM6	MEM_B_DM<6>
	171A	VSS49			172A	VSS50	
MEM_B_DQ<50>	173A	DQ50			174A	DQ54	MEM_B_DQ<52>
MEM_B_DQ<55>	175A	DQ51			176A	DQ55	MEM_B_DQ<49>
	177A	VSS51			178A	VSS52	
MEM_B_DQ<40>	179A	DQ56			180A	DQ60	MEM_B_DQ<46>
MEM_B_DQ<47>	181A	DQ57			182A	DQ61	MEM_B_DQ<43>
	183A	VSS53			184A	VSS54	
MEM_B_DM<5>	185A	DM7			186A	DQS7*	MEM_B_DQS_N<5>
	187A	VSS55			188A	DQS7	MEM_B_DQS_P<5>
MEM_B_DQ<42>	189A	DQ58			190A	VSS56	
MEM_B_DQ<45>	191A	DQ59			192A	DQ62	MEM_B_DQ<41>
PP3V3_S0	193A	VSS57			194A	DQ63	MEM_B_DQ<44>
SMBUS_SB_SDA	195A	SDA			196A	VSS58	Resistor prevents pwr-gnd short
SMBUS_SB_SCL	197A	SCL			198A	SA0	
	199A	VDDSPD			200A	SA1	SODIMM_B_SA1

516S0471

ADDR=0xA4(WR)/0xA5(RD)

PP3V3_S0

R3200 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C3208 10UF 20% 6.3V X5R 603

C3209 10UF 20% 6.3V X5R 603

C3210 1UF 10% 6.3V CERM 402

C3211 0.1UF 20% 10V CERM 402

C3212 1UF 10% 6.3V CERM 402

C3213 1UF 10% 6.3V CERM 402

C3214 1UF 10% 6.3V CERM 402

C3215 1UF 10% 6.3V CERM 402

C3216 1UF 10% 6.3V CERM 402

C3217 0.1UF 20% 10V CERM 402

C3218 0.1UF 20% 10V CERM 402

C3219 0.1UF 20% 10V CERM 402

C3220 0.1UF 20% 10V CERM 402

C3221 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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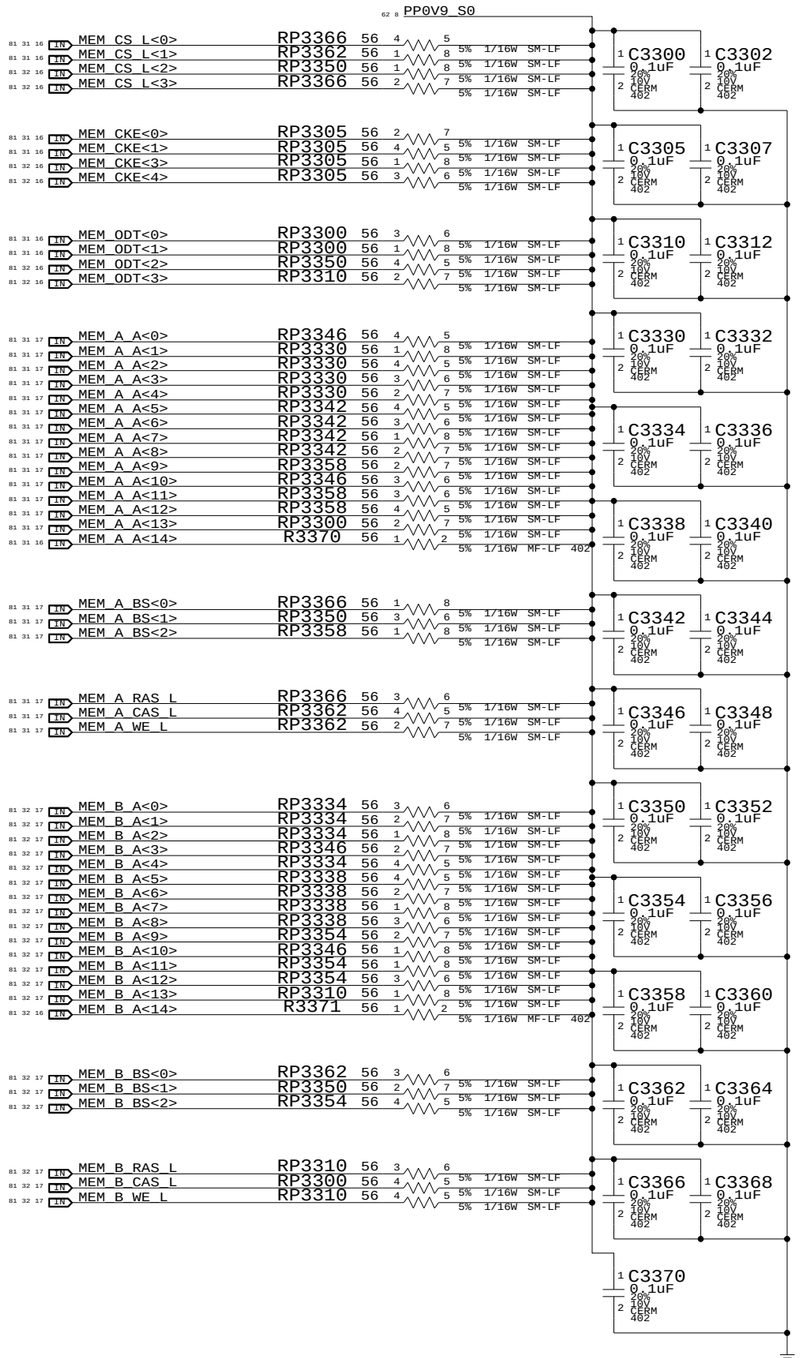
SCALE: NONE	SHT 32 OF 88	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE NONE SHT 33 OF 88

Left I/O Board Connector

(Output to LIO) PP3V42_G3H
(Input from LIO) PPDCIN_G3H
(Output to LIO) PP1V5_S0

CRITICAL
J3400
QT500806-L121-9F
M-ST-SM

SYS_ONEWIRE	BI	2	1	PCIE_WAKE_L	OUT
SMC_ADAPTER_EN	IN	4	3	SMBUS_SMC_B_S0_SDA	BI
SMC_BATT_CHG_EN	IN	6	5	SMBUS_SMC_B_S0_SCL	IN
		8	7		
LCDBKLT_PWM_UNBUF	IN	10	9	USB_EXCARD_N	BI
LCDBKLT_PWREN	IN	12	11	USB_EXCARD_P	BI
EXCARD_CLKREQ_L	OUT	14	13		
MINI_CLKREQ_L	OUT	16	15	USB_EXTB_N	BI
LIO_PLT_RST_L	IN	18	17	USB_EXTB_P	BI
		20	19		
		22	21	SMBUS_SB_SCL	IN
		24	23	SMBUS_SB_SDA	BI
		26	25		
EXCARD_OC_L	OUT	28	27	PCIE_CLK100M_MINI_N	IN
USB_EXTB_OC_L	OUT	30	29	PCIE_CLK100M_MINI_P	IN
LIO_BATT_ISENSE	OUT	32	31		
		34	33	PCIE_MINI_D2R_N	OUT
SMC_SYS_ISET	IN	36	35	PCIE_MINI_D2R_P	OUT
		38	37		
SMC_BATT_ISET	IN	40	39	PCIE_MINI_R2D_N	
SMC_BATT_TRICKLE_EN_L	IN	42	41	PCIE_MINI_R2D_P	
SMC_EXCARD_CP	OUT	44	43		
SMC_BC_ACOK	OUT	46	45	PCIE_CLK100M_EXCARD_N	IN
PM_SLP_S3_LS5V	IN	48	47	PCIE_CLK100M_EXCARD_P	IN
		50	49		
LIO_DCIN_ISENSE	OUT	52	51	PCIE_EXCARD_D2R_N	
PM_S4_STATE_L	IN	54	53	PCIE_EXCARD_D2R_P	
		56	55		
SMC_EXCARD_PWR_EN	IN	58	57	PCIE_EXCARD_R2D_N	
		60	59	PCIE_EXCARD_R2D_P	
HDA_SDOUT	IN	62	61		
HDA_BIT_CLK	OUT	64	63	HDA_RST_L	IN
		66	65		
HDA_SDIN0	OUT	68	67	USB_MINI_N	BI
HDA_SYNC	IN	70	69	USB_MINI_P	BI
		72	71		
NC		74	73		
		76	75	Pull-up on LIO, FETs to GND on MLB	
		78	77	PM_WLAN_EN_L	BI
		80	79	SMC_ENRGYSTR_LDO_EN	IN
		83	82		

516S0348

C3410 0.1uF
C3411 0.1uF
C3420 0.1uF
C3421 0.1uF
10% 16V X5R 402

Place caps close to SB
Place caps close to SB

PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P

MAKE_BASE=TRUE

Left I/O Board Connector			
SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006			
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 10.0.0
	SCALE NONE	SHT 34 OF 88	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

PP1V25_ENET

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701–C3708 0.1UF 10% 16V X5R 402 (C3706–C3708: 0.001UF 10% 50V CERM 402)

PP3V3_ENET

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711–C3713 0.1UF 10% 16V X5R 402; C3714–C3715 0.001UF 10% 50V CERM 402

PP1V9_ENET — L3720 FERR-120-OHM-1.5A 0402 — PP1V8R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721–C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

GND

Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P — C3735 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_C_P
PCIE_ENET_D2R_N — C3736 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_C_N
PLACEMENT_NOTE=Place C3730 close to southbridge.
PCIE_ENET_R2D_C_P — C3730 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_P
PCIE_ENET_R2D_C_N — C3731 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_N
PLACEMENT_NOTE=Place C3731 close to southbridge.

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
Yukon EC: Pin 42 should be NC (or TP) net.
ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

SIGNAL_MODEL=EMPTY
R3740 R3741 49.9 1% 1/16W MF-LF 402
R3742 R3743 49.9 1% 1/16W MF-LF 402
R3744 R3745 49.9 1% 1/16W MF-LF 402
R3746 R3747 49.9 1% 1/16W MF-LF 402

ENET_MDI0 — C3740 0.001UF 10% 50V CERM 402
ENET_MDI1 — C3742 0.001UF 10% 50V CERM 402
ENET_MDI2 — C3744 0.001UF 10% 50V CERM 402
ENET_MDI3 — C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN — CRITICAL — OMIT

Pin	Name	Pin	Name
32	NC	1	VDDO_TTL0
51	NC	40	VDDO_TTL1
52	NC	45	VDDO_TTL2
57	NC	61	VDDO_TTL3
64	NC	8	AVDDH
19	AVDD0	2	VDD0
22	AVDD1	7	VDD1
23	AVDD2	13	VDD2
28	AVDD3	33	VDD3
		39	VDD4
		44	VDD5
		48	VDD6
		58	VDD7

EC:AVDD 2.5V

PCI EXPRESS
- 49 TX_P ← PCIE_ENET_D2R_C_P
- 50 TX_N ← PCIE_ENET_D2R_C_N
- 54 RX_P ← PCIE_ENET_R2D_P
- 53 RX_N ← PCIE_ENET_R2D_N
- 55 REFCLKP ← PCIE_CLK100M_ENET_P
- 56 REFCLKN ← PCIE_CLK100M_ENET_N
- 42 CLKREQ* EC:NO CONNECT
- 6 WAKE* ← PCIE_WAKE_L
- 5 PERST* ← ENET_RESET_L

MEDIA
- 17 MDIP0 ↔ ENET_MDI_P<0>
- 18 MDIN0 ↔ ENET_MDI_N<0>
- 20 MDIP1 ↔ ENET_MDI_P<1>
- 21 MDIN1 ↔ ENET_MDI_N<1>
- 26 MDIP2 ↔ ENET_MDI_P<2>
- 27 MDIN2 ↔ ENET_MDI_N<2>
- 30 MDIP3 ↔ ENET_MDI_P<3>
- 31 MDIN3 ↔ ENET_MDI_N<3>

MAIN CLK
- 15 XTALI ← ENET_CLK25M_XTALI
- 14 XTALO → ENET_CLK25M_XTALO

THRML_PAD 65

ANALOG
- LOM_DISABLE* 10 ← ENET_LOM_DIS_L
- VAUX_AVLBL 12
- SWITCH_VAUX 9 NC
- VMAIN_AVLBL 47 ← PM_SLP_S3_L (Must be high in S0 state (can use PP3V3_S0 as input))
- SWITCH_VCC 11 NC
- EC:CTRL25 CTRL18 4 → TP_YUKON_CTRL18
- CTRL12 3 → TP_YUKON_CTRL12
- RSET 16 — YUKON_RSET

R3760 4.7K 5% 1/10W MF-LF 402

YUKON_ULTRA
R3765 4.99K 1% 1/16W MF-LF 402

LED
- LED_ACT* 59 NC
- LED_LINK10/100* 60 NC
- LED_LINK1000* 62 NC
- LED_DUPLEX* 63 NC

SPI
- (IPU) SPI_DO 34 NC
- (IPU) SPI_DI 35 NC
- (IPU) SPI_CLK 37 NC
- (IPU) SPI_CS 36 NC

TWSI
- (IPU) VPD_CLK 38 ↔ YUKON_VPD_CLK
- (IPU) VPD_DATA 41 ↔ YUKON_VPD_DATA

TEST/RSVD
- (IPD) TESTMODE 46
- RSVD_24 24 NC
- RSVD_25 25 NC
- RSVD_29 29 NC
- RSVD_43 43 NC

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/10W MF-LF 402
U3780 M24C08 SO8 — CRITICAL
VCC, E2, NC, NC, WC*, NC1, NC0, SDA, SCL, VSS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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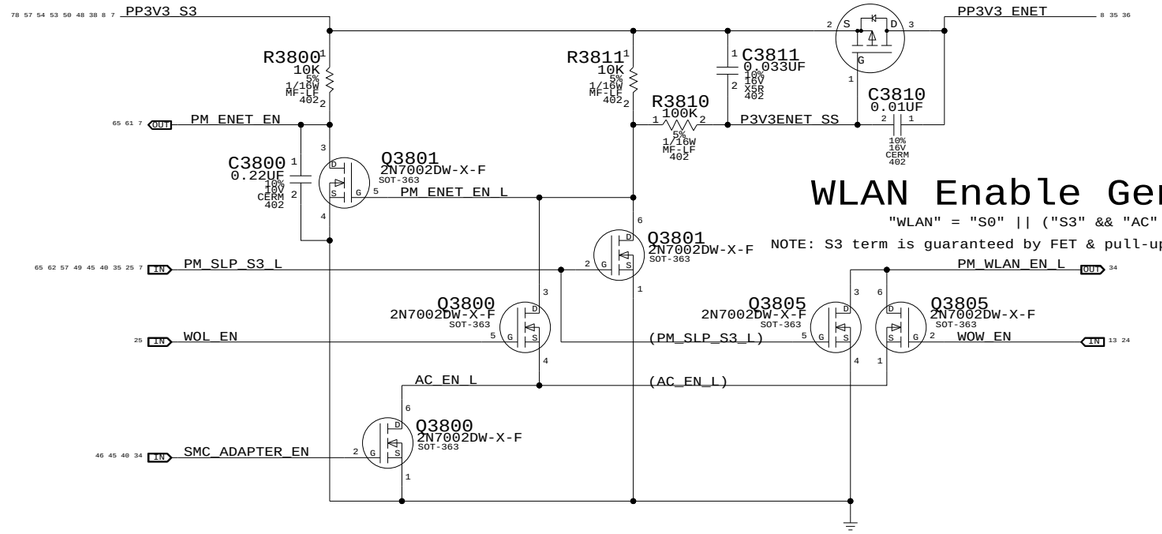
D	051-7225	10.0.0
SCALE: NONE	SHT 35 OF 88	

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

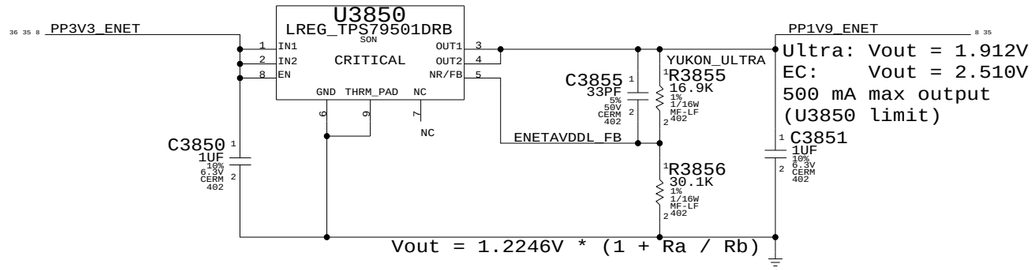
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

3.3V ENET FET

Yukon AVDDL LDO

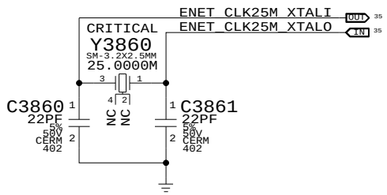
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=01/23/2007

APPLE COMPUTER INC.

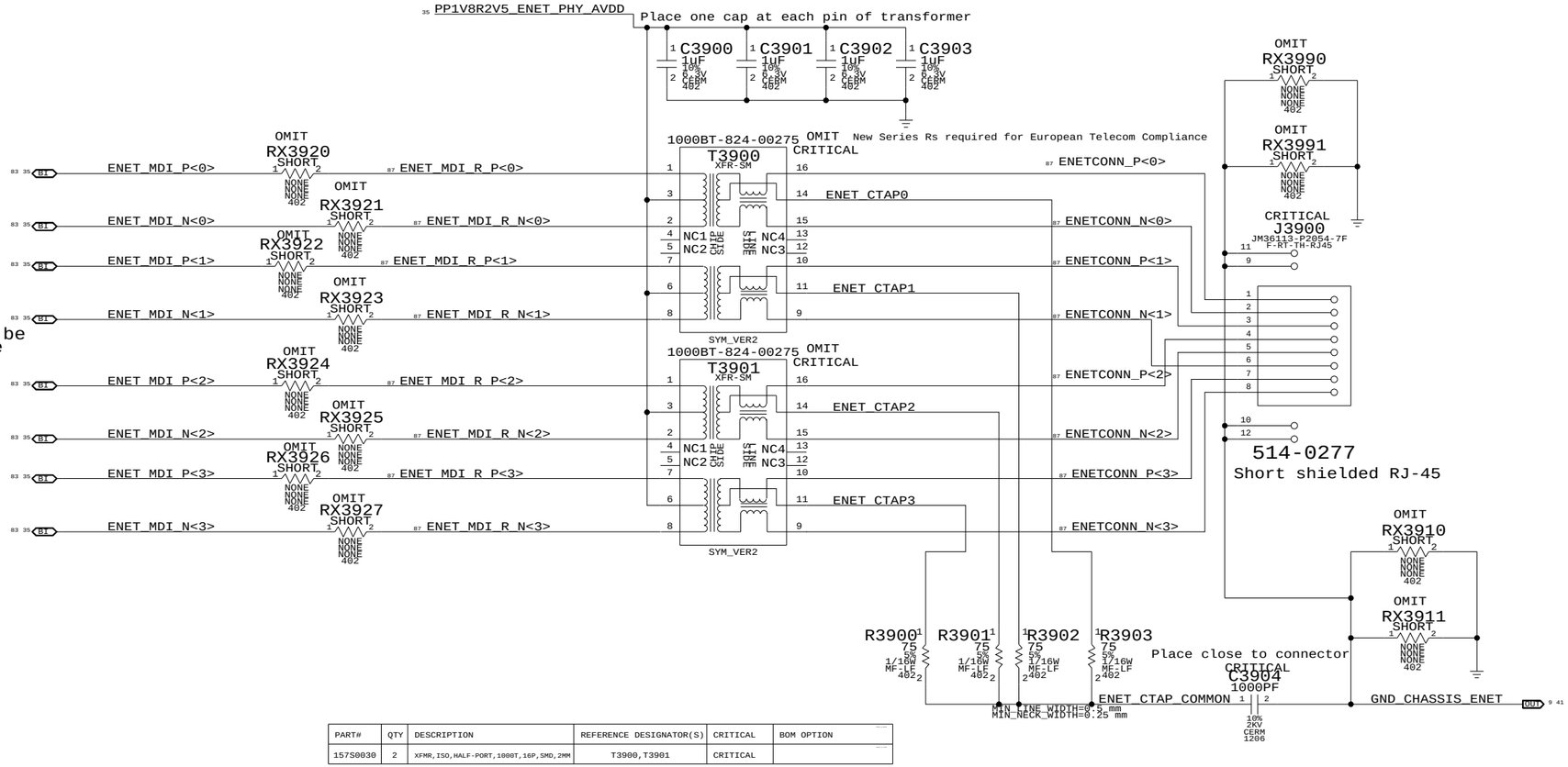
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 36 OF 88	

Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

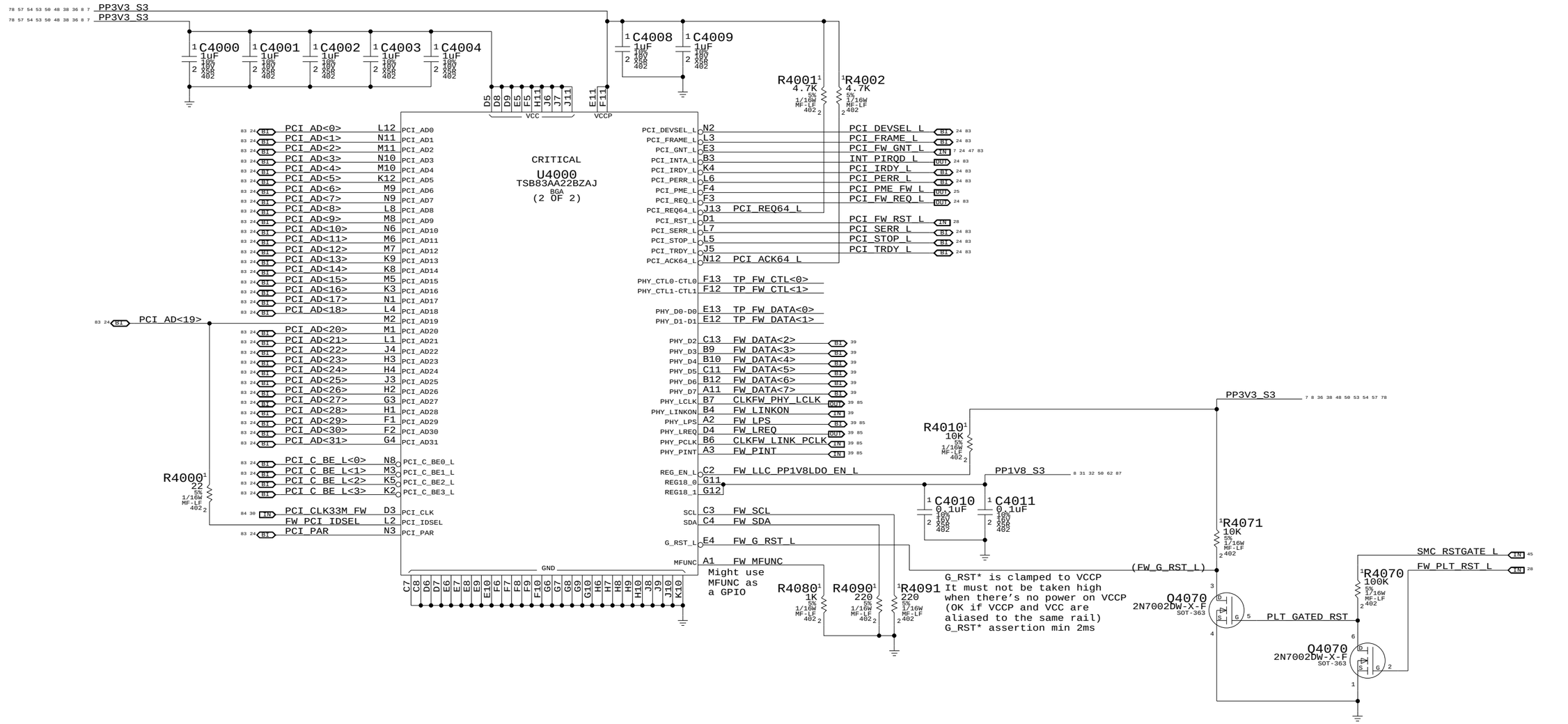
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0030	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 37 OF 88	



FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

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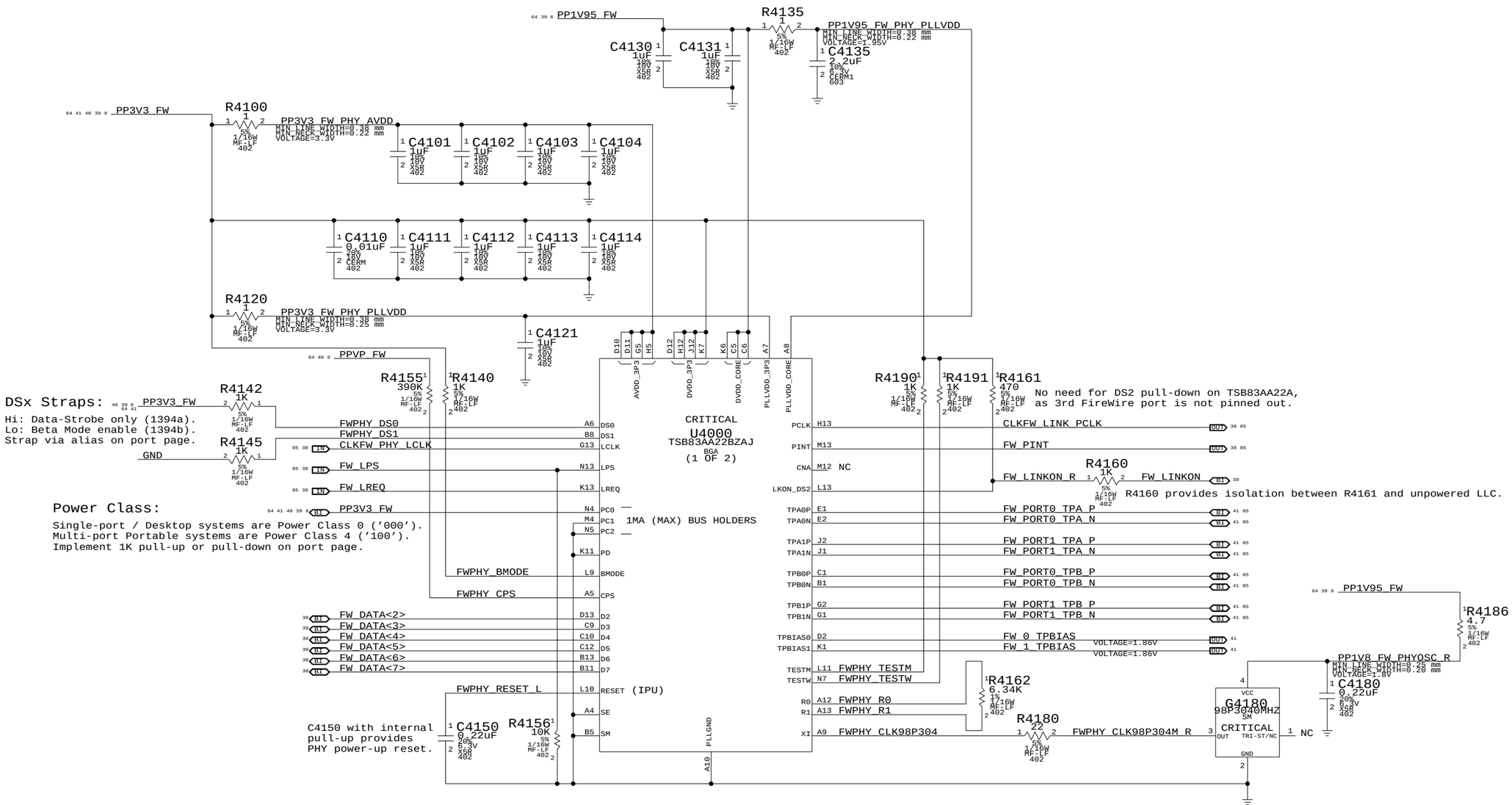
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE SHT 38 OF 88



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 39 OF 88	

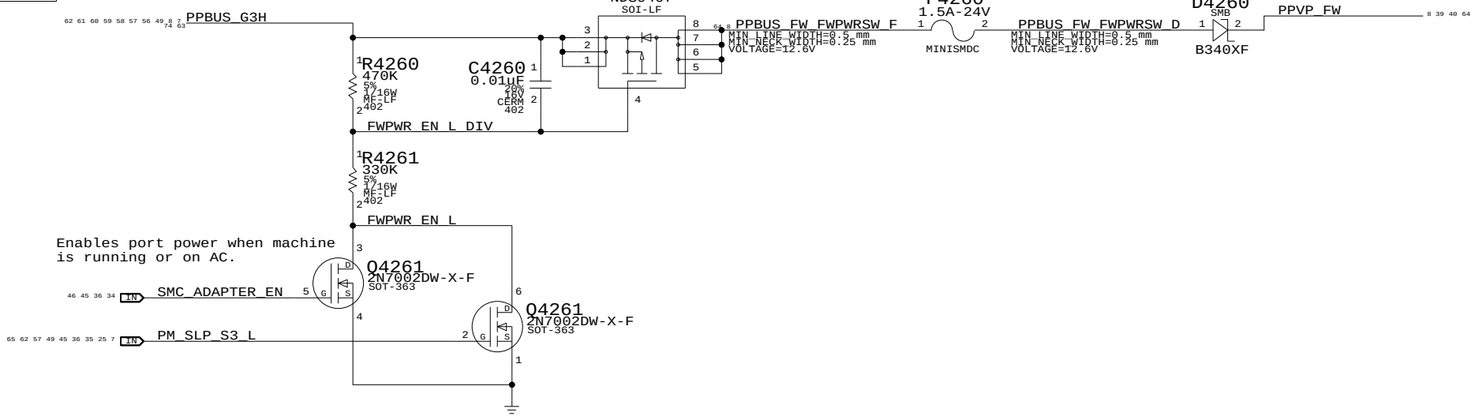
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

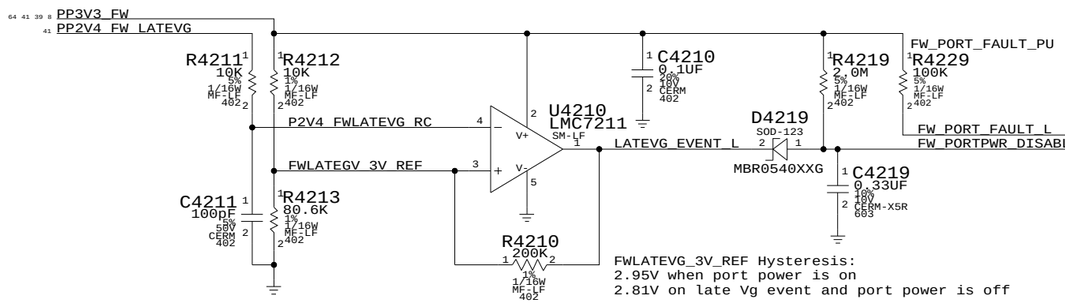
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch

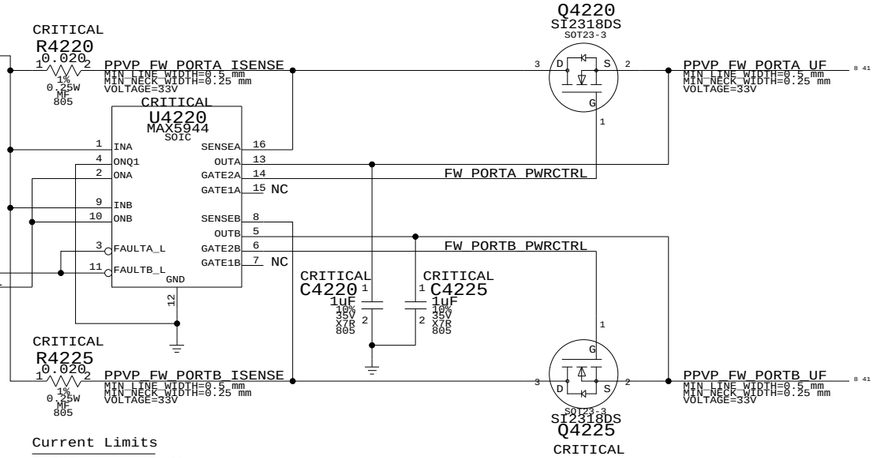


Late-Vg Event Detection



FWLATEVG_3V_REF Hysteresis:
2.95V when port power is on
2.81V on late Vg event and port power is off

Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 40 OF 88	

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

64 41 40 39 8 PP3V3_FW
41 40 39 8 PP3V3_FW
40 39 34 31 PP3V3_FW
GND

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39 FW_1_TPBIAS
39 FW_0_TPBIAS
C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402

CRITICAL L4360 18NH-250MA 0402 FW_B_TPA_L_P
CRITICAL L4361 18NH-250MA 0402 FW_B_TPA_L_N

R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

85 41 39 FW_PORT0_TPA_P — MAKE_BASE=TRUE — FW_PORT0_TPA_P 39 41 85
85 41 39 FW_PORT0_TPA_N — MAKE_BASE=TRUE — FW_PORT0_TPA_N 39 41 85
85 41 39 FW_PORT0_TPB_P — MAKE_BASE=TRUE — FW_PORT0_TPB_P 39 41 85
85 41 39 FW_PORT0_TPB_N — MAKE_BASE=TRUE — FW_PORT0_TPB_N 39 41 85
85 41 39 FW_PORT1_TPA_P — MAKE_BASE=TRUE — FW_PORT1_TPA_P 39 41 85
85 41 39 FW_PORT1_TPA_N — MAKE_BASE=TRUE — FW_PORT1_TPA_N 39 41 85
85 41 39 FW_PORT1_TPB_P — MAKE_BASE=TRUE — FW_PORT1_TPB_P 39 41 85
85 41 39 FW_PORT1_TPB_N — MAKE_BASE=TRUE — FW_PORT1_TPB_N 39 41 85

SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402

FW_B_TPB_L_N
FW_B_TPB_L_P
CRITICAL L4362 18NH-250MA 0402 SIGNAL_MODEL=EMPTY FW_PORT1_TPB_C
CRITICAL L4363 18NH-250MA 0402 SIGNAL_MODEL=EMPTY

FW_PORT0_TPB_C
C4354 220pF 5% 25V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

64 41 40 39 8 PP3V3_FW
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 40 41
CRITICAL D4390 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

Cable Power

CRITICAL L4300 FERR-250-OHM SM
Note: Trace PPVP_FW_PORT0 must handle up to 5A
40 8 PPVP_FW_PORTA_UF
PPVP_FW_PORT0 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4304 0.001uF 20% 50V CERM 402

"Snapback" & "Late VG" Protection

41 40 PP2V4_FW_LATEVG
DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402
DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402

85 41 39 FW_PORT0_TPA_P
85 41 39 FW_PORT0_TPA_N
85 41 39 FW_PORT0_TPB_P
85 41 39 FW_PORT0_TPB_N

CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1

87 FW_PORT0_TPA_FL_P
87 FW_PORT0_TPA_FL_N
87 FW_PORT0_TPB_FL_P
87 FW_PORT0_TPB_FL_N
(PPFW_PORT0_VP)
(GND_FW_PORT0_VG)
C4305 0.01uF 20% 50V CERM 603

43 41 9 GND_CHASSIS_RTUSB
OMIT CX4300 SHORT
OMIT CX4301 SHORT

PORT 0
1394A
CRITICAL J4300 1394A F-RT-TH-LF
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
514-0255

GND_CHASSIS_RTUSB 9 41 43
41 37 9 GND_CHASSIS_ENET
OMIT CX4302 SHORT
OMIT CX4303 SHORT

Cable Power

CRITICAL L4310 FERR-250-OHM SM
Note: Trace PPVP_FW_PORT1 must handle up to 5A
40 8 PPVP_FW_PORTB_UF
PPVP_FW_PORT1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4314 0.001uF 20% 50V CERM 402

"Snapback" & "Late VG" Protection

41 40 PP2V4_FW_LATEVG
DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402
DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402

85 41 39 FW_PORT1_TPB_N
85 41 39 FW_PORT1_TPB_P
85 41 39 FW_PORT1_TPA_N
85 41 39 FW_PORT1_TPA_P

(FW_PORT1_BREF)
(PPVP_FW_PORT1)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402
NO STUFF C4317 0.01uF 20% 16V CERM 402
C4315 0.01uF 20% 50V CERM 603

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

41 37 9 GND_CHASSIS_ENET
OMIT CX4304 SHORT
OMIT CX4305 SHORT

PORT 1
BILINGUAL
CRITICAL J4310 1394B-UG31903 F-RT-SM1
TPB- 1
TPB<R> 9 OUTPUT
TPB+ 2
VP 8
NC 7
VG 6
TPA- 3
TPA<R> 5 INPUT
TPA+ 4
514S0133

GND_CHASSIS_ENET
OMIT CX4306 SHORT
OMIT CX4307 SHORT

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

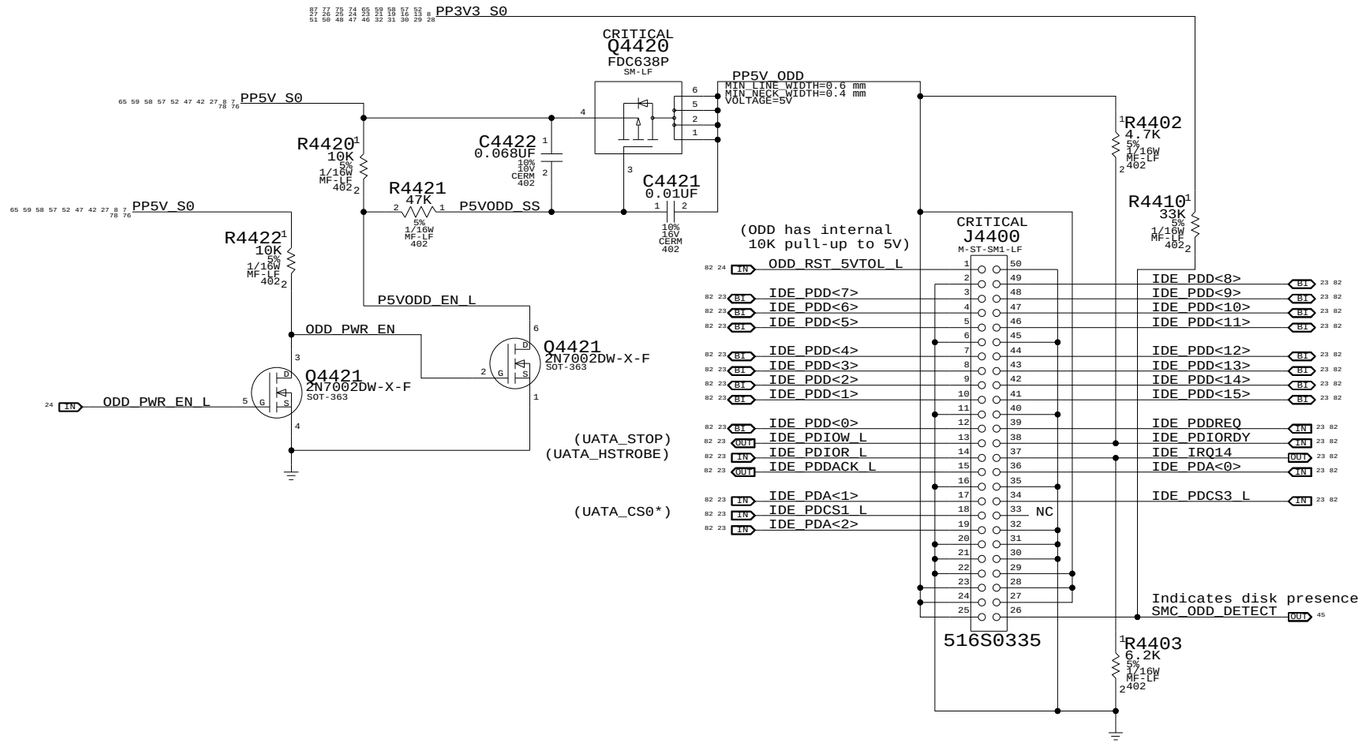
FireWire Ports

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

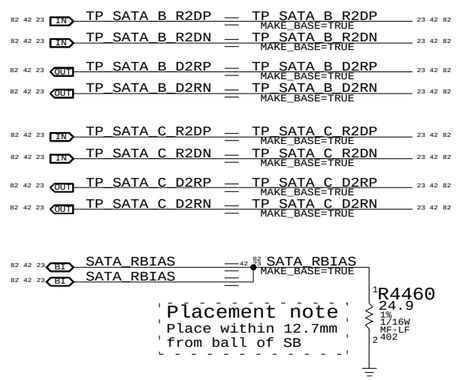
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 41 OF 88	

IDE (ODD) Connector



Unused SATA Ports



PATA Connector	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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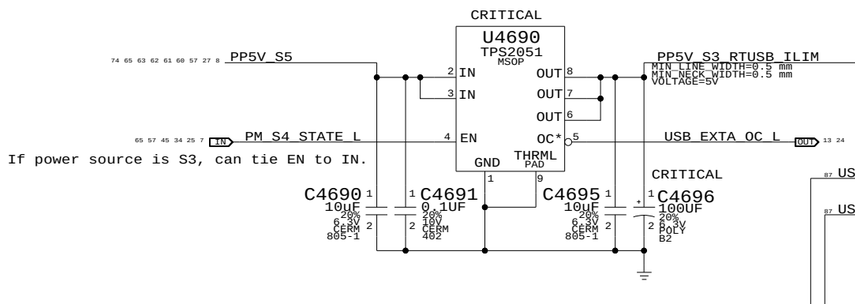
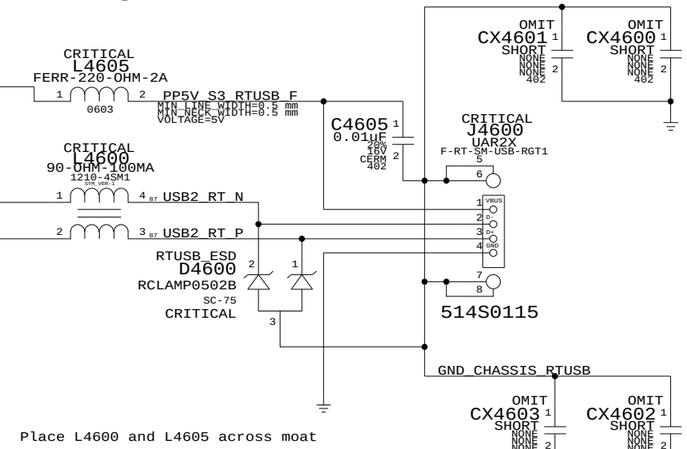
	D	051-7225	10.0.0
	SCALE: NONE	SHT 42 OF 88	

Port Power Switch

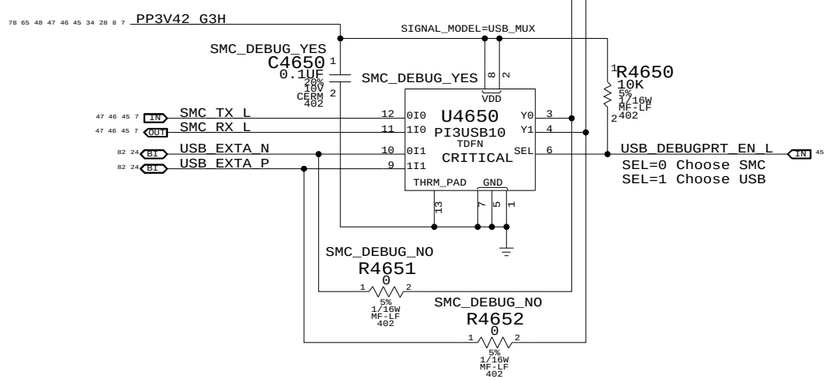


Right USB Port



Place L4600 and L4605 across moat

USB/SMC Debug Mux



External USB Connector

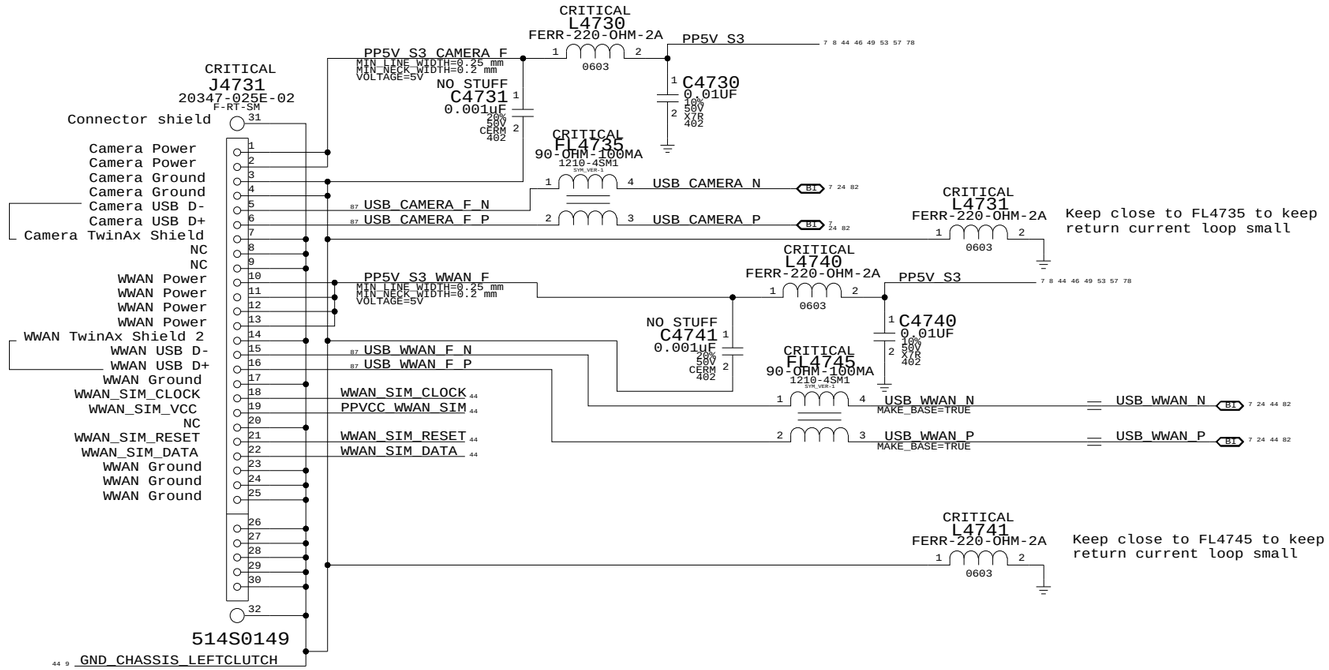
SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

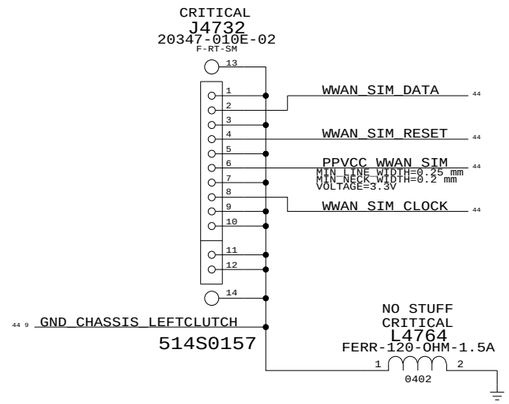
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	43	88

Left Clutch Barrel Interconnect



SIM Interconnect



Left Clutch Barrel Interconnect

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

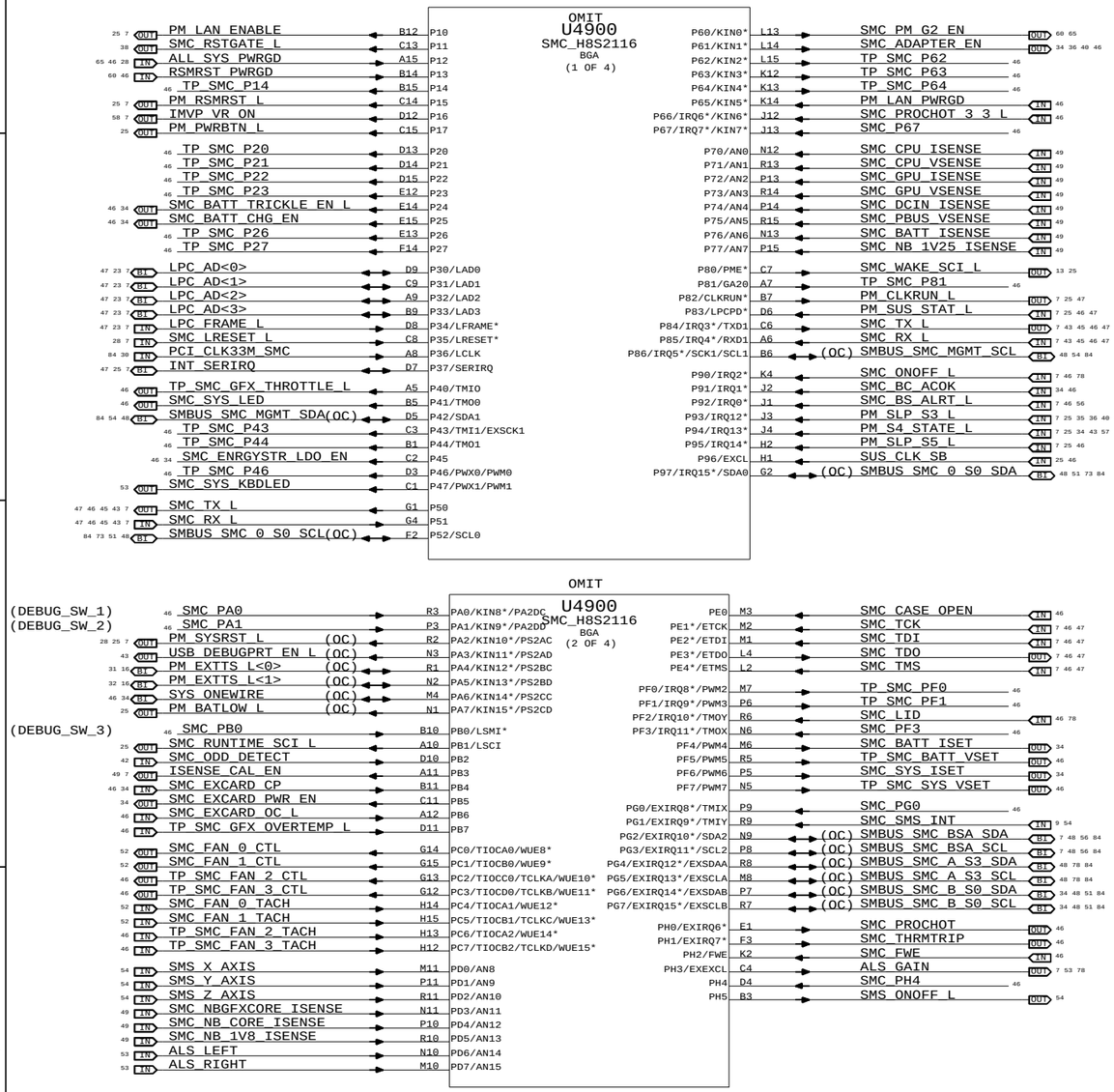
APPLE COMPUTER INC.

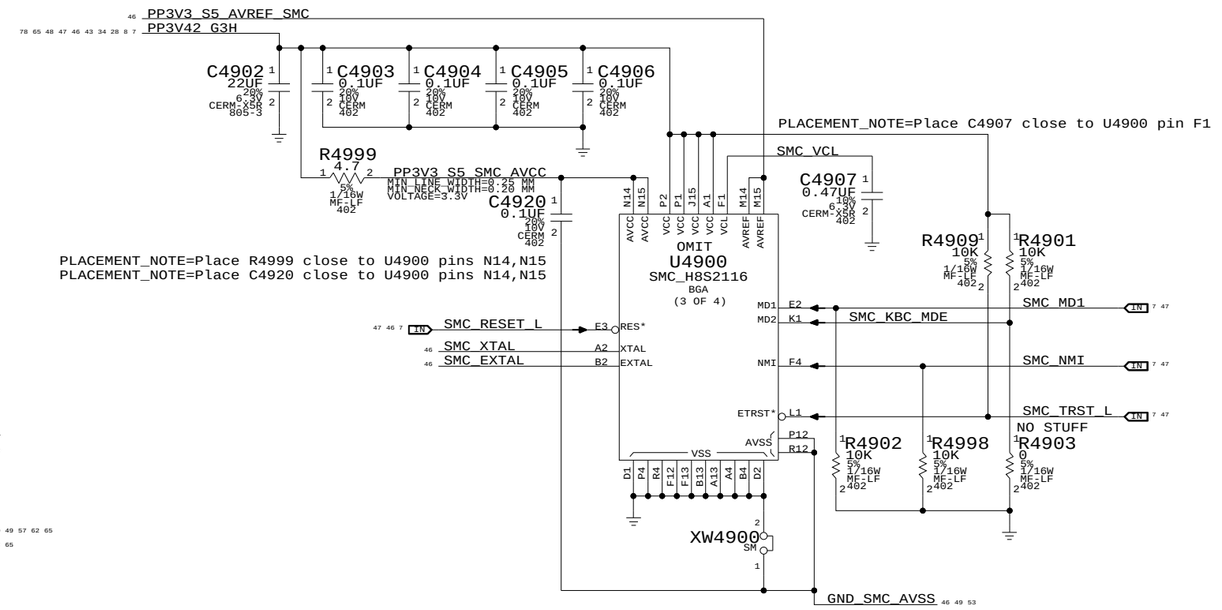
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE

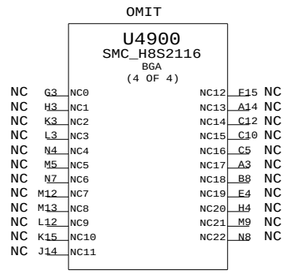
SHT 44 OF 88

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



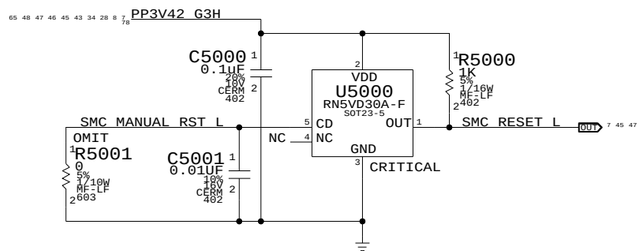
SMC

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

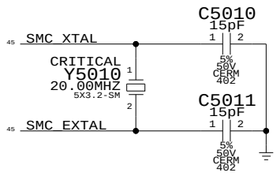
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 45 OF 88	

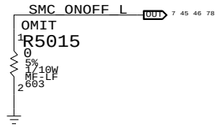
SMC Reset "Button" / Brownout Detect



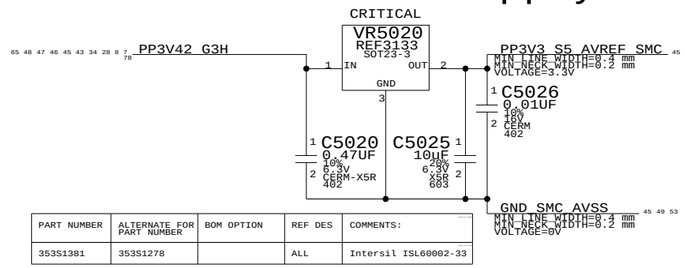
SMC Crystal Circuit



Debug Power "Button"

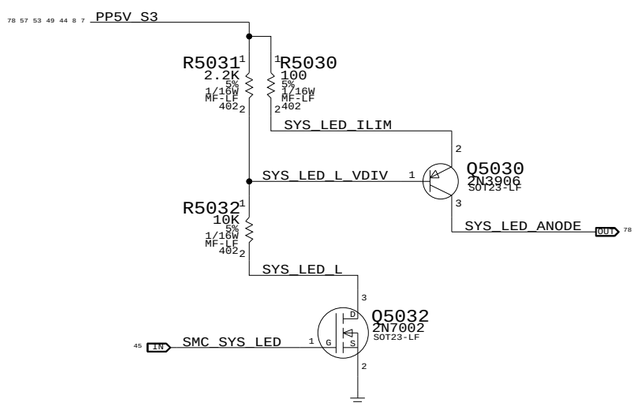


SMC AVREF Supply

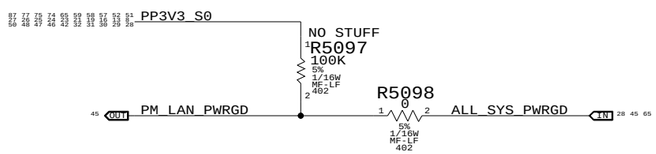


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit

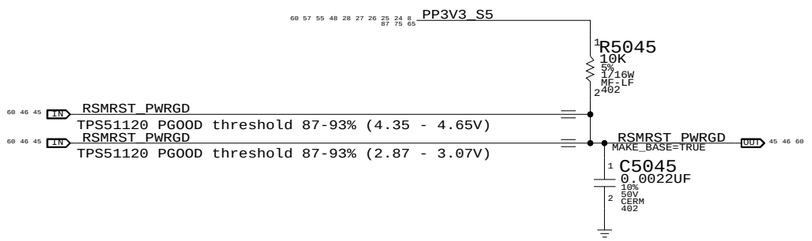


LAN PWRGD Circuit

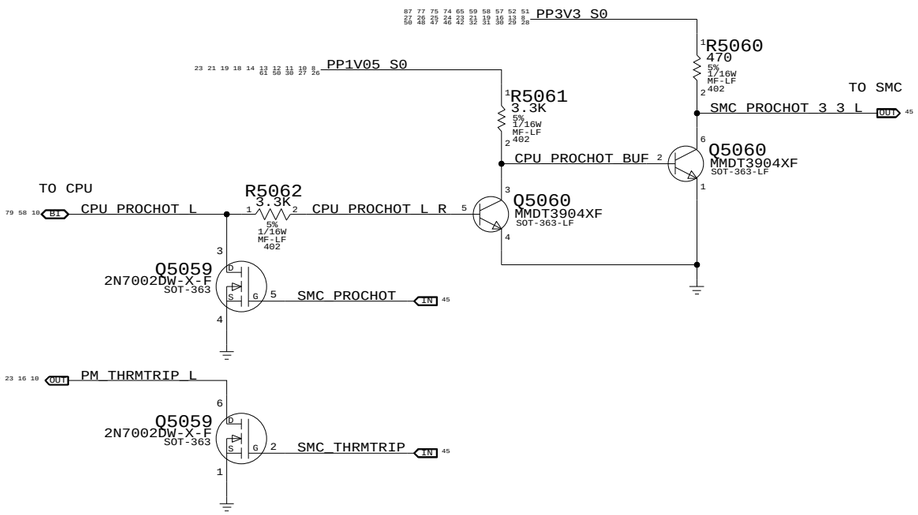


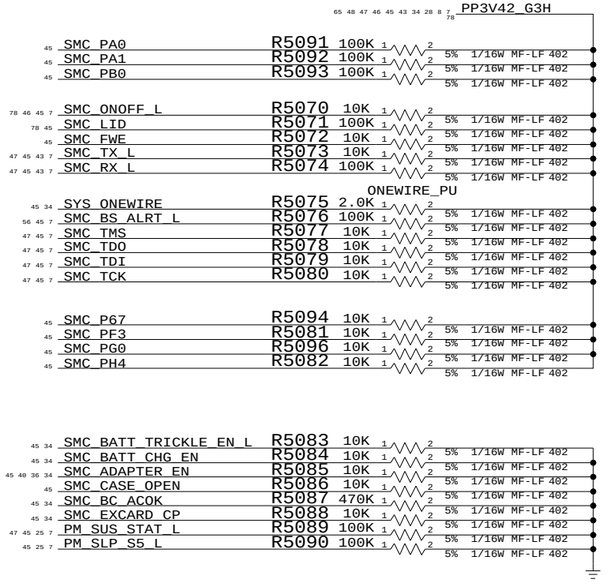
S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting





SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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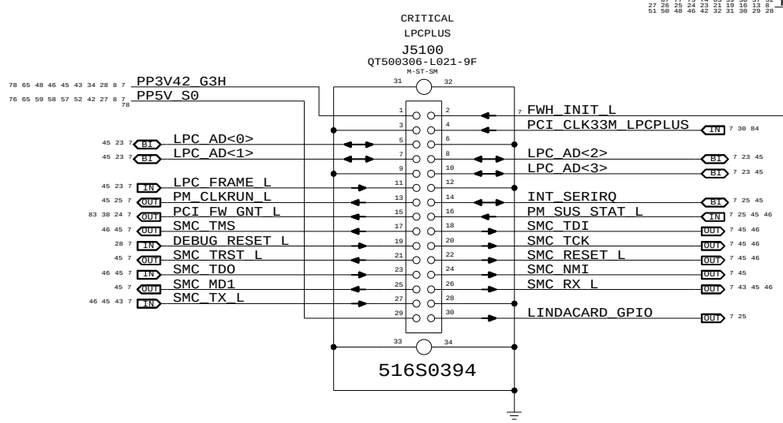
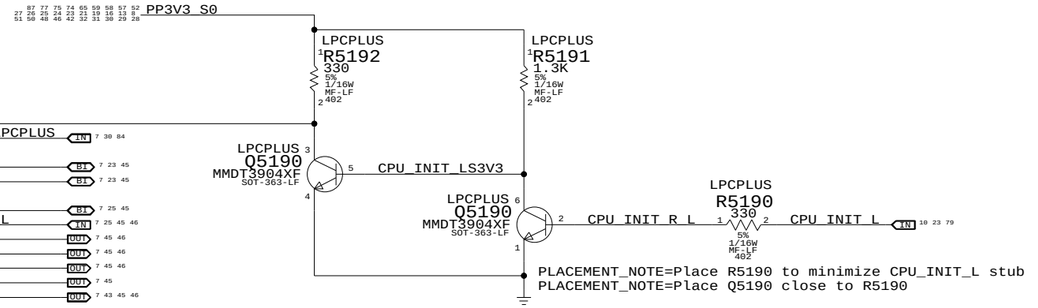
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 46 OF 88	

LPC+ Connector



FWH_INIT_L Generation



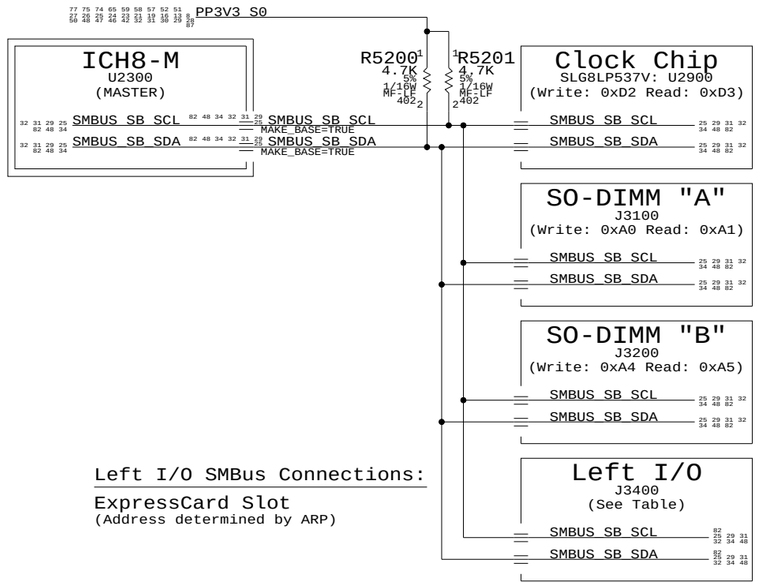
LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 47 OF 88	

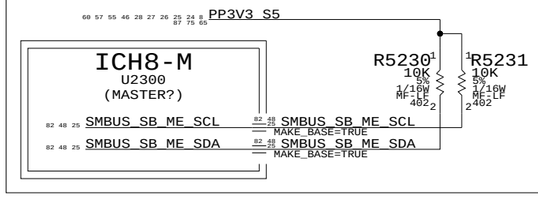
ICH8-M SMBus Connections



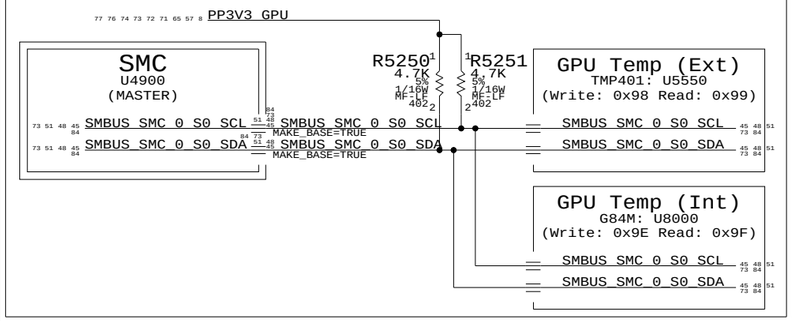
Left I/O SMBus Connections:

ExpressCard Slot
(Address determined by ARP)

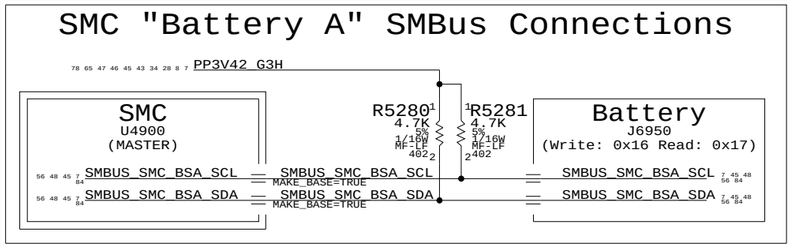
ICH8-M ME SMBus Connections



SMC "0" SMBus Connections

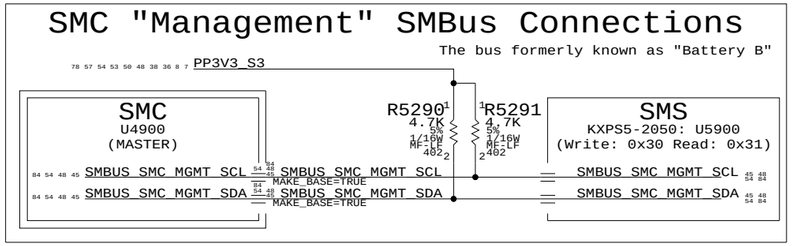


SMC "Battery A" SMBus Connections



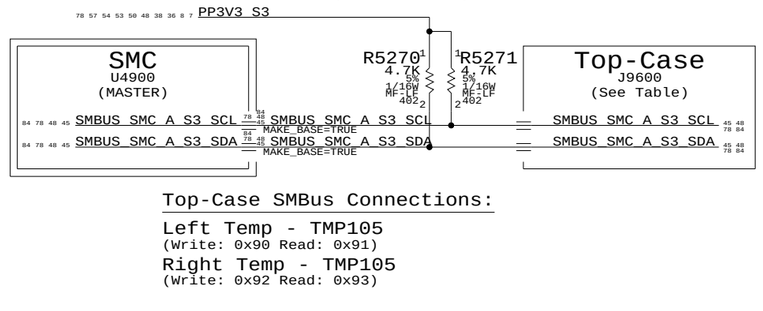
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

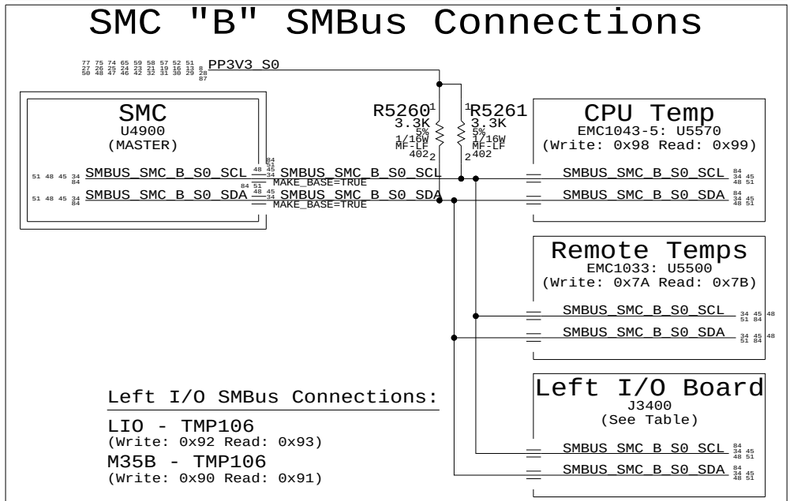


Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

SMC "B" SMBus Connections



Left I/O SMBus Connections:

LIO - TMP106
(Write: 0x92 Read: 0x93)

M35B - TMP106
(Write: 0x90 Read: 0x91)

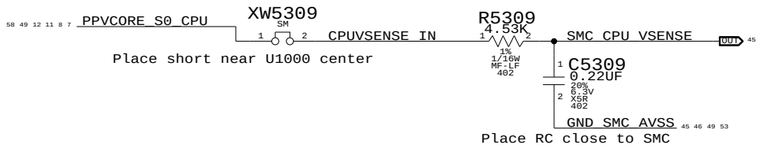
SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

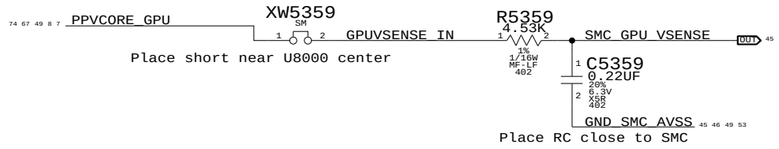
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 48 OF 88	

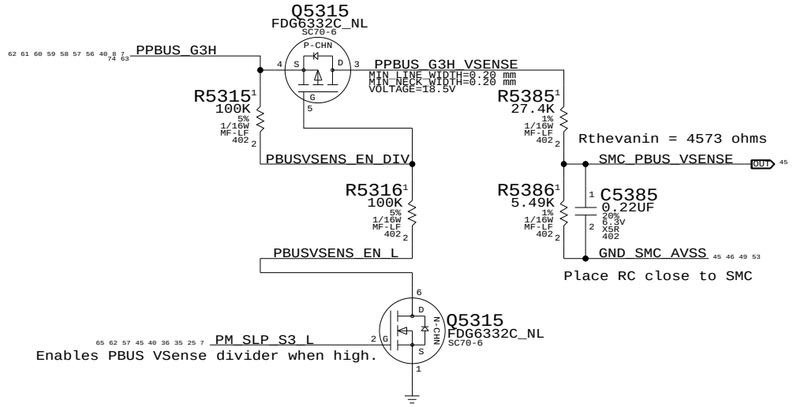
CPU Voltage Sense / Filter



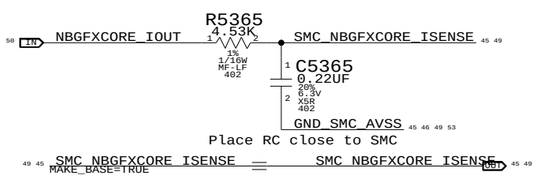
GPU Voltage Sense / Filter



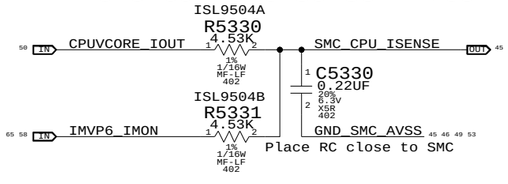
PBUS Voltage Sense & Filter



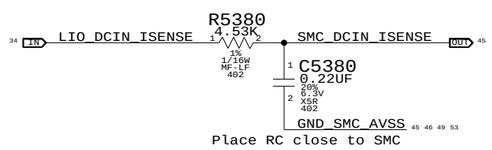
NB GFX Current Sense Filter



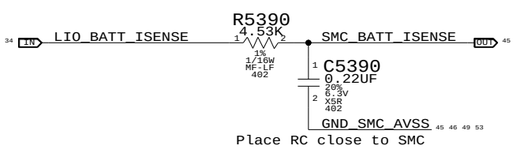
CPU Current Sense Filter



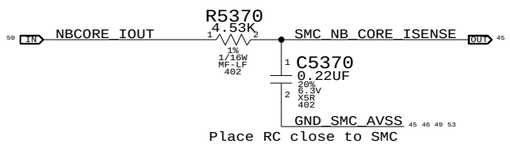
DCIN Current Sense Filter



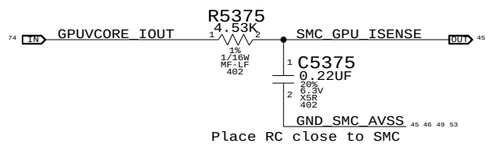
Battery (PBUS) Current Sense Filter



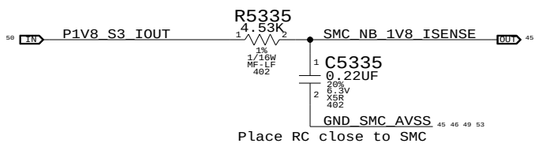
NB Core Current Sense Filter



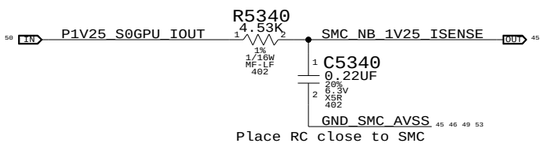
GPU Current Sense Filter



NB 1.8V Current Sense Filter

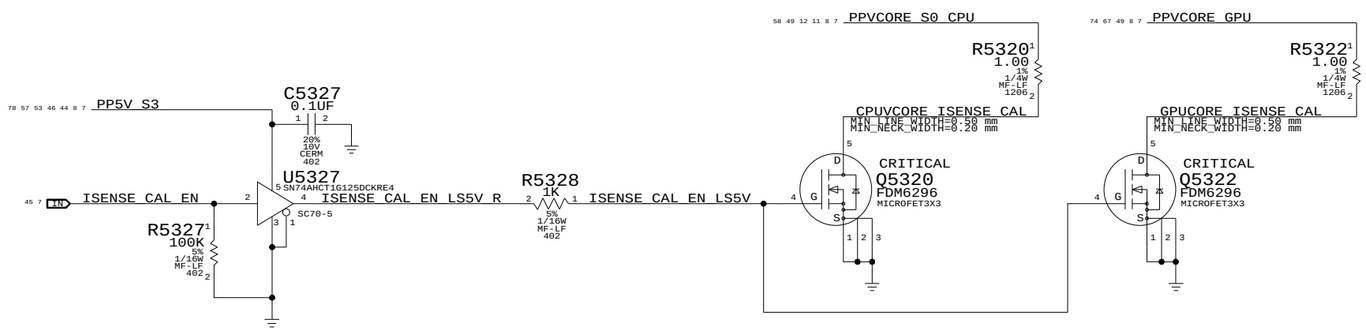


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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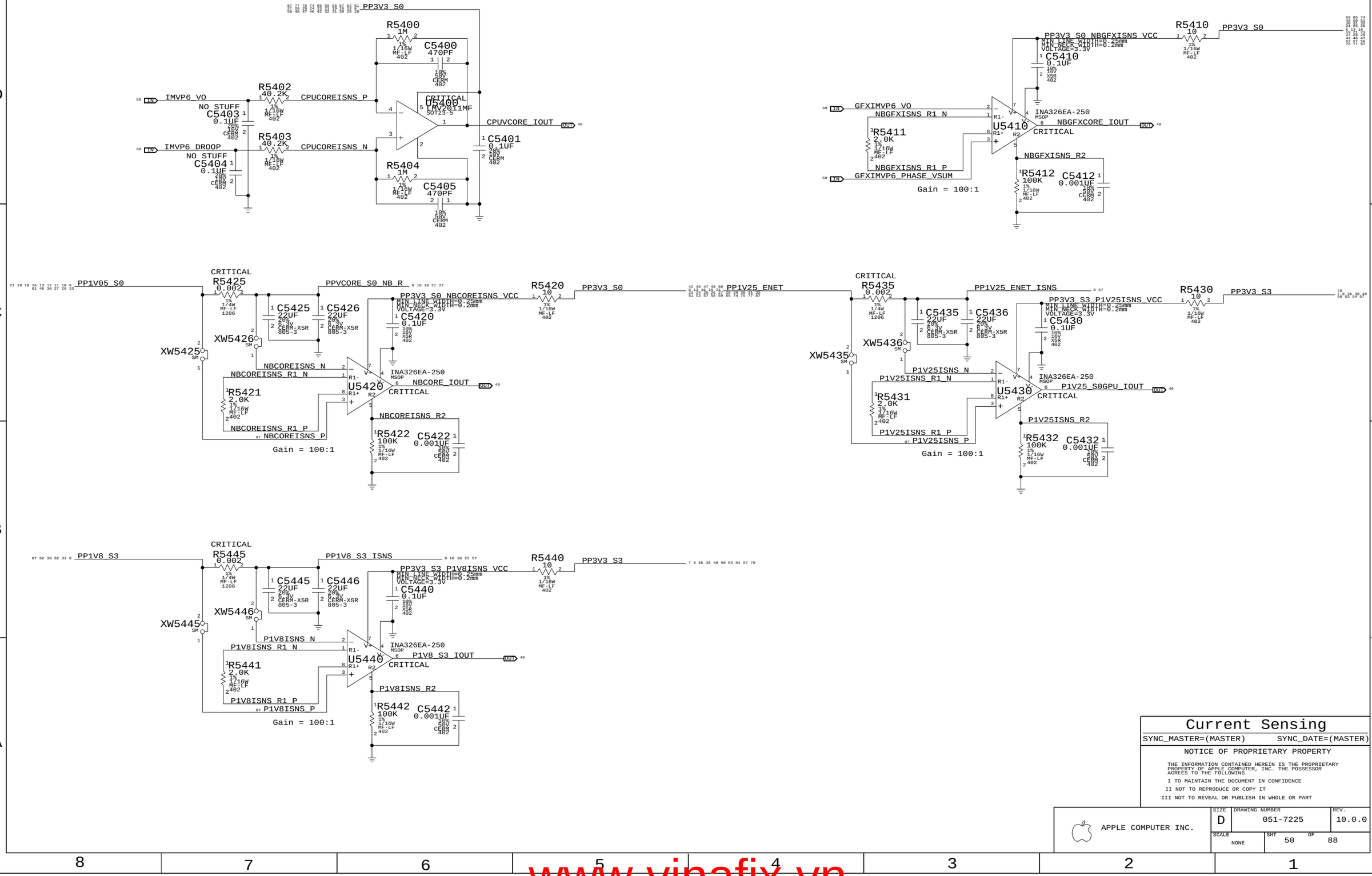
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 49 OF 88	



Current Sensing

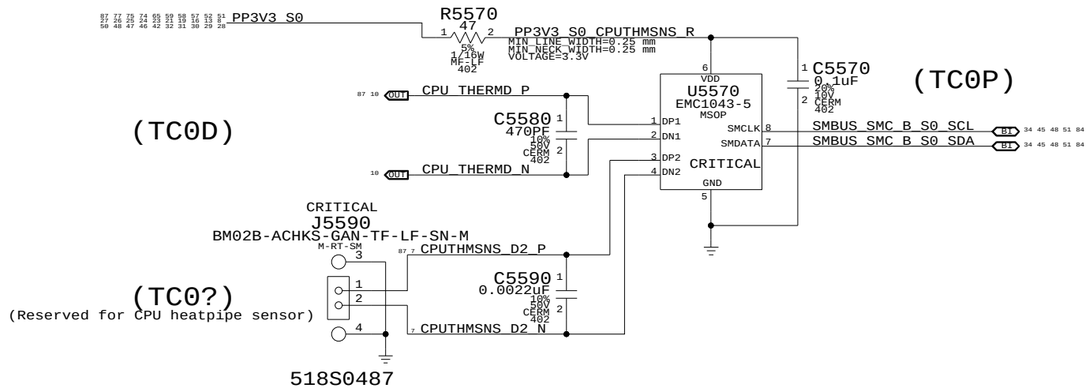
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

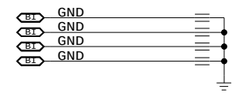
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	50	88

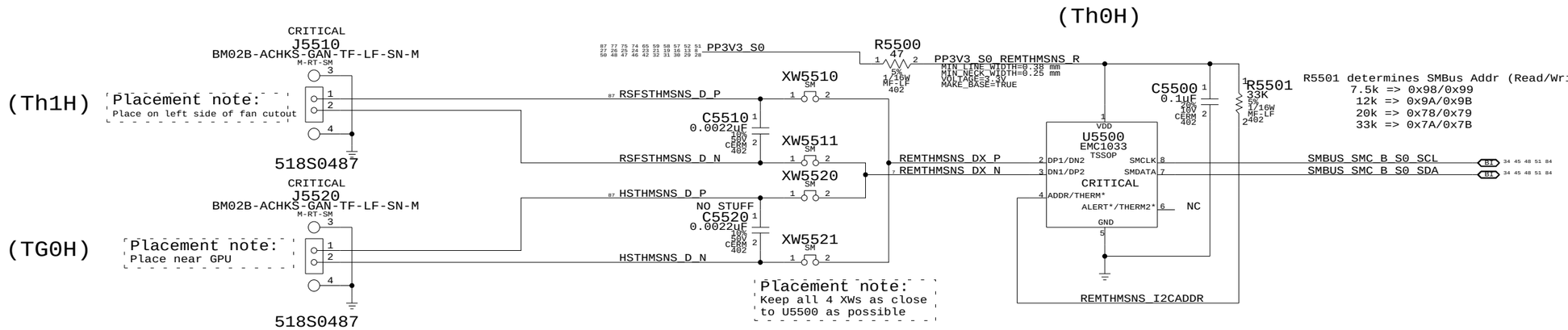
CPU T-Diode Thermal Sensor



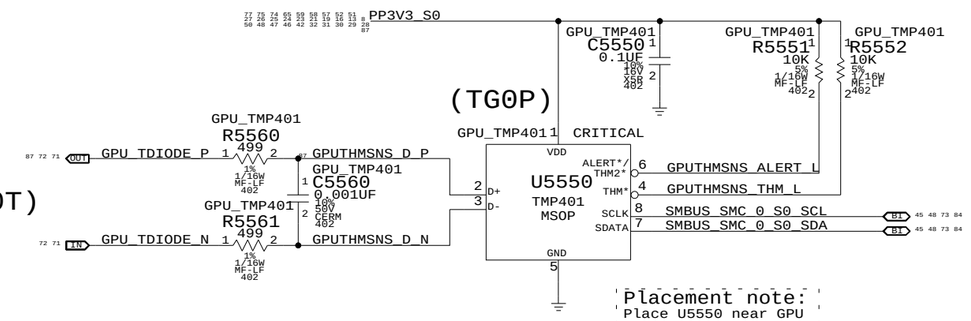
NB Thermal Diodes Not Used



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



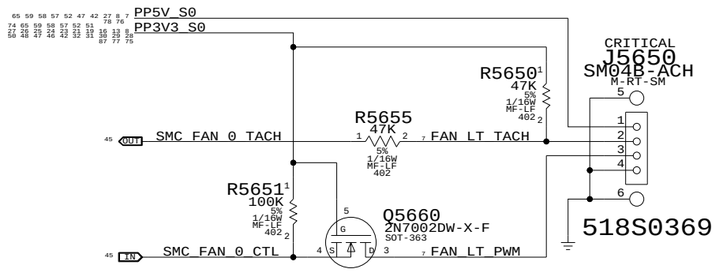
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

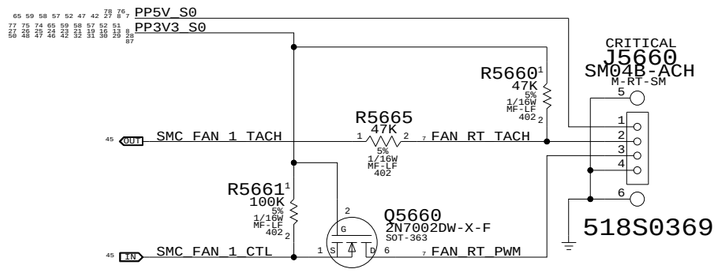
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 51 OF 88	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

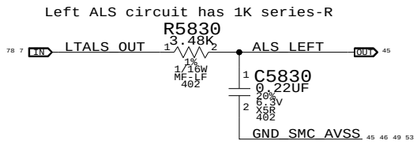
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

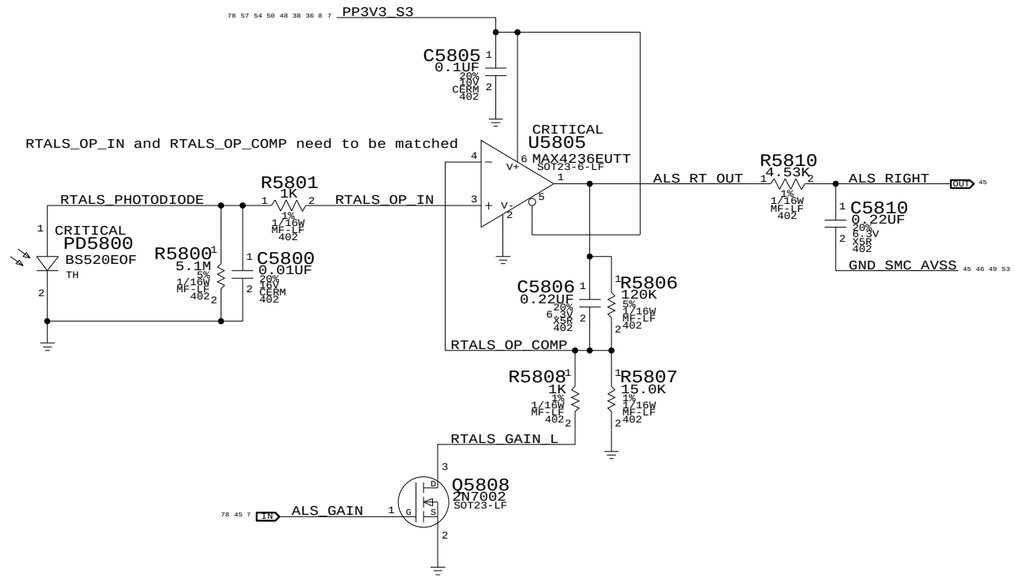
SCALE: NONE

SHT 52 OF 88

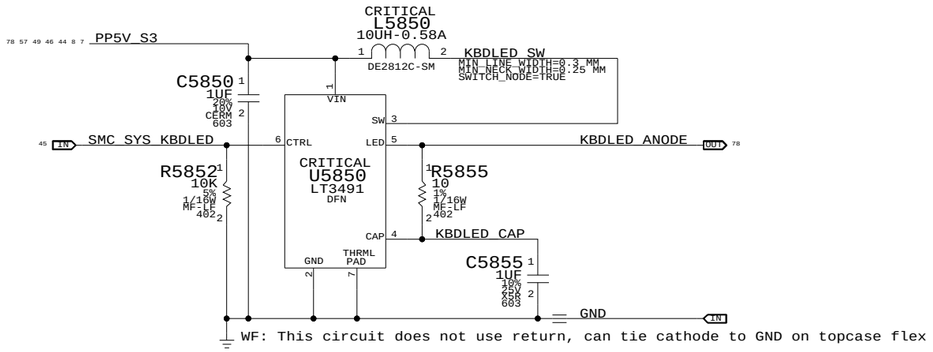
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



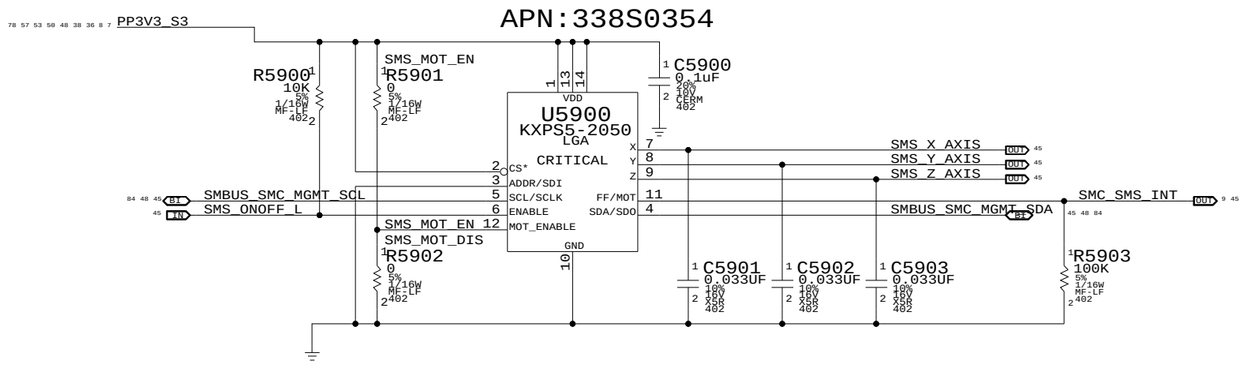
ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 53 OF 88	

APN:338S0354

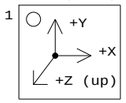


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

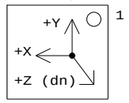
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



Sudden Motion Sensor (SMS)

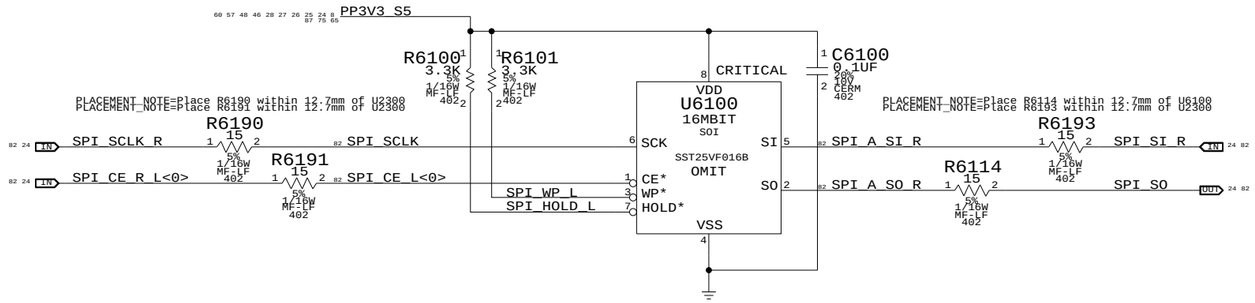
SYNC_MASTER=M76_MLB SYNC_DATE=01/18/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE

SHT 54 OF 88



SPI BootROM

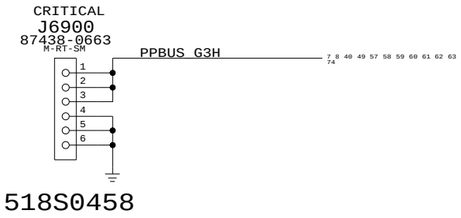
SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

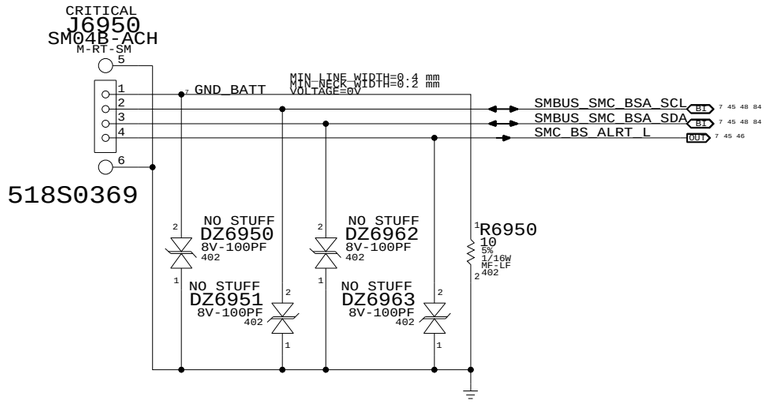
SCALE	SHT	OF
NONE	55	88

Left I/O Power Connector



518S0458

Battery Connector (Digital Signals)



518S0369

PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

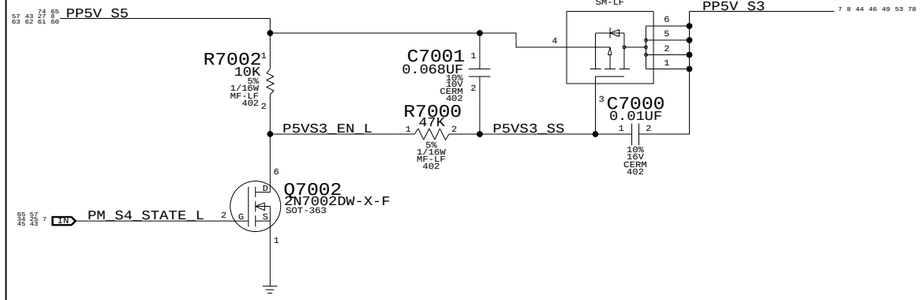
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

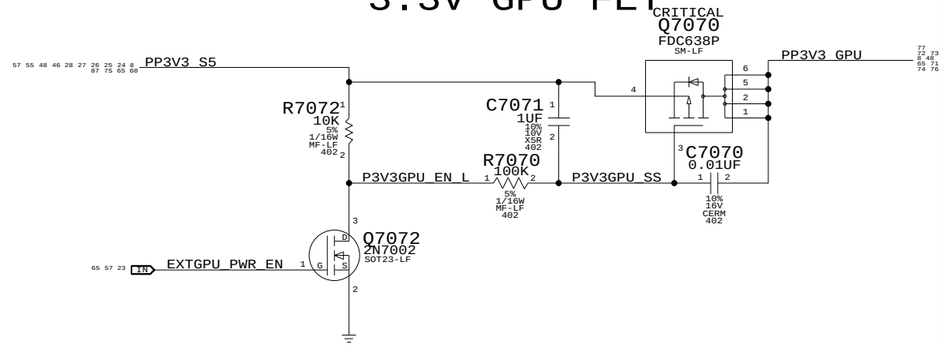
SCALE: NONE

SHT 56 OF 88

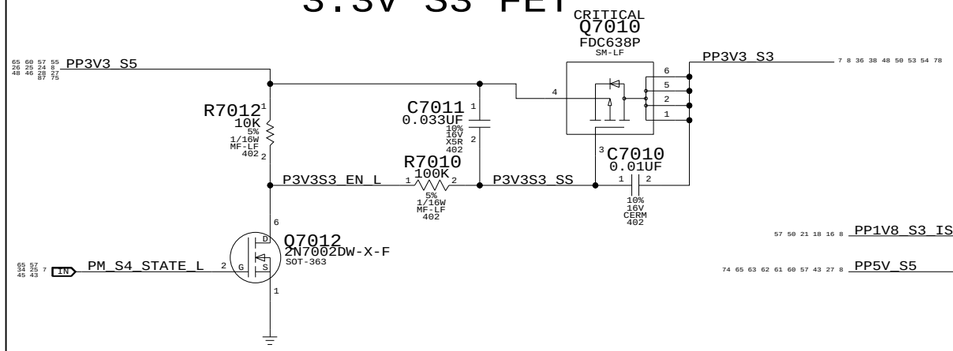
5V S3 FET



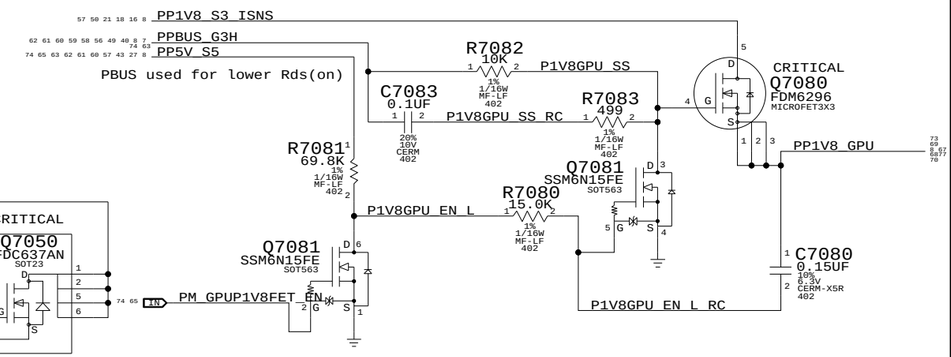
3.3V GPU FET



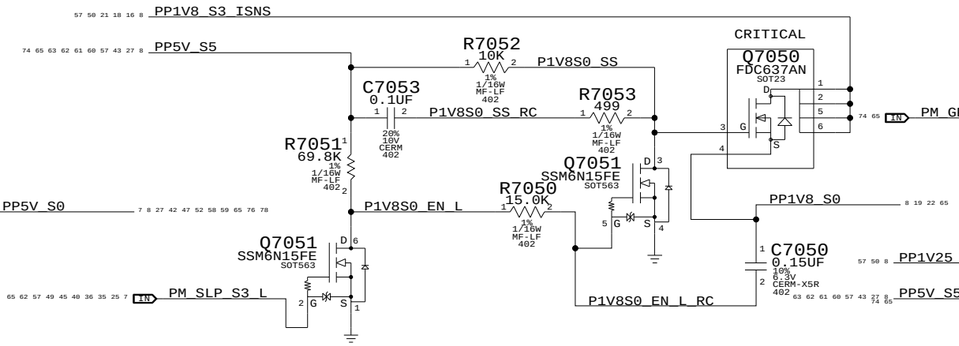
3.3V S3 FET



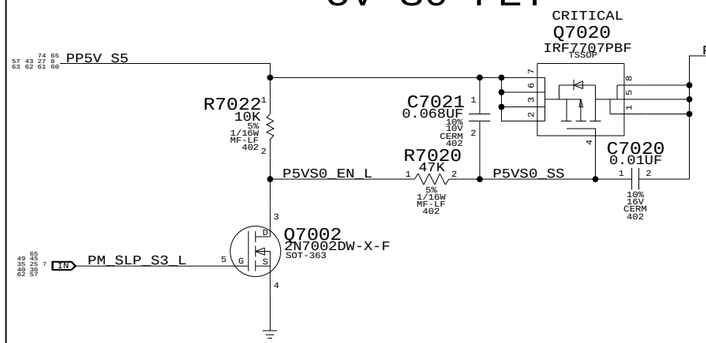
1.8V GPU FET



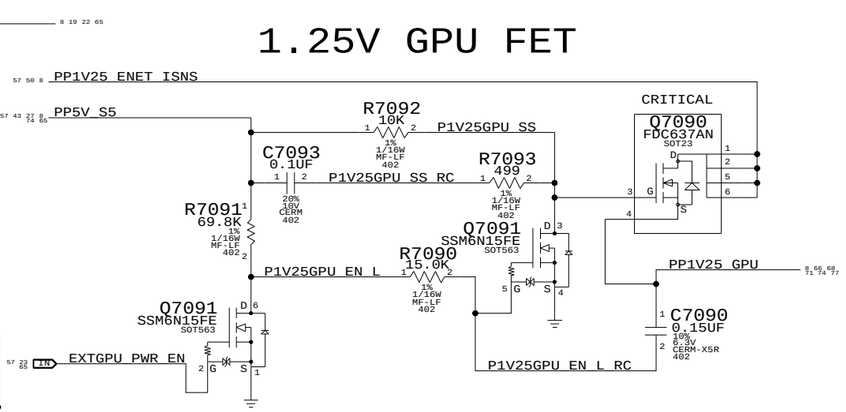
1.8V S0 FET



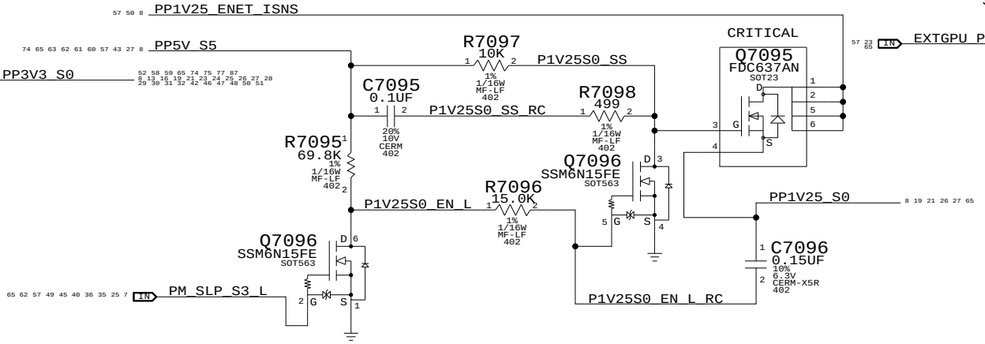
5V S0 FET



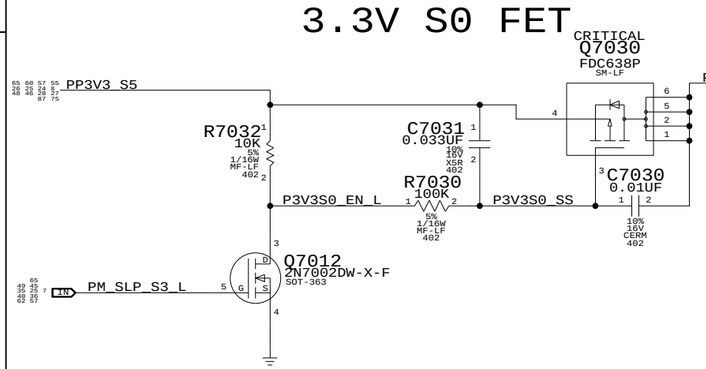
1.25V GPU FET



1.25V S0 FET



3.3V S0 FET



Power FETs

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 57 OF 88	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

PPBUS_G3H

PP5V_S0

PP3V3_S0

PM_DPRSLPVR

CPU_PROCHOT_L

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

IMVP6_NTC_R

IMVP6_VDIFF_RC

IMVP6_COMP_RC

PPVIN_S5_IMVP6_VIN
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V

PP5V_S0_IMVP6_VDD
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V

PP3V3_S0_IMVP6_3V3
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

GND_IMVP6_SGND
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

SIGNAL_MODEL=EMPTY

IMVP6_VID<6>
IMVP6_VID<5>
IMVP6_VID<4>
IMVP6_VID<3>
IMVP6_VID<2>
IMVP6_VID<1>
IMVP6_VID<0>
CPU_DPRSTP_L
IMVP_DPRSLPVR
CPU_PSI_L
IMVP6_IMON
VR_PWRGD_CLKEN_L
IMVP_VR_ON
VR_PWRGOOD_DELAY
IMVP6_VR_TT_L
IMVP6_NTC
(GND_IMVP6_SGND)
IMVP6_SOFT
IMVP6_RBIAS
(GND_IMVP6_SGND)
IMVP6_VDIFF
IMVP6_FB2
IMVP6_FB
IMVP6_COMP
IMVP6_VW

U7100 ISL9504BCRZ QFN
VIN VDD PVCC
BOOT1 BOOT2 UGATE1 PHASE1 LGATE1 PGND1 ISEN1
UGATE2 PHASE2 LGATE2 PGND2 ISEN2
VSUM OCSET VO DROOP DFB VSEN RTN
VID6 VID5 VID4 VID3 VID2 VID1 VID0
DPRSTP* DPRSLPVR PSI* IMON (PGD_IN) (ISL9504A)
3V3 CLK_EN* VR_ON PGOOD VR_TT* NTC SOFT RBIAS VDIFF FB2 FB COMP VW NC
GND TPAD

IMVP6_BOOT1
IMVP6_BOOT2
IMVP6_UGATE1
IMVP6_PHASE1
IMVP6_LGATE1
(GND)
IMVP6_ISEN1
IMVP6_UGATE2
IMVP6_PHASE2
IMVP6_LGATE2
(GND)
IMVP6_ISEN2
IMVP6_VSUM
IMVP6_OCSET
IMVP6_VO
IMVP6_DROOP
IMVP6_DFB

(IMVP6_PHASE1)
(IMVP6_ISEN1)
(IMVP6_PHASE2)
(IMVP6_ISEN2)
(IMVP6_VSUM)
(IMVP6_VO)
(IMVP6_NTC)
(IMVP6_FB)
(IMVP6_VW)
(IMVP6_COMP)
IMVP6_VO_R

CRITICAL Q7100 RJK0305DPB LFPAK
CRITICAL Q7101 RJK0301DPB LFPAK
CRITICAL Q7104 RJK0301DPB LFPAK
CRITICAL Q7102 RJK0305DPB LFPAK
CRITICAL Q7103 RJK0301DPB LFPAK
CRITICAL Q7105 RJK0301DPB LFPAK

CRITICAL L7100 0.36UH-27A FDUE1030D-SM
CRITICAL L7101 0.36UH-27A FDUE1030D-SM

XW7103 XW7104 XW7101 XW7102 XW7100 SM

IMVP6_VSUM1
IMVP6_VO1
IMVP6_VSUM2
IMVP6_VO2

PPVCORE_S0_CPU
44A MAX CURRENT

IMVP6_VSEN_P
IMVP6_VSEN_N
CPU_VCCSENSE_P
CPU_VCCSENSE_N

NO STUFF C7100 0.0022UF
NO STUFF C7102 0.0022UF
NO STUFF C7116 0.001UF
NO STUFF C7132 0.01UF

IMVP6_OCSET MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VO MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_DROOP MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_DFB MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_SOFT MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_RBIAS MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VDIFF MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_FB2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_FB MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_COMP MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VW MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM

IMVP6_PHASE1 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_ISEN1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VO1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_P MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM

IMVP6_PHASE2 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_ISEN2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VO2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_N MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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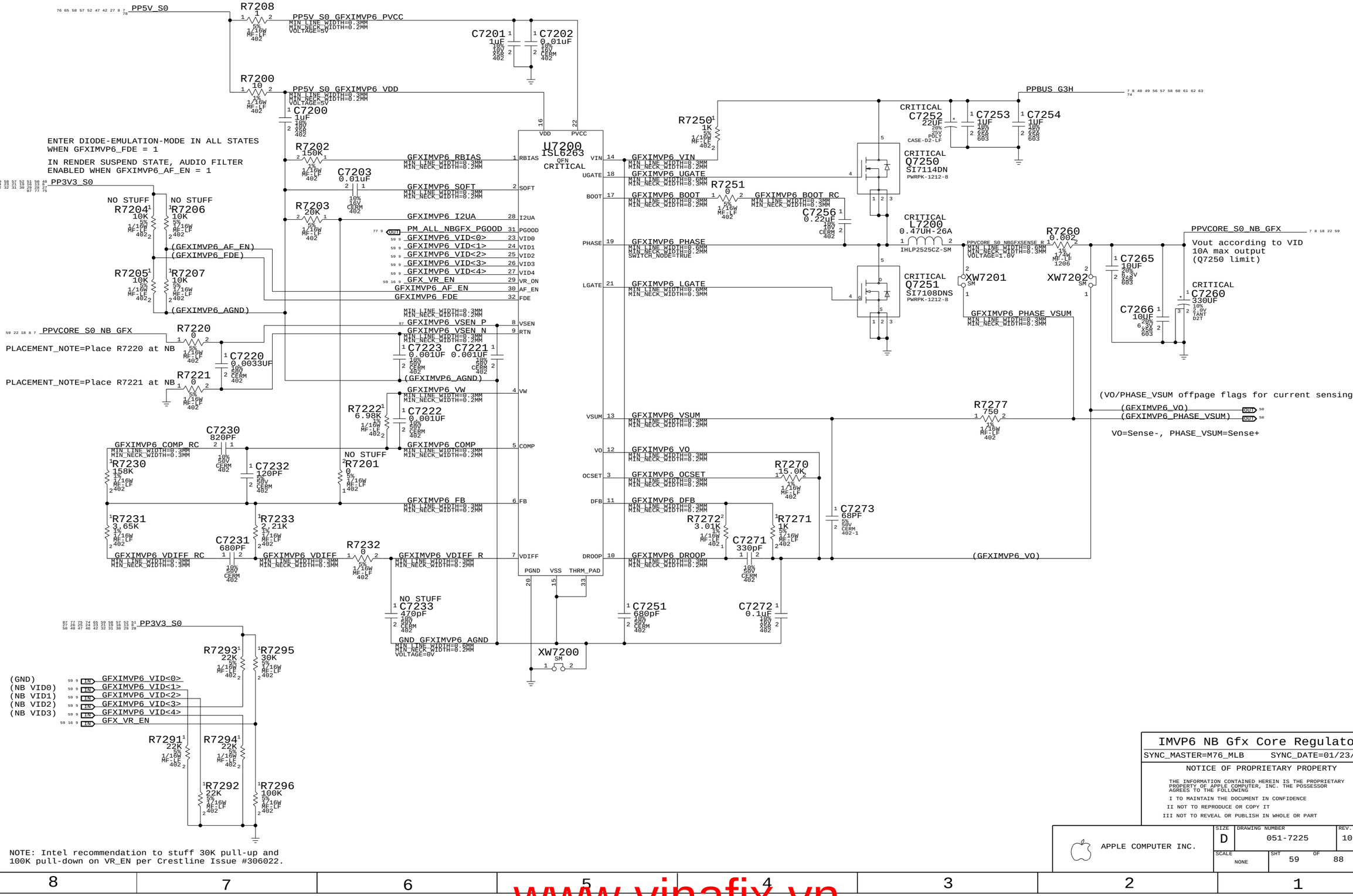
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 58 OF 88	



TPS51120 LDO/Buffer outputs

(Available for system use)

PP2V0_S5_P5VP3V3_BUF — 50uA max load when EN5 & EN3 high

PP5V_S5_P5VP3V3_LDO — 100mA max load when EN5 high

PPBUS_G3H

C7300 1UF 10% 25V X5R 603

PP5V_S5_P5VP3V3_LDO — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.20 mm, VOLTAGE=5V

P5VP3V3_VREG3

C7303 10UF 20% 6.3V X5R 603

C7305 10UF 20% 6.3V X5R 603

PP2V0_S5_P5VP3V3_BUF — MIN_LINE_WIDTH=0.20 mm, MIN_NECK_WIDTH=0.20 mm, VOLTAGE=2V

PPBUS_G3H

CRITICAL C7340 22UF 20% 25V POLY CASE-D2-LF

C7341 1UF 10% 25V X5R 603

R7306 4.7 5% 1/10W MF-LF 402

C7302 0.001UF 10% 50V CERM 402

PP5V_S5_P5VP3V3_V5FILT — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V

R7325 4.22K 1% 1/16W MF-LF 402

C7306 1UF 10% 10V X5R 402

P5VS5_VBST_RC — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm

C7324 0.1UF 20% 10V CERM 402

R7324 0 5% 1/16W MF-LF 402

PP5V_S5

Vout = 5.0V
8A max output
(L7320 limit)

CRITICAL Q7320 SI7114DN PWRPK-1212-8

CRITICAL L7320 2.2UH-14A IHLP2525CZ-SM

CRITICAL C7352 330UF 20% 6.3V POLY D3L

C7350 10UF 20% 10V CERM 805-2

C7351 10UF 20% 10V CERM 805-2

CRITICAL Q7325 SI7108DNS PWRPK-1212-8

XW7320 SM

XW7325 SM

PLACEMENT_NOTE=Place XW7320 next to C7350.

MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

CRITICAL U7300 TPS51120 LLP

SYM (3 OF 3)

32	SKIPSEL	EN5	9
31	TONSEL	EN3	10
28	VBST1	VBST2	13
27	DRVH1	DRVH2	14
26	LL1	LL2	15
25	DRVL1	DRVL2	16
23	CS1	CS2	18
24	PGND1	PGND2	17
1	VO1	VO2	8
3	VFB1	VFB2	6
2	COMP1	COMP2	7
29	EN1	EN2	12
30	PGOOD1	PGOOD2	11
20	V5FILT		
22	VIN		
21	VREG5		
19	VREG3		
4	VREF2		
5	GND		
33	THRML_PAD		

P5VS5_VBST — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm

P5VS5_DRVH — GATE_NODE=TRUE

P5VS5_LL — SWITCH_NODE=TRUE

P5VS5_DRVL — GATE_NODE=TRUE

P5VS5_CS

GND_P5VS5_PGND

P5VS5_VO — 5V Fixed

XW7300 SM

GND_P5VP3V3_SGND — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

R7365 3.57K 1% 1/16W MF-LF 402

P3V3S5_VBST_RC — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm

R7364 0 5% 1/16W MF-LF 402

C7364 0.1UF 20% 10V CERM 402

PPBUS_G3H

CRITICAL C7380 22UF 20% 25V POLY CASE-D2-LF

C7381 1UF 10% 25V X5R 603

CRITICAL Q7360 SI7114DN PWRPK-1212-8

PP3V3_S5

Vout = 3.3V
5.5A max output
(L7360 limit)

CRITICAL L7360 4.7UH IHLP

C7390 10UF 20% 6.3V X5R 603

CRITICAL C7392 150UF 20% 6.3V POLY CASE-B2

CRITICAL Q7365 SI7108DNS PWRPK-1212-8

XW7365 SM

XW7360 SM

PLACEMENT_NOTE=Place XW7360 next to C7390.

P3V3S5_VBST

P3V3S5_DRVH — GATE_NODE=TRUE

P3V3S5_LL — SWITCH_NODE=TRUE

P3V3S5_DRVL — GATE_NODE=TRUE

P3V3S5_CS

GND_P3V3S5_PGND

P3V3S5_VO — 3.3V Fixed

MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

TP_P5VS5_EN

RSMRST_PWRGD

RSMRST_PWRGD

TP_P3V3S5_EN

SMC_PM_G2_EN

SMC_PM_G2_EN

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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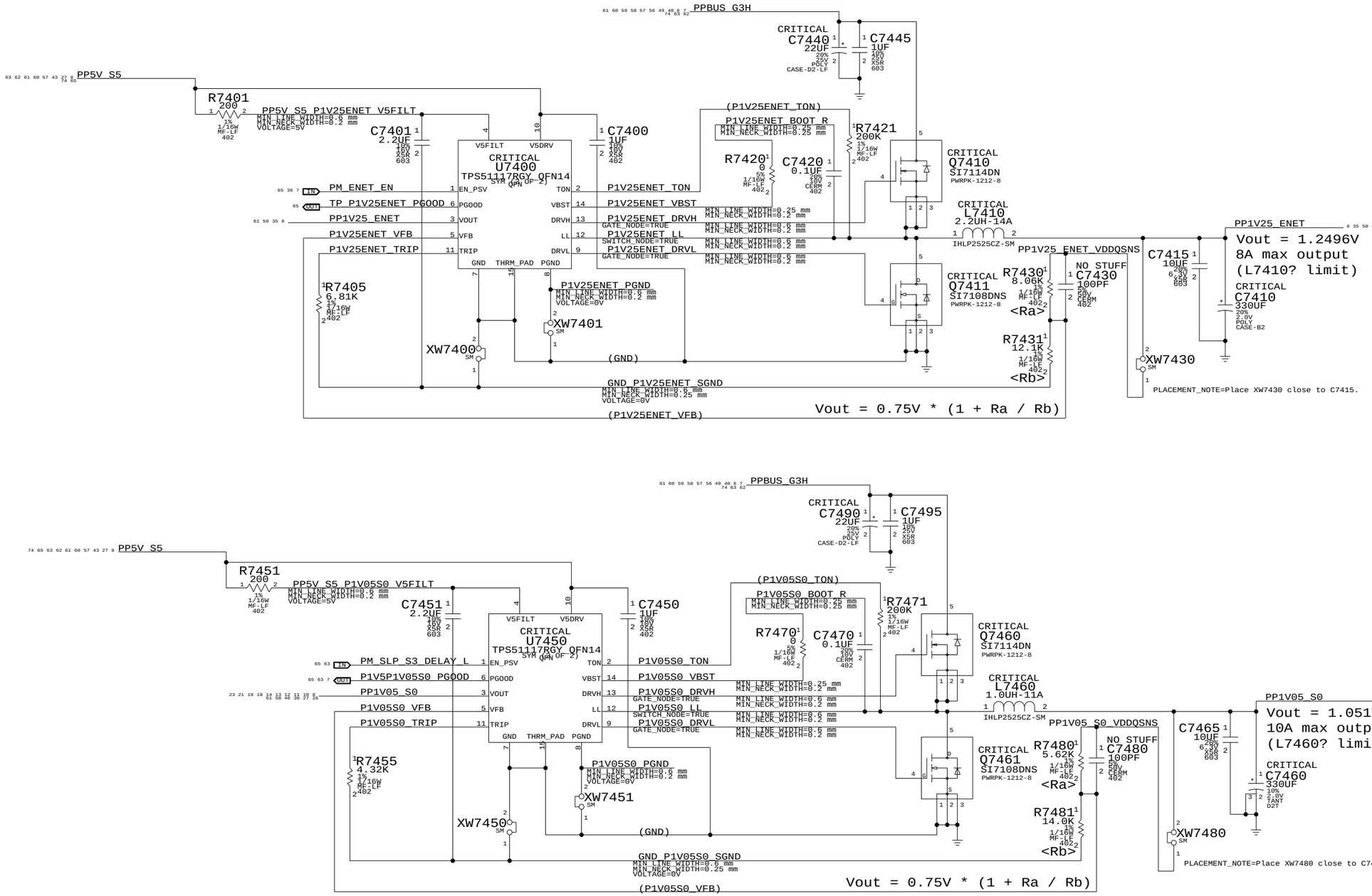
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE SHT 60 OF 88



1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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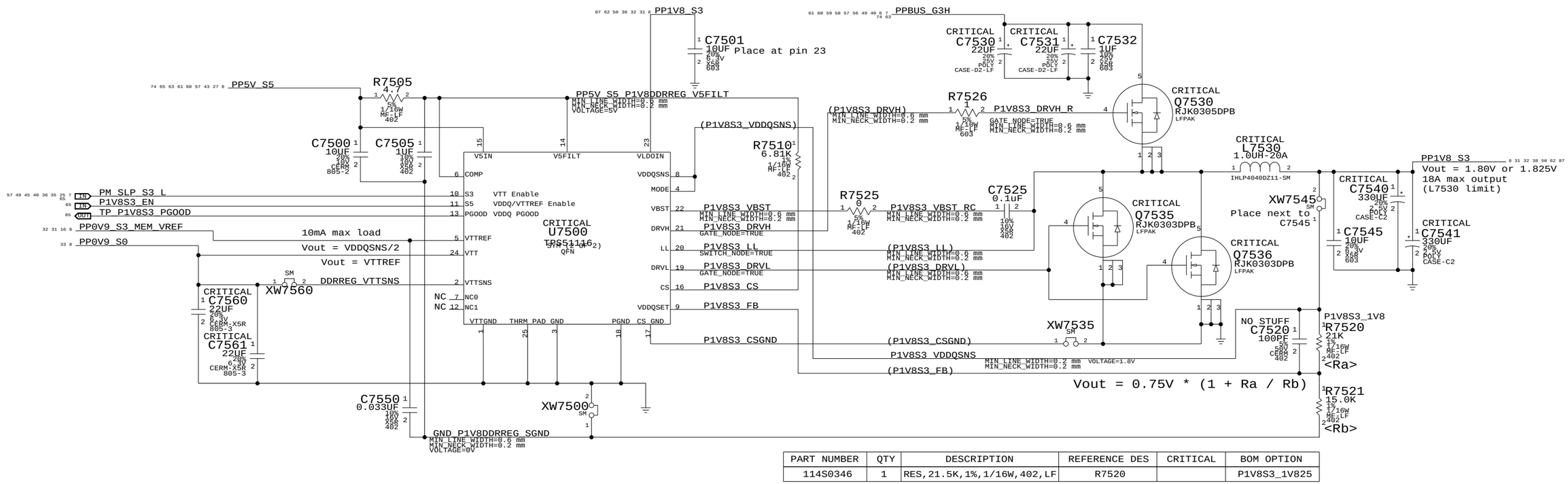
D	051-7225	10.0.0
SCALE: NONE	SHT 61 OF 88	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0346	1	RES,21.5K,1%,1/16W,402,LF	R7520		P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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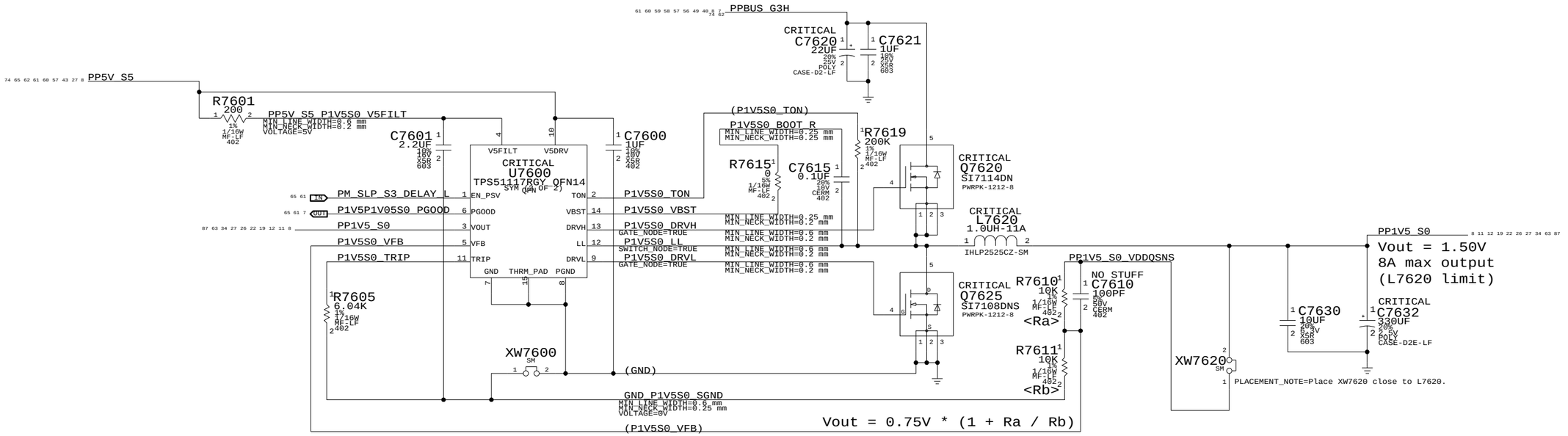
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 62 OF 88	



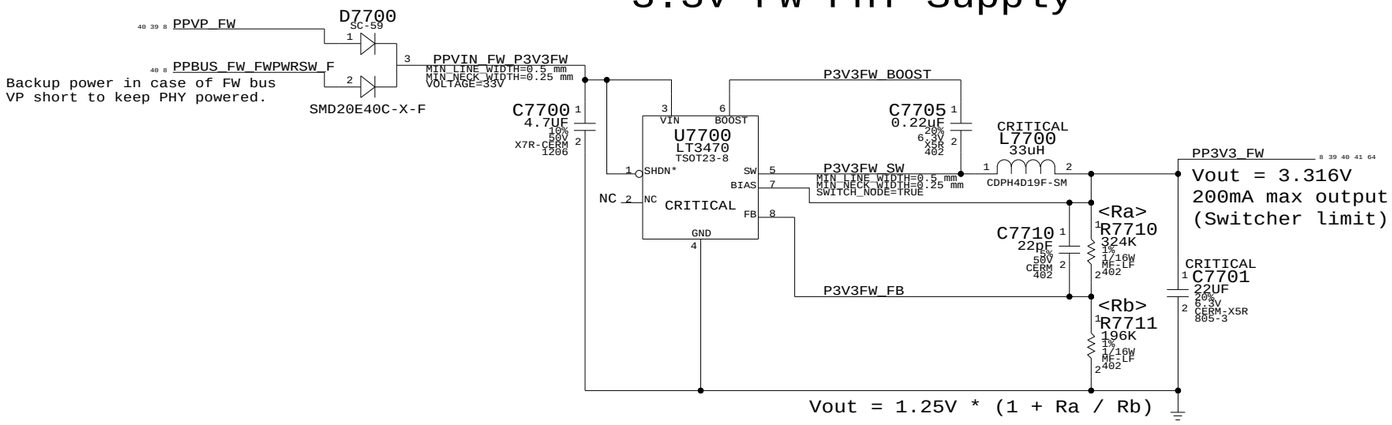
1.5V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

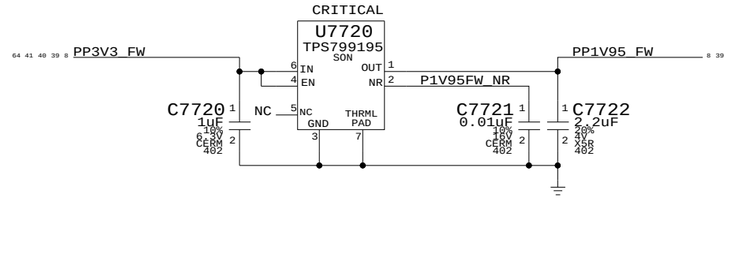
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 63 OF 88	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	64	88

Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PP5V_S5

PP3V3_GPU

R7850 10K 5% 1/16W MF-LF 402

R7851 100K 5% 1/16W MF-LF 402

R7852 100K 5% 1/16W MF-LF 402

R7854 10K 5% 1/16W MF-LF 402

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

PM_GPUP1V8FET_EN

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

PM_GPUP1V8FET_EN — MAKE_BASE=TRUE — PM_GPUP1V8FET_EN

PM_GPUVCORE_EN — MAKE_BASE=TRUE — PM_GPUVCORE_EN

Q7850 2N7002DW-X-F SOT-363

Q7851 2N7002DW-X-F SOT-363

PVCOREGPU_EN_L

Q7851 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V — MAKE_BASE=TRUE — PM_SLP_S3_LS5V

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

R7856 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) — MAKE_BASE=TRUE

PM_SLP_S3_L (x8)

R7853 10K 5% 1/16W MF-LF 402

PP3V3_S0

PP3V3_S5

MC74VHC1G09 SC70 U7850

PM_SLP_S3_DELAY_L — MAKE_BASE=TRUE

R7859 10K 5% 1/16W MF-LF 402

PM_SLP_S3_DELAY_L

NO STUFF C7859 0.047UF 10% 16V CERM 402

EXTGPU_PWR_EN

(EXTGPU_PWR_EN) — MAKE_BASE=TRUE

EXTGPU_PWR_EN (x3)

SB GPIO has ability to force all GPU rails off
R7853 acts as pull-up for open-drain GPIO.

NO STUFF C7853 0.047UF 10% 16V CERM 402

Fast wake glitch filter. Should not be necessary to stuff if GPU supplies and PGOOD revalidate before 99ms SMC timer expires.

PP1V2_GPU needs to ramp first via RC control

PM_ENET_EN

(PM_ENET_EN) — MAKE_BASE=TRUE

PM_ENET_EN (x2)

PM_S4_STATE_L

R7857 10K 5% 1/16W MF-LF 402

(PM_S4_STATE_L) — MAKE_BASE=TRUE

PM_S4_STATE_L (x4)

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN — MAKE_BASE=TRUE — P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

SMC_PM_G2_EN

R7858 10K 5% 1/16W MF-LF 402

(SMC_PM_G2_EN) — MAKE_BASE=TRUE

SMC_PM_G2_EN (x2)

TP_P5VS5_EN — MAKE_BASE=TRUE — TP_P5VS5_EN

TP_P3V3S5_EN — MAKE_BASE=TRUE — TP_P3V3S5_EN

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

P3V42G3H5_BOOST

C7800 10UF 20% 16V X5R 1206-1

U7800 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC FB GND

NC CRITICAL

P3V42G3H_SW — MIN_LINE_WIDTH=0.5 mm — MIN_NECK_WIDTH=0.25 mm — SWITCH_NODE=TRUE

C7805 0.22UF 20% 6.3V X5R 402

CRITICAL L7810 33uH CDPH4D19F-SM

PP3V42_G3H

Vout = 3.425
200mA max output
(Switcher limit)

C7810 22pF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

C7815 22UF 20% 6.3V CERM-X5R 805-3

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

Unused PGOOD Signals

TP_P1V25ENET_PGOOD — MAKE_BASE=TRUE — TP_P1V25ENET_PGOOD

TP_P1V8S3_PGOOD — MAKE_BASE=TRUE — TP_P1V8S3_PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

IMVP6_IMON

To CPU IMVP6

PP3V3_S5

R7865 10K 5% 1/16W MF-LF 402

ISL9504A

R7866 0 5% 1/16W MF-LF 402

P1V5P1V05S0_PGOOD

TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)

P1V5P1V05S0_PGOOD — MAKE_BASE=TRUE

TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

P1V5P1V05S0_PGOOD

PP3V3_S0

C7880 0.1UF 20% 10V CERM 402

MC74VHC1G08 SC70 U7880

PM_ALL_S0_PWRGD

ALL_SYS_PWRGD

NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include GFX rails

PM_ALL_GFX_PGOOD

PP3V3_S0

C7885 0.1UF 20% 10V CERM 402

MC74VHC1G08 SC70 U7885

PP5V_S0

PP3V3_S0

PP1V8_S0

PP1V25_S0

R7873 124K 1% 1/16W MF-LF 402

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

CRITICAL U7870 LTC2900 DFN

V1 V2 V3 V4 VREF VPG PBR* RST* CRT GND THRM_PAD

NC

S0PGOOD_P1V2_DIV

S0PGOOD_VREF

S0PGOOD_VPG

S0PGOOD_PWROK

S0PGOOD_CRT

R7874 100K 1% 1/16W MF-LF 402

R7870 9.53K 1% 1/16W MF-LF 402

R7871 93.1K 1% 1/16W MF-LF 402

C7873 0.1UF 20% 10V CERM 402

C7875 0.047UF 10% 16V CERM 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

3.425V G3Hot Supply & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE — SHT 65 OF 88

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEX 1.2V Current = 2A

PP1V25_GPU
PP1V25_GPU
PP1V25_GPU

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805

OMIT
U8000
NB8P-GS-A1
BGA
(2 OF 8)

C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805

C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

A26	PEX_IOVDD_1	AD23	
A28	PEX_IOVDD_2	AF23	
B32	PEX_IOVDD_3	AF24	
D1	PEX_IOVDD_4	AF25	
D31	PEX_IOVDD_5	AG24	
D32	PEX_IOVDD_6	AG25	
F1			
F6			
G8	PEX_IOVDDQ_1	AC16	
M5	PEX_IOVDDQ_2	AC17	
U6	PEX_IOVDDQ_3	AC21	
V1	PEX_IOVDDQ_4	AC22	
V3	PEX_IOVDDQ_5	AE18	
V4	PEX_IOVDDQ_6	AE21	
V5	PEX_IOVDDQ_7	AE22	
V6	NC	PEX_IOVDDQ_8	AF12
W1	PEX_IOVDDQ_9	AF18	
W3	PEX_IOVDDQ_10	AF21	
W4	PEX_IOVDDQ_11	AF22	
W5			
Y5			
Y6	PEX_PLLAVDD	AF15	
AC26	PEX_PLLDVDD	AE15	
AD26	PEX_PLLGND	AE16	
AE26			
AG12			
AH13			
AH31			
AH32			
AM8			
AM9			

180mA

PP1V2_GPU_PEX_PLLAVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

L8012 10NH-600MA 0603

C8014 0.1UF 20% 10V CERM 402
C8013 4.7UF 20% 6.3V CERM 603
C8012 4.7UF 20% 6.3V CERM 603

20mA

PP1V2_GPU_PEX_PLLDVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

L8015 10NH-600MA 0603

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

OMIT
U8000
NB8P-GS-A1
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AK13	PEX_RX0	
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AK14	PEX_RX0_L	
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AM14	PEX_RX1	
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AM15	PEX_RX1_L	
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AL15	PEX_RX2	
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AL16	PEX_RX2_L	
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AK16	PEX_RX3	
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AK17	PEX_RX3_L	
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AL17	PEX_RX4	
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AL18	PEX_RX4_L	
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AM18	PEX_RX5	
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AM19	PEX_RX5_L	
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AK19	PEX_RX6	
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AK20	PEX_RX6_L	
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AL20	PEX_RX7	
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AL21	PEX_RX7_L	
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AM21	PEX_RX8	
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AM22	PEX_RX8_L	
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AK22	PEX_RX9	
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AK23	PEX_RX9_L	
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AL23	PEX_RX10	
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AL24	PEX_RX10_L	
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AM24	PEX_RX11	
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AM25	PEX_RX11_L	
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AK25	PEX_RX12	
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AK26	PEX_RX12_L	
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AL26	PEX_RX13	
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AL27	PEX_RX13_L	
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AM27	PEX_RX14	
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AM28	PEX_RX14_L	
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AL28	PEX_RX15	
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AL29	PEX_RX15_L	
PEG_CLK100M_GPU_P			AH14	PEX_REFCLK	
PEG_CLK100M_GPU_N			AJ14	PEX_REFCLK_L	
GPU_RESET_L			AH15	PEX_RST_L	

PEX_TX0	AJ15	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>	
PEX_TX0_L	AK15	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>	
PEX_TX1	AH16	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>	
PEX_TX1_L	AG16	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>	
PEX_TX2	AG17	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>	
PEX_TX2_L	AH17	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>	
PEX_TX3	AG18	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>	
PEX_TX3_L	AH18	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>	
PEX_TX4	AK18	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>	
PEX_TX4_L	AJ18	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4>	
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PEX_TX5_L	AH19	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5>	
PEX_TX6	AG20	PEG_D2R_C_P<6>	C8067 0.1uF	PEG_D2R_P<6>	
PEX_TX6_L	AH20	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6>	
PEX_TX7	AG21	PEG_D2R_C_P<7>	C8069 0.1uF	PEG_D2R_P<7>	
PEX_TX7_L	AH21	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7>	
PEX_TX8	AK21	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8>	
PEX_TX8_L	AJ21	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8>	
PEX_TX9	AJ22	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9>	
PEX_TX9_L	AH22	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9>	
PEX_TX10	AG23	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10>	
PEX_TX10_L	AH23	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10>	
PEX_TX11	AK24	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11>	
PEX_TX11_L	AJ24	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11>	
PEX_TX12	AJ25	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12>	
PEX_TX12_L	AH25	PEG_D2R_C_N<12>	C8080 0.1uF	PEG_D2R_N<12>	
PEX_TX13	AH26	PEG_D2R_C_P<13>	C8081 0.1uF	PEG_D2R_P<13>	
PEX_TX13_L	AG26	PEG_D2R_C_N<13>	C8082 0.1uF	PEG_D2R_N<13>	
PEX_TX14	AK27	PEG_D2R_C_P<14>	C8083 0.1uF	PEG_D2R_P<14>	
PEX_TX14_L	AJ27	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14>	
PEX_TX15	AJ28	PEG_D2R_C_P<15>	C8085 0.1uF	PEG_D2R_P<15>	
PEX_TX15_L	AH27	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>	
PEX_TSTCLK_OUT	AM12	TP_GPU_PEXTSTCLK_P			
PEX_TSTCLK_OUT_L	AM11	TP_GPU_PEXTSTCLK_N			

All 0.1uF: 10% 16V X5R 402

NV G84M PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 66 OF 88	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 20% 10V 6.3V CERM 402
C8101 1UF 20% 10V 6.3V CERM 402
C8102 1UF 20% 10V 6.3V CERM 402
C8103 0.1UF 20% 10V CERM 402
C8104 0.1UF 20% 10V CERM 402
C8105 0.1UF 20% 10V CERM 402
C8106 0.1UF 20% 10V CERM 402
C8107 0.1UF 20% 10V CERM 402
C8108 0.1UF 20% 10V CERM 402
C8109 0.1UF 20% 10V CERM 402
C8110 0.1UF 20% 10V CERM 402
C8111 0.1UF 20% 10V CERM 402
C8112 0.1UF 20% 10V CERM 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB8P-GS-A1
BGA
(7 OF 8)

K16 K17 N13 N14 N16 N17 N19 P13 P14 P16 P17 P19 R16 R17 T13 T14 T15 T18 T19 U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 Y17 Y19 Y20 — VDD
P20 T20 T23 U20 U23 W20 — VDD_LP

A12 A18 A21 A24 A27 A3 A30 A6 A9 AA32 AD32 AG32 AK32 C32 F32 J32 M32 R32 — FBVDD
AA25 AA26 AB25 AB26 G11 G12 G15 G18 G21 G22 H11 H12 H15 H18 H21 H22 L25 L26 M25 M26 R25 R26 V25 V26 — FBVDDQ
AA23 AB23 H16 H17 J10 J23 J24 J9 K11 K12 K21 K22 K24 K9 L23 M23 T25 U25 — NC
FBVTT

TP_GPU_VDD_SENSE N20 — VDD_SENSE
TP_GPU_GND_SENSE M21 — GND_SENSE

77 73 70 69 68 57 8 PP1V8_GPU

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U8000
NB8P-GS-A1
BGA
(8 OF 8)

AE17 AE27 AE6 AF11 AF26 AF29 AF4 AF7 AG10 AG11 AB27 AB6 AC10 AC23 AC29 AC4 AD16 AD17 AD2 AD31 AA12 AA2 AA21 AA31 AG13 AG14 AG15 AG19 AG2 AG22 AG31 AG8 AH24 AJ10 AJ13 AJ16 AJ17 AJ20 AJ23 AJ26 AJ29 AJ4 AJ7 AK2 AK28 AK31 AL10 AL11 AL14 AL19 AL22 AL25 AL3 AL6 AL9 AM10 AM13 AM16 AM17 AM20 AM23 AM26 AM29 B12 B15 B18 B21 B24 B27 B3 B30 B6 B9 C2 C31 D10 D13 — GND
D16 D17 D20 D23 D26 D29 D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K10 K23 K29 K4 L27 L6 M12 M2 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 — GND

NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE

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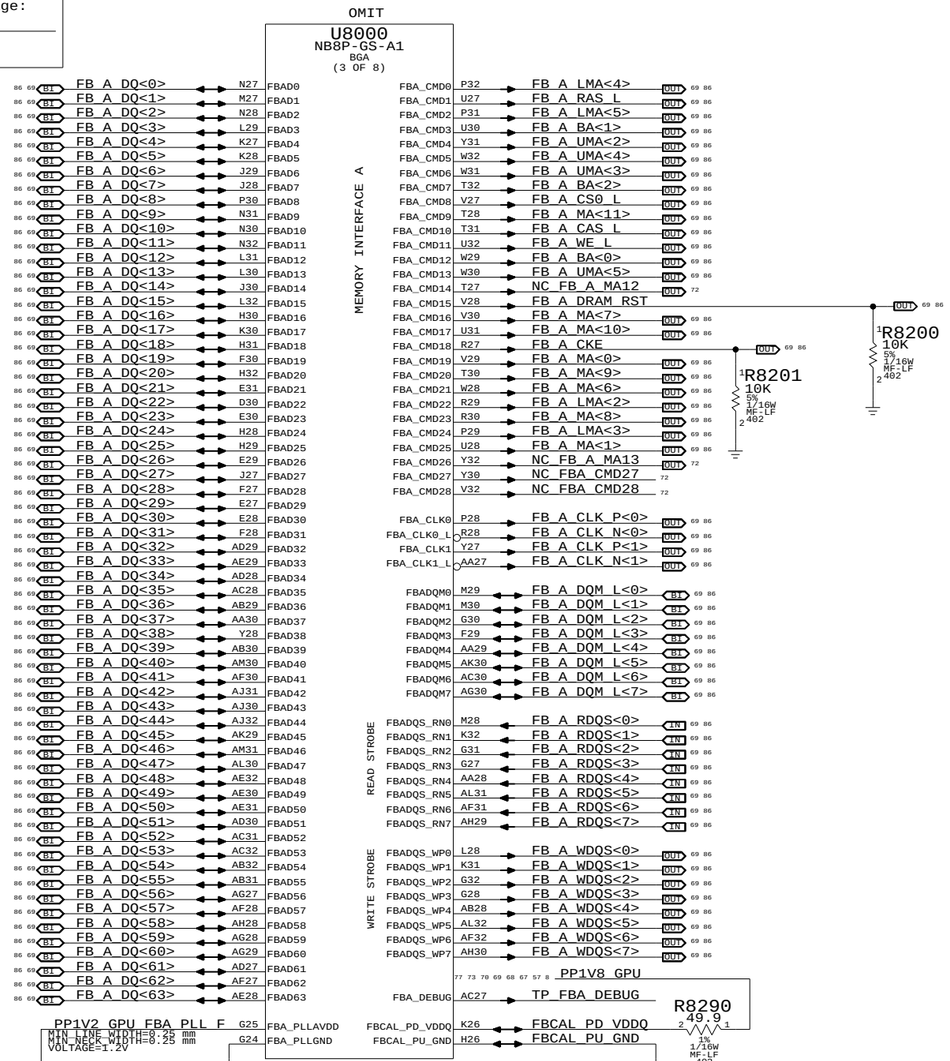
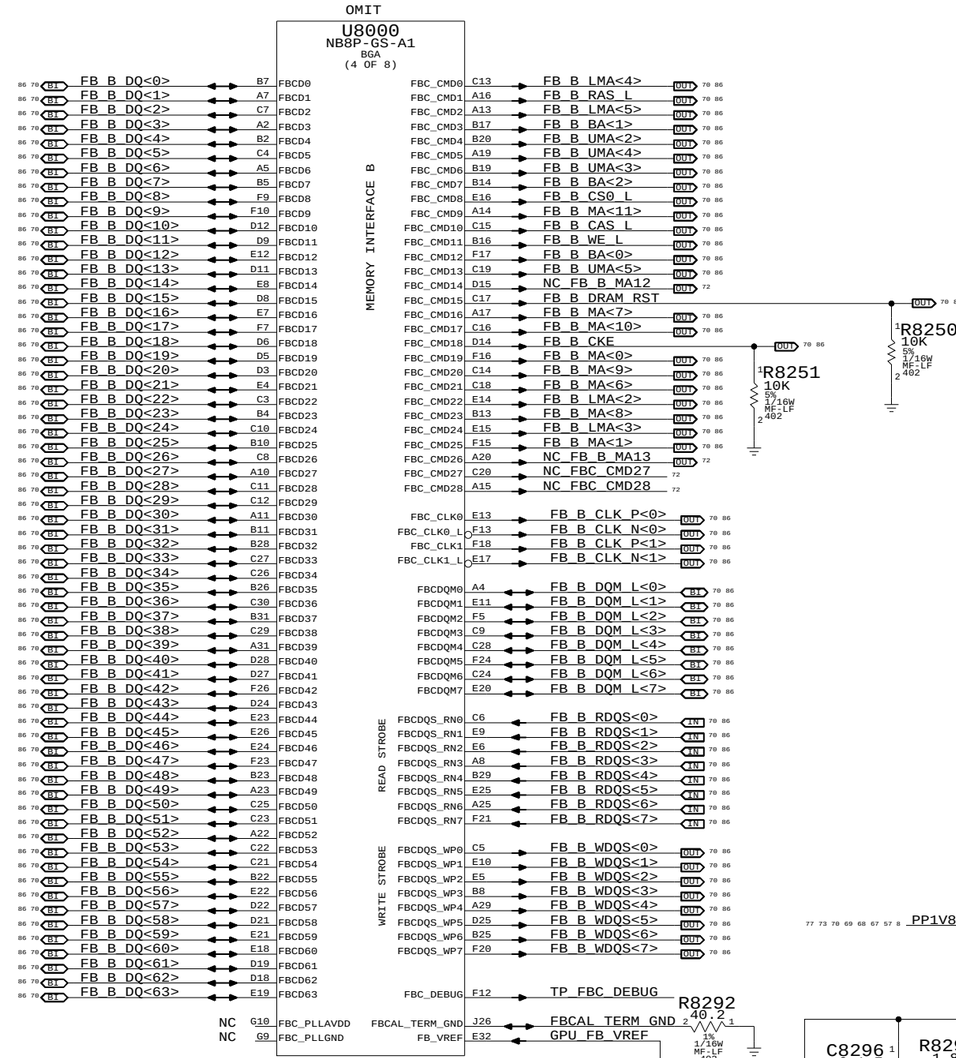
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	68	88

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V8_GPU

CRITICAL
OMIT

U8400
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8400 22UF 20% 6.3V CERM-X5R 805
C8401 C8402 C8403 C8404 0.1UF 10% 16V X5R 402
C8410 C8415 0.1UF 10% 16V X5R 402

Connect to designated pin, then GND

U8400.J1
U8400.J12

C8420 22UF 20% 6.3V CERM-X5R 805
C8421 C8422 C8423 C8424 C8425 C8426 0.1UF 10% 16V X5R 402

R8430 2.37K 1% 1/16W MF-LF 402
R8431 5.49K 1% 1/16W MF-LF 402
R8432 4.32K 1% 1/16W MF-LF 402

FB_A0_VREF
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

C8431 C8433 0.1UF 10% 16V X5R 402

FB_A0_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

FB_A_CLK0_TERM

R8440 1K 1% 1/16W MF-LF 402
R8442 121 1% 1/16W MF-LF 402
R8444 121 1% 1/16W MF-LF 402
R8446 60.4 1% 1/16W MF-LF 402
R8443 121 1% 1/16W MF-LF 402
R8445 121 1% 1/16W MF-LF 402
R8447 60.4 1% 1/16W MF-LF 402

C8446 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8400
2N7002DW-X-F
SOT-363

CRITICAL
OMIT

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FB_A_MA<2>
FB_A_MA<3>
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FB_A_MA<5>
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FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L

FB_A0_ZQ
FB_A0_MF
FB_A0_SEN

FB_A_DRAM_RST

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FB_A_RDQS<3>

FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>

FB_A_BA<0>
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FB_A_BA<2>

R8448 243 1% 1/16W MF-LF 402
R8449 100 5% 1/16W MF-LF 402

NC
NC

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FB_A_DQM_L<3>

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PP1V8_GPU

CRITICAL
OMIT

U8450
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8450 22UF 20% 6.3V CERM-X5R 805
C8451 C8452 C8453 C8454 0.1UF 10% 16V X5R 402
C8460 C8465 0.1UF 10% 16V X5R 402

Connect to designated pin, then GND

U8400.J1
U8400.J12

C8470 22UF 20% 6.3V CERM-X5R 805
C8471 C8472 C8473 C8474 C8475 C8476 0.1UF 10% 16V X5R 402

R8480 2.37K 1% 1/16W MF-LF 402
R8481 5.49K 1% 1/16W MF-LF 402
R8482 4.32K 1% 1/16W MF-LF 402

FB_A1_VREF
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

C8481 C8483 0.1UF 10% 16V X5R 402

FB_A1_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

FB_A_CLK1_TERM

R8490 1K 1% 1/16W MF-LF 402
R8492 121 1% 1/16W MF-LF 402
R8494 121 1% 1/16W MF-LF 402
R8496 60.4 1% 1/16W MF-LF 402
R8493 121 1% 1/16W MF-LF 402
R8495 121 1% 1/16W MF-LF 402
R8497 60.4 1% 1/16W MF-LF 402

C8496 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8400
2N7002DW-X-F
SOT-363

CRITICAL
OMIT

FB_A_MA<0>
FB_A_MA<1>
FB_A_UMA<2>
FB_A_UMA<3>
FB_A_UMA<4>
FB_A_UMA<5>
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FB_A_CKE
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L

FB_A1_ZQ
FB_A1_MF
FB_A1_SEN

FB_A_DRAM_RST

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FB_A_RDQS<4>

FB_A_WDQS<7>
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FB_A_BA<0>
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FB_A_BA<2>

R8498 243 1% 1/16W MF-LF 402
R8499 100 5% 1/16W MF-LF 402

NC
NC

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FB_A_DQ<33>
FB_A_DQ<35>
FB_A_DQ<32>
FB_A_DQ<36>
FB_A_DQ<37>
FB_A_DQ<39>
FB_A_DQ<38>

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

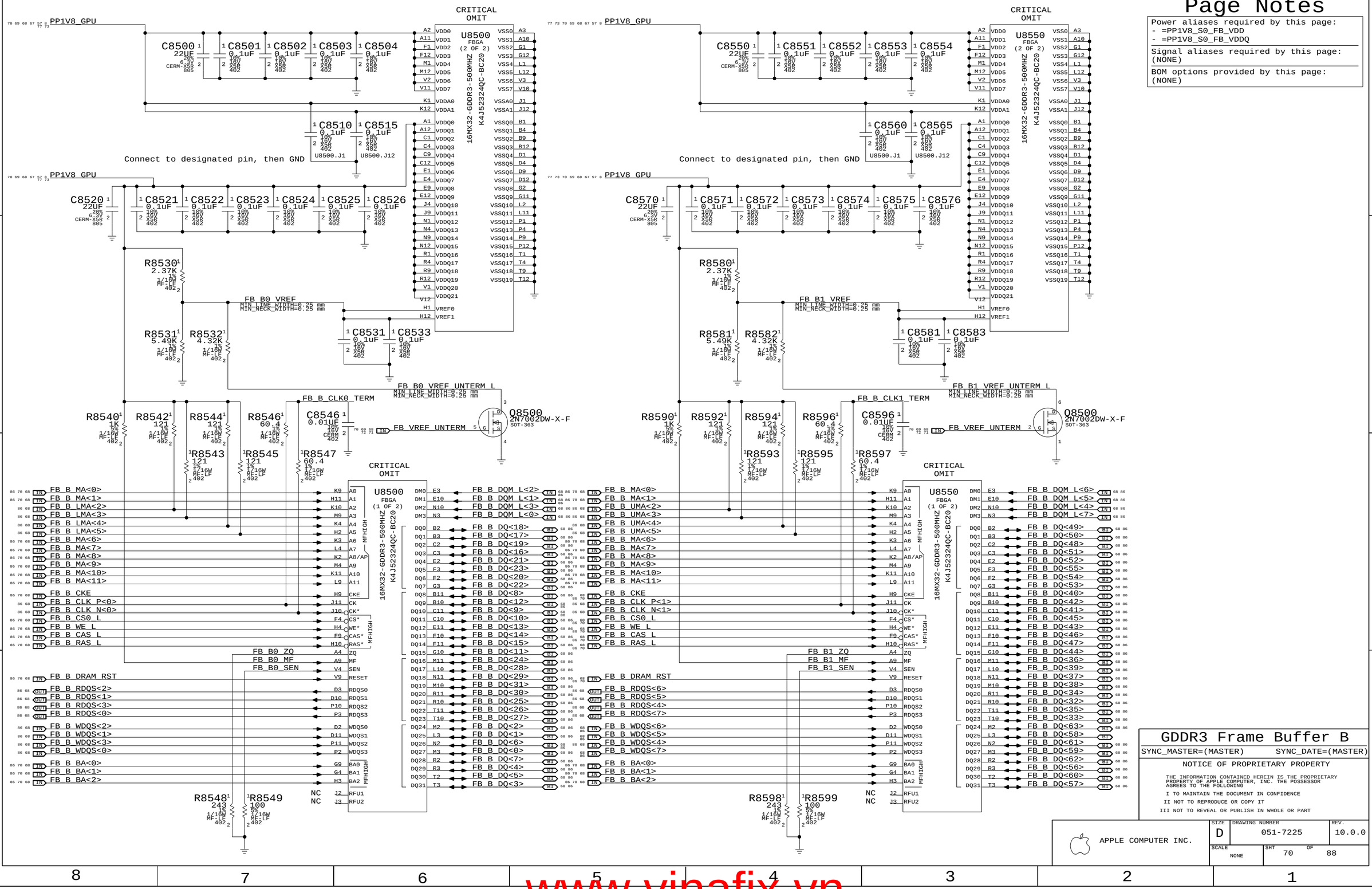
SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 69 OF 88	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

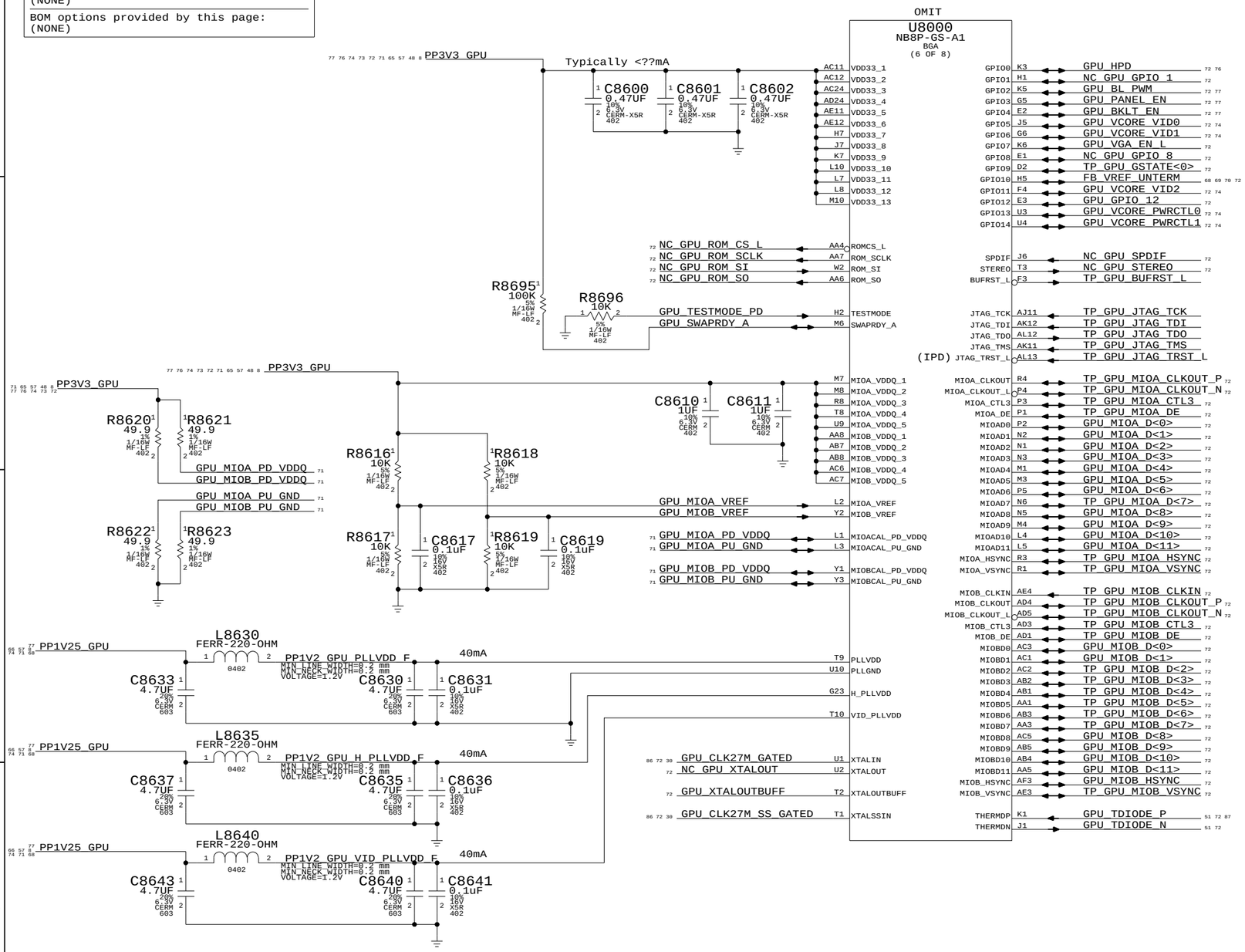
SCALE	SHT	OF
NONE	70	88

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M GPIO/MIO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	71	88

GPIOs

	Native Func		
GPU_HPD	HPD0	GPU_HPD	IN
NC_GPU_GPIO_1	HPD1	NC_GPU_GPIO_1	
GPU_BL_PWM	LCD0_BL_PWM	GPU_BL_PWM	OUT
GPU_PANEL_EN	LCD0_VDD	GPU_PANEL_EN	OUT
GPU_BKLT_EN	LCD0_BL_EN	GPU_BKLT_EN	OUT
GPU_VCORE_VID0	VID0	GPU_VCORE_VID0	OUT
GPU_VCORE_VID1	VID1	GPU_VCORE_VID1	OUT
GPU_VGA_EN_L	MEM_VID	GPU_VGA_EN_L	
NC_GPU_GPIO_8	THERM	NC_GPU_GPIO_8	
TP_GPU_GSTATE<0>	FAN_PWM	TP_GPU_GSTATE<0>	
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM	OUT
GPU_VCORE_VID2	SLI_SYNC	GPU_VCORE_VID2	OUT
GPU_GPIO_12	AC_DET	TP_GPU_GSTATE<1>	
GPU_VCORE_PWRCTL0	PWR_CTL0	GPU_VCORE_PWRCTL0	OUT
GPU_VCORE_PWRCTL1	PWR_CTL1	GPU_VCORE_PWRCTL1	OUT

Config Straps

PP3V3_GPU

VRAM_SAMSUNG		VRAM_128	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
R8720	R8722	R8724	R8726	R8728	R8729	R8730	R8731	R8732
10K	10K	10K	10K	1K	1K	1K	1K	1K

Supported straps:	
RAMCFG0	GPU_MIOB_D<0>
RAMCFG1	GPU_MIOB_D<1>
RAMCFG2	GPU_MIOB_D<8>
RAMCFG3	GPU_MIOB_D<9>
3GIO_PADCFG0	GPU_MIOA_D<6>
3GIO_PADCFG1	GPU_MIOA_D<8>
3GIO_PADCFG2	GPU_MIOA_D<9>
3GIO_PADCFG3	GPU_MIOB_HSYNC
PEX_PLL_EN_TERM	GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)	GPU_MIOA_D<1>

VRAM_HYNIX	NO STUFF	VRAM_256		
R8721	R8723	R8725	R8727	R8733
10K	10K	10K	10K	1K

Straps not supported:	
CRYSTAL	MIOB_D<2>
TVMODE<2..0>	MIOB_D<6,10,7>
PCI_DEVID<4..0>	MIOB_CTL3, MIOB_D<11,3,5,4>
USER<3..0>	MIOA_D<5..2>
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE

Renamed signals

GPU_CLK27M_GATED	GPU_CLK27M_GATED
GPU_CLK27M_SS_GATED	GPU_CLK27M_SS_GATED
GPU_TDIODE_P	GPU_TDIODE_P
GPU_TDIODE_N	GPU_TDIODE_N
GPU_DVI_DDC_CLK	GPU_DVI_DDC_CLK
GPU_DVI_DDC_DATA	GPU_DVI_DDC_DATA
GPU_PANEL_DDC_CLK	GPU_PANEL_DDC_CLK
GPU_PANEL_DDC_DATA	GPU_PANEL_DDC_DATA

Unused I2C Buses

NC_GPU_I2CA_SCL	NC_GPU_I2CA_SCL
NC_GPU_I2CA_SDA	NC_GPU_I2CA_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

Unused signals

NC_GPU_XTALOUT	NC_GPU_XTALOUT
NC_GPU_SPDIF	NC_GPU_SPDIF
NC_GPU_STEREO	NC_GPU_STEREO
NC_FB_A_MA12	NC_FB_A_MA12
NC_FB_B_MA12	NC_FB_B_MA12
NC_FB_A_MA13	NC_FB_A_MA13
NC_FB_B_MA13	NC_FB_B_MA13
NC_FBA_CMD27	NC_FBA_CMD27
NC_FBC_CMD27	NC_FBC_CMD27
NC_FBA_CMD28	NC_FBA_CMD28
NC_FBC_CMD28	NC_FBC_CMD28
NC_GPU_ROM_CS_L	NC_GPU_ROM_CS_L
NC_GPU_ROM_SCLK	NC_GPU_ROM_SCLK
NC_GPU_ROM_SI	NC_GPU_ROM_SI
NC_GPU_ROM_SO	NC_GPU_ROM_SO
NC_GPU_CSYNC	NC_GPU_CSYNC
NC_GPU_R2	NC_GPU_R2
NC_GPU_G2	NC_GPU_G2
NC_GPU_B2	NC_GPU_B2
NC_GPU_H2SYNC	NC_GPU_H2SYNC
NC_GPU_V2SYNC	NC_GPU_V2SYNC
NC_LVDS_U_DATAP<3>	NC_LVDS_U_DATAP<3>
NC_LVDS_U_DATAN<3>	NC_LVDS_U_DATAN<3>
NC_LVDS_L_DATAP<3>	NC_LVDS_L_DATAP<3>
NC_LVDS_L_DATAN<3>	NC_LVDS_L_DATAN<3>
TP_GPU_MIOA_CLKOUT_P	TP_GPU_MIOA_CLKOUT_P
TP_GPU_MIOA_CLKOUT_N	TP_GPU_MIOA_CLKOUT_N
TP_GPU_MIOA_CTL3	TP_GPU_MIOA_CTL3
TP_GPU_MIOA_DE	TP_GPU_MIOA_DE
TP_GPU_MIOA_D<5..2>	GPU_MIOA_D<5..2>
TP_GPU_MIOA_D<7>	TP_GPU_MIOA_D<7>
TP_GPU_MIOA_D<11..10>	GPU_MIOA_D<11..10>
TP_GPU_MIOA_HSYNC	TP_GPU_MIOA_HSYNC
TP_GPU_MIOA_VSYNC	TP_GPU_MIOA_VSYNC
TP_GPU_MIOB_CLKIN	TP_GPU_MIOB_CLKIN
TP_GPU_MIOB_CLKOUT_P	TP_GPU_MIOB_CLKOUT_P
TP_GPU_MIOB_CLKOUT_N	TP_GPU_MIOB_CLKOUT_N
TP_GPU_MIOB_CTL3	TP_GPU_MIOB_CTL3
TP_GPU_MIOB_DE	TP_GPU_MIOB_DE
TP_GPU_MIOB_D<7..2>	GPU_MIOB_D<7..2>
TP_GPU_MIOB_D<11..10>	GPU_MIOB_D<11..10>
TP_GPU_MIOB_VSYNC	TP_GPU_MIOB_VSYNC
NC_GPU_IFPD_CLK_P	NC_GPU_IFPD_CLK_P
NC_GPU_IFPD_CLK_N	NC_GPU_IFPD_CLK_N

HDCP Support

PP3V3_GPU

HDCP C8770 0.1UF

HDCP R8770 10K

HDCP CRITICAL

U8770 AT88SC080C SO1

GPU_I2CH_SCL

GPU_I2CH_SDA

HDCP R8771 10K

NC

Analog Video Mux

PP3V3_GPU

C8700 0.1UF

CRITICAL U8700 QFN TS3V330 OMIT

GPU_VGA_R

GPU_VGA_G

GPU_VGA_B

Place Rs near GPU

R8740 150 | R8741 150 | R8742 150

GPU_TV_C_VGA_R

GPU_TV_Y_VGA_G

GPU_TV_COMP_VGA_B

NC

GPU_VGA_EN_L

R8700 10K

GPU_TV_C

GPU_TV_Y

GPU_TV_COMP

Place Rs near GPU

R8743 150 | R8744 150 | R8745 150

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1718	1	IC,TS3V340,QUAD VIDEO SW,QFN16	U8700	CRITICAL	

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1579	353S1718		ALL (U8700)	TS3V330 alt to TS3V340

TMDS Backdrive Protection

CRITICAL Q8790 SI2305DS SOT-23

PP3V3_GPU

PP3V3_GPU_TMDS

R8790 10K

GPU_TMDS_PWREN_L

Q8925 2N7002DW-X-F SOT-363

PM_GPUVCORE_EN

R8791 100K

Unused Clocks

GPU_CLK27M_SS_GATED

GPU_XTALOUTBUFF

R8780 10K | R8781 10K

GPU_SS_INT

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	72	88

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

69 68 67 57 5 77 70 8 PP1V8_GPU

L8800 FERR-220-OHM 0402
L8805 FERR-220-OHM 0402
L8810 FERR-220-OHM 0402
L8815 FERR-220-OHM 0402

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AF9
Place at AF8

20mA peak per diff pair
160mA peak for all pairs

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

40mA peak

76 72 8 PP3V3_GPU_TMDS

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AD6
Place at AE7

20mA peak per diff pair
200mA peak for all pairs

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

40mA peak

Sum of peak currents: 390mA

77 76 74 72 71 65 57 48 8 PP3V3_GPU

L8820 FERR-220-OHM 0402
L8830 FERR-220-OHM 0402
NO STUFF
L8840 FERR-220-OHM 0402

C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402
C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402
C8845 4.7UF 20% 6.3V CERM 603
NO STUFF C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402

120mA peak
150mA peak
120mA peak

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

OMIT
U8000 NB8P-GS-A1 BGA (5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC AK9	LVDS_L_CLK_P
AF8	IFPB_IOVDD	IFPA_TXC_L AJ9	LVDS_L_CLK_N
		IFPA_TXD0 AH6	LVDS_L_DATA_P<0>
		IFPA_TXD0_L AJ6	LVDS_L_DATA_N<0>
		IFPA_TXD1 AH8	LVDS_L_DATA_P<1>
		IFPA_TXD1_L AH7	LVDS_L_DATA_N<1>
		IFPA_TXD2 AJ8	LVDS_L_DATA_P<2>
		IFPA_TXD2_L AK8	LVDS_L_DATA_N<2>
		IFPA_TXD3 AJ5	NC_LVDS_L_DATAP<3>
		IFPA_TXD3_L AH5	NC_LVDS_L_DATAN<3>
AC9	IFPAB_PLLVDD		
AD9	IFPAB_PLLGND		
73 GPU_IFPAB_VPROBE	AM4 IFPAB_VPROBE		
73 GPU_IFPAB_RSET	AL5 IFPAB_RSET		
		IFPB_TXC AK4	LVDS_U_CLK_P
		IFPB_TXC_L AL4	LVDS_U_CLK_N
		IFPB_TXD4 AM6	LVDS_U_DATA_P<0>
		IFPB_TXD4_L AM5	LVDS_U_DATA_N<0>
		IFPB_TXD5 AM7	LVDS_U_DATA_P<1>
		IFPB_TXD5_L AL7	LVDS_U_DATA_N<1>
		IFPB_TXD6 AK6	LVDS_U_DATA_P<2>
		IFPB_TXD6_L AK5	LVDS_U_DATA_N<2>
		IFPB_TXD7 AK7	NC_LVDS_U_DATAP<3>
		IFPB_TXD7_L AL8	NC_LVDS_U_DATAN<3>
AD6	IFPC_IOVDD	IFPC_TXC AM2	TMDS_CLK_P
AE7	IFPD_IOVDD	IFPC_TXC_L AM3	TMDS_CLK_N
		IFPC_TXD0 AE2	TMDS_DATA_P<0>
		IFPC_TXD0_L AE1	TMDS_DATA_N<0>
		IFPC_TXD1 AF1	TMDS_DATA_P<1>
		IFPC_TXD1_L AF2	TMDS_DATA_N<1>
		IFPC_TXD2 AG1	TMDS_DATA_P<2>
		IFPC_TXD2_L AH1	TMDS_DATA_N<2>
		IFPD_TXC AG3	NC_GPU_IFPD_CLK_P
		IFPD_TXC_L AH2	NC_GPU_IFPD_CLK_N
		IFPD_TXD4 AK1	TMDS_DATA_P<3>
		IFPD_TXD4_L AJ1	TMDS_DATA_N<3>
		IFPD_TXD5 AL2	TMDS_DATA_P<4>
		IFPD_TXD5_L AL1	TMDS_DATA_N<4>
		IFPD_TXD6 AJ2	TMDS_DATA_P<5>
		IFPD_TXD6_L AJ3	TMDS_DATA_N<5>
AA10	IFPCD_PLLVDD		
AB10	IFPCD_PLLGND		
73 GPU_IFPCD_VPROBE	AK3 IFPCD_VPROBE		
73 GPU_IFPCD_RSET	AH3 IFPCD_RSET		
AD10	DACA_VDD	DACA_RED AH11	GPU_VGA_R
AG9	DACA_IDUMP	DACA_GREEN AJ12	GPU_VGA_G
73 GPU_DACA_VREF	AH10 DACA_VREF	DACA_BLUE AH12	GPU_VGA_B
73 GPU_DACA_RSET	AH9 DACA_RSET	DACA_HSYNC AF10	GPU_VGA_HSYNC
		DACA_VSYNC AK10	GPU_VGA_VSYNC
V8	DACB_VDD	DACB_RED R6	GPU_TV_C
V7	DACB_IDUMP	DACB_GREEN T5	GPU_TV_Y
73 GPU_DACB_VREF	R5 DACB_VREF	DACB_BLUE T6	GPU_TV_COMP
73 GPU_DACB_RSET	R7 DACB_RSET	DACB_CSYNC U5	NC_GPU_CSYNC
AD7	DACC_VDD	DACC_RED AF6	NC_GPU_R2
AG4	DACC_IDUMP	DACC_GREEN AG6	NC_GPU_G2
73 GPU_DACC_VREF	AH4 DACC_VREF	DACC_BLUE AE5	NC_GPU_B2
73 GPU_DACC_RSET	AF5 DACC_RSET	DACC_HSYNC AG7	NC_GPU_H2SYNC
		DACC_VSYNC AG5	NC_GPU_V2SYNC
77 72 B1 GPU_PANEL_DDC_CLK	G2 I2CC_SCL		
77 72 B1 GPU_PANEL_DDC_DATA	G1 I2CC_SDA		
72 B1 GPU_I2CH_SCL	G3 I2CH_SCL	I2CA_SCL K2	NC_GPU_I2CA_SCL B1 72
72 B1 GPU_I2CH_SDA	H3 I2CH_SDA	I2CA_SDA J3	NC_GPU_I2CA_SDA B1 72
84 51 48 45 B1 SMBUS_SMC_0_S0_SCL	C1 I2CS_SCL	I2CB_SCL H4	GPU_DVI_DDC_CLK B1 72 76
84 51 48 45 B1 SMBUS_SMC_0_S0_SDA	B1 I2CS_SDA	I2CB_SDA J4	GPU_DVI_DDC_DATA B1 72 76

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

GPU_IFPAB_RSET 73
GPU_IFPCD_RSET 73
GPU_DACA_RSET 73
GPU_DACB_RSET 73
GPU_DACC_RSET 73

NO STUFF R8850 1K 1% 1/16W ME-LF 402
NO STUFF R8851 1K 1% 1/16W ME-LF 402
R8852 124 1% 1/16W ME-LF 402
R8853 124 1% 1/16W ME-LF 402
R8854 124 1% 1/16W ME-LF 402

GPU_DACA_VREF 73
GPU_DACB_VREF 73
GPU_DACC_VREF 73

C8852 0.1UF 20% 10V CERM 402
C8853 0.1UF 20% 10V CERM 402
C8854 0.1UF 20% 10V CERM 402

GPU_IFPAB_VPROBE 73
GPU_IFPCD_VPROBE 73

NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 73 OF 88	

GPU VCore Regulator

GPU VCore Current Sense

PP5V_S5
PP5V_S5_GPUVCORE_V5FILT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
R8901 200 1% 1/16W MF-LF 402
C8901 2.2UF 10% 16V X5R 603
C8900 1UF 10% 16V X5R 603
U8900 CRITICAL
TPS51117RGY_QFN14
SYM 1 OF 2
V5FILT V5DRV EN_PSV PGOOD VOUT VFB TRIP TON VBST DRVH LL DRVL GND THRM_PAD PGND
PM_GPUVCORE_EN
PM_GPUP1V8FET_EN
(=PPVCORE_GPU_REG)
GPUVCORE_VFB
GPUVCORE_TRIP
GPUVCORE_TON
GPUVCORE_VBST
GPUVCORE_DRVH
GPUVCORE_LL
GPUVCORE_DRVL
R8905 10.5K 1% 1/16W MF-LF 402
XW8900 SM
(GND)
(GPUVCORE_TON)
GPUVCORE_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R8915 0 5% 1/16W MF-LF 402
C8915 0.1UF 20% 16V CERM 402
R8919 200K 1% 1/16W MF-LF 402
PPBUS_G3H
C8931 CRITICAL 22UF 20% 25V POLY CASE-D2-LF
C8930 CRITICAL 22UF 20% 25V POLY CASE-D2-LF
C8932 1UF 10% 25V X5R 603
Q8920 CRITICAL RJK0305DPB LFPAK
Q8922 CRITICAL RJK0301DPB LFPAK
Q8921 CRITICAL RJK0301DPB LFPAK
NO STUFF C8921 1000PF 10% 25V X7R 402
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
SWITCH_NODE=TRUE
Vout = 0.75V * (1 + Ra / Reg)
Vout(min) = 0.75V * (1 + Ra / Rb)
Reg = Rb || Rc || Rd || Re
GND_GPUVCORE_SGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=0V
(GPUVCORE_VFB)
(=PPVCORE_GPU_REG)
GPUVCORE_VFB_PC1
GPUVCORE_VFB_PC0
PP3V3_S0
R8996 1K 1% 1/16W MF-LF 402
GPUISENS_NTC
CRITICAL R8997 10KOHM-5% 0603-LF
NO STUFF R8994 1K 1% 1/16W MF-LF 402
C8990 0.47UF 10% 6.3V CERM-X5R 402
R8993 20.0K 1% 1/16W MF-LF 402
GPUISENS_NEG
C8991 0.22UF 10% 6.3V CERM-X5R 402
PVCORE_GPU_NTC
GPUISENS_RC
R8991 20.0K 1% 1/16W MF-LF 402
GPUISENS_POS
R8990 649 1% 1/16W MF-LF 402
CRITICAL L8920 1.0UH-20A IHLP4040DZ11-SM
XW8901 SM
PLACEMENT_NOTE=Place R8997 close to L8920
PLACEMENT_NOTE=Place R8994 close to L8920
PLACEMENT_NOTE=Place C8990 close to L8920
PLACEMENT_NOTE=Place C8991 close to L8920
PLACEMENT_NOTE=Place R8990 close to L8920
C8998 470PF 10% 50V CERM 402
R8998 1M 1% 1/16W MF-LF 402
C8995 1UF 10% 6.3V CERM 402
U8995 HPA00141AIDCKR SC70-5 CRITICAL
GPUVCORE_IOUT
R8992 1M 1% 1/16W MF-LF 402
C8992 470PF 10% 50V CERM 402
PPVCORE_GPU
Vout = 1.25V - 0.96V
18A max output
(L8920 limit)
Place near C8940 2
XW8920 SM
PPVCORE_GPU_XW
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.20 mm
VOLTAGE=1.25V
C8942 CRITICAL 330UF 10% 2.0V TANT D2T
C8940 10UF 20% 6.3V X5R 603
C8943 CRITICAL 330UF 10% 2.0V TANT D2T
<Ra> R8921 2.87K 1% 1/16W MF-LF 402
NO STUFF C8920 100PF 5% 50V CERM 402
<Rb> R8922 10K 1% 1/16W MF-LF 402
<Rc> R8923 22.6K 1% 1/16W MF-LF 402
<Rd> R8924 22.6K 1% 1/16W MF-LF 402
<Re> R8925 22.6K 1% 1/16W MF-LF 402
R8926 53.6K 1% 1/16W MF-LF 402
R8927 53.6K 1% 1/16W MF-LF 402
(GPUVCORE_VFB)

PP1V25_GPU
GPU_VCORE_PWRCTL0
R8960 4.99K 1% 1/16W MF-LF 402
C8961 0.01UF 10% 16V CERM 402
R8962 1K 5% 1/16W MF-LF 402
R8961 1K 5% 1/16W MF-LF 402
R8963 1.5K 5% 1/16W MF-LF 402
PC0_DIV
PC0_BIAS
R8964 10K 5% 1/16W MF-LF 402
PC0_BIAS_B
Q8927 MMDT3904XF SOT-363-LF
GND_GPUVCORE_SGND
R8967 1.5K 5% 1/16W MF-LF 402
GPU_VCORE_PWRCTL1
R8965 4.99K 1% 1/16W MF-LF 402
C8966 0.01UF 10% 16V CERM 402
R8966 1K 5% 1/16W MF-LF 402
R8968 1K 5% 1/16W MF-LF 402
PC1_DIV
PC1_BIAS
R8969 10K 5% 1/16W MF-LF 402
PC1_BIAS_B
Q8927 MMDT3904XF SOT-363-LF
GND_GPUVCORE_SGND

PP3V3_GPU
R8970 100K 5% 1/16W MF-LF 402
R8971 100K 5% 1/16W MF-LF 402
R8972 100K 5% 1/16W MF-LF 402
GPU_VCORE_VID0
R8973 7.5K 5% 1/16W MF-LF 402
GPU_VCORE_VID0_RC
C8973 0.1UF 20% 10V CERM 402
GPU_VCORE_VID1
R8974 7.5K 5% 1/16W MF-LF 402
GPU_VCORE_VID1_RC
C8974 0.1UF 20% 10V CERM 402
GPU_VCORE_VID2
R8975 7.5K 5% 1/16W MF-LF 402
GPU_VCORE_VID2_RC
C8975 0.1UF 20% 10V CERM 402
GPUVCORE_VFB_C
GPUVCORE_VFB_D
GPUVCORE_VFB_E
Q8923 2N7002DW-X-F SOT-363
Q8925 2N7002DW-X-F SOT-363

GPU VCore Setpoints

VID2	VID1	VID0	C D E	Vout
0	0	0	- - -	0.965 (rsvd state)
0	0	1	Y - -	1.060 (max batt)
0	1	1	Y Y -	1.156 (balanced)
1	1	1	Y Y Y	1.251 (max perf)

All other states not defined

GPU (G84M) Core Supply

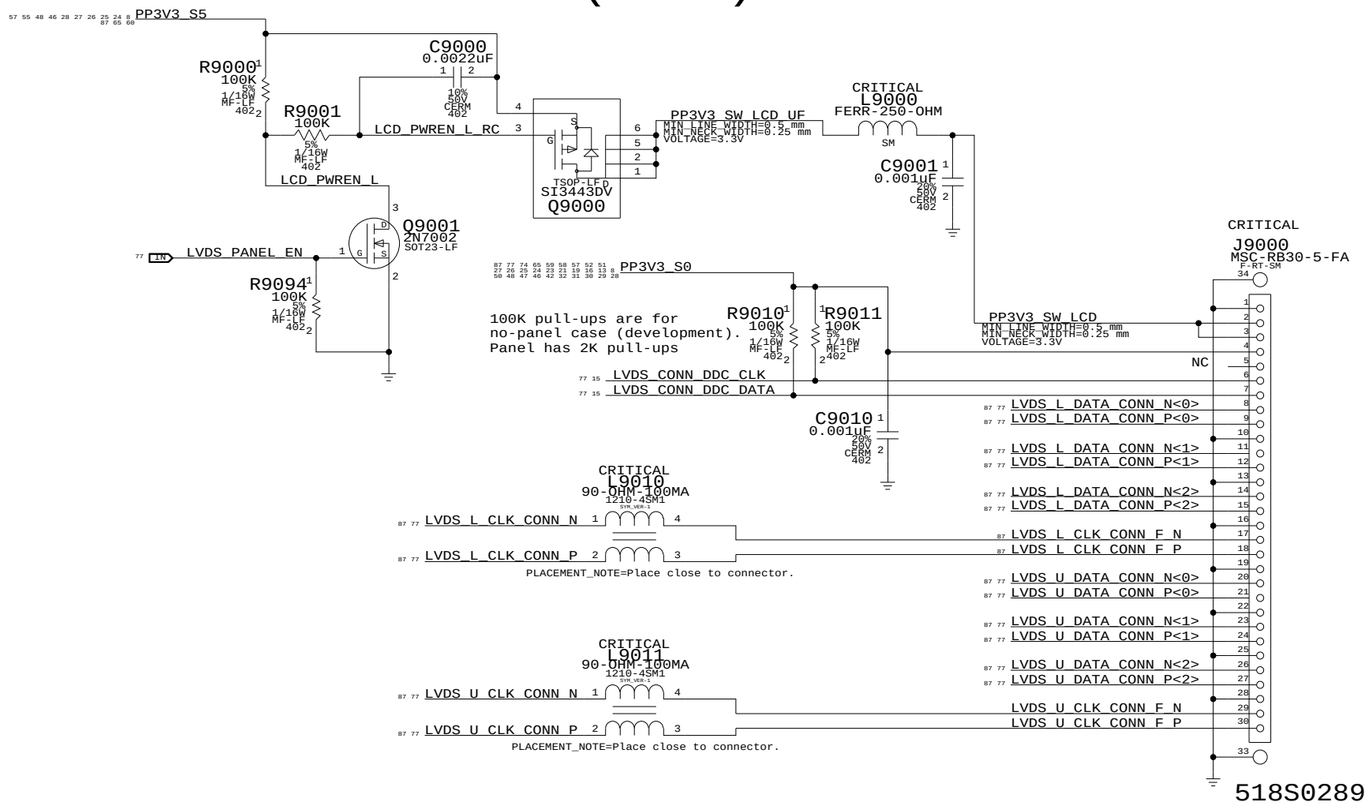
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE SHT 74 OF 88

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE: NONE SHT 75 OF 88

TMDS Filtering

(Place close to GPU) (Place close to connector)

TMDS_DATA_N<0> → NO STUFF R9462 49.9 1% 1/16W MF-LF 402 → CRITICAL L9460 90-OHM-100MA 1210-4SM1 → TMDS_DATA_F_N<0>
TMDS_DATA_P<0> → NO STUFF R9463 49.9 1% 1/16W MF-LF 402 → CRITICAL L9460 → TMDS_DATA_F_P<0>
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9462 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

TMDS_DATA_N<1> → NO STUFF R9466 49.9 1% 1/16W MF-LF 402 → CRITICAL L9464 90-OHM-100MA 1210-4SM1 → TMDS_DATA_F_N<1>
TMDS_DATA_P<1> → NO STUFF R9467 49.9 1% 1/16W MF-LF 402 → CRITICAL L9464 → TMDS_DATA_F_P<1>
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9466 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

TMDS_DATA_N<2> → NO STUFF R9470 49.9 1% 1/16W MF-LF 402 → CRITICAL L9468 90-OHM-100MA 1210-4SM1 → TMDS_DATA_F_N<2>
TMDS_DATA_P<2> → NO STUFF R9471 49.9 1% 1/16W MF-LF 402 → CRITICAL L9468 → TMDS_DATA_F_P<2>
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9470 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

TMDS_CLK_N → R9472 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_N → CRITICAL L9472 370-OHM SM → TMDS_CLK_F_N
TMDS_CLK_P → R9473 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_P → CRITICAL L9472 → TMDS_CLK_F_P
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9474 0.01UF 10% 16V CERM 402
NO STUFF R9475 49.9 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

TMDS_DATA_N<3> → NO STUFF R9478 49.9 1% 1/16W MF-LF 402 → CRITICAL L9476 90-OHM-100MA 1210-4SM1 → TMDS_DATA_F_N<3>
TMDS_DATA_P<3> → NO STUFF R9479 49.9 1% 1/16W MF-LF 402 → CRITICAL L9476 → TMDS_DATA_F_P<3>
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9478 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

TMDS_DATA_N<4> → NO STUFF R9482 49.9 1% 1/16W MF-LF 402 → CRITICAL L9480 90-OHM-100MA 1210-4SM1 → TMDS_DATA_F_N<4>
TMDS_DATA_P<4> → NO STUFF R9483 49.9 1% 1/16W MF-LF 402 → CRITICAL L9480 → TMDS_DATA_F_P<4>
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9482 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

TMDS_DATA_N<5> → NO STUFF R9486 49.9 1% 1/16W MF-LF 402 → CRITICAL L9484 90-OHM-100MA 1210-4SM1 → TMDS_DATA_F_N<5>
TMDS_DATA_P<5> → NO STUFF R9487 49.9 1% 1/16W MF-LF 402 → CRITICAL L9484 → TMDS_DATA_F_P<5>
PLACEMENT_NOTE=Place close to connector.
NO STUFF C9486 0.01UF 10% 16V CERM 402
SIGNAL_MODEL=EMPTY PP3V3_GPU_TMDS

VGA SYNC Buffers

PP3V3_GPU → C9450 0.1UF 10% 16V CERM 402 → U9450 MC74VHC1G08 SC70
GPU_VGA_VSYNC → U9450 → VGA_VSYNC_R → R9450 33 5% 1/16W MF-LF 402 → VGA_VSYNC
PLACEMENT_NOTE=Place close to connector.

PP3V3_GPU → C9451 0.1UF 10% 16V CERM 402 → U9451 MC74VHC1G08 SC70
GPU_VGA_HSYNC → U9451 → VGA_HSYNC_R → R9451 33 5% 1/16W MF-LF 402 → VGA_HSYNC
PLACEMENT_NOTE=Place close to connector.

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_TV_COMP_VGA_B → VGA_TERM_FILTER R9440 150 1% 1/16W MF-LF 402 → CRITICAL FL9440 210MHZ MEA2010P-SM → C9440 3.3PF 0.25PF 50V CERM 402 → VGA_B (DACB TV COMP)
GPU_TV_Y_VGA_G → VGA_TERM_FILTER R9441 150 1% 1/16W MF-LF 402 → FL9440 → C9441 3.3PF 0.25PF 50V CERM 402 → VGA_G (DACB TV Y)
GPU_TV_C_VGA_R → VGA_TERM_FILTER R9442 150 1% 1/16W MF-LF 402 → FL9440 → C9442 3.3PF 0.25PF 50V CERM 402 → VGA_R (DACB TV C)

DVI INTERFACE

DVI DDC Current Limit
(55mA requirement per DVI spec)

PP5V_S0 → CRITICAL F9410 0.5AMP-13.2V SM-LF → PP5V_S0_DDC_F → CRITICAL L9410 400-OHM-EMI SM-1 → PP5V_S0_DDC
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

Isolation required for DVI->ADC Adapter
PP5V_S0_DDC → D9410 SOD-123 B0530WXF → PP5V_S0_DDC_PULLUPS
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V

GND_CHASSIS_DVI_BOT → CRITICAL J9400 QH11121-RIG02-4F F-RT-TH-DVI

TMDS_DATA_F_N<0> 17 → TMDS_DATA_F_N<2> 1
TMDS_DATA_F_N<1> 9
TMDS_DATA_F_P<0> 18 → TMDS_DATA_F_P<2> 2
TMDS_DATA_F_P<1> 10
19 3
11
TMDS_DATA_F_N<5> 20 → TMDS_DATA_F_N<4> 4
TMDS_DATA_F_N<3> 12
TMDS_DATA_F_P<5> 21 → TMDS_DATA_F_P<4> 5
TMDS_DATA_F_P<3> 13
DVI_DDC_CLK_R 22 → 6
(PP5V_S0_DDC) 14
TMDS_CLK_F_P 23 → DVI_DDC_DATA_R 7
15
TMDS_CLK_F_N 24 → VGA_VSYNC 8
DVI_HPD_R 16
VGA_B C3 → C1 VGA_R
VGA_HSYNC C5B → C5A
C4 → C2 VGA_G
34 32
514-0278

VGA_TERM_CONN R9445 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9443 150 1% 1/16W MF-LF 402
VGA_TERM_CONN R9444 150 1% 1/16W MF-LF 402
C9410 0.01UF 50V CERM 603

OMIT CX9490 SHORT NONE NONE 402
OMIT CX9491 SHORT NONE NONE 402
OMIT CX9492 SHORT NONE NONE 402
OMIT CX9493 SHORT NONE NONE 402
GND_CHASSIS_DVI_TOP
OMIT CX9400 SHORT NONE NONE 402
OMIT CX9401 SHORT NONE NONE 402
OMIT CX9402 SHORT NONE NONE 402
OMIT CX9403 SHORT NONE NONE 402
GND_CHASSIS_DVI_BOT

GPU Isolation / Level-Shift

PP3V3_GPU → R9410 4.7K 5% 1/16W MF-LF 402 → DVI_DDC_CLK
PP3V3_GPU → R9412 4.7K 5% 1/16W MF-LF 402 → DVI_DDC_DATA
PP3V3_GPU → R9411 100 5% 1/16W MF-LF 402 → DVI_DDC_CLK
PP3V3_GPU → R9413 100 5% 1/16W MF-LF 402 → DVI_DDC_DATA
PP3V3_GPU → R9414 100 5% 1/16W MF-LF 402 → DVI_HPD
C9411 100PF 5% 50V CERM 402
C9413 100PF 5% 50V CERM 402
C9414 100PF 5% 50V CERM 402

Q9411 2N7002DW-X-F SOT-363: DVI_DDC_CLK → GPU_DVI_DDC_CLK (OUT)
Q9411 2N7002DW-X-F SOT-363: DVI_DDC_DATA → GPU_DVI_DDC_DATA (OUT)
GPU_HPD_BILAT
GPU_IOENABLE_RC (IN)
Q9414 2N7002DW-X-F SOT-363: DVI_HPD → GPU_HPD (OUT)
Q9415 2N7002DW-X-F SOT-363: PP5V_S0 → DVI_HOTPLUG_DET (OUT)

PP3V3_GPU → R9420 10K 5% 1/16W MF-LF 402 → GPU_DVI_DDC_CLK
R9421 10K 5% 1/16W MF-LF 402 → GPU_DVI_DDC_DATA
R9422 270K 5% 1/16W MF-LF 402 → GPU_HPD
R9423 270K 5% 1/16W MF-LF 402 → DVI_HOTPLUG_DET
R9415 20K 5% 1/16W MF-LF 402 → DVI_HOTPLUG_DET

DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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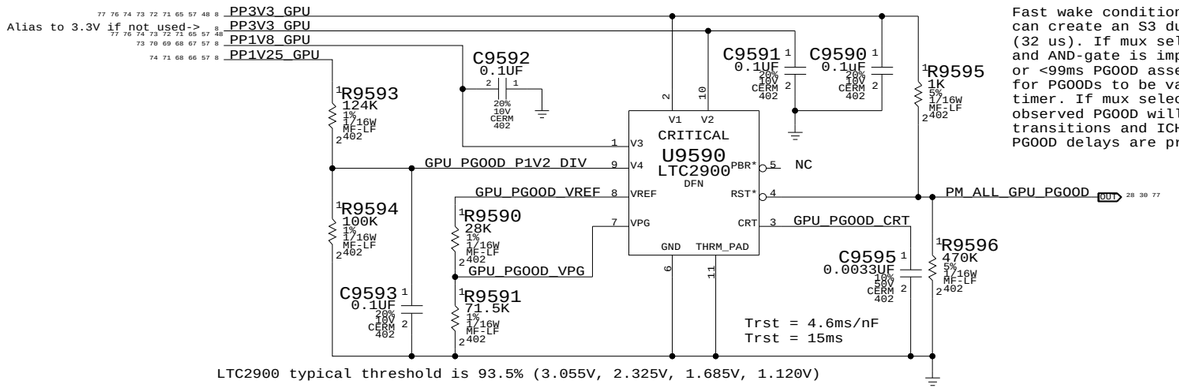
D	051-7225	10.0.0
SCALE: NONE	SHT 76 OF 88	

PGOOD Monitor for GPU Rails

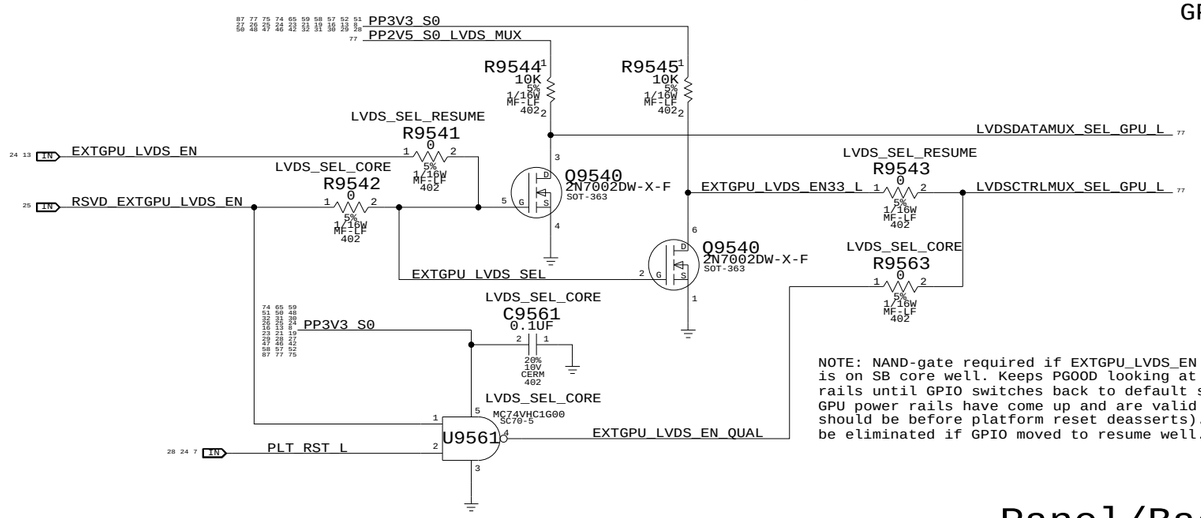
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

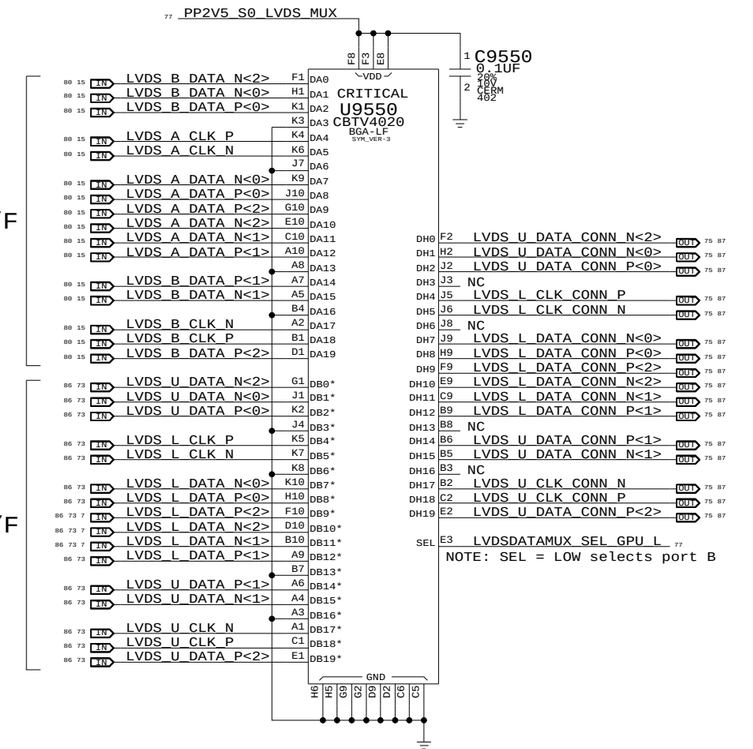
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

Mux Select Conditioning



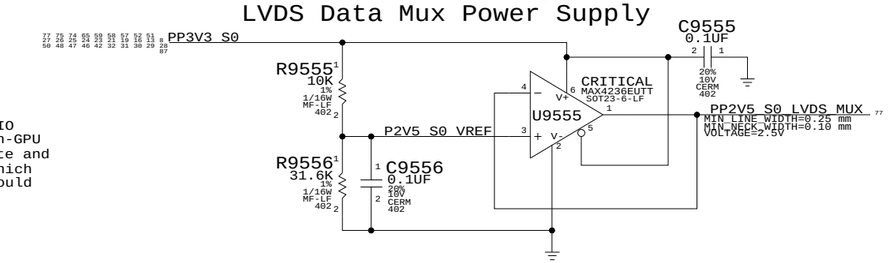
NOTE: NAND-gate required if EXTGPU_LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

LVDS I/F Mux

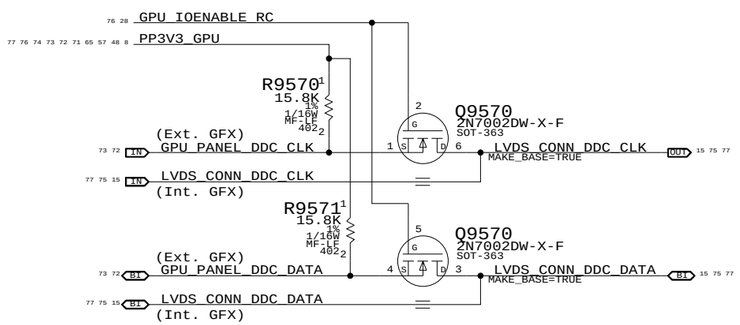


NOTE: SEL = LOW selects port B

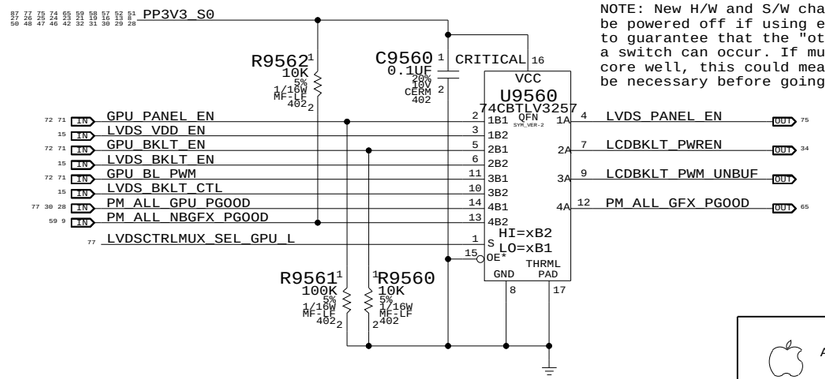
LVDS Data Mux Power Supply



GPU DDC Pass FETs



Panel/Backlight Control Mux



NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

LVDS Interface Mux

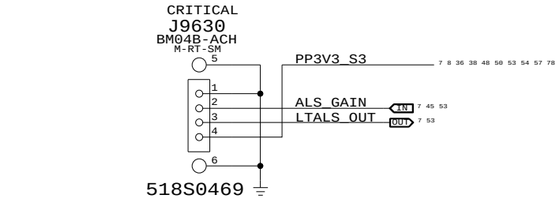
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

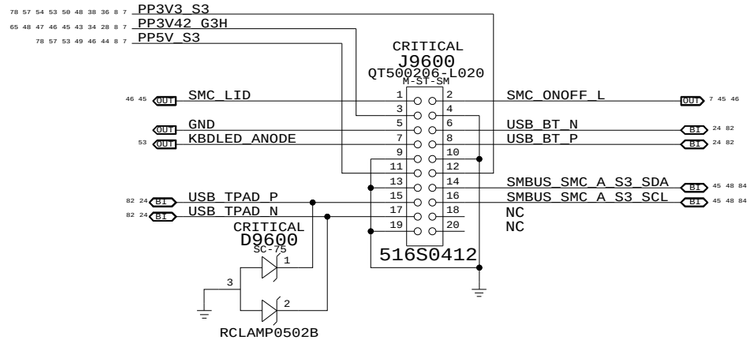
SCALE: NONE SHT 77 OF 88

Left ALS Connector

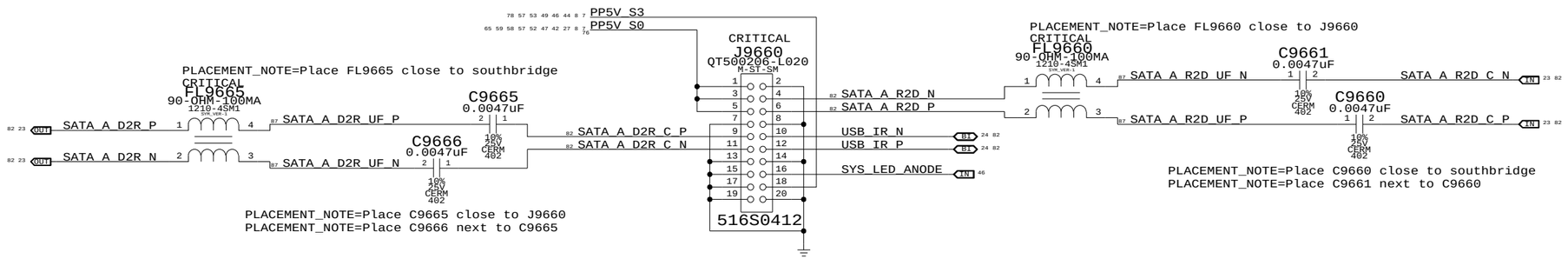


White colored version of 518S0369

Top-Case Connector



SATA HDD & IR & SIL Flex Connector



NOTE: SATA _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M75 Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
SCALE: NONE	SHT 78 OF 88	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 58
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 84
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 84
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

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D	051-7225	10.0.0

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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	66
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	66
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 66
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 66
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 66
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 66
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	66
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	66
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0
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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 78
	SATA_100D	SATA	SATA_A_R2D_C_N	23 78
	SATA_100D	SATA	SATA_A_R2D_P	78
	SATA_100D	SATA	SATA_A_R2D_N	78
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	23 78
	SATA_100D	SATA	SATA_A_D2R_N	23 78
	SATA_100D	SATA	SATA_A_D2R_C_P	78
	SATA_100D	SATA	SATA_A_D2R_C_N	78
SATA_B_R2D	SATA_100D	SATA	TP_SATA_B_R2DP	23 42
	SATA_100D	SATA	TP_SATA_B_R2DN	23 42
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	TP_SATA_B_D2RP	23 42
	SATA_100D	SATA	TP_SATA_B_D2RN	23 42
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	TP_SATA_C_R2DP	23 42
	SATA_100D	SATA	TP_SATA_C_R2DN	23 42
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	TP_SATA_C_D2RP	23 42
	SATA_100D	SATA	TP_SATA_C_D2RN	23 42
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 34
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 34
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 34
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 43
	USB_90D	USB	USB_EXTA_N	24 43
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_WWAN_P	7 24 44
	USB_90D	USB	USB_WWAN_N	7 24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 44
	USB_90D	USB	USB_CAMERA_N	7 24 44
USB_BT	USB_90D	USB	USB_BT_P	24 78
	USB_90D	USB	USB_BT_N	24 78
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 78
	USB_90D	USB	USB_TPAD_N	24 78
USB_IR	USB_90D	USB	USB_IR_P	24 78
	USB_90D	USB	USB_IR_N	24 78
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	TP_USB_EXTCP	9 24
	USB_90D	USB	TP_USB_EXTCN	9 24
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL	25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA	25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL	25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA	25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 55
	SPI_55S	SPI	SPI_SCLK	55
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 55
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	55
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 55
	SPI_55S	SPI	SPI_A_SO_R	55
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_I0	SPI_55S	SPI	SPI_CE_R_L<0>	24 55
	SPI_55S	SPI	SPI_CE_L<0>	55
SPI_CE_I1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE NONE SHT 82 OF 88

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	10.0.0

SCALE	SHT	OF
NONE	83	88

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 29 30 84
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 29 30 84
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 84
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 84
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 79 84
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 79 84
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	TP_CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	TP_CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M_SS	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 16 22 29 30 84
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 16 22 29 30 84
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 66 84
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 66 84
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 84
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 84
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 84
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 84
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 84
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 84
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 84
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 84
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 84
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 84
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 84
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 84
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 29 30 84
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 29 30 84
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 84
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 84
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 79 84
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 79 84
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 16 22 29 30 84
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 16 22 29 30 84
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 66 84
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 66 84
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 84
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 84
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 84
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 84
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 84
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 84
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 84
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 84
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 84
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 84
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 84
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 84

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	45 48 78
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	45 48 78
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	34 45 48 51
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	34 45 48 51
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	45 48 51 73
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	45 48 51 73
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 45 48 56
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 45 48 56
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	45 48 54
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	45 48 54

Clock & SMC Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

APPLE COMPUTER INC.

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 41
Port 2 Not Used				

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0> 68 69
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0> 68 69
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1> 68 69
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1> 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<1..0> 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_MA<11..6> 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_BA<2..0> 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_RAS_L 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CAS_L 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_WE_L 68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CKE 68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_A_CS0_L 68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_A_DRAM_RST 68 69
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_LMA<5..2> 68 69
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_UMA<5..2> 68 69
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<0> 68 69
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<1> 68 69
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<2> 68 69
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<3> 68 69
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<0> 68 69
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<1> 68 69
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<2> 68 69
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<3> 68 69
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<7..0> 68 69
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<15..8> 68 69
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<23..16> 68 69
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<31..24> 68 69
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<0> 68 69
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<1> 68 69
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<2> 68 69
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<3> 68 69
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<4> 68 69
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<5> 68 69
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<6> 68 69
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<7> 68 69
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<4> 68 69
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<5> 68 69
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<6> 68 69
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<7> 68 69
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<39..32> 68 69
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<47..40> 68 69
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<55..48> 68 69
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<63..56> 68 69
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<4> 68 69
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<5> 68 69
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<6> 68 69
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<7> 68 69

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0> 68 70
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0> 68 70
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1> 68 70
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1> 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<1..0> 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_MA<11..6> 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_BA<2..0> 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_RAS_L 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CAS_L 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_WE_L 68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CKE 68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB_B_CS0_L 68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB_B_DRAM_RST 68 70
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_LMA<5..2> 68 70
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_UMA<5..2> 68 70
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<0> 68 70
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<1> 68 70
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2> 68 70
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<3> 68 70
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<0> 68 70
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<1> 68 70
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<2> 68 70
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<3> 68 70
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0> 68 70
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<15..8> 68 70
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<23..16> 68 70
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<31..24> 68 70
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<0> 68 70
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<1> 68 70
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<2> 68 70
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<3> 68 70
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<4> 68 70
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<5> 68 70
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<6> 68 70
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<7> 68 70
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<4> 68 70
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<5> 68 70
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<6> 68 70
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<7> 68 70
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<39..32> 68 70
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<47..40> 68 70
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<55..48> 68 70
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<63..56> 68 70
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<4> 68 70
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<5> 68 70
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<6> 68 70
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<7> 68 70

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED 30 71 72
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS 30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED 30 71 72
	LVDS_100D	LVDS	LVDS_L_CLK_P 73 77
	LVDS_100D	LVDS	LVDS_L_CLK_N 73 77
	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0> 7 73 77
	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0> 7 73 77
	LVDS_100D	LVDS	LVDS_U_CLK_P 73 77
	LVDS_100D	LVDS	LVDS_U_CLK_N 73 77
	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0> 73 77
	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0> 73 77
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P 73 76
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N 73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0> 73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0> 73 76
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R 72 76
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G 72 76
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B 72 76
	VGA_50S	VGA	GPU_VGA_R 72 73
	VGA_50S	VGA	GPU_VGA_G 72 73
	VGA_50S	VGA	GPU_VGA_B 72 73
	VGA_50S	VGA	GPU_TV_C 72 73
	VGA_50S	VGA	GPU_TV_Y 72 73
	VGA_50S	VGA	GPU_TV_COMP 72 73
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC 73 76
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC 73 76

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*			0.100 MM	2.54 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

M75 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_SRC7)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_XDP_P	
(CK505_SRC7)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_XDP_N	
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P	34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P	78
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N	78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P	78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N	78
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>	37
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N	41
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_90D	USB	USB2_RT_P	43
(USB_EXTA)	USB_90D	USB	USB2_RT_N	43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P	44
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P	44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	59
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P	50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 71 72
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	REMTHMSNS_DX_P	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P	51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P	75
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N	75
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_P	75 77
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_N	75 77
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_P<3..0>	75 77
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_N<3..0>	75 77
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_P	75 77
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_N	75 77
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_P<3..0>	75 77
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_N<3..0>	75 77
	TMDS_100D	TMDS	TMDS_CLK_R_P	76
	TMDS_100D	TMDS	TMDS_CLK_R_N	76
	TMDS_100D	TMDS	TMDS_CLK_F_P	76
	TMDS_100D	TMDS	TMDS_CLK_F_N	76
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>	76
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>	76
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R	76
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G	76
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC	76
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC	76
		PP1V8_MEM	PP1V8_S3	8 31 32 38 50 62 87
		PP1V8_MEM	PP1V8_S3	8 31 32 38 50 62 87
		GND	GND	
		SB_POWER	PP3V3_S5	8 24 25 26 27 28 46 48 55 57 60
		SB_POWER	PP3V3_S0	52 57 58 59 65 74 75 77 78 82 83 84 85 86 87
		SB_POWER	PP1V5_S0	8 11 12 19 22 26 27 34 63
		SB_POWER	PP1V25_S0_SB_DMI	29 30 31 32 42 46 47 48 50 51
		ENET_POWER	PP1V05_ENET_SRC	
		FW_POWER	LCL_FW_1V8	

M75 Specific Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

M75 Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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