3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
### BOARD STACK-UP AND CONSTRUCTION

#### Top Layer

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>MLB STACKUP</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUND</td>
<td>CONFORMAL_COAT 0.018</td>
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<tr>
<td>SIGNAL(High Speed)</td>
<td>L1-L2 0.043</td>
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<tr>
<td>SIGNAL(High Speed)</td>
<td>L1 SIGNAL(TOP) 0.018</td>
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<tr>
<td>GROUND</td>
<td>L2-GROUND 0.014</td>
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<tr>
<td>POWER</td>
<td>L2-L3 0.076</td>
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<tr>
<td>SIGNAL(High Speed)</td>
<td>L3 SIGNAL 0.014</td>
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<tr>
<td>SIGNAL(High Speed)</td>
<td>L3-L4 0.156</td>
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<tr>
<td>GROUND</td>
<td>L4 SIGNAL 0.014</td>
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<tr>
<td>SIGNAL(High Speed)</td>
<td>L4-L5 0.076</td>
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<tr>
<td>SIGNAL(High Speed)</td>
<td>L5 GND 0.014</td>
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<tr>
<td>SIGNAL</td>
<td>L5-L6 0.076</td>
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<tr>
<td>POWER</td>
<td>L6 POWER 0.031</td>
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<td>SIGNAL</td>
<td>L6-L7 0.076</td>
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<tr>
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<td>L7 POWER 0.07</td>
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<td>L7-L8 0.014</td>
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<td>SIGNAL</td>
<td>L8-L9 0.014</td>
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<td>L9 SIGNAL 0.014</td>
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<tr>
<td>SIGNAL</td>
<td>L9-L10 0.156</td>
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<td>SIGNAL</td>
<td>L10 SIGNAL 0.014</td>
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<td>L10-L11 0.076</td>
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<td>L11 SIGNAL 0.014</td>
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<td>SIGNAL</td>
<td>L11-L12 0.07</td>
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<td>L12 SIGNAL(BOTTOM) 0.047</td>
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#### Bottom Layer

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<td>CONFORMAL_COAT 0.018</td>
</tr>
</tbody>
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**TOTAL** 1.276

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**Page Notes**: Page dimensions 1224.0x792.0

**BOM TABLE FOR HF POSCAPS**

**CONFIGURATION OPTIONS**

**SYNC_MASTER**

---

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CPU VCORE HF AND BULK DECOUPLING
4x 330uF, 20x 10uF 0805

VCCP (CPU I/O) DECOUPLING
1x 330uF, 6x 0.1uF

VCCA (CPU AVdd) DECOUPLING
1x 10uF, 1x 0.01uF

CPU Decoupling & VID

PLACE C1235 CLOSE TO CPU
PLACE C1236, C1237, C1238 AND C1239 NEAR PIN B26 OF U1000

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)
C1235, C1236, C1237 AND C1238 NEED TO SEE SOCKET CAVITY

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

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D 051-7559 *
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PRO PIN.
Tie VCC_AXG and VCC_AXG_NCTF to GND.

Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

Internal Graphics Disable and filtered at all times!

NOTE: Must keep VDDC_TVDAC powered VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, rails must be filtered except for VCCA_CRT.

All CRT/TVDAC rails must be powered. All CRT Disable / TV-Out Enable TVx_DAC and TVx_RTN to GND. Must power all should connect to GND through 75-ohm resistors.

omit filtering components. Unused DAC outputs S-Video: DACB & DACC only

Composite: DACA only

Tie VCC_TX_LVDS and VCCA_LVDS to GND.

against the National Semiconductor mark.

8C6 8C6 8C6

8B6 8B6 8B6

8B6 8B6 8B6

68B6 71D3 68B6 71D3

68C6 71D3 68C6 71D3


67B6 67B6 67B6

67C6 67C6 67C6

www.vinafix.vn
Current numbers from Crestline EDS, doc #21749.

7700 mA (Int Graphics)
5 mA (standby)
1700 mA (1 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1310 mA (Ext Graphics)

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SCALE
051-7559
NOTE: This filter is required even if using only external graphics. TACT_PUC also powers internal thermal sensors.

Current numbers from Crestline EDS Addendum, doc #20127.

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.3 MM

VOLTAGE=1.25V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.3 MM

MIN_LINE_WIDTH=0.4 MM

WF: Check part properties

WF: Matanzas has 2x 330uF

NEED TO FIND A "1£GH, 500MA, 78MOHM" INDUCTOR

These 2 caps should be

Layout Note: Route to caps, then GND

Layout Note: Place in GMCH cavity

WF: Is this the best part to use?

WF: Is this the best part to use?

WF: Check part properties

WF: Check part properties

These 4 caps should be

Layout Note: Route to caps, then GND

Layout Note: Place in GMCH cavity

Layout Note: Place in GMCH cavity

Layout Note: Place in GMCH cavity

Layout Note: Place in GMCH cavity

Layout Note: Place in GMCH cavity

WF: SYNC_MASTER=WFERRY

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

APPLE INC.
In CLOSE=12.5pF
Change Y2800 to 197S019 -7.0mmx1.5mmx1.4mm

This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Initial resistor values are based on CRB, but may change after characterization.

Initial resistor values are based on CRB, but may change after characterization.

It may take a few days before this is done through 2-input NAND gate-APN:311S0304
Pulled a new APN for U2803(0.6mm max
2-input NAND gate-APN:311S0304)
This will allow us to sequence this part under wireless card
CLK Termination

CLKREQ Controls

For reducing noise coupling to wireless frequencies

Clock Termination

www.vinafix.vn
When they get cheaper.
The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.
One cap for each side of every RPAK, one cap for every two discrete resistors

Layout note: place one cap close to every two pullup resistors terminated to PP099_06_MEM_TERM
BLEED CIRCUIT TO DISCHARGE ODD POWER RAIL WHEN ODD IS DISABLED.
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NOTE: Unused pins have "NC" names. Unused pins designated as inputs should be left floating.
Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits.
HEAT-PIPE/FIN-STACK TEMPERATURE ZONE

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GUARD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GUARD

CPU TEMPERATURE ZONE

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GUARD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GUARD

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1.8V/0.9V POWER SUPPLY

State | PM_SLP_S4 | PM_SLP_S3 | PP1V8_S3 | PP0V9_S0
-----|----------|----------|---------|---------
S0   | HIGH    | HIGH     | 1.8V    | 0.9V    |
S3   | HIGH    | LOW      | 1.8V    | 0.9V    |
S5/G3HIGH | LOW | LOW      | 0.6V    | 0.9V    |

Vout = 0.75V * (1 + Ra / Rb)

Routing Note:
- put 6 vias under the thermal pad
- using Kevin connection.
- using separate trace.
- Place C7543 near NB
- Place C7504 near U7501 pin 7

1.8V/0.9V Supplies
SYNC MASTER-SUBMIT DATE: 07/13/2005
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AGREES TO THE FOLLOWING

www.vinafix.vn
3.425V G3H SUPPLY

Supply needs to guarantee 3.3V delivered to SMC VRef generator

Vout = 1.25V \times (1 + \frac{Ra}{Rb})

1.25V So REGULATOR

Vout = 0.8V \times (1 + \frac{Ra}{Rb + Rc})

3.42V/1.25V Switcher

LATEST ISSUE: 2007/3/8
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL

1.8V S3 RUN/SS CONTROL

5V S3 FET

- MOSFET: P-738P
- RDS(ON): 0.051 A
- 3.3V S3 RUN/SS CONTROL

3.3V S3 FET

- MOSFET: P-738P
- RDS(ON): 0.098 A

LATEST ISSUE: 2006/12/22
**CPU / FSB Net Properties**

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<tr>
<th>Name</th>
<th>Direction</th>
<th>Type</th>
<th>Width</th>
<th>Min Net</th>
<th>Max Net</th>
<th>Min Neck</th>
<th>Max Neck</th>
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<tbody>
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<td>CPU_POWER1</td>
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**CPU Signal Constraints**

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<tbody>
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All FSB signals with impedance requirements are 55-ohm single-ended.

**FSB (Front-Side Bus) Constraints**

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<th>Direction</th>
<th>Type</th>
<th>Width</th>
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<th>Min Neck</th>
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<td>IN, OUT</td>
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**CPU/FSB Constraints**

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</tbody>
</table>

**SOURCE:** Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

Most CPU signals with impedance requirements are 55-ohm single-ended.
**CRT_HSYNC/CRT_VSYNC** signals are 55-ohm +/- 15% single-ended impedance.
- 55-ohm +/- 15% from second termination resistor to connector.
- 50-ohm +/- 15% from first to second termination resistor.
- 37.5-ohm +/- 15% from GMCH to first termination resistor.

**CRT & TVDAC** signal single-ended impedence varies by location:

**LVDS** signals are 100-ohm +/- 20% differential impedence.

---

### PCI-Express / DMI Bus Constraints

**PHYSICAL_RULE_SET**

- **TVDAC_2TVDAC**
- **CRT_2CRT**
- **PCIE_100D**
- **DMI_100D**
- **CRT_55S**
- **CRT_50S**

**SPACING_RULE_SET**

- **CRT_SYNC2SYNC**
- **TVDAC_2TVDAC**
- **CRT_2CRT**

**ELECTRICAL_CONSTRAINT_SET**

- **LVDS_A_DATA**
- **LVDS_A_CLK**
- **DMI_S2N**
- **DMI_N2S**
- **PEG_R2D**
- **PEG_D2R**
- **LVDS_100D**
- **DMI_100D**
- **PCIE_100D**

**AREA_TYPE**

- **MINIMUM LINE WIDTH**
- **DIFFPAIR PRIMARY GAP**
- **DIFFPAIR NECK GAP**

**TABLE_PHYSICAL_RULE_ITEM**

- **MAXIMUM NECK LENGTH**
- **MINIMUM NECK WIDTH**

**TABLE_SPACING_RULE_ITEM**

- **LINE-TO-LINE SPACING ON LAYER?**
- **ALLOW ROUTE ON LAYER?**

**TABLE_SPACING_ASSIGNMENT_ITEM**

- **WEIGHT**

**NB Constraints**

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Sync Date = 06/12/2006"
### FireWire Interface Constraints

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<tr>
<th>Port</th>
<th>Type</th>
<th>Name</th>
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<th>Min Width</th>
<th>Min Length</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Min Pair Gap</th>
<th>Min Neck Gap</th>
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<td>0.2</td>
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### FireWire Net Properties

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<th>Constraint-Property</th>
<th>Min Width</th>
<th>Min Length</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Min Pair Gap</th>
<th>Min Neck Gap</th>
</tr>
</thead>
<tbody>
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<td>Port 1</td>
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<td>0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.1</td>
</tr>
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<td>0.1</td>
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<td>0.1</td>
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</tbody>
</table>

### SMC SMBus Net Properties

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<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Min Pair Gap</th>
<th>Min Neck Gap</th>
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<td>0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.1</td>
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<td>0.1</td>
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### FireWire & SMC Constraints

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<th>Min Length</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Min Pair Gap</th>
<th>Min Neck Gap</th>
</tr>
</thead>
<tbody>
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<td>Port 1</td>
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<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.1</td>
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<tr>
<td>Port 2</td>
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<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.1</td>
</tr>
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