1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K23

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0000774489	PRODUCTION RELEASED	2009-08-20

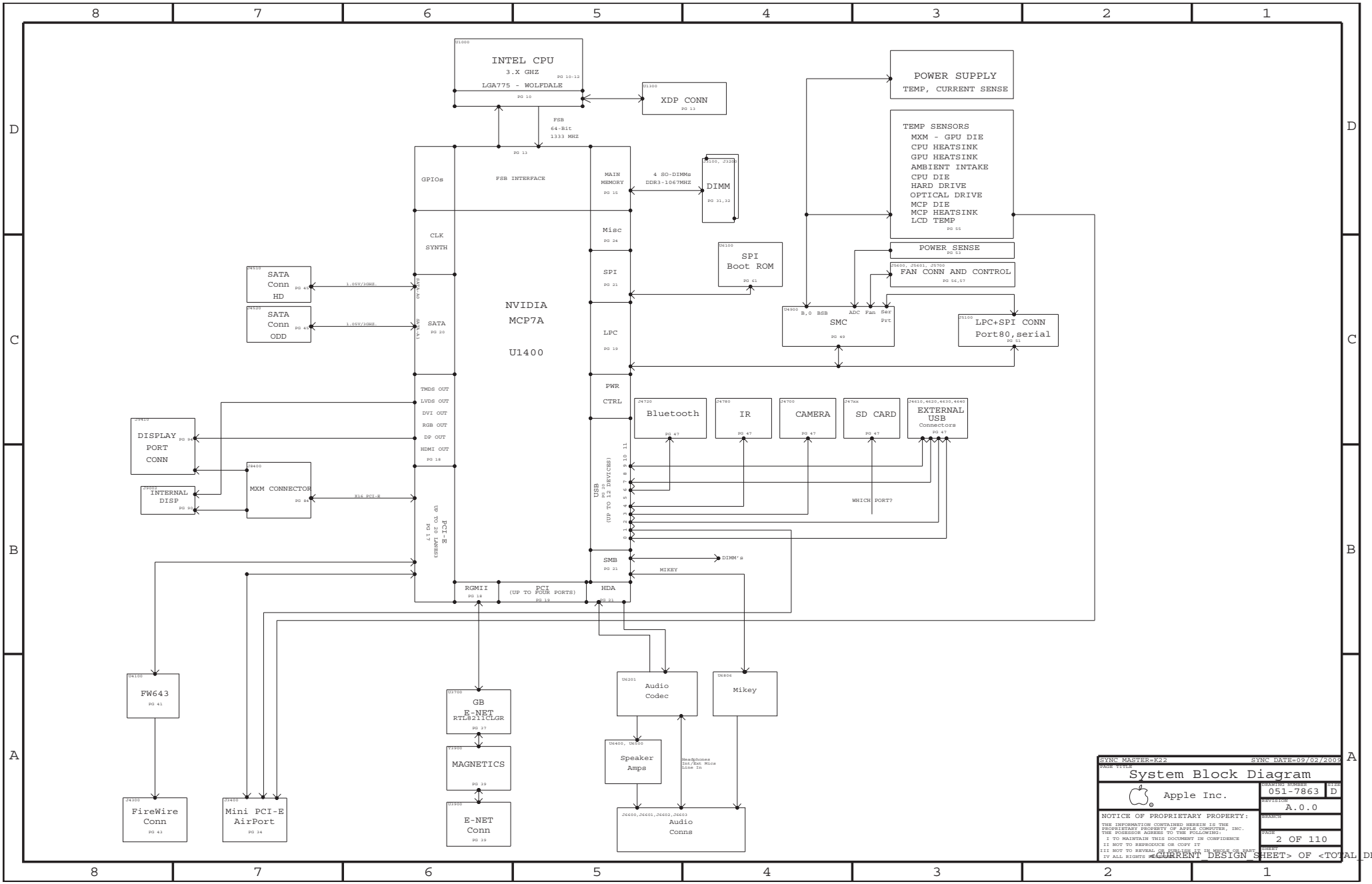
LAST_MODIFIED=Wed Sep 2 16:45:56 2009

DRAWING
TITLE=K22
ASSET=DRAWING
LAST_MODIFIED=Wed Sep 2 16:45:56 2009

DRAWING TITLE: SCH,K23,MLB

Apple Inc.

DRAWING NUMBER: 051-7863 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 110



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

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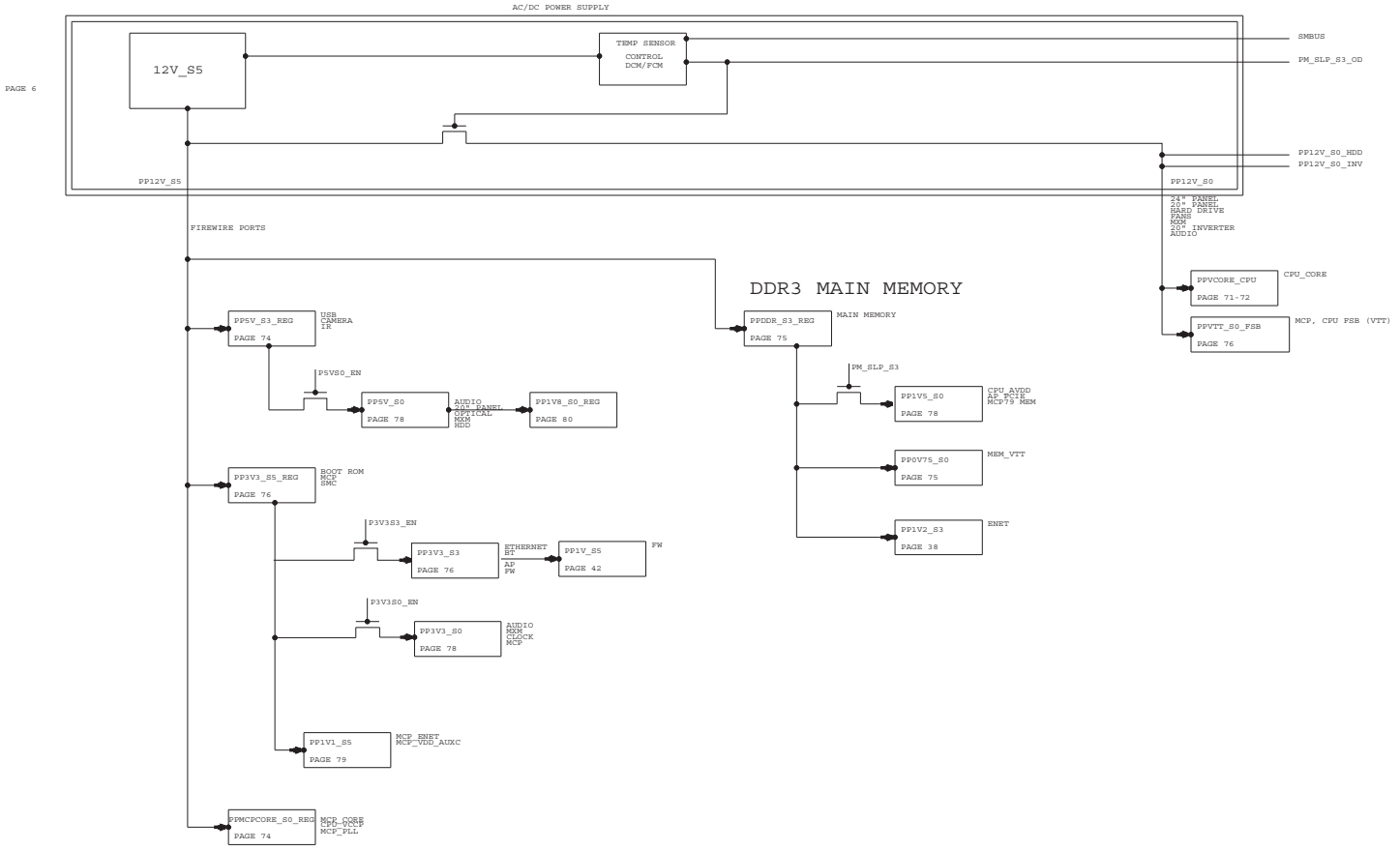

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9879	PCBA,MLB,BETTER,K23	K23,2P80GHZ_CPU,BASIC,MXM,K23_MXM
639-0394	PCBA,MLB,2.80 GHZ-2M,K23	K23,2P80GHZ_2M_CPU,BASIC,MXM,K23_MXM
639-0185	PCBA,MLB,2.93 GHZ,K23	K23,2P93GHZ_CPU,BASIC,MXM,K23_MXM
630-9983	PCBA,MLB,BEST,K23	K23,3P0GHZ_CPU,BASIC,MXM,K23_MXM
639-0509	PCBA,MLB,3.06 GHZ,K23	K23,3P06GHZ_CPU,BASIC,MXM,K23_MXM
639-0109	PCBA,MLB,3.16 GHZ,K23(INVESTIGATION)	K23,3P16GHZ_CPU,BASIC,MXM,K23_MXM
630-9880	PCBA,MLB,ULTIMATE,K23	K23,3P33GHZ_CPU,BASIC,MXM,K23_MXM
607-4427	PCBA,MLB,DEV,K23	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP7A,XDP,BETTER,MCP_ISL9563A,PRODUCTION
MCP7A	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP
DEV_GROUP	XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE,MCP_CPU_TDIODE,PECI_SMB,MOJOMUX

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
338S0731	1	IC,GMCP,MCP7A-JA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	IG	MCP -J SKU HAS INTEGRATED GPU
338S0732	1	IC,MCP,MCP7A-DA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	MXM	MCP -D SKU DOES NOT
341T0170	1	IC,EFI BOOTROM,K22/K23	U6100	CRITICAL		
338S0765	1	IC,XIO2211ZAY,1394B,167BGA	U4100	CRITICAL		
338S0694	1	IC,RTL8251CA,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL		
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL		

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3745	1	WLP,QXXX,Q8,2.80G,65W,1066,R0.9M,LGA	CPU	CRITICAL	2P80GHZ_CPU
337S3742	1	WLP,SLB9J,PRQ,2.83G,65W,1333,R0,6M,LGA	CPU	CRITICAL	2P83GHZ_CPU
337S3726	1	WLP,SLB9J,PRQ,3.00,65W,1333,R0,6M,LGA	CPU	CRITICAL	3P0GHZ_CPU
337S3715	1	WLP,SLB9K,PRQ,3.16G,65W,1333,R0,6M,LGA	CPU	CRITICAL	3P16GHZ_CPU
337S3727	1	WLP,SLB9L,PRQ,3.33G,65W,1333,R0,6M,LGA	CPU	CRITICAL	3P33GHZ_CPU
337S3807	1	WLP,SLB9L,PRQ,2.93G,65W,1333,R0,6M,LGA	CPU	CRITICAL	2P93GHZ_CPU
337S3766	1	WLP,SLB9L,PRQ,3.06G,65W,1333,R0,6M,LGA	CPU	CRITICAL	3P06GHZ_CPU
337S3804	1	WLP,SLGU9,PRQ,2.80G,65W,1066,R0.9M,LGA	CPU	CRITICAL	2P80GHZ_2M_CPU

K23 PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7863	1	SCH,K23,MLB	SCH1		K23
	820-2507	1	PCBF,K23,MLB	MLB1		K23
(338S0489 - BLNK)	341T0169	1	IC,SMC,K23	U4900	CRITICAL	K23

ALTERNATES

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

BOM Configuration

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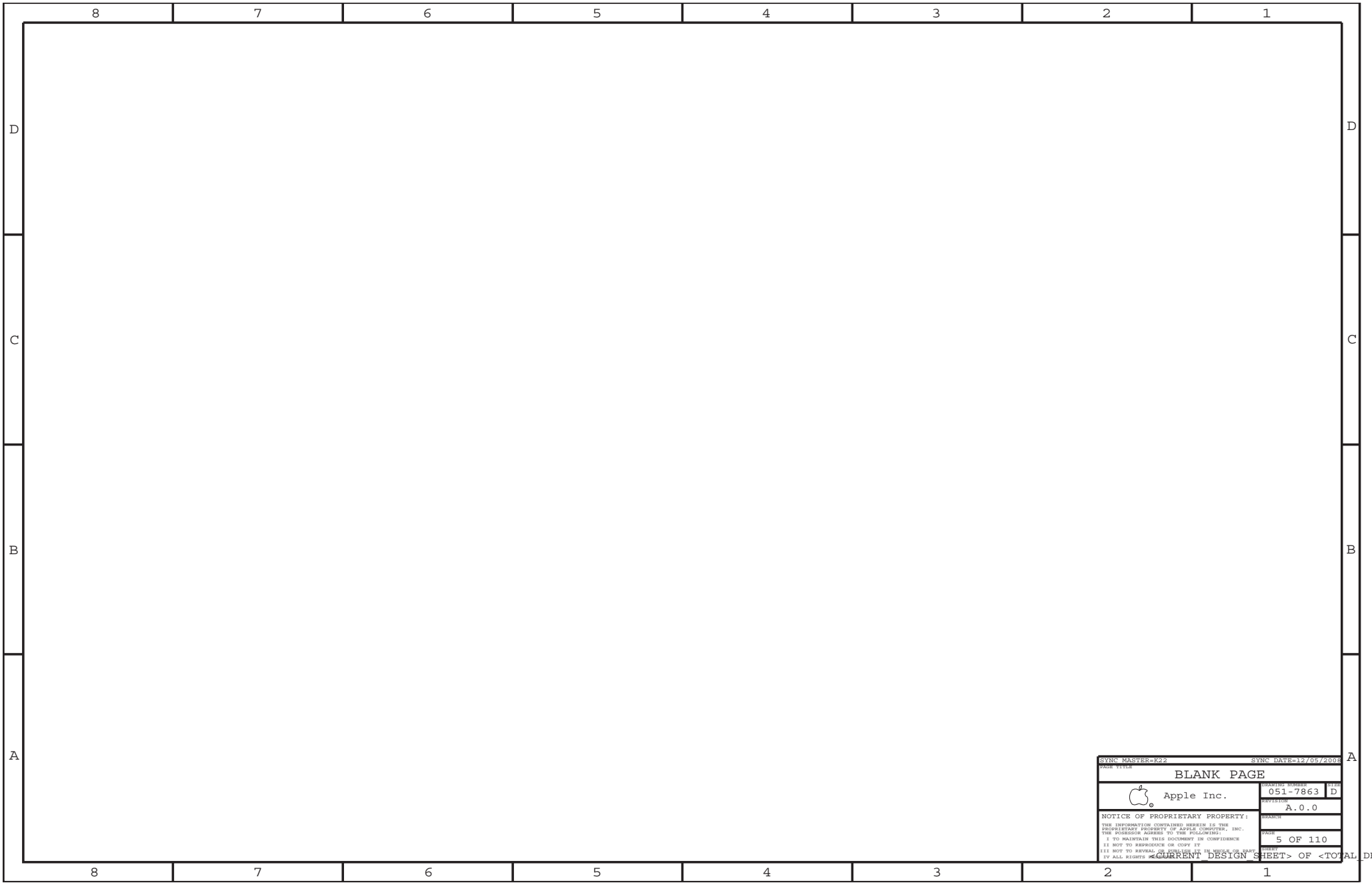
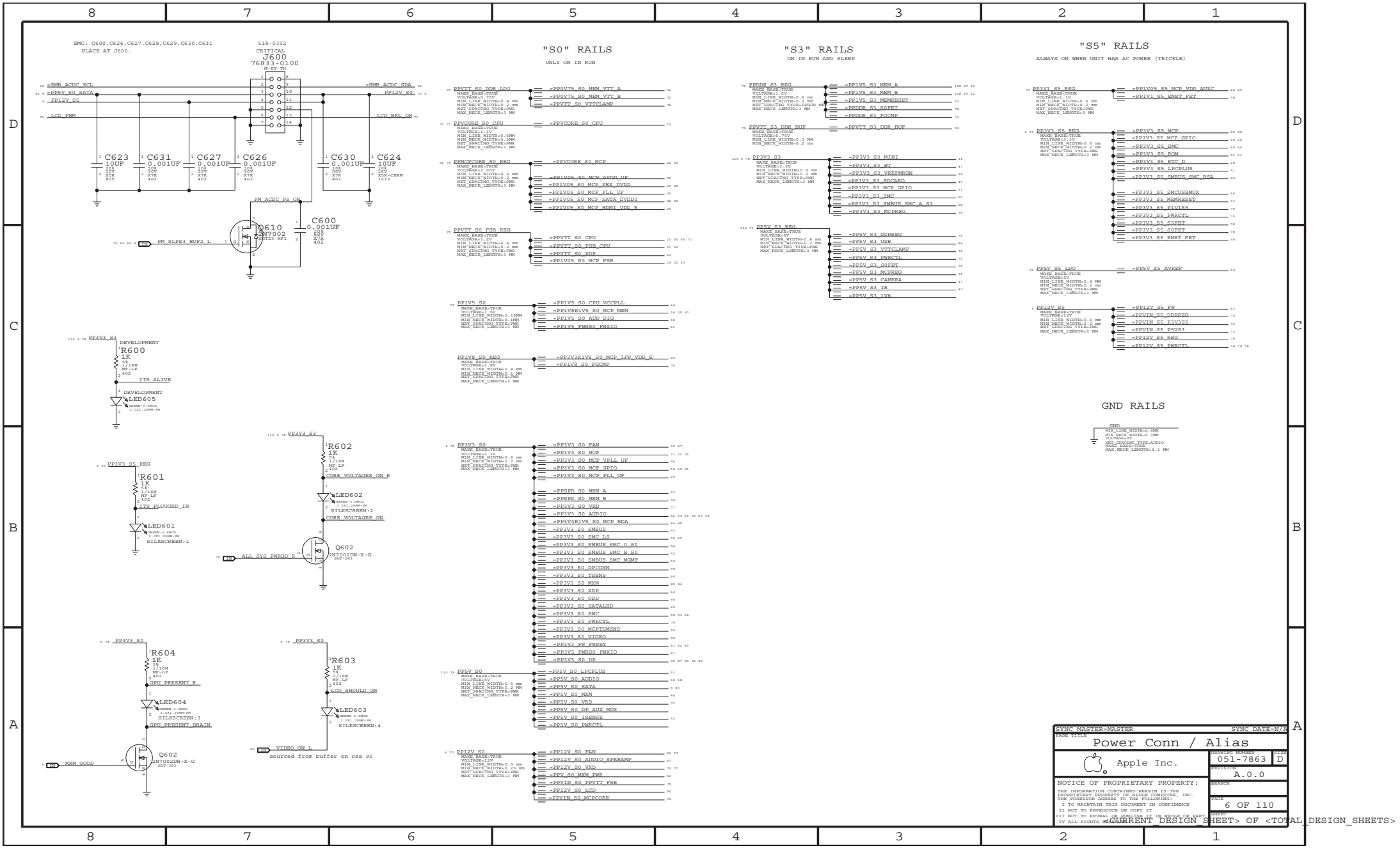
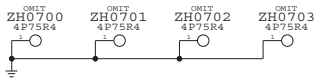




CPU Heatsink

4mm Plated Holes (998-0850)

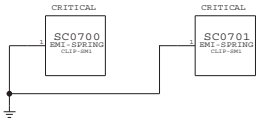


DIMM CONNECTOR NUTS

Nuts (805-9582)

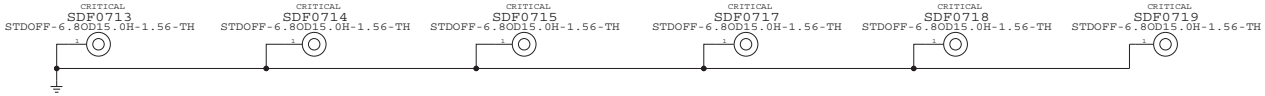
MCP Heatsink

EMC Springs (870-1125)



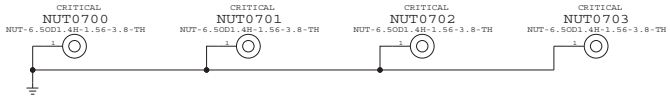
Rear Cover

Standoffs (860-1255)



Backer Plate

Nuts (835-0269)



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Holes

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NC ON UNUSED ALIASES

MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE, NO_TEST=TRUE
MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE, NO_TEST=TRUE
MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE, NO_TEST=TRUE
MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE, NO_TEST=TRUE
CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE, NO_TEST=TRUE
CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE, NO_TEST=TRUE
CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE, NO_TEST=TRUE
CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MCP_RGB_HSYNC	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MCP_RGB_VSYNC	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_AD<31..15>	NC_PCI_AD<31..15>	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_C_BE_L<1..0>	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MCP_BUF_SIO_CLK	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE, NO_TEST=TRUE

TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_ENET_PWRDWN_L	NC_ENET_PWDWN_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MCP_KBDRSTIN_L	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MCP_GPIO_18	NC_MCP_GPIO_18	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_C_BE_L<3>	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_CLK0	NC_PCI_CLK0	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_GNT0_L	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_INTY_L	NC_PCI_INTY_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_EXCARD_PRSNT_L	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PE4_CLKREQ_L	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_MINI_N	NC_USB_MINI_N	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_MINI_P	NC_USB_MINI_P	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_EXCARD_N	NC_USB_EXCARD_N	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_EXCARD_P	NC_USB_EXCARD_P	MAKE_BASE=TRUE, NO_TEST=TRUE
ODD_PWR_EN_L	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE, NO_TEST=TRUE
EXCARD_CLKREQ_L	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_AD<12..10>	NC_PCI_AD<12..10>	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCI_AD<8>	NC_PCI_AD<8>	MAKE_BASE=TRUE, NO_TEST=TRUE

TP_PCIE_PE4_R2D_CP	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_PE4_D2RP	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE, NO_TEST=TRUE
PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_TPAD_N	NC_USB_TPAD_N	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_TPAD_P	NC_USB_TPAD_P	MAKE_BASE=TRUE, NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

TP_MEM_A_CLK2P	NC_MEM_A_CLK2P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_A_CLK5P	NC_MEM_A_CLK5P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_A_CLK5N	NC_MEM_A_CLK5N	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_B_CLK2P	NC_MEM_B_CLK2P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_B_CLK2N	NC_MEM_B_CLK2N	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_B_CLK5P	NC_MEM_B_CLK5P	MAKE_BASE=TRUE, NO_TEST=TRUE
TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE, NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

GMUX_JTAG_TCK_L	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE, NO_TEST=TRUE
GMUX_JTAG_TDO	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE, NO_TEST=TRUE
GMUX_JTAG_TDI	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE, NO_TEST=TRUE
GMUX_JTAG_TMS	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE, NO_TEST=TRUE

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PAGE TITLE
UNUSED SIGNAL ALIAS

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SIGNAL ALIAS

TP_MLB_RAM_VENDOR = MXM_GOOD (MAKE_BASE=TRUE)

PM_SLP_S3_L — R910 15 — PM_SLPS3_BUF2_L (MAKE_BASE=TRUE)
(P50 HAS A 100K TO GROUND)

PM_SLPS3_BUF1_L (MAKE_BASE=TRUE) — R911 15 — R912 100K

PEG Slot Support

PEG_CLK100M_P	GPU_CLK100M_PCIE_P
PEG_CLK100M_N	GPU_CLK100M_PCIE_N
=PEG_R2D_C_P<0..15>	PEG_R2D_C_P<0..15>
=PEG_R2D_C_N<0..15>	PEG_R2D_C_N<0..15>
=PEG_D2R_P<0..15>	PEG_D2R_P<0..15>
=PEG_D2R_N<0..15>	PEG_D2R_N<0..15>
PEG_PRSNT_L	MXM_DETECT_L

(all MAKE_BASE=TRUE)

USB_EXTC_OC_L (MAKE_BASE=TRUE) = USB_EXTD_OC_L

K22/K23 Use one GPIO for both ports 2&3 OC

USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD IT'S OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

=DVI_HPD_GMUX_INT = HPLUG_DET2 (MAKE_BASE=TRUE) — R900 20K

PCIE_FW_PRSNT_L
PCIE_MINI_PRSNT_L

Platform Reset Connections

LPC Reset (Unbuffered)

LPC_RESET_L — R981 33 — DEBUG_RESET_L
PLACEMENT_NOTE=Place close to U1400
R983 33 — SMC_LRESET_L
PLACEMENT_NOTE=Place close to U1400

PCIE Reset (Unbuffered)

PCIE_RESET_L — R992 0 — FW_RESET_L
R991 0 — MINI_RESET_L
R990 0 — PEG_RESET_L
R971 0 — PCA9557D_RESET_L
R993 0 — CARDREADER_PLT_RST_L

MEM_VTT_EN_R — R972 33 — DDRVTT_EN
NO STUFF C973 0.47UF

LPC_CLK33M_SMC_R — R925 33 — LPC_CLK33M_SMC
R926 33 — LPC_CLK33M_LPCPLUS
PLACEMENT_NOTE=Place close to U1400

PM_CLK32K_SUSCLK_R — R929 22 — PM_CLK32K_SUSCLK
PLACEMENT_NOTE=Place close to U1400

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

MCP_CPUVDD_EN — R930 22 — MCP_CPU_VLD
PLACEMENT_NOTE=Place close to U1400

-MCP_MII_RXER
-MCP_MII_COL
-MCP_MII_CRS
= MCP_MII_NU (MAKE_BASE=TRUE) — R955 47K

SYNC MASTER=MASTER SYNC DATE=N/A
PAGE TITLE: Signal Aliases
Apple Inc.
DRAWING NUMBER: 051-7863 SIZE: D
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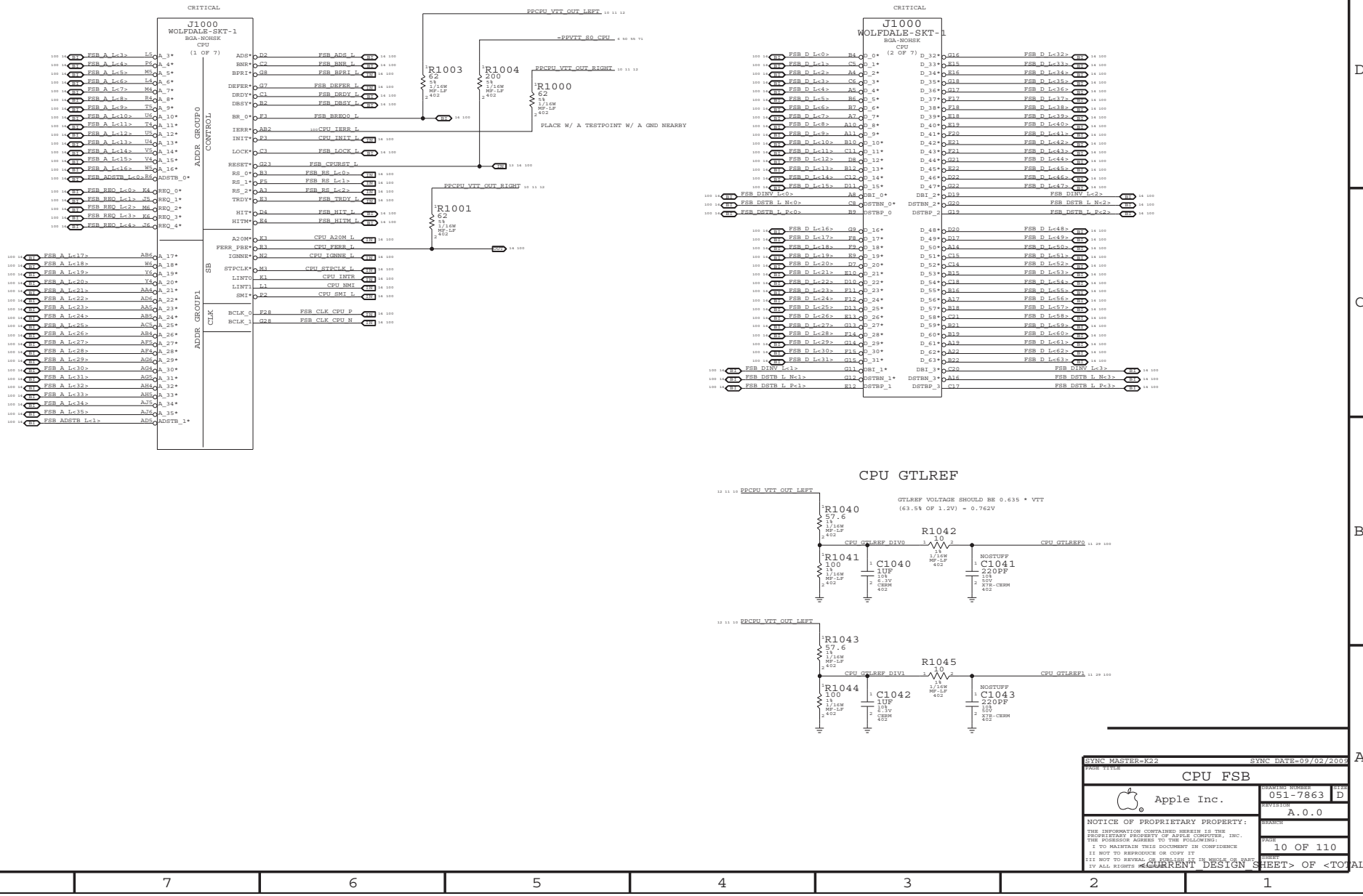
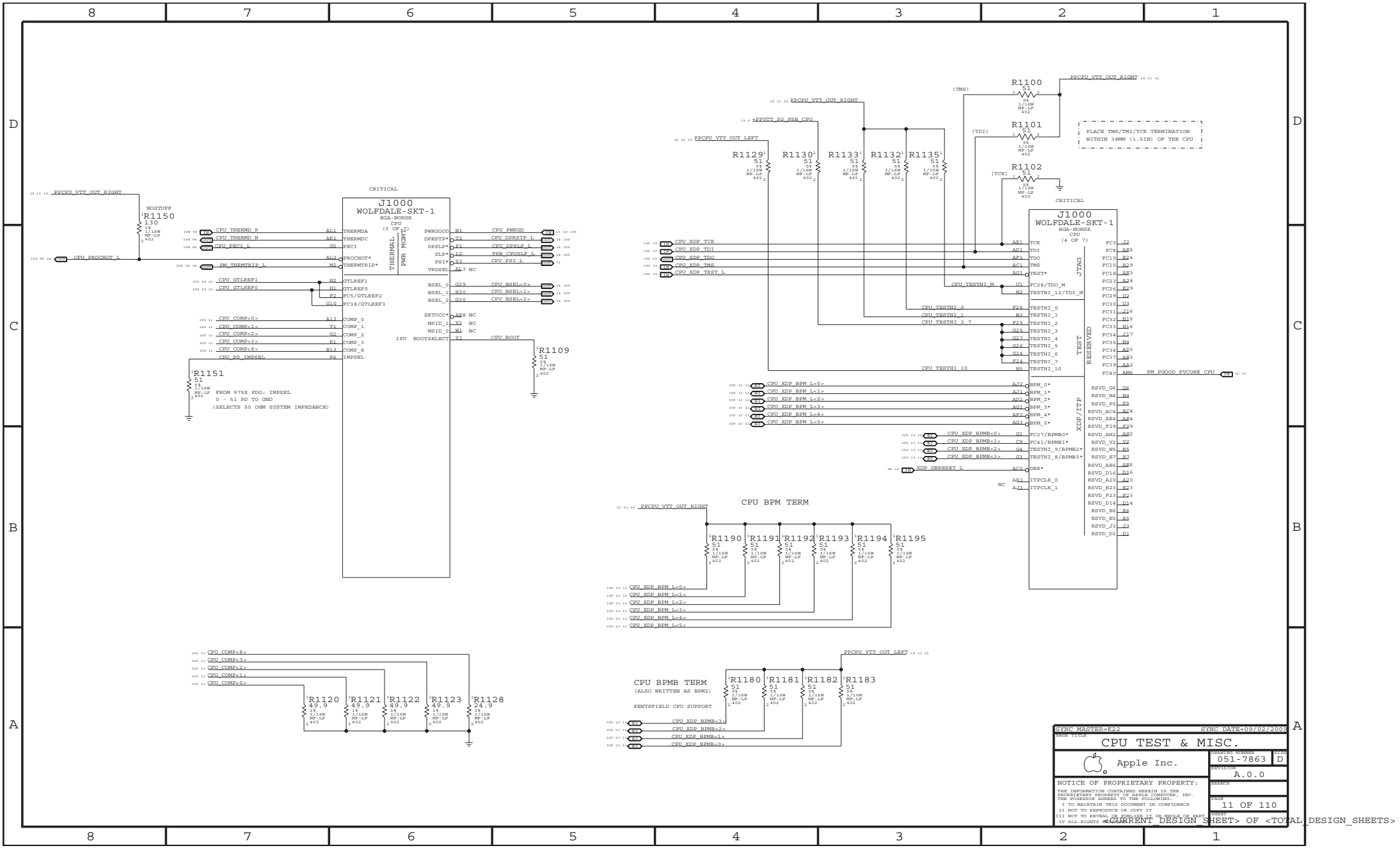
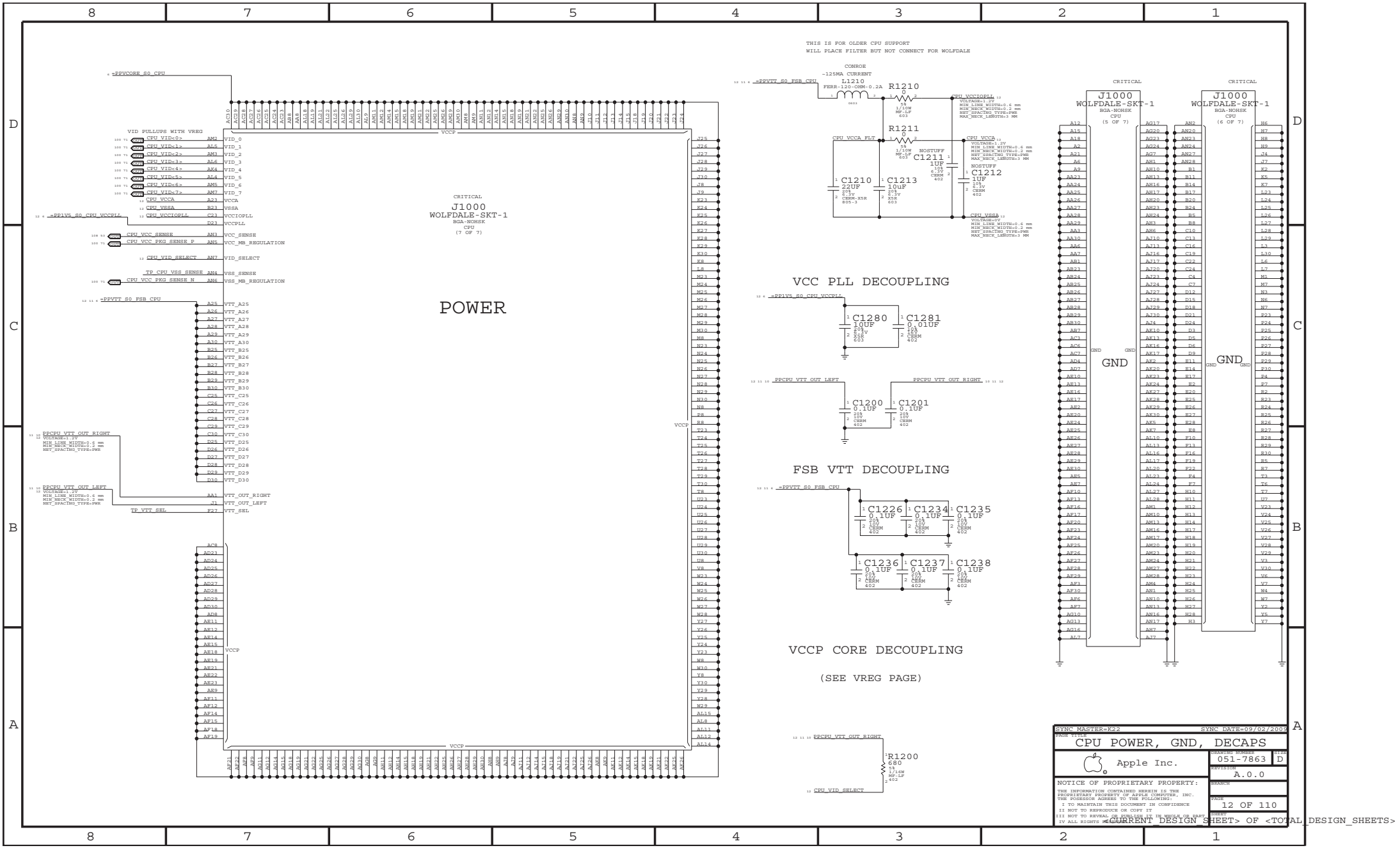
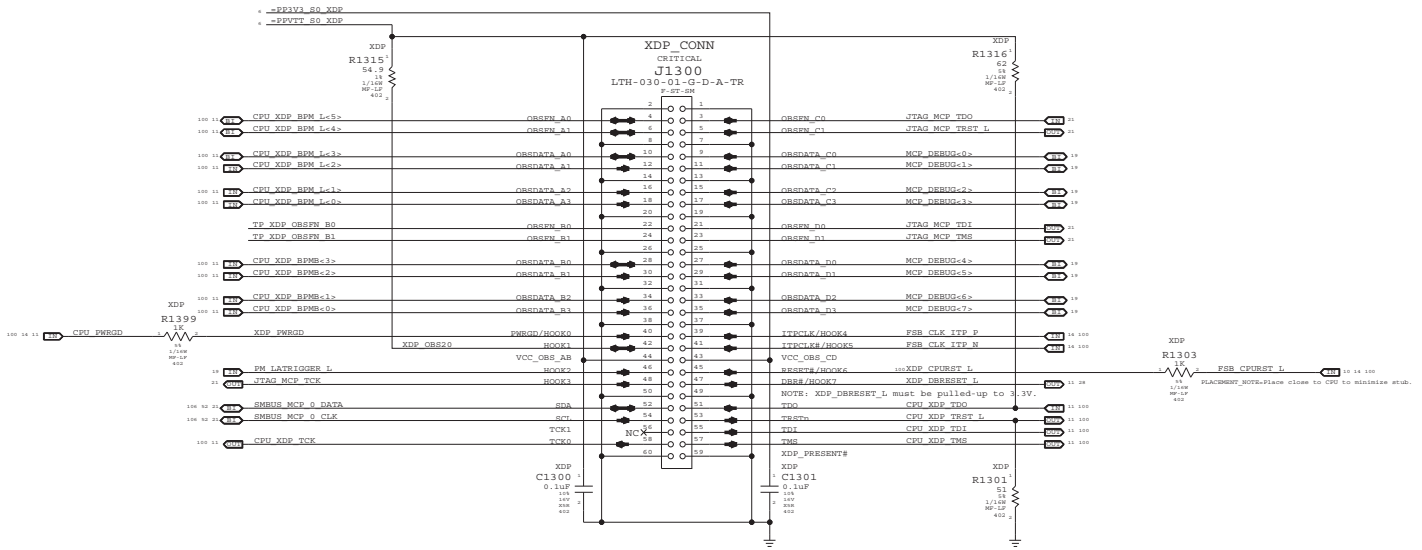
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>







MCP79-specific pinout



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
eXtended Debug Port (XDP)

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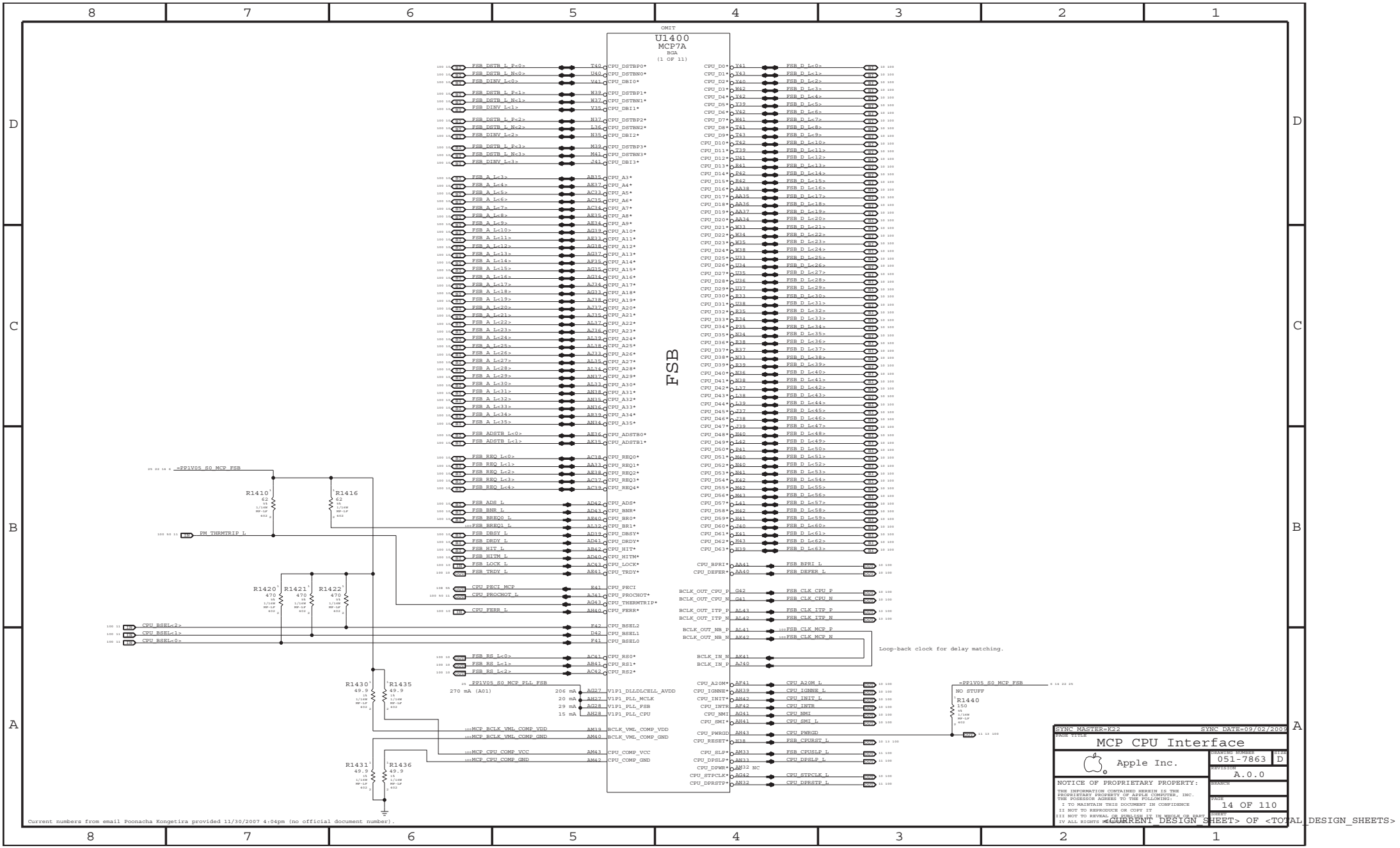

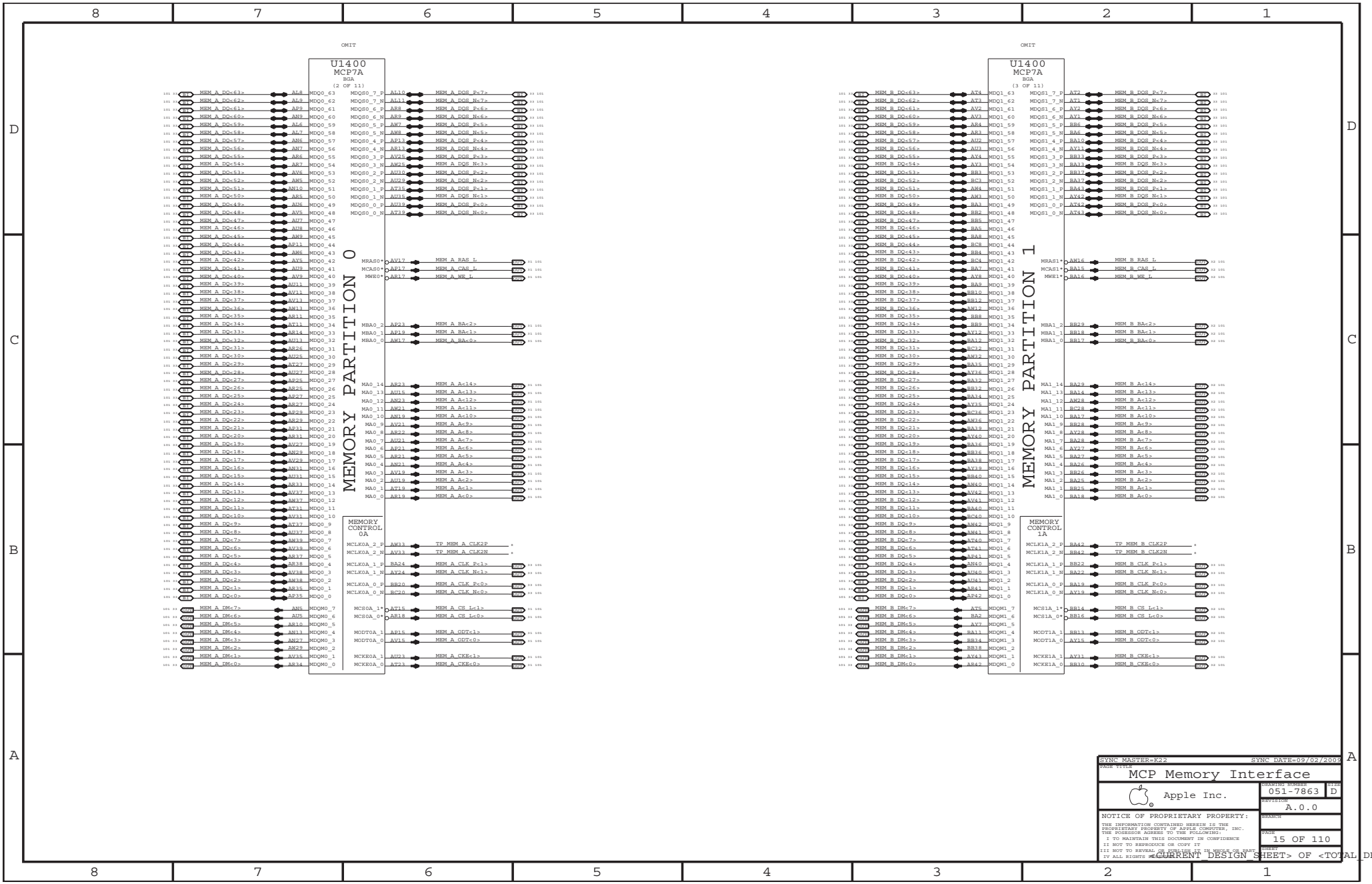

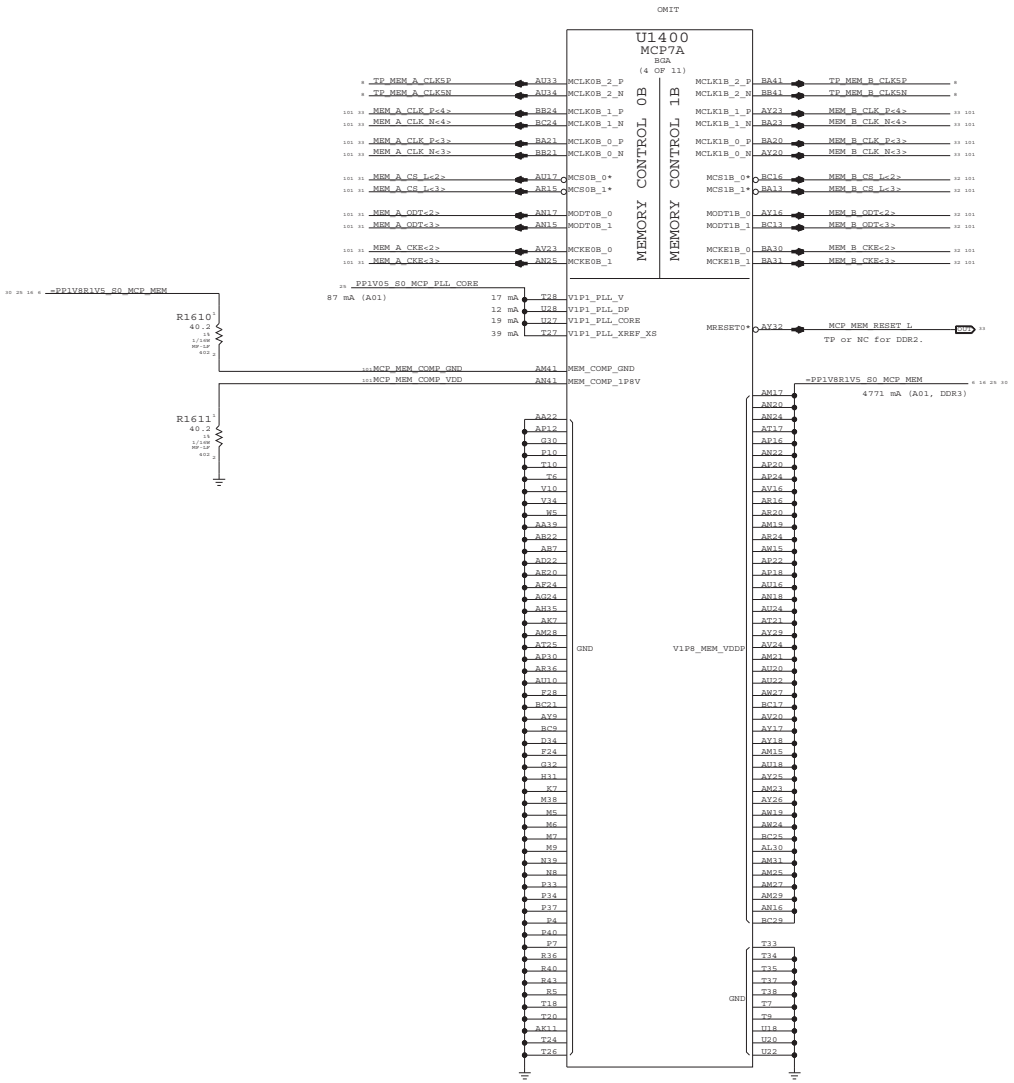

SYNC MASTER=K22 SYNC DATE=09/02/2006

PAGE TITLE

MCP MEMORY CNTRL & MISC

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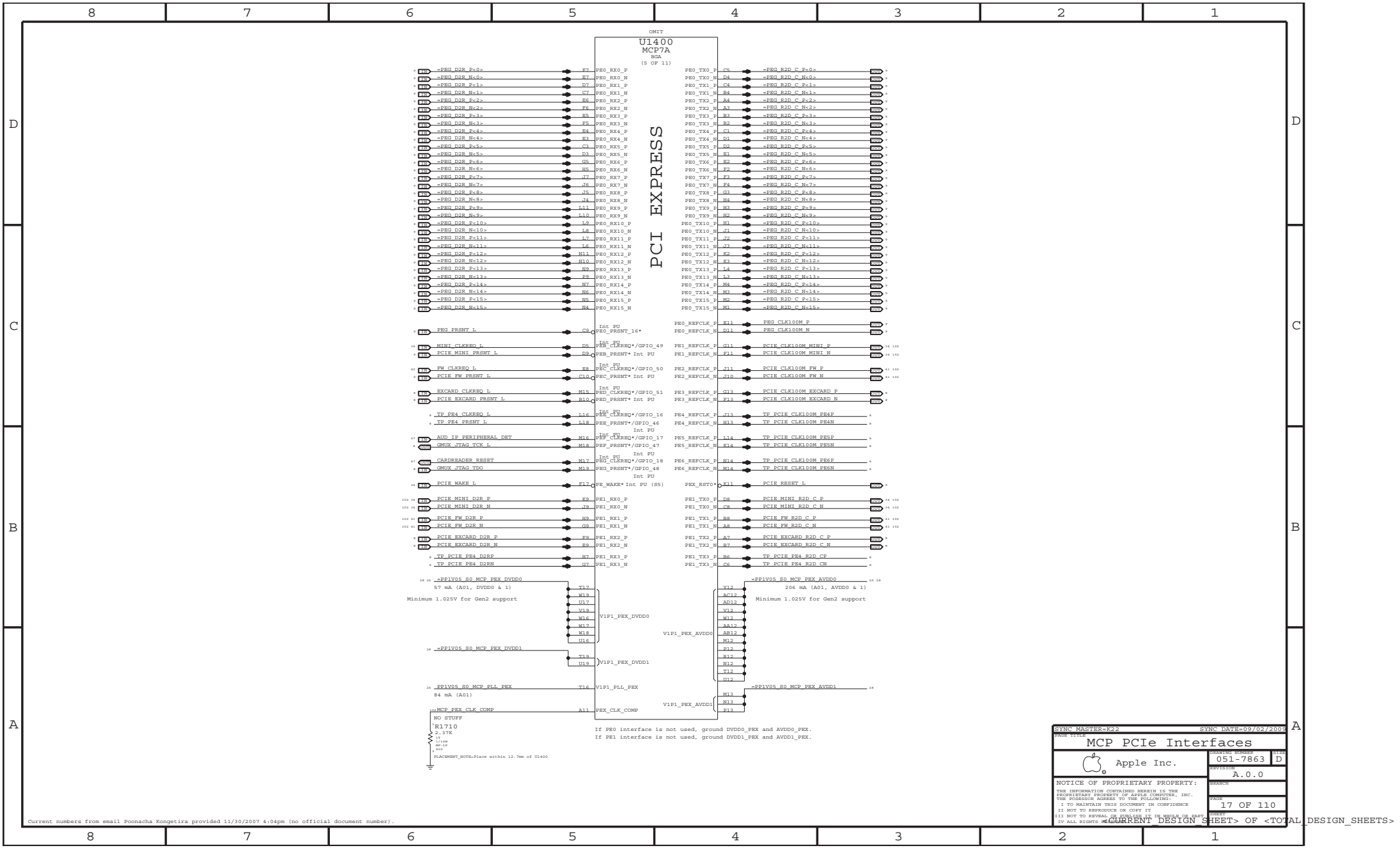
SHEET

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

MCP PCIe Interfaces

Apple Inc.

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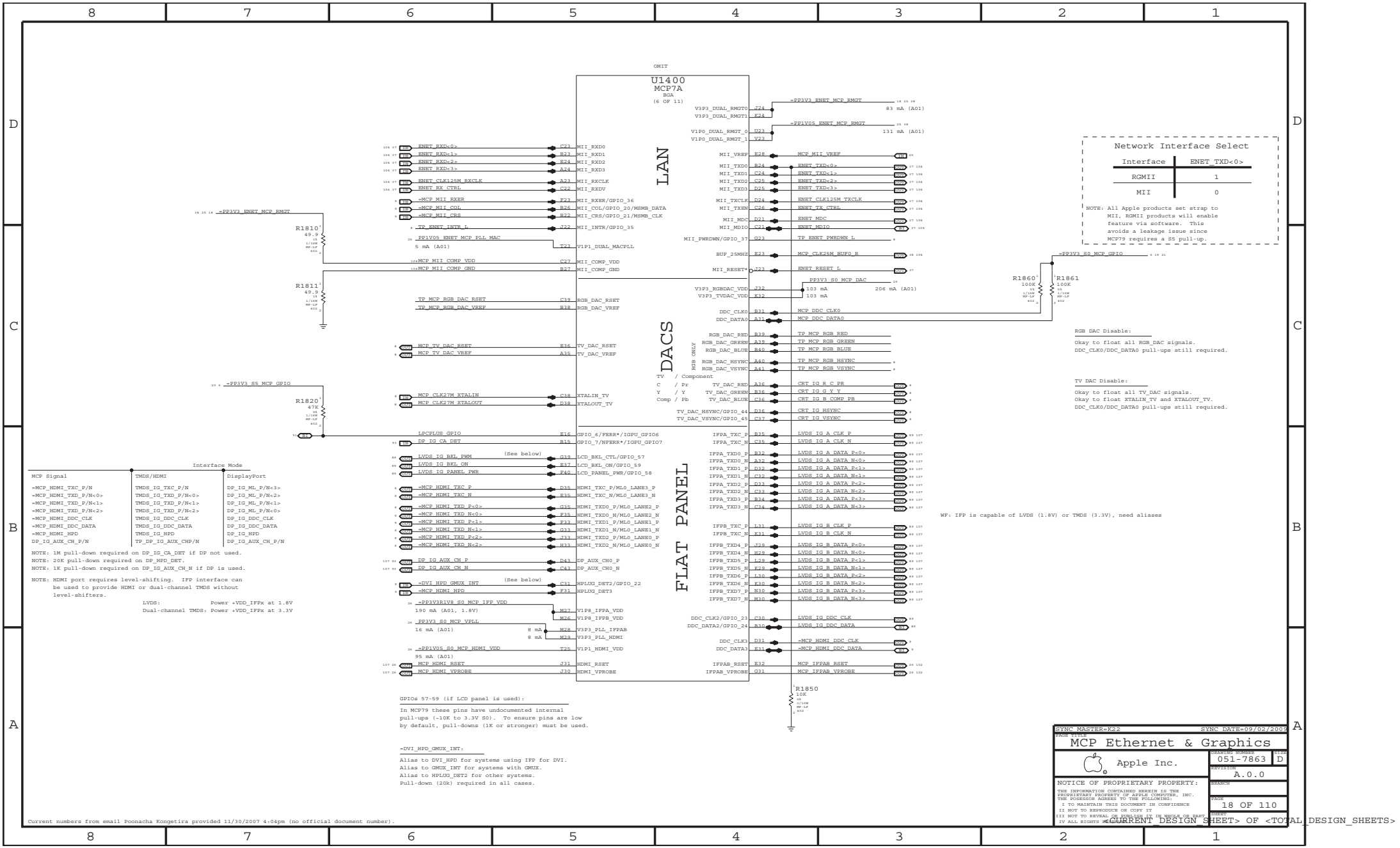
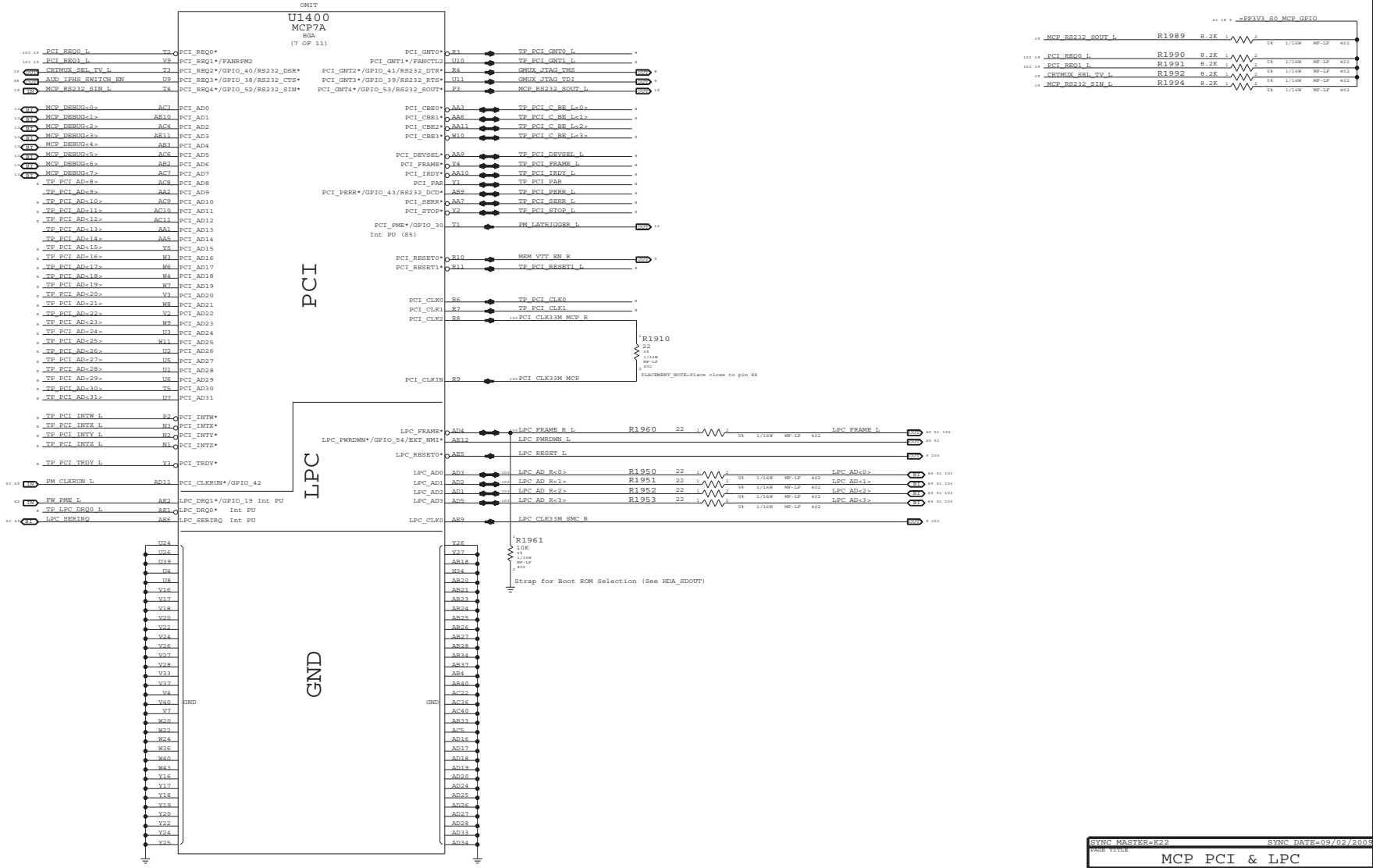
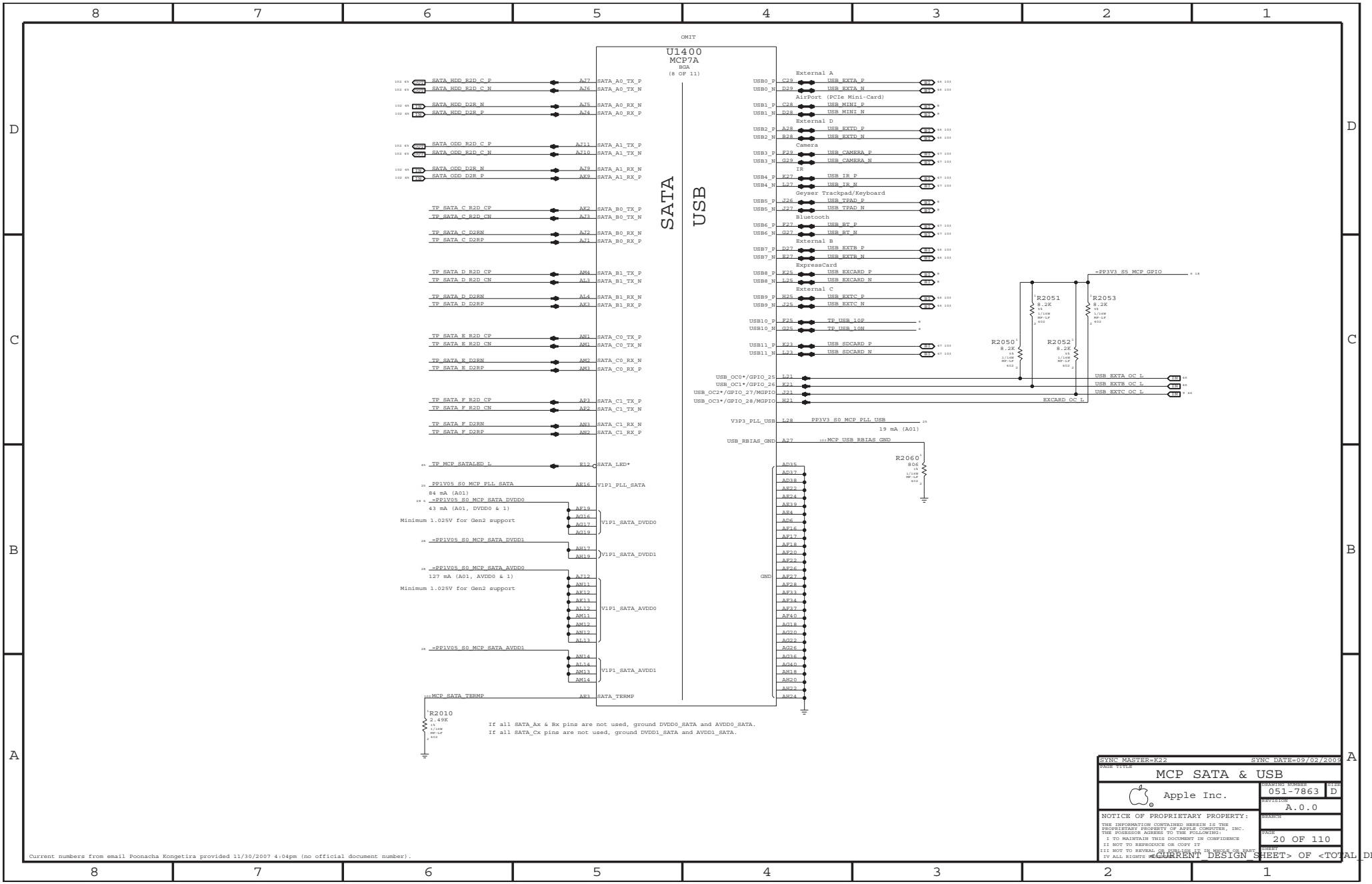
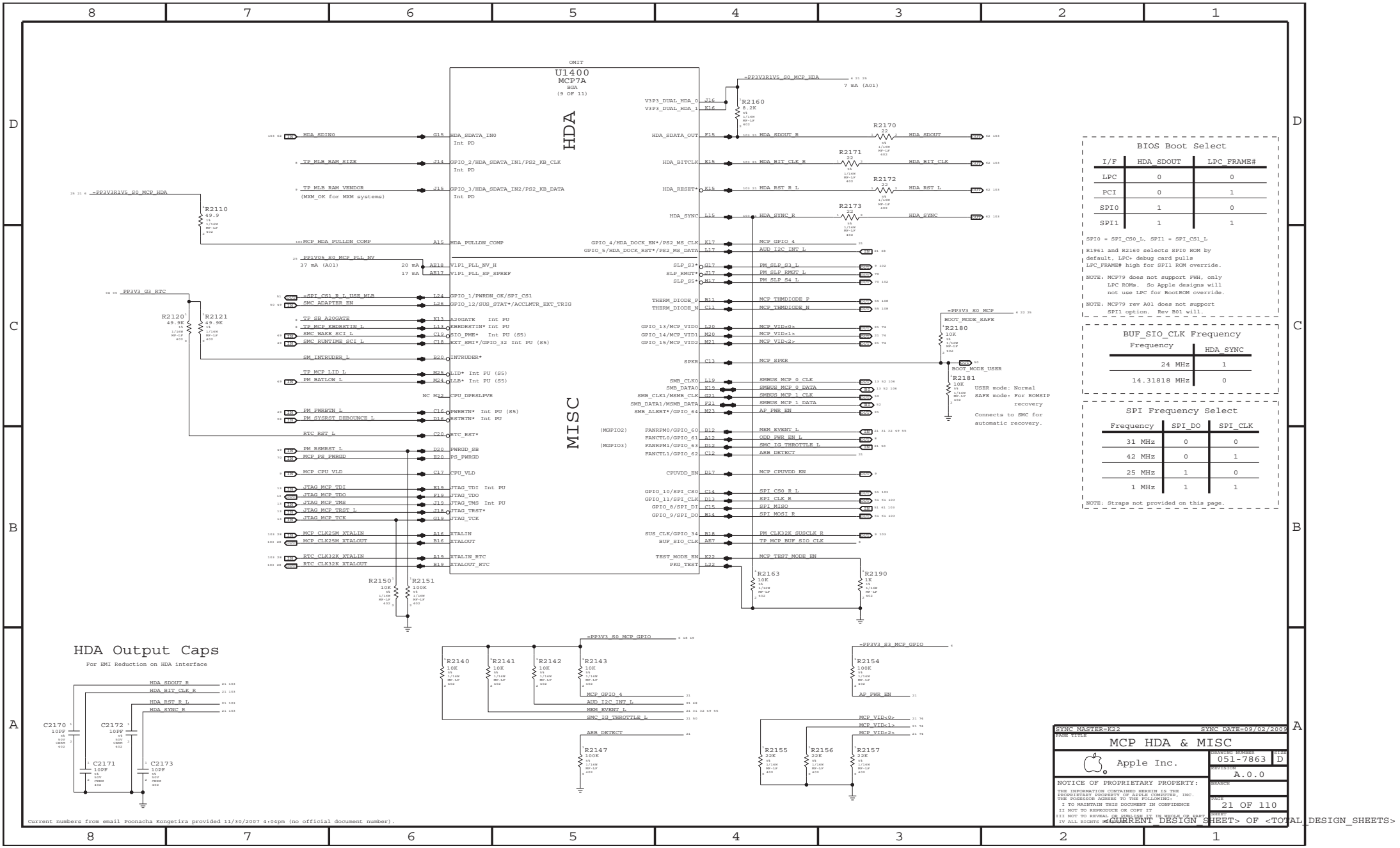
SHEET

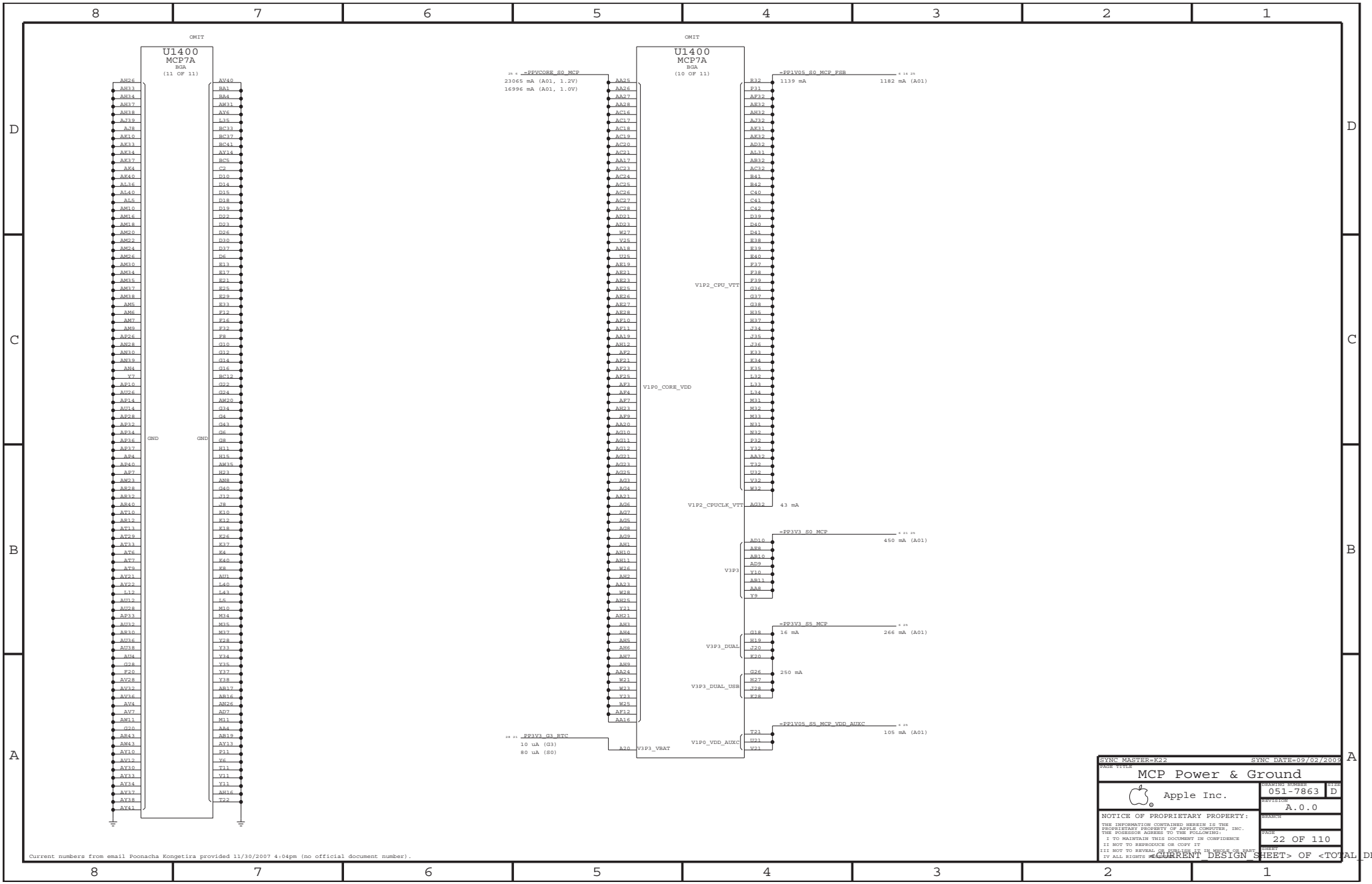
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

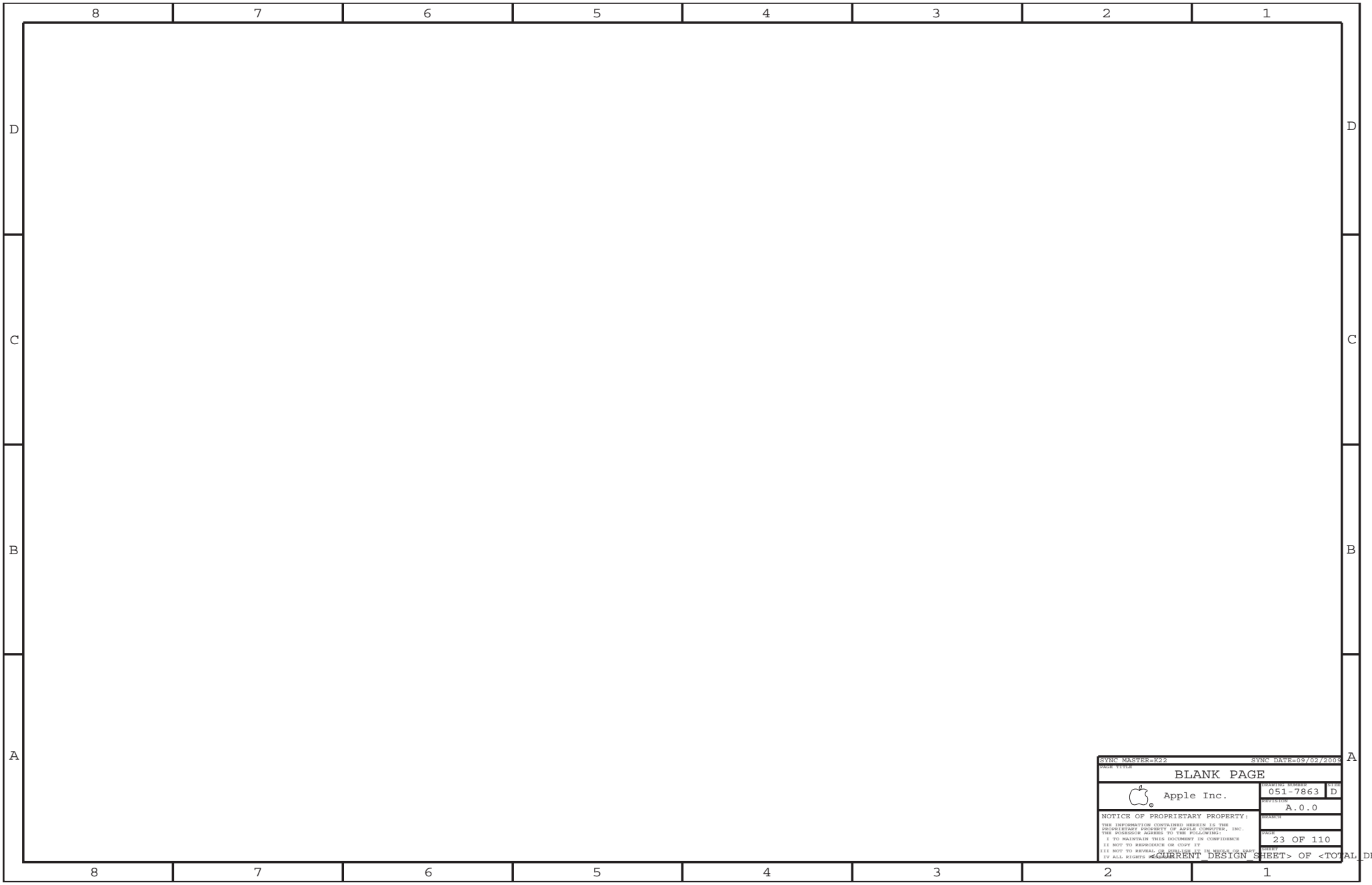


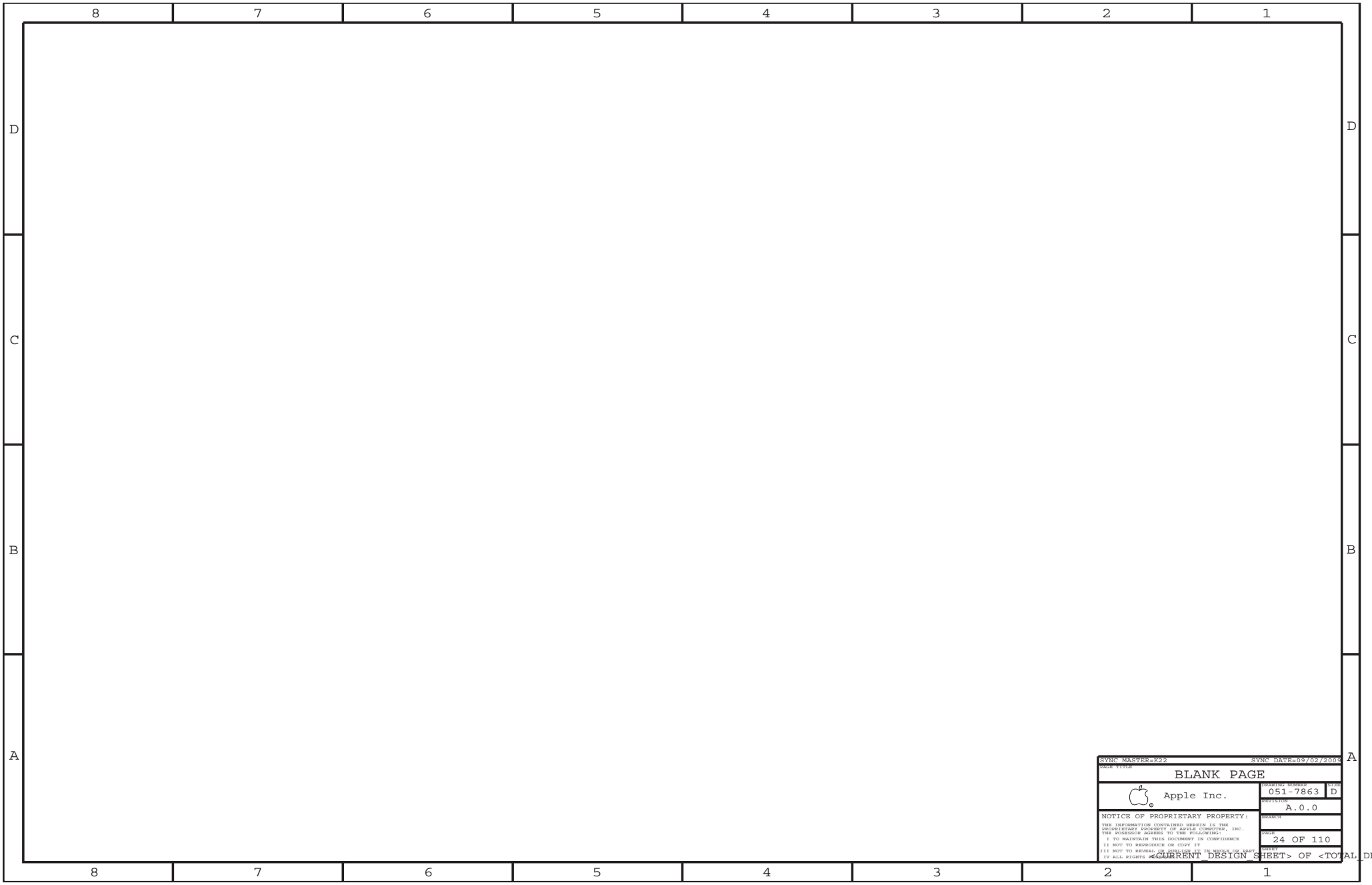


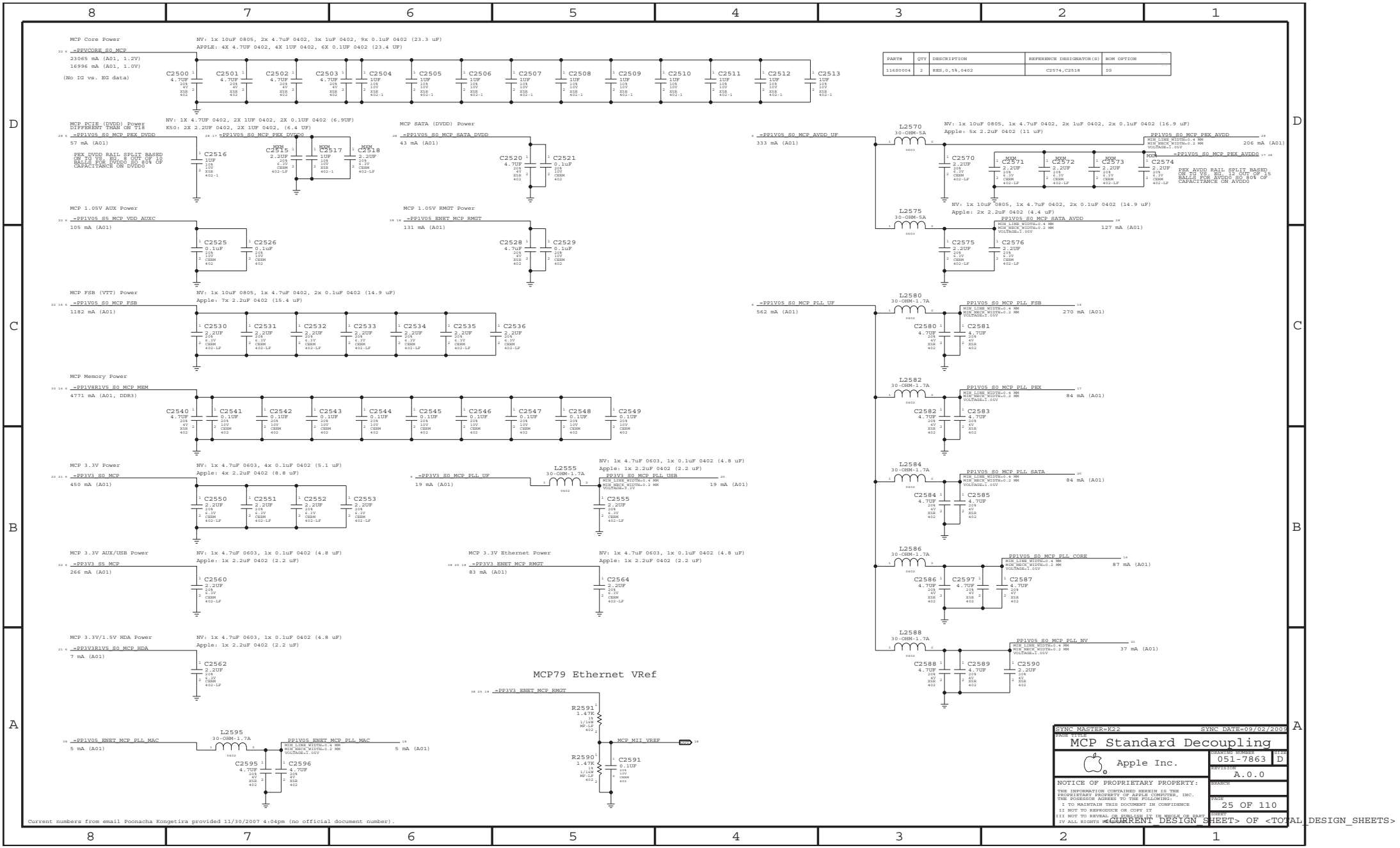






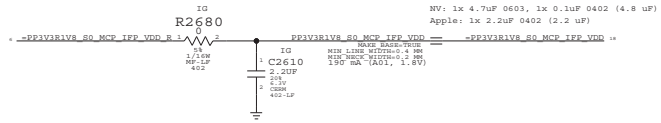




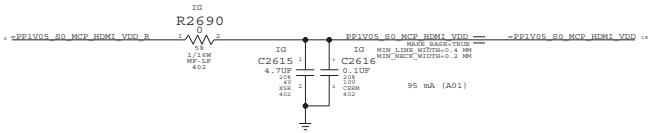


WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



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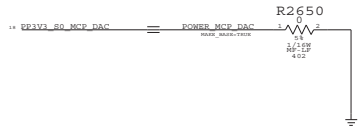
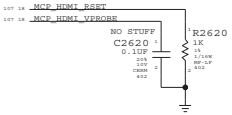
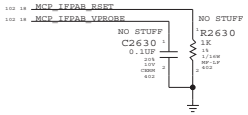
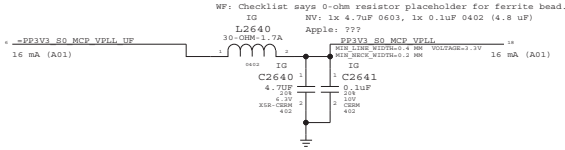






WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

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MCP Graphics Support

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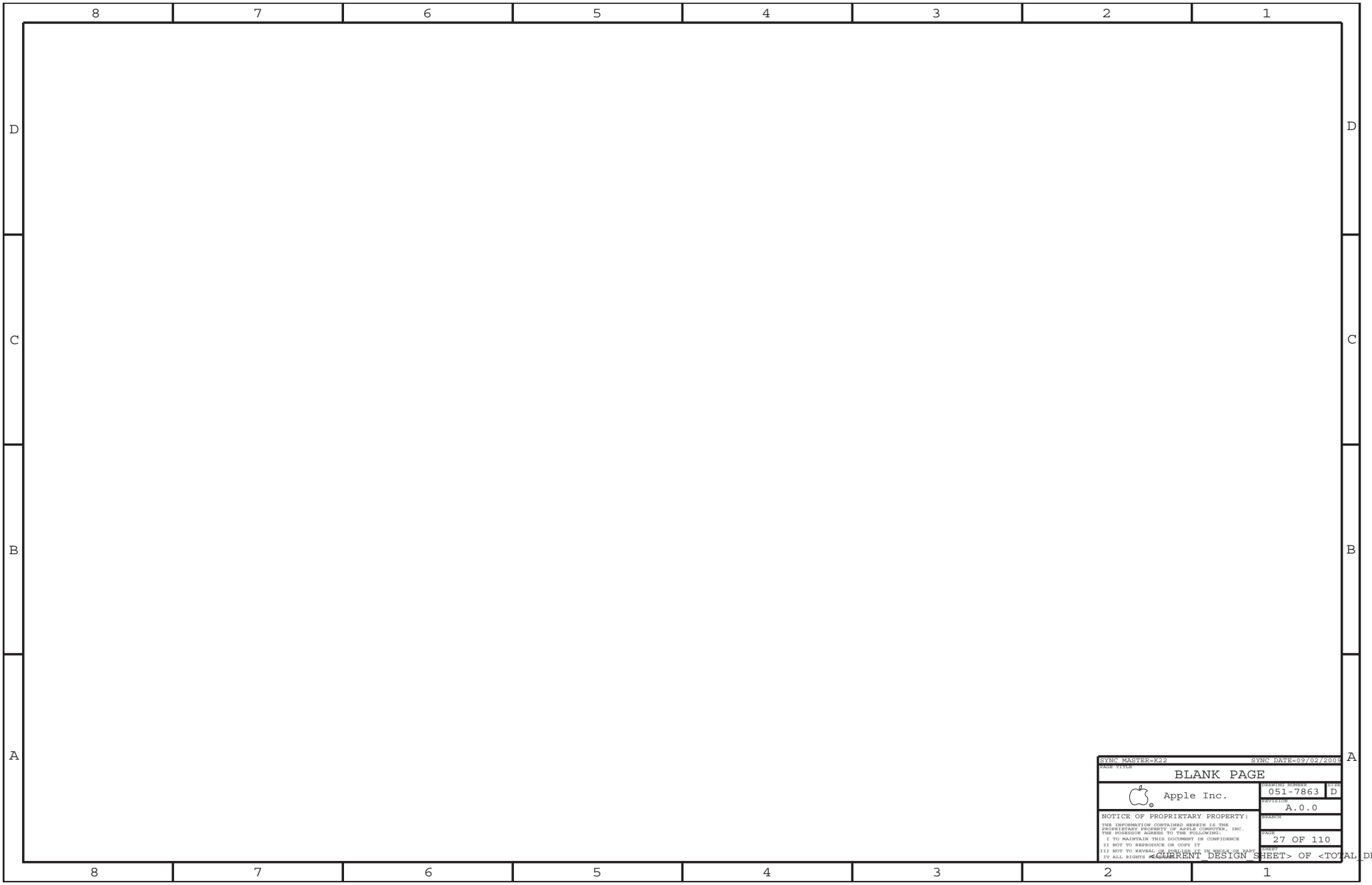
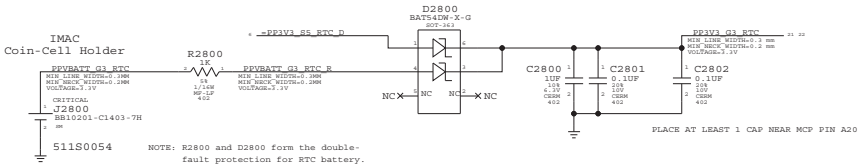
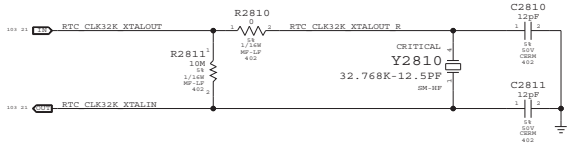
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



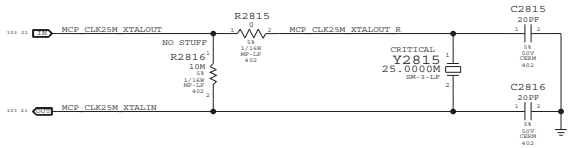
RTC Power Sources



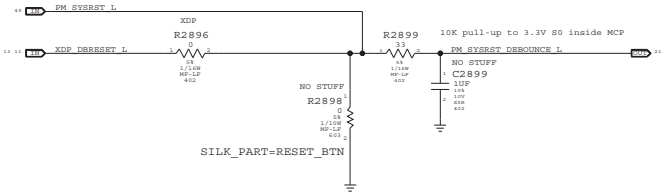
RTC Crystal



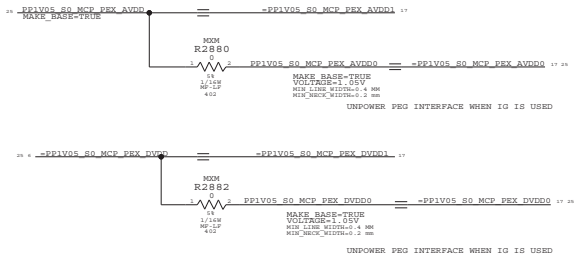
MCP 25MHz Crystal



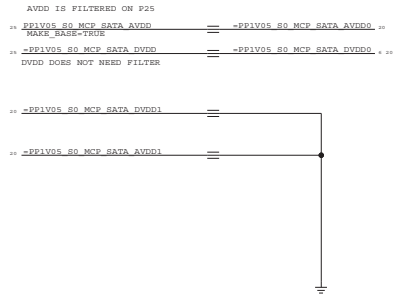
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN



SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

SB Misc

Apple Inc.

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Page Notes

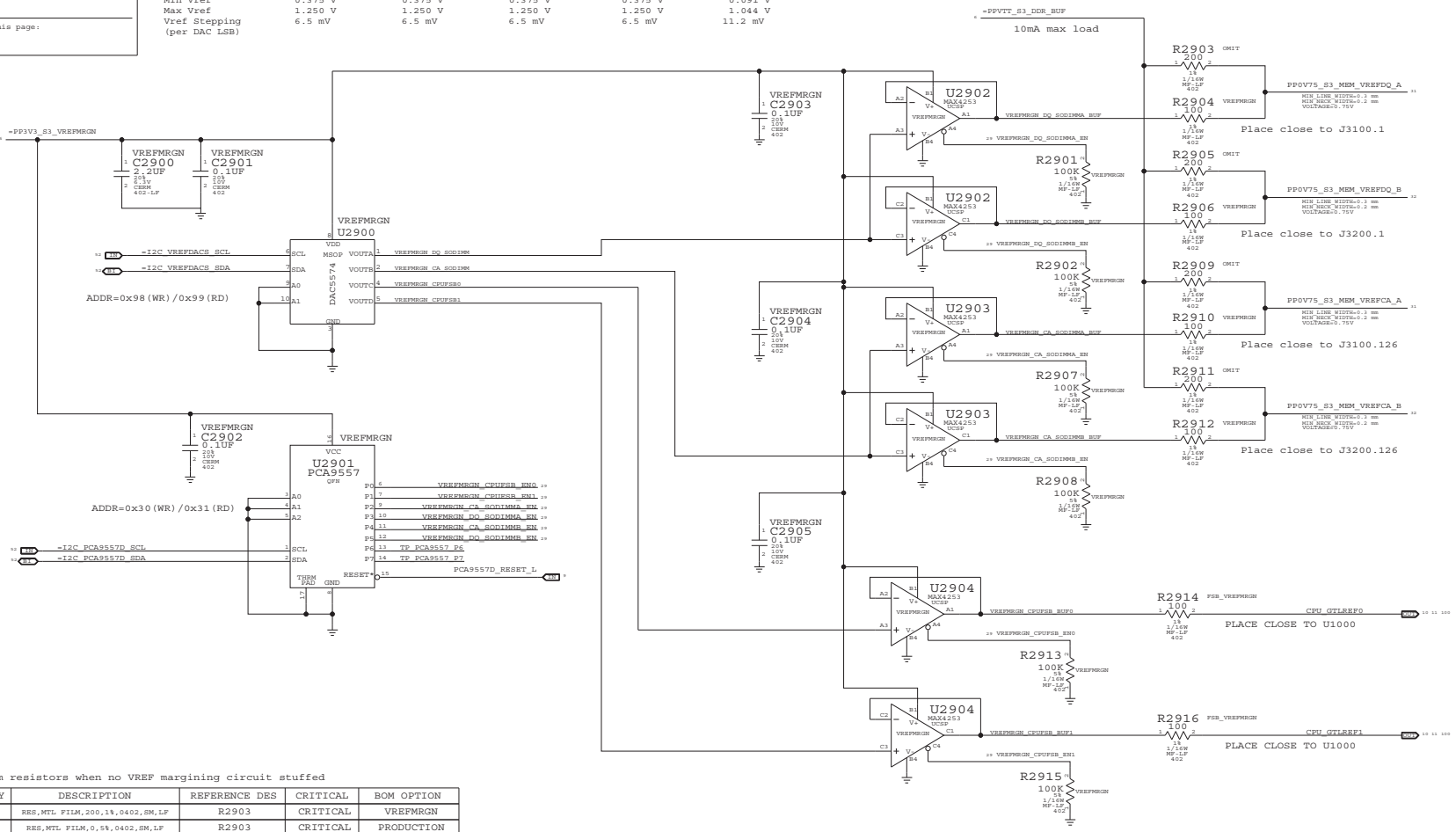
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

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PAGE TITLE
FSB/DDR3 Vref Margining

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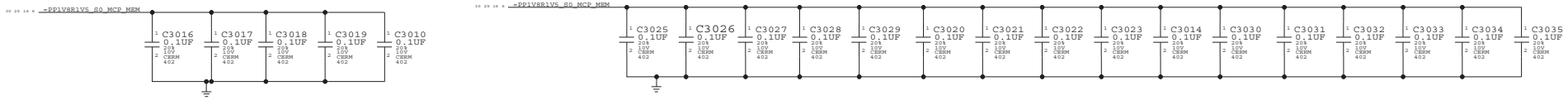
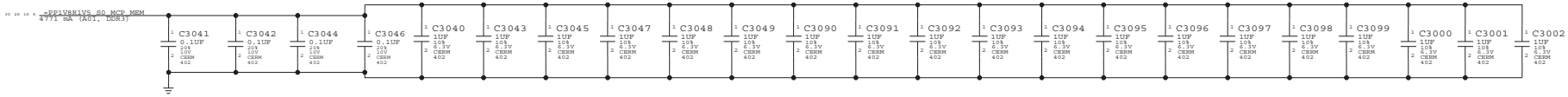
DIMM A (FURTHER FROM MCP)

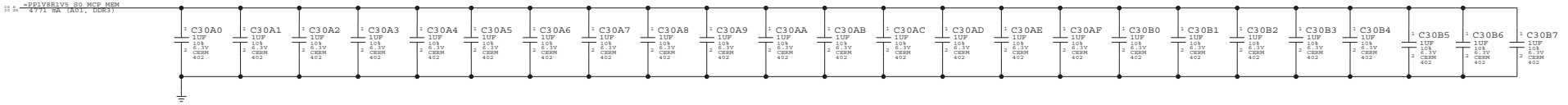
CAPS TO COUPLE MCP 1V5_S0_MEM

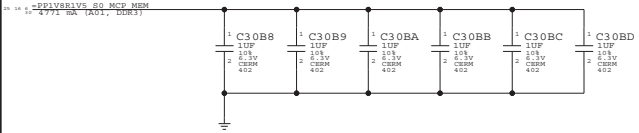
DIMM B (CLOSER TO MCP)



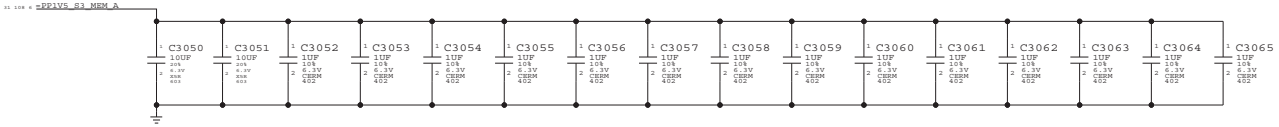
EXTRA DECOUPLING CAPS FOR MCP MEM RAIL



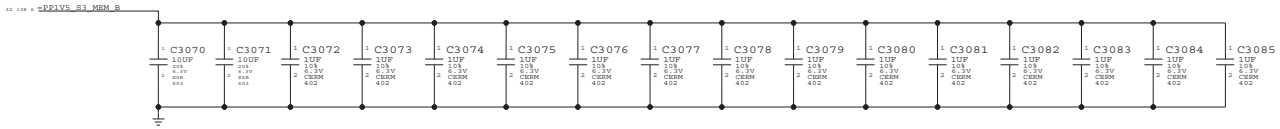




DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR



DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

MEMORY CAPS

Apple Inc.

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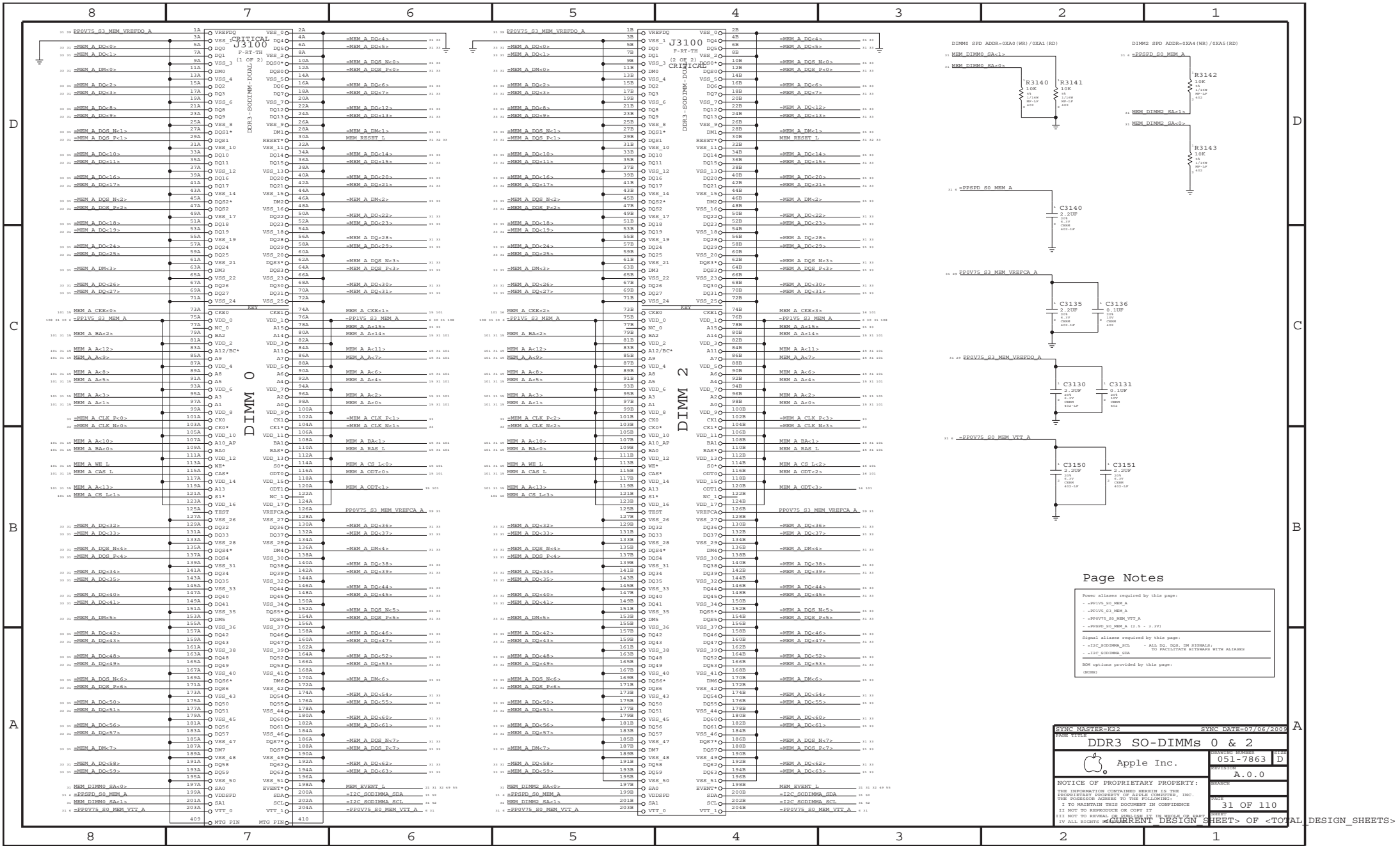

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC MASTER=K22 SYNC DATE=07/06/2009

PAGE TITLE

DDR3 SO-DIMMs 0 & 2

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SHEET

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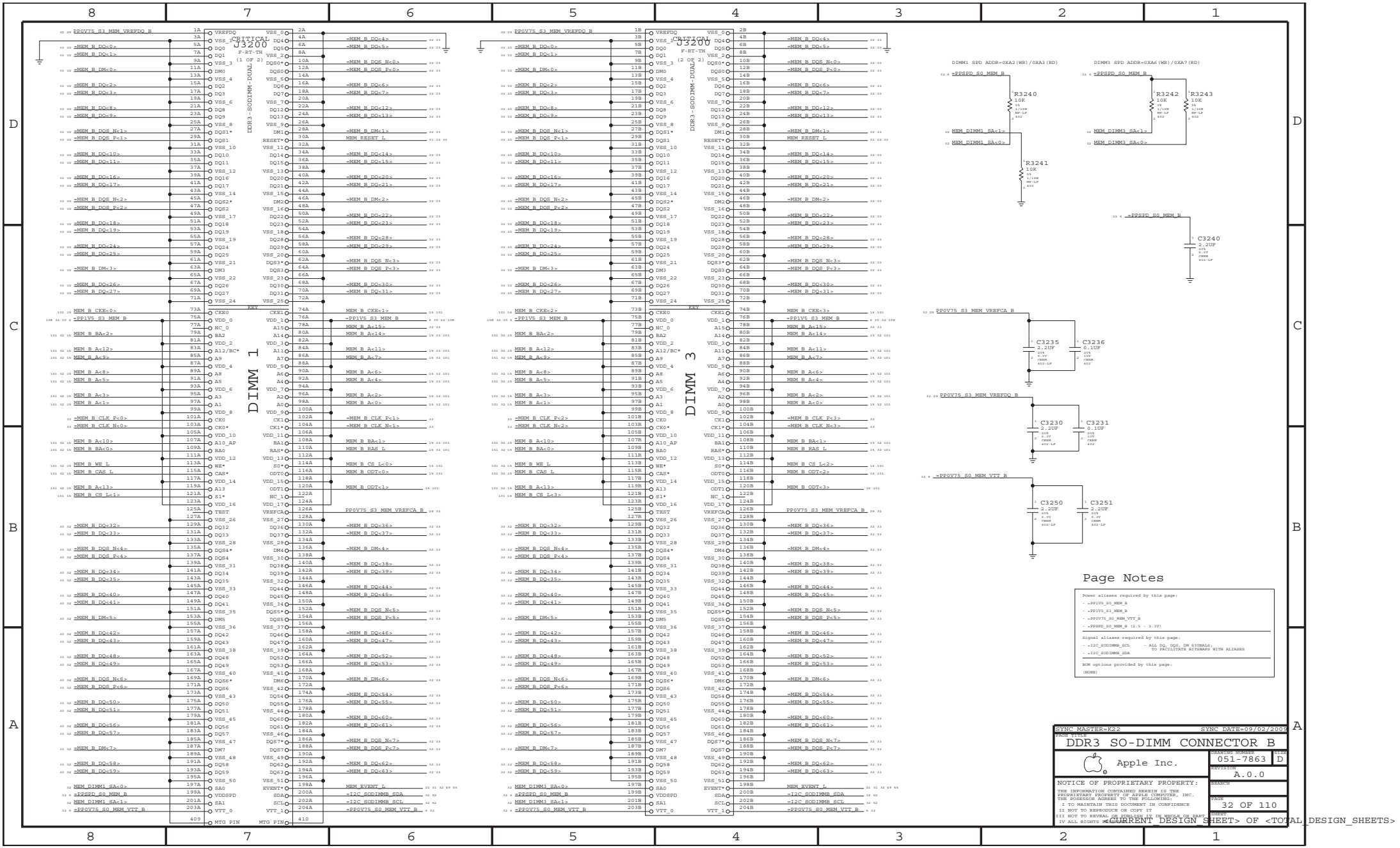

Page Notes

Power aliases required by this page:
- =PP1V5_S3_MEM_R
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM0_SCL
- =I2C_SODIMM0_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B

Apple Inc.

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MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<0>
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<1>
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<2>
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<3>
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>
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MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<4>
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>
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MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<5>
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>
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MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<6>
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<7>
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<0>
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<1>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<0>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<4>

MCP CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<1>
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>

MCP CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<2>
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<3>
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<4>
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<5>
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

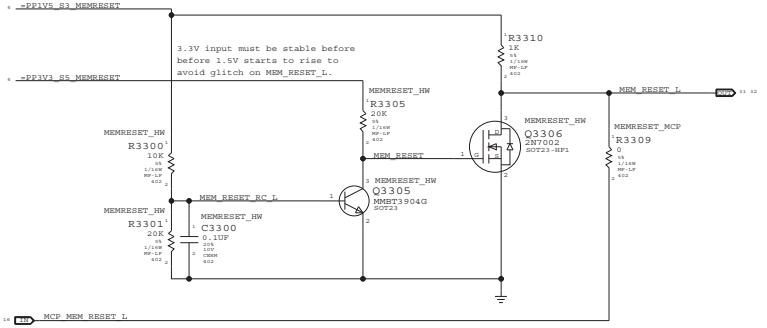
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<6>
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<7>
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



MCP MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<4>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<4>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>

MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<4>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<4>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>

MCP MEMORY TEST POINT ALIASING

TP_MEM_A_A<15>	MAKE_BASE=TRUE	MEM_A_A<15>
TP_MEM_B_A<15>	MAKE_BASE=TRUE	MEM_B_A<15>

SYNC MASTER=MASTER SYNC DATE=N/A

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DDR3 SUPPORT AND BITSWAPS

Apple Inc.

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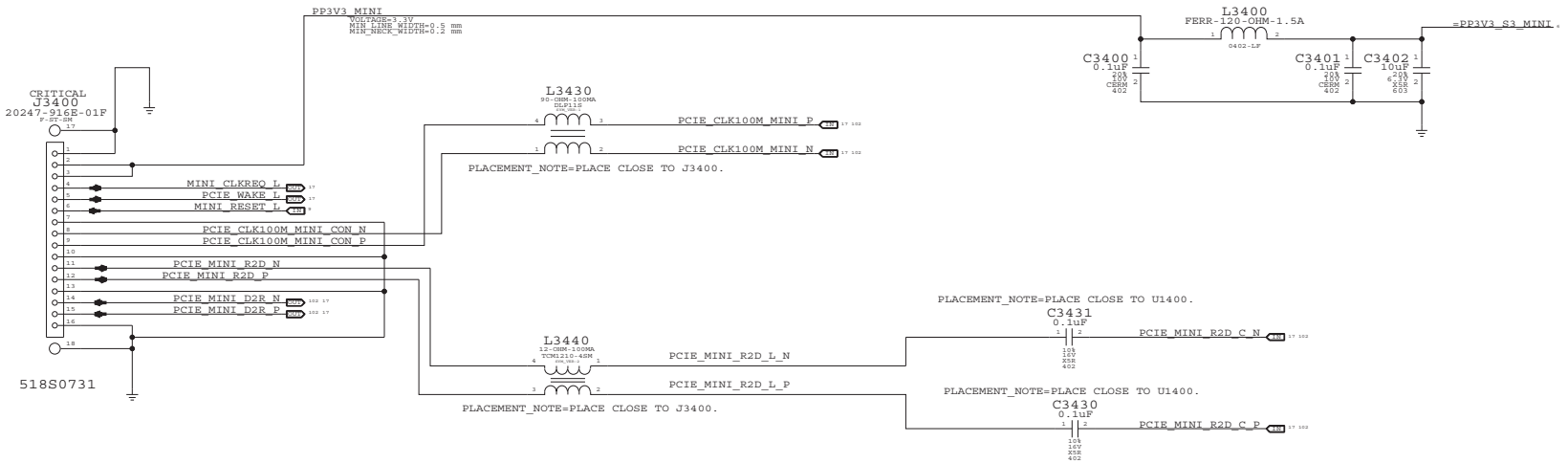

SYNC MASTER=K22 SYNC DATE=05/28/2008

PAGE TITLE
PCI-E Wireless Connector

Apple Inc.

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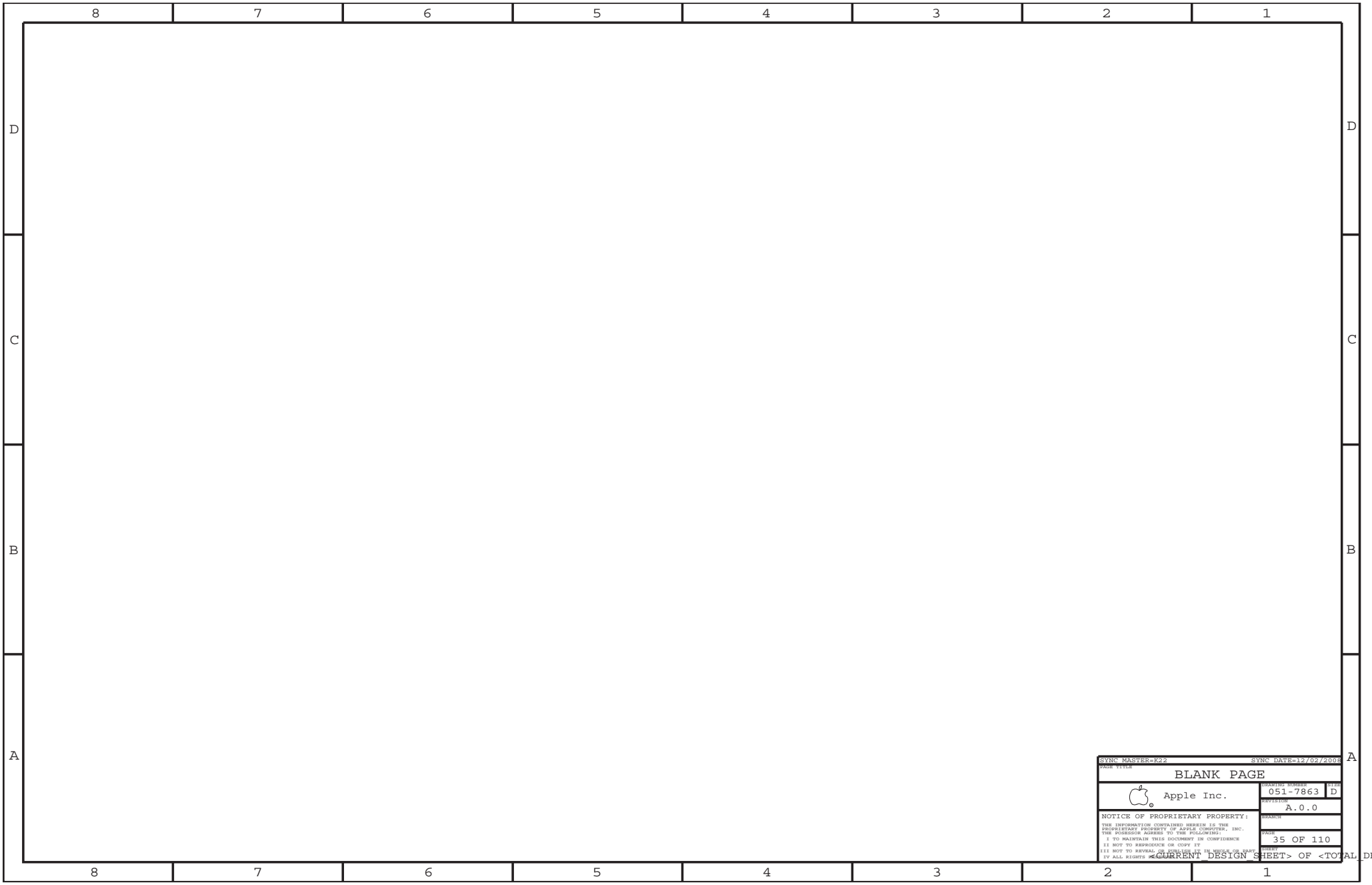
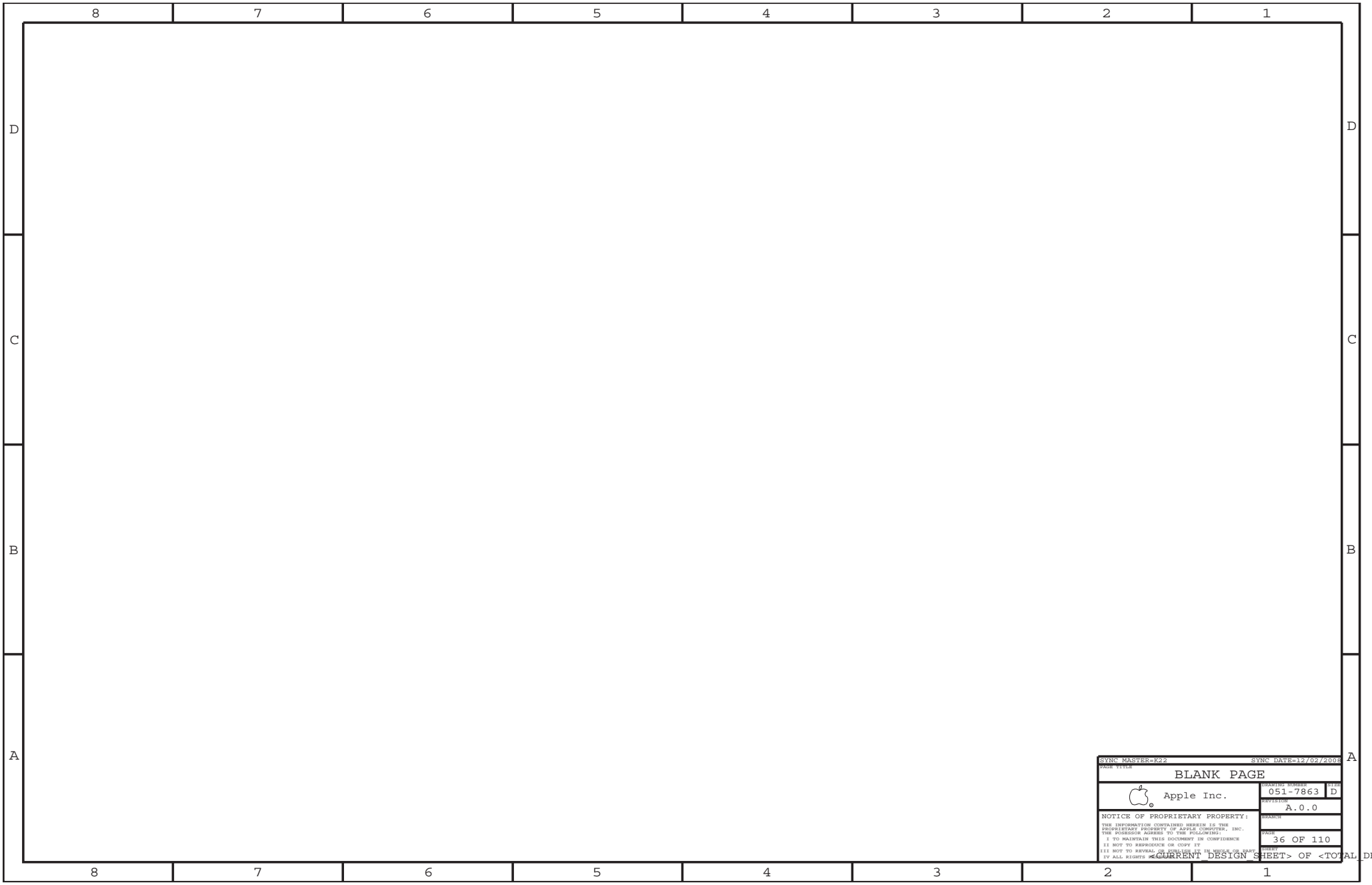
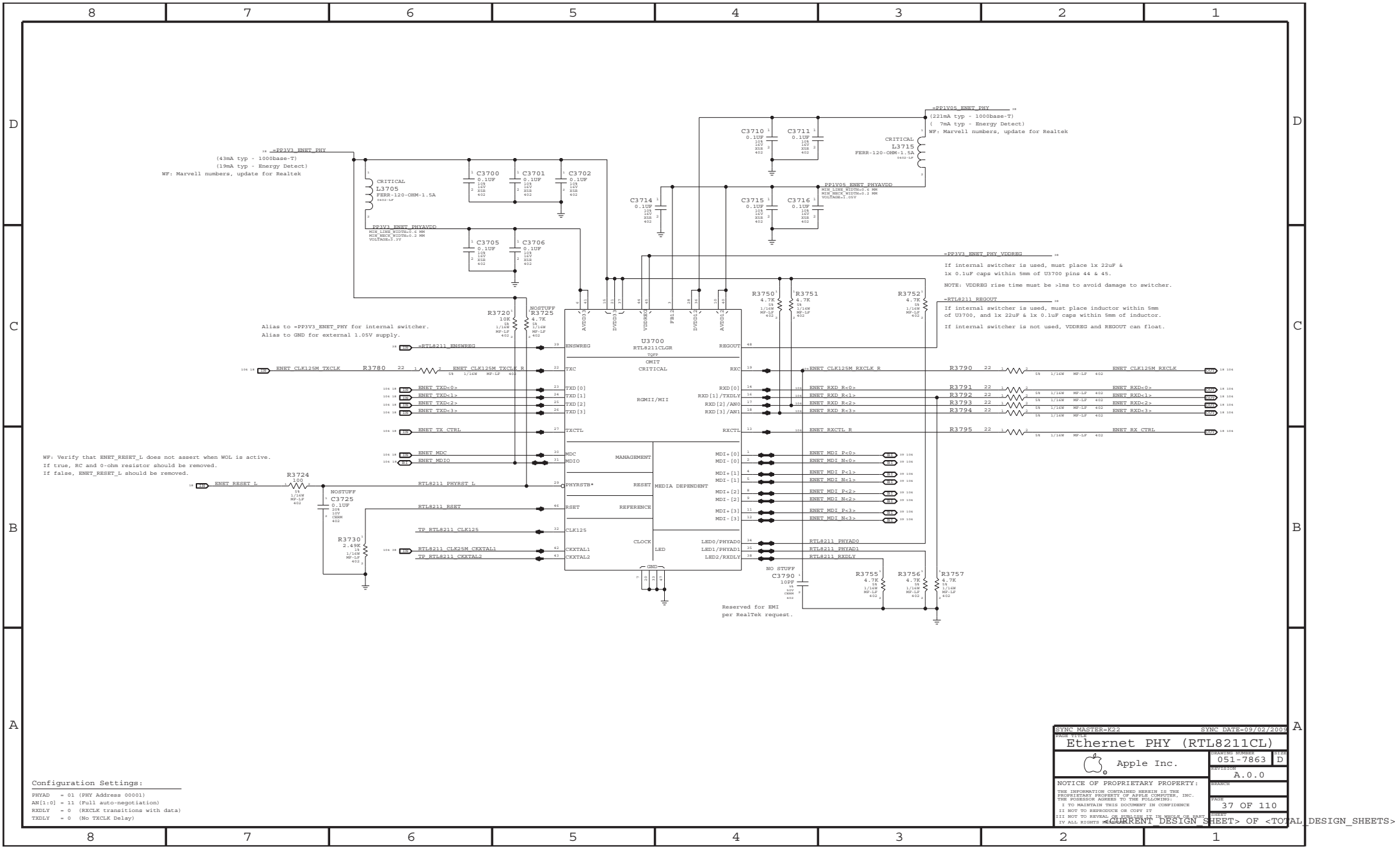
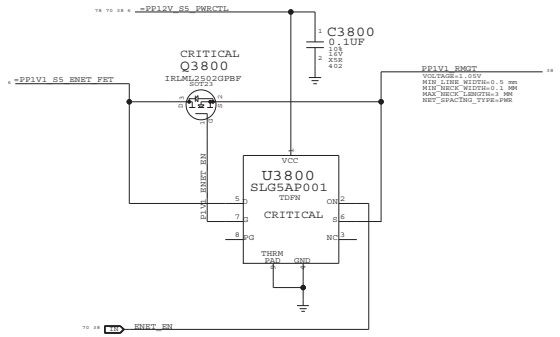


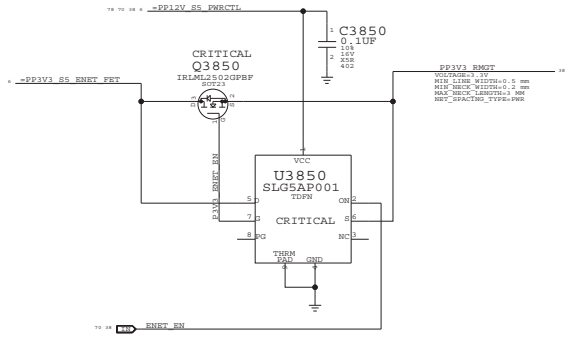




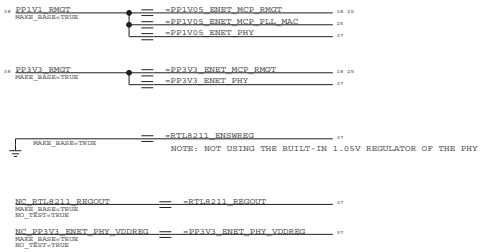
1.1V ENET FET



3.3V ENET FET

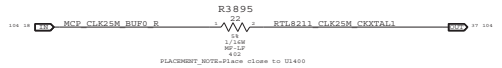


ENET ALIASES



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC MASTER=K22 SYNC DATE=09/02/2008

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Ethernet Support

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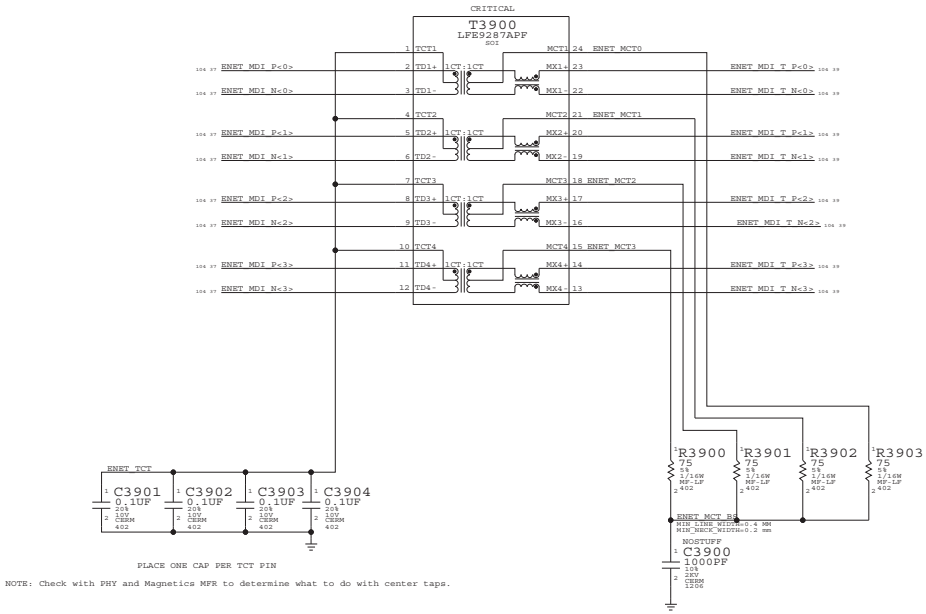

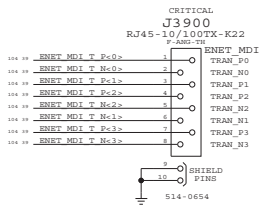

SYNC MASTER=MASTER SYNC DATE=N/A

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ETHERNET CONNECTOR

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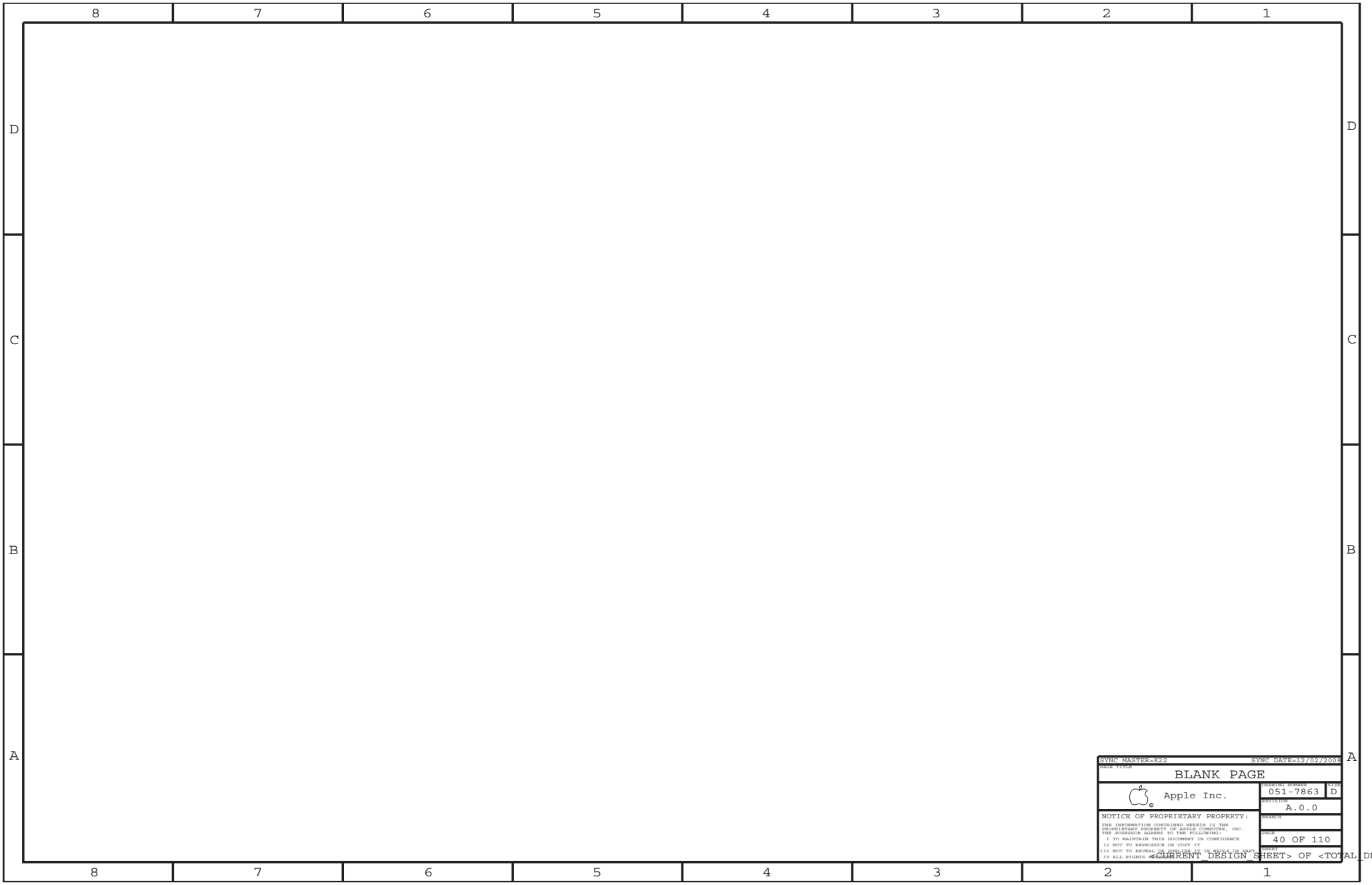
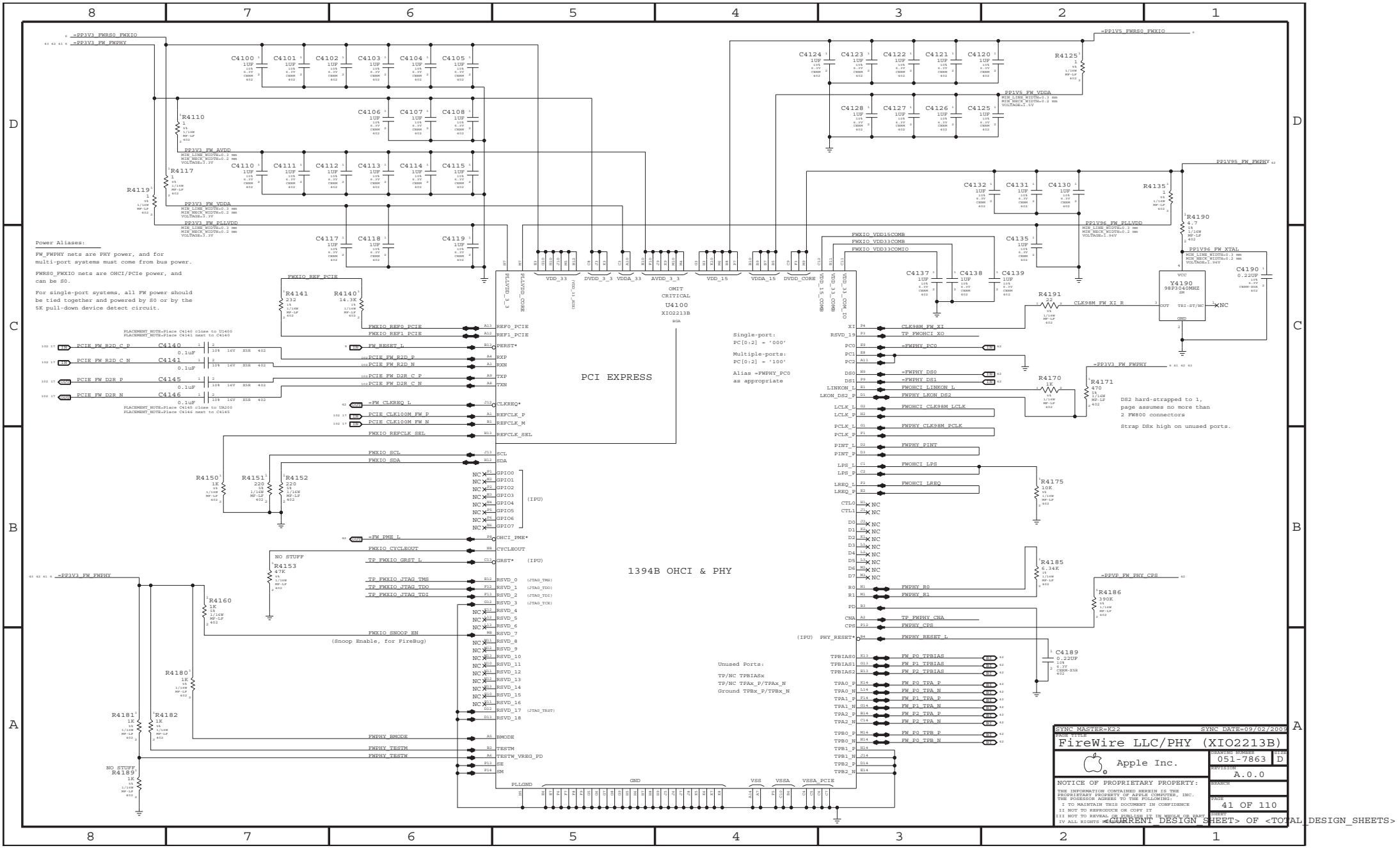
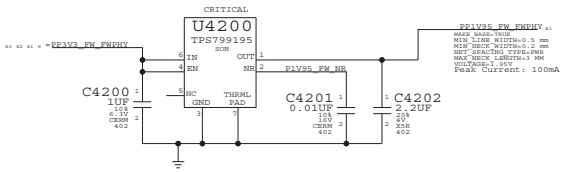
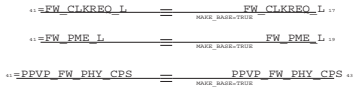




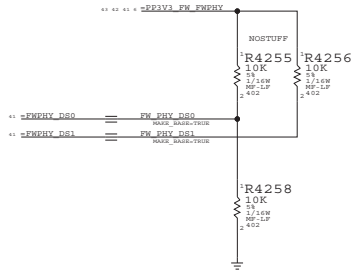
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



1394 PHY STRAPPING OPTIONS

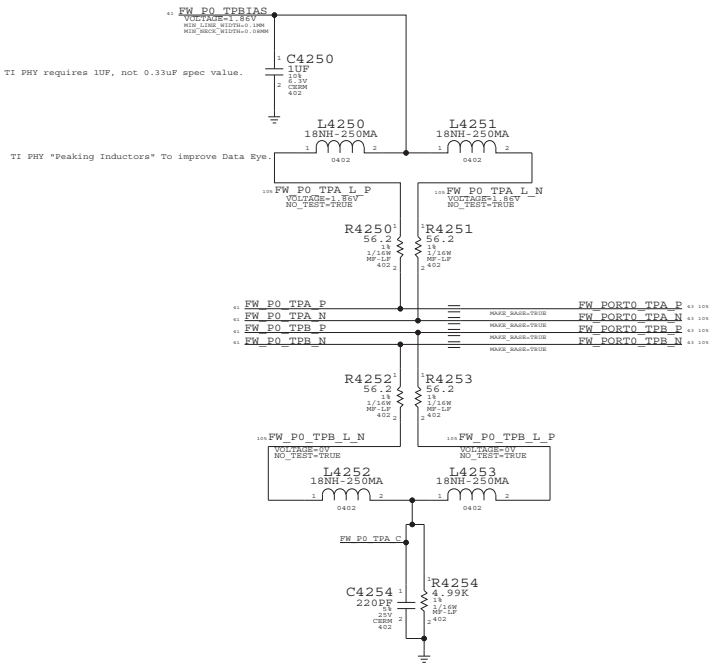


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

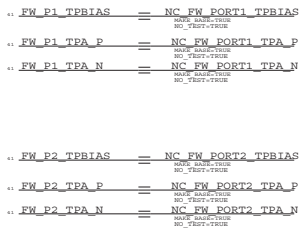
iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED



SYNC MASTER=K22 SYNC DATE=09/02/2008

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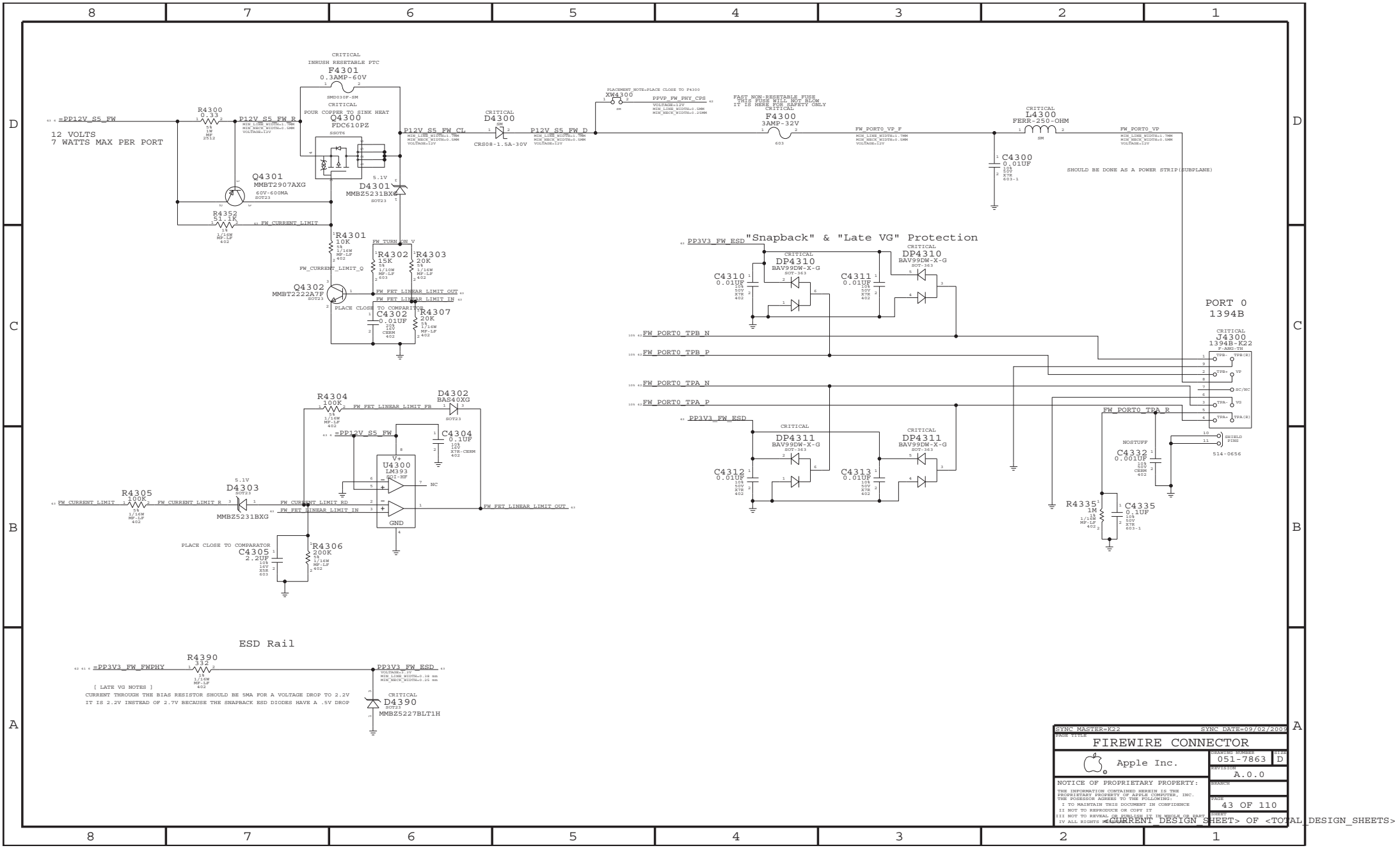
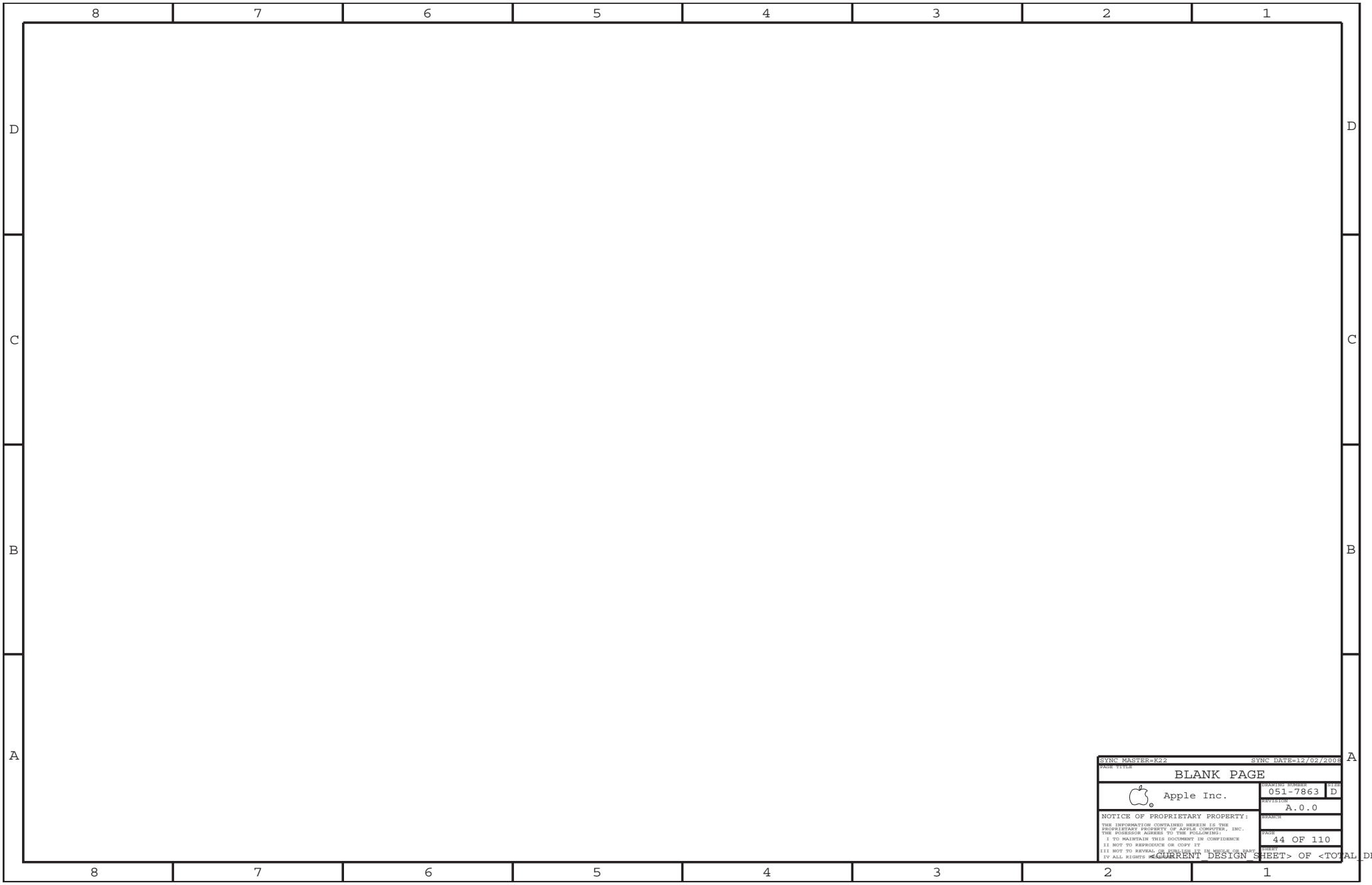
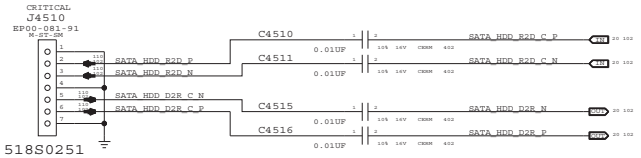


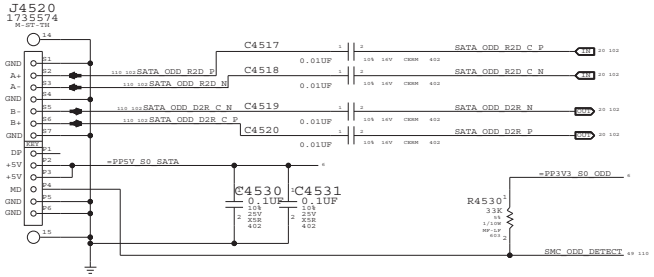


SATA PORT A0 FOR HDD

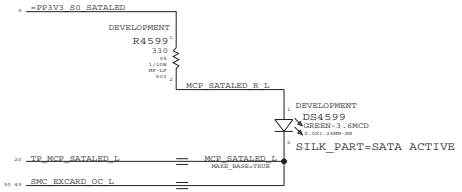


518-0361

SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



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SATA Connectors

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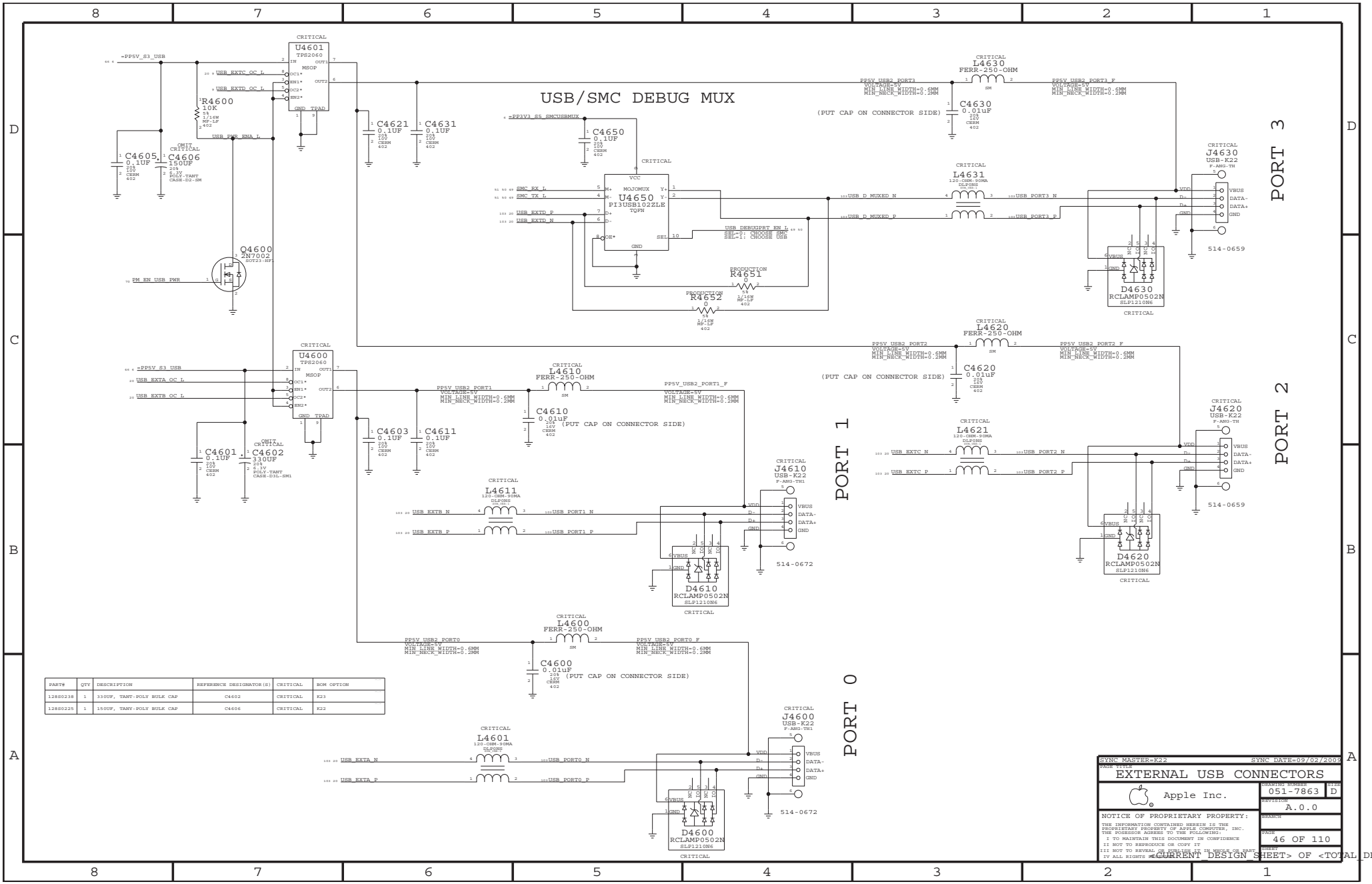

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0238	1	330UF, TANT-POLY BULK CAP	C4602	CRITICAL	K23
128S0225	1	150UF, TANT-POLY BULK CAP	C4606	CRITICAL	K22

SYNC MASTER=K22 SYNC DATE=09/02/2008

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EXTERNAL USB CONNECTORS

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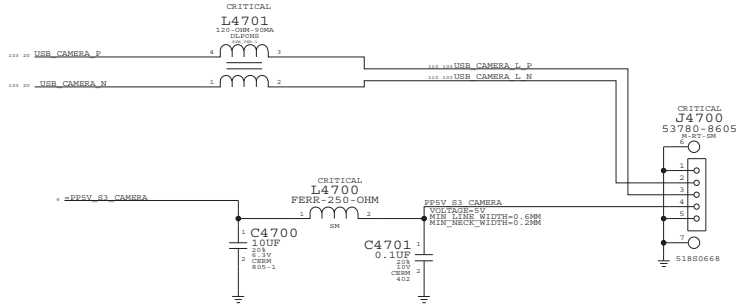
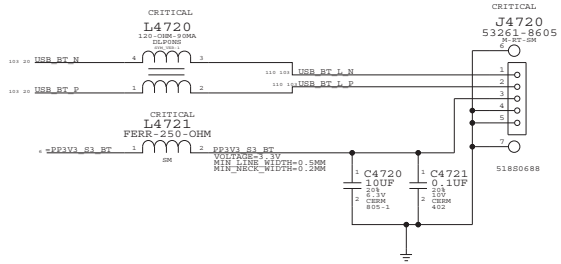
CAMERA CONNECTOR & FILTER

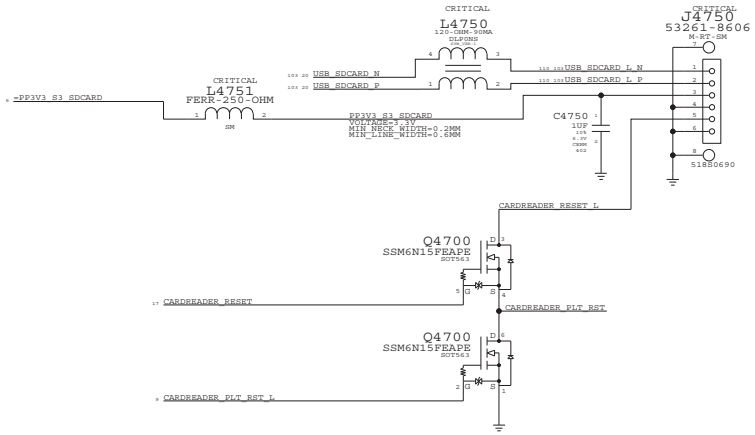


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

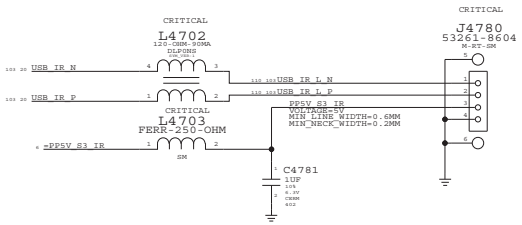
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



IR RECEIVER CONNECTOR



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
Internal USB Connections

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

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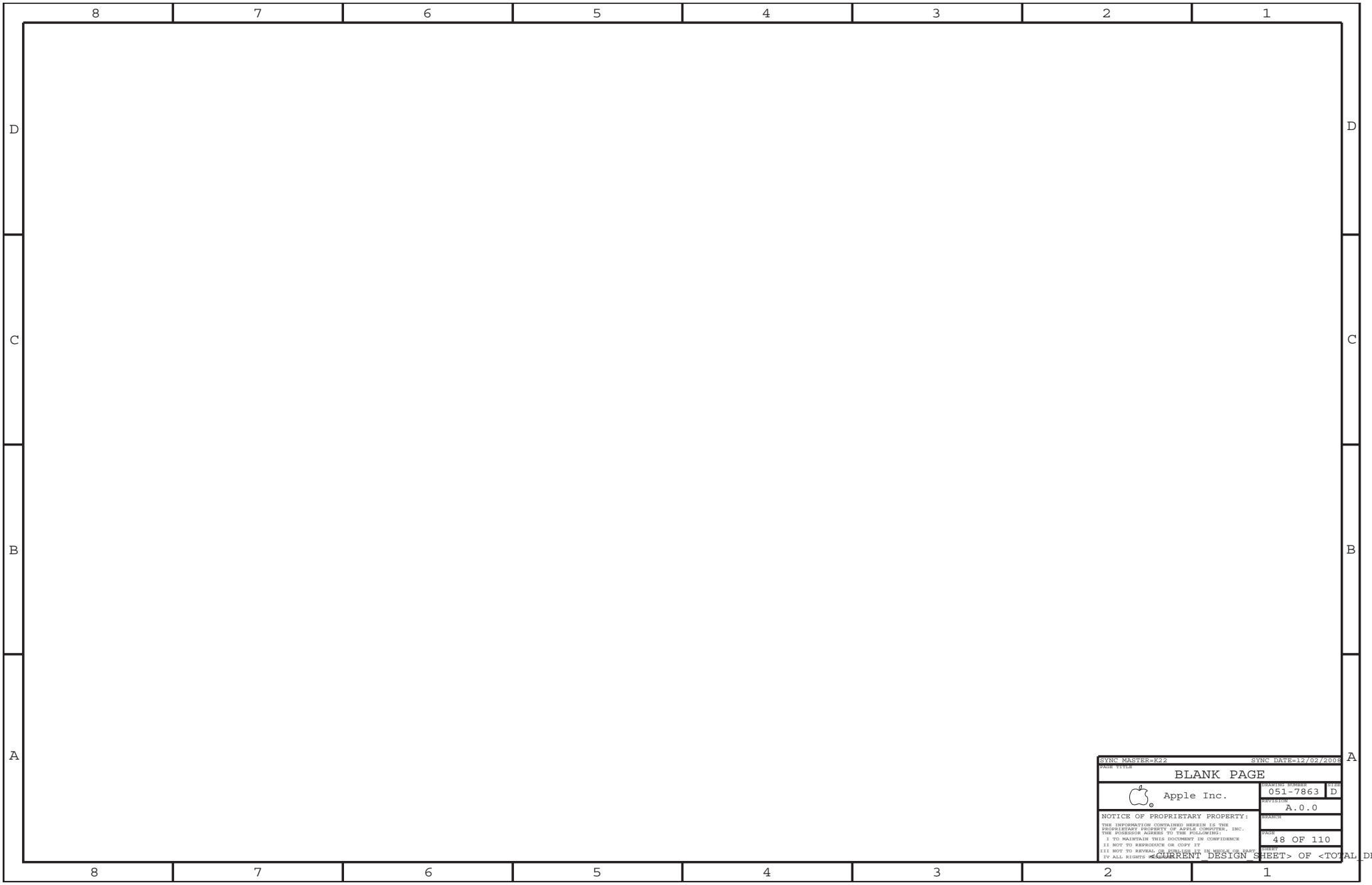
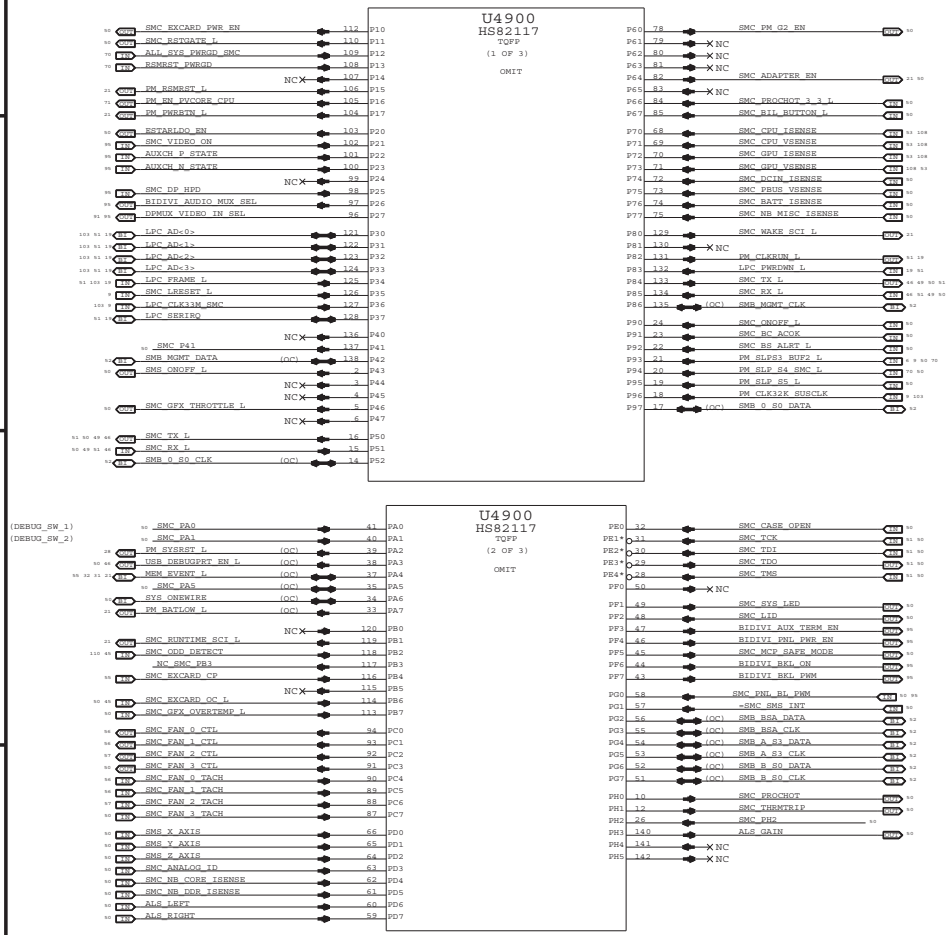
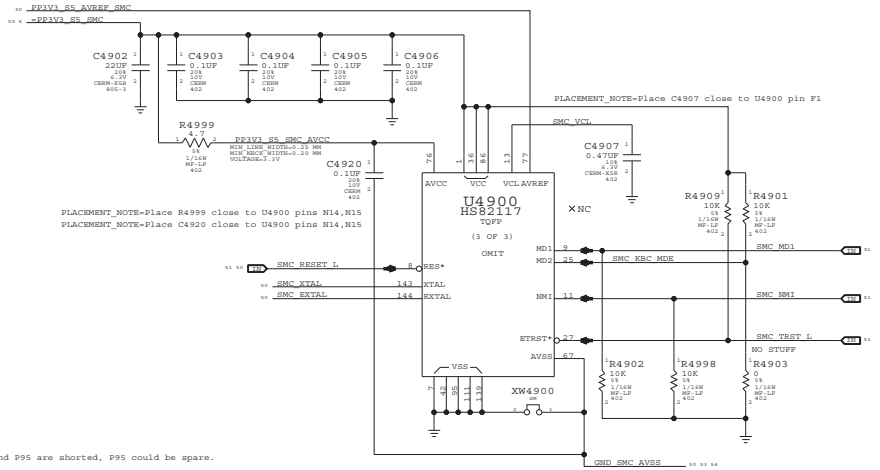


NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=MARKVIDEO SYNC DATE=03/12/2008

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SMC

Apple Inc.

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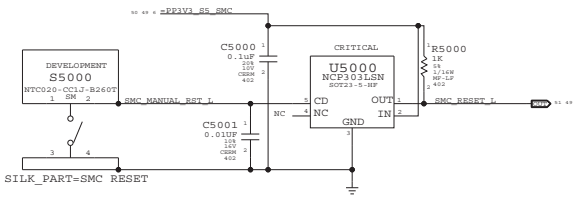
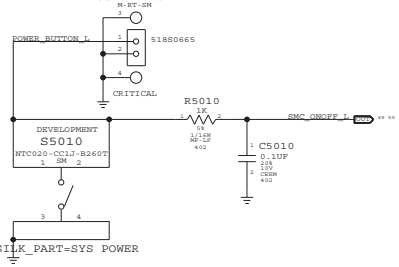
SHEET

SMC Reset Button / Brownout Detect

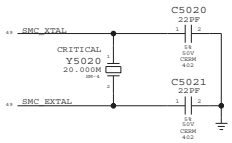


POWER BUTTON

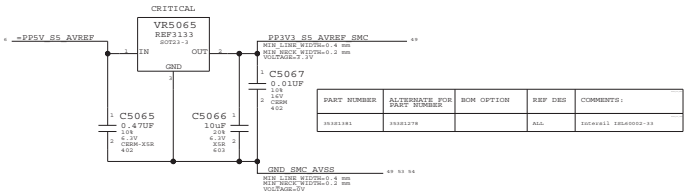
SILK_PART=PWR BTN



SMC Crystal Circuit



SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL6302-33

UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

SMS_Z_AXIS	NC_SMS_Z_AXIS	NO_TEST=TRUE
ALS_LEFT	NC_ALS_LEFT	NO_TEST=TRUE
ALS_RIGHT	NC_ALS_RIGHT	NO_TEST=TRUE
SMC_ANALOG_ID	NC_SMC_ANALOG_ID	NO_TEST=TRUE

UNUSED TP/NC ALIASES

ALS_GAIN	NC_ALS_GAIN	NO_TEST=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	
SMS_ONOFF_L	TP_SMS_ONOFF_L	
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	
SMC_PA1	TP_SMC_PA1	
RSTARLDO_EN	TP_RSTARLDO_EN	

ANALOG SENSORS

SMC_DCIN_ISENSE	SMC_CPU_INPUT_ISENSE
SMC_PBUS_VSENSE	SMC_CPU_INPUT_VSENSE
SMS_X_AXIS	SMC_1V5_S0_VSENSE
SMS_Y_AXIS	SMC_MCP_CORE_VSENSE
SMC_NB_DDR_ISENSE	SMC_1V5_S0_ISENSE
SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE
SMC_BATT_ISENSE	SMC_UNUSED_ADC_PORT7
SMC_NB_MISC_ISENSE	

R5050 10K 1% 1/16W MF-LF 402

MISC. SIGNAL ALIASES

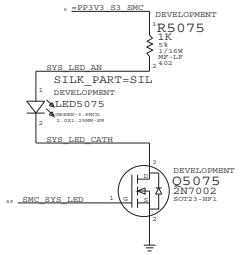
SMC_GFX_OVERTEMP_L	MXM_ALERT_L
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL

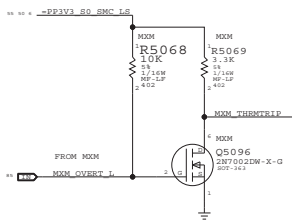
R5020 51 1/16W MF-LF 402 — SMC_IG_THROTTLE_L

R5019 0 1/16W MF-LF 402 — SMC_MCP_SAFE_MODE — MCP_SPKR

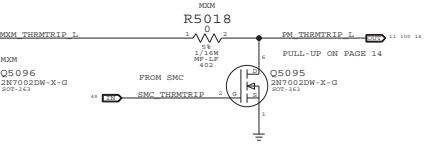
FOR <RDAR://PROBLEM/5925345>

SIL: FOR DEVELOPMENT USE ONLY





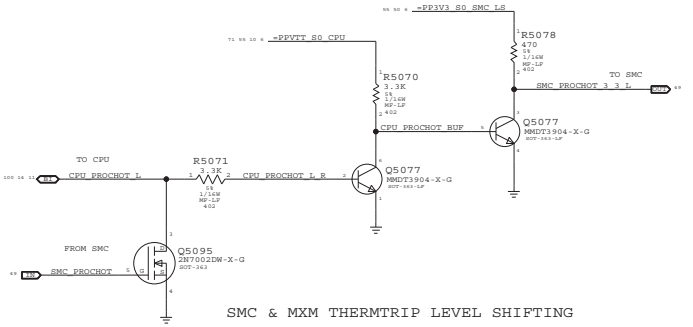
SMC & MXM THERMTRIP LEVEL SHIFTING



SMC_ONOFF_L	R5032 10K
SMC_PWL_BL_PWM	R5033 100K
SMC_PH2	R5034 10K
SMC_TX_L	R5035 10K
SMC_RX_L	R5036 100K
SYS_ONEWIRE	R5037 2.0K
SMC_BS_ALRT_L	R5038 100K
SMC_TMS	R5039 10K
SMC_TDO	R5040 10K
SMC_TDI	R5041 10K
SMC_TCK	R5042 10K
SMC_EXCARD_OC_L	R5043 10K (NO STUFF)
SMC_PA0	R5096 10K
SMC_PA1	R5090 10K
SMC_BIL_BUTTON_L	R5092 10K
SMC_FAN_3_CTL	R5095 100K
SMC_FAN_3_TACH	R5097 100K
SMC_BC_ACOK	R5047 10K
SMC_ADAPTER_EN	R5049 10K
USB_DEBUGPRT_EN_L	R5098 10K
=SMC_SMS_INT — SMC_SMS_INT	R5091 10K
SMC_LID	R5087 10K

SMC_PA5	R5093 10K
SMC_GFX_OVERTEMP_L	R5099 10K
SMC_CASE_OPEN	R5046 10K
PM_SLP83_BUF2_L	R5094 100K
PM_SLP_S4_SMC_L	R5089 100K (PLACEMENT_NOT=PLACE CLOSE TO U4900(SMC))
PM_SLP_S5_L	

SMC PROCHOT 3.3V LEVEL SHIFTING



SYNC MASTER=MARKVIDEO — SYNC DATE=03/12/2008

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-7863 — SIZE: D

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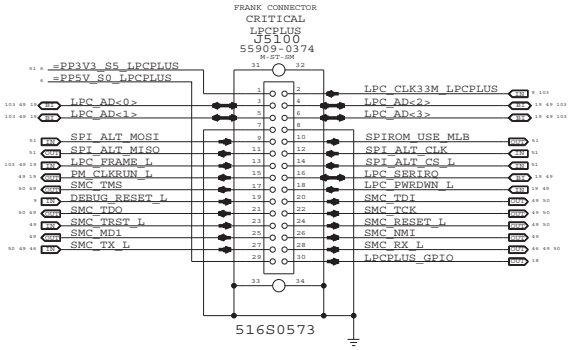
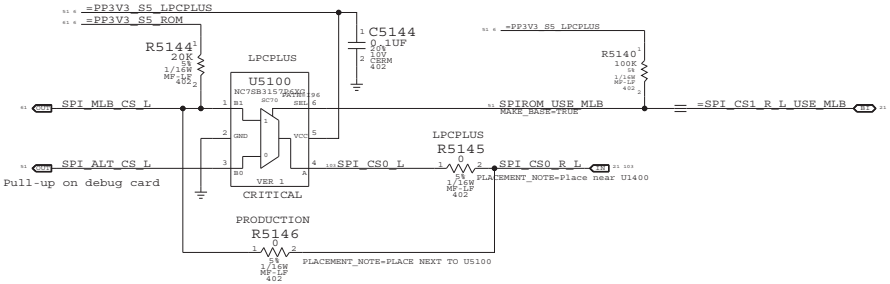
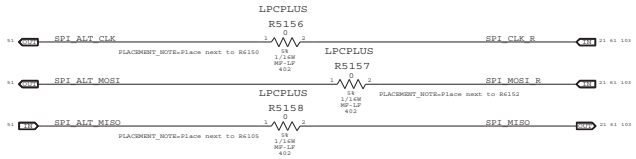
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
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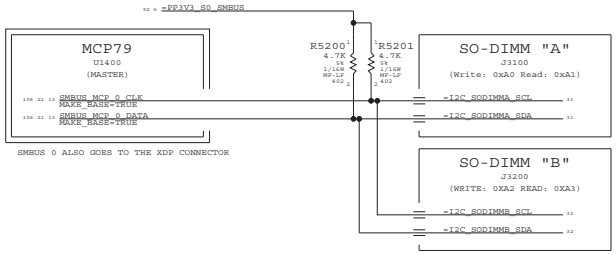
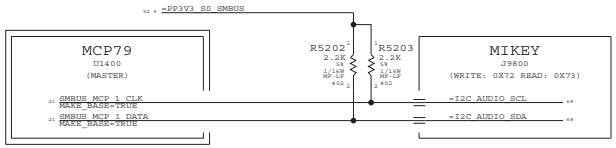
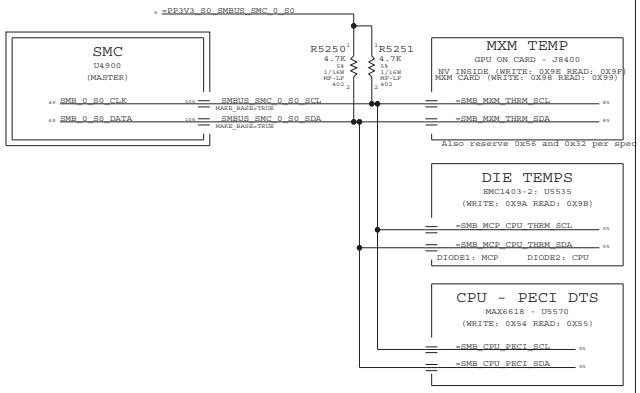
MCP79 SMBUS "0" CONNECTIONS



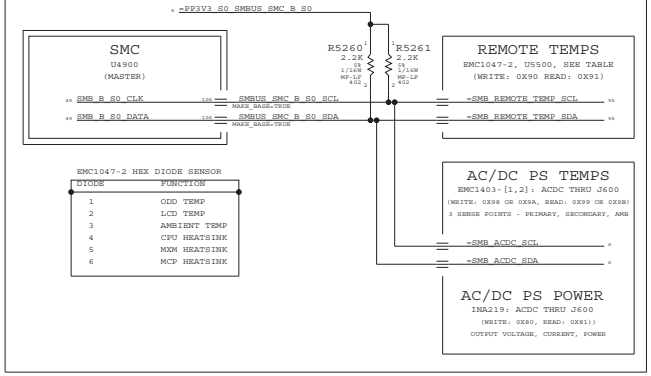
MCP79 SMBUS "1" CONNECTIONS



SMC "0" SMBus Connections

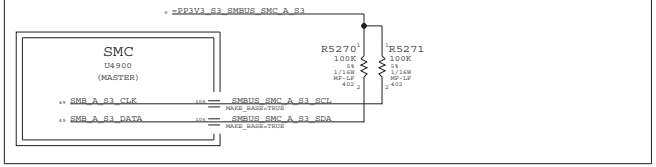


SMC "B" SMBus Connections

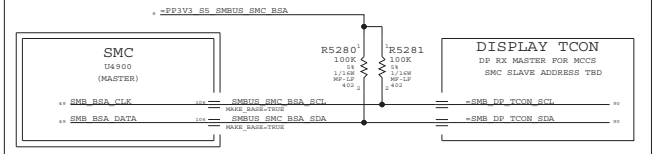


SMC "A" SMBus Connections

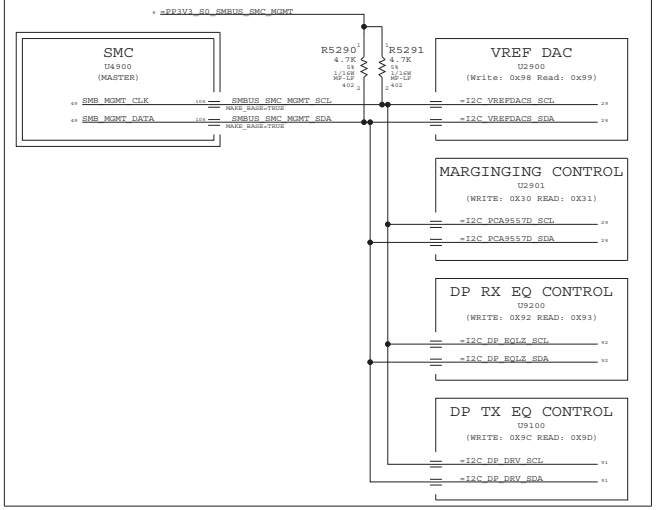
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



POTENTIAL SMC SLAVE SMBUS CONNECTIONS



SMC "MANAGEMENT" SMBUS CONNECTIONS



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

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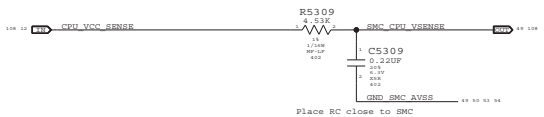
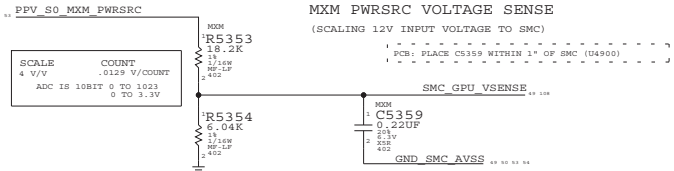
CPU Voltage Sense / Filter

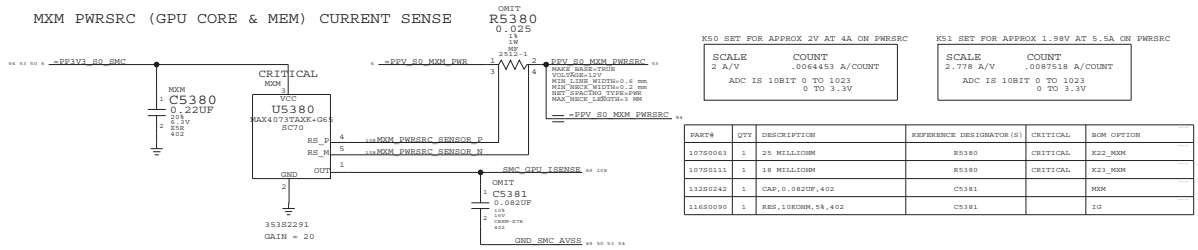


MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023, 0 TO 3.3V

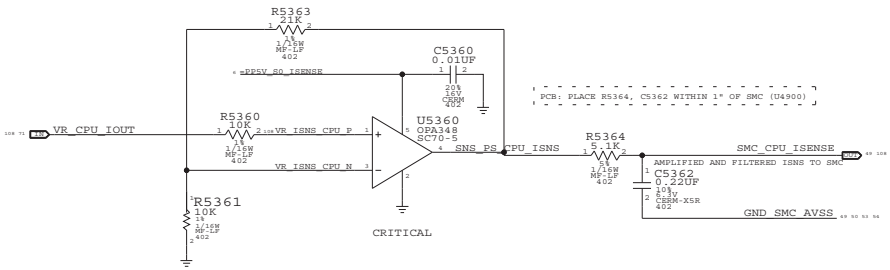
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

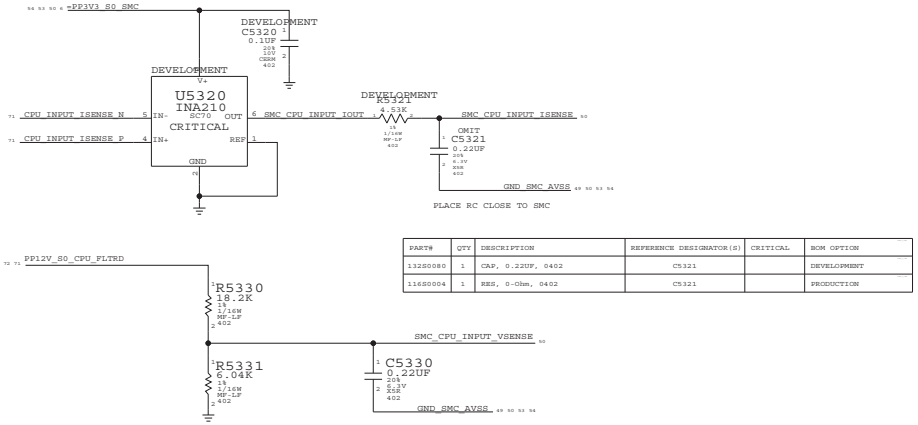
ADC IS 10BIT 0 TO 1023, 0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
1075O063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
1075O111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
1325O242	1	CAP,0.082UF,402	C5381		MXM
116SO090	1	RES,10KOHM,5%,402	C5381		IG

CPU CURRENT SENSE AMP & FILTER



CPU CORE INPUT SIDE CURRENT & VOLTAGE SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5321		DEVELOPMENT
116S0004	1	RES, 0-Ohm, 0402	C5321		PRODUCTION

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE: CPU/MXM CURRENT AND VOLTAGE SENSE

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

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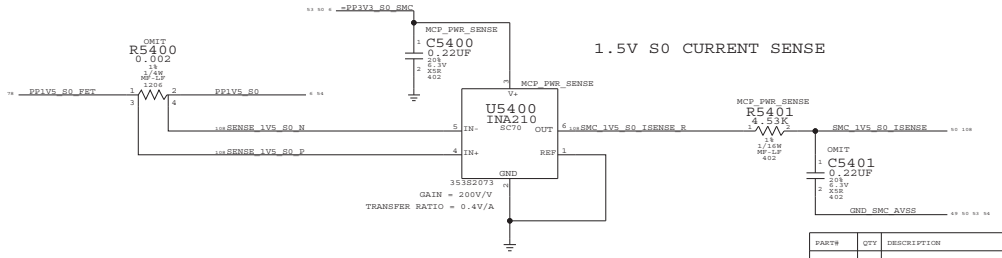
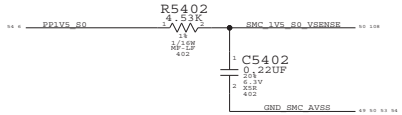
1.5V S0 CURRENT SENSE



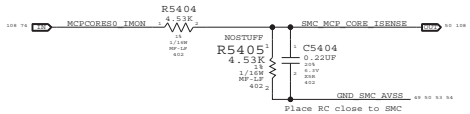
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5401		MCP_PWR_SENSE
116S0004	1	RES, 0 OHM, 0402	C5401		PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

1.5V S0 VOLTAGE SENSE

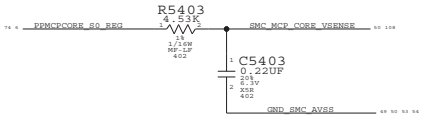


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
MCP CURRENT AND VOLTAGE SENSE

Apple Inc.

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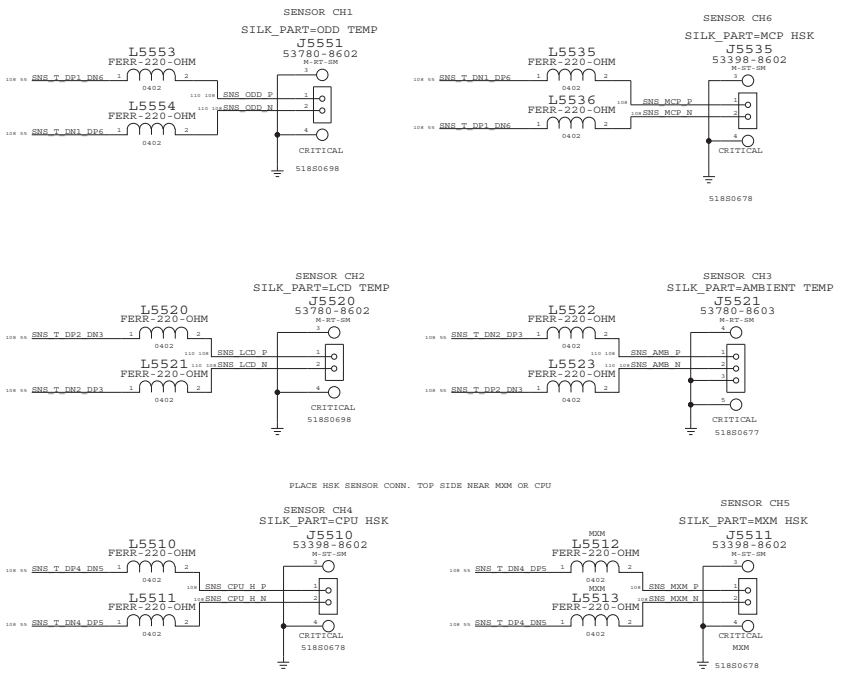
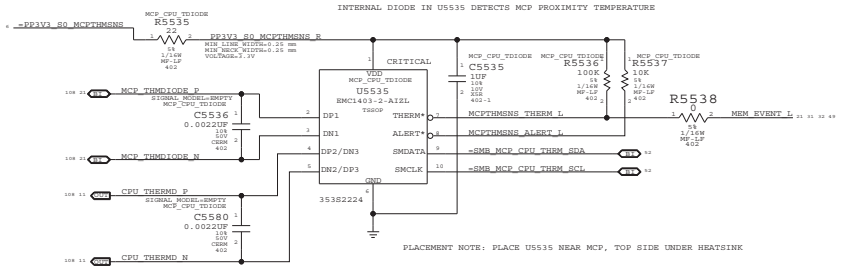
REMOTE THERMAL SENSORS

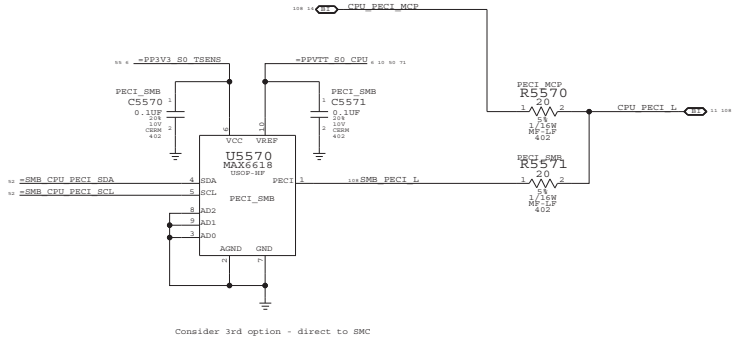
HEATSINKS, AMBIENT, PANEL AND ODD



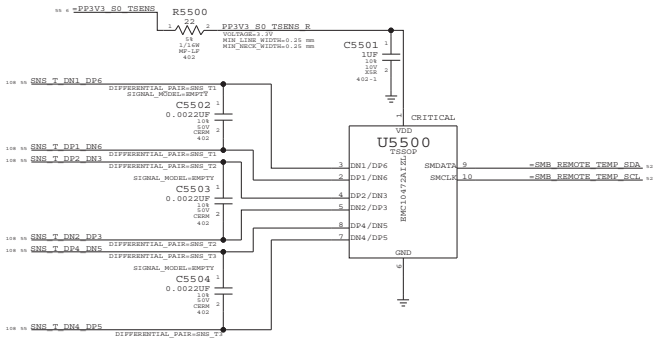
MCP & CPU T-Diode Thermal Sensor



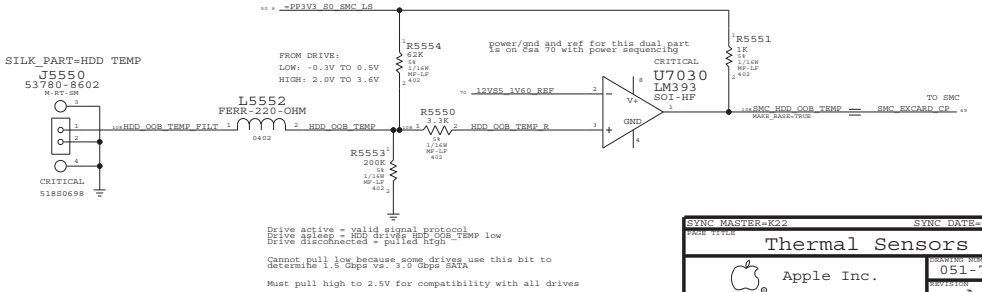
CPU PECI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

Thermal Sensors

Apple Inc.

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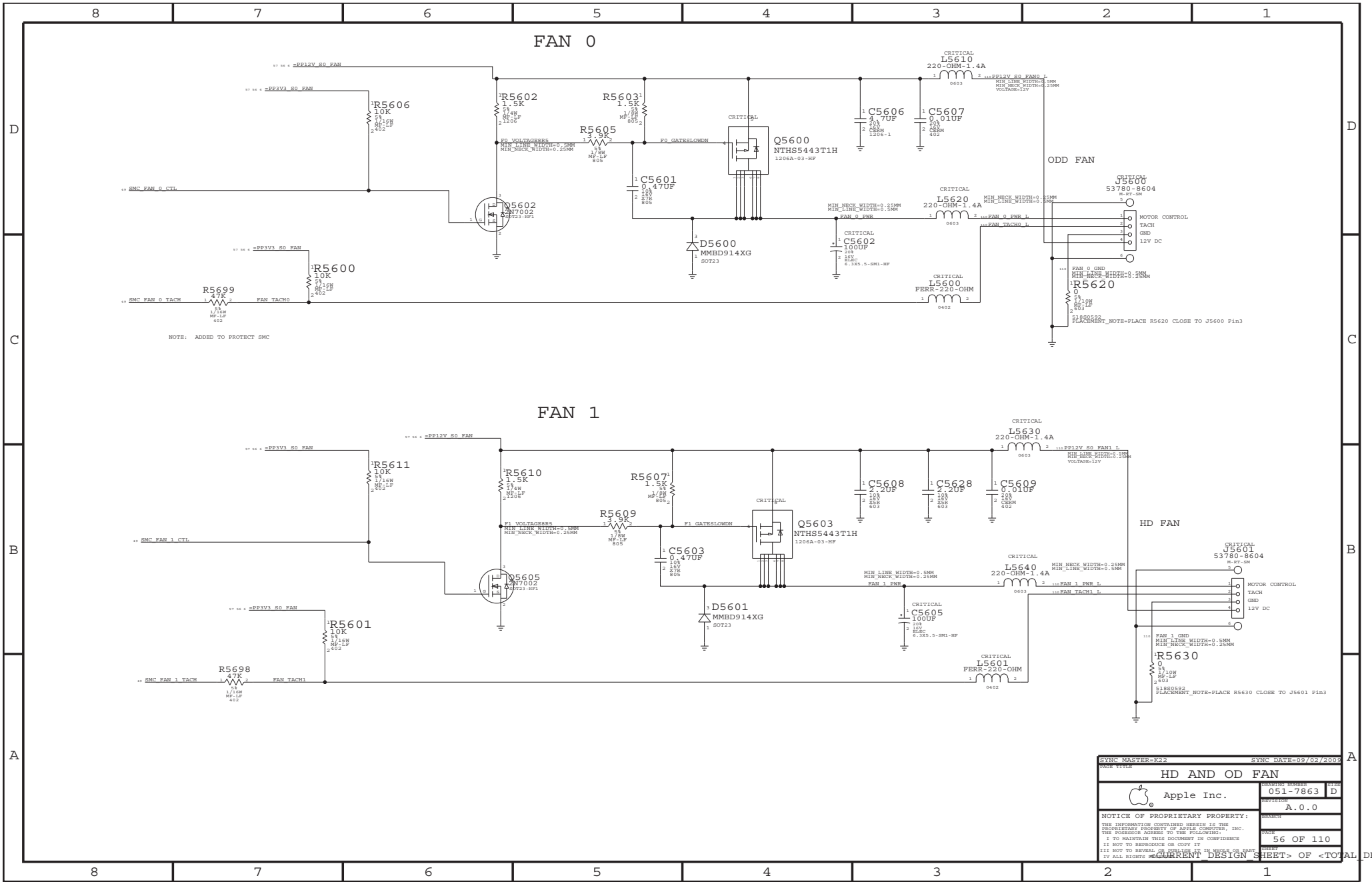
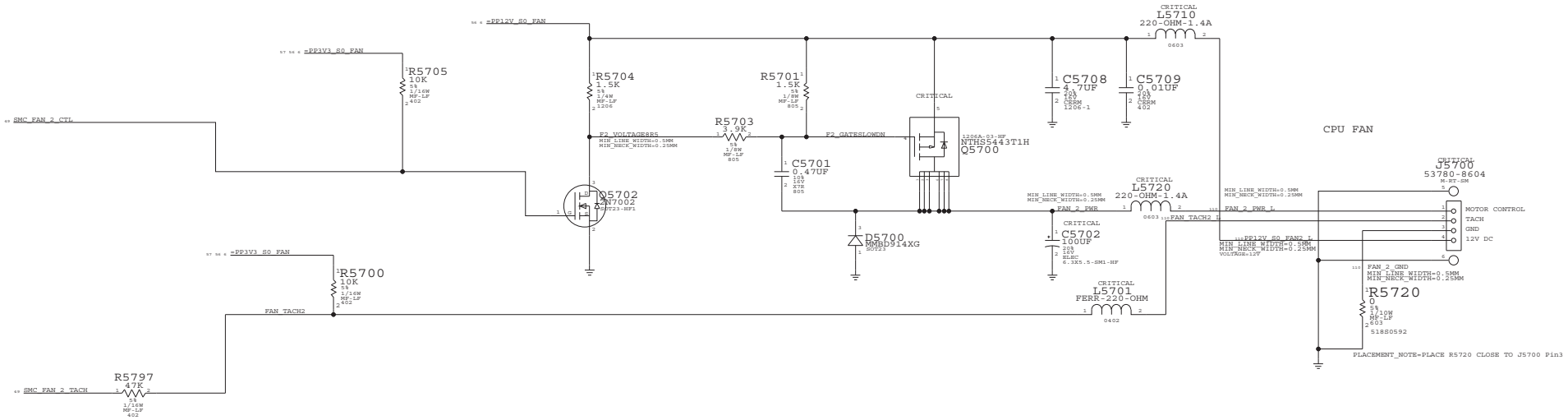


FAN 2



SYNC MASTER=K22 SYNC DATE=09/02/2008

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CPU FAN

Apple Inc.

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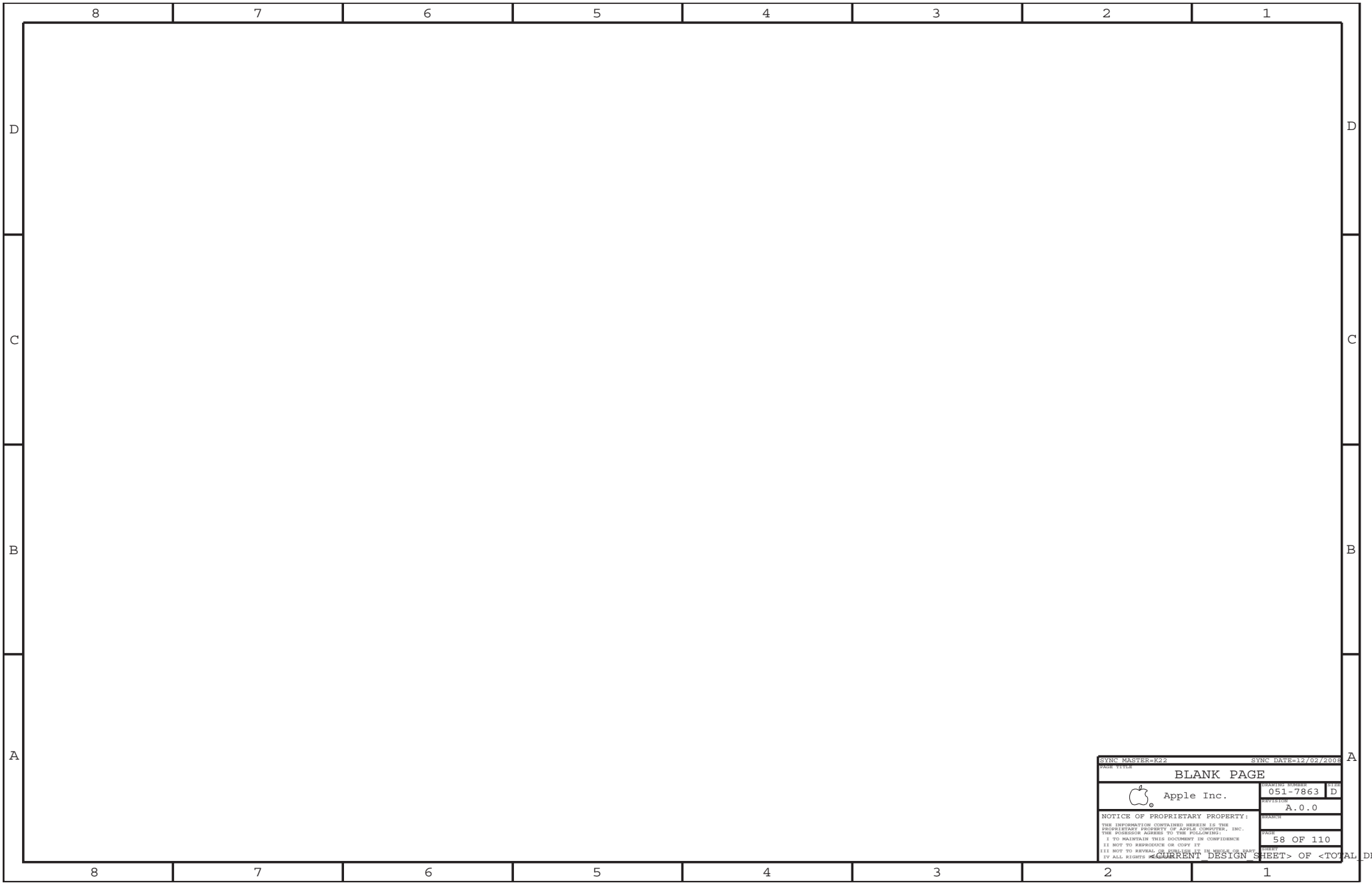
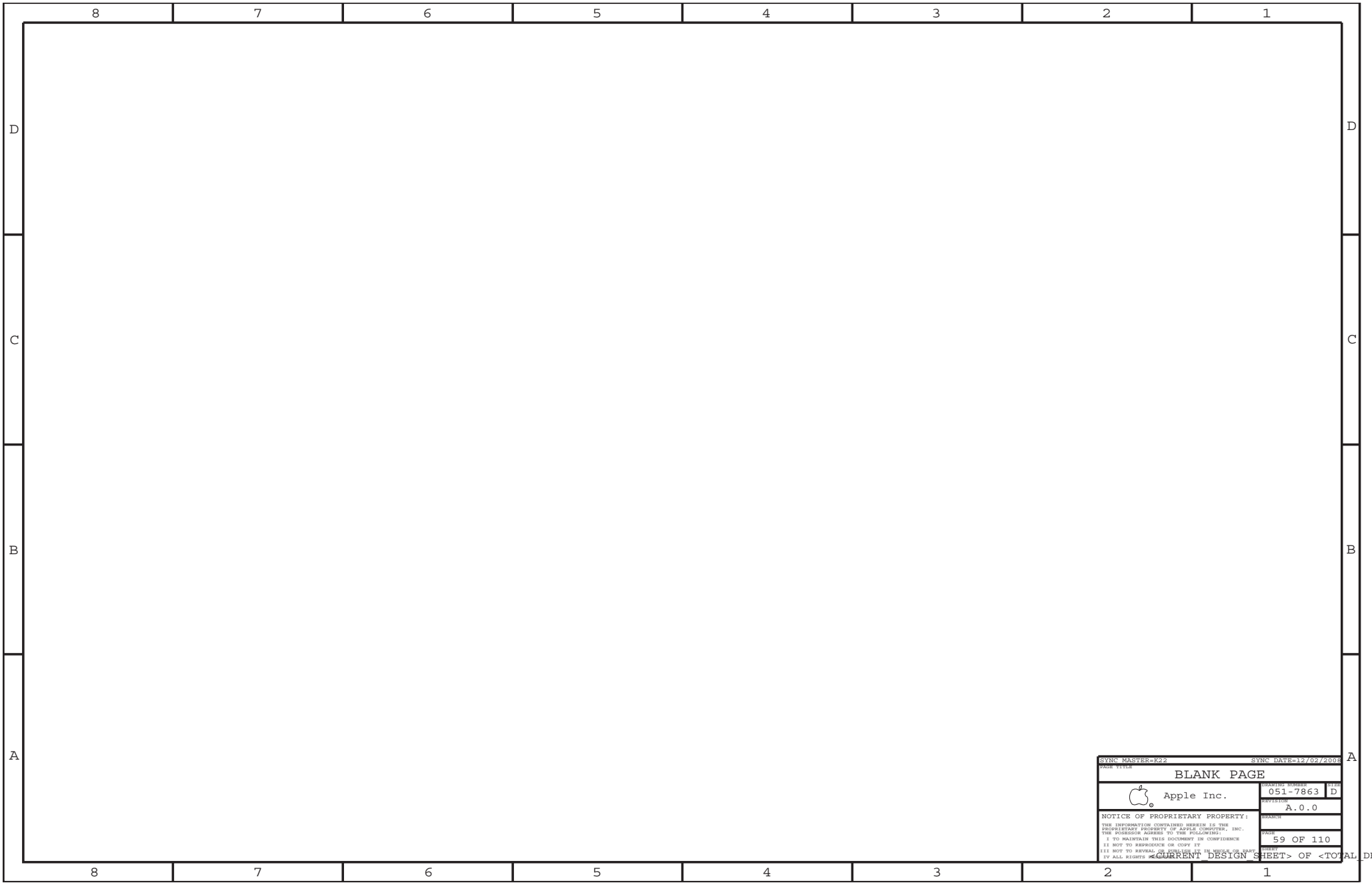
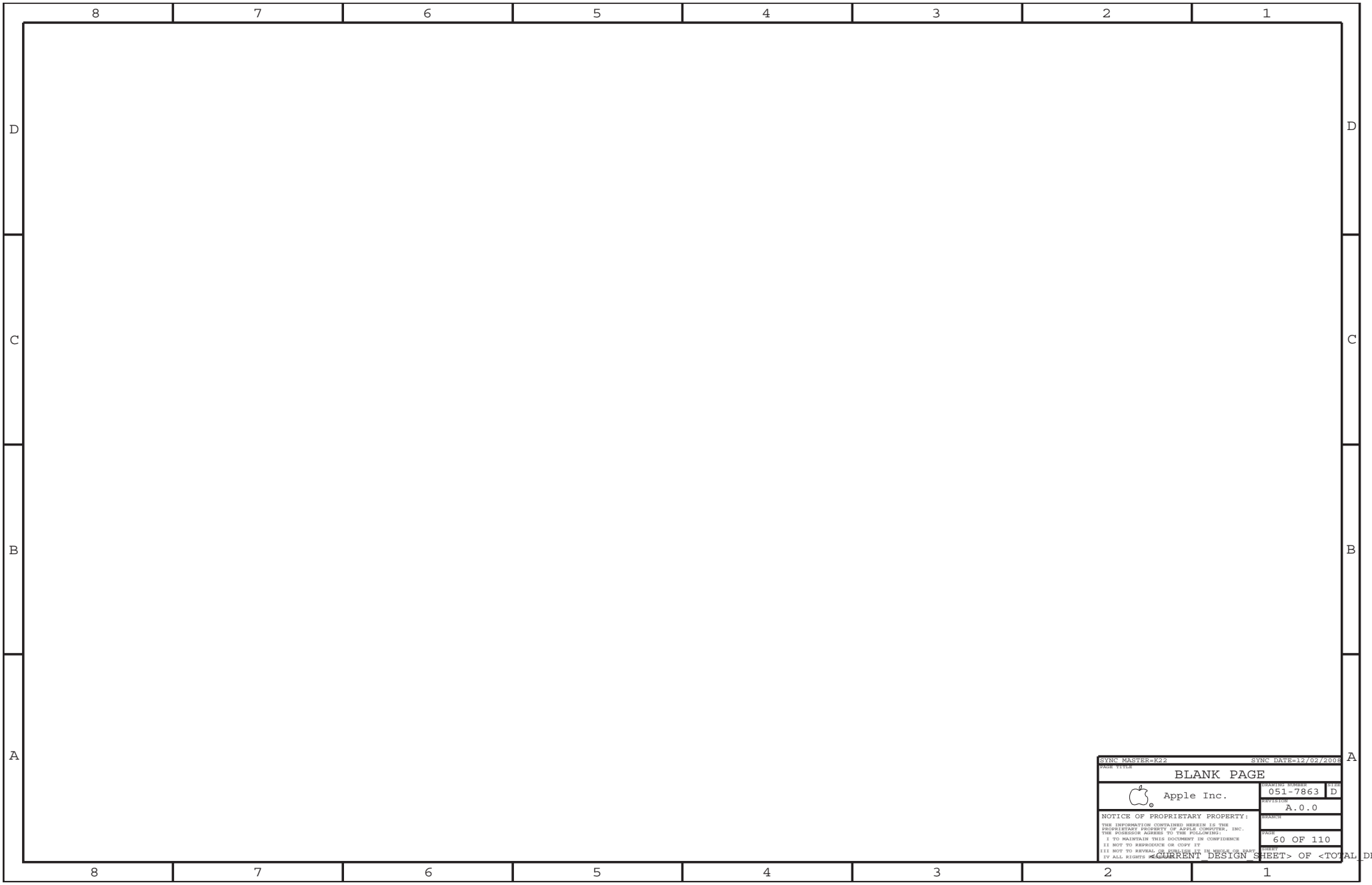
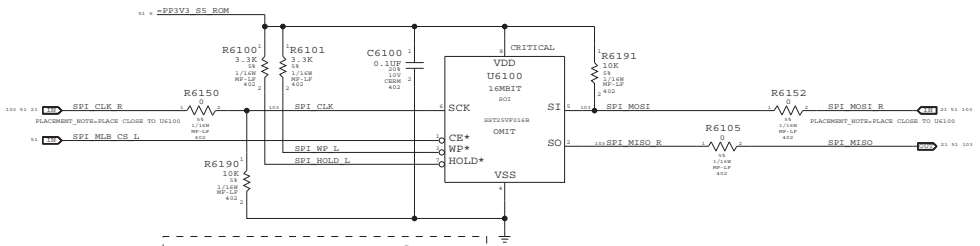
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>









MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

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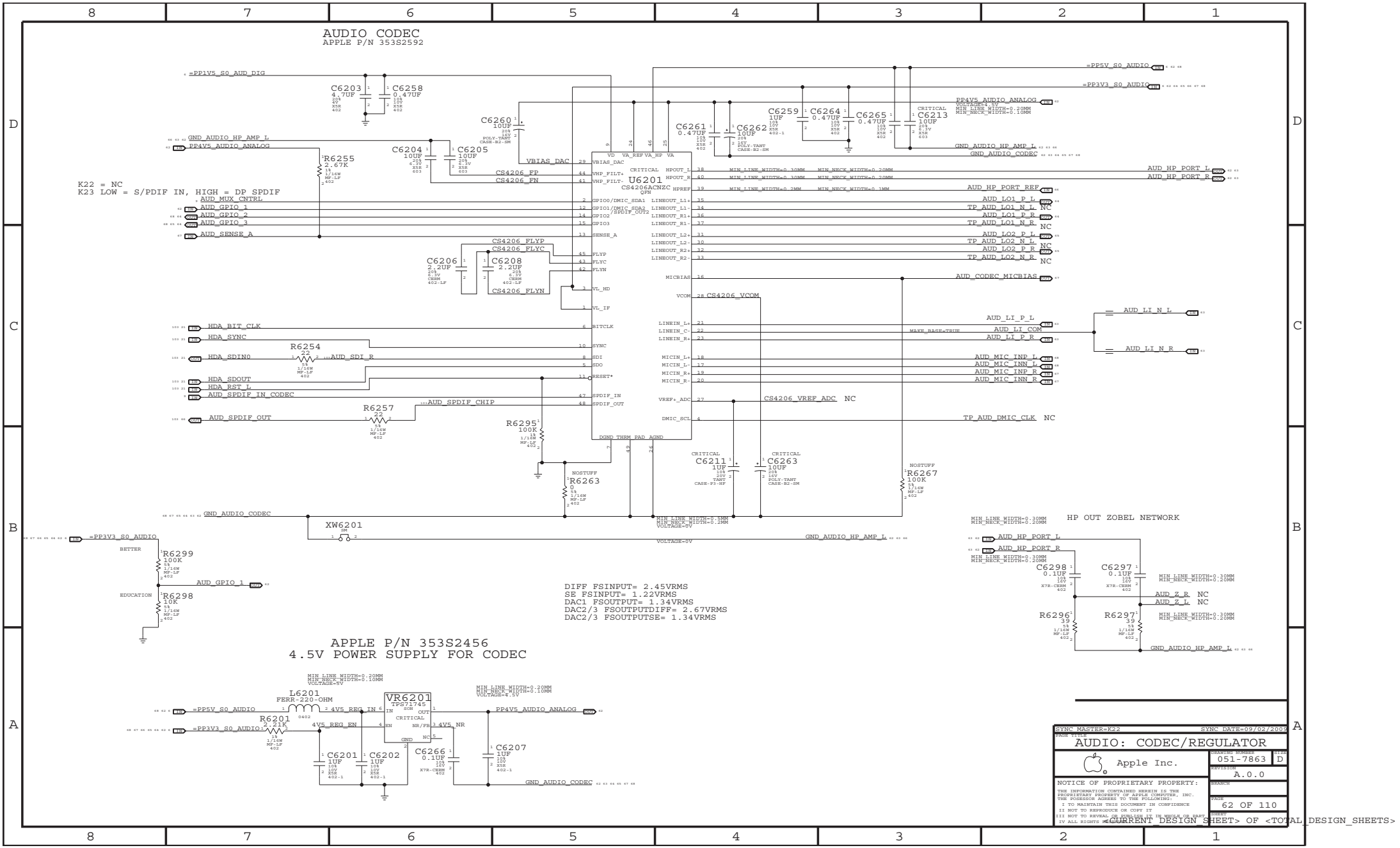
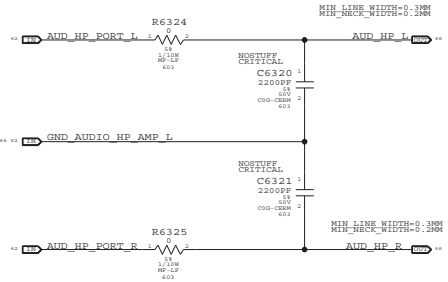
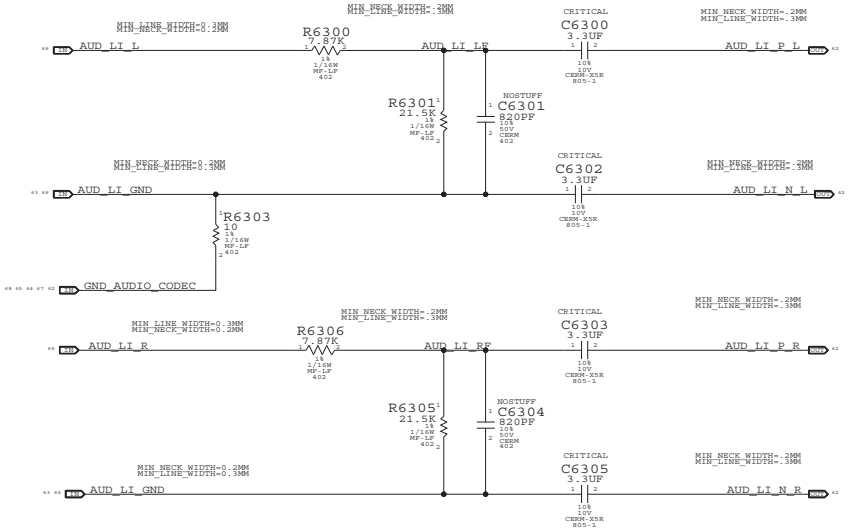


1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC MASTER=SKIPAUDIO	SYNC DATE=04/20/2005
PAGE TITLE: AUDIO: FILTER/BUFFER	
Apple Inc.	DRAWING NUMBER: 051-7863 SIZE: D
	REVISION: A.0.0
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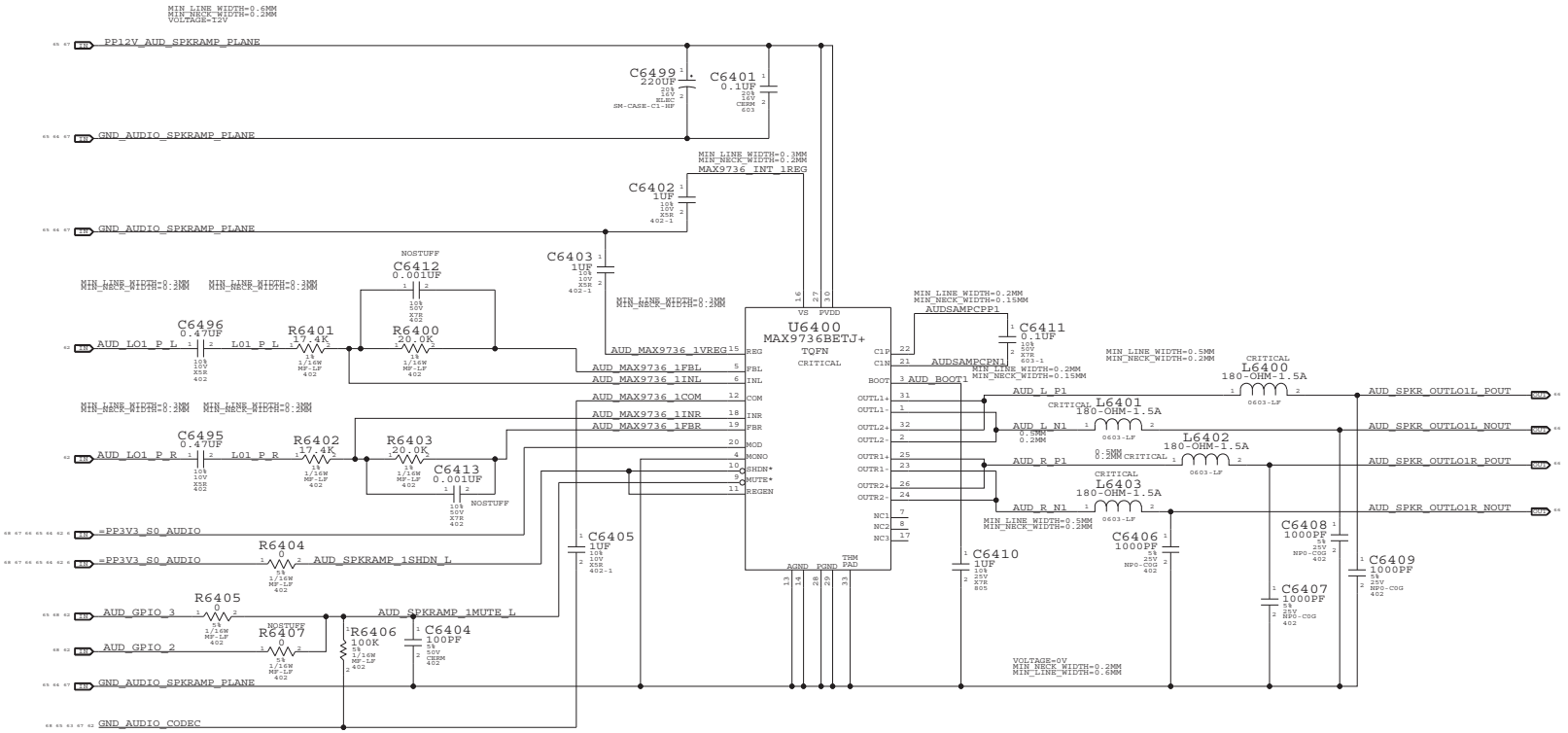
	PAGE: 63 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC MASTER=SKIPAUDIO SYNC DATE=04/20/2005

PAGE TITLE
AUDIO: Tweeter Amp 1

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
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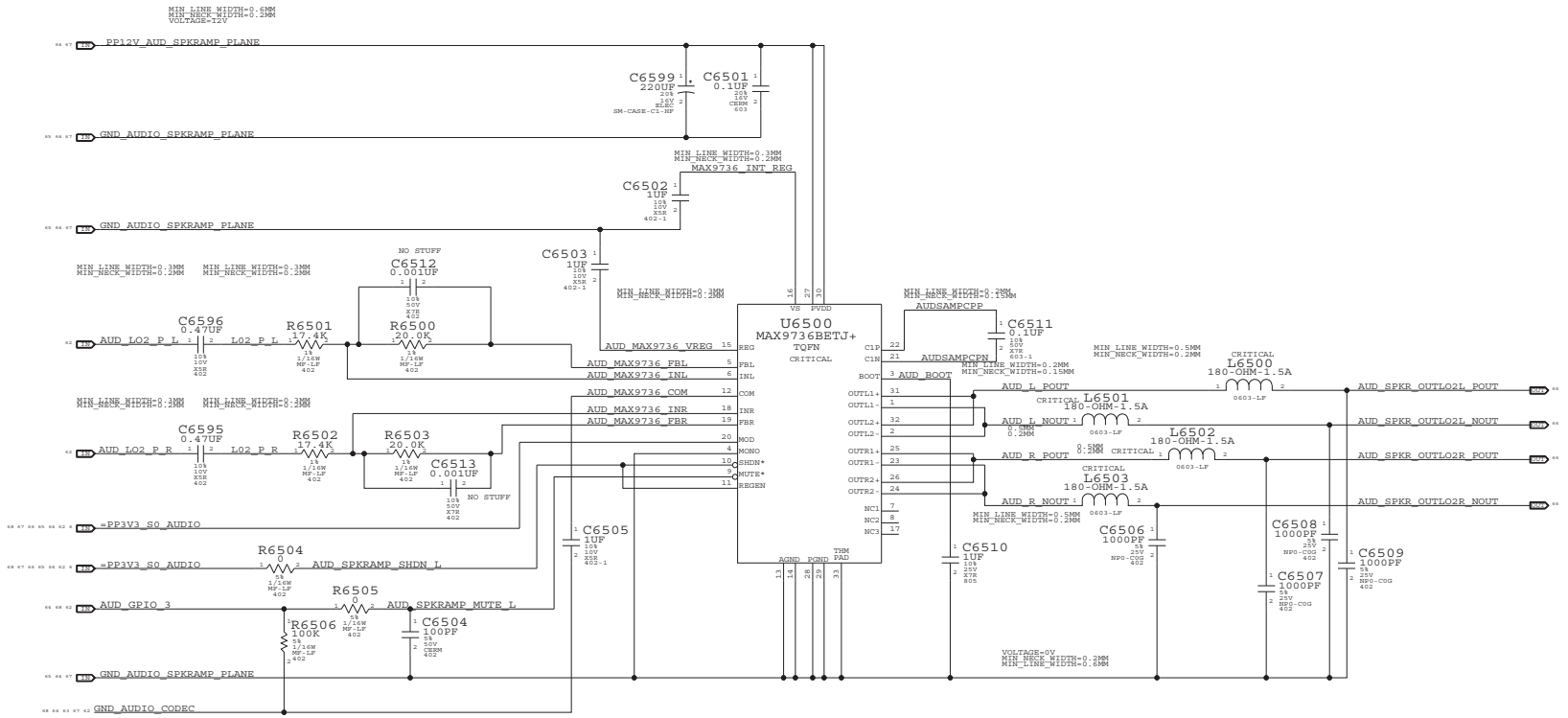
SHEET

WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC MASTER=SKIPAUDIO SYNC DATE=04/20/2005

PAGE TITLE: AUDIO: Woofer Amp

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

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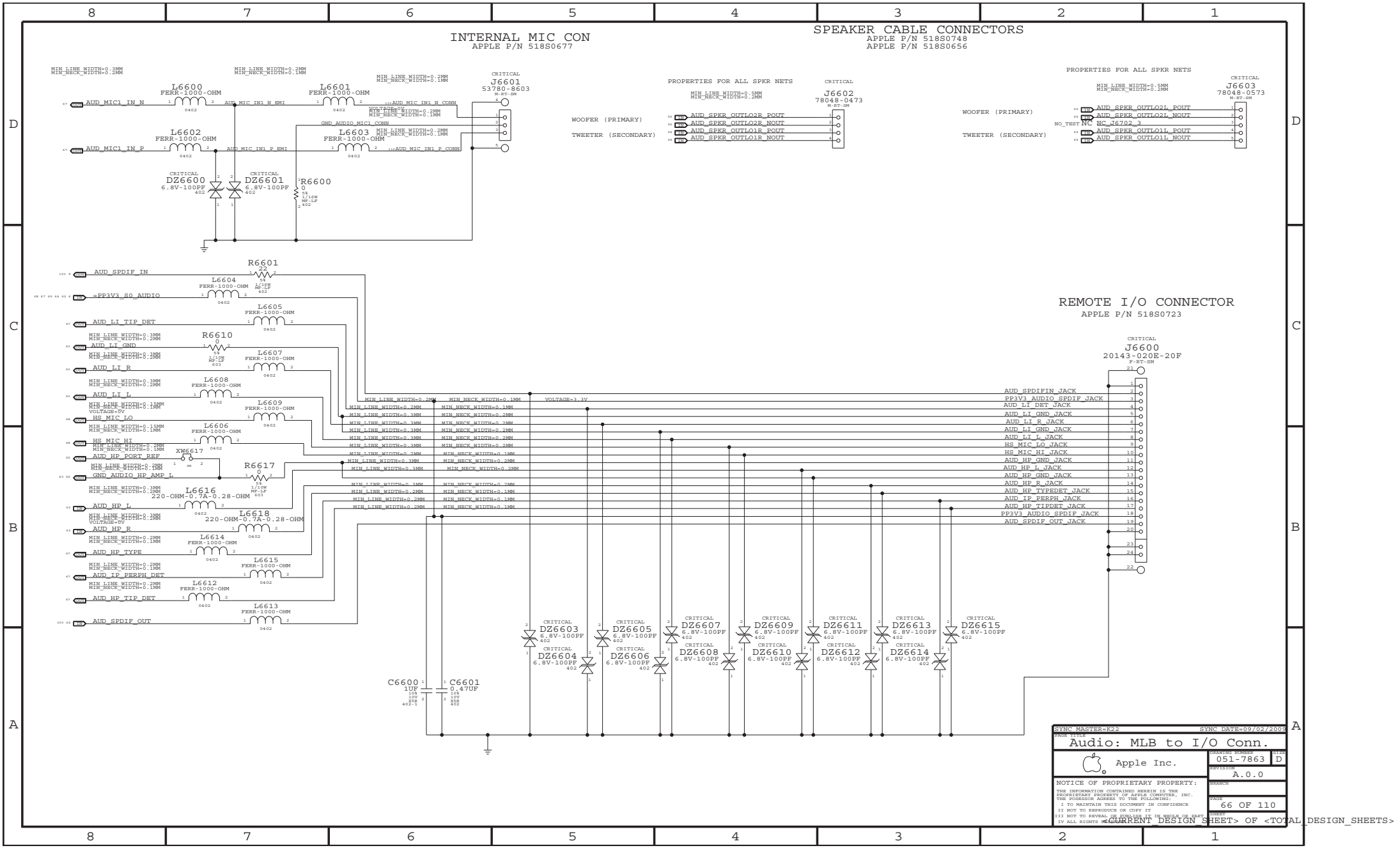
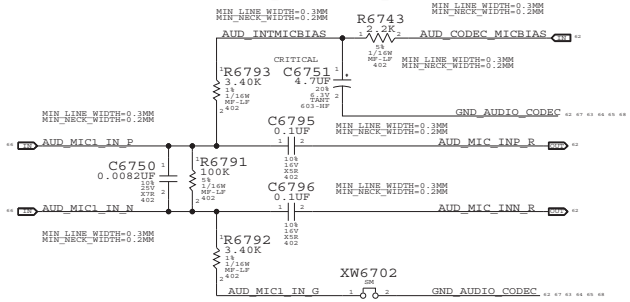
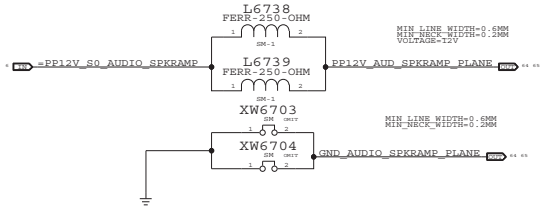


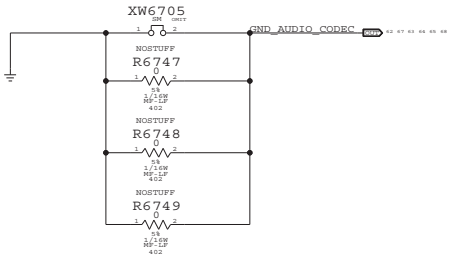
Internal Microphone Impedance Matching



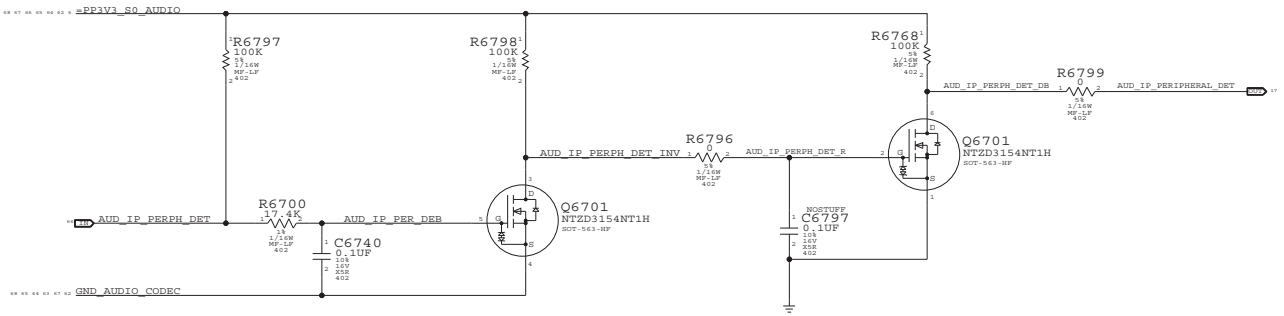
Place Across Ground Split



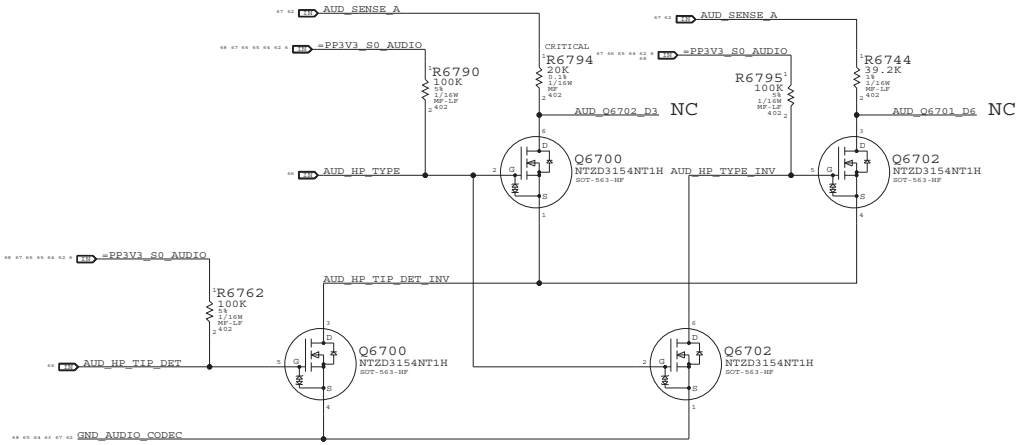
Audio Ground Returns



IPHS HS Detect Debounce CKT

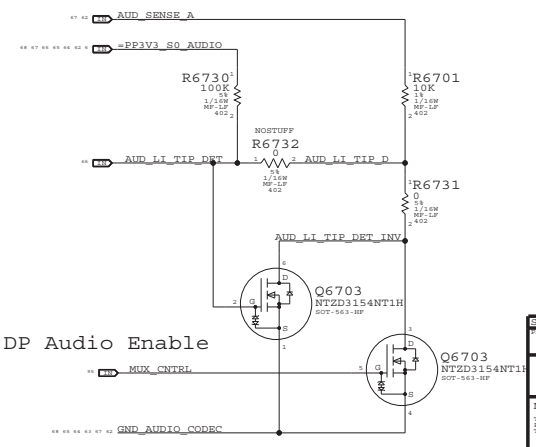


Digital Out



Headphone Out

LI Insert Detect



DP Audio Enable

SYNC MASTER=SKIPAUDIO SYNC DATE=04/20/2005

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

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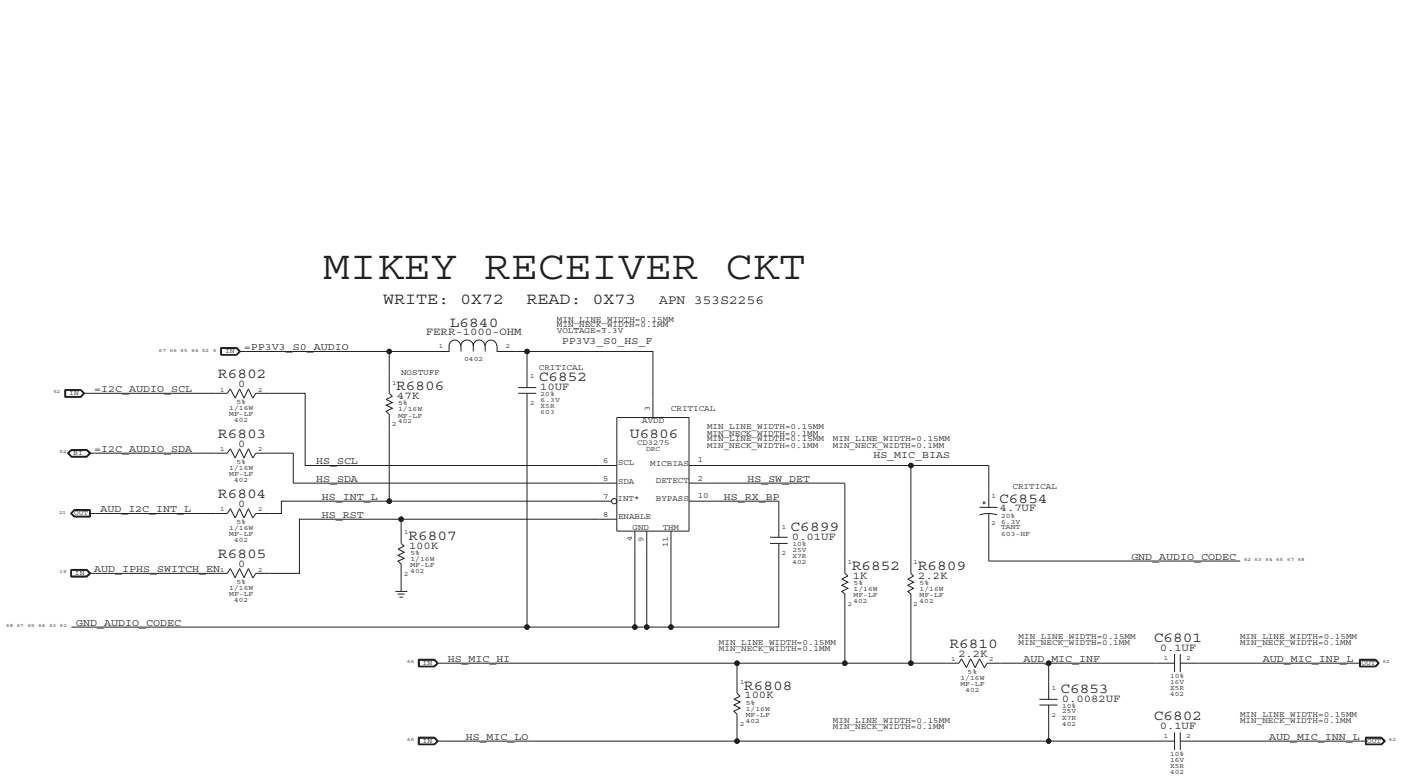
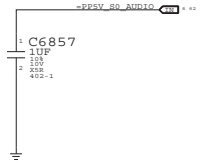
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256





FLP = 8.82 KHZ
PHP = 80 HZ

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

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BRANCH:

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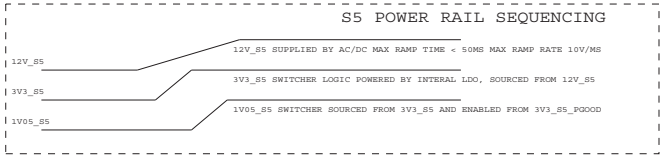
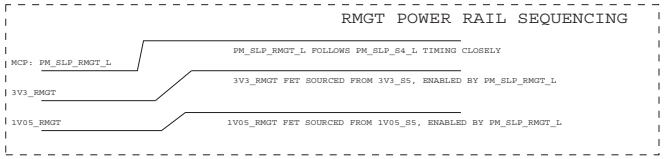
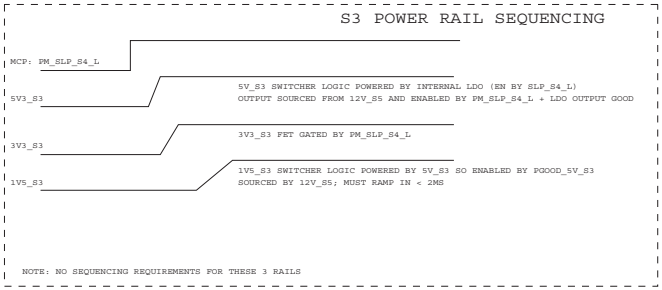
S5 POWER RAIL SEQUENCING



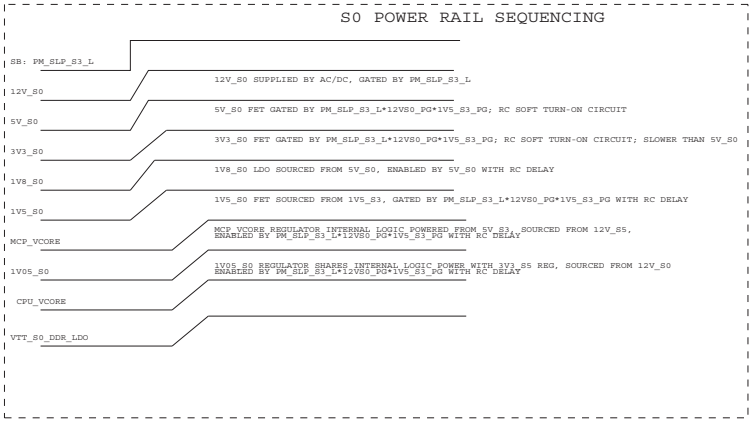
RMGT POWER RAIL SEQUENCING



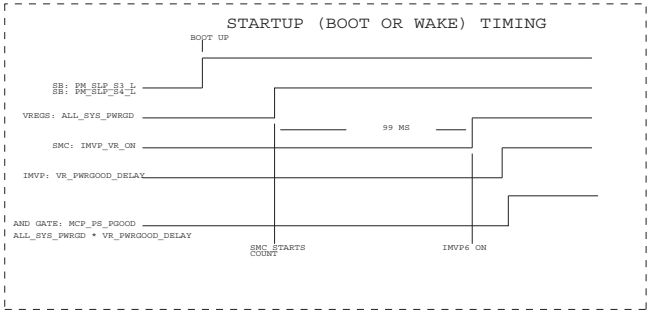
S3 POWER RAIL SEQUENCING



S0 POWER RAIL SEQUENCING

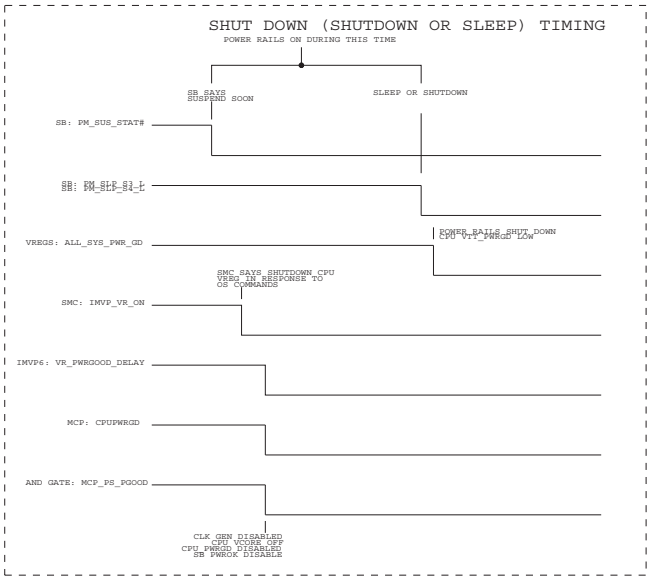


STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
POWER SEQUENCING BLOCK DIAGRAM

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

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Power Control Signals
3.3V,5V S3 enable

State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Enable regulator

USB Port Switch

Enable FET

ENABLE REGULATOR

To SMC

MXM POWER SEQUENCE

MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

Enable FET

Enable FET DELAY OF ~15MS FROM PM_SLP_S3_L

Enable regulator DELAY OF ~18MS FROM PM_SLP_S3_L

Enable regulator DELAY OF ~16MS FROM PM_SLP_S3_L

1.5V_S3 NEED TO BE ON BEFORE S0 FET ON
12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN

1V705V_S0 DERIVES FROM 3.3V_S5

FROM SMC GENERATES PM_RSMRST_L WHICH GOES INTO PGOOD_S5 OF MCP
DELAY IS ABOUT 200MS

PGOOD Comparators

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V

PLACE SHORTS CLOSE TO PLANE CUTS

(9.91V/9.58V; 330MV HYSTERESIS)

(1.30V/1.22V; 80MV HYSTERESIS)

(1.67V/1.53V; 132MV HYSTERESIS)

USING COMPARTOR INSTEAD OF REGULATOR
PGOOD_OUTPUT BECAUSE IF 5V_S3 DOES
NOT COME UP, PTDDR REGULATOR HAS
NO INTERNAL POWER TO PULL PGOOD
LOW

(PULLUPS ARE NEAR LOADS)

ALL_SYS_PWRGD IS ALSO AN INPUT TO THIS
AND GATE BY THE FACT THAT
PM_MXM_PGOOD IS PULLED UP TO IT

S0 RAILS PGOOD

PLACE RESISTORS CLOSE TO U7020

	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
PGOOD and Power Sequencing

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
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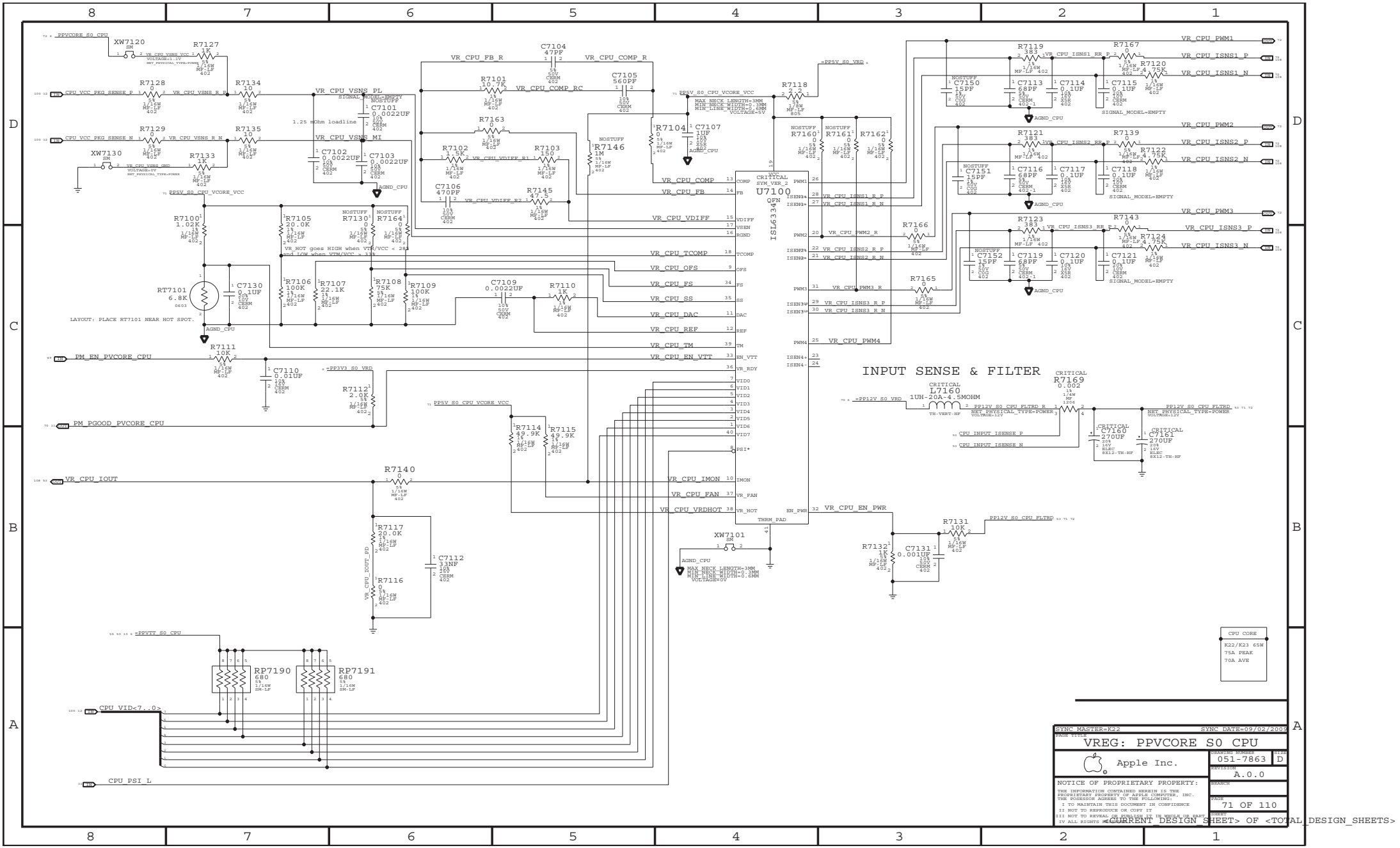
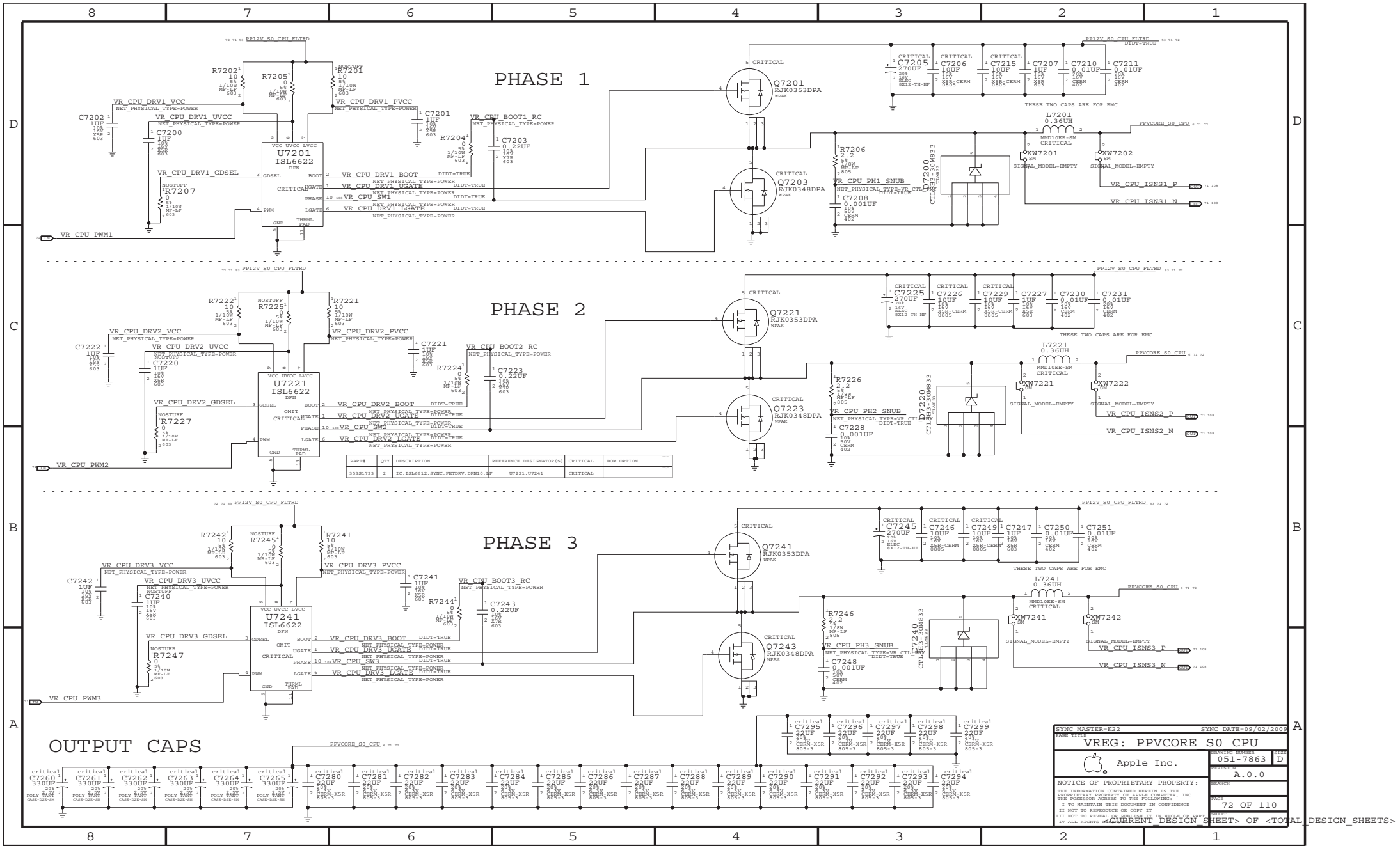
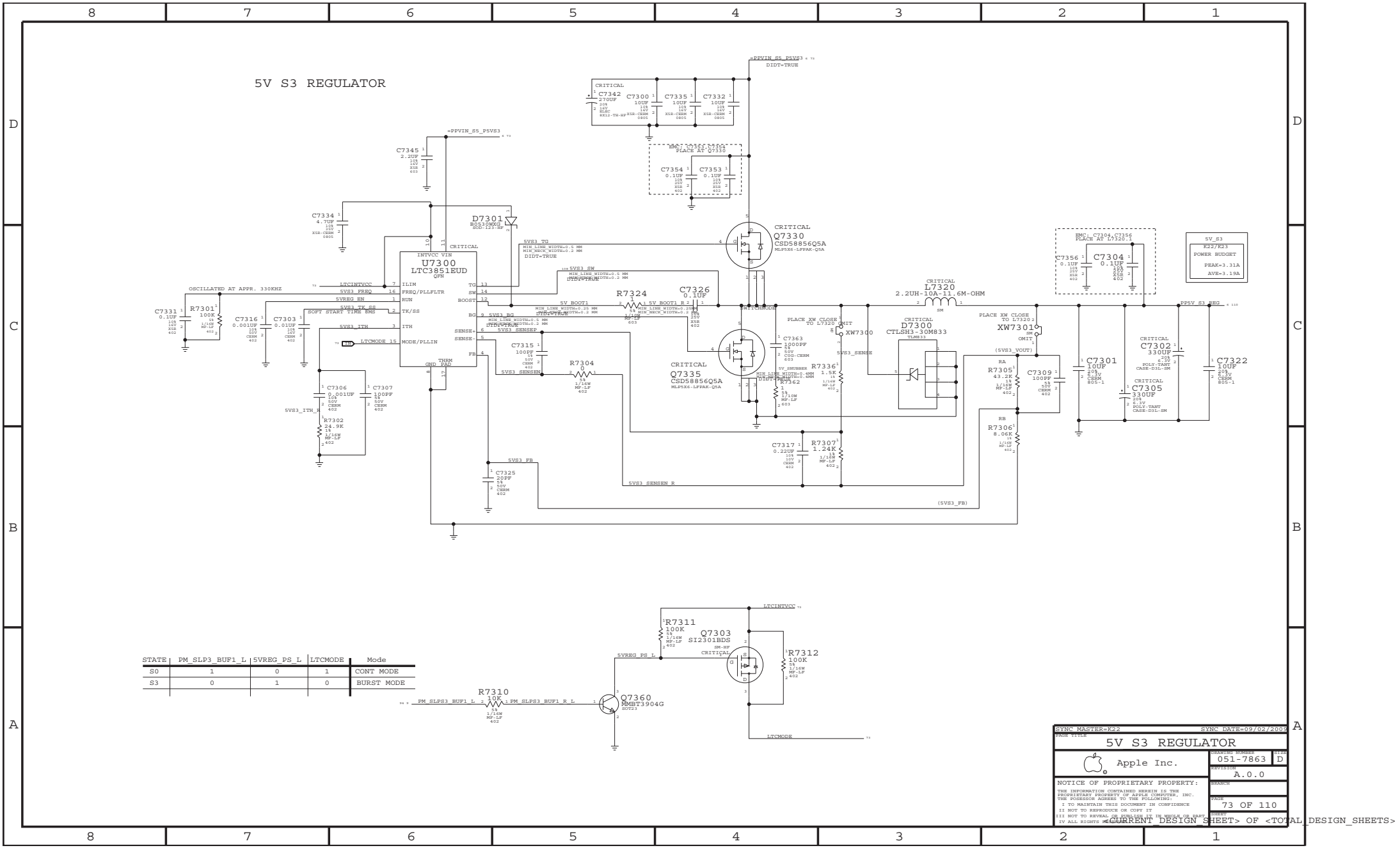
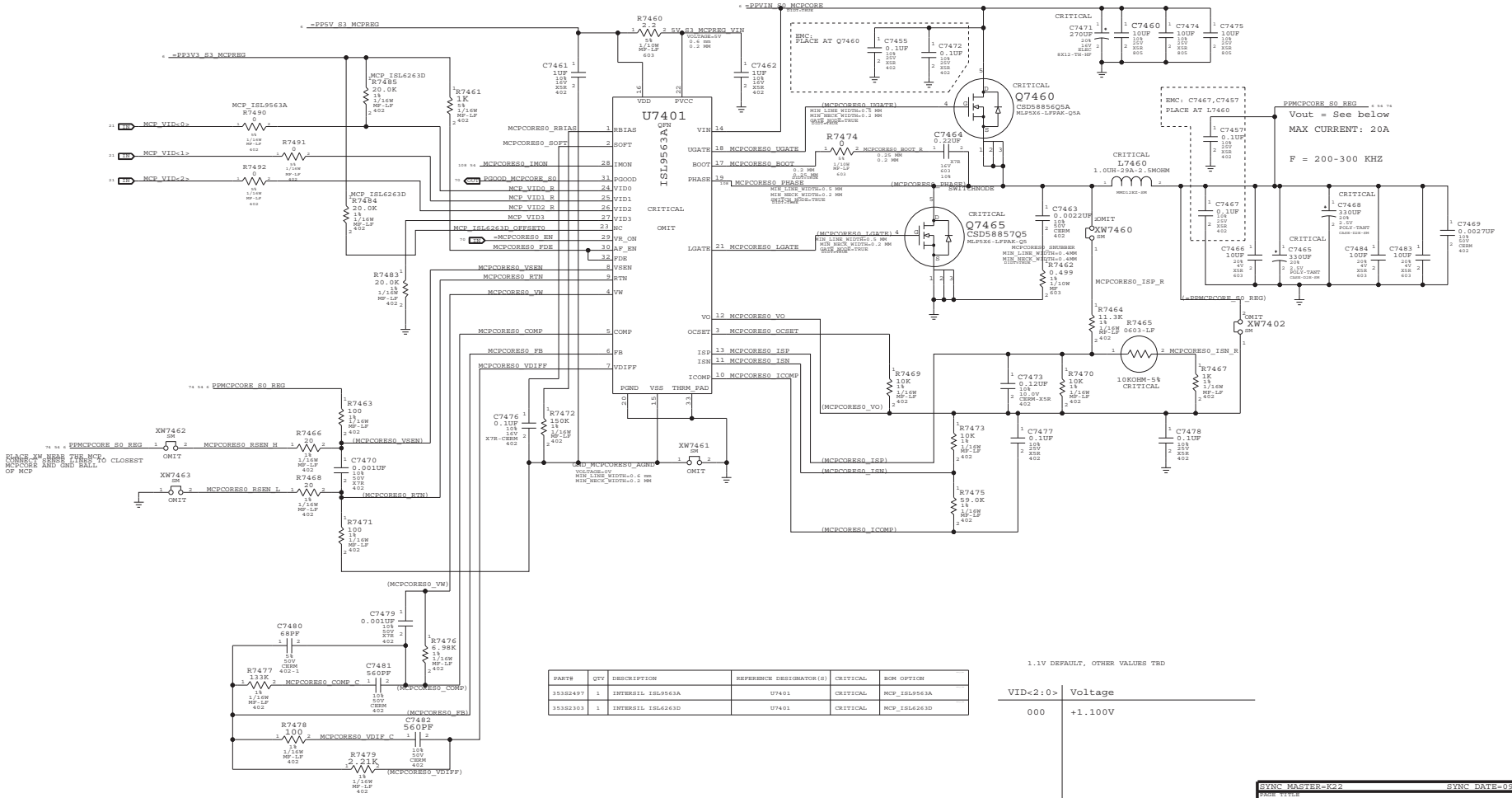






STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

MCP CORE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
353S2303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

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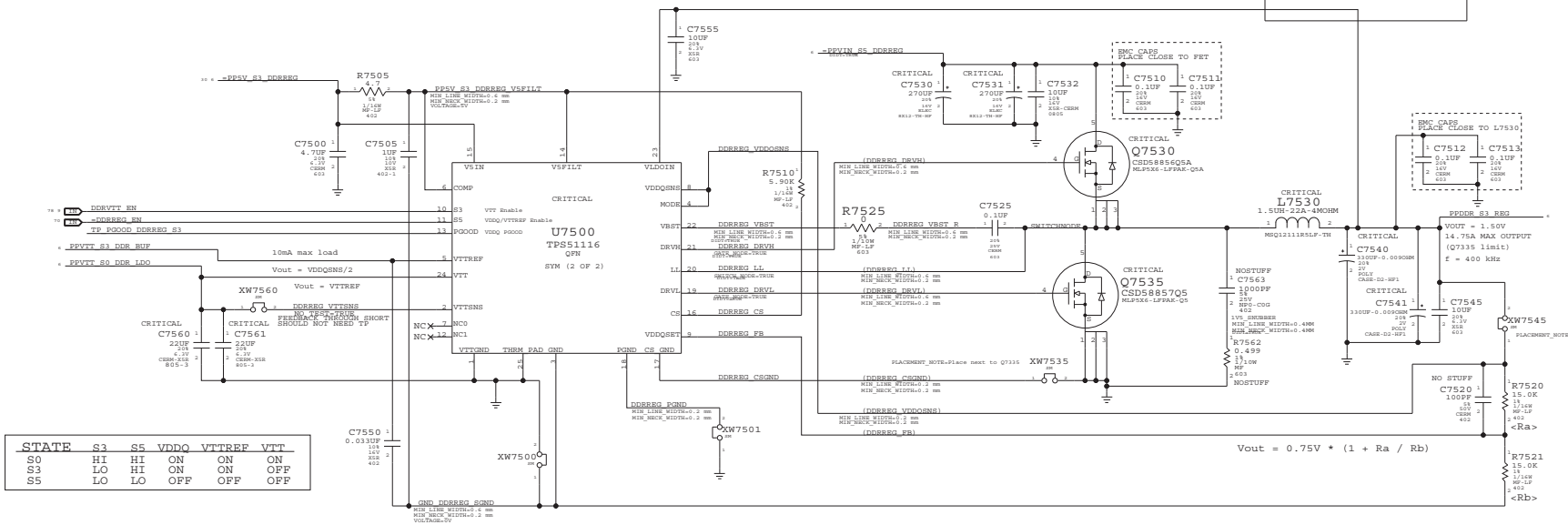
SHEET:

1.5 V DDR SUPPLY

PPDDR_S3_REG

VOUT = 1.5V

PEAK = 11.28A
AVG = 6.72A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

1.5V DDR SUPPLY

Apple Inc.

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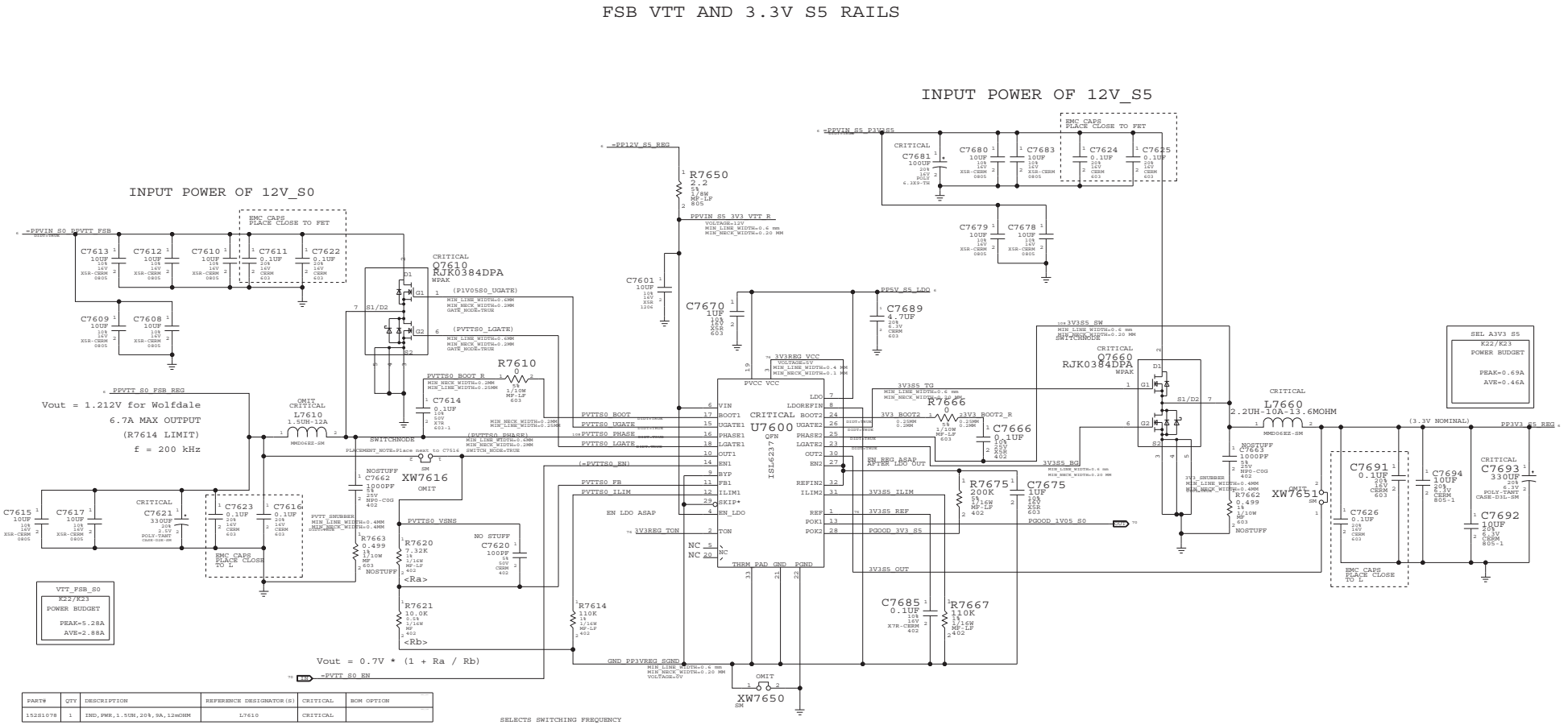
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FSB VTT AND 3.3V S5 RAILS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1078	1	IND,PWR,1.5UH,20%,9A,12mOHM	L7610	CRITICAL	

SYNC MASTER=K22	SYNC DATE=09/02/2008
PAGE TITLE	FSB VTT/3.3V S5 SUPPLIES
Apple Inc.	DRAWING NUMBER 051-7863 REV D
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8	7	6	5	4	3	2	1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

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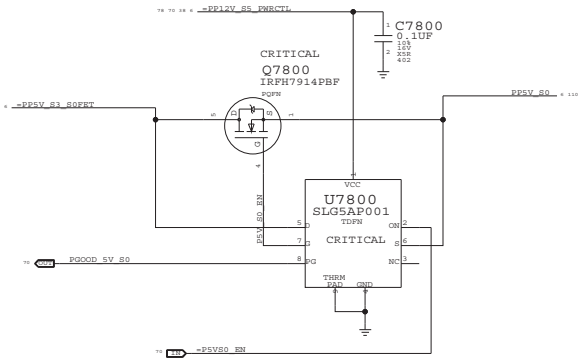
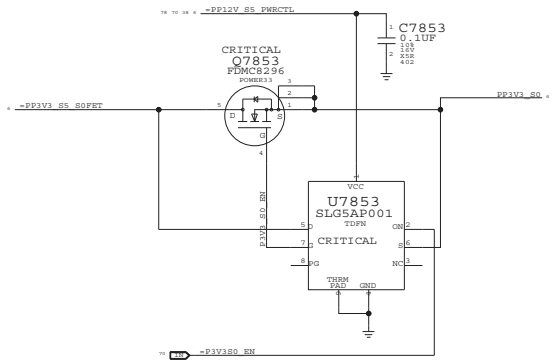
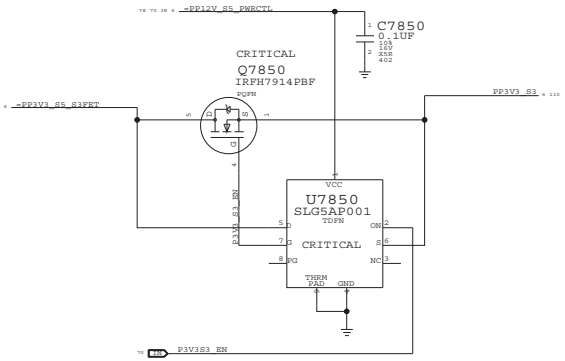
5V S0 FET



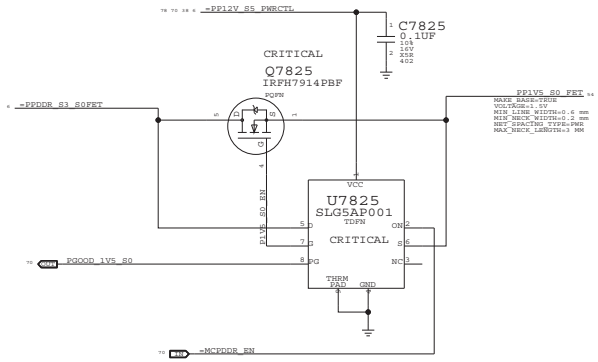
3.3V S0 FET



3.3V S3 FET

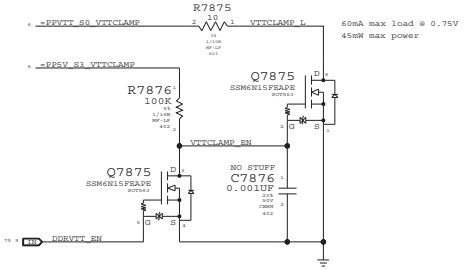


1.5V S0 FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



SYNC MASTER=K22	SYNC DATE=09/02/2008
PAGE TITLE	S3 & S0 FETs
Apple Inc.	DRAWING NUMBER 051-7863 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 78 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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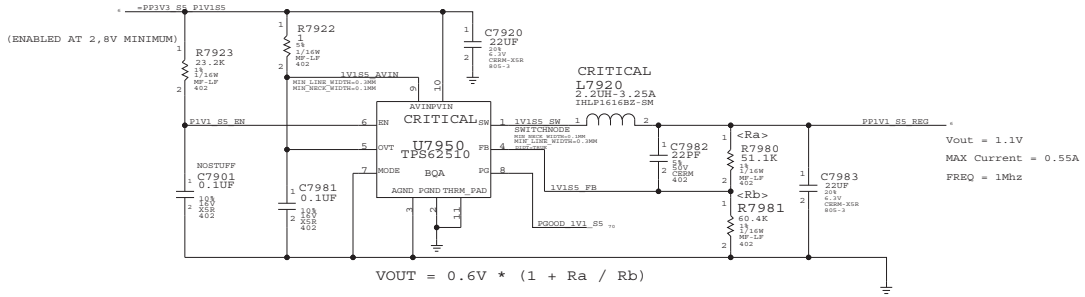
MCP 1.1V_S5 AUXC SUPPLY



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

1V1 S5 POWER SUPPLY

Apple Inc.

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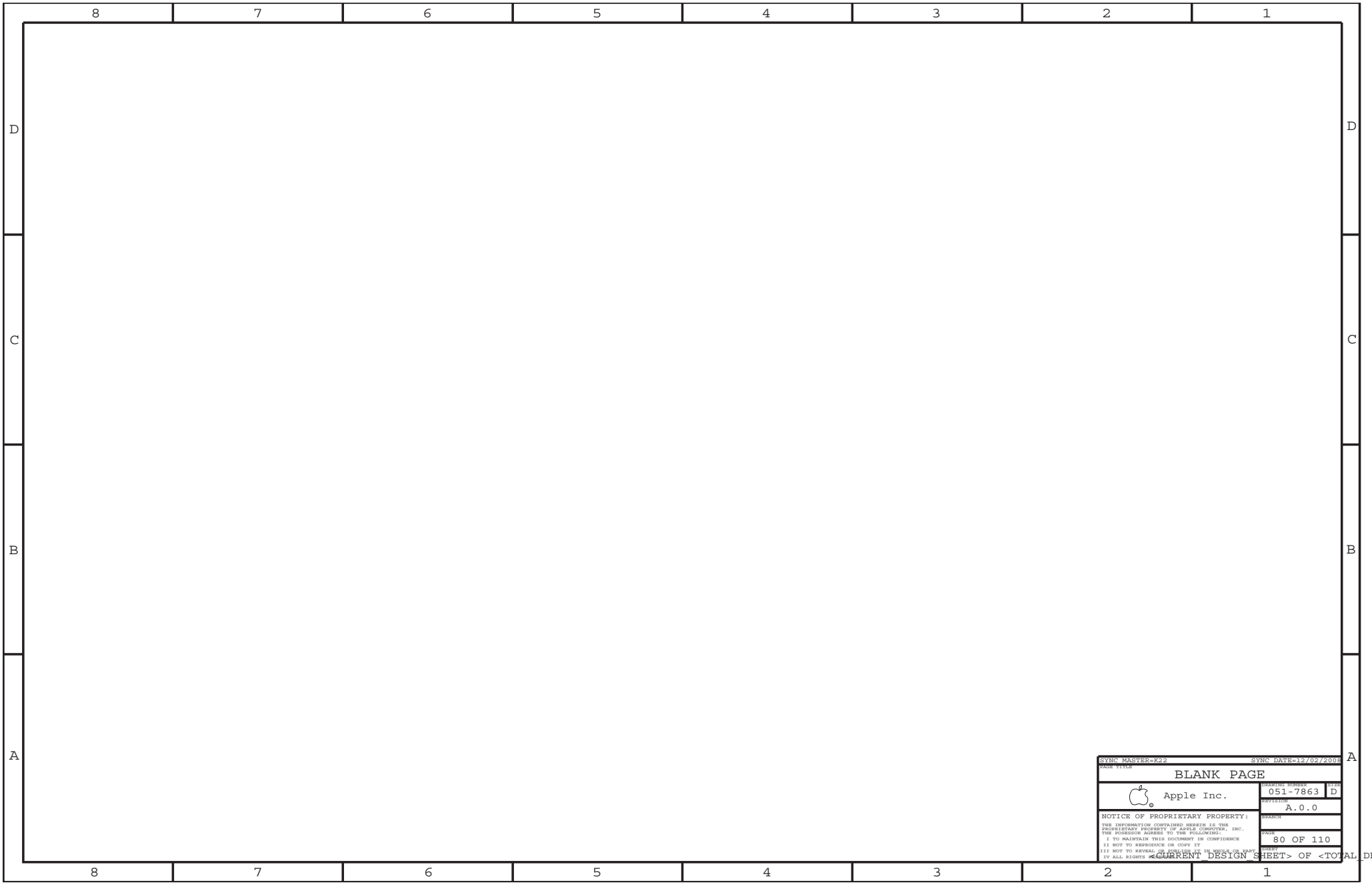

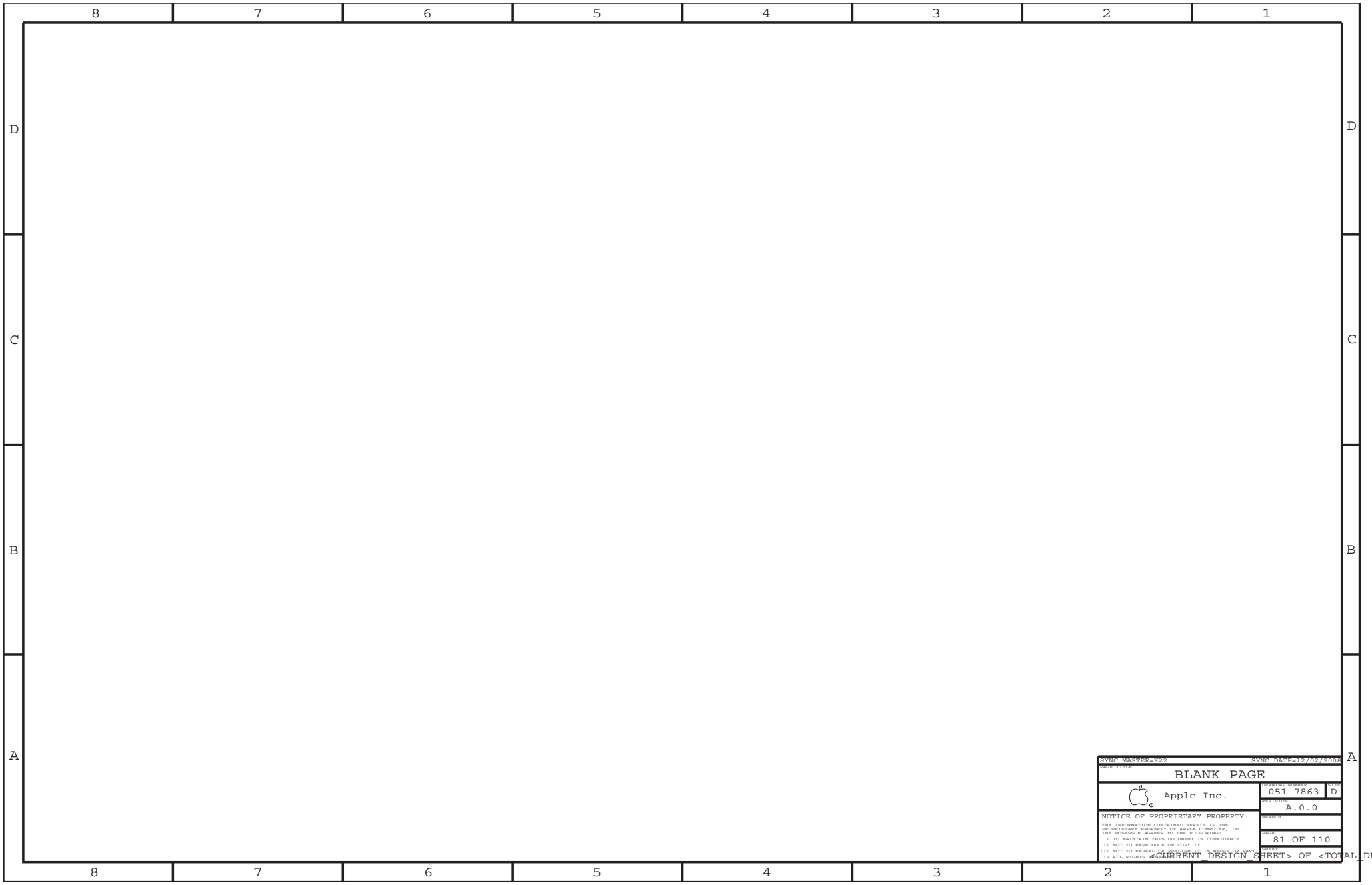

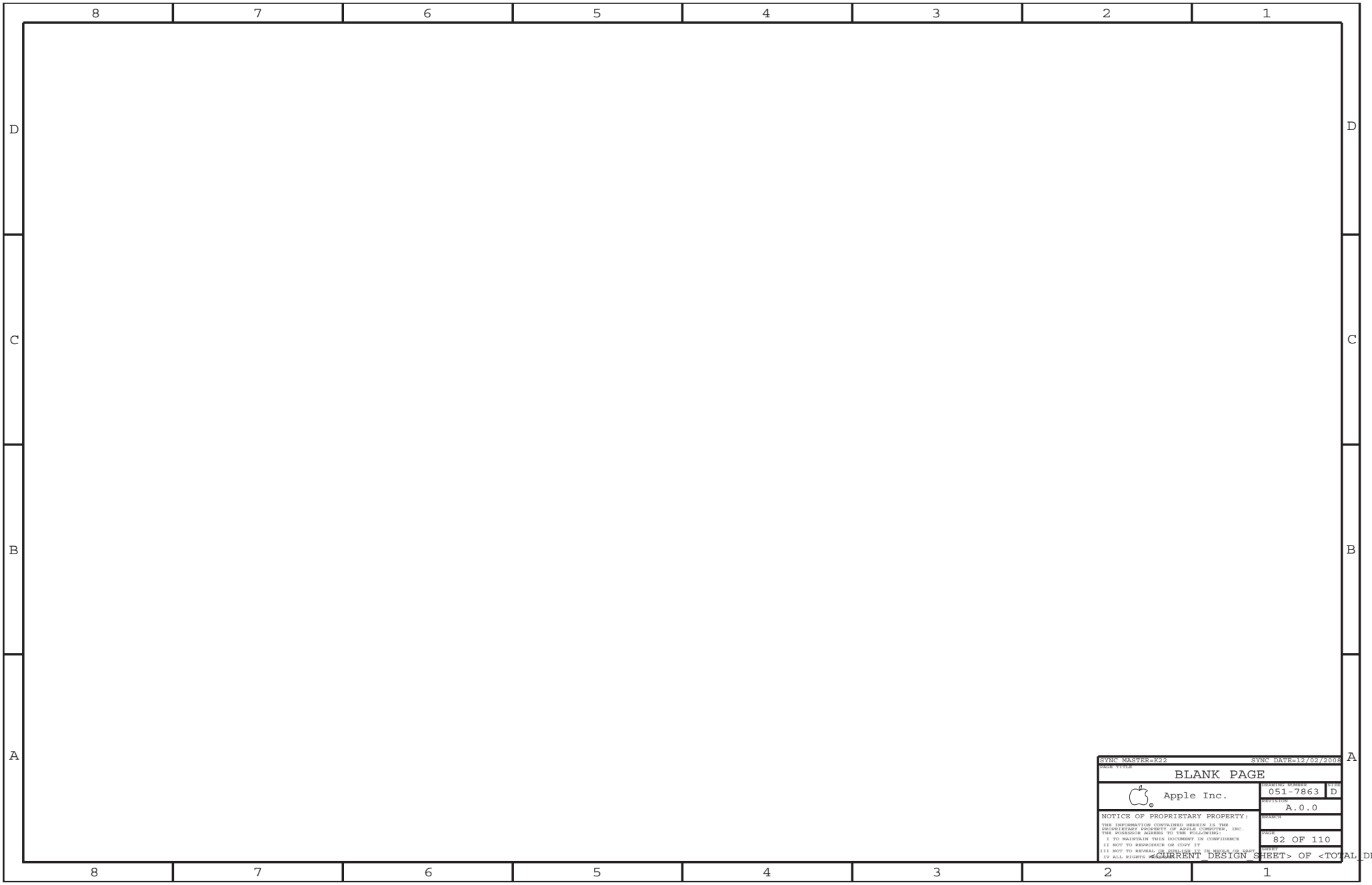

8	7	6	5	4	3	2	1

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SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

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Apple Inc.

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BRANCH

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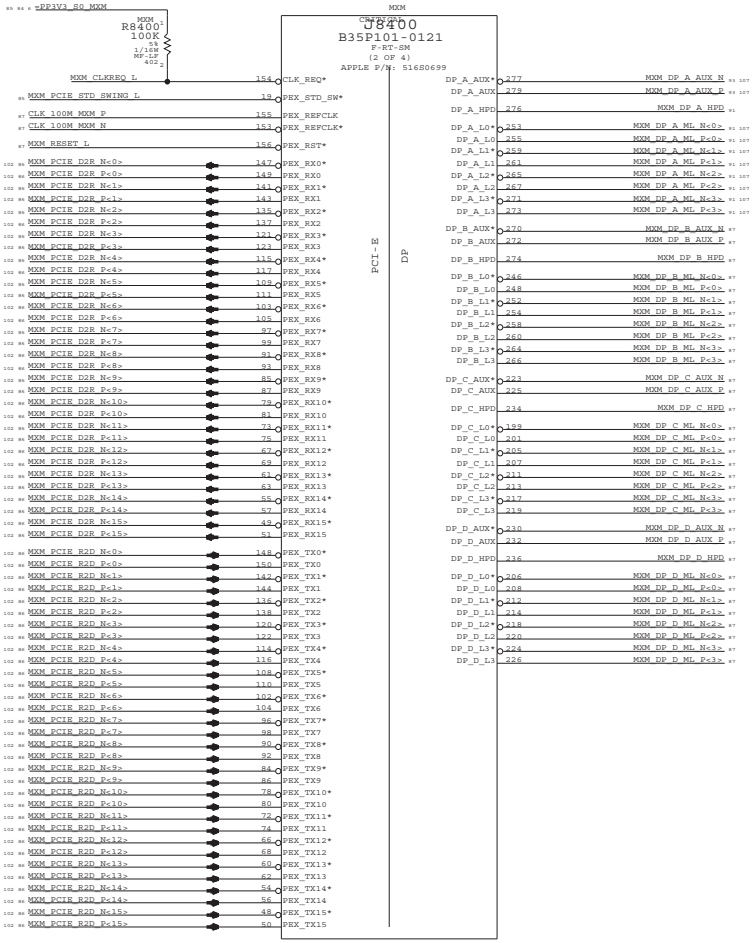
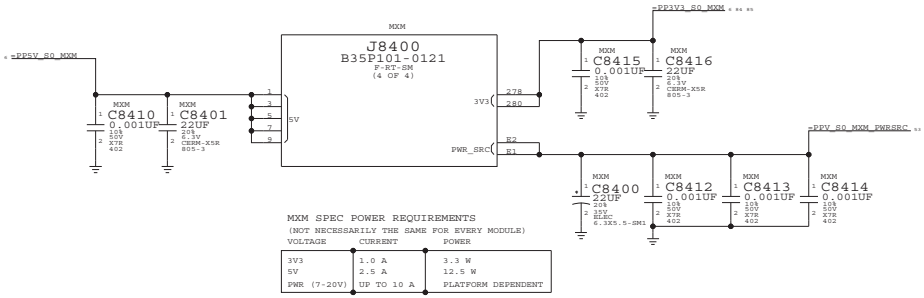
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE
MXM PCIe, DP & Power

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<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =SMB_MXM_THRM_CLK
- =PM_MXM_PGOOD_PULLUP

BOM options provided by this page:

MXM
J8400
B35P101-0121
F-RT-SM
(1 OF 4)

LVDS
MXM_LVDS_DDC_CLK 35 LVDS_DDC_CLK
MXM_LVDS_DDC_DAT 33 LVDS_DDC_DAT
TP_MXM_DVI_HPD 31 DVI_HPD
MXM_LVDS_A_CLK_N 176 LVDS_LCLK*
MXM_LVDS_A_CLK_P 178 LVDS_LCLK
MXM_LVDS_A_DATA_N<0> 200 LVDS_LTX0*
MXM_LVDS_A_DATA_P<0> 202 LVDS_LTX0
MXM_LVDS_A_DATA_N<1> 194 LVDS_LTX1*
MXM_LVDS_A_DATA_P<1> 196 LVDS_LTX1
MXM_LVDS_A_DATA_N<2> 188 LVDS_LTX2*
MXM_LVDS_A_DATA_P<2> 190 LVDS_LTX2
MXM_LVDS_A_DATA_N<3> 182 LVDS_LTX3*
MXM_LVDS_A_DATA_P<3> 184 LVDS_LTX3
MXM_LVDS_B_CLK_N 169 LVDS_UCLK*
MXM_LVDS_B_CLK_P 171 LVDS_UCLK
MXM_LVDS_B_DATA_N<0> 193 LVDS_UTX0*
MXM_LVDS_B_DATA_P<0> 195 LVDS_UTX0
MXM_LVDS_B_DATA_N<1> 187 LVDS_UTX1*
MXM_LVDS_B_DATA_P<1> 189 LVDS_UTX1
MXM_LVDS_B_DATA_N<2> 181 LVDS_UTX2*
MXM_LVDS_B_DATA_P<2> 183 LVDS_UTX2
MXM_LVDS_B_DATA_N<3> 175 LVDS_UTX3*
MXM_LVDS_B_DATA_P<3> 177 LVDS_UTX3

POWER/THERMAL MANAGEMENT
PM_MXM_EN 8 PWR_EN
PM_MXM_PGOOD 6 PWRGOOD
MXM_PWR_LEVEL 18 PWR_LEVEL
=SMB_MXM_THRM_SCL 14 SMB_CLK
=SMB_MXM_THRM_SDA 12 SMB_DAT
MXM_ALERT_L 22 TH_ALERT*
MXM_OVERT_L 20 TH_OVERT*
TP_MXM_TH_PWM 24 TH_PWM

ANALOG DISPLAY
TP_MXM_VGA_DDC_CLK 160 VGA_DDC_CLK
TP_MXM_VGA_DDC_DAT 158 VGA_DDC_DAT
TP_MXM_VGA_BLUE 172 VGA_BLUE
TP_MXM_VGA_GREEN 170 VGA_GREEN
TP_MXM_VGA_HSYNC 164 VGA_HSYNC
TP_MXM_VGA_RED 168 VGA_RED
TP_MXM_VGA_VSYNC 162 VGA_VSYNC

SYSTEM MANAGEMENT
VGA_DISABLE* 21 MXM_VGA_DISABLE_L
GPIO0 26 TP_MXM_GPIO0
GPIO1 28 TP_MXM_GPIO1
GPIO2 30 TP_MXM_GPIO2
HDMI_CEC 29 TP_MXM_HDMI_CEC
OEM0 38
OEM1 39
OEM2 40
OEM3 41
OEM4 42
OEM5 43
OEM6 44
OEM7 45
PNL_BL_EN 25 MXM_PNL_BL_EN
PNL_BL_PWM 27 MXM_PNL_BL_PWM
PNL_PWR_EN 23 MXM_PNL_PWR_EN
RSVD0 10
RSVD1 159
RSVD2 12
RSVD3 161
RSVD4 163
RSVD5 165
RSVD6 167
RSVD7 227
RSVD8 229
RSVD9 231
RSVD10 233
RSVD11 235
RSVD12 237
RSVD13 238
RSVD14 239
RSVD15 240
RSVD16 241
RSVD17 242
RSVD18 243
RSVD19 245
RSVD20 247
RSVD21 249
RSVD22 14
RSVD23 16
PRSNT_L* 281 MXM_DETECT_L
PRSNT_R* 2 MXM_DETECT_R
WAKE* 4 TP_MXM_WAKE_L

MXM
J8400
B35P101-0121
F-RT-SM
(3 OF 4)

GND: 11, 13, 15, 17, 36, 37, 46, 47, 52, 53, 58, 59, 64, 65, 70, 71, 76, 77, 82, 83, 88, 89, 94, 95, 100, 101, 106, 107, 112, 113, 118, 119, 124, 125, 131, 134, 139, 140
GND: 145, 146, 151, 152, 157, 166, 173, 174, 179, 180, 185, 186, 191, 192, 197, 198, 203, 204, 209, 210, 215, 216, 221, 222, 228, 244, 83, 250, 251, 256, 257, 262, 263, 268, 269, 275, 282, 283, E4

PULLUPS & PULLDOWNS AT MXM CONNECTOR

FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD
NOSTUFF
R8510 0 MF-LF 5% 1/16W 402 MXM
MXM_VGA_DISABLE_L

FLOAT = LOW SWING
GND = HIGH SWING
R8504 0 MF-LF 5% 1/16W 402 MXM
MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM
R8500 100K MF-LF 5% 1/16W 402
MXM_DETECT_L
PULLED TO GROUND ON MXM WE DON'T USE CARD DETECT
R8501 100K MF-LF 5% 1/16W 402
MXM_DETECT_R

=PM_MXM_PGOOD_PULLUP
SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL, OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR
R8503 10K MF-LF 5% 1/16W 402
PM_MXM_PGOOD

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800

=PP3V3_S0_MXM
MXM C8570 0.1UF 10V CERM 402
STUFF FOR WRITE PROTECT
NOSTUFF
R8570 0 1/16W MF-LF 402
I2C ADDRESS: AC
U8570 M24C02-WMN6TPHF SO8 VSS
E2/NC2 MXM
E1/NC1 CRITICAL
E0/NC0
WC*
VCC
SDA
SCL
MXM_LVDS_DDC_DAT
MXM_LVDS_DDC_CLK
MXM_ROM_WP

SYNC MASTER=K22 SYNC DATE=09/02/2008
PAGE TITLE
MXM I/O
Apple Inc.
DRAWING NUMBER 051-7863
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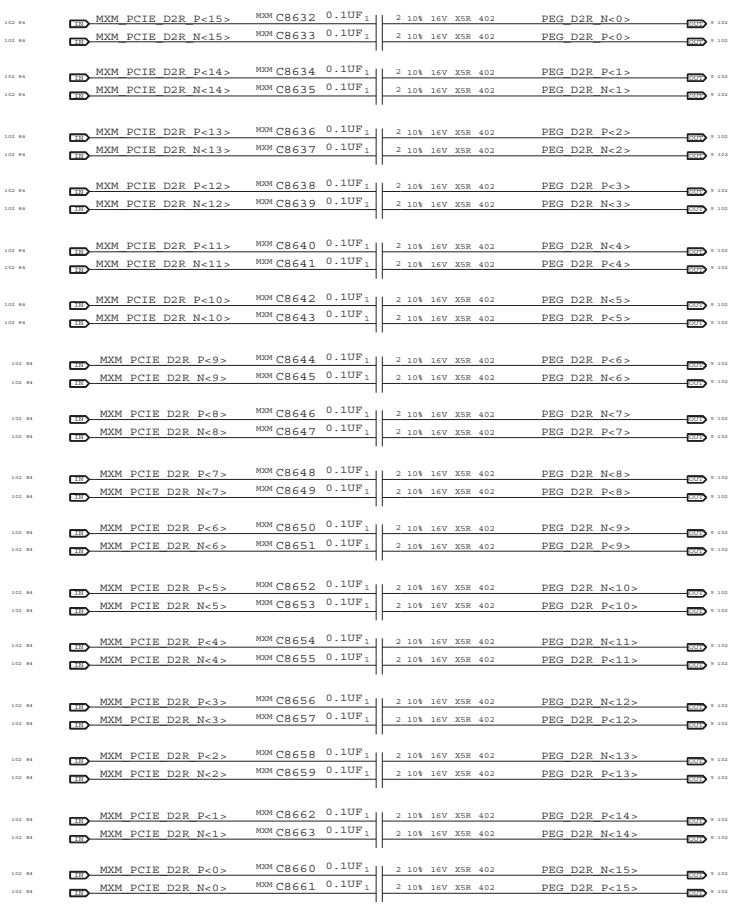
MXM TX CAPS

MXM RX CAPS



SYNC MASTER=K22 SYNC DATE=09/02/2008

PAGE TITLE

MXM PCIE CAPS

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP Connections

CLK_100M_MXM_P	GPU_CLK100M_PCIE_P	MAKE_BASE=TRUE
CLK_100M_MXM_N	GPU_CLK100M_PCIE_N	MAKE_BASE=TRUE
MXM_RESET_L	PEG_RESET_L	MAKE_BASE=TRUE

Unused LVDS Interfaces

LVDS_IG_A_CLK_P	NC_LVDS_IG_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_CLK_N	NC_LVDS_IG_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_P<0>	NC_LVDS_IG_A_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_N<0>	NC_LVDS_IG_A_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_P<1>	NC_LVDS_IG_A_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_N<1>	NC_LVDS_IG_A_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_P<2>	NC_LVDS_IG_A_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_N<2>	NC_LVDS_IG_A_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_P<0>	NC_LVDS_IG_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_N<0>	NC_LVDS_IG_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_P<1>	NC_LVDS_IG_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_N<1>	NC_LVDS_IG_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_P<2>	NC_LVDS_IG_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_N<2>	NC_LVDS_IG_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_P<3>	NC_LVDS_IG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_B_DATA_N<3>	NC_LVDS_IG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_DDC_CLK	NC_LVDS_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_DDC_DATA	NC_LVDS_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM Interfaces

MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_N<0>	NC_MXM_LVDS_A_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_P<0>	NC_MXM_LVDS_A_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_N<1>	NC_MXM_LVDS_A_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_P<1>	NC_MXM_LVDS_A_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_N<2>	NC_MXM_LVDS_A_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_P<2>	NC_MXM_LVDS_A_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_N<3>	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_A_DATA_P<3>	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_P<0>	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_N<1>	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_P<1>	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_N<2>	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_P<2>	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_N<3>	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

MXM_DP_B_ML_P<0..3>	NC_MXM_DP_B_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_B_AUX_P	NC_MXM_DP_B_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_B_AUX_N	NC_MXM_DP_B_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_B_HPD	NC_MXM_DP_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_D_ML_P<0..3>	NC_MXM_DP_D_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_D_ML_N<0..3>	NC_MXM_DP_D_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_D_AUX_P	NC_MXM_DP_D_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_D_AUX_N	NC_MXM_DP_D_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
MXM_DP_D_HPD	NC_MXM_DP_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MCP Interfaces

LVDS_IG_BKL_ON	NC_LVDS_IG_BKL_ON	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_BKL_PWM	NC_LVDS_IG_BKL_PWM	MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_IG_PANEL_PWR	NC_LVDS_IG_PANEL_PWR	MAKE_BASE=TRUE NO_TEST=TRUE
=MCP_HDMI_TXD_P<0..2>	NC_MCP_HDMI_TXD_P<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
=MCP_HDMI_TXD_N<0..2>	NC_MCP_HDMI_TXD_N<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
=MCP_HDMI_TXC_P	NC_MCP_HDMI_TXC_P	MAKE_BASE=TRUE NO_TEST=TRUE
=MCP_HDMI_TXC_N	NC_MCP_HDMI_TXC_N	MAKE_BASE=TRUE NO_TEST=TRUE

=PP3V3_S0_DP

R8700 2.7K 5% 1/16W MF-LF 402

R8701 2.7K 5% 1/16W MF-LF 402

=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	MAKE_BASE=TRUE
=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BASE=TRUE
=MCP_HDMI_HPD	DP_IG_HPD	

R8710 22K 5% 1/16W MF-LF 402

DP_IG_AUX_CH_P	NC_DP_IG_AUX_CH_P	MAKE_BASE=TRUE NO_TEST=TRUE
DP_IG_AUX_CH_N	NC_DP_IG_AUX_CH_N	MAKE_BASE=TRUE NO_TEST=TRUE

DP_IG_CA_DET

R8711 1M 5% 1/16W MF-LF 402

SYNC MASTER=MARKVIDEO SYNC DATE=03/12/2008

PAGE TITLE

Display: Aliases

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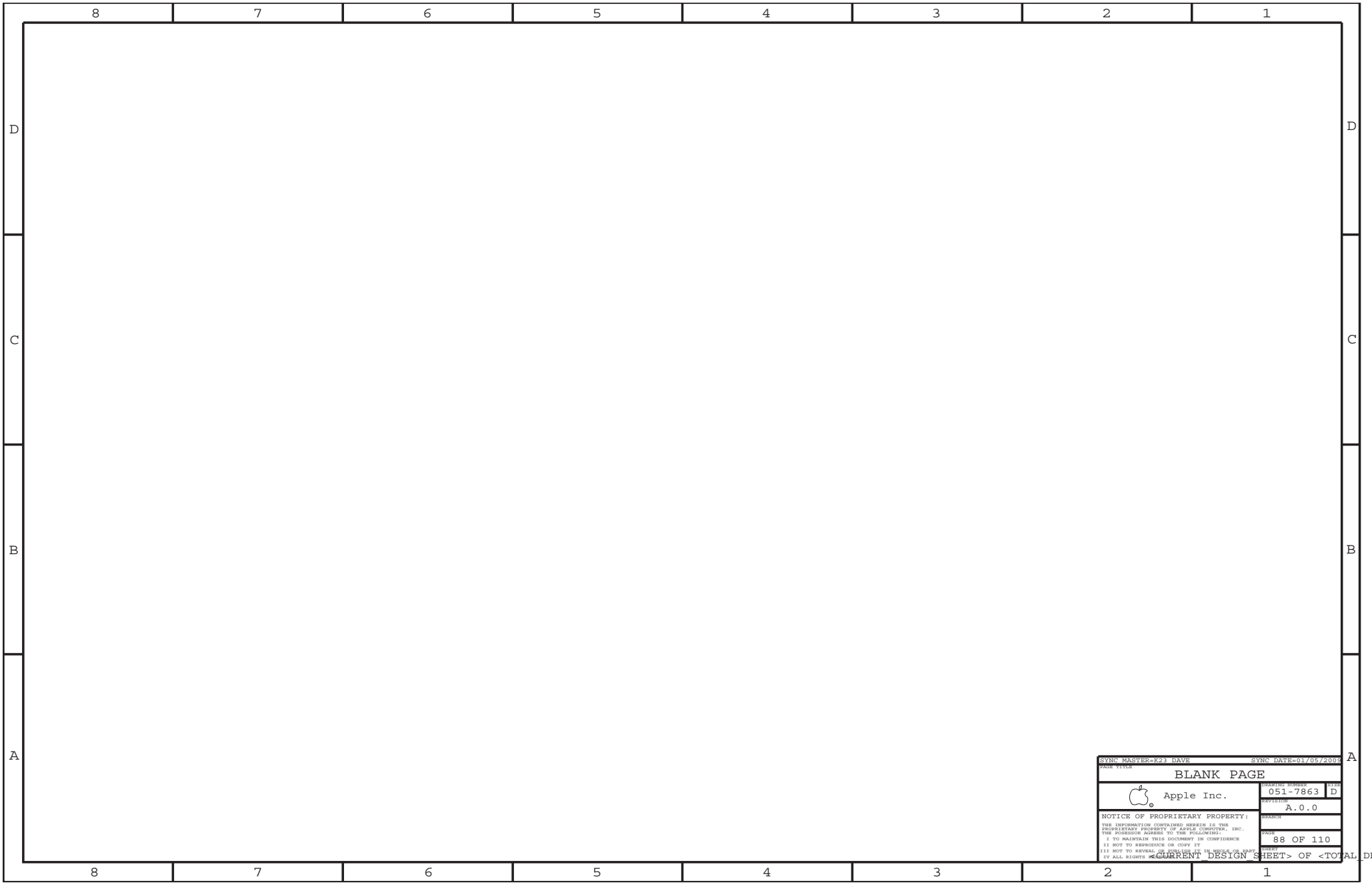
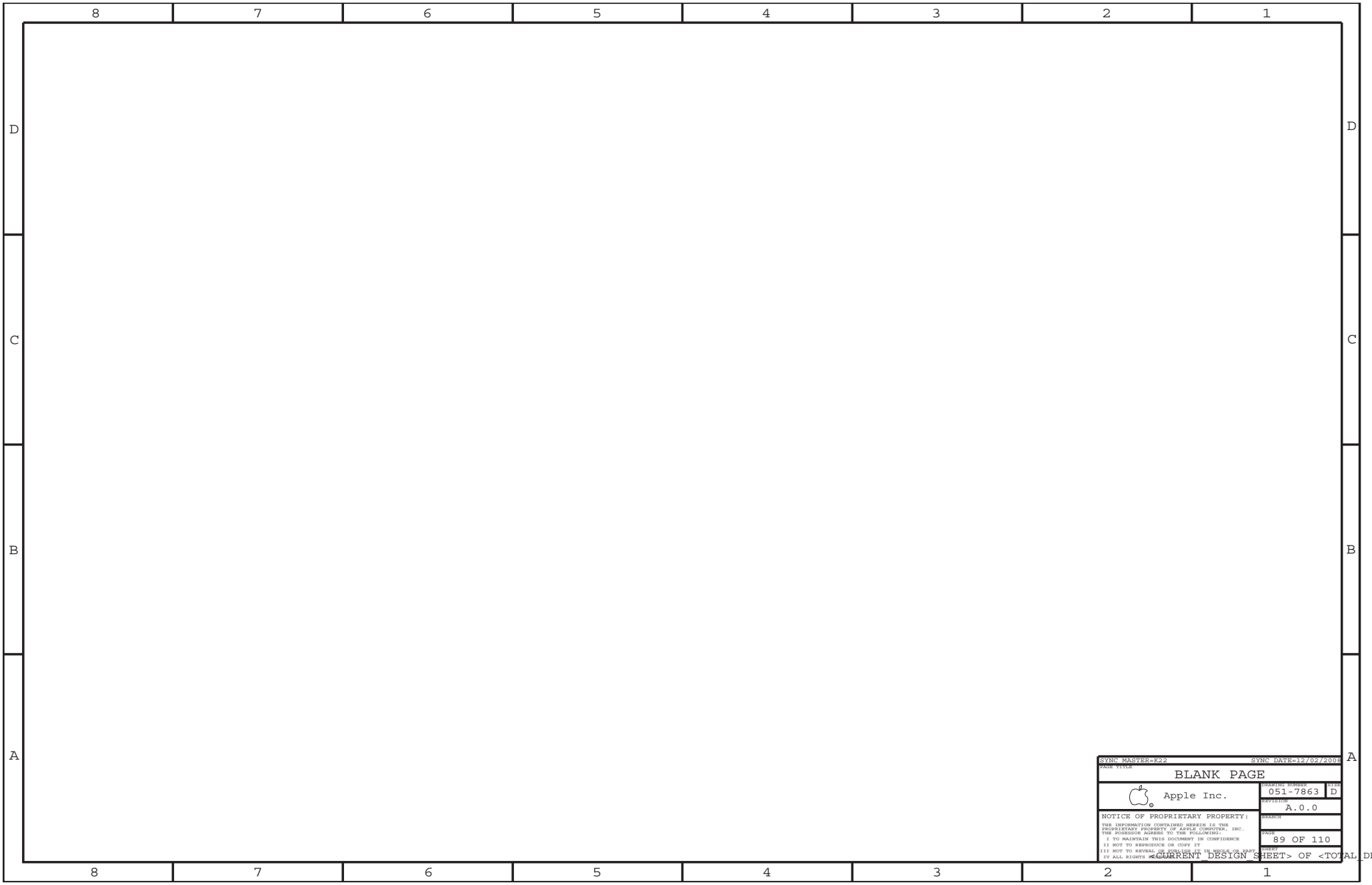




Page Notes

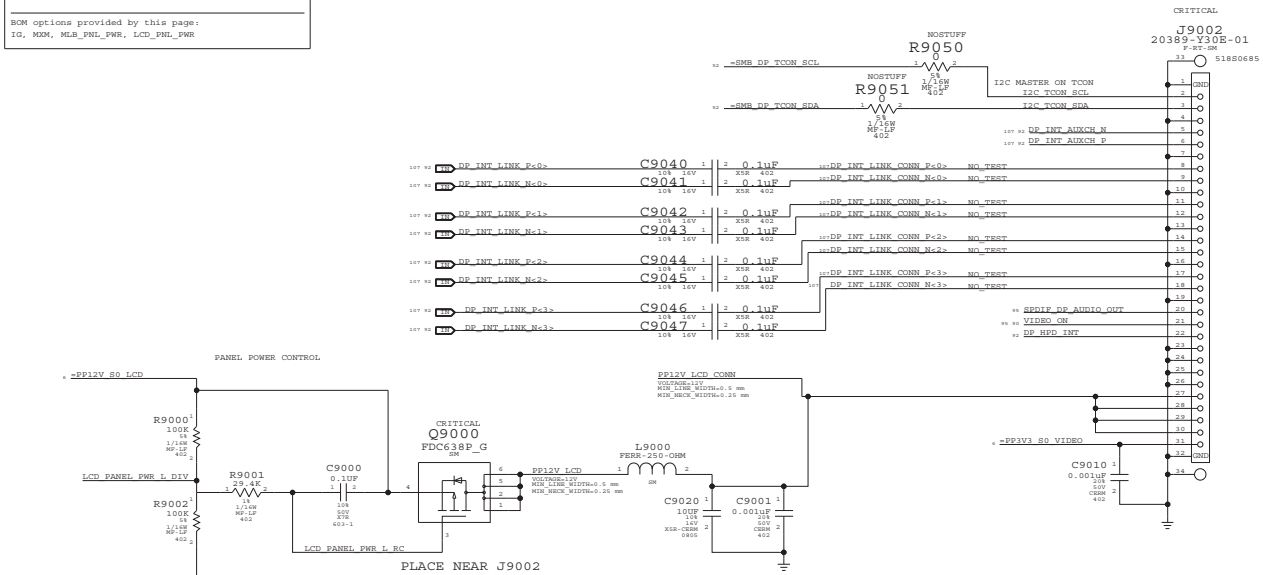
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

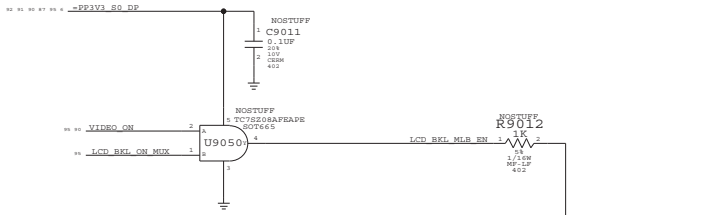
BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

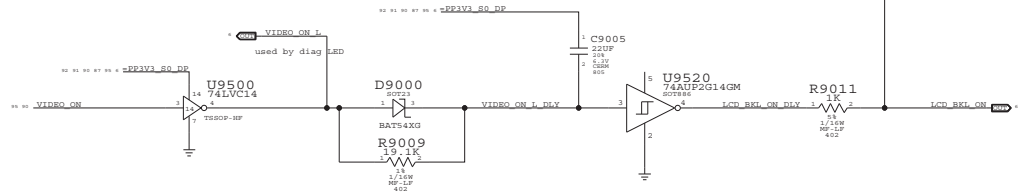
INTERNAL DP INTERFACE



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video
Options for GPU or MLB HW controlled backlight enable are included





buffers are multiple parts, other parts are on csa 95

SYNC MASTER=MARKVIDEO SYNC DATE=03/12/2008

PAGE TITLE
Display: Int DP Connector

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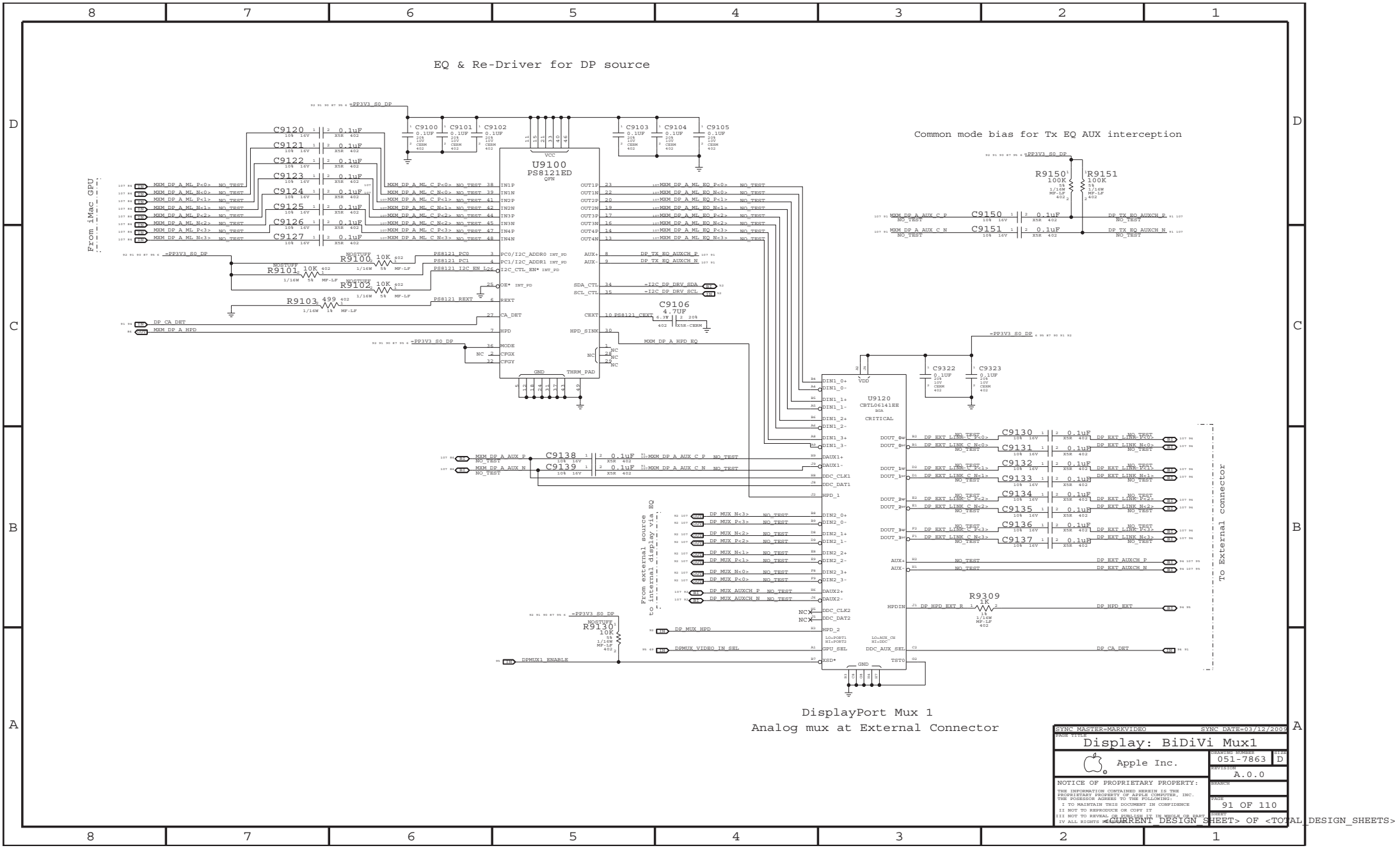

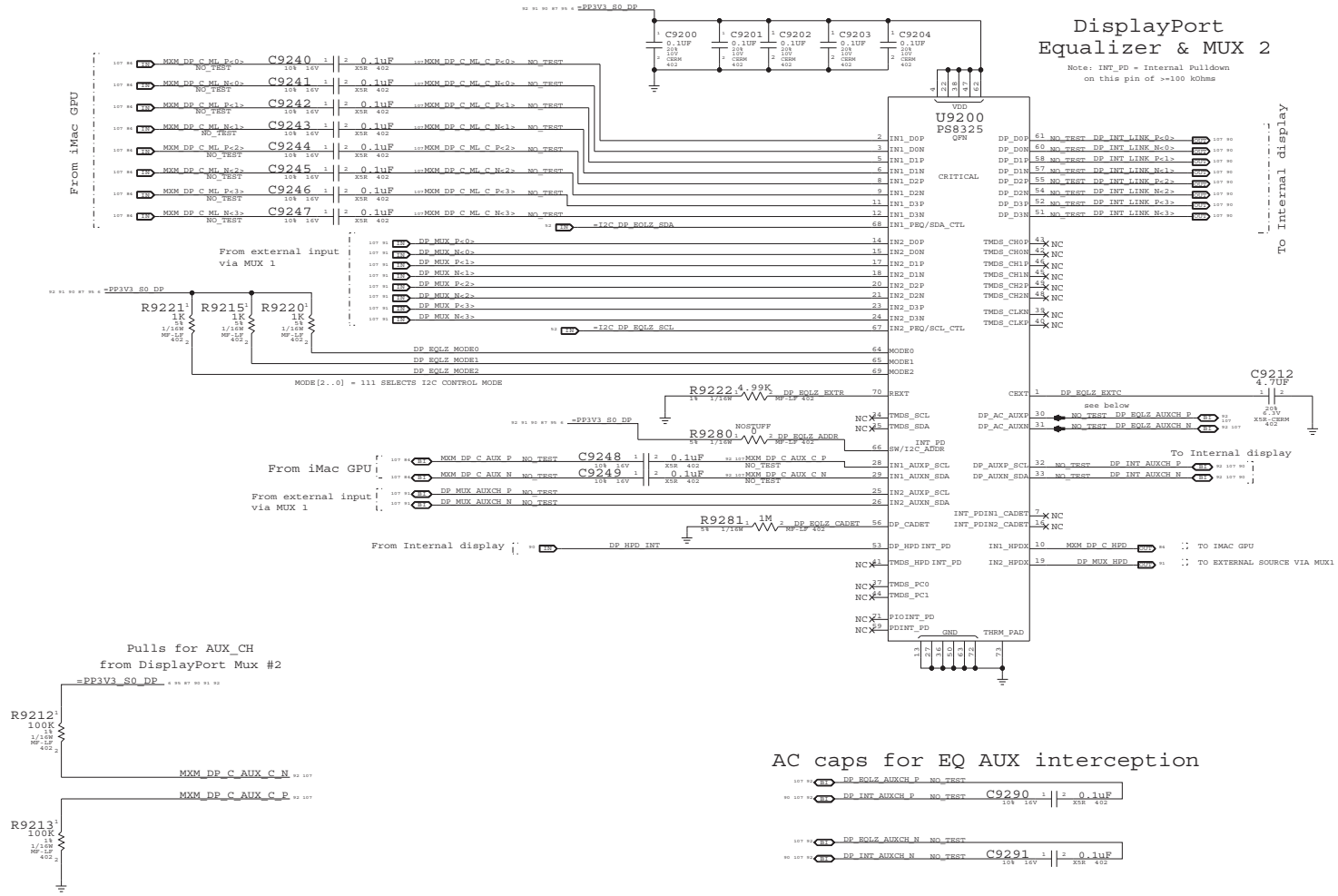

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE	BIDIVI DP MUX2
Apple Inc.	DRAWING NUMBER 051-7863 D
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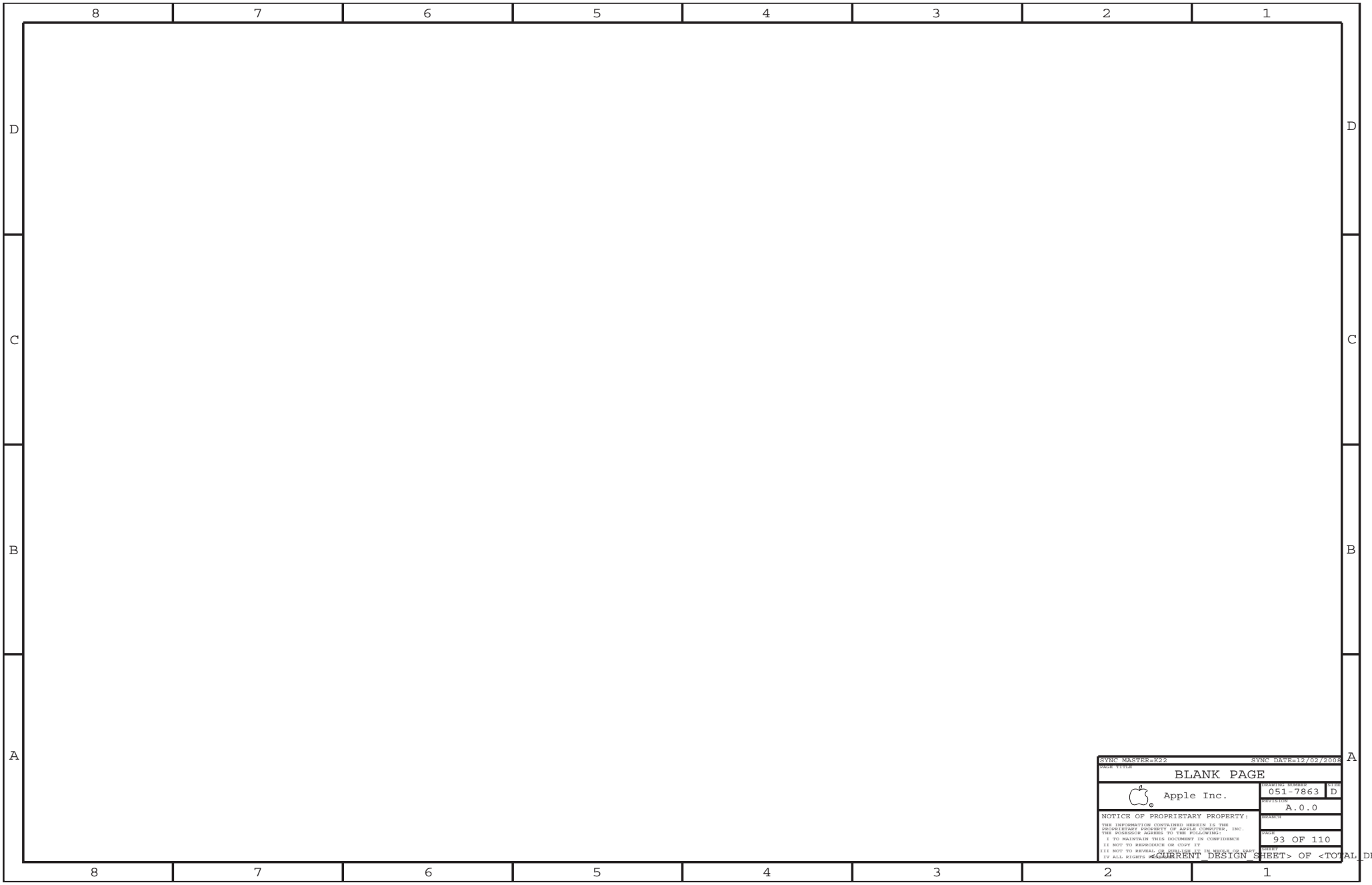

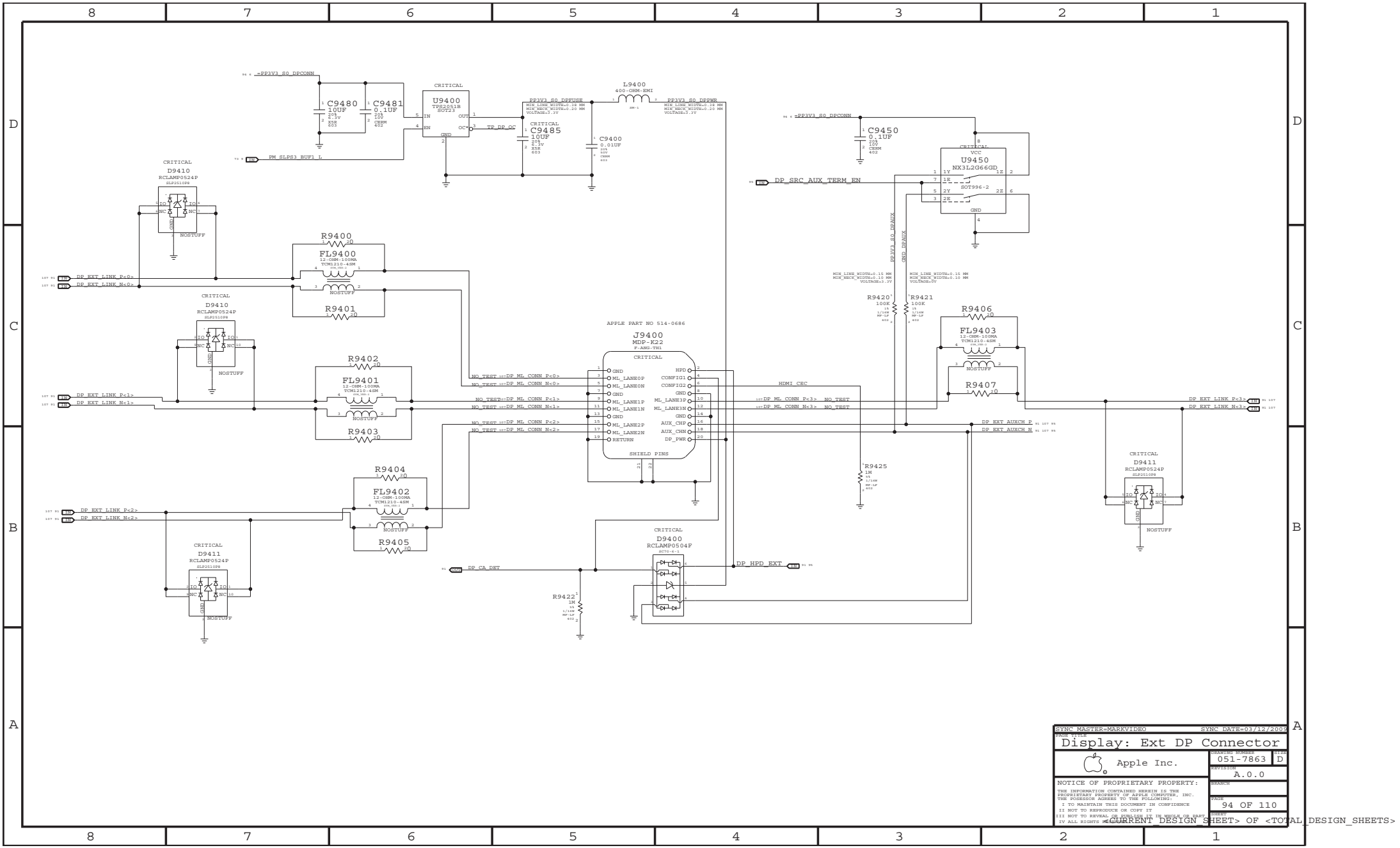

SYNC MASTER=MARKVIDEO SYNC DATE=03/12/2008

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Display: Ext DP Connector

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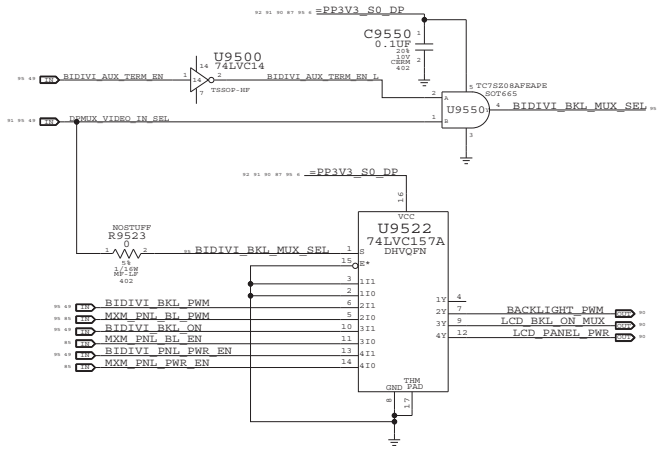
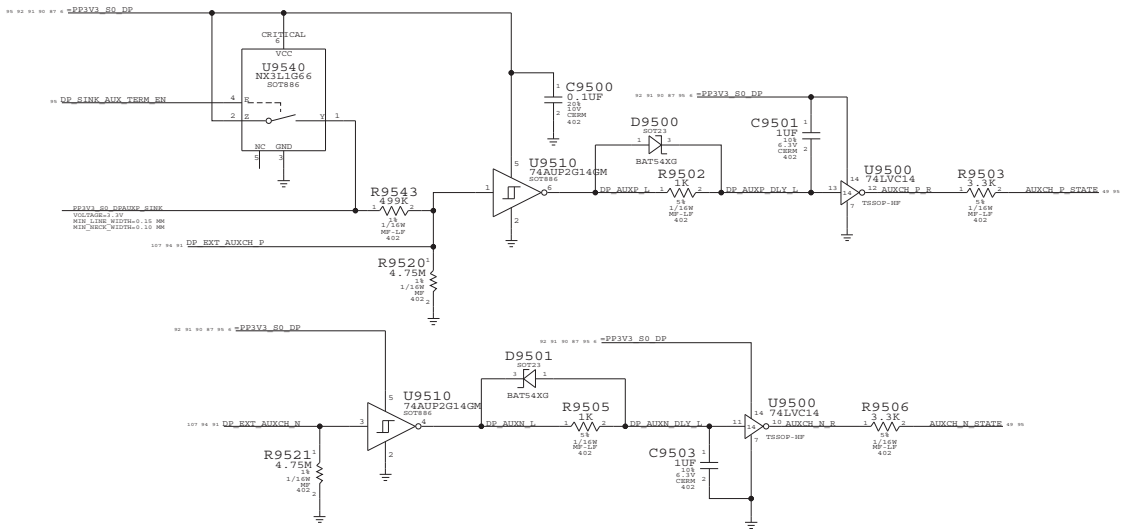
PANEL/BACKLIGHT CONTROL MUX

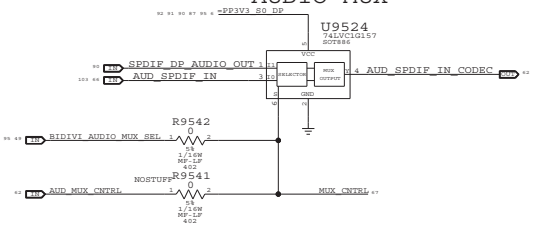


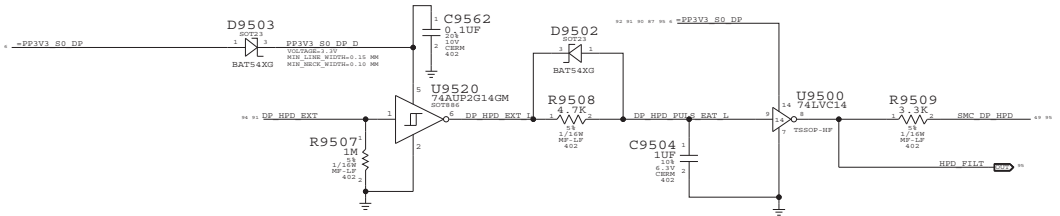
External AUX Channel and HPD Buffers & filters



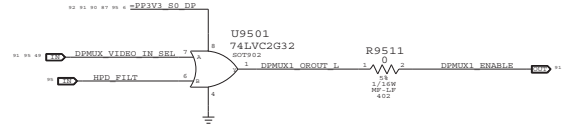
DisplayPort AUDIO MUX

PLACE NEAR U6201



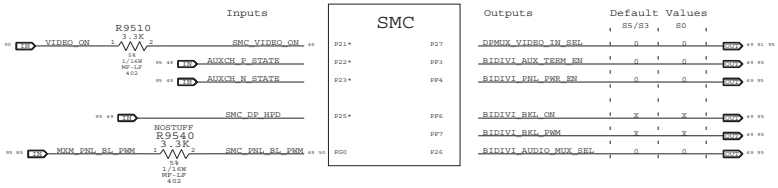


BiDiVi MUX Enable

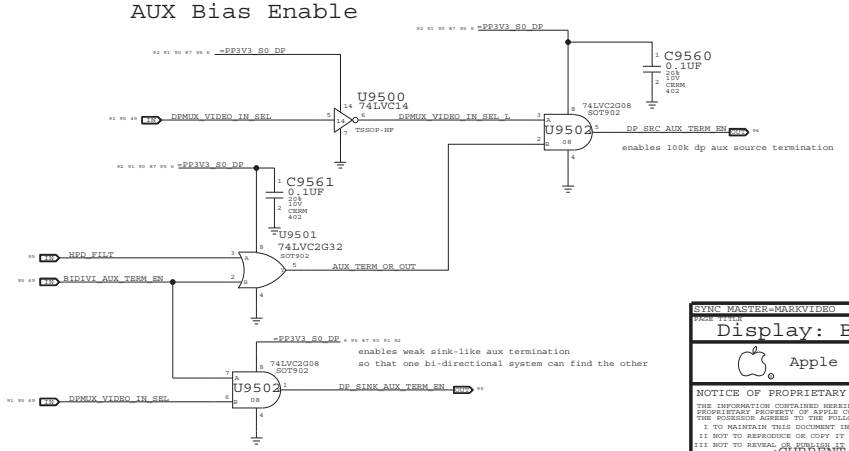


*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

SMC Signals for BiDiVi



AUX Bias Enable



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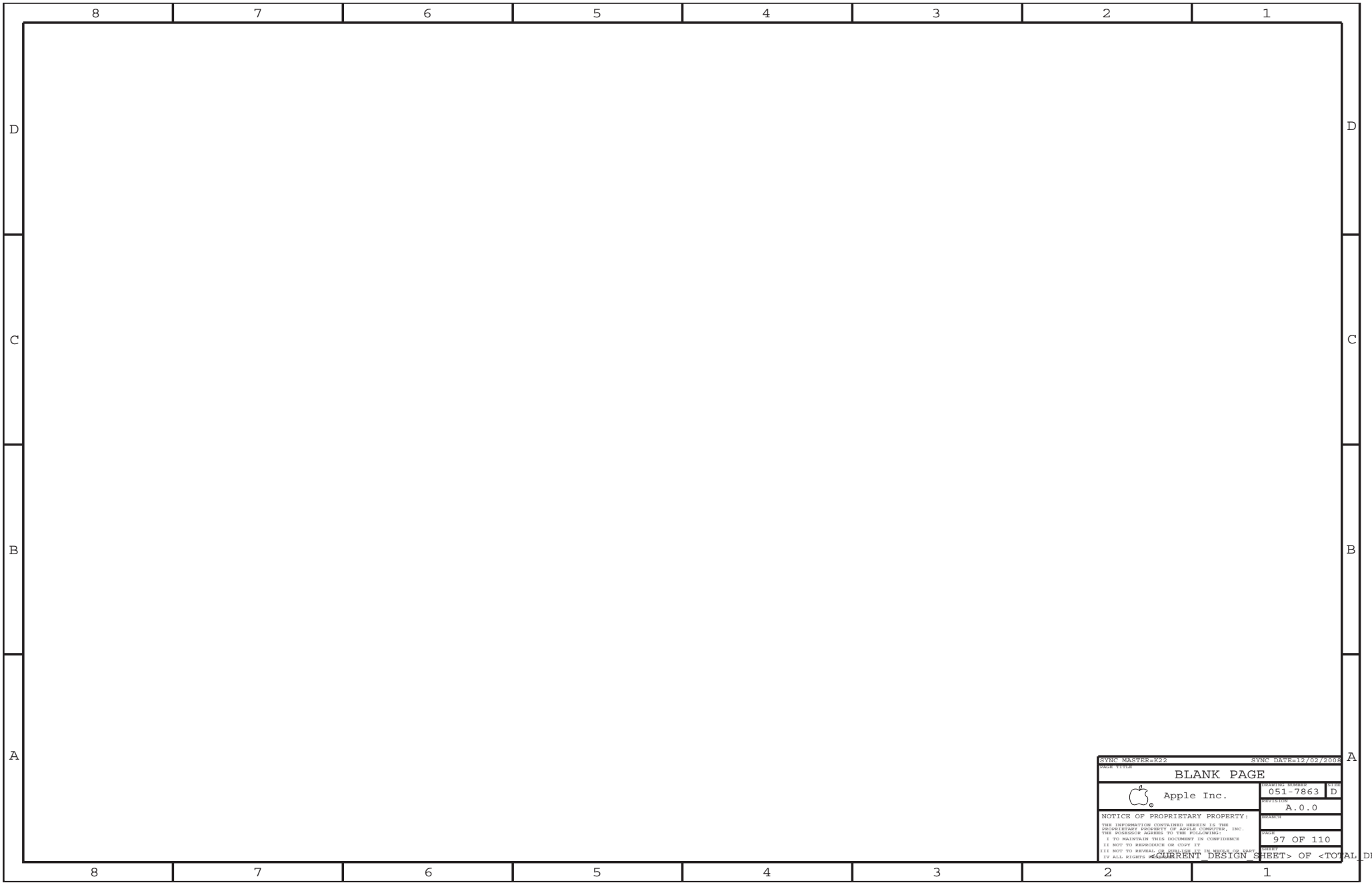

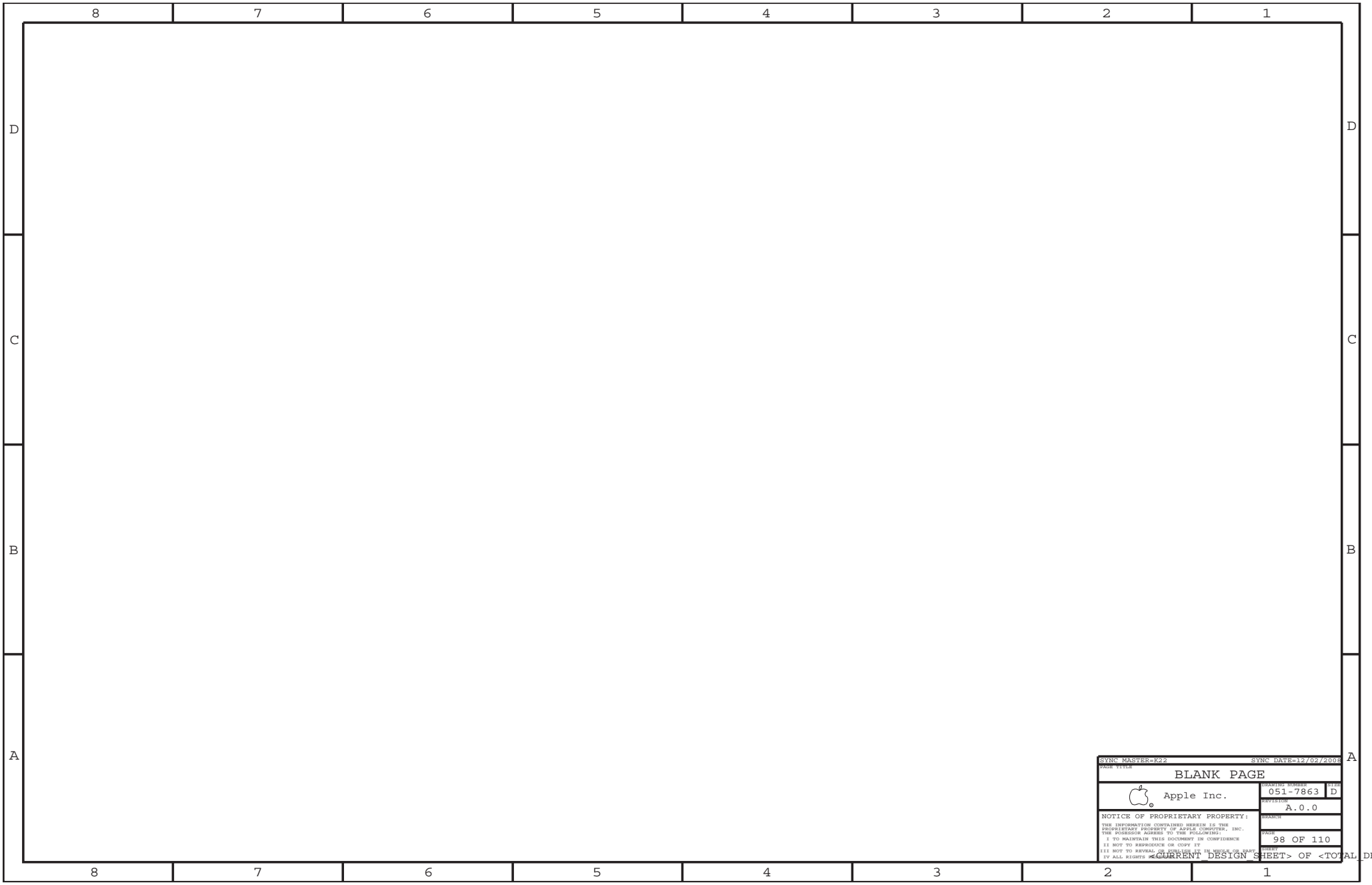

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighther than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

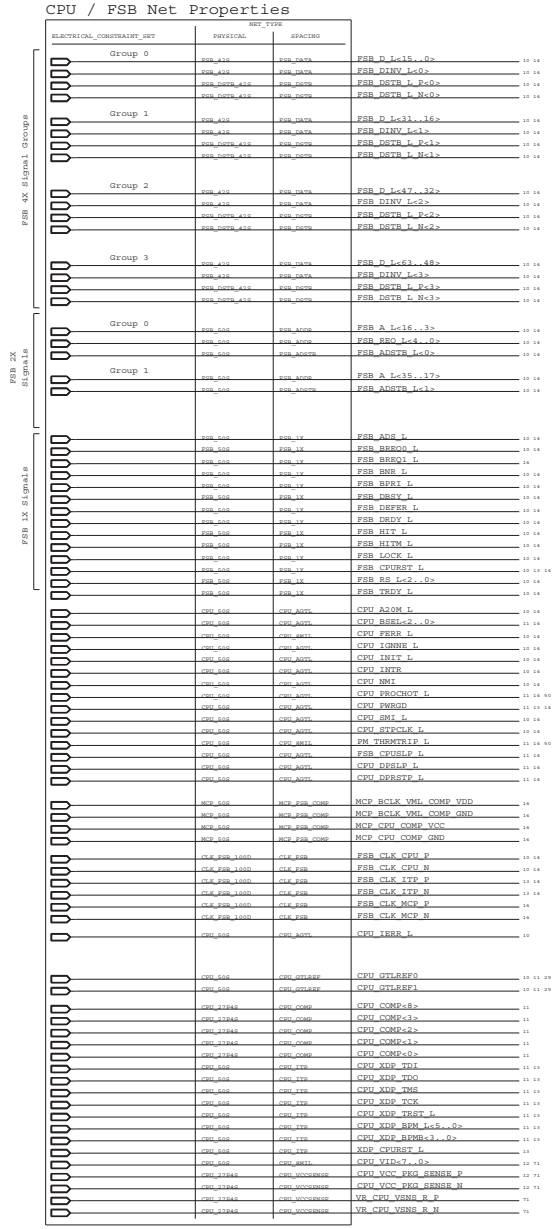
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties



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CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4GS	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_4GS_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

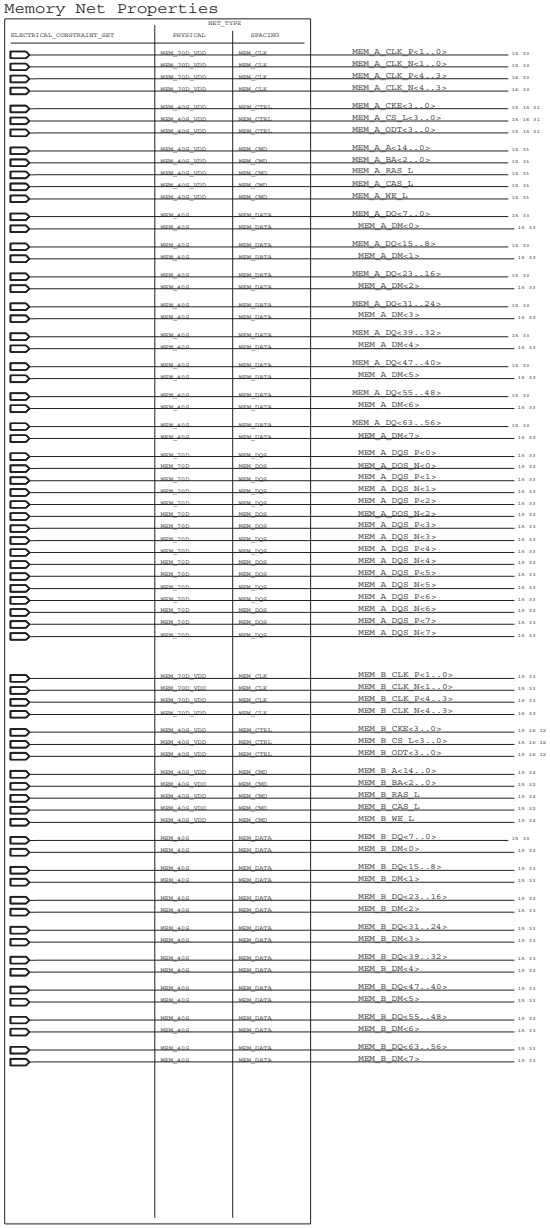
MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

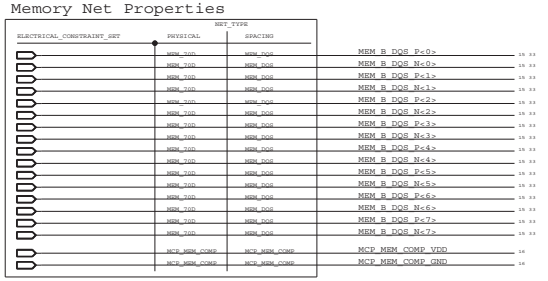
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties



Memory Net Properties



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Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE GRAPHICS			
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>
	PCIE_90D	PCIE	PEG_D2R_P<15..0>
	PCIE_90D	PCIE	PEG_D2R_N<15..0>
	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>
	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..0>
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>
PCIE I/O			
	PCIE_90D	PCIE	PCIE_MINI_R2D_P
	PCIE_90D	PCIE	PCIE_MINI_R2D_N
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_P
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_N
	PCIE_90D	PCIE	PCIE_MINI_D2R_P
	PCIE_90D	PCIE	PCIE_MINI_D2R_N
	PCIE_90D	PCIE	PCIE_FW_R2D_P
	PCIE_90D	PCIE	PCIE_FW_R2D_N
	PCIE_90D	PCIE	PCIE_FW_R2D_C_P
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N
	PCIE_90D	PCIE	PCIE_FW_D2R_P
	PCIE_90D	PCIE	PCIE_FW_D2R_N
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N
PCIE REF CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N
SATA			
	SATA_100D	SATA	SATA_HDD_R2D_C_P
	SATA_100D	SATA	SATA_HDD_R2D_C_N
	SATA_100D	SATA	SATA_HDD_R2D_P
	SATA_100D	SATA	SATA_HDD_R2D_N
	SATA_100D	SATA	SATA_HDD_D2R_P
	SATA_100D	SATA	SATA_HDD_D2R_N
	SATA_100D	SATA	SATA_HDD_D2R_C_P
	SATA_100D	SATA	SATA_HDD_D2R_C_N
	SATA_100D	SATA	SATA_ODD_R2D_C_P
	SATA_100D	SATA	SATA_ODD_R2D_C_N
	SATA_100D	SATA	SATA_ODD_R2D_P
	SATA_100D	SATA	SATA_ODD_R2D_N
	SATA_100D	SATA	SATA_ODD_D2R_P
	SATA_100D	SATA	SATA_ODD_D2R_N
	SATA_100D	SATA	SATA_ODD_D2R_C_P
	SATA_100D	SATA	SATA_ODD_D2R_C_N
	MCP_SOS	SATA_TERMP	MCP_SATA_TERMP
MISC			
	MCP_SOS	MCP_PEX_COMP	MCP_PEX_CLK_COMP
	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET
	MCP_SOS	MCP_PEX_COMP	MCP_IFPAB_VPROBE
			PM_SLP_S3_L
			PM_SLP_S4_L

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_5S	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_5S	PCI	PCI_REQ0_L	19
	PCI_5S	PCI	PCI_REQ1_L	19
	CLK_PCI_5S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_5S	CLK_PCI	PCI_CLK33M_MCP	19
	LPC_5S	LPC	LPC_AD<3..0>	19 49 51
	LPC_5S	LPC	LPC_AD_R<3..0>	19
	LPC_5S	LPC	LPC_FRAME_L	19 49 51
	LPC_5S	LPC	LPC_FRAME_R_L	19
	LPC_5S	LPC	LPC_RESET_L	9 19
	CLK_LPC_5S	CLK_LPC	LPC_CLK33M_SMC_R	9 19
	CLK_LPC_5S	CLK_LPC	LPC_CLK33M_SMC	9 49
	CLK_LPC_5S	CLK_LPC	LPC_CLK33M_LPCPLUS	9 51
	CLK_LPC_5S	CLK_LPC	PM_CLK32K_SUSCLK_R	9 21
	CLK_LPC_5S	CLK_LPC	PM_CLK32K_SUSCLK	9 49
	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
	USB_90D	USB	USB_EXTA_P	20 46
	USB_90D	USB	USB_EXTA_N	20 46
	USB_90D	USB	USB_PORT0_P	46
	USB_90D	USB	USB_PORT0_N	46
	USB_90D	USB	USB_EXTB_P	20 46
	USB_90D	USB	USB_EXTB_N	20 46
	USB_90D	USB	USB_PORT1_P	46
	USB_90D	USB	USB_PORT1_N	46
	USB_90D	USB	USB_EXTC_P	20 46
	USB_90D	USB	USB_EXTC_N	20 46
	USB_90D	USB	USB_PORT2_P	46
	USB_90D	USB	USB_PORT2_N	46
	USB_90D	USB	USB_EXTD_P	20 46
	USB_90D	USB	USB_EXTD_N	20 46
	USB_90D	USB	USB_D_MUXED_P	46
	USB_90D	USB	USB_D_MUXED_N	46
	USB_90D	USB	USB_PORT3_P	46
	USB_90D	USB	USB_PORT3_N	46
	USB_90D	USB	USB_CAMERA_P	20 47
	USB_90D	USB	USB_CAMERA_N	20 47
	USB_90D	USB	USB_CAMERA_L_P	47 110
	USB_90D	USB	USB_CAMERA_L_N	47 110
	USB_90D	USB	USB_BT_P	20 47
	USB_90D	USB	USB_BT_N	20 47
	USB_90D	USB	USB_BT_L_P	47 110
	USB_90D	USB	USB_BT_L_N	47 110
	USB_90D	USB	USB_IR_P	20 47
	USB_90D	USB	USB_IR_N	20 47
	USB_90D	USB	USB_IR_L_P	47 110
	USB_90D	USB	USB_IR_L_N	47 110
	USB_90D	USB	USB_SDCARD_P	20 47
	USB_90D	USB	USB_SDCARD_N	20 47
	USB_90D	USB	USB_SDCARD_L_P	47 110
	USB_90D	USB	USB_SDCARD_L_N	47 110
	MCP_5S	SPI	SPI_CLK_R	21 51 61
	MCP_5S	SPI	SPI_CLK	61
	MCP_5S	SPI	SPI_MOSI_R	21 51 61
	MCP_5S	SPI	SPI_MOSI	61
	MCP_5S	SPI	SPI_MISO	21 51 61
	MCP_5S	SPI	SPI_MISO_R	61
	MCP_5S	SPI	SPI_CS0_R_L	21 51
	MCP_5S	SPI	SPI_CS0_L	51
	HDA_5S	HDA	HDA_BIT_CLK	21 62
		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
	HDA_5S	HDA	HDA_BIT_CLK_R	21
	HDA_5S	HDA	HDA_RST_L	21 62
	HDA_5S	HDA	HDA_RST_R_L	21
	HDA_5S	HDA	HDA_SDOUT	21 62
	HDA_5S	HDA	HDA_SDOUT_R	21
	HDA_5S	HDA	HDA_SYNC	21 62
	HDA_5S	HDA	HDA_SYNC_R	21
	HDA_5S	HDA	HDA_SDIN0	21 62
	HDA_5S	HDA	AUD_SDI_R	62
		HDA	AUD_SPDIF_IN	9 66
		HDA	AUD_SPDIF_OUT	62 66
		HDA	AUD_SPDIF_CHIP	62
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN	21 28

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

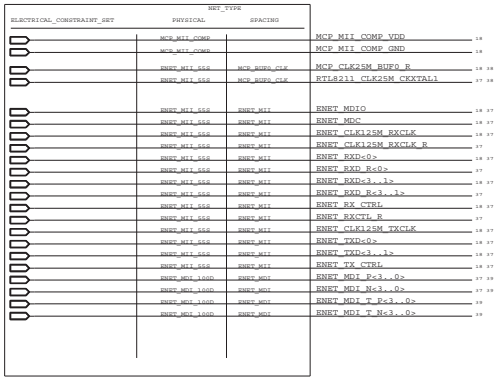
SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4



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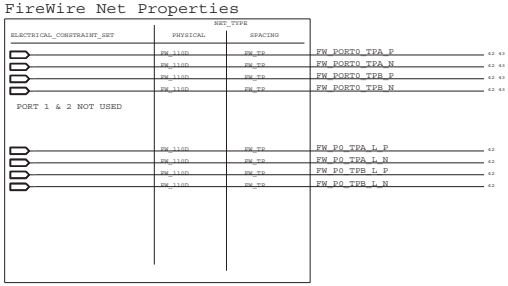
FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties



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SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_555	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	7

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	SMB_555	SMB	SMBUS_SMC_A_S3_SCL
	SMB_555	SMB	SMBUS_SMC_A_S3_SDA
	SMB_555	SMB	SMBUS_SMC_B_S0_SCL
	SMB_555	SMB	SMBUS_SMC_B_S0_SDA
	SMB_555	SMB	SMBUS_SMC_0_S0_SCL
	SMB_555	SMB	SMBUS_SMC_0_S0_SDA
	SMB_555	SMB	SMBUS_SMC_BSA_SCL
	SMB_555	SMB	SMBUS_SMC_BSA_SDA
	SMB_555	SMB	SMBUS_SMC_MGMT_SCL
	SMB_555	SMB	SMBUS_SMC_MGMT_SDA
	SMB_555	SMB	SMBUS_SMC_MGMT_SCL
	SMB_555	SMB	SMBUS_SMC_MGMT_SDA
	SMB_555	SMB	SMBUS_MCP_0_CLK
	SMB_555	SMB	SMBUS_MCP_0_DATA

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	3:1_SPACING
DISPLAYPORT	POWER	*	PWR_P2MM
DISPLAYPORT	GND	*	GND_P2MM

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
ASSIGNED IN CONT. MGR.			
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_P
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_N
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_C_P
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_C_N
	DP_100D	DISPLAYPORT	DP_EXT_LINK_P<3..0>
	DP_100D	DISPLAYPORT	DP_EXT_LINK_N<3..0>
	DP_100D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0>
	DP_100D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0>
	DP_100D	DISPLAYPORT	DP_EXT_AUXCH_P
	DP_100D	DISPLAYPORT	DP_EXT_AUXCH_N
	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0>
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_P
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_N
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_C_P
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_C_N
	DP_100D	DISPLAYPORT	DP_INT_LINK_P<3..0>
	DP_100D	DISPLAYPORT	DP_INT_LINK_N<3..0>
	DP_100D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0>
	DP_100D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0>
	DP_100D	DISPLAYPORT	DP_INT_AUXCH_P
	DP_100D	DISPLAYPORT	DP_INT_AUXCH_N
	DP_100D	DISPLAYPORT	DP_MUX_P<3..0>
	DP_100D	DISPLAYPORT	DP_MUX_N<3..0>
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_P
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_N
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_P
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_N
	DP_100D	DISPLAYPORT	DP_TX_EQ_AUXCH_P
	DP_100D	DISPLAYPORT	DP_TX_EQ_AUXCH_N
	DP_100D	DISPLAYPORT	DP_EQLZ_AUXCH_P
	DP_100D	DISPLAYPORT	DP_EQLZ_AUXCH_N
	MCP_DV_COMP		MCP_HDMI_RSET
	MCP_DV_COMP		MCP_HDMI_VPROBE

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	7
PPDDR_MEM	*	=STANDARD	7

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING	
		PPDDR_MEM	=PP1V5_S3_MEM_A 6 30 31
		PPDDR_MEM	=PP1V5_S3_MEM_B 6 30 32
		SWITCHNODE	VR_CPU_SW1 72
		SWITCHNODE	VR_CPU_SW2 72
		SWITCHNODE	VR_CPU_SW3 72
		SWITCHNODE	1V8_SW 80
		SWITCHNODE	1V1S5_SW 79
		SWITCHNODE	PVTTR0_PHASE 76
		SWITCHNODE	3V3S5_SW 76
		SWITCHNODE	SYS3_SW 73
		SWITCHNODE	MCPCORES0_PHASE 74
	THERM_DIFF	THERMAL	SNS_T_DP1_DN6 55
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6 55
	THERM_DIFF	THERMAL	SNS_T_DP2_DN3 55
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3 55
	THERM_DIFF	THERMAL	CPU_THERMD_P 11 55
	THERM_DIFF	THERMAL	CPU_THERMD_N 11 55
	THERM_DIFF	THERMAL	SNS_T_DP4_DN5 55
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P 21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N 21 55
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P 53
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N 53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P 55
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N 55
	THERM_DIFF	THERMAL	SNS_LCD_P 55 110
	THERM_DIFF	THERMAL	SNS_LCD_N 55 110
	THERM_DIFF	THERMAL	SNS_ODD_P 55 110
	THERM_DIFF	THERMAL	SNS_ODD_N 55 110
	THERM_DIFF	THERMAL	SNS_CPU_H_P 55
	THERM_DIFF	THERMAL	SNS_CPU_H_N 55
	THERM_DIFF	THERMAL	SNS_MCP_P 55
	THERM_DIFF	THERMAL	SNS_MCP_N 55
	THERM_DIFF	THERMAL	SNS_AMB_P 55 110
	THERM_DIFF	THERMAL	SNS_AMB_N 55 110
	THERM_DIFF	THERMAL	SNS_MXM_P 55
	THERM_DIFF	THERMAL	SNS_MXM_N 55
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P 71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N 71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P 71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N 71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P 71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N 71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N 71
PD		THERMAL	SMC_CPU_ISENSE 49 53
PD		THERMAL	VR_CPU_IOUT 53 71
PD		THERMAL	VR_ISNS_CPU_P 53
PD		THERMAL	VR_ISNS_CPU_N 53
PD		THERMAL	SNS_PS_CPU_ISNS 53
PD		THERMAL	SMC_CPU_VSENSE 49 53
PD		THERMAL	CPU_VCC_SENSE 12 53
PD		THERMAL	SMC_GPU_VSENSE 49 53
PD		THERMAL	SMC_GPU_ISENSE 49 53
PD		THERMAL	SMC_1V5_S0_ISENSE 50 54
PD		THERMAL	SMC_1V5_S0_ISENSE_R 54
PD		THERMAL	SMC_1V5_S0_VSENSE 50 54
PD		THERMAL	SMC_MCP_CORE_ISENSE 50 54
PD		THERMAL	SMC_MCP_CORE_VSENSE 50 54
PD		THERMAL	MCPCORES0_IMON 54 74
PD		THERMAL	CPU_PECI_L 11 55
PD		THERMAL	SMB_PECI_L 55
PD		THERMAL	CPU_PECI_MCP 14 55
		THERMAL	HDD_OOB_TEMP_FILT 55
PD		THERMAL	HDD_OOB_TEMP 55
PD		THERMAL	HDD_OOB_TEMP_R 55
PD		THERMAL	SMC_HDD_OOB_TEMP 55

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K22/K23 SPECIFIC CONSTRAINTS

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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	16.6.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

- USB_CAMERA_L_P
- USB_CAMERA_L_N

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

- USB_SDCARD_L_P
- USB_SDCARD_L_N

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

- USB_BT_L_P
- USB_BT_L_N

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

- USB_IR_L_P
- USB_IR_L_N

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

- SATA_ODD_R2D_P
- SATA_ODD_R2D_N
- SATA_ODD_D2R_C_N
- SATA_ODD_D2R_C_P
- SMC_ODD_DETECT

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

- SATA_HDD_R2D_P
- SATA_HDD_R2D_N
- SATA_HDD_D2R_C_N
- SATA_HDD_D2R_C_P

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

- SNS_LCD_P
- SNS_LCD_N

J5521 AMBIENT TEMP SENSOR

- SNS_AMB_P
- SNS_AMB_N

J5551 ODD TEMP SENSOR

- SNS_ODD_P
- SNS_ODD_N

J5600 ODD FAN

- FAN_0_PWR_L
- FAN_TACH0_L
- PP12V_S0_FAN0_L
- FAN_0_GND

J5700 CPU FAN

- FAN_2_PWR_L
- FAN_TACH2_L
- PP12V_S0_FAN2_L
- FAN_2_GND

J5601 HD FAN

- FAN_1_PWR_L
- FAN_TACH1_L
- PP12V_S0_FAN1_L
- FAN_1_GND

J6601 AUDIO MICROPHONE

- AUD_MIC_IN1_N_CONN
- GND_AUDIO_MIC1_CONN
- AUD_MIC_IN1_P_CONN

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

- AUD_SPKR_OUTLO2R_P
- AUD_SPKR_OUTLO2R_N
- AUD_SPKR_OUTLO1R_P
- AUD_SPKR_OUTLO1R_N

J6603 AUDIO LEFT SPEAKER

- AUD_SPKR_OUTLO2L_P
- AUD_SPKR_OUTLO2L_N
- AUD_SPKR_OUTLO1L_P
- AUD_SPKR_OUTLO1L_N

GND — MIN_ALLOWED_TPS=15
PP3V3_S3 — MIN_ALLOWED_TPS=2
PP5V_S3_REG — MIN_ALLOWED_TPS=2
PP5V_S0 — MIN_ALLOWED_TPS=1

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