1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K23

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
A	0000774489	PRODUCTION RELEASED	2009-08-20

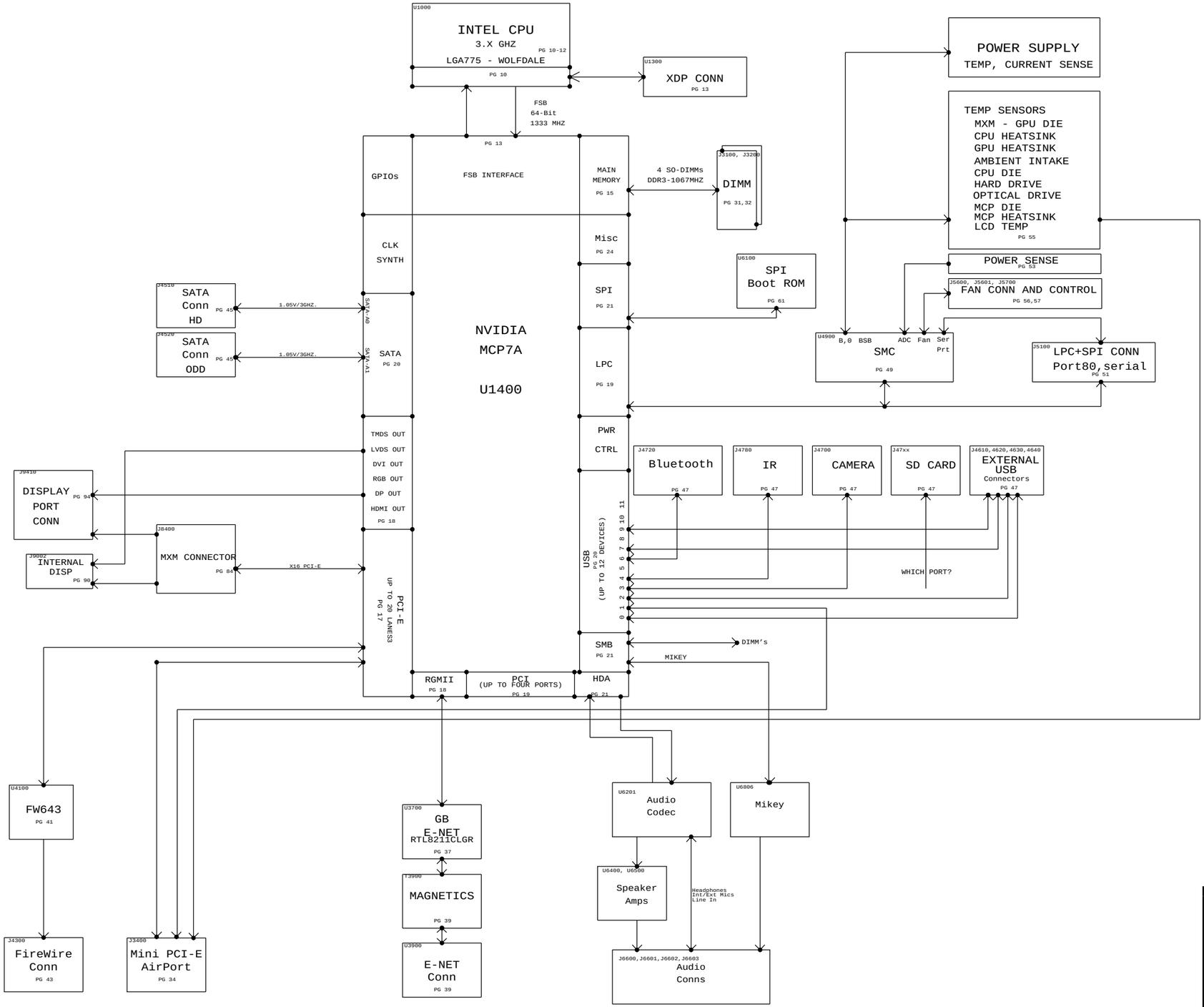
LAST_MODIFIED=Wed Sep 2 16:45:56 2009

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Wed Sep 2 16:45:56 2009

DRAWING TITLE: SCH,K23,MLB

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 110

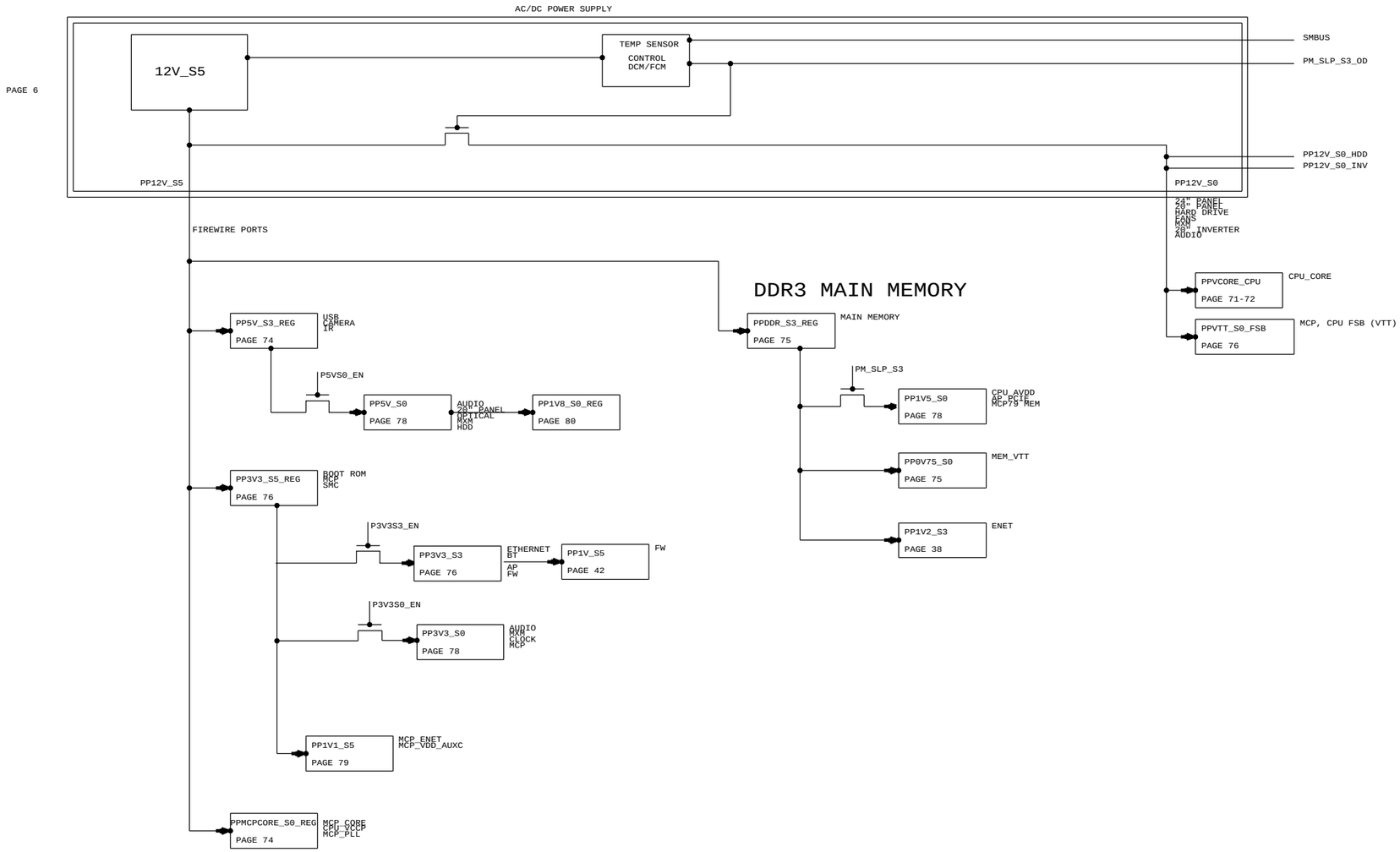


SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
System Block Diagram

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 2 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-7863

SIZE D

REVISION A.0.0

BRANCH

PAGE 3 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9879	PCBA,MLB,BETTER,K23	K23,2P80GHZ_CPU,BASIC,MXM,K23_MXM
639-0394	PCBA,MLB,2.80 GHZ-2M,K23	K23,2P80GHZ_2M_CPU,BASIC,MXM,K23_MXM
639-0185	PCBA,MLB,2.93 GHZ,K23	K23,2P93GHZ_CPU,BASIC,MXM,K23_MXM
639-9983	PCBA,MLB,BEST,K23	K23,3P0GHZ_CPU,BASIC,MXM,K23_MXM
639-0509	PCBA,MLB,3.06 GHZ,K23	K23,3P06GHZ_CPU,BASIC,MXM,K23_MXM
639-0109	PCBA,MLB,3.16 GHZ,K23(INVESTIGATION)	K23,3P16GHZ_CPU,BASIC,MXM,K23_MXM
630-9880	PCBA,MLB,ULTIMATE,K23	K23,3P33GHZ_CPU,BASIC,MXM,K23_MXM
607-4427	PCBA,MLB,DEV,K23	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP7A,XDP,BETTER,MCP_ISL9563A,PRODUCTION
MCP7A	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP
DEV_GROUP	XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE,MCP_CPU_TDIODE,PECI_SMB,MOJOMUX

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0731	1	IC,GMCP,MCP7A-JA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	IG
338S0732	1	IC,MCP,MCP7A-DA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	MXM
341T0170	1	IC,EFI BOOTROM,K22/K23	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B,167BGA	U4100	CRITICAL	
338S0694	1	IC,RTL8251CA,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

MCP -J SKU HAS INTEGRATED GPU
MCP -D SKU DOES NOT

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3745	1	WLF,QXXX,QS,2.80G,65W,1066,R0,3M,LGA	CPU	CRITICAL	2P80GHZ_CPU
337S3742	1	WLF,SLB9J,PRQ,2.83G,65W,1333,E0,6M,LGA	CPU	CRITICAL	2P83GHZ_CPU
337S3726	1	WLF,SLB9J,PRQ,3.0G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P0GHZ_CPU
337S3715	1	WLF,SLB9K,PRQ,3.16G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P16GHZ_CPU
337S3727	1	WLF,SLB9L,PRQ,3.33G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P33GHZ_CPU
337S3807	1	WLF,SLB9L,PRQ,2.93G,65W,1333,E0,6M,LGA	CPU	CRITICAL	2P93GHZ_CPU
337S3766	1	WLF,SLB9L,PRQ,3.06G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P06GHZ_CPU
337S3804	1	WLF,SLGU9,PRQ,2.80G,65W,1066,R0,2M,LGA	CPU	CRITICAL	2P80GHZ_2M_CPU

K23 PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7863	1	SCH,K23,MLB	SCH1		K23
	820-2507	1	PCBF,K23,MLB	MLB1		K23
(338S0489 - BLNK)	341T0169	1	IC,SMC,K23	U4900	CRITICAL	K23

ALTERNATES

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 4 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=12/05/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 5 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

52 =SMB_ACDC_SCL
45 6 =PP5V_S0_SATA
6 PP12V_S5
90 LCD_PWM

=SMB_ACDC_SDA 52
PP12V_S0 70 6
LCD_BKL_ON 90

C623 10UF 20% 10V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
70 50 49 9 EN PM_SLPS3_BUF2_L

Q610 2N7002 SOT23-HF1
C600 0.001UF 10% 50V X7R 402

110 6 78 PP3V3_S3
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT LED605 GREEN-3.6MCD 2.0X1.25MM-SM

6 76 PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:1

110 6 78 PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:2
CORE_VOLTAGES_ON
70 EN ALL_SYS_PWRGD_R
Q602 2N7002DW-X-G SOT-363

6 78 PP3V3_S0
R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
LED604 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:3
GPU_PRESENT_DRAIN
9 EN MXM_GOOD
Q602 2N7002DW-X-G SOT-363

6 78 PP3V3_S0
R603 1K 5% 1/16W MF-LF 402
LCD_SHOULD_ON
LED603 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:4
90 EN VIDEO_ON_L
sourced from buffer on csa 90

"S0" RAILS
ONLY ON IN RUN

75 PPVTT_S0_DDR_LDO
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP0V75_S0_MEM_VTT_A 31
=PP0V75_S0_MEM_VTT_B 32
=PPVTT_S0_VTTCLAMP 78

72 71 PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU 12

54 74 PPMCPCORE_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_MCP 22 25
=PP1V05_S0_MCP_AVDD_UF 25
=PP1V05_S0_MCP_PEX_DVDD 25 28
=PP1V05_S0_MCP_PLL_UF 25
=PP1V05_S0_MCP_SATA_DVDD0 28 20
=PP1V05_S0_MCP_HDMI_VDD_R 26

76 PPVTT_S0_FSB_REG
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_CPU 10 50 55 71
=PPVTT_S0_FSB_CPU 11 12
=PPVTT_S0_XDP 13
=PP1V05_S0_MCP_FSB 14 22 25

54 PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_VCCPLL 12
=PP1V8R1V5_S0_MCP_MEM 16 25 30
=PP1V5_S0_AUD_DIG 62
=PP1V5_FWRS0_FWXIO 41

PP1V8_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3R1V8_S0_MCP_IFP_VDD_R 26
=PP1V8_S0_PGCMP 70

6 78 PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FAN 56 57
=PP3V3_S0_MCP 21 22 25
=PP3V3_S0_MCP_VPLL_UF 26
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_MCP_PLL_UF 25
=PPSPD_S0_MEM_A 31
=PPSPD_S0_MEM_B 32
=PP3V3_S0_VRD 71
=PP3V3_S0_AUDIO 62 64 65 66 67 68
=PP3V3R1V5_S0_MCP_HDA 21 25
=PP3V3_S0_SMBUS 52
=PP3V3_S0_SMC_LS 50 55
=PP3V3_S0_SMBUS_SMC_0_S0 52
=PP3V3_S0_SMBUS_SMC_B_S0 52
=PP3V3_S0_SMBUS_SMC_MGMT 52
=PP3V3_S0_DPCONN 94
=PP3V3_S0_TSENS 55
=PP3V3_S0_MXM 85 84
=PP3V3_S0_XDP 13
=PP3V3_S0_ODD 45
=PP3V3_S0_SATALED 45
=PP3V3_S0_SMC 50 53 54
=PP3V3_S0_PWRCTL 78
=PP3V3_S0_MCPTHMSNS 55
=PP3V3_S0_VIDEO 90
=PP3V3_FW_FWPHY 41 42 43
=PP3V3_FWRS0_FWXIO 41
=PP3V3_S0_DP 95 87 90 91 92

110 78 PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S0_LPCPLUS 51
=PP5V_S0_AUDIO 62 68
=PP5V_S0_SATA 6 45
=PP5V_S0_MXM 84
=PP5V_S0_VRD 71
=PP5V_S0_DP_AUX_MUX
=PP5V_S0_ISENSE 53
=PP5V_S0_PWRCTL

6 70 PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S0_FAN 56 57
=PP12V_S0_AUDIO_SPKRAMP 67
=PP12V_S0_VRD 70 71
=PPV_S0_MXM_PWR 53
=PPVIN_S0_PPVTT_FSB 76
=PP12V_S0_LCD 90
=PPVIN_S0_MCPCORE 74

"S3" RAILS
ON IN RUN AND SLEEP

75 PPDDR_S3_REG
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PPDDR_MEM
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_A 108 30 31
=PP1V5_S3_MEM_B 108 30 32
=PP1V5_S3_MEMRESET 33
=PPDDR_S3_S0FET 78
=PPDDR_S3_PGCMP 70

75 PPVTT_S3_DDR_BUF
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 mm
=PPVTT_S3_DDR_BUF 29

110 6 78 PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_MINI 34
=PP3V3_S3_BT 47
=PP3V3_S3_VREFMRGN 29
=PP3V3_S3_SDCARD 47
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_SMC 50
=PP3V3_S3_SMBUS_SMC_A_S3 52
=PP3V3_S3_MCPREG 74

110 73 PP5V_S3_REG
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S3_DDRREG 75
=PP5V_S3_USB 46
=PP5V_S3_VTTCLAMP 78
=PP5V_S3_PWRCTL 70
=PP5V_S3_S0FET 78
=PP5V_S3_MCPREG 74
=PP5V_S3_CAMERA 47
=PP5V_S3_IR 47
=PP5V_S3_1V8

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

79 PP1V1_S5_REG
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S5_MCP_VDD_AUXC 22 25
=PP1V1_S5_ENET_FET 38

6 76 PP3V3_S5_REG
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_MCP 22 25
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_S5_SMC 49 50
=PP3V3_S5_ROM 51 61
=PP3V3_S5_RTC_D 28
=PP3V3_S5_LPCPLUS 51
=PP3V3_S5_SMBUS_SMC_BSA 52
=PP3V3_S5_SMCUSBMUX 46
=PP3V3_S5_MEMRESET 33
=PP3V3_S5_P1V1S5 79
=PP3V3_S5_PWRCTL 70
=PP3V3_S5_S3FET 78
=PP3V3_S5_S0FET 78
=PP3V3_S5_ENET_FET 38

76 PP5V_S5_LDO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S5_AVREF 50

6 PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FW 43
=PPVIN_S5_DDRREG 75
=PPVIN_S5_P3V3S5 76
=PPVIN_S5_P5VS3 73
=PP12V_S5_REG 76
=PP12V_S5_PWRCTL 38 70 78

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=0V
NET_SPACING_TYPE=AUDIO
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

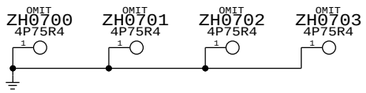
SYNC_MASTER=MASTER SYNC_DATE=N/A
PAGE TITLE
Power Conn / Alias

Apple Inc.

DRAWING NUMBER 051-7863
SIZE D
REVISION A.0.0
BRANCH
PAGE 6 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

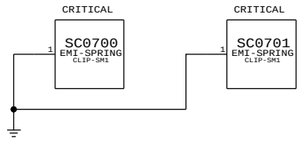
CPU Heatsink

4mm Plated Holes (998-0850)



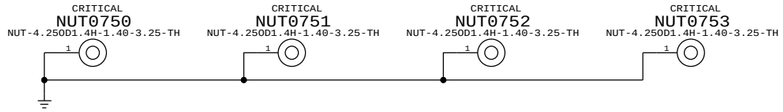
MCP Heatsink

EMC Springs (870-1125)



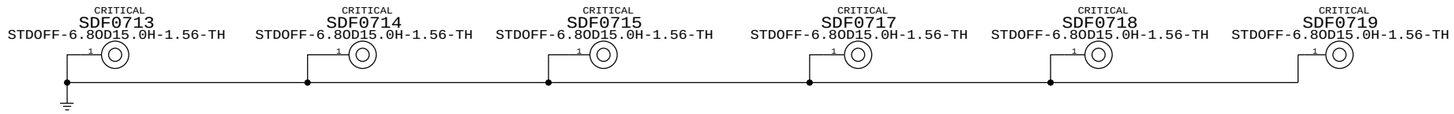
DIMM CONNECTOR NUTS

Nuts (805-9582)



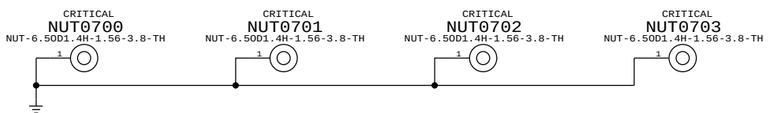
Rear Cover

Standoffs (860-1255)



Backer Plate

Nuts (835-0269)



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 7 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NC ON UNUSED ALIASES

18	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE
18	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_RGB_HSYNC	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_MCP_RGB_VSYNC	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_AD<31..15>	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_C_BE_L<1..0>	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MCP_BUF_SIO_CLK	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE

18	TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE
18	TP_ENET_PWRDWN_L	NC_ENET_PWDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MCP_KBDRSTIN_L	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
	TP_MCP_GPIO_18	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_C_BE_L<3>	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_CLK0	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_GNT0_L	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTY_L	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_PRSNT_L	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PE4_CLKREQ_L	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE
21	TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_MINI_N	NC_USB_MINI_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_MINI_P	NC_USB_MINI_P	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_EXCARD_N	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_EXCARD_P	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
21	ODD_PWR_EN_L	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	EXCARD_CLKREQ_L	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_AD<12..10>	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE
19	TP_PCI_AD<8>	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE

17	TP_PCIE_PE4_R2D_CP	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_D2RP	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
17	TP_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_TPAD_N	NC_USB_TPAD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
20	USB_TPAD_P	NC_USB_TPAD_P	MAKE_BASE=TRUE	NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

15	TP_MEM_A_CLK2P	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_A_CLK5P	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_A_CLK5N	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_B_CLK2P	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE
15	TP_MEM_B_CLK2N	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_B_CLK5P	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE
16	TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

17	GMUX_JTAG_TCK_L	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
17	GMUX_JTAG_TDO	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE	NO_TEST=TRUE
19	GMUX_JTAG_TDI	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE	NO_TEST=TRUE
19	GMUX_JTAG_TMS	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE	NO_TEST=TRUE

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 8 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SIGNAL ALIAS

21 TP_MLB_RAM_VENDOR = MXM_GOOD (MAKE_BASE=TRUE) 6

102 21 PM_SLP_S3_L — R910 15 5% 1/10W MF-LF 402 — PM_SLPS3_BUF2_L (MAKE_BASE=TRUE) 6 49 50 70

(P50 HAS A 100K TO GROUND)

R911 15 5% 1/10W MF-LF 402 — PM_SLPS3_BUF1_L (MAKE_BASE=TRUE) 73 94

R912 100K 5% 1/10W MF-LF 402

PEG Slot Support

17 IN PEG_CLK100M_P = GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE) OUT 87 102

17 IN PEG_CLK100M_N = GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE) OUT 87 102

17 IN =PEG_R2D_C_P<0..15> = PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE) OUT 102 86

17 IN =PEG_R2D_C_N<0..15> = PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE) OUT 102 86

17 OUT =PEG_D2R_P<0..15> = PEG_D2R_P<0..15> (MAKE_BASE=TRUE) IN 86 102

17 OUT =PEG_D2R_N<0..15> = PEG_D2R_N<0..15> (MAKE_BASE=TRUE) IN 86 102

17 IN PEG_PRSNT_L = MXM_DETECT_L (MAKE_BASE=TRUE) OUT 85

20 46 USB_EXTC_OC_L (MAKE_BASE=TRUE)

46 USB_EXTD_OC_L

K22/K23 Use one GPIO for both ports 2&3 OC

USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD IT'S OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

18 =DVI_HPD_GMUX_INT = HPLUG_DET2 (MAKE_BASE=TRUE) — R900 20K 5% 1/10W MF-LF 402

= PCIE_FW_PRSNT_L OUT 17

= PCIE_MINI_PRSNT_L OUT 17

Platform Reset Connections

LPC Reset (Unbuffered)

103 19 IN LPC_RESET_L — R981 33 5% 1/10W MF-LF 402 (PLACEMENT_NOTE=Place close to U1400) — DEBUG_RESET_L OUT 51

R983 33 5% 1/10W MF-LF 402 (PLACEMENT_NOTE=Place close to U1400) — SMC_LRESET_L OUT 49

PCIE Reset (Unbuffered)

17 IN PCIE_RESET_L — R992 0 5% 1/10W MF-LF 402 — FW_RESET_L OUT 41

R991 0 5% 1/10W MF-LF 402 — MINI_RESET_L OUT 34

R990 0 5% 1/10W MF-LF 402 — PEG_RESET_L OUT 87

R971 0 5% 1/10W MF-LF 402 — PCA9557D_RESET_L OUT 29

R993 0 5% 1/10W MF-LF 402 — CARDREADER_PLT_RST_L OUT 47

19 IN MEM_VTT_EN_R — R972 33 5% 1/10W MF-LF 402 — DDRVTT_EN OUT 75 78

NO STUFF C973 0.47UF 10% 6.3V CERM-X5R 402

103 19 IN LPC_CLK33M_SMC_R — R925 33 5% 1/10W MF-LF 402 (PLACEMENT_NOTE=Place close to U1400) — LPC_CLK33M_SMC OUT 103 49

R926 33 5% 1/10W MF-LF 402 (PLACEMENT_NOTE=Place close to U1400) — LPC_CLK33M_LPCPLUS OUT 103 51

103 21 IN PM_CLK32K_SUSCLK_R — R929 22 5% 1/10W MF-LF 402 (PLACEMENT_NOTE=Place close to U1400) — PM_CLK32K_SUSCLK OUT 103 49

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

21 IN MCP_CPUVDD_EN — R930 22 5% 1/10W MF-LF 402 (PLACEMENT_NOTE=Place close to U1400) — MCP_CPU_VLD OUT 21

18 =MCP_MII_RXER

18 =MCP_MII_COL — MCP_MII_NU (MAKE_BASE=TRUE)

18 =MCP_MII_CRS — R955 47K 5% 1/10W MF-LF 402

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Signal Aliases

Apple Inc.

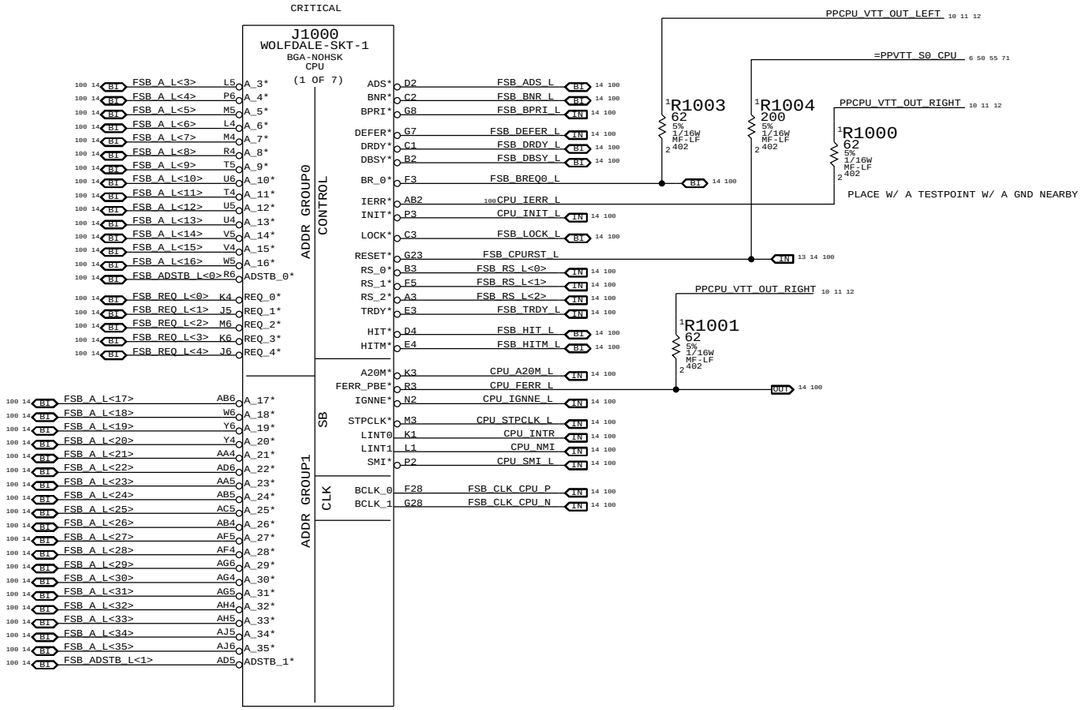
DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

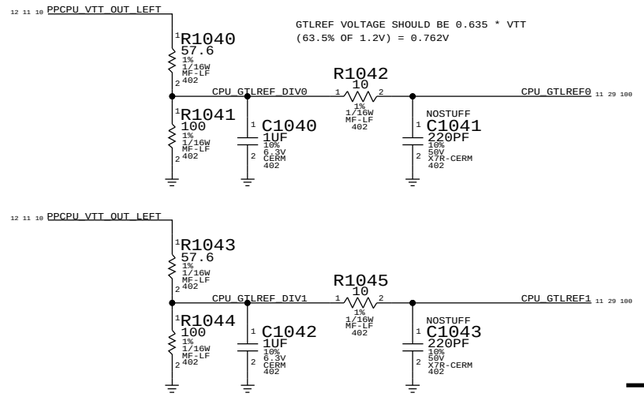
BRANCH:

PAGE: 9 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



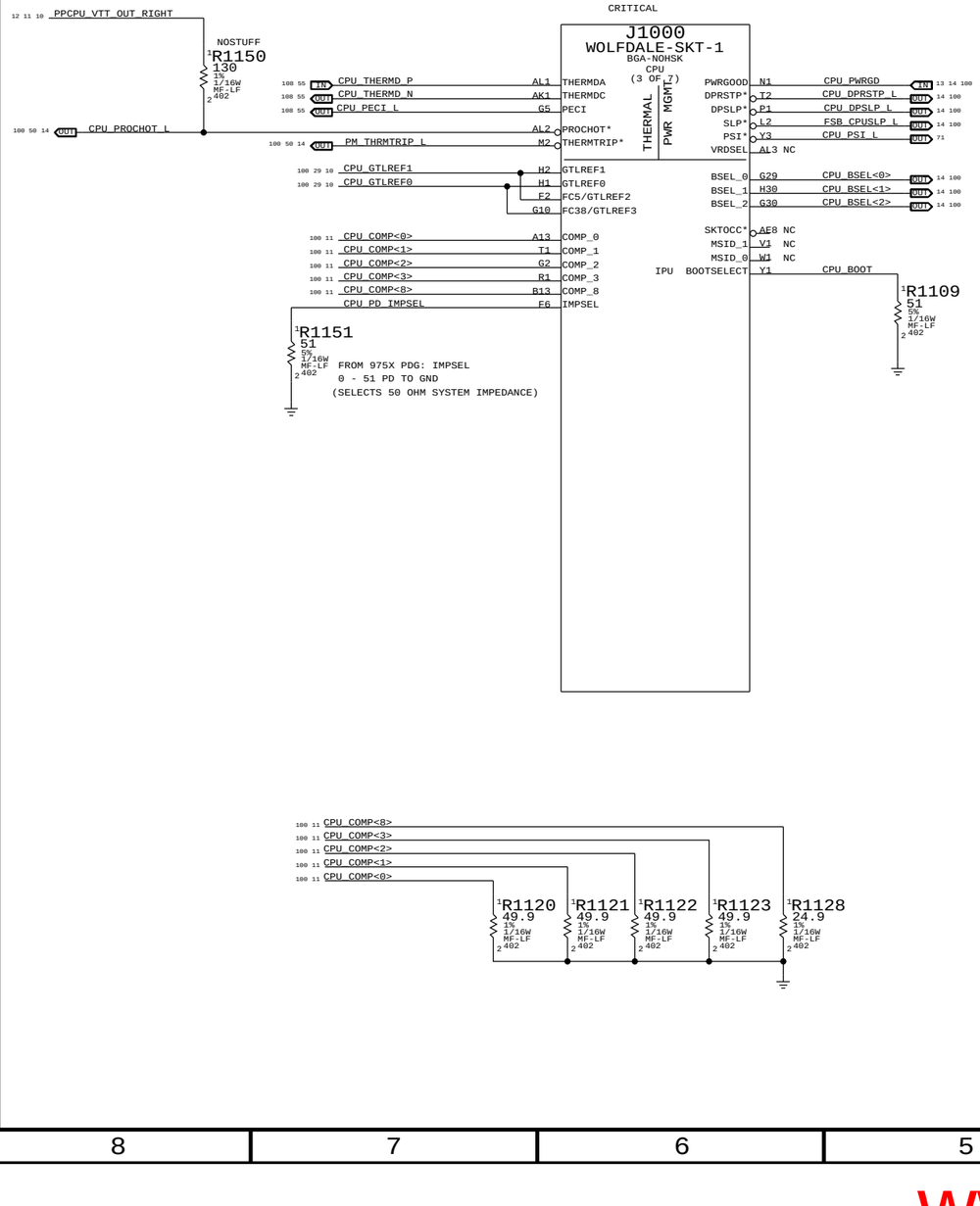
CPU GTLREF

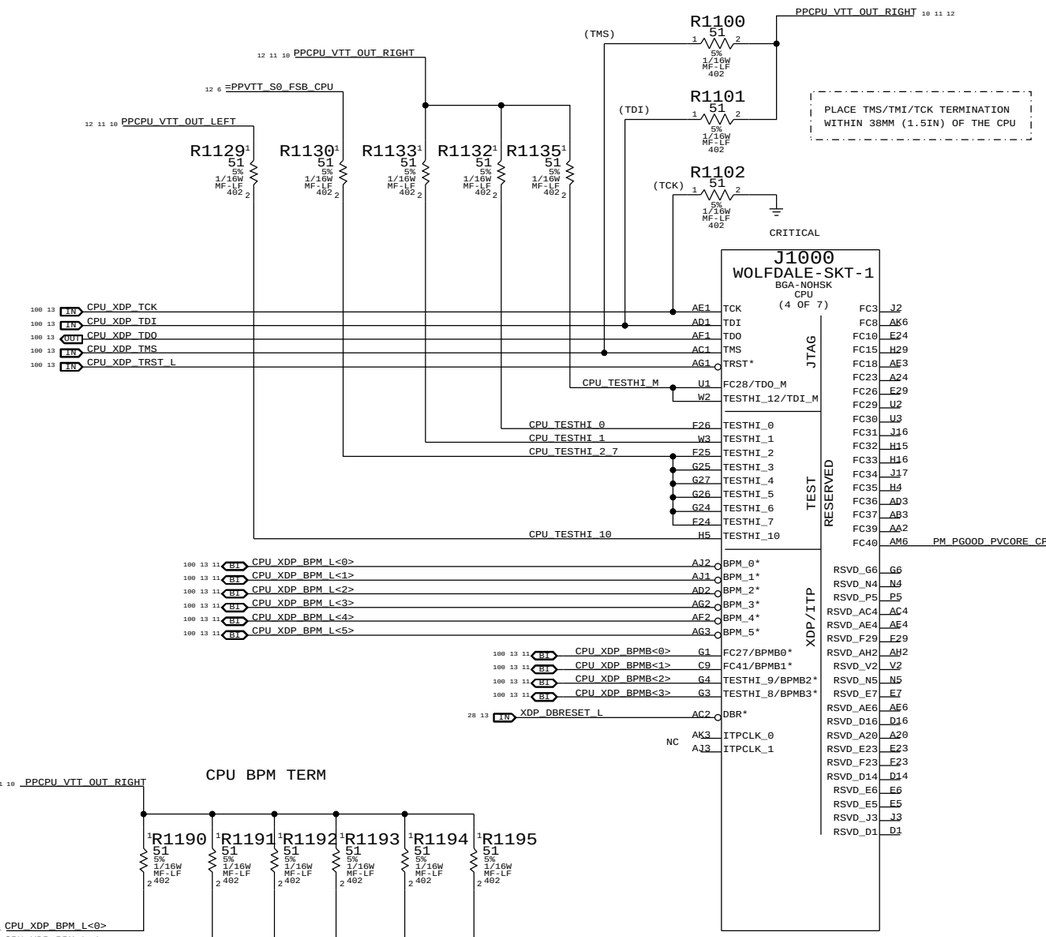


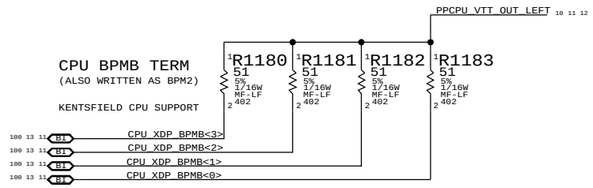
SYNC_MASTER=K22	SYNC_DATE=09/02/2009
PAGE TITLE	CPU FSB
Apple Inc.	DRAWING NUMBER 051-7863 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 10 OF 110
	SHEET

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED







SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

CPU TEST & MISC.

Apple Inc.

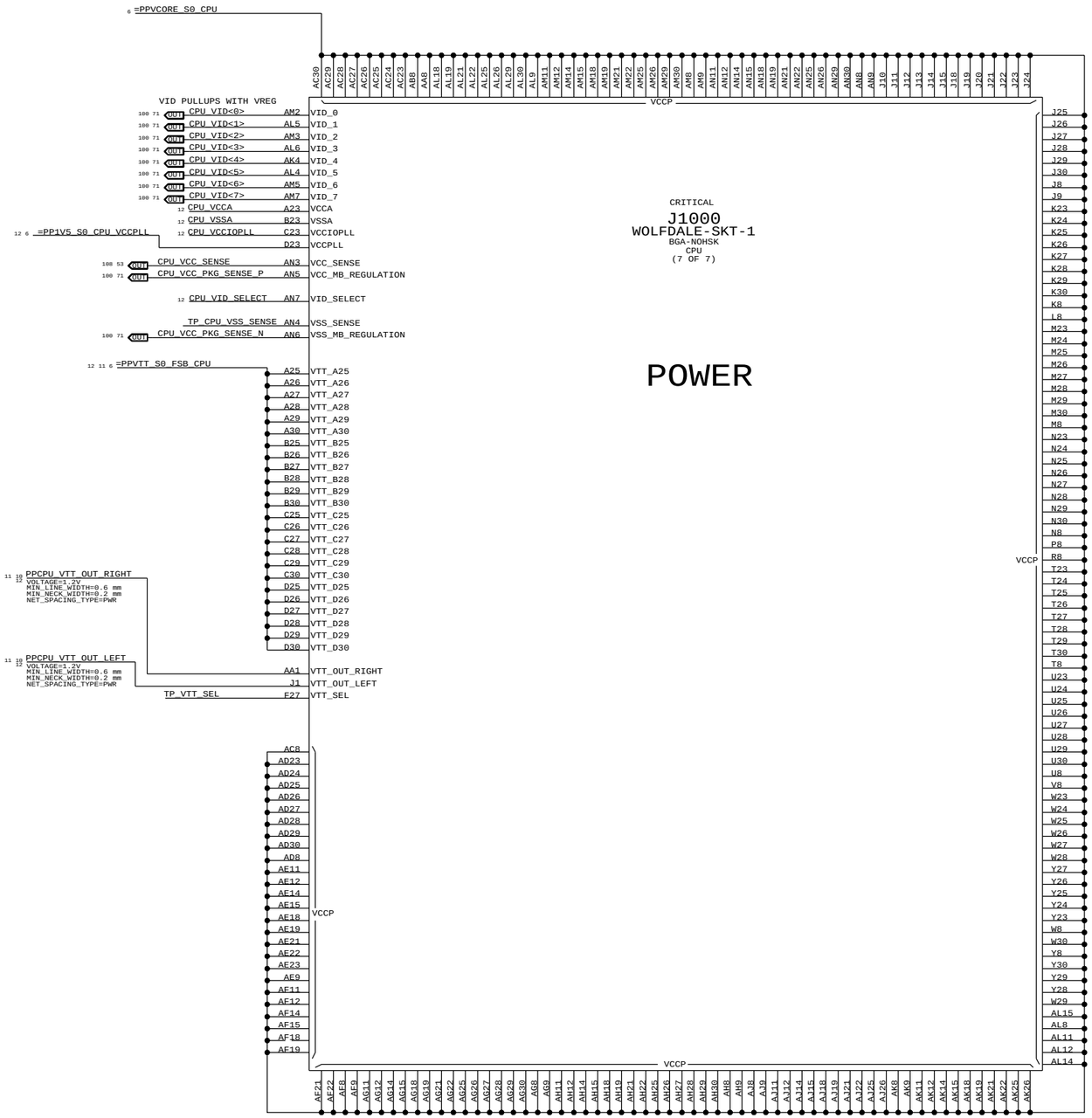
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

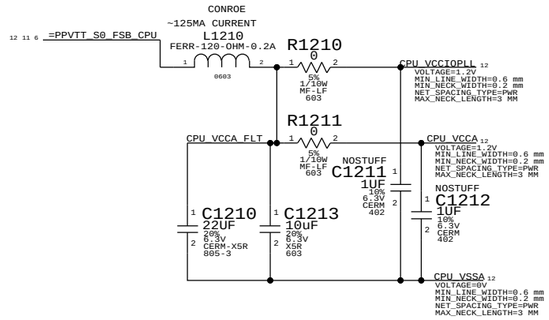
BRANCH

PAGE 11 OF 110

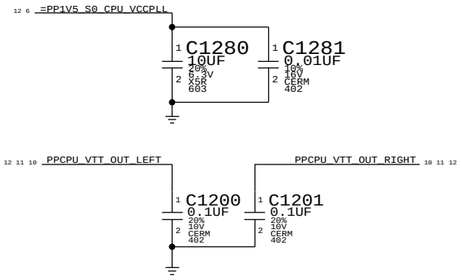
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



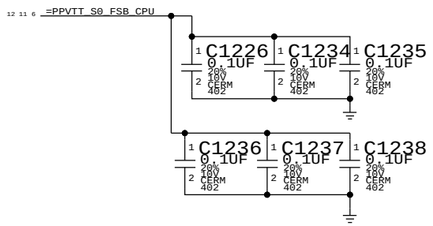
THIS IS FOR OLDER CPU SUPPORT
WILL PLACE FILTER BUT NOT CONNECT FOR WOLFDALE



VCC PLL DECOUPLING

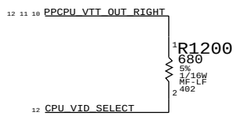


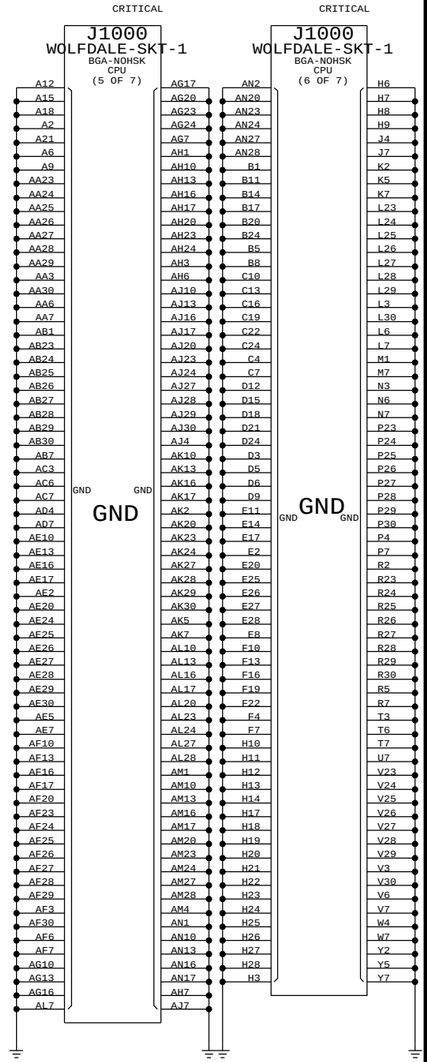
FSB VTT DECOUPLING



VCCP CORE DECOUPLING

(SEE VREG PAGE)





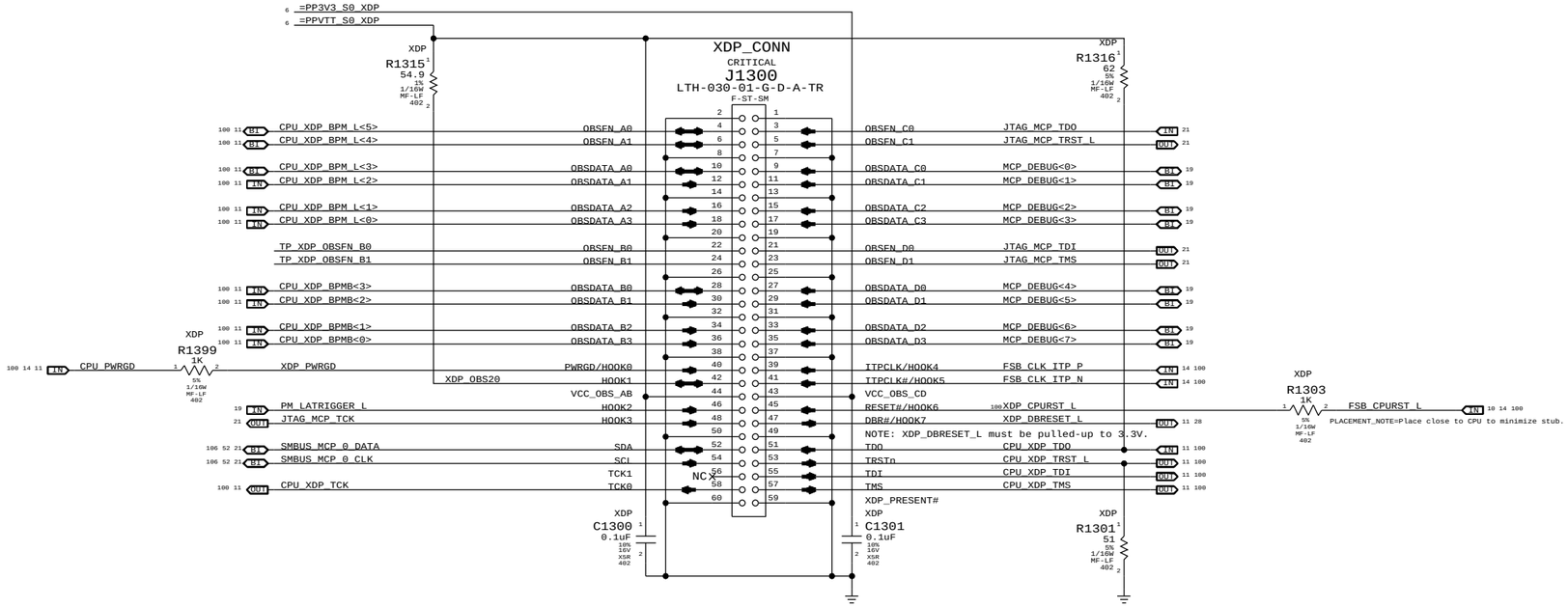
SYNC_MASTER=K22 SYNC_DATE=09/07/2005

PAGE TITLE
CPU POWER, GND, DECAPS

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 12 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP79-specific pinout



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

eXtended Debug Port (XDP)

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 13 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
MCP7A
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0*	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0*	
FSB_DINV_L<0>	V41	CPU_DBI0*	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1*	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1*	
FSB_DINV_L<1>	V35	CPU_DBI1*	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2*	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2*	
FSB_DINV_L<2>	N35	CPU_DBI2*	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3*	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3*	
FSB_DINV_L<3>	J41	CPU_DBI3*	
FSB_A_L<3>	AB35	CPU_A3*	
FSB_A_L<4>	AE37	CPU_A4*	
FSB_A_L<5>	AC33	CPU_A5*	
FSB_A_L<6>	AC35	CPU_A6*	
FSB_A_L<7>	AC34	CPU_A7*	
FSB_A_L<8>	AE35	CPU_A8*	
FSB_A_L<9>	AE34	CPU_A9*	
FSB_A_L<10>	AG39	CPU_A10*	
FSB_A_L<11>	AE33	CPU_A11*	
FSB_A_L<12>	AG38	CPU_A12*	
FSB_A_L<13>	AG37	CPU_A13*	
FSB_A_L<14>	AF35	CPU_A14*	
FSB_A_L<15>	AG35	CPU_A15*	
FSB_A_L<16>	AG34	CPU_A16*	
FSB_A_L<17>	AJ34	CPU_A17*	
FSB_A_L<18>	AG33	CPU_A18*	
FSB_A_L<19>	AJ38	CPU_A19*	
FSB_A_L<20>	AJ37	CPU_A20*	
FSB_A_L<21>	AJ35	CPU_A21*	
FSB_A_L<22>	AL37	CPU_A22*	
FSB_A_L<23>	AJ36	CPU_A23*	
FSB_A_L<24>	AL39	CPU_A24*	
FSB_A_L<25>	AL38	CPU_A25*	
FSB_A_L<26>	AJ33	CPU_A26*	
FSB_A_L<27>	AL35	CPU_A27*	
FSB_A_L<28>	AL34	CPU_A28*	
FSB_A_L<29>	AN37	CPU_A29*	
FSB_A_L<30>	AL33	CPU_A30*	
FSB_A_L<31>	AN38	CPU_A31*	
FSB_A_L<32>	AN35	CPU_A32*	
FSB_A_L<33>	AN36	CPU_A33*	
FSB_A_L<34>	AR39	CPU_A34*	
FSB_A_L<35>	AN34	CPU_A35*	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0*	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1*	
FSB_REQ_L<0>	AC38	CPU_REQ0*	
FSB_REQ_L<1>	AA33	CPU_REQ1*	
FSB_REQ_L<2>	AE38	CPU_REQ2*	
FSB_REQ_L<3>	AC37	CPU_REQ3*	
FSB_REQ_L<4>	AC39	CPU_REQ4*	
FSB_ADS_L	AD42	CPU_ADS*	
FSB_BNR_L	AD43	CPU_BNR*	
FSB_BREQ0_L	AE40	CPU_BR0*	
FSB_BREQ1_L	AL32	CPU_BR1*	
FSB_DBSY_L	AD39	CPU_DBSY*	
FSB_DRDY_L	AD41	CPU_DRDY*	
FSB_HIT_L	AB42	CPU_HIT*	
FSB_HITM_L	AD40	CPU_HITM*	
FSB_LOCK_L	AC43	CPU_LOCK*	
FSB_TRDY_L	AE41	CPU_TRDY*	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT*	
	AG43	CPU_THERMTRIP*	
CPU_FERR_L	AH40	CPU_FERR*	
	F42	CPU_BSEL2	
	D42	CPU_BSEL1	
	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0*	
FSB_RS_L<1>	AB41	CPU_RS1*	
FSB_RS_L<2>	AC42	CPU_RS2*	

CPU_D0*	Y41	FSB_D_L<0>	
CPU_D1*	Y43	FSB_D_L<1>	
CPU_D2*	Y40	FSB_D_L<2>	
CPU_D3*	W42	FSB_D_L<3>	
CPU_D4*	Y42	FSB_D_L<4>	
CPU_D5*	Y39	FSB_D_L<5>	
CPU_D6*	V42	FSB_D_L<6>	
CPU_D7*	W41	FSB_D_L<7>	
CPU_D8*	T41	FSB_D_L<8>	
CPU_D9*	T43	FSB_D_L<9>	
CPU_D10*	T42	FSB_D_L<10>	
CPU_D11*	T39	FSB_D_L<11>	
CPU_D12*	U41	FSB_D_L<12>	
CPU_D13*	R41	FSB_D_L<13>	
CPU_D14*	P42	FSB_D_L<14>	
CPU_D15*	R42	FSB_D_L<15>	
CPU_D16*	AA38	FSB_D_L<16>	
CPU_D17*	AA35	FSB_D_L<17>	
CPU_D18*	AA36	FSB_D_L<18>	
CPU_D19*	AA37	FSB_D_L<19>	
CPU_D20*	AA34	FSB_D_L<20>	
CPU_D21*	W33	FSB_D_L<21>	
CPU_D22*	W34	FSB_D_L<22>	
CPU_D23*	W35	FSB_D_L<23>	
CPU_D24*	W38	FSB_D_L<24>	
CPU_D25*	U33	FSB_D_L<25>	
CPU_D26*	U34	FSB_D_L<26>	
CPU_D27*	U35	FSB_D_L<27>	
CPU_D28*	U36	FSB_D_L<28>	
CPU_D29*	U37	FSB_D_L<29>	
CPU_D30*	R33	FSB_D_L<30>	
CPU_D31*	U38	FSB_D_L<31>	
CPU_D32*	R35	FSB_D_L<32>	
CPU_D33*	R34	FSB_D_L<33>	
CPU_D34*	P35	FSB_D_L<34>	
CPU_D35*	N34	FSB_D_L<35>	
CPU_D36*	R38	FSB_D_L<36>	
CPU_D37*	R37	FSB_D_L<37>	
CPU_D38*	N33	FSB_D_L<38>	
CPU_D39*	R39	FSB_D_L<39>	
CPU_D40*	N36	FSB_D_L<40>	
CPU_D41*	N38	FSB_D_L<41>	
CPU_D42*	L37	FSB_D_L<42>	
CPU_D43*	L38	FSB_D_L<43>	
CPU_D44*	L39	FSB_D_L<44>	
CPU_D45*	J37	FSB_D_L<45>	
CPU_D46*	J38	FSB_D_L<46>	
CPU_D47*	J39	FSB_D_L<47>	
CPU_D48*	H40	FSB_D_L<48>	
CPU_D49*	L42	FSB_D_L<49>	
CPU_D50*	P41	FSB_D_L<50>	
CPU_D51*	M40	FSB_D_L<51>	
CPU_D52*	N40	FSB_D_L<52>	
CPU_D53*	N41	FSB_D_L<53>	
CPU_D54*	K42	FSB_D_L<54>	
CPU_D55*	M42	FSB_D_L<55>	
CPU_D56*	M43	FSB_D_L<56>	
CPU_D57*	L41	FSB_D_L<57>	
CPU_D58*	H42	FSB_D_L<58>	
CPU_D59*	H41	FSB_D_L<59>	
CPU_D60*	J40	FSB_D_L<60>	
CPU_D61*	K41	FSB_D_L<61>	
CPU_D62*	H43	FSB_D_L<62>	
CPU_D63*	H39	FSB_D_L<63>	
CPU_BPRI*	AA41	FSB_BPRI_L	
CPU_DEFER*	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M*	AF41	CPU_A20M_L	
CPU_IGNNE*	AH39	CPU_IGNNE_L	
CPU_INIT*	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI*	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET*	H38	FSB_CPURST_L	
CPU_SLP*	AM33	FSB_CPUSLP_L	
CPU_DPSLP*	AN33	CPU_DPSLP_L	
CPU_DPWR*	AM32	NC	
CPU_STPCLK*	AG42	CPU_STPCLK_L	
CPU_DPRSTP*	AN32	CPU_DPRSTP_L	

PP1V05_S0_MCP_PLL_FSB			
270 mA (A01)	206 mA	AG27	V1P1_DLLDLCELL_AVDD
	20 mA	AH27	V1P1_PLL_MCLK
	29 mA	AG28	V1P1_PLL_FSB
	15 mA	AH28	V1P1_PLL_CPU
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

=PP1V05_S0_MCP_FSB

R1410 62 5% 1/16W MF-LF 402

R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L

R1420 470 5% 1/16W MF-LF 402

R1421 470 5% 1/16W MF-LF 402

R1422 470 5% 1/16W MF-LF 402

CPU_BSEL<2>
CPU_BSEL<1>
CPU_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402

R1435 49.9 1% 1/16W MF-LF 402

R1431 49.9 1% 1/16W MF-LF 402

R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

NO STUFF
R1440 150 5% 1/16W MF-LF 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K22 SYNC_DATE=09/02/2005

PAGE TITLE
MCP CPU Interface

Apple Inc.

DRAWING NUMBER 051-7863
SIZE D
REVISION A.0.0
BRANCH
PAGE 14 OF 110
SHEET

<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400 MCP7A BGA (2 OF 11) — MEMORY PARTITION 0

MEM_A_DQ<63>	AL8	MDQ0_63	MDQS0_7_P	AL10	MEM_A_DQS_P<7>
MEM_A_DQ<62>	AL9	MDQ0_62	MDQS0_7_N	AL11	MEM_A_DQS_N<7>
MEM_A_DQ<61>	AP9	MDQ0_61	MDQS0_6_P	AR8	MEM_A_DQS_P<6>
MEM_A_DQ<60>	AN9	MDQ0_60	MDQS0_6_N	AR9	MEM_A_DQS_N<6>
MEM_A_DQ<59>	AL6	MDQ0_59	MDQS0_5_P	AW7	MEM_A_DQS_P<5>
MEM_A_DQ<58>	AL7	MDQ0_58	MDQS0_5_N	AW8	MEM_A_DQS_N<5>
MEM_A_DQ<57>	AN6	MDQ0_57	MDQS0_4_P	AP13	MEM_A_DQS_P<4>
MEM_A_DQ<56>	AN7	MDQ0_56	MDQS0_4_N	AR13	MEM_A_DQS_N<4>
MEM_A_DQ<55>	AR6	MDQ0_55	MDQS0_3_P	AV25	MEM_A_DQS_P<3>
MEM_A_DQ<54>	AR7	MDQ0_54	MDQS0_3_N	AW25	MEM_A_DQS_N<3>
MEM_A_DQ<53>	AV6	MDQ0_53	MDQS0_2_P	AU30	MEM_A_DQS_P<2>
MEM_A_DQ<52>	AW5	MDQ0_52	MDQS0_2_N	AU29	MEM_A_DQS_N<2>
MEM_A_DQ<51>	AN10	MDQ0_51	MDQS0_1_P	AT35	MEM_A_DQS_P<1>
MEM_A_DQ<50>	AR5	MDQ0_50	MDQS0_1_N	AU35	MEM_A_DQS_N<1>
MEM_A_DQ<49>	AU6	MDQ0_49	MDQS0_0_P	AU39	MEM_A_DQS_P<0>
MEM_A_DQ<48>	AV5	MDQ0_48	MDQS0_0_N	AT39	MEM_A_DQS_N<0>
MEM_A_DQ<47>	AU7	MDQ0_47			
MEM_A_DQ<46>	AU8	MDQ0_46			
MEM_A_DQ<45>	AW9	MDQ0_45			
MEM_A_DQ<44>	AP11	MDQ0_44			
MEM_A_DQ<43>	AW6	MDQ0_43			
MEM_A_DQ<42>	AY5	MDQ0_42	MRAS0*	AV17	MEM_A_RAS_L
MEM_A_DQ<41>	AU9	MDQ0_41	MCAS0*	AP17	MEM_A_CAS_L
MEM_A_DQ<40>	AV9	MDQ0_40	MWE0*	AR17	MEM_A_WE_L
MEM_A_DQ<39>	AU11	MDQ0_39			
MEM_A_DQ<38>	AV11	MDQ0_38			
MEM_A_DQ<37>	AV13	MDQ0_37			
MEM_A_DQ<36>	AW13	MDQ0_36			
MEM_A_DQ<35>	AR11	MDQ0_35			
MEM_A_DQ<34>	AT11	MDQ0_34	MBA0_2	AP23	MEM_A_BA<2>
MEM_A_DQ<33>	AR14	MDQ0_33	MBA0_1	AP19	MEM_A_BA<1>
MEM_A_DQ<32>	AU13	MDQ0_32	MBA0_0	AW17	MEM_A_BA<0>
MEM_A_DQ<31>	AR26	MDQ0_31			
MEM_A_DQ<30>	AU25	MDQ0_30			
MEM_A_DQ<29>	AT27	MDQ0_29			
MEM_A_DQ<28>	AU27	MDQ0_28			
MEM_A_DQ<27>	AP25	MDQ0_27	MA0_14	AR23	MEM_A_A<14>
MEM_A_DQ<26>	AR25	MDQ0_26	MA0_13	AU15	MEM_A_A<13>
MEM_A_DQ<25>	AP27	MDQ0_25	MA0_12	AN23	MEM_A_A<12>
MEM_A_DQ<24>	AR27	MDQ0_24	MA0_11	AW21	MEM_A_A<11>
MEM_A_DQ<23>	AP29	MDQ0_23	MA0_10	AN19	MEM_A_A<10>
MEM_A_DQ<22>	AR29	MDQ0_22	MA0_9	AV21	MEM_A_A<9>
MEM_A_DQ<21>	AP31	MDQ0_21	MA0_8	AR22	MEM_A_A<8>
MEM_A_DQ<20>	AR31	MDQ0_20	MA0_7	AU21	MEM_A_A<7>
MEM_A_DQ<19>	AV27	MDQ0_19	MA0_6	AP21	MEM_A_A<6>
MEM_A_DQ<18>	AN29	MDQ0_18	MA0_5	AR21	MEM_A_A<5>
MEM_A_DQ<17>	AV29	MDQ0_17	MA0_4	AN21	MEM_A_A<4>
MEM_A_DQ<16>	AN31	MDQ0_16	MA0_3	AV19	MEM_A_A<3>
MEM_A_DQ<15>	AU31	MDQ0_15	MA0_2	AU19	MEM_A_A<2>
MEM_A_DQ<14>	AR33	MDQ0_14	MA0_1	AT19	MEM_A_A<1>
MEM_A_DQ<13>	AV37	MDQ0_13	MA0_0	AR19	MEM_A_A<0>
MEM_A_DQ<12>	AW37	MDQ0_12			
MEM_A_DQ<11>	AT31	MDQ0_11			
MEM_A_DQ<10>	AV31	MDQ0_10			
MEM_A_DQ<9>	AT37	MDQ0_9			
MEM_A_DQ<8>	AU37	MDQ0_8			
MEM_A_DQ<7>	AW39	MDQ0_7			
MEM_A_DQ<6>	AV39	MDQ0_6			
MEM_A_DQ<5>	AR37	MDQ0_5			
MEM_A_DQ<4>	AR38	MDQ0_4			
MEM_A_DQ<3>	AV38	MDQ0_3			
MEM_A_DQ<2>	AW38	MDQ0_2			
MEM_A_DQ<1>	AR35	MDQ0_1			
MEM_A_DQ<0>	AP35	MDQ0_0			
MEM_A_DM<7>	AN5	MDQM0_7			
MEM_A_DM<6>	AU5	MDQM0_6			
MEM_A_DM<5>	AR10	MDQM0_5			
MEM_A_DM<4>	AN13	MDQM0_4			
MEM_A_DM<3>	AN27	MDQM0_3			
MEM_A_DM<2>	AW29	MDQM0_2			
MEM_A_DM<1>	AV35	MDQM0_1			
MEM_A_DM<0>	AR34	MDQM0_0			

MEMORY CONTROL 0A

MCLK0A_2_P	AW33	TP_MEM_A_CLK2P	
MCLK0A_2_N	AV33	TP_MEM_A_CLK2N	
MCLK0A_1_P	BA24	MEM_A_CLK_P<1>	
MCLK0A_1_N	AY24	MEM_A_CLK_N<1>	
MCLK0A_0_P	BB20	MEM_A_CLK_P<0>	
MCLK0A_0_N	BC20	MEM_A_CLK_N<0>	
MCS0A_1*	AT15	MEM_A_CS_L<1>	
MCS0A_0*	AR18	MEM_A_CS_L<0>	
MODT0A_1	AP15	MEM_A_ODT<1>	
MODT0A_0	AV15	MEM_A_ODT<0>	
MCKE0A_1	AU23	MEM_A_CKE<1>	
MCKE0A_0	AT23	MEM_A_CKE<0>	

OMIT

U1400 MCP7A BGA (3 OF 11) — MEMORY PARTITION 1

MEM_B_DQ<63>	AT4	MDQ1_63	MDQS1_7_P	AT2	MEM_B_DQS_P<7>
MEM_B_DQ<62>	AT3	MDQ1_62	MDQS1_7_N	AT1	MEM_B_DQS_N<7>
MEM_B_DQ<61>	AV2	MDQ1_61	MDQS1_6_P	AY2	MEM_B_DQS_P<6>
MEM_B_DQ<60>	AV3	MDQ1_60	MDQS1_6_N	AY1	MEM_B_DQS_N<6>
MEM_B_DQ<59>	AR4	MDQ1_59	MDQS1_5_P	BB6	MEM_B_DQS_P<5>
MEM_B_DQ<58>	AR3	MDQ1_58	MDQS1_5_N	BA6	MEM_B_DQS_N<5>
MEM_B_DQ<57>	AU2	MDQ1_57	MDQS1_4_P	BA10	MEM_B_DQS_P<4>
MEM_B_DQ<56>	AU3	MDQ1_56	MDQS1_4_N	AY11	MEM_B_DQS_N<4>
MEM_B_DQ<55>	AY4	MDQ1_55	MDQS1_3_P	BB33	MEM_B_DQS_P<3>
MEM_B_DQ<54>	AY3	MDQ1_54	MDQS1_3_N	BA33	MEM_B_DQS_N<3>
MEM_B_DQ<53>	BB3	MDQ1_53	MDQS1_2_P	BB37	MEM_B_DQS_P<2>
MEM_B_DQ<52>	BC3	MDQ1_52	MDQS1_2_N	BA37	MEM_B_DQS_N<2>
MEM_B_DQ<51>	AW4	MDQ1_51	MDQS1_1_P	BA43	MEM_B_DQS_P<1>
MEM_B_DQ<50>	AW3	MDQ1_50	MDQS1_1_N	AY42	MEM_B_DQS_N<1>
MEM_B_DQ<49>	BA3	MDQ1_49	MDQS1_0_P	AT42	MEM_B_DQS_P<0>
MEM_B_DQ<48>	BB2	MDQ1_48	MDQS1_0_N	AT43	MEM_B_DQS_N<0>
MEM_B_DQ<47>	BB5	MDQ1_47			
MEM_B_DQ<46>	BA5	MDQ1_46			
MEM_B_DQ<45>	BA8	MDQ1_45			
MEM_B_DQ<44>	BC8	MDQ1_44			
MEM_B_DQ<43>	BB4	MDQ1_43			
MEM_B_DQ<42>	BC4	MDQ1_42	MRAS1*	AW16	MEM_B_RAS_L
MEM_B_DQ<41>	BA7	MDQ1_41	MCAS1*	BA15	MEM_B_CAS_L
MEM_B_DQ<40>	AY8	MDQ1_40	MWE1*	BA16	MEM_B_WE_L
MEM_B_DQ<39>	BA9	MDQ1_39			
MEM_B_DQ<38>	BB10	MDQ1_38			
MEM_B_DQ<37>	BB12	MDQ1_37			
MEM_B_DQ<36>	AW12	MDQ1_36			
MEM_B_DQ<35>	BB8	MDQ1_35			
MEM_B_DQ<34>	BB9	MDQ1_34	MBA1_2	BB29	MEM_B_BA<2>
MEM_B_DQ<33>	AY12	MDQ1_33	MBA1_1	BB18	MEM_B_BA<1>
MEM_B_DQ<32>	BA12	MDQ1_32	MBA1_0	BB17	MEM_B_BA<0>
MEM_B_DQ<31>	BC32	MDQ1_31			
MEM_B_DQ<30>	AW32	MDQ1_30			
MEM_B_DQ<29>	BA35	MDQ1_29			
MEM_B_DQ<28>	AY36	MDQ1_28			
MEM_B_DQ<27>	BA32	MDQ1_27	MA1_14	BA29	MEM_B_A<14>
MEM_B_DQ<26>	BB32	MDQ1_26	MA1_13	BA14	MEM_B_A<13>
MEM_B_DQ<25>	BA34	MDQ1_25	MA1_12	AW28	MEM_B_A<12>
MEM_B_DQ<24>	AY35	MDQ1_24	MA1_11	BC28	MEM_B_A<11>
MEM_B_DQ<23>	BC36	MDQ1_23	MA1_10	BA17	MEM_B_A<10>
MEM_B_DQ<22>	AW36	MDQ1_22	MA1_9	BB28	MEM_B_A<9>
MEM_B_DQ<21>	BA39	MDQ1_21	MA1_8	AY28	MEM_B_A<8>
MEM_B_DQ<20>	AY40	MDQ1_20	MA1_7	BA28	MEM_B_A<7>
MEM_B_DQ<19>	BA36	MDQ1_19	MA1_6	AY27	MEM_B_A<6>
MEM_B_DQ<18>	BB36	MDQ1_18	MA1_5	BA27	MEM_B_A<5>
MEM_B_DQ<17>	BA38	MDQ1_17	MA1_4	BA26	MEM_B_A<4>
MEM_B_DQ<16>	AY39	MDQ1_16	MA1_3	BB26	MEM_B_A<3>
MEM_B_DQ<15>	BB40	MDQ1_15	MA1_2	BA25	MEM_B_A<2>
MEM_B_DQ<14>	AW40	MDQ1_14	MA1_1	BB25	MEM_B_A<1>
MEM_B_DQ<13>	AV42	MDQ1_13	MA1_0	BA18	MEM_B_A<0>
MEM_B_DQ<12>	AV41	MDQ1_12			
MEM_B_DQ<11>	BA40	MDQ1_11			
MEM_B_DQ<10>	BC40	MDQ1_10			
MEM_B_DQ<9>	AW42	MDQ1_9			
MEM_B_DQ<8>	AW41	MDQ1_8			
MEM_B_DQ<7>	AT40	MDQ1_7			
MEM_B_DQ<6>	AT41	MDQ1_6			
MEM_B_DQ<5>	AP41	MDQ1_5			
MEM_B_DQ<4>	AN40	MDQ1_4			
MEM_B_DQ<3>	AU40	MDQ1_3			
MEM_B_DQ<2>	AU41	MDQ1_2			
MEM_B_DQ<1>	AR41	MDQ1_1			
MEM_B_DQ<0>	AP42	MDQ1_0			
MEM_B_DM<7>	AT5	MDQM1_7			
MEM_B_DM<6>	BA2	MDQM1_6			
MEM_B_DM<5>	AY7	MDQM1_5			
MEM_B_DM<4>	BA11	MDQM1_4			
MEM_B_DM<3>	BB34	MDQM1_3			
MEM_B_DM<2>	BB38	MDQM1_2			
MEM_B_DM<1>	AY43	MDQM1_1			
MEM_B_DM<0>	AR42	MDQM1_0			

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P	
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N	
MCLK1A_1_P	BB22	MEM_B_CLK_P<1>	
MCLK1A_1_N	BA22	MEM_B_CLK_N<1>	
MCLK1A_0_P	BA19	MEM_B_CLK_P<0>	
MCLK1A_0_N	AY19	MEM_B_CLK_N<0>	
MCS1A_1*	BB14	MEM_B_CS_L<1>	
MCS1A_0*	BB16	MEM_B_CS_L<0>	
MODT1A_1	BB13	MEM_B_ODT<1>	
MODT1A_0	AY15	MEM_B_ODT<0>	
MCKE1A_1	AY31	MEM_B_CKE<1>	
MCKE1A_0	BB30	MEM_B_CKE<0>	

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MCP Memory Interface

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 15 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
MCP7A
BGA
(4 OF 11)

MEMORY CONTROL 0B

8 TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
8 TP_MEM_A_CLK5N	AU34	MCLK0B_2_N	
101 33 MEM_A_CLK_P<4>	BB24	MCLK0B_1_P	
101 33 MEM_A_CLK_N<4>	BC24	MCLK0B_1_N	
101 33 MEM_A_CLK_P<3>	BA21	MCLK0B_0_P	
101 33 MEM_A_CLK_N<3>	BB21	MCLK0B_0_N	
101 31 MEM_A_CS_L<2>	AU17	MCS0B_0*	
101 31 MEM_A_CS_L<3>	AR15	MCS0B_1*	
101 31 MEM_A_ODT<2>	AN17	MODT0B_0	
101 31 MEM_A_ODT<3>	AN15	MODT0B_1	
101 31 MEM_A_CKE<2>	AV23	MCKE0B_0	
101 31 MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

MCLK1B_2_P	BA41	TP_MEM_B_CLK5P	8
MCLK1B_2_N	BB41	TP_MEM_B_CLK5N	8
MCLK1B_1_P	AY23	MEM_B_CLK_P<4>	33 101
MCLK1B_1_N	BA23	MEM_B_CLK_N<4>	33 101
MCLK1B_0_P	BA20	MEM_B_CLK_P<3>	33 101
MCLK1B_0_N	AY20	MEM_B_CLK_N<3>	33 101
MCS1B_0*	BC16	MEM_B_CS_L<2>	32 101
MCS1B_1*	BA13	MEM_B_CS_L<3>	32 101
MODT1B_0	AY16	MEM_B_ODT<2>	32 101
MODT1B_1	BC13	MEM_B_ODT<3>	32 101
MCKE1B_0	BA30	MEM_B_CKE<2>	32 101
MCKE1B_1	BA31	MEM_B_CKE<3>	32 101

25 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T28	V1P1_PLL_V
12 mA	U28	V1P1_PLL_DP
19 mA	U27	V1P1_PLL_CORE
39 mA	T27	V1P1_PLL_XREF_XS

MRESET0* AY32 MCP_MEM_RESET_L → ODT 33
TP or NC for DDR2.

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

R1610[1] 40.2 1% 1/16W MF-LF 402 [2]

R1611[1] 40.2 1% 1/16W MF-LF 402 [2]

101 MCP_MEM_COMP_GND — AM41 MEM_COMP_GND
101 MCP_MEM_COMP_VDD — AN41 MEM_COMP_1P8V

=PP1V8R1V5_S0_MCP_MEM 6 16 25 30
4771 mA (A01, DDR3)

	AA22	
	AP12	
	G30	
	P10	
	T10	
	T6	
	V10	
	V34	
	W5	
	AA39	
	AB22	
	AB7	
	AD22	
	AE20	
	AE24	
	AG24	
	AH35	
	AK7	
	AM28	
	AT25	
GND	AP30	V1P8_MEM_VDDP
	AR36	
	AU10	
	F28	
	BC21	
	AY9	
	BC9	
	D34	
	F24	
	G32	
	H31	
	K7	
	M38	
	M5	
	M6	
	M7	
	M9	
	N39	
	N8	
	P33	
	P34	
	P37	
	P4	
	P40	
	P7	
	R36	
	R40	
	R43	
	R5	
	T18	
	T20	
	AK11	
	T24	
	T26	

AM17		
AN20		
AN24		
AT17		
AP16		
AN22		
AP20		
AP24		
AV16		
AR16		
AR20		
AM19		
AR24		
AW15		
AP22		
AP18		
AU16		
AN18		
AU24		
AT21		
AY29		
AV24		
AM21		
AU20		
AU22		
AW27		
BC17		
AV20		
AY17		
AY18		
AM15		
AU18		
AY25		
AM23		
AY26		
AW19		
AW24		
BC25		
AL30		
AM31		
AM25		
AM27		
AM29		
AN16		
BC29		
	T33	
	T34	
	T35	
	T37	
GND	T38	
	T7	
	T9	
	U18	
	U20	
	U22	

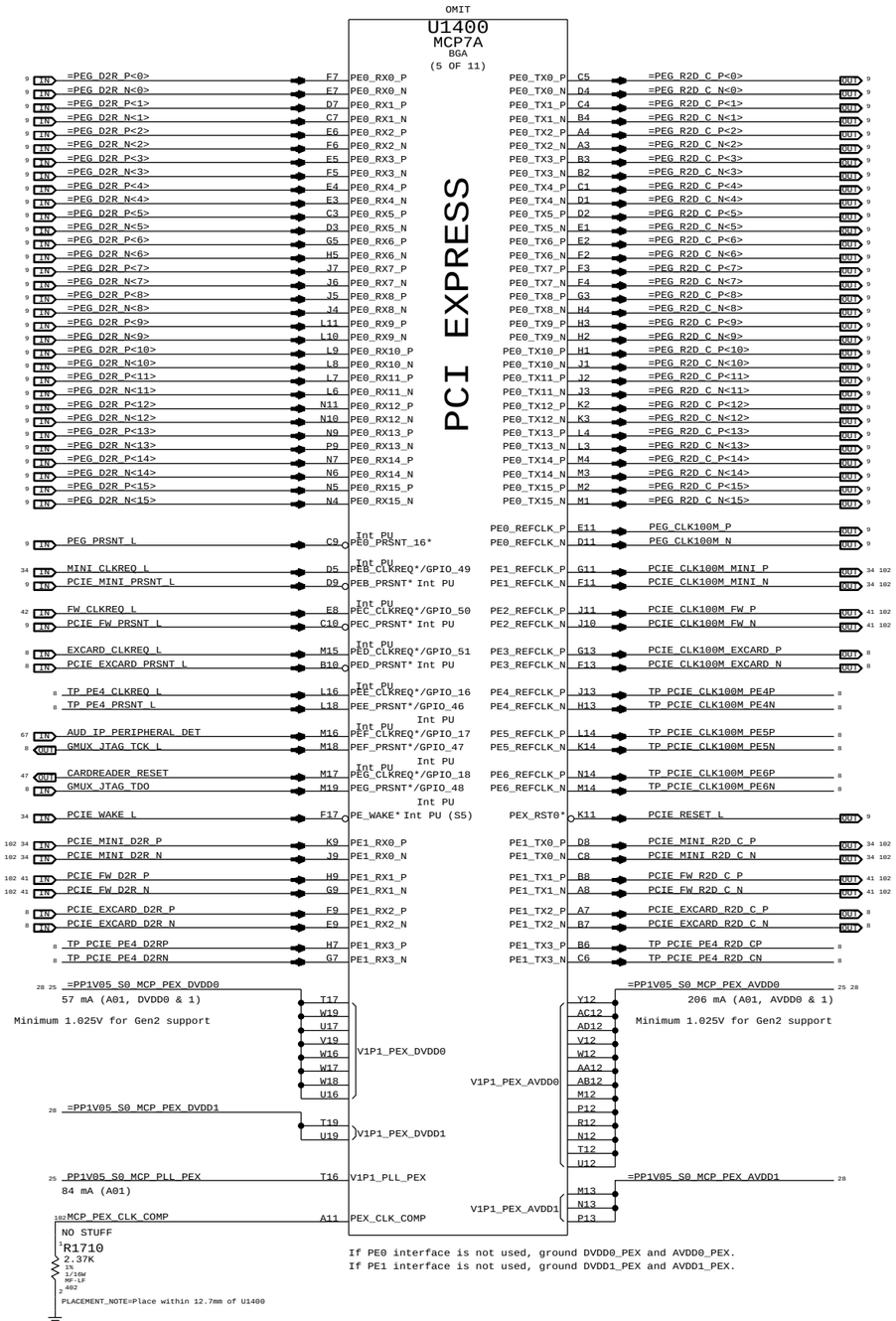
SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
MCP MEMORY CNTRL & MISC

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 16 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



SYNC_MASTER=K22	SYNC_DATE=09/02/2009
PAGE TITLE	MCP PCIe Interfaces
Apple Inc.	DRAWING NUMBER 051-7863 SIZE D
	REVISION A.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE 17 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP7A
BGA
(6 OF 11)

LAN

ENET_RXD<0>	C23	MII_RXD0	
ENET_RXD<1>	B23	MII_RXD1	
ENET_RXD<2>	E24	MII_RXD2	
ENET_RXD<3>	A24	MII_RXD3	
ENET_CLK125M_RXCLK	A23	MII_RXCLK	
ENET_RX_CTRL	C22	MII_RXDV	
=MCP_MII_RXER	F23	MII_RXER/GPIO_36	
=MCP_MII_COL	B26	MII_COL/GPIO_20/MSMB_DATA	
=MCP_MII_CRS	B22	MII_CRS/GPIO_21/MSMB_CLK	
TP_ENET_INTR_L	J22	MII_INTR/GPIO_35	
PP1V05_ENET_MCP_PLL_MAC	T23	V1P1_DUAL_MACPLL	5 mA (A01)
MCP_MII_COMP_VDD	C27	MII_COMP_VDD	
MCP_MII_COMP_GND	B27	MII_COMP_GND	

=PP3V3_ENET_MCP_RMGT	J24	V3P3_DUAL_RMGT0	83 mA (A01)
	K24	V3P3_DUAL_RMGT1	
=PP1V05_ENET_MCP_RMGT	U23	V1P0_DUAL_RMGT_0	131 mA (A01)
	V23	V1P0_DUAL_RMGT_1	
MCP_MII_VREF	E28	MII_VREF	
ENET_TXD<0>	B24	MII_TXD0	
ENET_TXD<1>	C24	MII_TXD1	
ENET_TXD<2>	C25	MII_TXD2	
ENET_TXD<3>	D25	MII_TXD3	
ENET_CLK125M_TXCLK	D24	MII_TXCLK	
ENET_TX_CTRL	C26	MII_TXEN	
ENET_MDC	D21	MII_MDC	
ENET_MDIO	C21	MII_MDIO	
TP_ENET_PWRDWN_L	G23	MII_PWRDWN/GPIO_37	
MCP_CLK25M_BUF0_R	E23	BUF_25MHZ	
ENET_RESET_L	J23	MII_RESET*	

DACS

PP3V3_S0_MCP_DAC	J32	V3P3_RGBDAC_VDD	103 mA
	K32	V3P3_TVDAC_VDD	103 mA
			206 mA (A01)
MCP_DDC_CLK0	B31	DDC_CLK0	
MCP_DDC_DATA0	A31	DDC_DATA0	
TP_MCP_RGB_DAC_RSET	C39	RGB_DAC_RSET	
TP_MCP_RGB_DAC_VREF	B38	RGB_DAC_VREF	
MCP_TV_DAC_RSET	E36	TV_DAC_RSET	
MCP_TV_DAC_VREF	A35	TV_DAC_VREF	

RGB ONLY

TP_MCP_RGB_RED	B39	RGB_DAC_RED	
TP_MCP_RGB_GREEN	A39	RGB_DAC_GREEN	
TP_MCP_RGB_BLUE	B40	RGB_DAC_BLUE	
TP_MCP_RGB_HSYNC	A40	RGB_DAC_HSYNC	
TP_MCP_RGB_VSYNC	A41	RGB_DAC_VSYNC	

TV / Component
C / Pr
Y / Y
Comp / Pb

	A36	TV_DAC_RED	CRT_IG_R_C_PR
	B36	TV_DAC_GREEN	CRT_IG_G_Y_Y
	C36	TV_DAC_BLUE	CRT_IG_B_COMP_PB
	D36	TV_DAC_HSYNC/GPIO_44	CRT_IG_HSYNC
	C37	TV_DAC_VSYNC/GPIO_45	CRT_IG_VSYNC
MCP_CLK27M_XTALIN	C38	XTALIN_TV	
MCP_CLK27M_XTALOUT	D38	XTALOUT_TV	

FLAT PANEL

	B35	IFPA_TXC_P	LVDS_IG_A_CLK_P
	C35	IFPA_TXC_N	LVDS_IG_A_CLK_N
	B32	IFPA_TXD0_P	LVDS_IG_A_DATA_P<0>
	A32	IFPA_TXD0_N	LVDS_IG_A_DATA_N<0>
	D32	IFPA_TXD1_P	LVDS_IG_A_DATA_P<1>
	C32	IFPA_TXD1_N	LVDS_IG_A_DATA_N<1>
	D33	IFPA_TXD2_P	LVDS_IG_A_DATA_P<2>
	C33	IFPA_TXD2_N	LVDS_IG_A_DATA_N<2>
	B34	IFPA_TXD3_P	LVDS_IG_A_DATA_P<3>
	C34	IFPA_TXD3_N	LVDS_IG_A_DATA_N<3>
	L31	IFPB_TXC_P	LVDS_IG_B_CLK_P
	K31	IFPB_TXC_N	LVDS_IG_B_CLK_N
	J29	IFPB_TXD4_P	LVDS_IG_B_DATA_P<0>
	H29	IFPB_TXD4_N	LVDS_IG_B_DATA_N<0>
	L29	IFPB_TXD5_P	LVDS_IG_B_DATA_P<1>
	K29	IFPB_TXD5_N	LVDS_IG_B_DATA_N<1>
	L30	IFPB_TXD6_P	LVDS_IG_B_DATA_P<2>
	K30	IFPB_TXD6_N	LVDS_IG_B_DATA_N<2>
	N30	IFPB_TXD7_P	LVDS_IG_B_DATA_P<3>
	M30	IFPB_TXD7_N	LVDS_IG_B_DATA_N<3>
	C30	DDC_CLK2/GPIO_23	LVDS_IG_DDC_CLK
	B30	DDC_DATA2/GPIO_24	LVDS_IG_DDC_DATA
=MCP_HDMI_DDC_CLK	D31	DDC_CLK3	
=MCP_HDMI_DDC_DATA	E31	DDC_DATA3	
MCP_IFPAB_RSET	E32	IFPAB_RSET	
MCP_IFPAB_VPROBE	G31	IFPAB_VPROBE	

DP_IG_AUX_CH_P	D43	DP_AUX_CH0_P	
DP_IG_AUX_CH_N	C43	DP_AUX_CH0_N	
=DVI_HPD_GMUX_INT	C31	HPLUG_DET2/GPIO_22	(See below)
=MCP_HDMI_HPD	F31	HPLUG_DET3	
=PP3V3R1V8_S0_MCP_IFP_VDD	M27	V1P8_IFPA_VDD	190 mA (A01, 1.8V)
	M26	V1P8_IFPB_VDD	
=PP3V3_S0_MCP_VPLL	M28	V3P3_PLL_IFPAB	16 mA (A01) 8 mA
	M29	V3P3_PLL_HDMI	8 mA
=PP1V05_S0_MCP_HDMI_VDD	T25	V1P1_HDMI_VDD	95 mA (A01)
MCP_HDMI_RSET	J31	HDMI_RSET	
MCP_HDMI_VPROBE	J30	HDMI_VPROBE	

LPCPLUS_GPIO	E16	GPIO_6/FERR*/IGPU_GPIO6	
DP_IG_CA_DET	B15	GPIO_7/NFERR*/IGPU_GPIO7	
LVDS_IG_BKL_PWM	G39	LCD_BKL_CTL/GPIO_57	(See below)
LVDS_IG_BKL_ON	E37	LCD_BKL_ON/GPIO_59	
LVDS_IG_PANEL_PWR	F40	LCD_PANEL_PWR/GPIO_58	
=MCP_HDMI_TXC_P	D35	HDMI_TXC_P/ML0_LANE3_P	
=MCP_HDMI_TXC_N	E35	HDMI_TXC_N/ML0_LANE3_N	
=MCP_HDMI_TXD_P<0>	G35	HDMI_TXD0_P/ML0_LANE2_P	
=MCP_HDMI_TXD_N<0>	F35	HDMI_TXD0_N/ML0_LANE2_N	
=MCP_HDMI_TXD_P<1>	F33	HDMI_TXD1_P/ML0_LANE1_P	
=MCP_HDMI_TXD_N<1>	G33	HDMI_TXD1_N/ML0_LANE1_N	
=MCP_HDMI_TXD_P<2>	J33	HDMI_TXD2_P/ML0_LANE0_P	
=MCP_HDMI_TXD_N<2>	H33	HDMI_TXD2_N/ML0_LANE0_N	

R1810 49.9 1% 1/16W MF-LF 402
R1811 49.9 1% 1/16W MF-LF 402
R1820 47K 5% 1/16W MF-LF 402
R1850 10K 5% 1/16W MF-LF 402
R1860 100K 5% 1/16W MF-LF 402
R1861 100K 5% 1/16W MF-LF 402

=PP3V3_ENET_MCP_RMGT
=PP3V3_S5_MCP_GPIO
=PP3V3_S0_MCP_GPIO

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Signal	Interface Mode: TMDS/HDMI	Interface Mode: DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

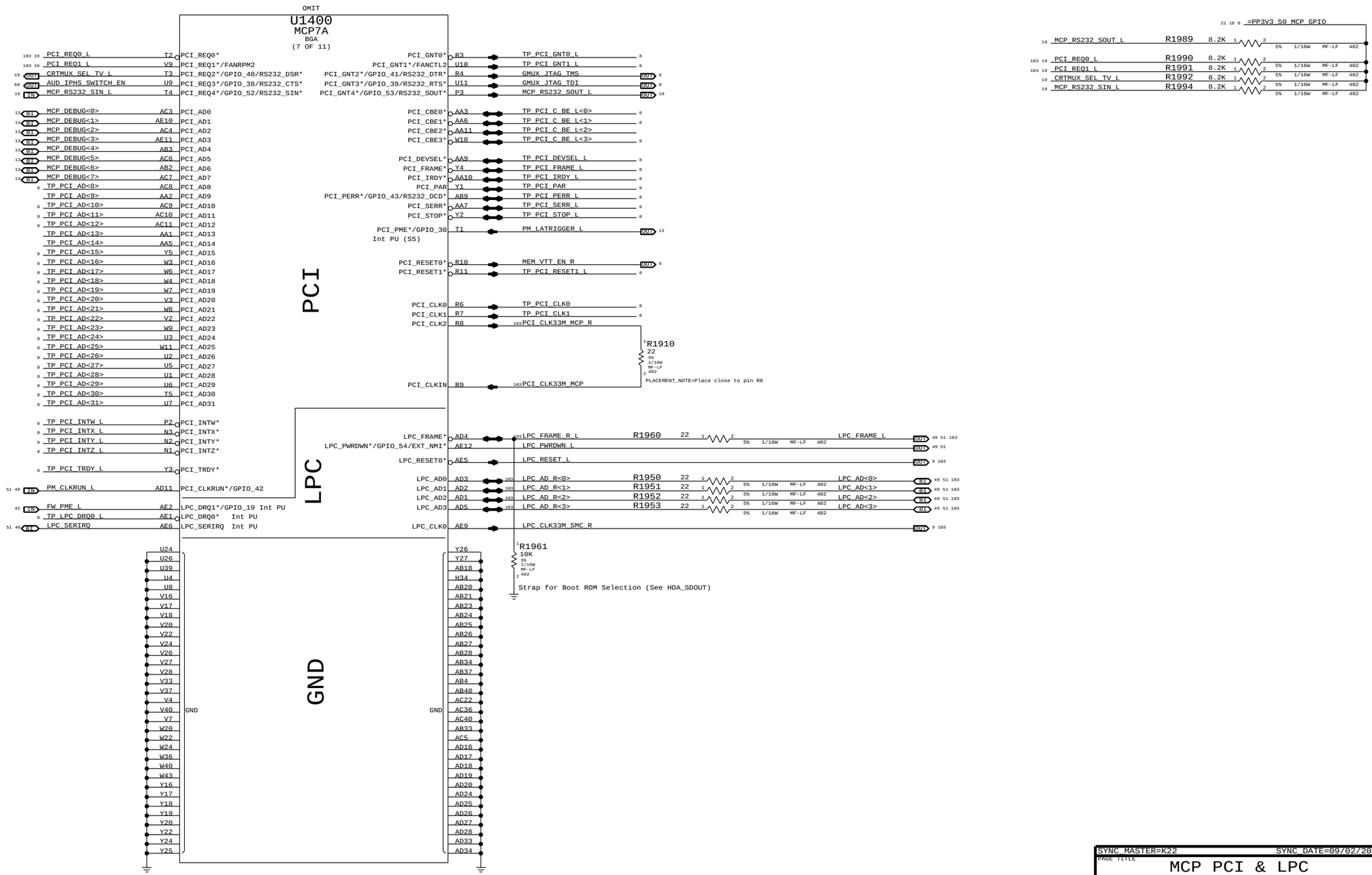
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER 051-7863
SIZE D
REVISION A.0.0
BRANCH
PAGE 18 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=K22 SYNC DATE=09/02/2009

PAGE TITLE: MCP PCI & LPC

Apple Inc.

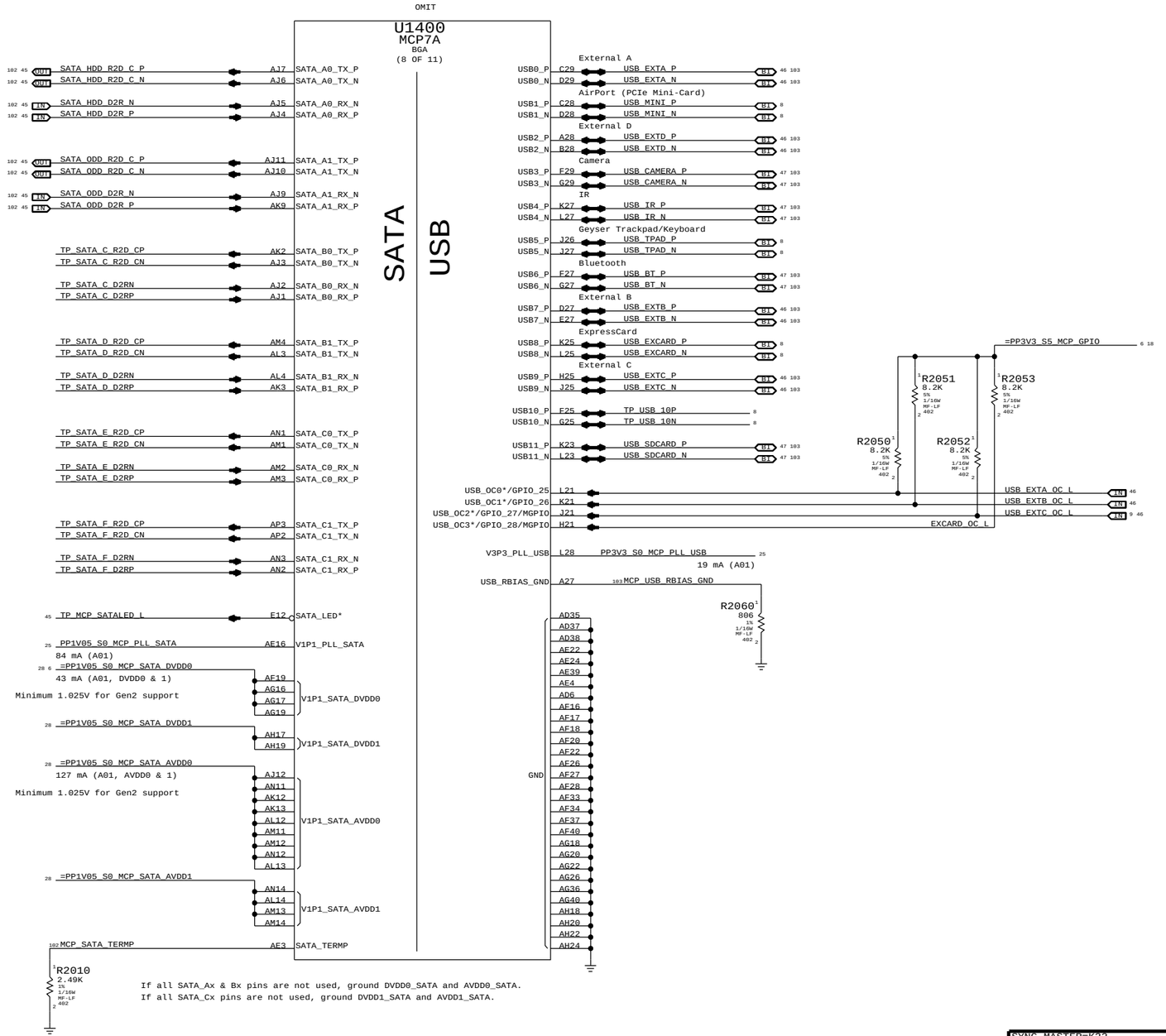
DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 19 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MCP SATA & USB

Apple Inc.

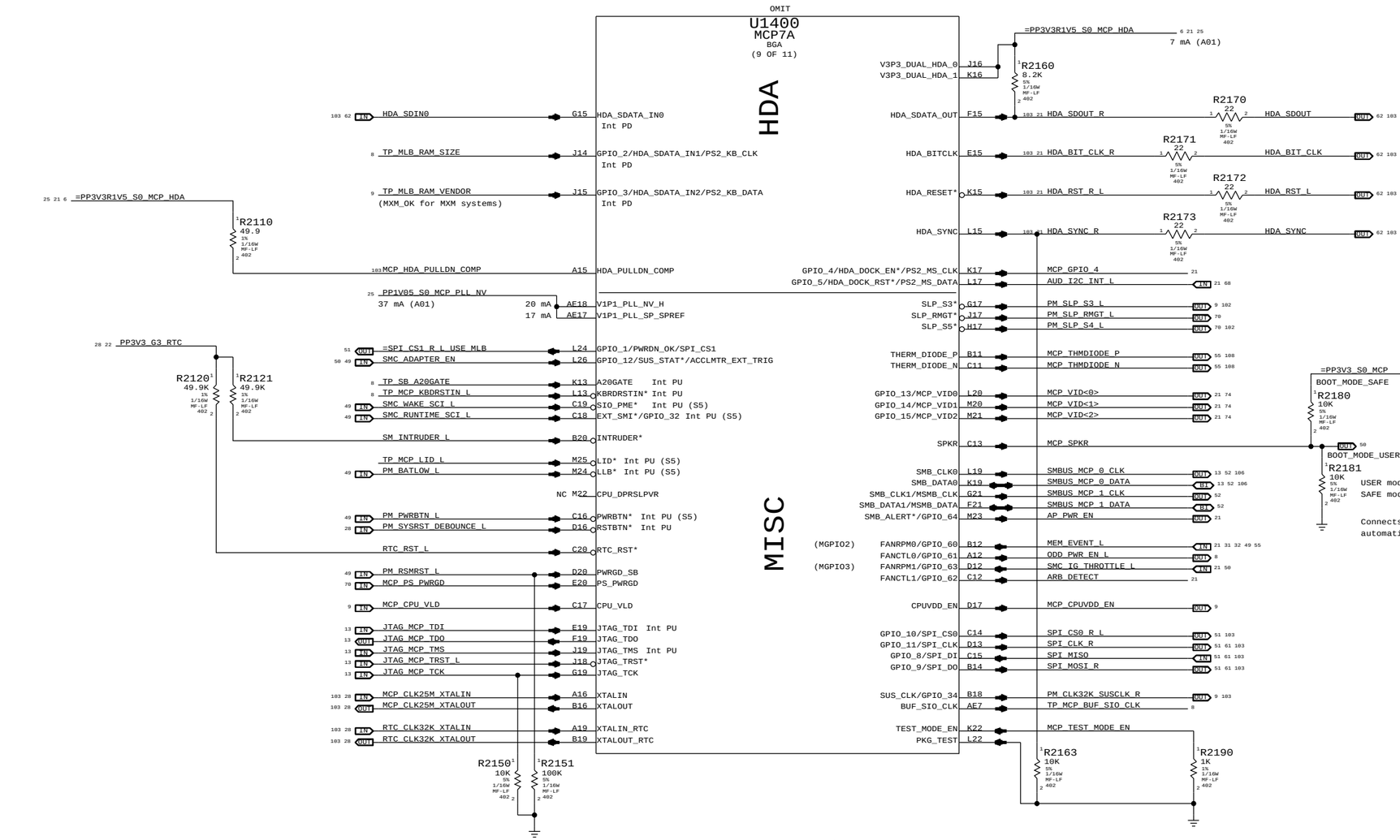
DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 20 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



OMIT

U1400
MCP7A
BGA
(11 OF 11)

AH26		AV40	
AH33		BA1	
AH34		BA4	
AH37		AW31	
AH38		AY6	
AJ39		L35	
AJ8		BC33	
AK10		BC37	
AK33		BC41	
AK34		AY14	
AK37		BC5	
AK4		C2	
AK40		D10	
AL36		D14	
AL40		D15	
AL5		D18	
AM10		D19	
AM16		D22	
AM18		D23	
AM20		D26	
AM22		D30	
AM24		D37	
AM26		D6	
AM30		E13	
AM34		E17	
AM35		E21	
AM37		E25	
AM38		E29	
AM5		E33	
AM6		F12	
AM7		F16	
AM9		F32	
AP26		F8	
AN28		G10	
AN30		G12	
AN39		G14	
AN4		G16	
Y7		BC12	
AP10		G22	
AU26		G24	
AP14		AW20	
AU14		G34	
AP28		G4	
AP32		G43	
AP34		G6	
AP36	GND	G8	GND
AP37		H11	
AP4		H15	
AP40		AW35	
AP7		H23	
AW23		AN8	
AR28		G40	
AR32		J12	
AR40		J8	
AT10		K10	
AR12		K12	
AT13		K18	
AT29		K26	
AT33		K37	
AT6		K4	
AT7		K40	
AT9		K8	
AY21		AU1	
AY22		L40	
L12		L43	
AU12		L5	
AU28		M10	
AP33		M34	
AU32		M35	
AR30		M37	
AU36		Y28	
AU38		Y33	
AU4		Y34	
G28		Y35	
F20		Y37	
AV28		Y38	
AV32		AB17	
AV36		AB16	
AV4		AN26	
AV7		AD7	
AW11		M11	
G20		AA4	
AR43		AB19	
AW43		AY13	
AY10		P11	
AV12		Y6	
AY30		T11	
AY33		V11	
AY34		Y11	
AY37		AH16	
AY38		T22	
AY41			

OMIT

U1400
MCP7A
BGA
(10 OF 11)

25 6 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25		R32	
AA26		P31	
AA27		AF32	
AA28		AE32	
AC16		AH32	
AC17		AJ32	
AC18		AK31	
AC19		AK32	
AC20		AD32	
AC21		AL31	
AA17		AB32	
AC23		AC32	
AC24		B41	
AC25		B42	
AC26		C40	
AC27		C41	
AC28		C42	
AD21		D39	
AD23		D40	
W27		D41	
V25		E38	
AA18		F39	
U25		E40	
AE19		F37	
AE21		F38	
AE23	V1P2_CPU_VTT	E39	
AE25		G36	
AE26		G37	
AE27		G38	
AE28		H35	
AE10		H37	
AE11		J34	
AA19		J35	
AH12		J36	
AF2		K33	
AE21		K34	
AF23		K35	
AE25		L32	
AF3	V1P0_CORE_VDD	L33	
AF4		L34	
AF7		M31	
AH23		M32	
AF9		M33	
AA20		N31	
AG10		N32	
AG11		P32	
AG12		Y32	
AG21		AA32	
AG23		T32	
AG25		U32	
AG3		V32	
AG4		W32	
AA21			
AG6	V1P2_CPUCLK_VTT	AG32	43 mA
AG7			
AG5			
AG8			
AG9			
AH1			
AH10			
AH11			
W26			
AH2			
AA23			
W28			
AH25			
Y21			
AH21			
AH3			
AH4			
AH5			
AH6			
AH7			
AH9			
AA24			
W21			
W23			
Y23			
W25			
AF12			
AA16			

=PP1V05_S0_MCP_FSB 6 14 25
1139 mA — 1182 mA (A01)

=PP3V3_S0_MCP 6 21 25
450 mA (A01)

AD10		
AE8		
AB10		
AD9		
Y10	V3P3	
AB11		
AA8		
Y9		

=PP3V3_S5_MCP 6 25
16 mA — 266 mA (A01)

G18		
H19		
J20	V3P3_DUAL	
K20		

250 mA

G26		
H27		
J28	V3P3_DUAL_USB	
K28		

=PP1V05_S5_MCP_VDD_AUXC 6 25
105 mA (A01)

T21		
U21	V1P0_VDD_AUXC	
V21		

28 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

A20 V3P3_VBAT

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K22 SYNC_DATE=09/02/2005

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 22 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 23 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

BLANK PAGE

Apple Inc.

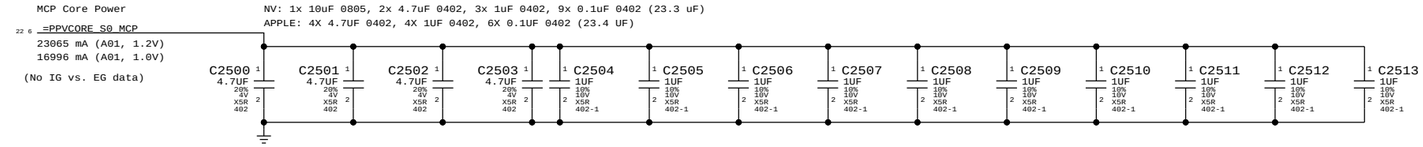
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

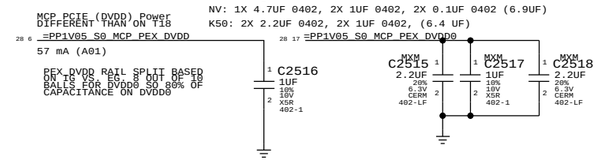
BRANCH

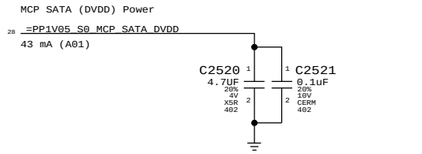
PAGE 24 OF 110

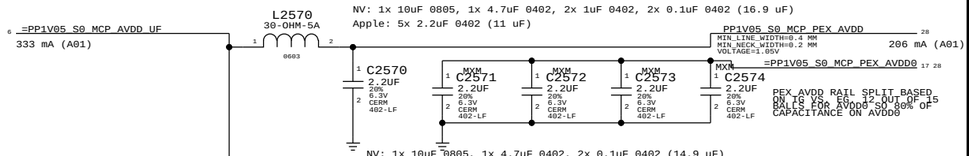
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

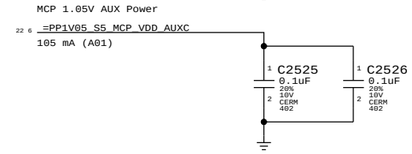


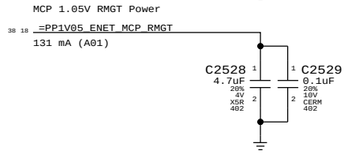
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

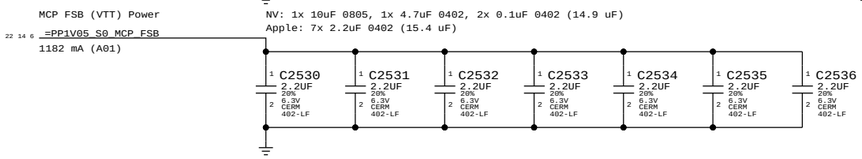


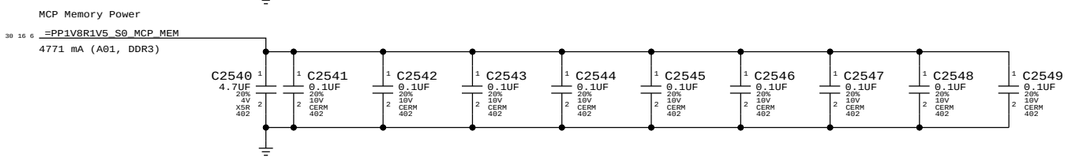


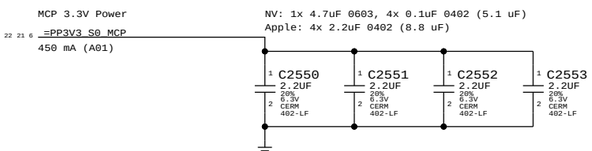


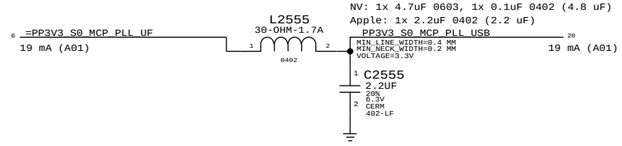


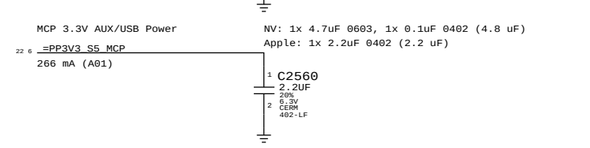


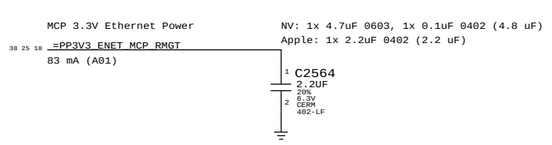


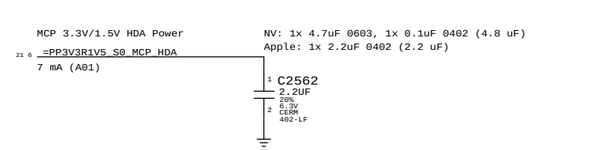


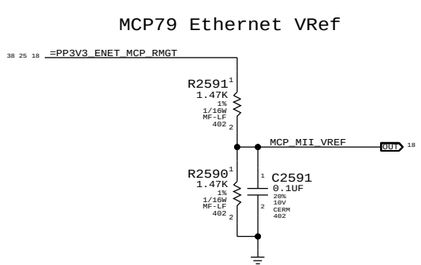


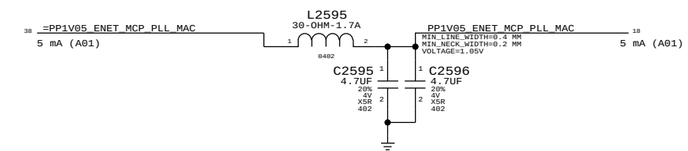


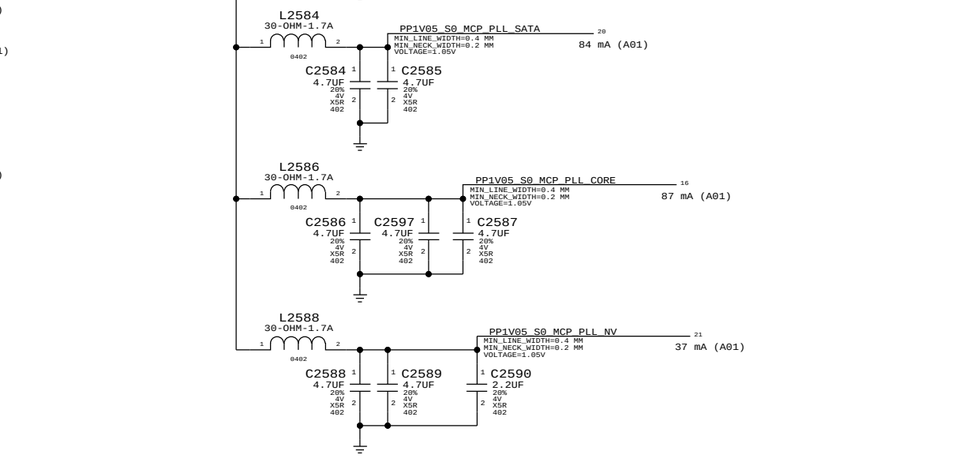












Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

MCP Standard Decoupling

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

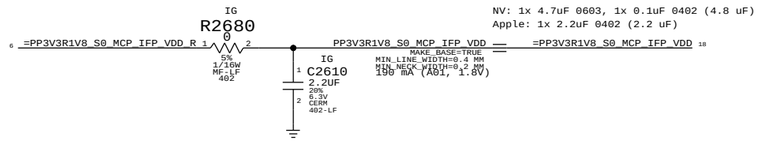
REVISION A.0.0

BRANCH

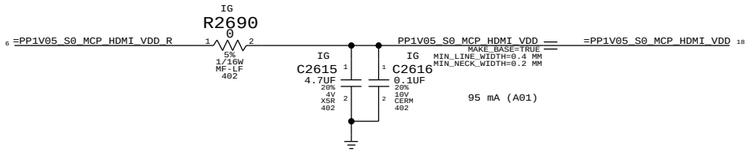
PAGE 25 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

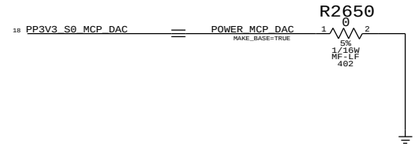
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

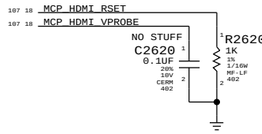


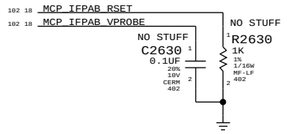
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



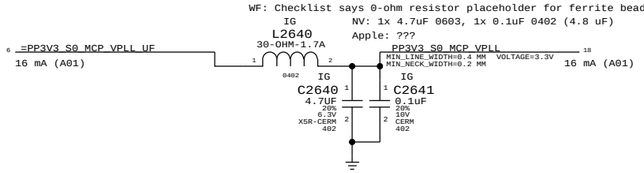
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM







WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 26 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=09/02/2009

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

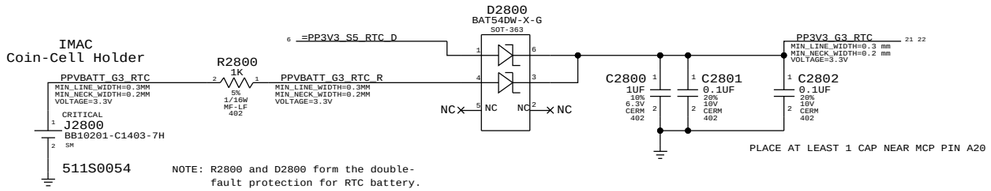
REVISION A.0.0

BRANCH

PAGE 27 OF 110

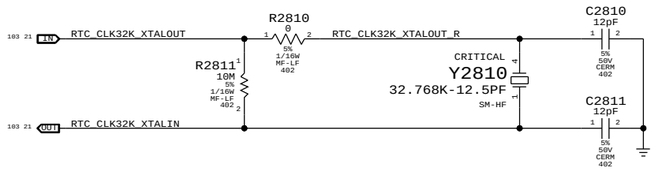
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

RTC Power Sources

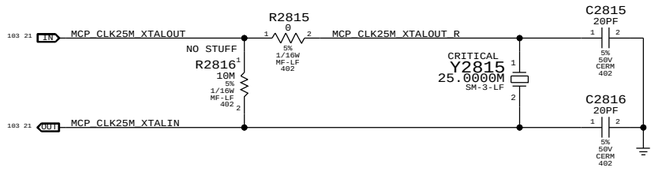


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

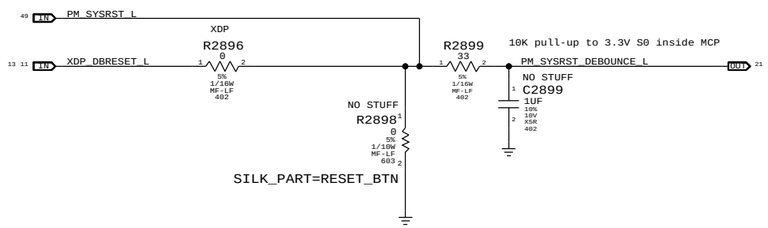
RTC Crystal



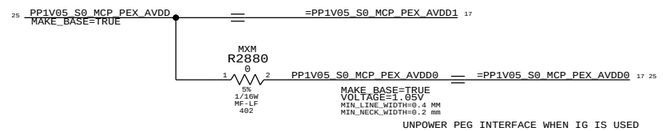
MCP 25MHz Crystal

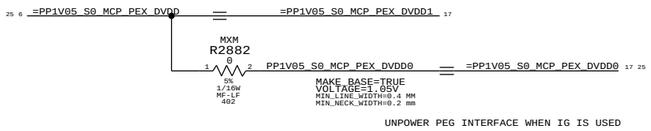


Reset Button

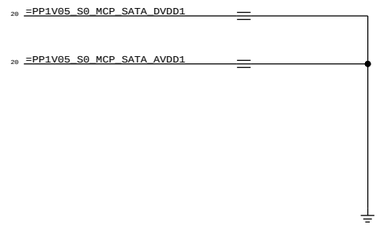


PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN





SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: SB Misc

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 28 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

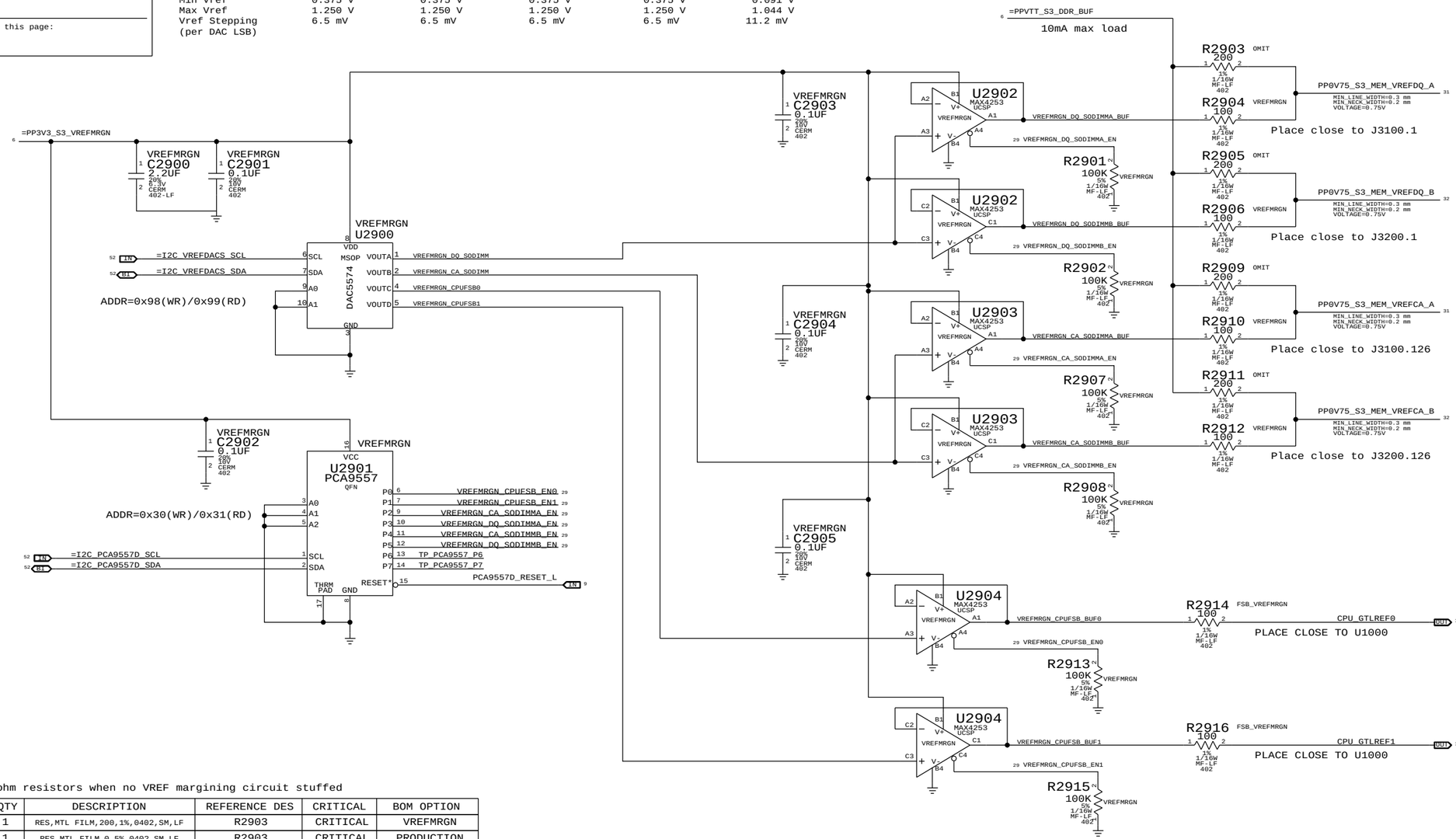
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
FSB/DDR3 Vref Margining

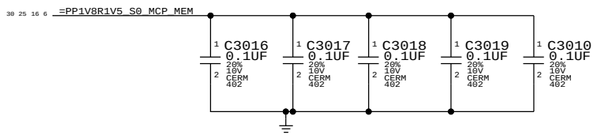
Apple Inc.

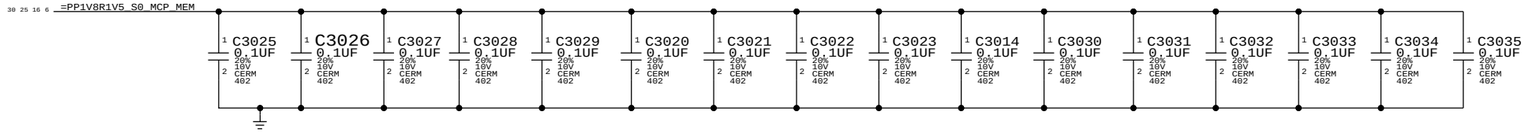
DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 29 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DIMM A (FURTHER FROM MCP)

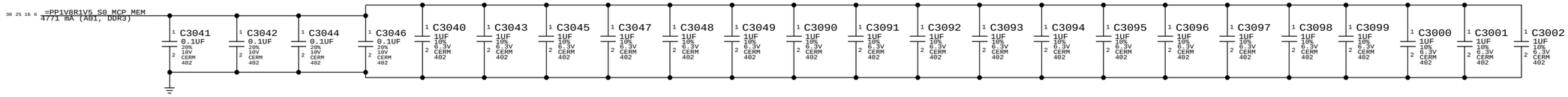
CAPS TO COUPLE MCP 1V5_S0_MEM

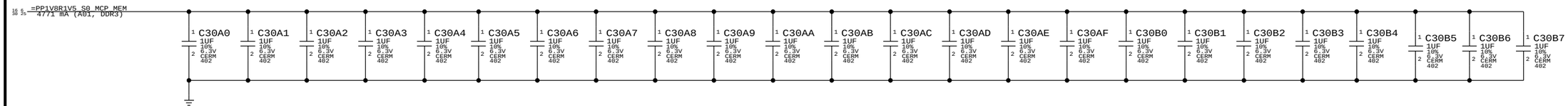
DIMM B (CLOSER TO MCP)

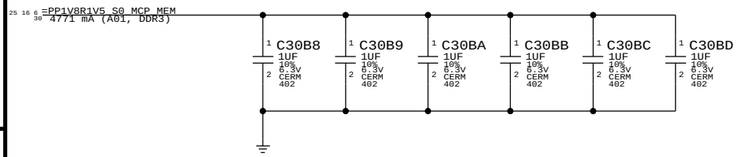




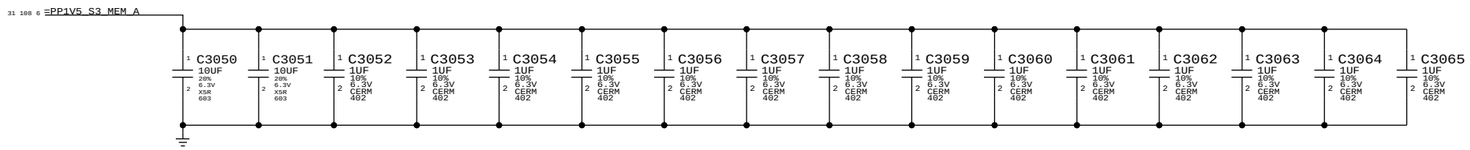
EXTRA DECOUPLING CAPS FOR MCP MEM RAIL



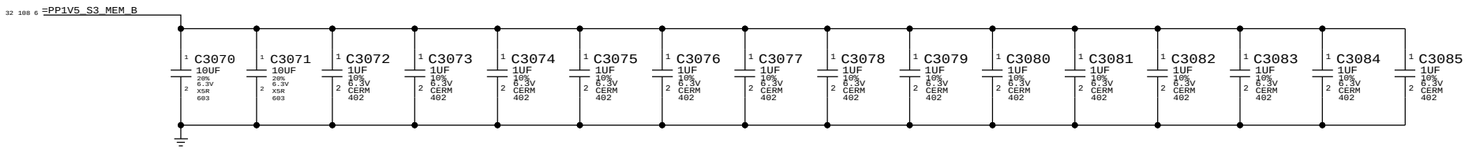




DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR



DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

MEMORY CAPS

Apple Inc.

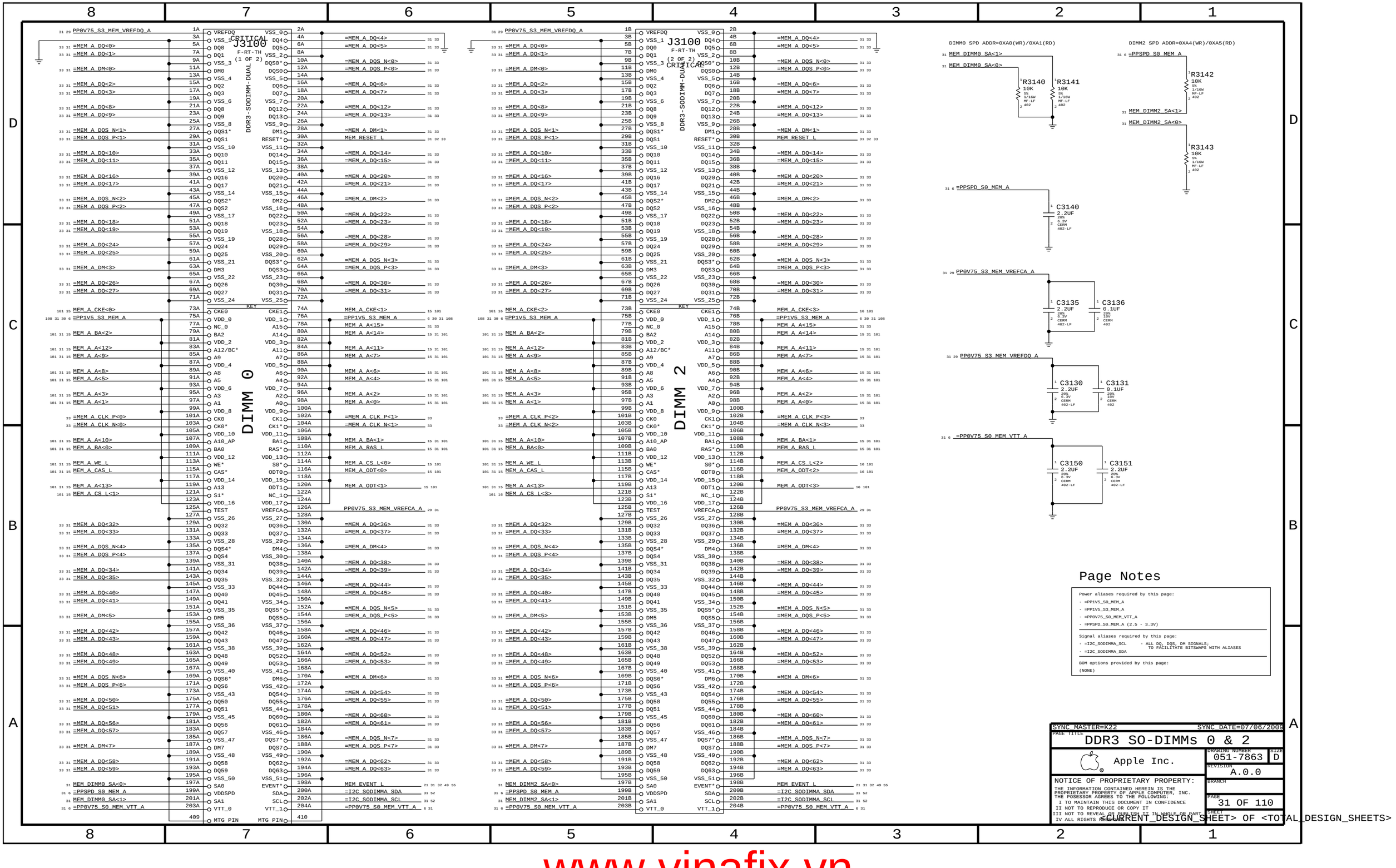
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 30 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



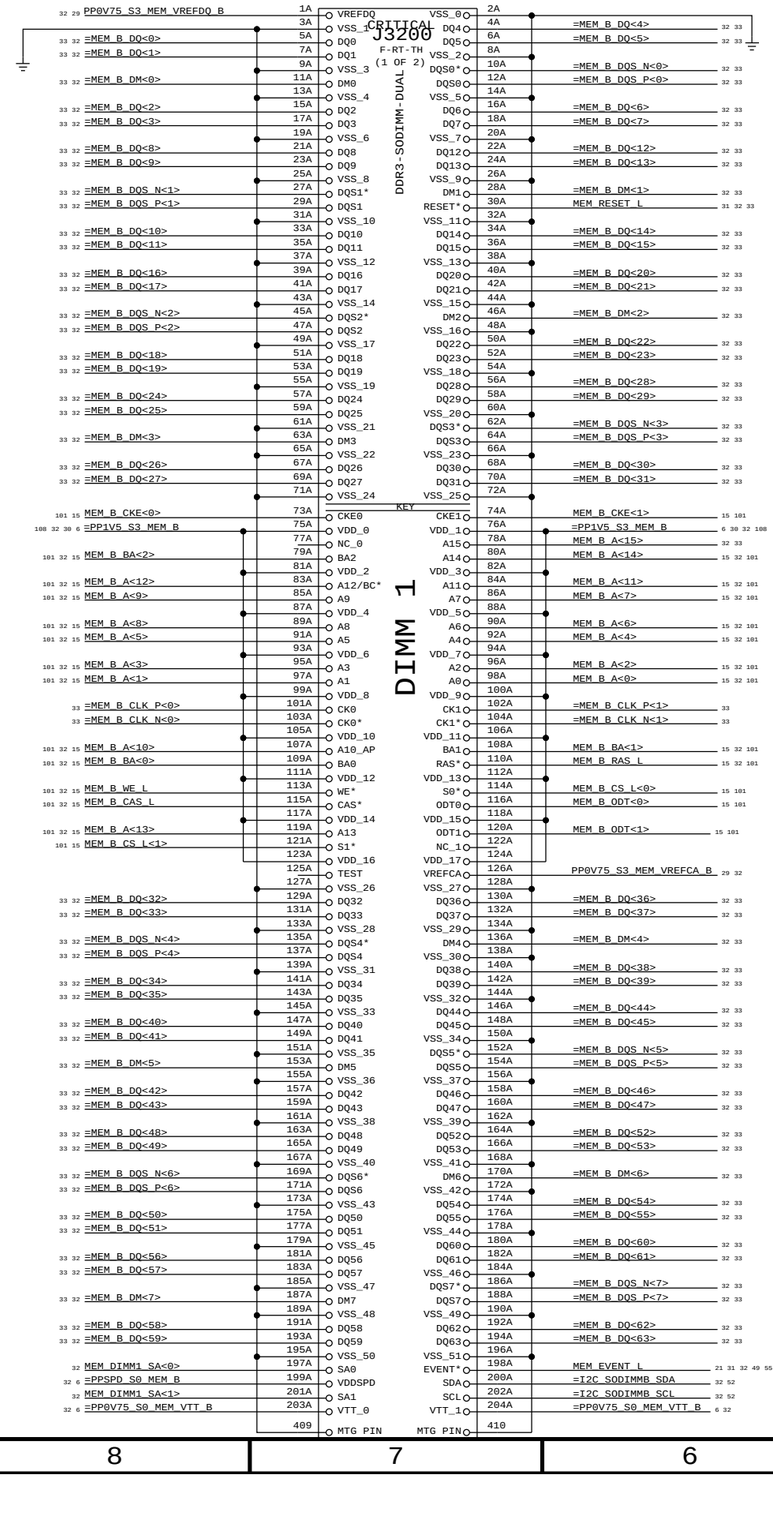
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K22	SYNC_DATE=07/06/2009
PAGE TITLE	DDR3 SO-DIMMs 0 & 2
Apple Inc.	DRAWING NUMBER 051-7863 · SIZE D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION A.0.0 · BRANCH · PAGE 31 OF 110 · SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 32 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE		=MEM_A_DQS_N<0>	31
MEM_A_DQS_P<0>	MAKE_BASE=TRUE		=MEM_A_DQS_P<0>	31
MEM_A_DM<0>	MAKE_BASE=TRUE		=MEM_A_DM<0>	31
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<7>	31
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<6>	31
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<5>	31
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<4>	31
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<3>	31
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<2>	31
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<1>	31
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<0>	31

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE		=MEM_A_DQS_N<1>	31
MEM_A_DQS_P<1>	MAKE_BASE=TRUE		=MEM_A_DQS_P<1>	31
MEM_A_DM<1>	MAKE_BASE=TRUE		=MEM_A_DM<1>	31
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<15>	31
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<14>	31
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<13>	31
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<12>	31
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<11>	31
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<10>	31
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<9>	31
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<8>	31

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE		=MEM_A_DQS_N<2>	31
MEM_A_DQS_P<2>	MAKE_BASE=TRUE		=MEM_A_DQS_P<2>	31
MEM_A_DM<2>	MAKE_BASE=TRUE		=MEM_A_DM<2>	31
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<23>	31
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<22>	31
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<21>	31
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<20>	31
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<19>	31
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<18>	31
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<17>	31
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<16>	31

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE		=MEM_A_DQS_N<3>	31
MEM_A_DQS_P<3>	MAKE_BASE=TRUE		=MEM_A_DQS_P<3>	31
MEM_A_DM<3>	MAKE_BASE=TRUE		=MEM_A_DM<3>	31
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<31>	31
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<30>	31
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<29>	31
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<28>	31
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<27>	31
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<26>	31
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<25>	31
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<24>	31

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE		=MEM_A_DQS_N<4>	31
MEM_A_DQS_P<4>	MAKE_BASE=TRUE		=MEM_A_DQS_P<4>	31
MEM_A_DM<4>	MAKE_BASE=TRUE		=MEM_A_DM<4>	31
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<39>	31
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<38>	31
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<37>	31
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<36>	31
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<35>	31
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<34>	31
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<33>	31
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<32>	31

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE		=MEM_A_DQS_N<5>	31
MEM_A_DQS_P<5>	MAKE_BASE=TRUE		=MEM_A_DQS_P<5>	31
MEM_A_DM<5>	MAKE_BASE=TRUE		=MEM_A_DM<5>	31
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<47>	31
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<46>	31
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<45>	31
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<44>	31
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<43>	31
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<42>	31
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<41>	31
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<40>	31

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE		=MEM_A_DQS_N<6>	31
MEM_A_DQS_P<6>	MAKE_BASE=TRUE		=MEM_A_DQS_P<6>	31
MEM_A_DM<6>	MAKE_BASE=TRUE		=MEM_A_DM<6>	31
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<55>	31
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<54>	31
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<53>	31
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<52>	31
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<51>	31
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<50>	31
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<49>	31
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<48>	31

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE		=MEM_A_DQS_N<7>	31
MEM_A_DQS_P<7>	MAKE_BASE=TRUE		=MEM_A_DQS_P<7>	31
MEM_A_DM<7>	MAKE_BASE=TRUE		=MEM_A_DM<7>	31
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<63>	31
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<62>	31
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<57>	31
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<56>	31
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<59>	31
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<58>	31
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<61>	31
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<60>	31

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE		=MEM_B_DQS_N<0>	32
MEM_B_DQS_P<0>	MAKE_BASE=TRUE		=MEM_B_DQS_P<0>	32
MEM_B_DM<0>	MAKE_BASE=TRUE		=MEM_B_DM<0>	32
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<7>	32
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<6>	32
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<1>	32
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<0>	32
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<3>	32
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<2>	32
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<5>	32
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<4>	32

MCP CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE		=MEM_B_DQS_N<1>	32
MEM_B_DQS_P<1>	MAKE_BASE=TRUE		=MEM_B_DQS_P<1>	32
MEM_B_DM<1>	MAKE_BASE=TRUE		=MEM_B_DM<1>	32
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<15>	32
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<14>	32
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<13>	32
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<12>	32
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<11>	32
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<10>	32
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<9>	32
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<8>	32

MCP CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE		=MEM_B_DQS_N<2>	32
MEM_B_DQS_P<2>	MAKE_BASE=TRUE		=MEM_B_DQS_P<2>	32
MEM_B_DM<2>	MAKE_BASE=TRUE		=MEM_B_DM<2>	32
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<23>	32
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<22>	32
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<21>	32
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<20>	32
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<19>	32
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<18>	32
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<17>	32
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<16>	32

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE		=MEM_B_DQS_N<3>	32
MEM_B_DQS_P<3>	MAKE_BASE=TRUE		=MEM_B_DQS_P<3>	32
MEM_B_DM<3>	MAKE_BASE=TRUE		=MEM_B_DM<3>	32
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<31>	32
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<30>	32
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<29>	32
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<28>	32
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<27>	32
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<26>	32
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<25>	32
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<24>	32

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE		=MEM_B_DQS_N<4>	32
MEM_B_DQS_P<4>	MAKE_BASE=TRUE		=MEM_B_DQS_P<4>	32
MEM_B_DM<4>	MAKE_BASE=TRUE		=MEM_B_DM<4>	32
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<39>	32
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<38>	32
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<37>	32
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<36>	32
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<35>	32
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<34>	32
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<33>	32
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<32>	32

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE		=MEM_B_DQS_N<5>	32
MEM_B_DQS_P<5>	MAKE_BASE=TRUE		=MEM_B_DQS_P<5>	32
MEM_B_DM<5>	MAKE_BASE=TRUE		=MEM_B_DM<5>	32
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<47>	32
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<46>	32
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<45>	32
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<44>	32
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<43>	32
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<42>	32
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<41>	32
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<40>	32

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

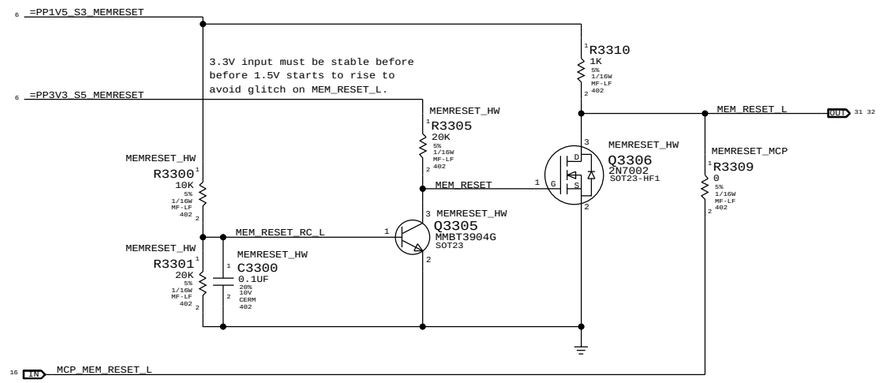
MEM_B_DQS_N<6>	MAKE_BASE=TRUE		=MEM_B_DQS_N<6>	32
MEM_B_DQS_P<6>	MAKE_BASE=TRUE		=MEM_B_DQS_P<6>	32
MEM_B_DM<6>	MAKE_BASE=TRUE		=MEM_B_DM<6>	32
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<55>	32
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<54>	32
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<53>	32
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<52>	32
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<51>	32
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<50>	32
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<49>	32
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<48>	32

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE		=MEM_B_DQS_N<7>	32
MEM_B_DQS_P<7>	MAKE_BASE=TRUE		=MEM_B_DQS_P<7>	32
MEM_B_DM<7>	MAKE_BASE=TRUE		=MEM_B_DM<7>	32
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<63>	32
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<62>	32
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<61>	32
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<60>	32
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<59>	32
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<58>	32
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<57>	32
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<56>	32

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



MCP MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE		=MEM_A_CLK_P<0>	31
MEM_A_CLK_N<0>	MAKE_BASE=TRUE		=MEM_A_CLK_N<0>	31
MEM_A_CLK_P<1>	MAKE_BASE=TRUE		=MEM_A_CLK_P<1>	31
MEM_A_CLK_N<1>	MAKE_BASE=TRUE		=MEM_A_CLK_N<1>	31
MEM_A_CLK_P<3>	MAKE_BASE=TRUE		=MEM_A_CLK_P<2>	31
MEM_A_CLK_N<3>	MAKE_BASE=TRUE		=MEM_A_CLK_N<2>	31
MEM_A_CLK_P<4>	MAKE_BASE=TRUE		=MEM_A_CLK_P<3>	31
MEM_A_CLK_N<4>	MAKE_BASE=TRUE		=MEM_A_CLK_N<3>	31

MEM_B_CLK_P<0>	MAKE_BASE=TRUE		=MEM_B_CLK_P<0>	32
MEM_B_CLK_N<0>	MAKE_BASE=TRUE		=MEM_B_CLK_N<0>	32
MEM_B_CLK_P<1>	MAKE_BASE=TRUE		=MEM_B_CLK_P<1>	32
MEM_B_CLK_N<1>	MAKE_BASE=TRUE		=MEM_B_CLK_N<1>	32
MEM_B_CLK_P<3>	MAKE_BASE=TRUE		=MEM_B_CLK_P<2>	32
MEM_B_CLK_N<3>	MAKE_BASE=TRUE		=MEM_B_CLK_N<2>	32
MEM_B_CLK_P<4>	MAKE_BASE=TRUE		=MEM_B_CLK_P<3>	32
MEM_B_CLK_N<4>	MAKE_BASE=TRUE		=MEM_B_CLK_N<3>	32

MCP MEMORY TEST POINT ALIASING

TP_MEM_A_A<15>	MAKE_BASE=TRUE		MEM_A_A<15>	31
TP_MEM_B_A<15>	MAKE_BASE=TRUE		MEM_B_A<15>	32

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

DDR3 SUPPORT AND BITSWAPS

Apple Inc.

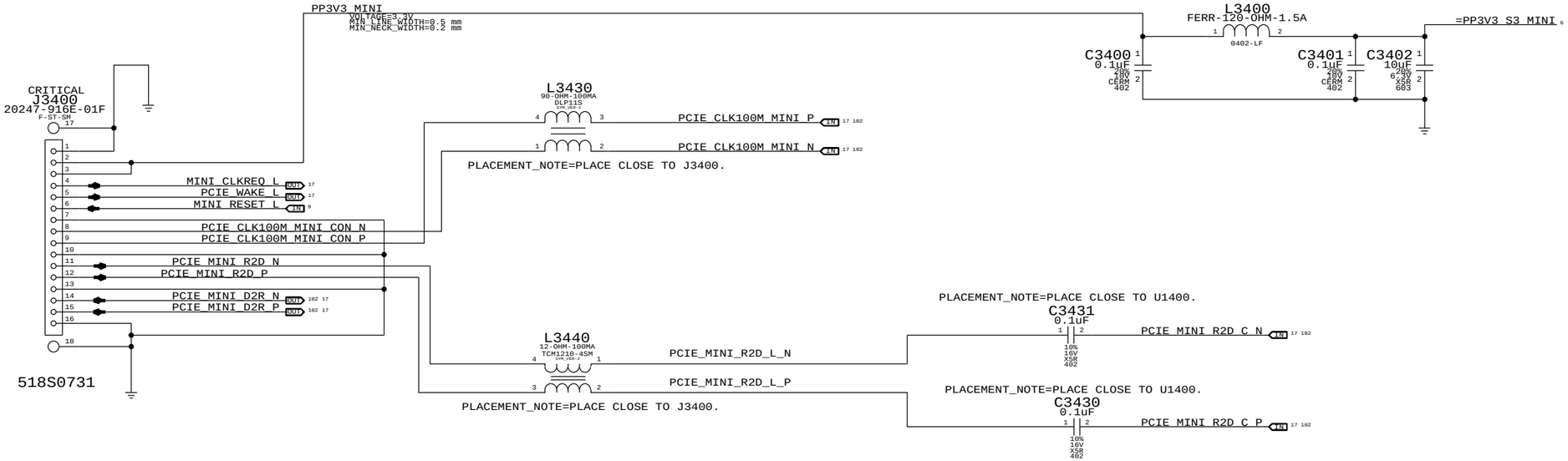
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 33 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K22 SYNC_DATE=05/28/2009

PAGE TITLE

PCI-E Wireless Connector

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 34 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 35 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

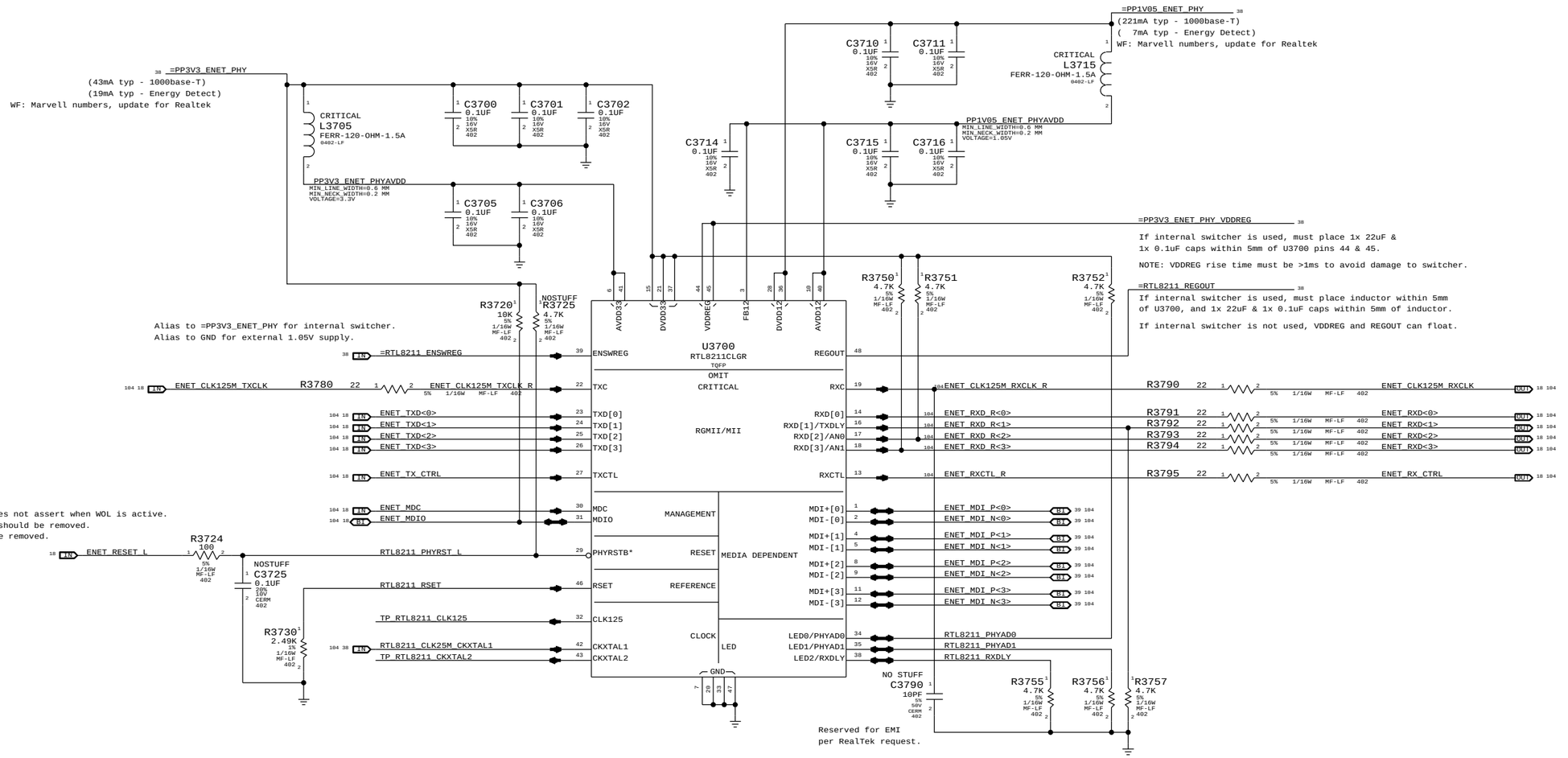
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 36 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

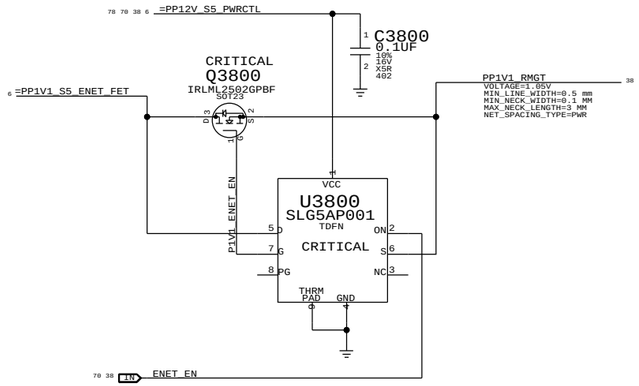
SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: Ethernet PHY (RTL8211CL)

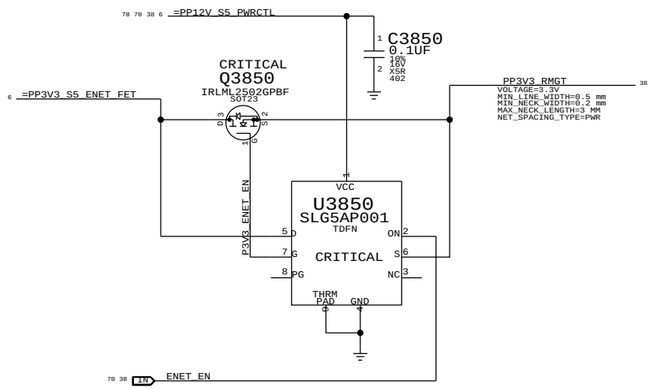
Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 37 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.1V ENET FET



3.3V ENET FET



ENET ALIASES

38 PP1V1_RMGT
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_RMGT 18 25
=PP1V05_ENET_MCP_PLL_MAC 25
=PP1V05_ENET_PHY 37

38 PP3V3_RMGT
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 18 25
=PP3V3_ENET_PHY 37

MAKE_BASE=TRUE
=RTL8211_ENSWREG 37

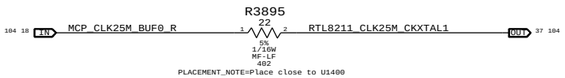
NOTE: NOT USING THE BUILT-IN 1.05V REGULATOR OF THE PHY

NC_RTL8211_REGOUT
MAKE_BASE=TRUE
NO_TEST=TRUE
=RTL8211_REGOUT 37

NC_PP3V3_ENET_PHY_VDDREG
MAKE_BASE=TRUE
NO_TEST=TRUE
=PP3V3_ENET_PHY_VDDREG 37

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



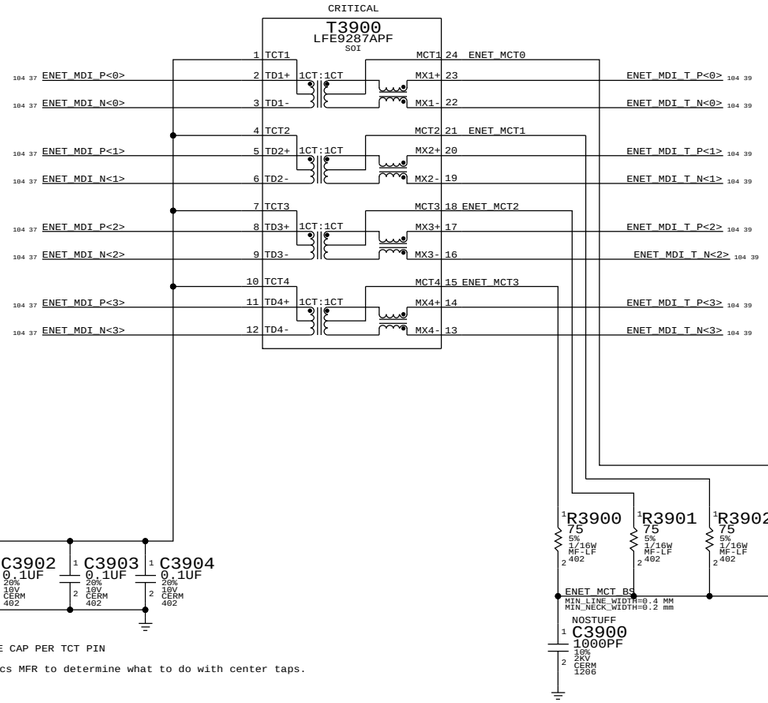
PLACEMENT_NOTE=Place close to U1400

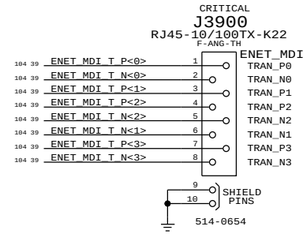
SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
Ethernet Support

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 38 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 39 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 40 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Power Aliases:

FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.

FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.

For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

PCI EXPRESS

1394B OHCI & PHY

Single-port: PC[0:2] = '000'

Multiple-ports: PC[0:2] = '100'

Alias =FWPHY_PC0 as appropriate

Unused Ports:

TP/NC TPBIASx

TP/NC TPAx_P/TPAx_N

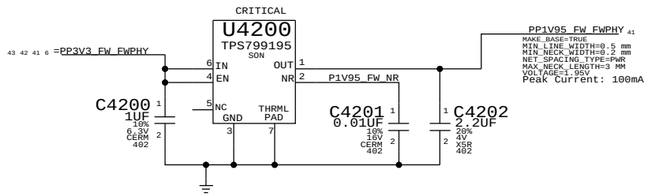
Ground TPBx_P/TPBx_N

DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors

Strap DSx high on unused ports.

SYNC_MASTER=K22	SYNC_DATE=09/02/2009
PAGE TITLE: FireWire LLC/PHY (XIO2213B)	
Apple Inc.	DRAWING NUMBER: 051-7863 SIZE: D
	REVISION: A.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE: 41 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1394 PHY 1.95V SUPPLY



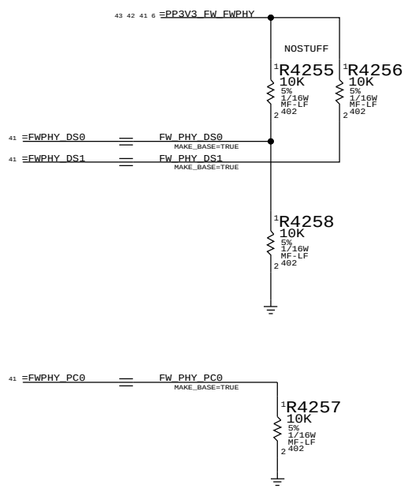
FireWire Aliases For Connectivity

=FW_CLKREQ_L — FW_CLKREQ_L (MAKE_BASE=TRUE)

=FW_PME_L — FW_PME_L (MAKE_BASE=TRUE)

=PPVP_FW_PHY_CPS — PPVP_FW_PHY_CPS (MAKE_BASE=TRUE)

1394 PHY STRAPPING OPTIONS

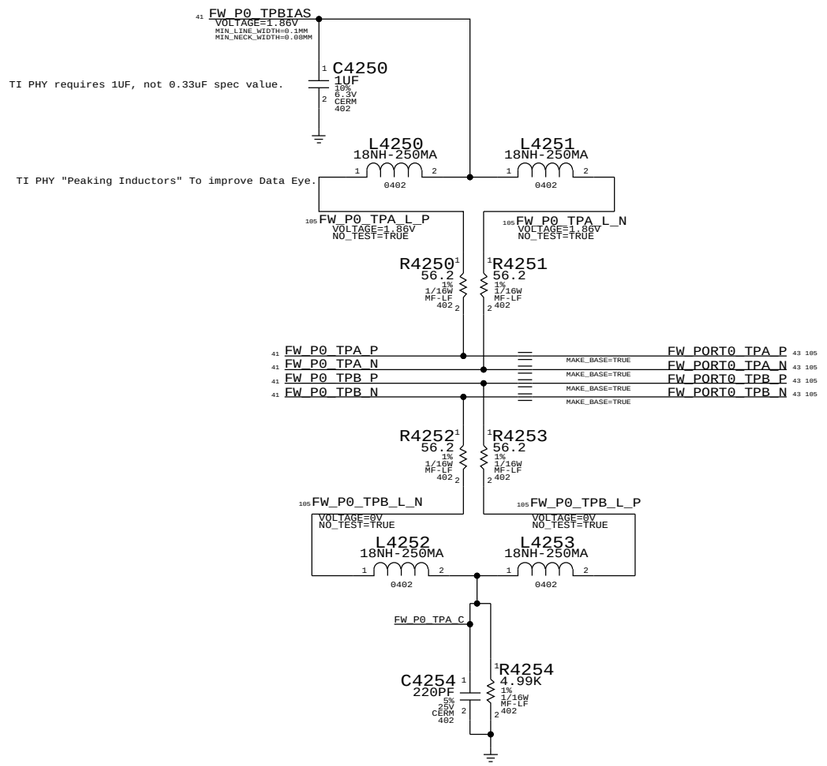


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS — NC_FW_PORT1_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P1_TPA_P — NC_FW_PORT1_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P1_TPA_N — NC_FW_PORT1_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPBIAS — NC_FW_PORT2_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPA_P — NC_FW_PORT2_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPA_N — NC_FW_PORT2_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: FW: 1394B MISC

Apple Inc.

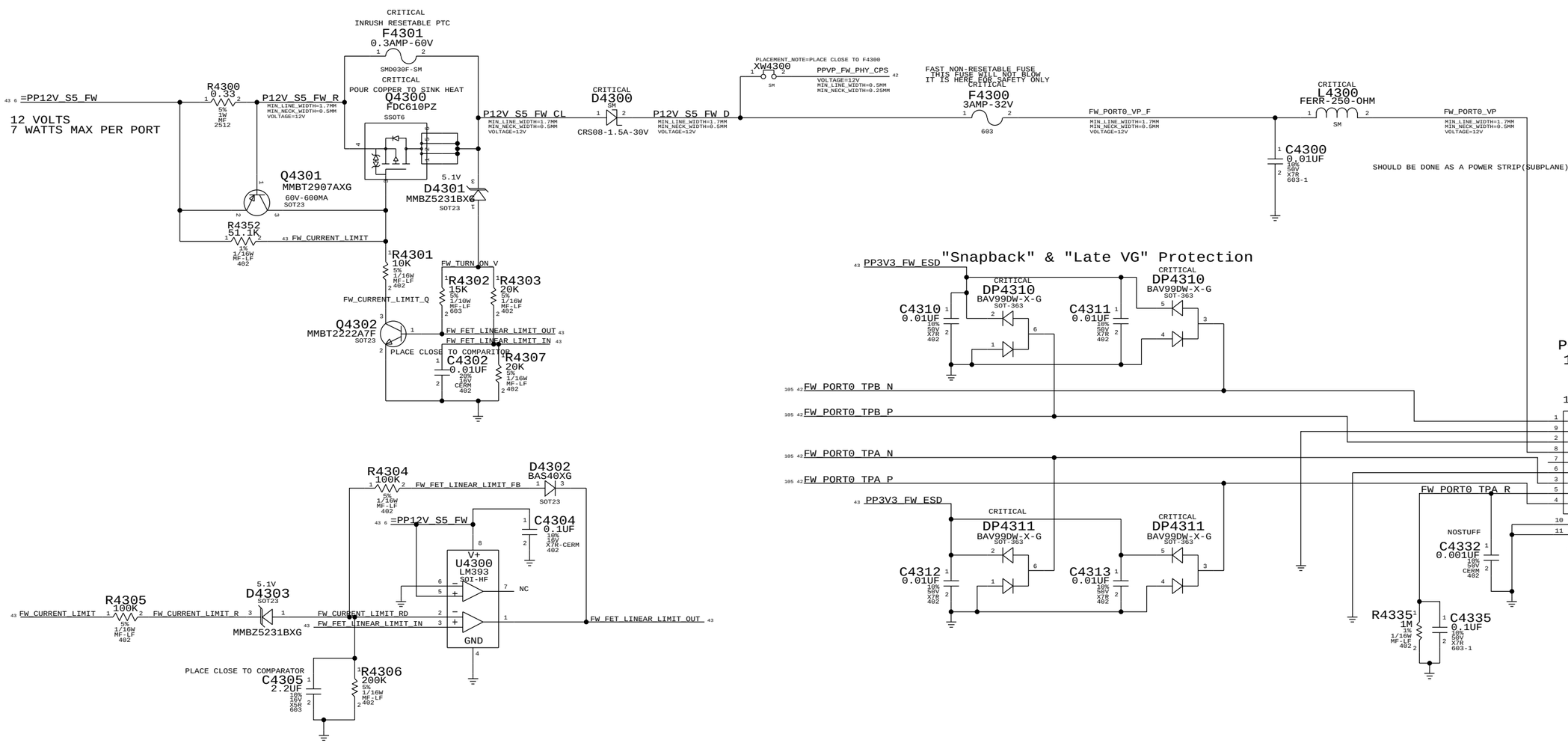
DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 42 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=K22 SYNC DATE=09/02/2009

PAGE TITLE

FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 43 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

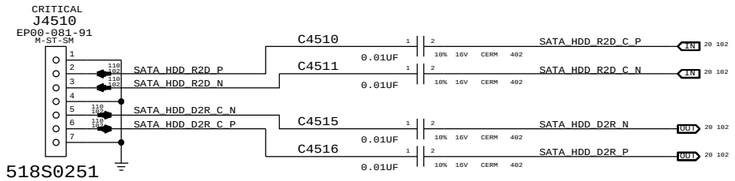
REVISION A.0.0

BRANCH

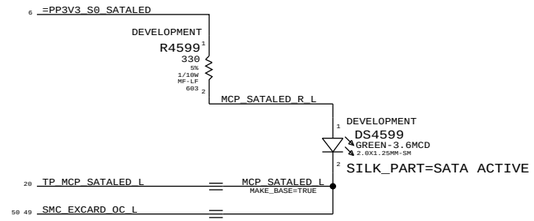
PAGE 44 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SATA PORT A0 FOR HDD

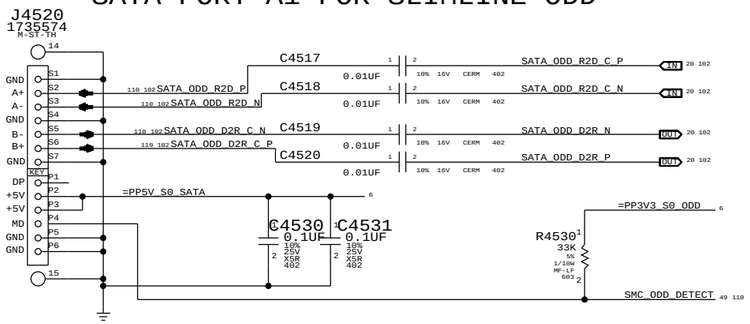


SATA Activity LED



518-0361

SATA PORT A1 FOR SLIMLINE ODD



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 45 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

USB/SMC DEBUG MUX

=PP5V_S3_USB
USB_EXTC_OC_L
USB_EXTD_OC_L
USB_PWR_ENA_L
R4600 10K 5% 1/16W MF-LF 402
U4601 TPS2060 MSOP
C4605 0.1UF 20% 16V CERM 402
C4606 150UF 20% 6.3V POLY-TANT CASE-D2-SM
Q4600 2N7002 SOT23-HF
PM_EN_USB_PWR
C4621 0.1UF 20% 16V CERM 402
C4631 0.1UF 20% 16V CERM 402
=PP3V3_S5_SMCUSBMUX
C4650 0.1UF 20% 16V CERM 402
U4650 PI3USB102ZLE TQFN MOJOMUX
SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
R4651 0 5% 1/10W MF-LF 402 PRODUCTION
R4652 0 5% 1/10W MF-LF 402 PRODUCTION
L4630 FERR-250-OHM SM
C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4631 120-OHM-90MA DLP0NS
USB_D_MUXED_N
USB_D_MUXED_P
USB_PORT3_N
USB_PORT3_P
J4630 USB-K22 F-ANG-TH
VDD D- D+ GND VBUS DATA- DATA+
514-0659
D4630 RCLAMP0502N SLP1210N6
PORT 3

=PP5V_S3_USB
USB_EXTA_OC_L
USB_EXTB_OC_L
U4600 TPS2060 MSOP
C4601 0.1UF 20% 16V CERM 402
C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM1
C4603 0.1UF 20% 16V CERM 402
C4611 0.1UF 20% 16V CERM 402
L4610 FERR-250-OHM SM
C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4611 120-OHM-90MA DLP0NS
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P
J4610 USB-K22 F-ANG-TH1
514-0672
D4610 RCLAMP0502N SLP1210N6
PORT 1

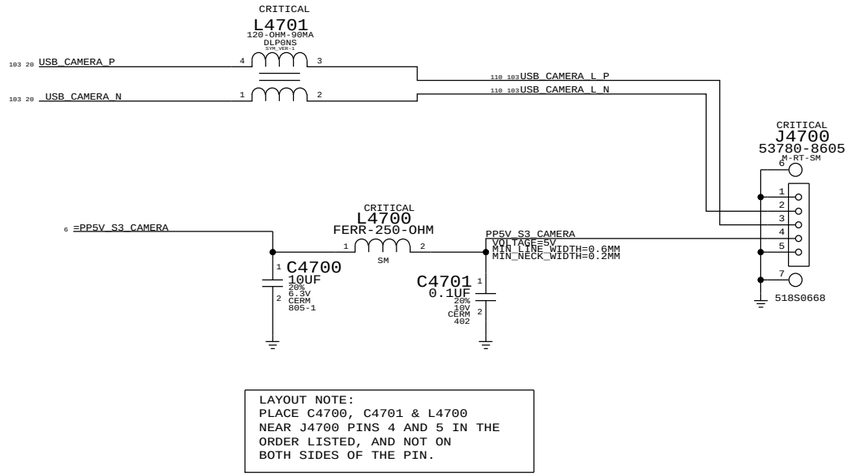
L4620 FERR-250-OHM SM
C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4621 120-OHM-90MA DLP0NS
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P
J4620 USB-K22 F-ANG-TH
514-0659
D4620 RCLAMP0502N SLP1210N6
PORT 2

L4600 FERR-250-OHM SM
C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4601 120-OHM-90MA DLP0NS
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P
J4600 USB-K22 F-ANG-TH1
514-0672
D4600 RCLAMP0502N SLP1210N6
PORT 0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0238	1	330UF, TANT-POLY BULK CAP	C4602	CRITICAL	K23
128S0225	1	150UF, TANY-POLY BULK CAP	C4606	CRITICAL	K22

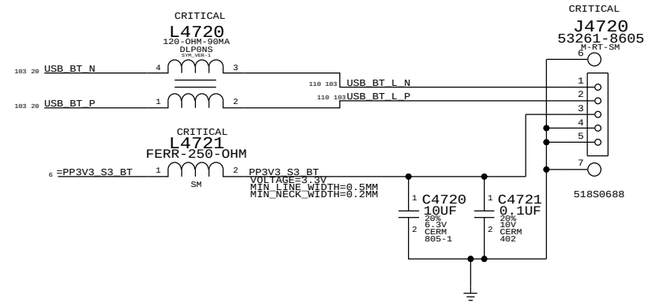
SYNC_MASTER=K22 SYNC_DATE=09/02/2009
PAGE TITLE
EXTERNAL USB CONNECTORS
Apple Inc.
DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 46 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CAMERA CONNECTOR & FILTER

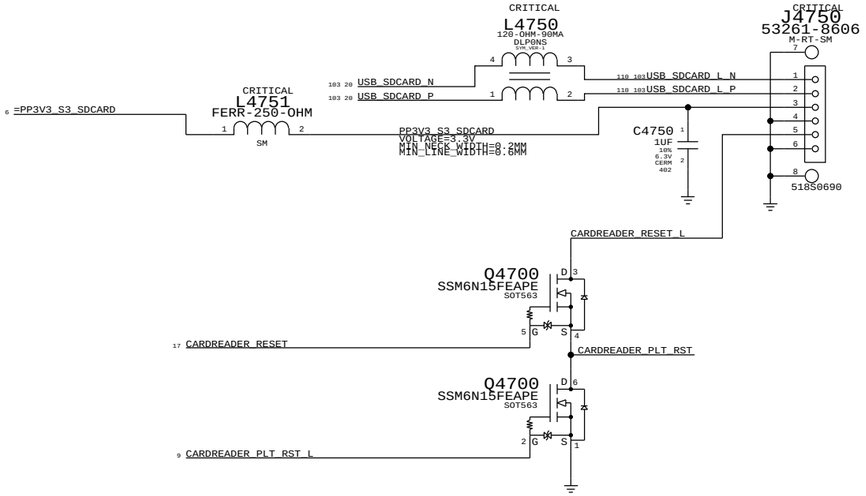


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

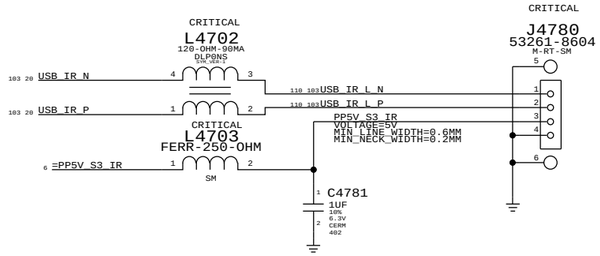
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



IR RECEIVER CONNECTOR



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE_TITLE
Internal USB Connections

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 47 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863

SIZE D

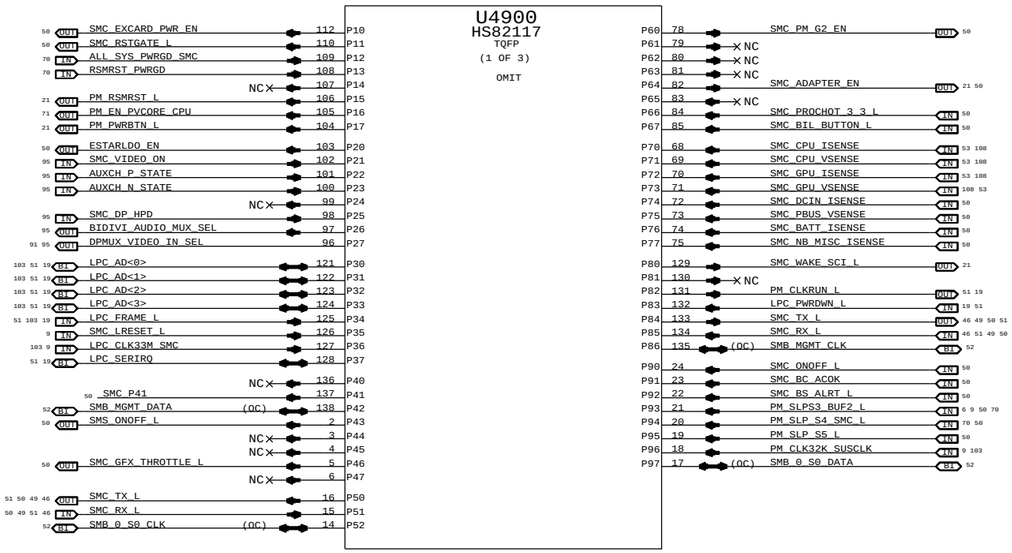
REVISION A.0.0

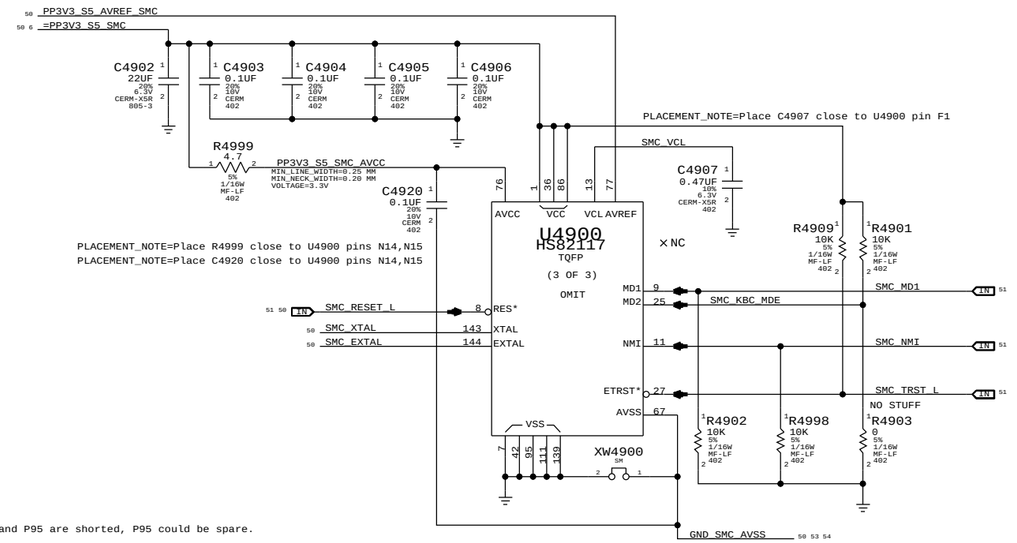
BRANCH

PAGE 48 OF 110

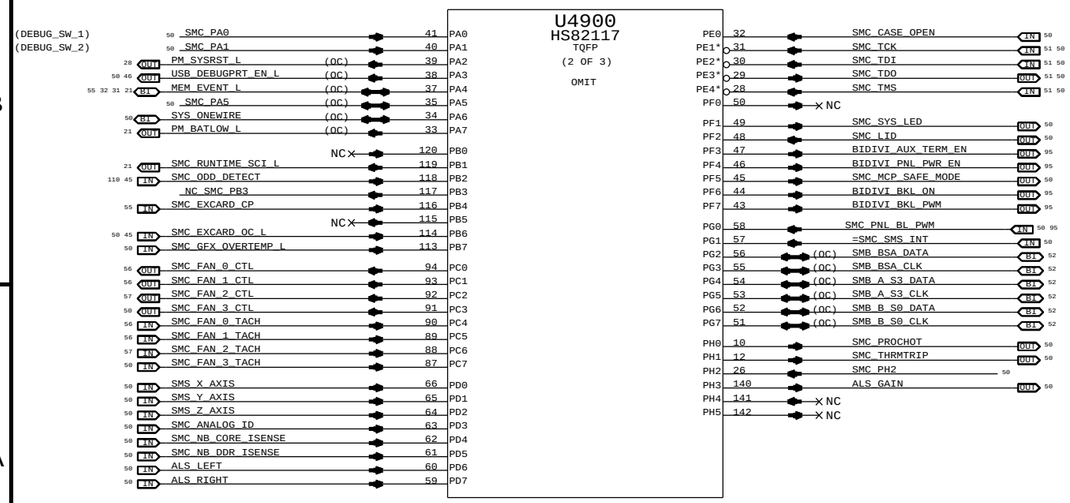
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

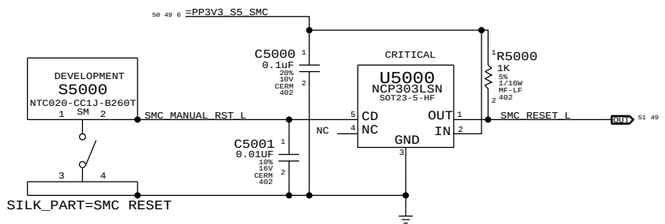
SYNC_MASTER=MARKVIDEO SYNC_DATE=03/12/2009

PAGE TITLE: SMC

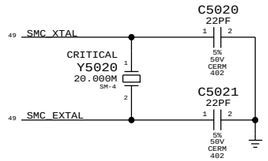
Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 49 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

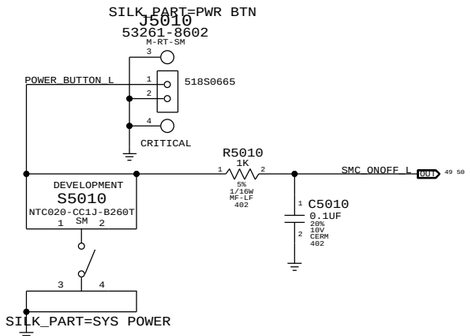
SMC Reset Button / Brownout Detect



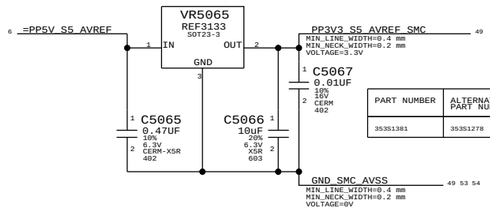
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_LEFT	NC_ALS_LEFT	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_RIGHT	NC_ALS_RIGHT	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED TP/NC ALIASES

ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
ESTARLDO_EN	TP_ESTARLDO_EN	MAKE_BASE=TRUE	

ANALOG SENSORS

SMC_DCIN_ISENSE	SMC_CPU_INPUT_ISENSE	MAKE_BASE=TRUE	53
SMC_PBUS_VSENSE	SMC_CPU_INPUT_VSENSE	MAKE_BASE=TRUE	53
SMS_X_AXIS	SMC_1V5_S0_VSENSE	MAKE_BASE=TRUE	108 54
SMS_Y_AXIS	SMC_MCP_CORE_VSENSE	MAKE_BASE=TRUE	108 54
SMC_NB_DDR_ISENSE	SMC_1V5_S0_ISENSE	MAKE_BASE=TRUE	108 54
SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	54 108
SMC_BATT_ISENSE	SMC_UNUSED_ADC_PORT7	MAKE_BASE=TRUE	
SMC_NB_MISC_ISENSE			

R5050 10K 5% 1/10W MF-LF 402

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L	MXM_ALERT_L	MAKE_BASE=TRUE	85
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	MAKE_BASE=TRUE	85

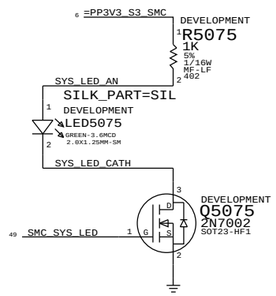
IG R5020 51 5% 1/16W MF-LF 402 — SMC_IG_THROTTLE_L (MAKE_BASE=TRUE) 21

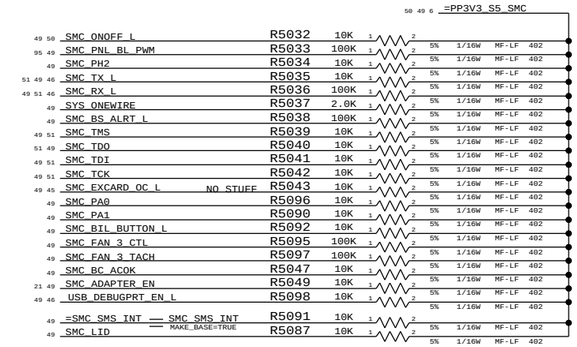
R5019 0 5% 1/16W MF-LF 402

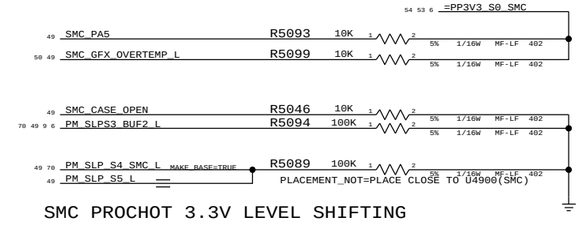
SMC_MCP_SAFE_MODE — MCP_SPKR 21

FOR <RDAR://PROBLEM/5925345>

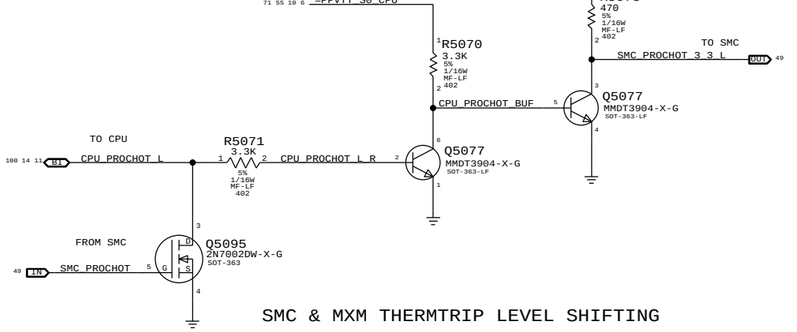
SIL: FOR DEVELOPMENT USE ONLY



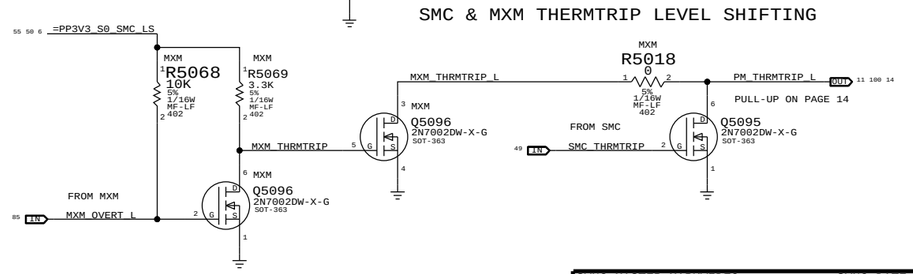




SMC PROCHOT 3.3V LEVEL SHIFTING

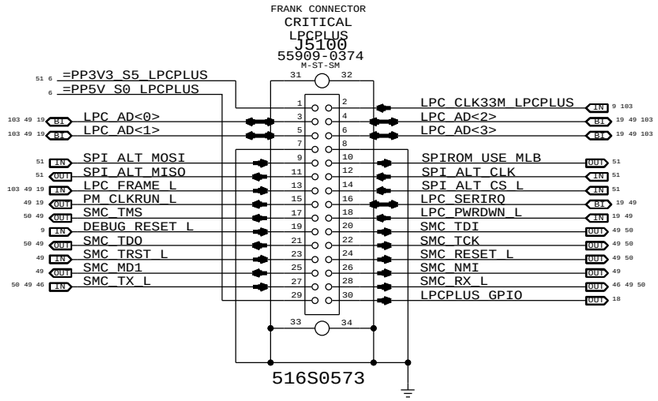


SMC & MXM THERMTRIP LEVEL SHIFTING

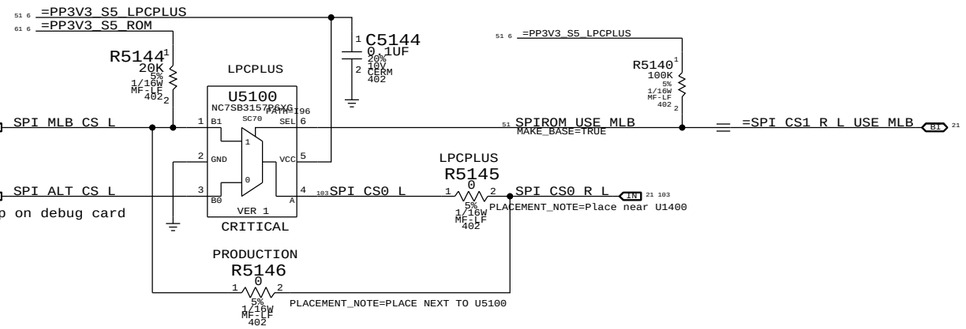


SYNC MASTER=MARKVIDEO	SYNC DATE=03/12/2009
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-7863 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 50 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

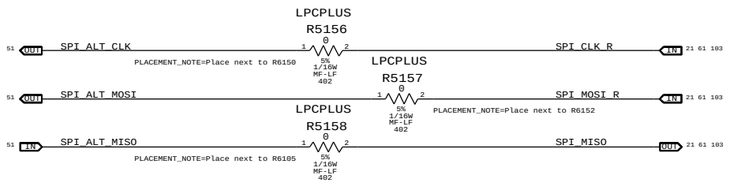
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

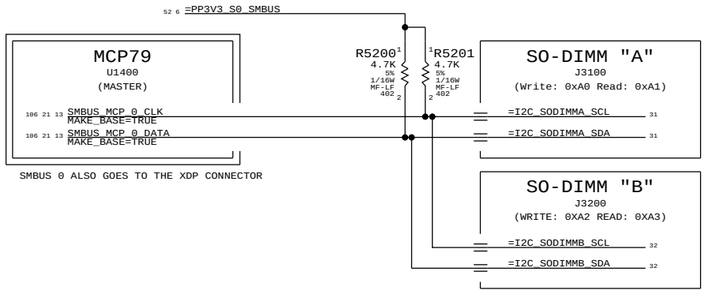
REVISION A.0.0

BRANCH

PAGE 51 OF 110

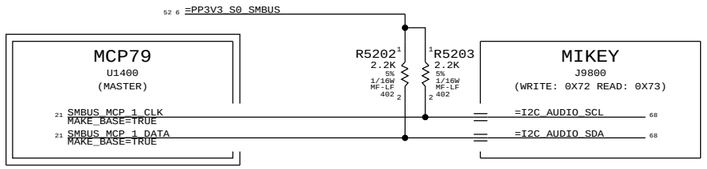
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP79 SMBUS "0" CONNECTIONS

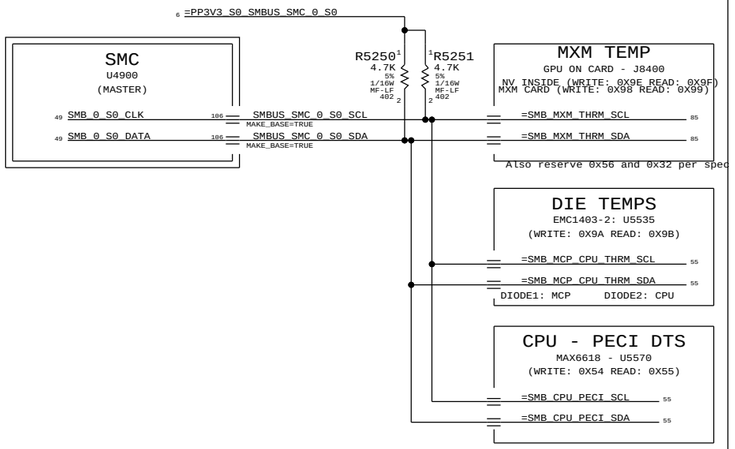


SMBUS 0 ALSO GOES TO THE XDP CONNECTOR

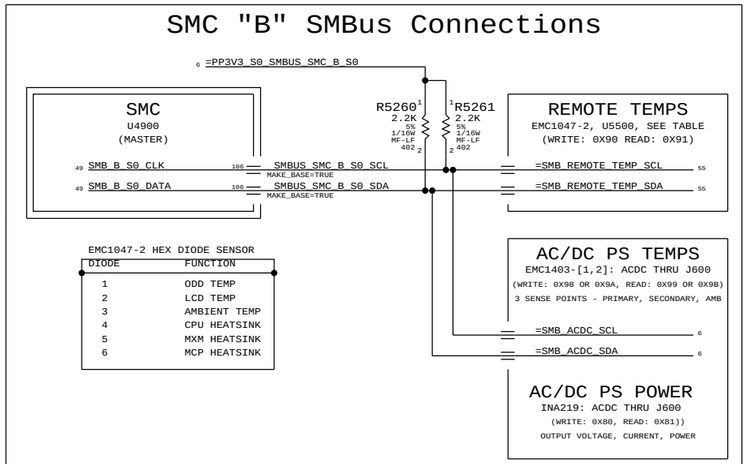
MCP79 SMBUS "1" CONNECTIONS



SMC "0" SMBus Connections



SMC "B" SMBus Connections

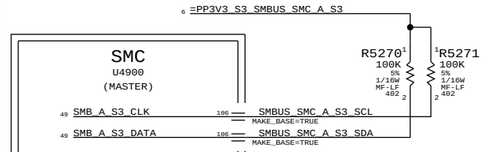


EMC1047-2 HEX DIODE SENSOR

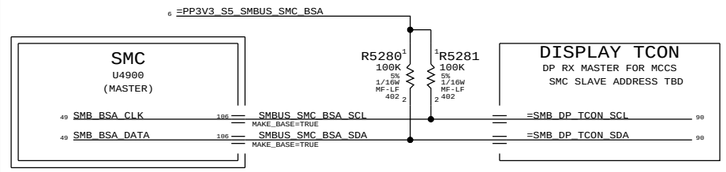
DIODE	FUNCTION
1	ODD TEMP
2	LCD TEMP
3	AMBIENT TEMP
4	CPU HEATSINK
5	MXM HEATSINK
6	MCP HEATSINK

SMC "A" SMBus Connections

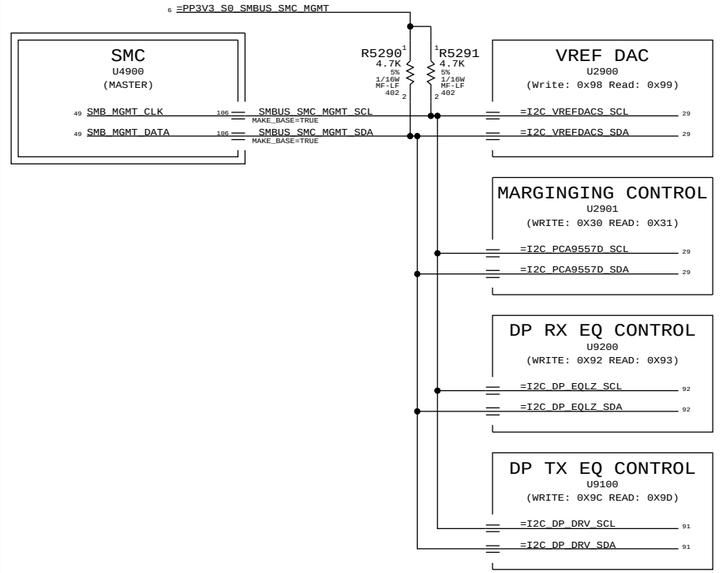
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



POTENTIAL SMC SLAVE SMBUS CONNECTIONS



SMC "MANAGEMENT" SMBUS CONNECTIONS



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

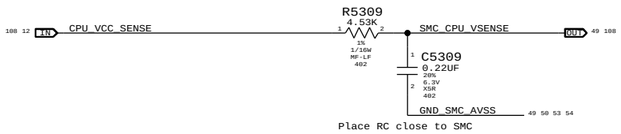
REVISION: A.0.0

BRANCH:

PAGE: 52 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

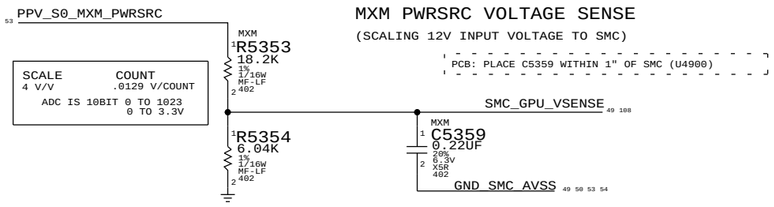
CPU Voltage Sense / Filter



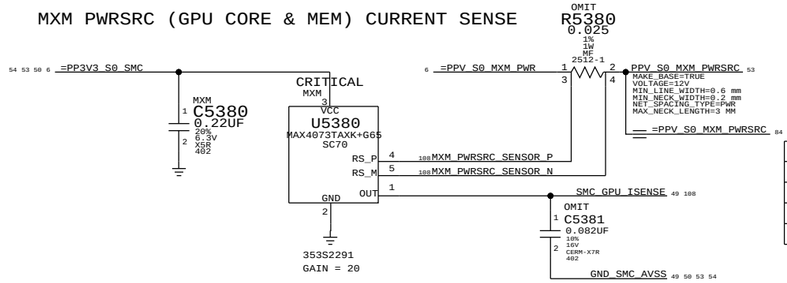
Place RC close to SMC

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

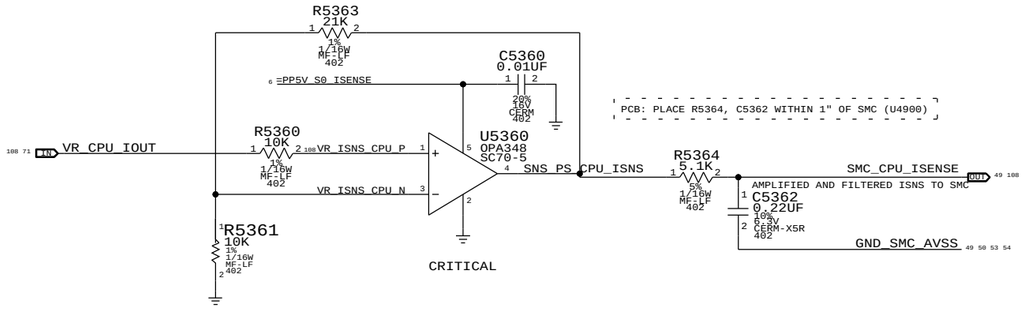
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

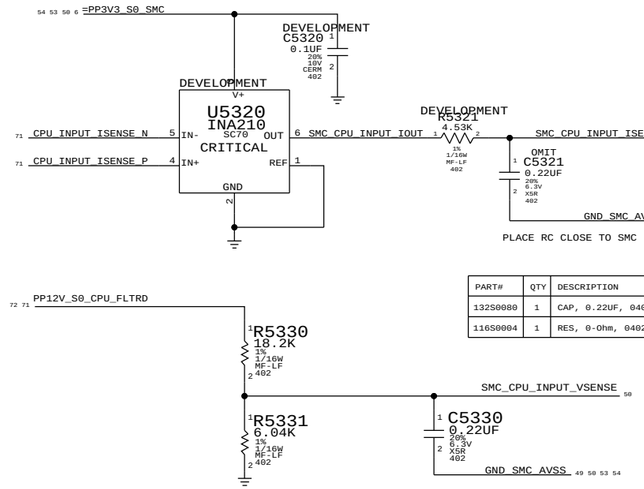
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
107S0111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
132S0242	1	CAP,0.082UF,402	C5381		MXM
116S0090	1	RES,10KOHM,5%,402	C5381		IG

CPU CURRENT SENSE AMP & FILTER



CPU CORE INPUT SIDE CURRENT & VOLTAGE SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5321		DEVELOPMENT
116S0004	1	RES, 0-Ohm, 0402	C5321		PRODUCTION

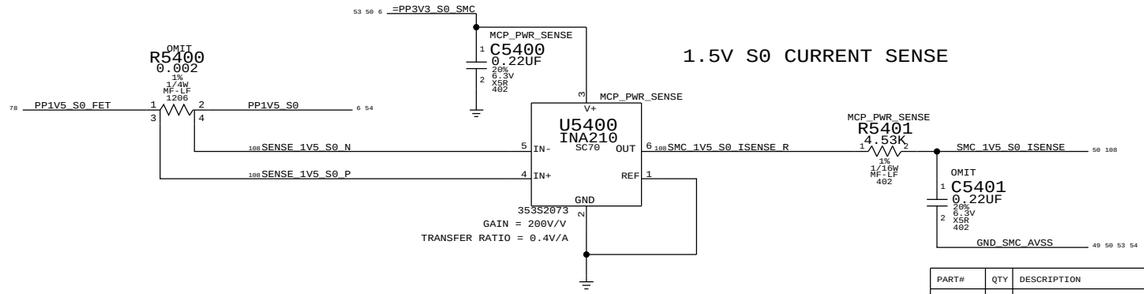
SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
CPU/MXM CURRENT AND VOLTAGE SENSE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 53 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

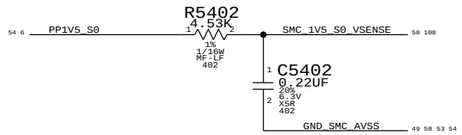
1.5V S0 CURRENT SENSE



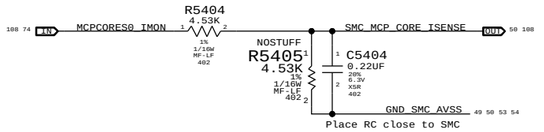
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5401		MCP_PWR_SENSE
116S0004	1	RES, 0 OHM, 402	C5401		PRODUCTION

1.5V S0 VOLTAGE SENSE

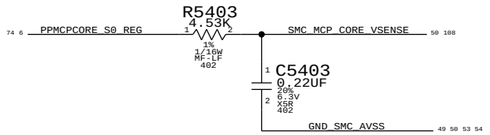


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



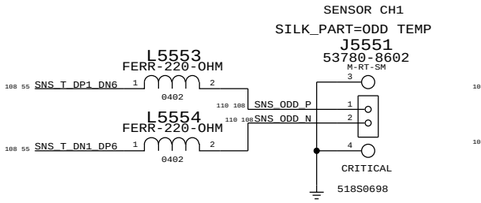
SYNC_MASTER=K22 SYNC_DATE=09/02/2009

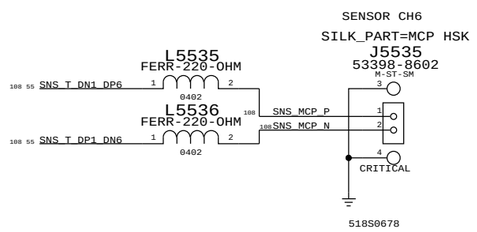
PAGE TITLE
MCP CURRENT AND VOLTAGE SENSE

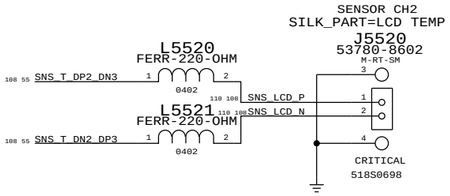
Apple Inc.

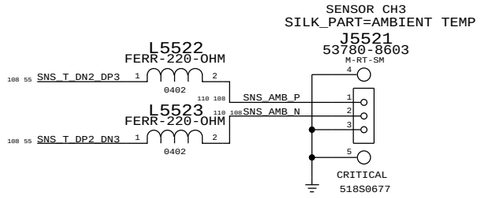
DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 54 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

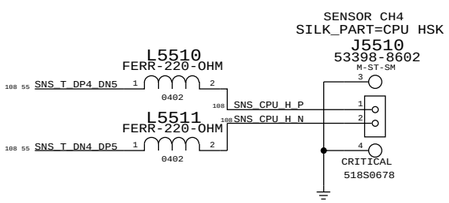


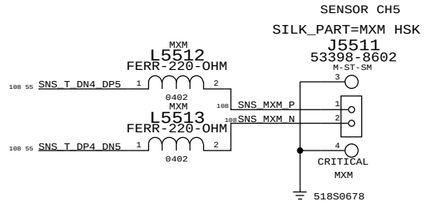






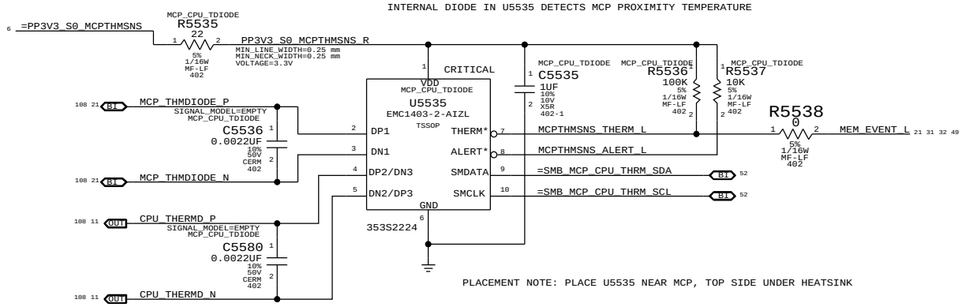
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU



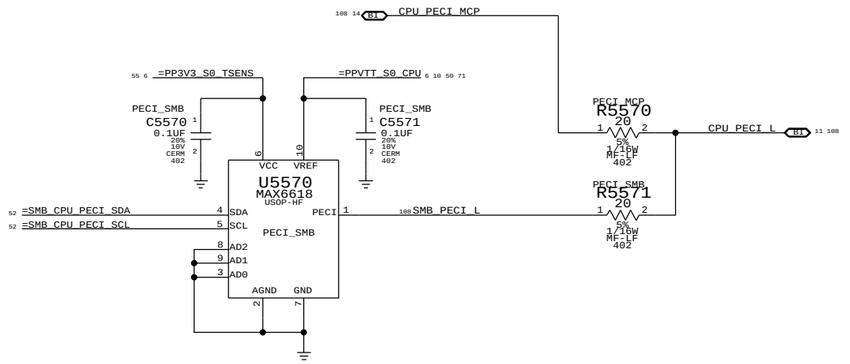


MCP & CPU T-Diode Thermal Sensor

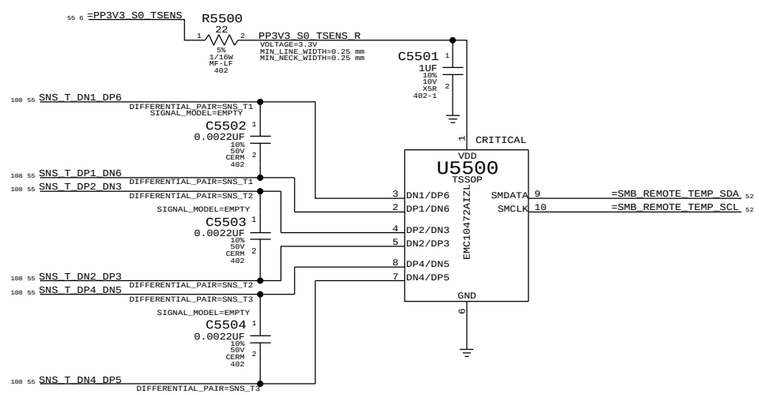
INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE



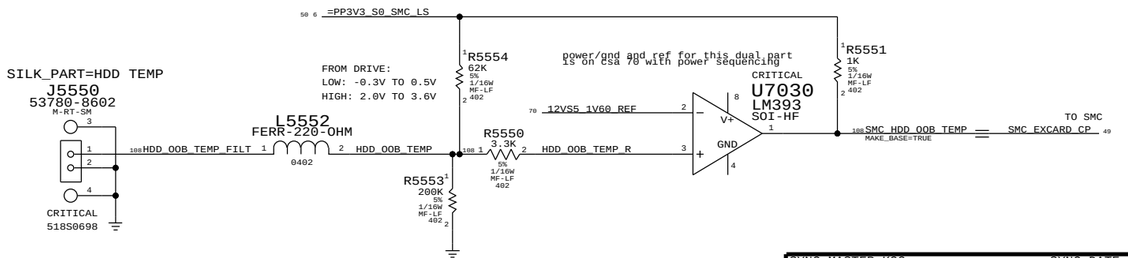
CPU PECI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



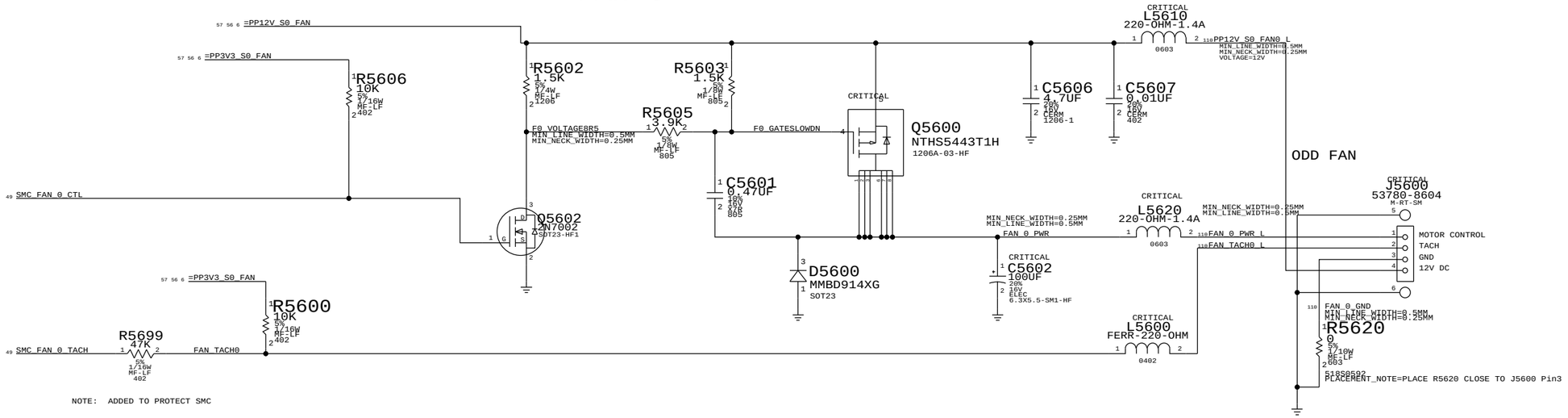
SYNC_MASTER=K22 SYNC_DATE=09/07/2005

PAGE TITLE: Thermal Sensors

Apple Inc.

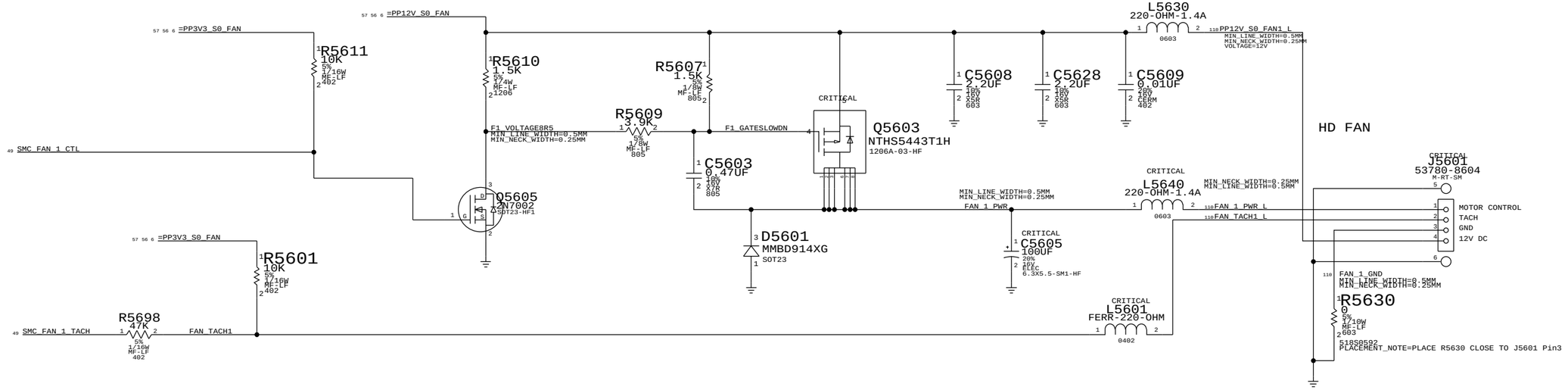
DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 55 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

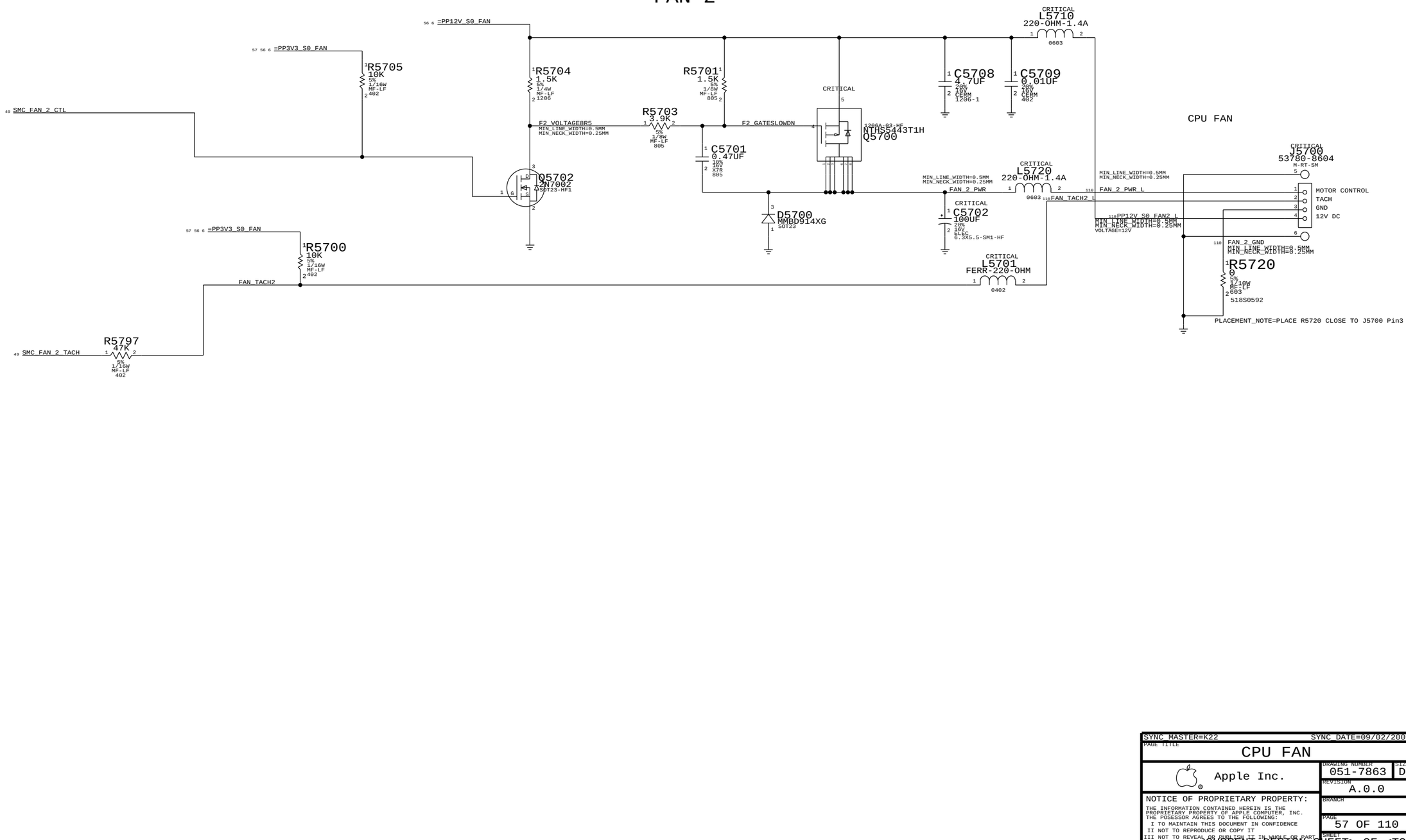
REVISION: A.0.0

BRANCH:

PAGE: 56 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FAN 2



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: CPU FAN

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 57 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 58 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 59 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

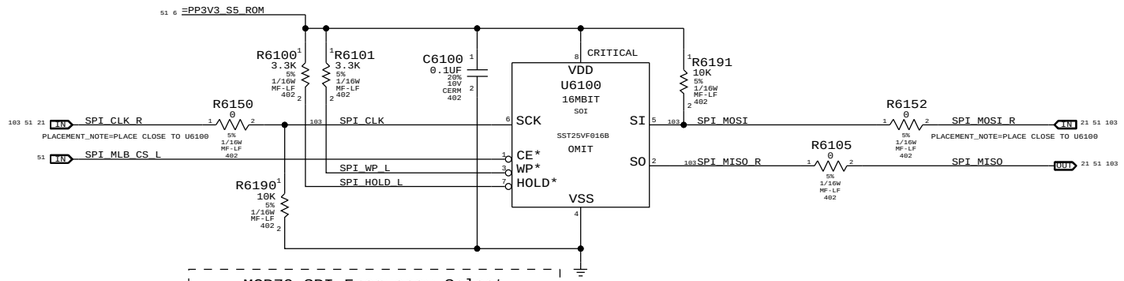
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 60 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues ‘READ’ (0x03) commands not ‘READ_FAST’ (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 61 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO CODEC
APPLE P/N 353S2592

=PP1V5_S0_AUD_DIG

C6203 4.7UF 20% 4V X5R 402
C6258 0.47UF 10% 10V X5R 402

C6260 10UF 20% 16V POLY-TANT CASE-B2-SM

C6204 10UF 20% 6.3V X5R 603
C6205 10UF 20% 6.3V X5R 603

C6259 1UF 10% 10V X5R 402-1
C6264 0.47UF 10% 10V X5R 402
C6265 0.47UF 10% 10V X5R 402
C6261 0.47UF 10% 10V X5R 402
C6262 10UF 20% 16V POLY-TANT CASE-B2-SM
C6213 CRITICAL 10UF 20% 6.3V X5R 603

=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG VOLTAGE=4.5V MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM
GND_AUDIO_HP_AMP_L
GND_AUDIO_CODEC

GND_AUDIO_HP_AMP_L
PP4V5_AUDIO_ANALOG
R6255 2.67K 1% 1/16W MF-LF 402

VBIAS_DAC
CS4206_FP
CS4206_FN

K22 = NC
K23 LOW = S/PDIF IN, HIGH = DP SPDIF

AUD_MUX_CNTRL
AUD_GPIO_1
AUD_GPIO_2
AUD_GPIO_3
AUD_SENSE_A

CS4206_FLYP
CS4206_FLYC
C6206 2.2UF 20% 6.3V CERM 402-LF
C6208 2.2UF 20% 6.3V CERM 402-LF
CS4206_FLYN

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
AUD_SPDIF_IN_CODEC
AUD_SPDIF_OUT

R6254 22 5% 1/10W MF-LF 402
AUD_SDI_R
R6257 22 5% 1/10W MF-LF 402
AUD_SPDIF_CHIP

R6295 100K 1% 1/16W MF-LF 402
NOSTUFF R6263 0 5% 1/16W MF-LF 402

DGND_THRM_PAD_AGND

CRITICAL C6211 1UF 10% 20V TANT CASE-P3-HF
CRITICAL C6263 10UF 20% 16V POLY-TANT CASE-B2-SM

NOSTUFF R6267 100K 5% 1/10W MF-LF 402

GND_AUDIO_CODEC
XW6201 SM
GND_AUDIO_HP_AMP_L

MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

BETTER
R6299 100K 5% 1/16W MF-LF 402
AUD_GPIO_1
EDUCATION
R6298 10K 5% 1/16W MF-LF 402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

U6201 CS4206ACNZC QFN

9	VD			
24	VA_REF			
46	VA_HP			
25	VA			
29	VBIAS_DAC			
44	VHP_FILT+	CRITICAL	HPOUT_L	38
41	VHP_FILT-		HPOUT_R	40
			HPREF	39
2	GPIO0/DMIC_SDA1		LINEOUT_L1+	35
12	GPIO1/DMIC_SDA2		LINEOUT_L1-	34
14	GPIO2/SPDIF_OUT2		LINEOUT_R1+	36
15	GPIO3		LINEOUT_R1-	37
13	SENSE_A		LINEOUT_L2+	31
			LINEOUT_L2-	30
			LINEOUT_R2+	32
			LINEOUT_R2-	33
45	FLYP		MICBIAS	16
43	FLYC		VCOM	28
42	FLYN			
3	VL_HD			
1	VL_IF			
6	BITCLK		LINEIN_L+	21
			LINEIN_C-	22
			LINEIN_R+	23
10	SYNC			
8	SDI		MICIN_L+	18
5	SDO		MICIN_L-	17
11	RESET*		MICIN_R+	19
			MICIN_R-	20
47	SPDIF_IN			
48	SPDIF_OUT			
			VREF+_ADC	27
			DMIC_SCL	4
7	DGND			
49	THRM_PAD			
26	AGND			

MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

AUD_HP_PORT_L
AUD_HP_PORT_R
AUD_HP_PORT_REF
AUD_LO1_P_L
TP_AUD_LO1_N_L NC
AUD_LO1_P_R
TP_AUD_LO1_N_R NC
AUD_LO2_P_L
TP_AUD_LO2_N_L NC
AUD_LO2_P_R
TP_AUD_LO2_N_R NC
AUD_CODEC_MICBIAS
CS4206_VCOM
AUD_LI_P_L
MAKE_BASE=TRUE AUD_LI_COM
AUD_LI_P_R
AUD_LI_N_L
AUD_LI_N_R
AUD_MIC_INP_L
AUD_MIC_INN_L
AUD_MIC_INP_R
AUD_MIC_INN_R
CS4206_VREF_ADC NC
TP_AUD_DMIC_CLK NC

HP OUT ZOBEL NETWORK

MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
AUD_HP_PORT_L
AUD_HP_PORT_R
C6298 0.1UF 10% 16V X7R-CERM 402
C6297 0.1UF 10% 16V X7R-CERM 402
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
AUD_Z_R NC
AUD_Z_L NC
R6296 39 5% 1/10W MF-LF 402
R6297 39 5% 1/10W MF-LF 402
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
GND_AUDIO_HP_AMP_L

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

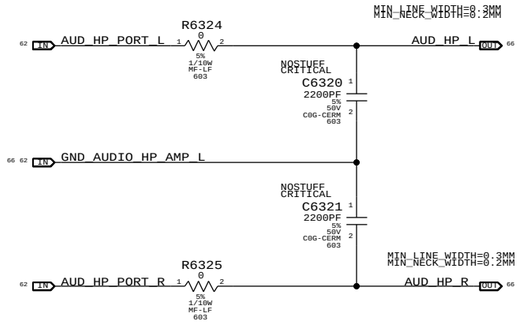
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=5V
L6201 FERR-220-OHM 0402
=PP5V_S0_AUDIO
R6201 2.21K 1% 1/10W MF-LF 402
=PP3V3_S0_AUDIO

VR6201 TPS71745 SON CRITICAL
IN 4V5_REG_IN
EN 4V5_REG_EN
NR/FB 4V5_NR
GND
NC
OUT

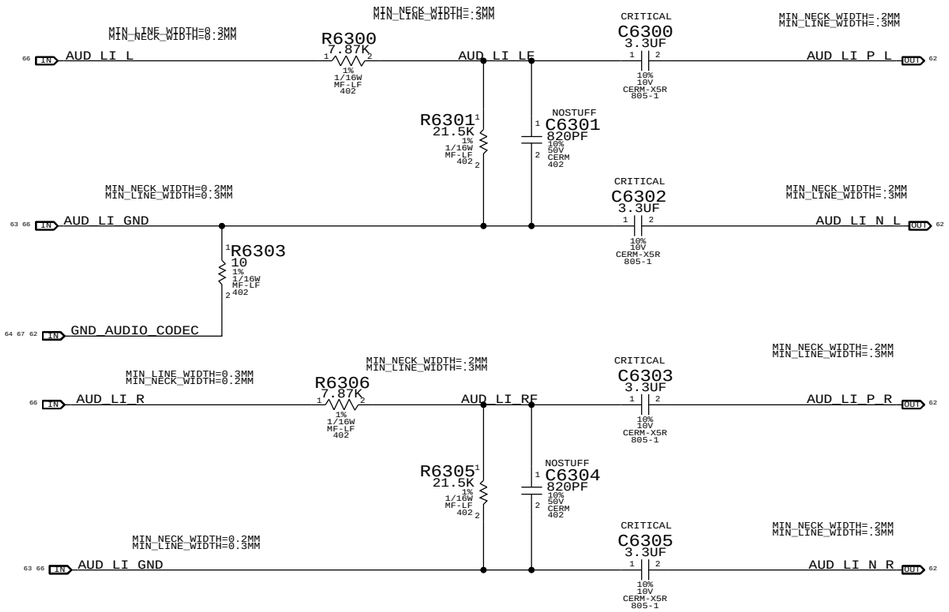
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V
PP4V5_AUDIO_ANALOG

C6201 1UF 10% 10V X5R 402-1
C6202 1UF 10% 10V X5R 402-1
C6266 0.1UF 10% 16V X7R-CERM 402
C6207 1UF 10% 10V X5R 402-1
GND_AUDIO_CODEC

1ST ORDER DAC FILTER PLACEHOLDER



CODEC_Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=SKIPAUDIO SYNC_DATE=04/20/2009

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-7863
SIZE D
REVISION A.0.0
BRANCH
PAGE 63 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

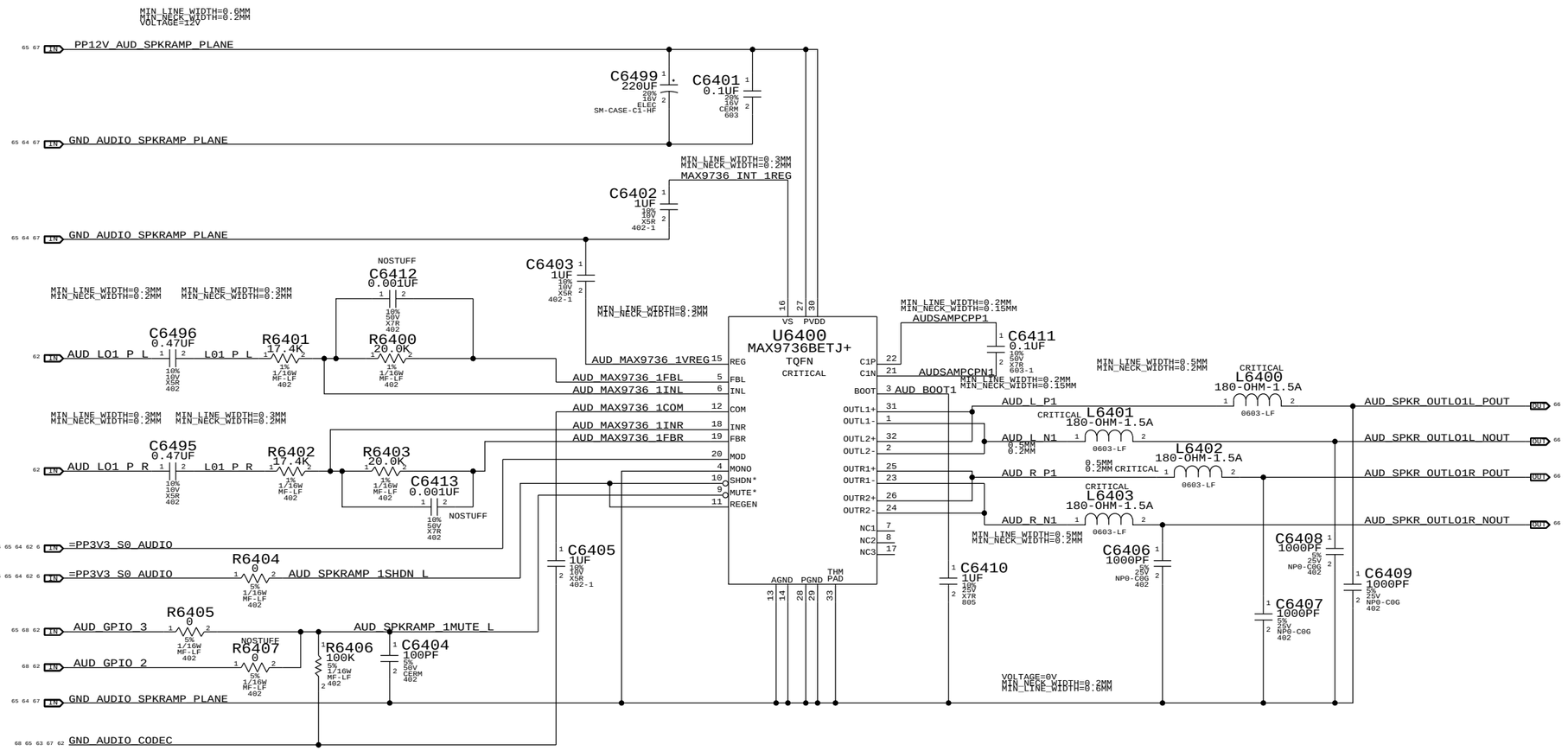
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



SYNC_MASTER=SKIPAUDIO SYNC_DATE=04/20/2009

PAGE TITLE: AUDIO: Tweeter Amp 1

Apple Inc.

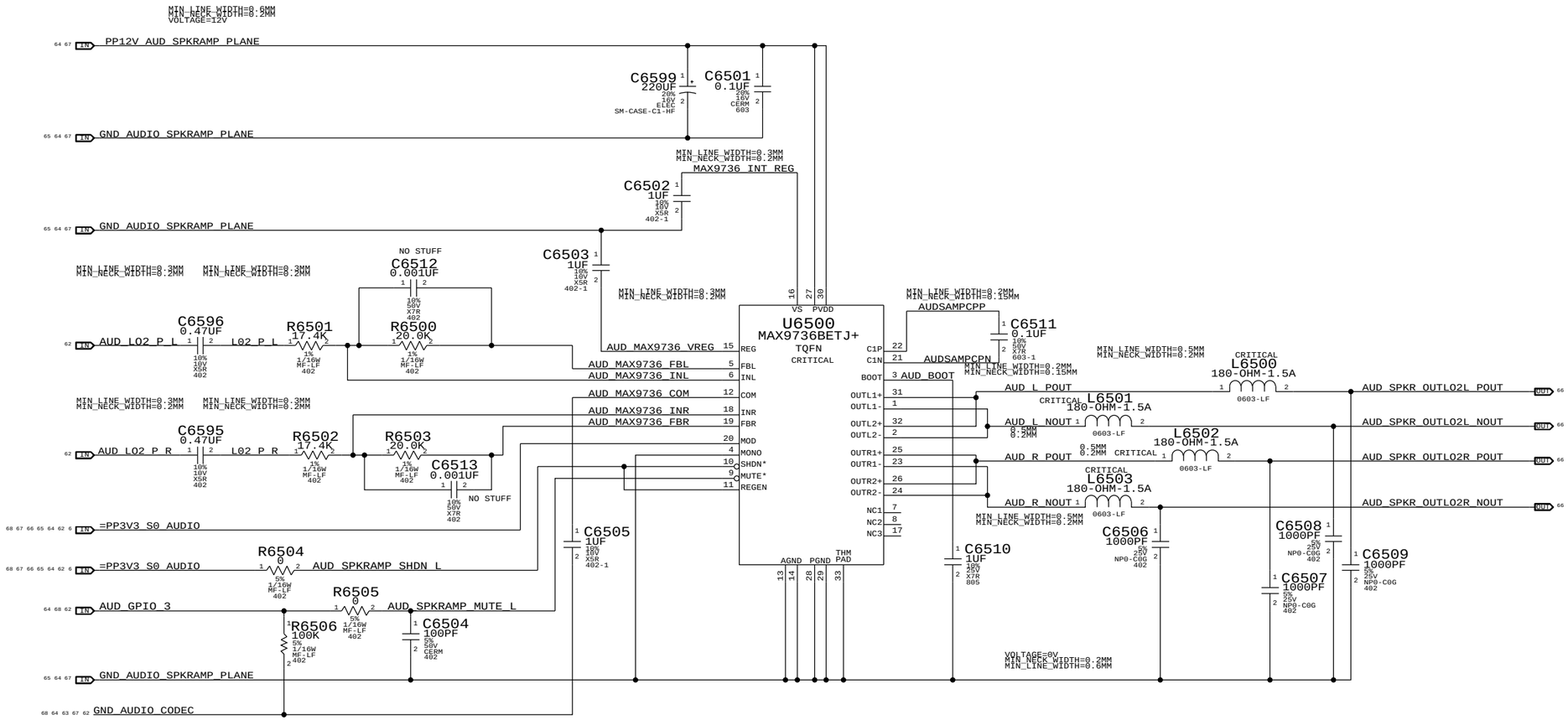
DRAWING NUMBER: 051-7863
SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 64 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



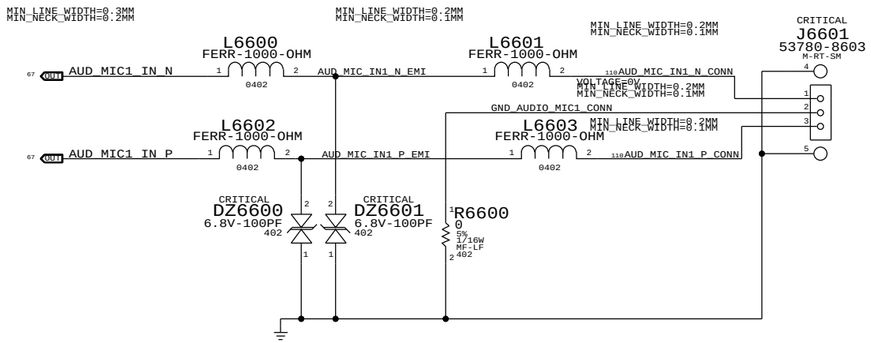
SYNC_MASTER=SKIPAUDIO SYNC_DATE=04/20/2009

PAGE TITLE
AUDIO: Woofer Amp

Apple Inc.

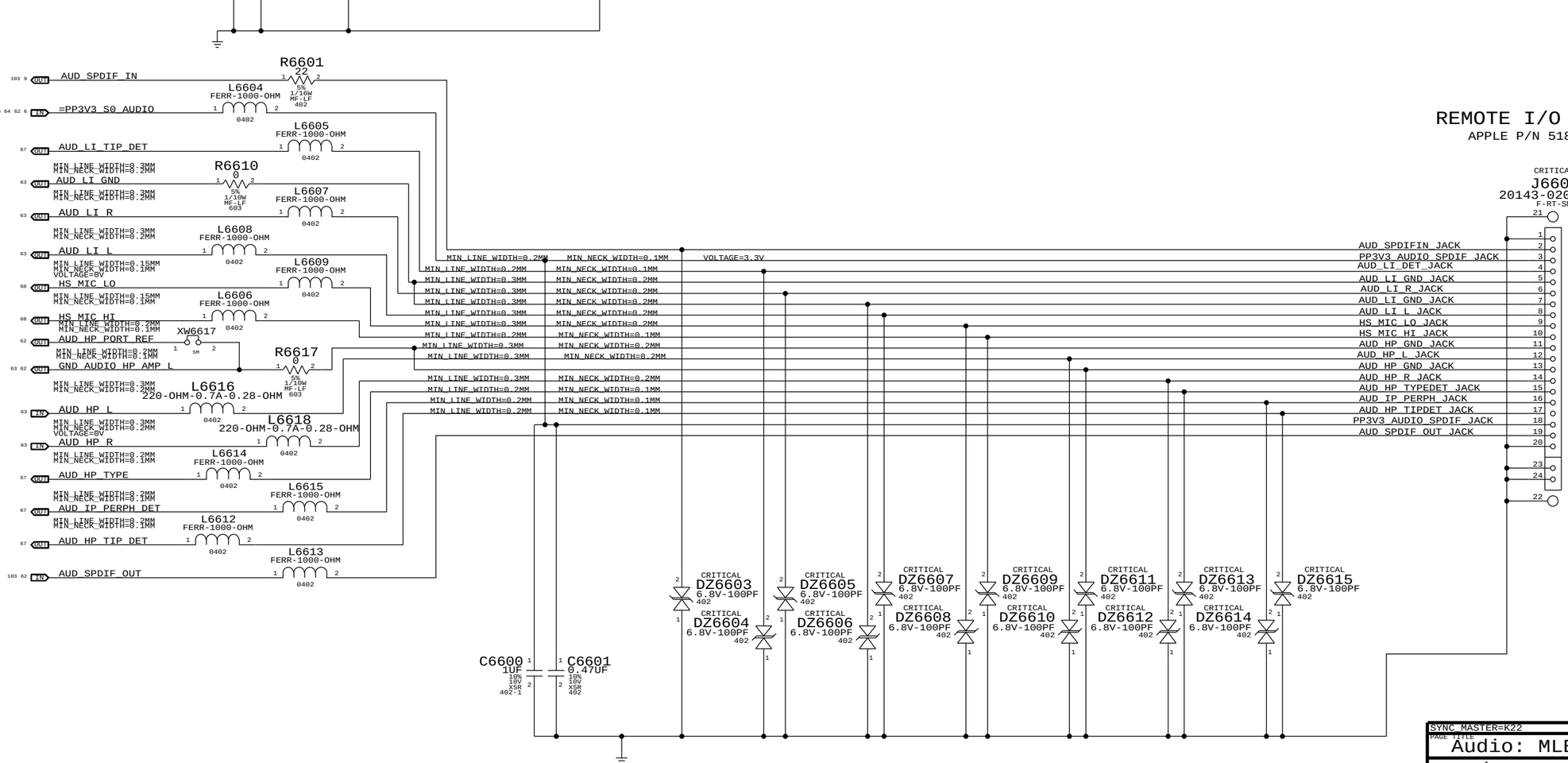
DRAWING NUMBER 051-7863
SIZE D
REVISION A.0.0
BRANCH
PAGE 65 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

INTERNAL MIC CON
APPLE P/N 518S0677



SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

REMOTE I/O CONNECTOR
APPLE P/N 518S0723



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

Audio: MLB to I/O Conn.

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

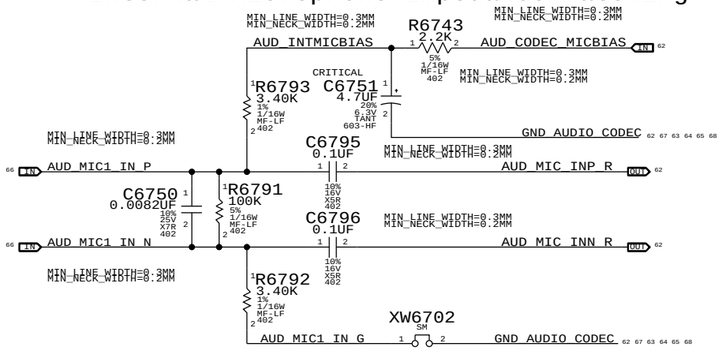
REVISION A.0.0

BRANCH

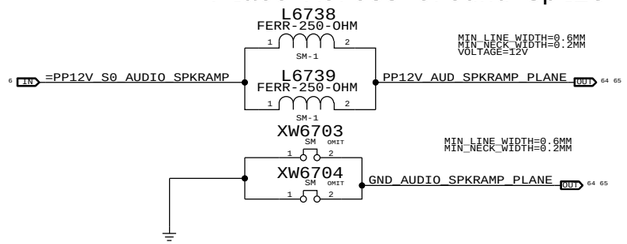
PAGE 66 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

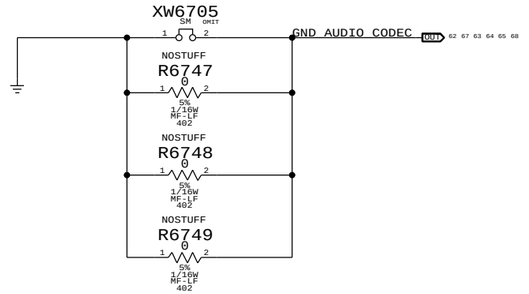
Internal Microphone Impedance Matching



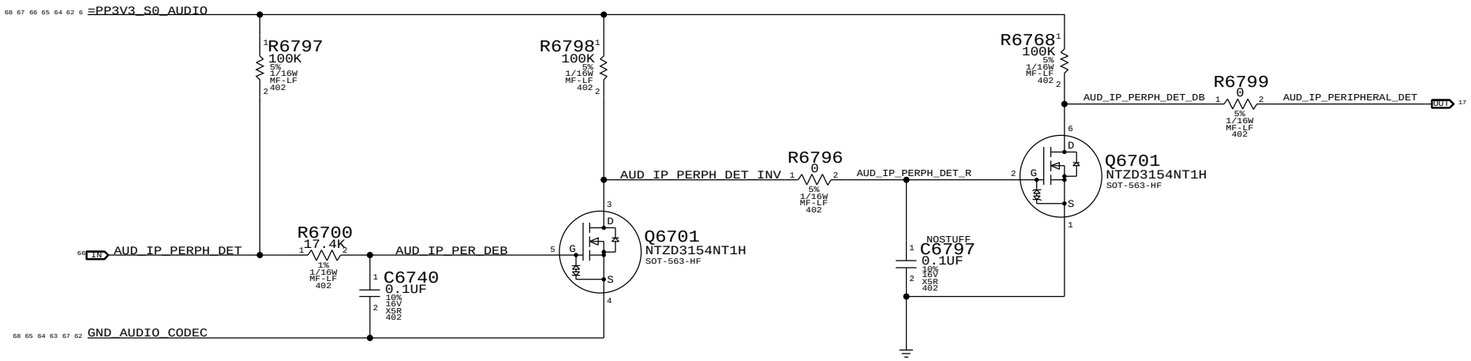
Place Across Ground Split



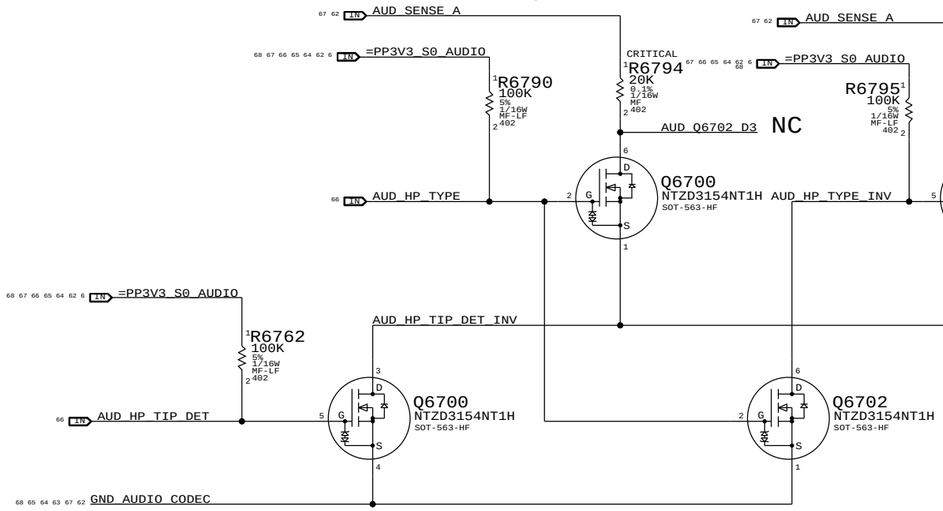
Audio Ground Returns



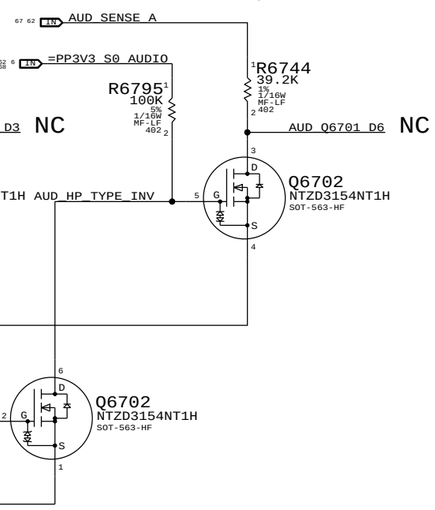
IPHS HS Detect Debounce CKT



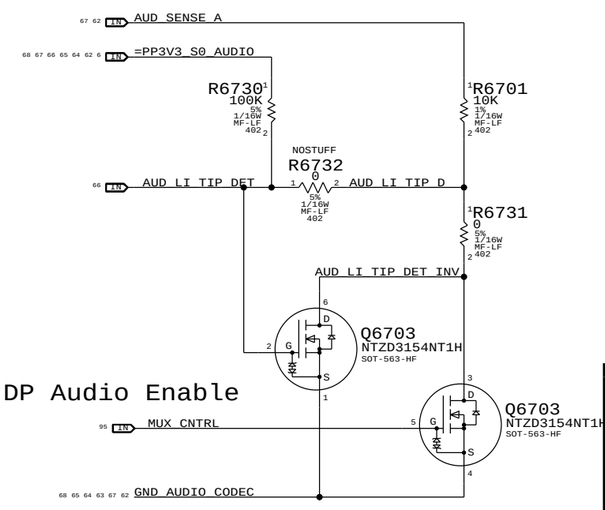
Digital Out



Headphone Out



LI Insert Detect



DP Audio Enable

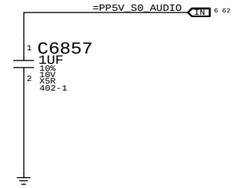
SYNC_MASTER=SKIPAUDIO SYNC_DATE=04/20/2009

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

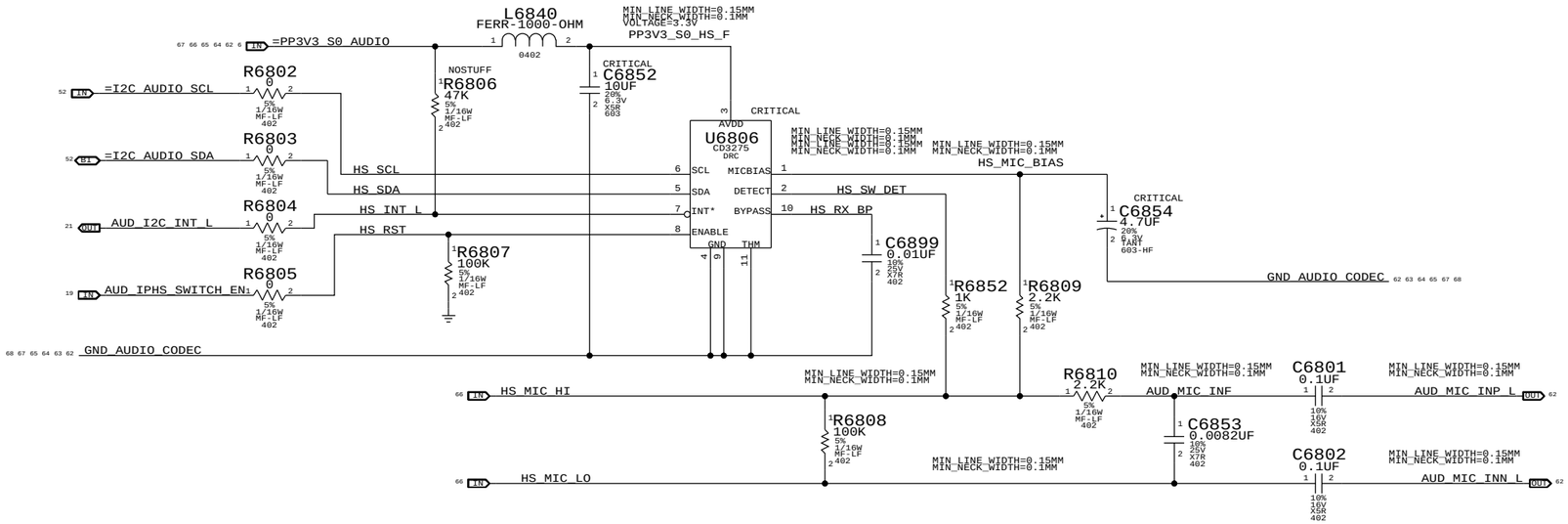
DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 67 OF 110
SHEET

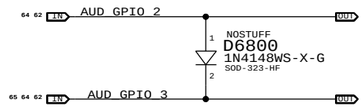
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5



MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256





FLP = 8.82 KHZ
FHP = 80 HZ

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

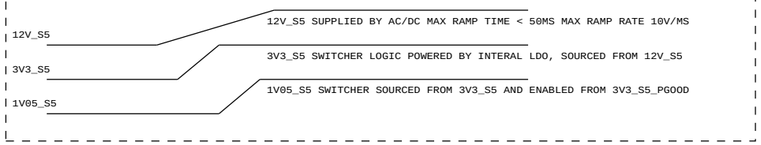
REVISION: A.0.0

BRANCH:

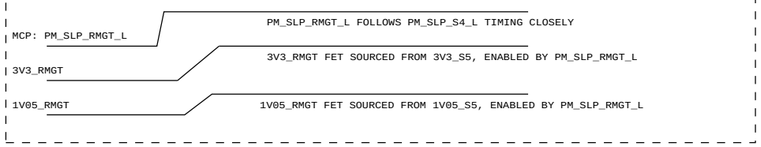
PAGE: 68 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

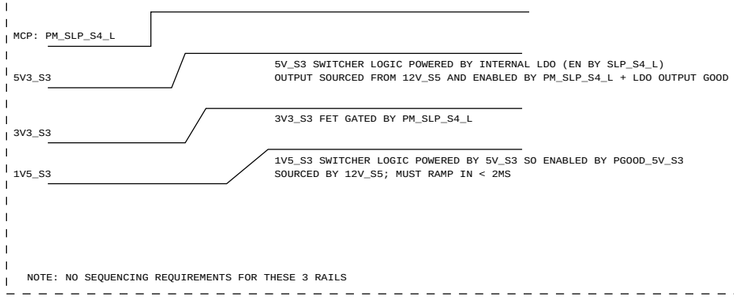
S5 POWER RAIL SEQUENCING



RMGT POWER RAIL SEQUENCING

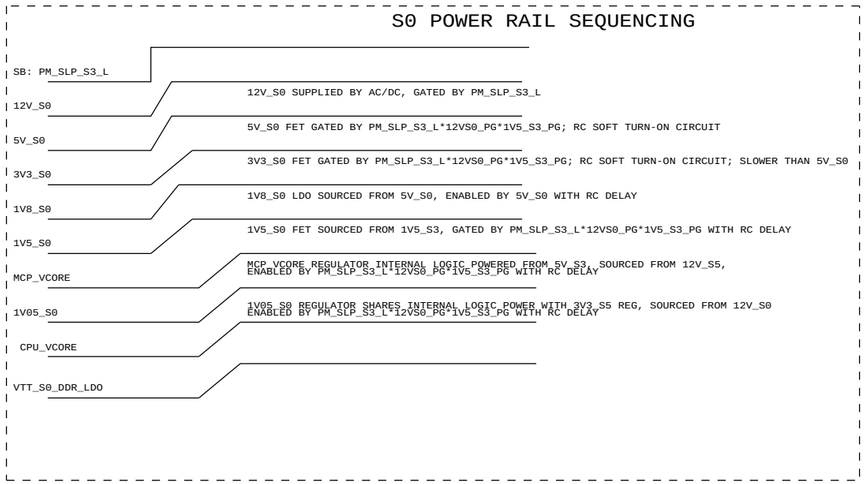


S3 POWER RAIL SEQUENCING

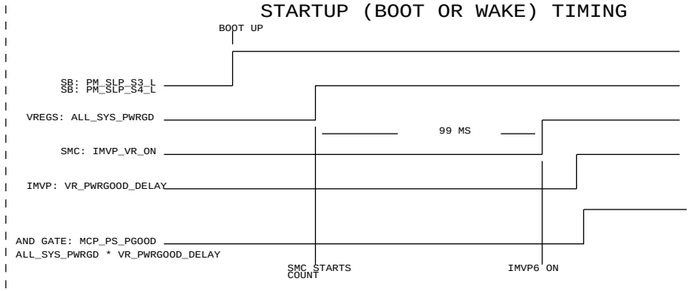


NOTE: NO SEQUENCING REQUIREMENTS FOR THESE 3 RAILS

S0 POWER RAIL SEQUENCING

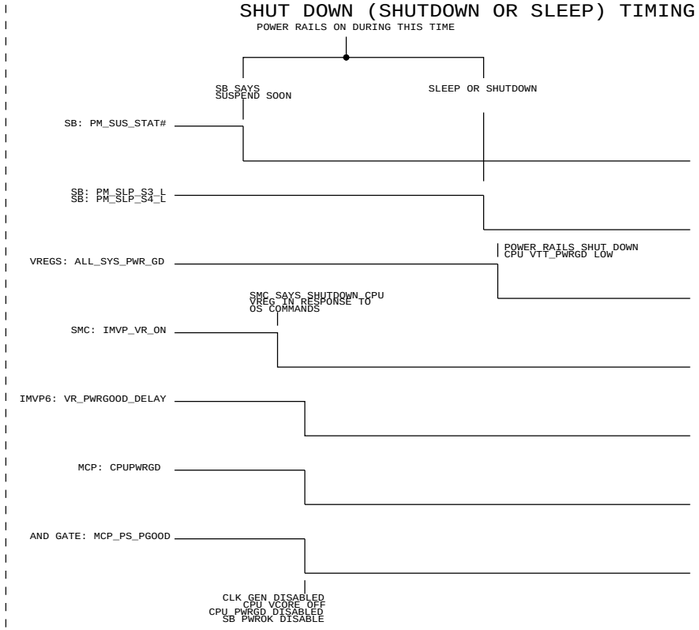


STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

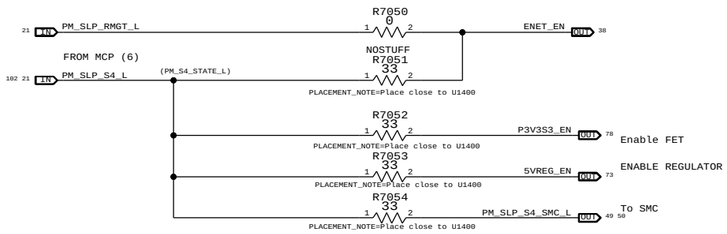
PAGE TITLE
POWER SEQUENCING BLOCK DIAGRAM

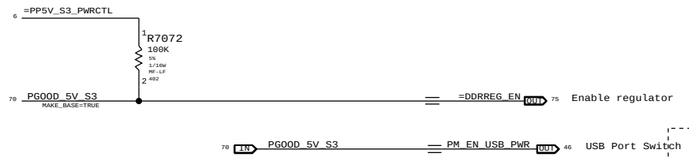
Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 69 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

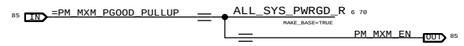
Power Control Signals
3.3V,5V S3 enable

State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

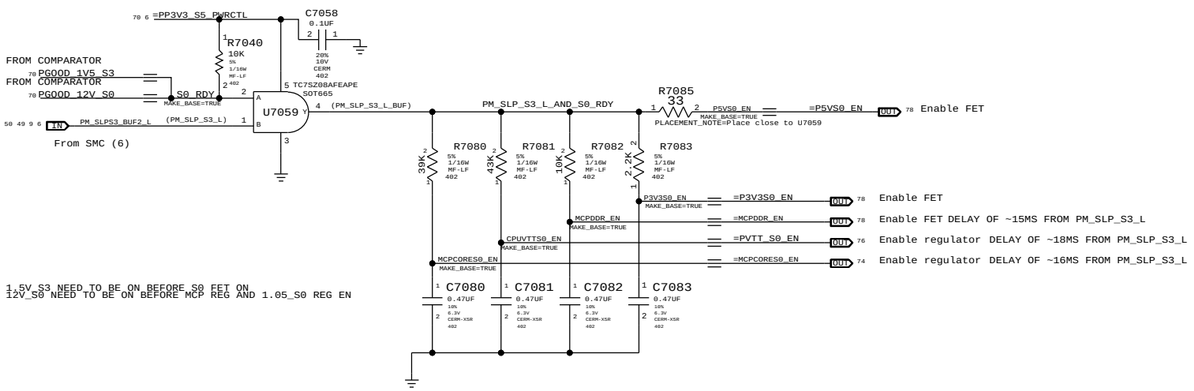


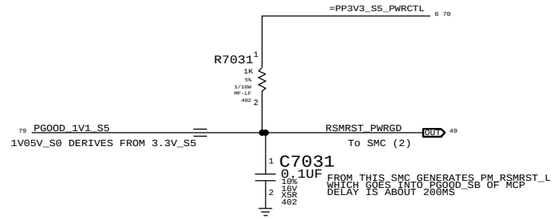


MXM POWER SEQUENCE



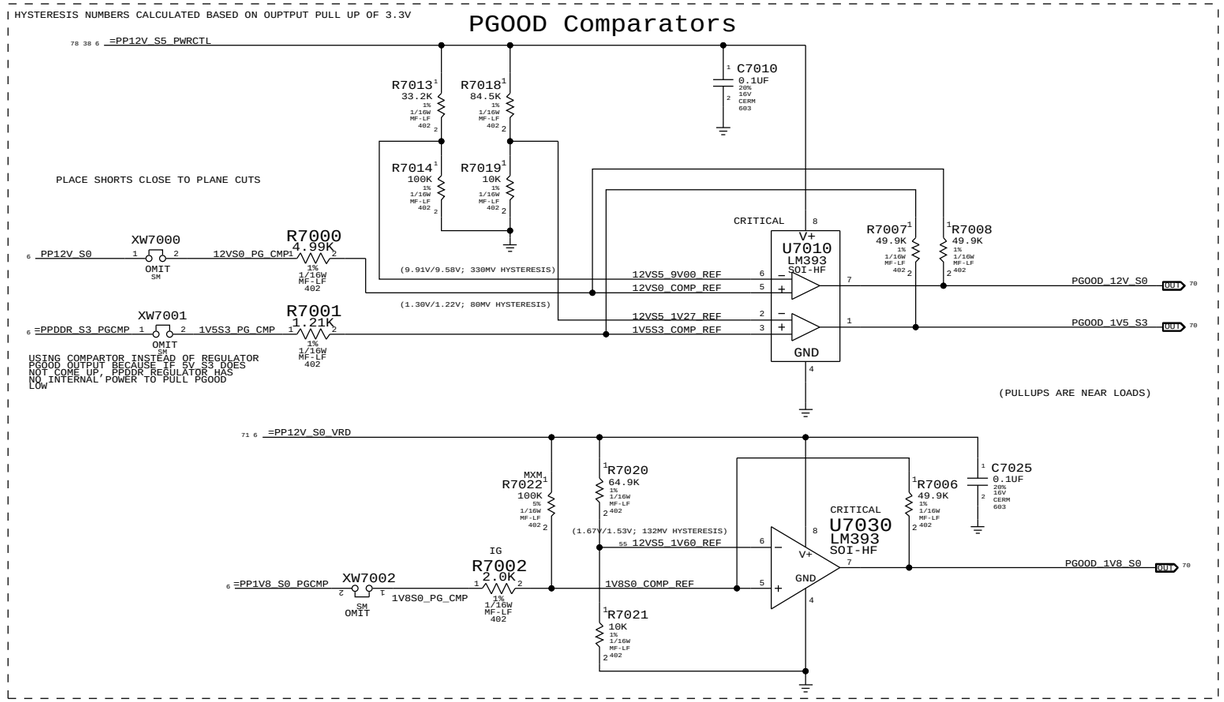
MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD



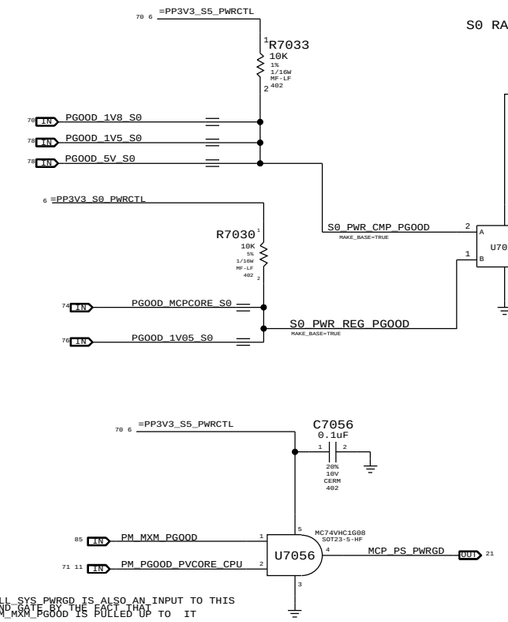


PGOOD Comparators

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V



S0 RAILS PGOOD



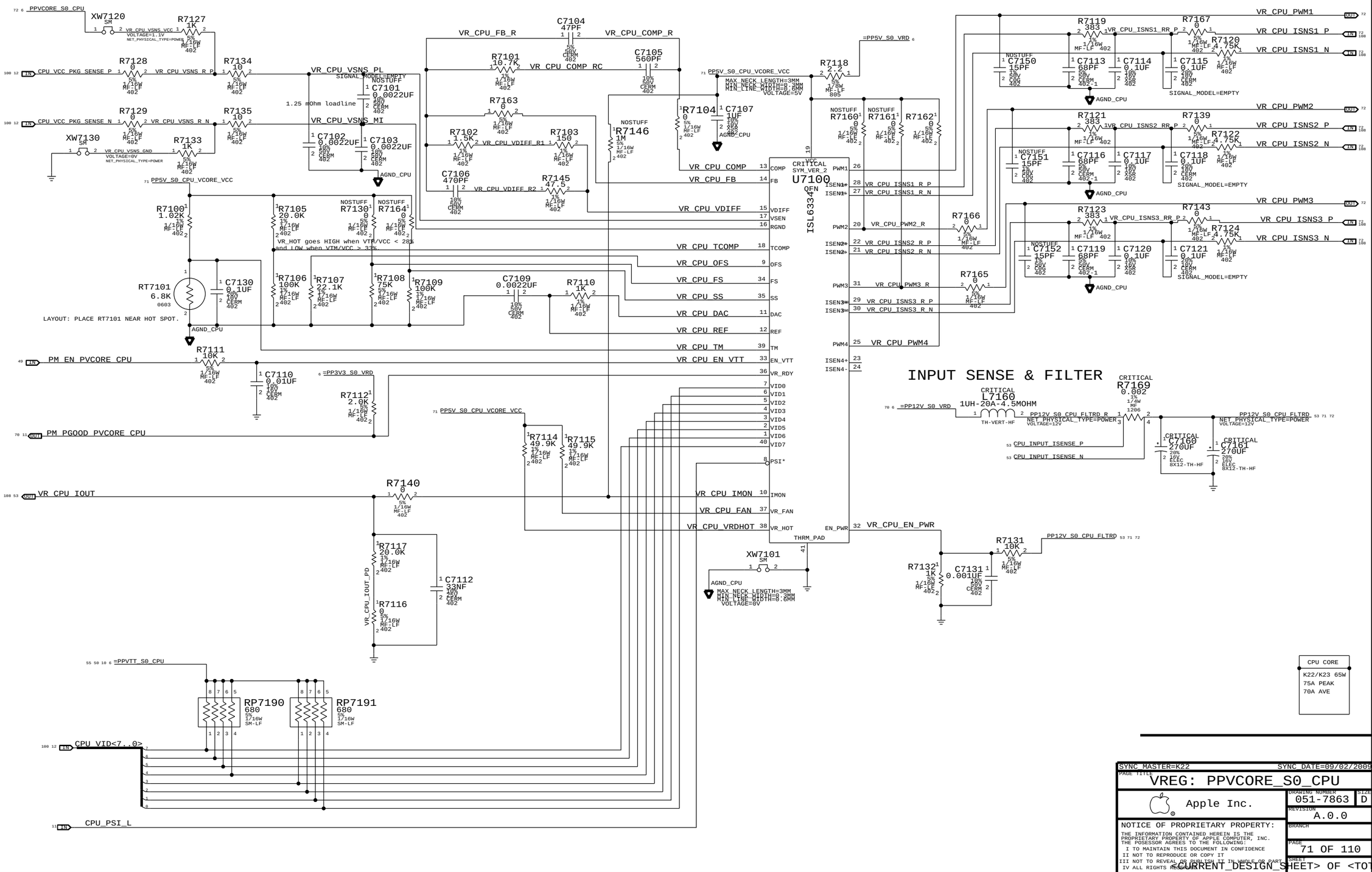
	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

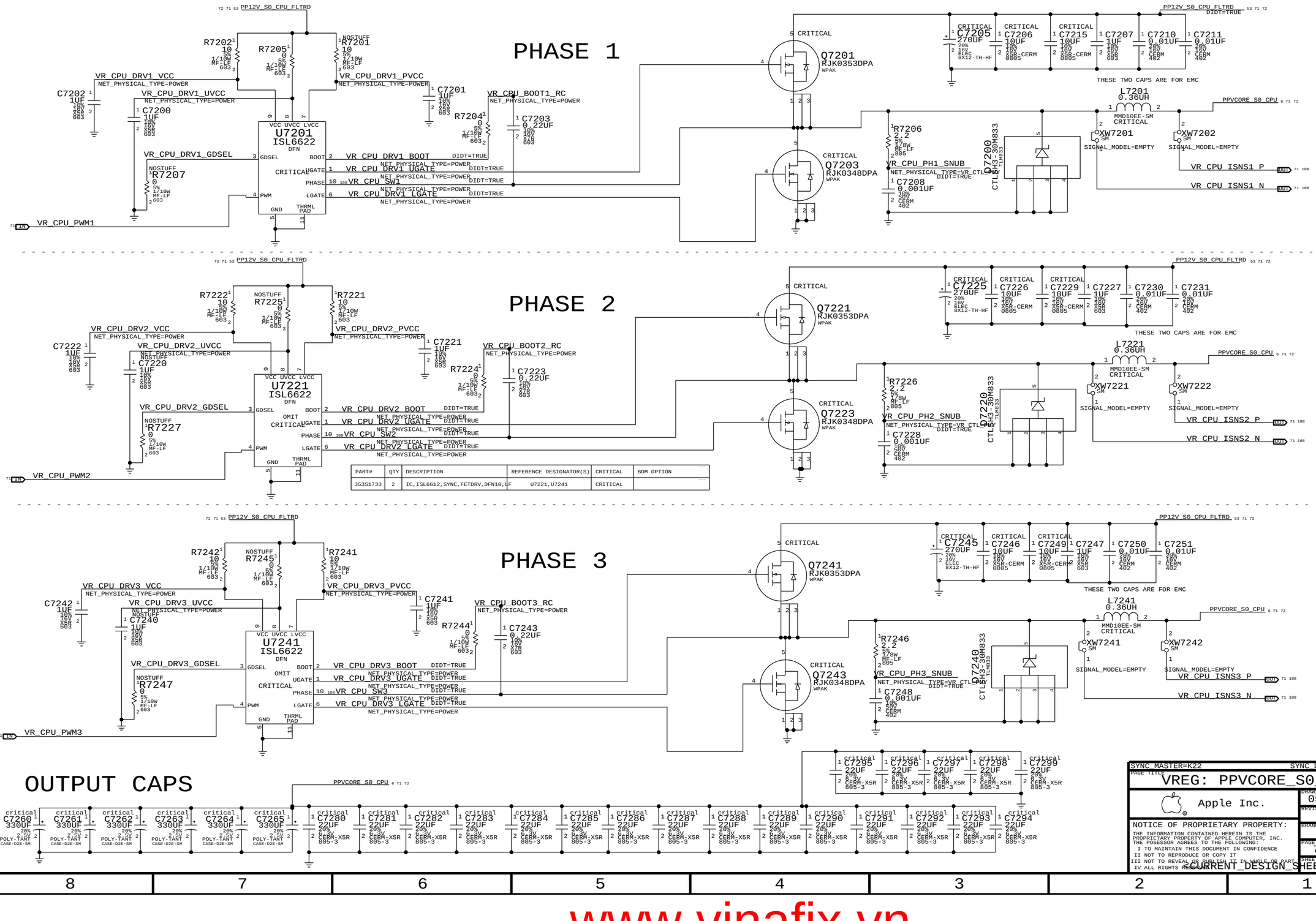
SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
PGOOD and Power Sequencing

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 70 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1733	2	IC,ISL6612,SYNC,FETDRV,DFN10,UF	U7221,U7241	CRITICAL	

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: VREG: PPVCORE_S0_CPU

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

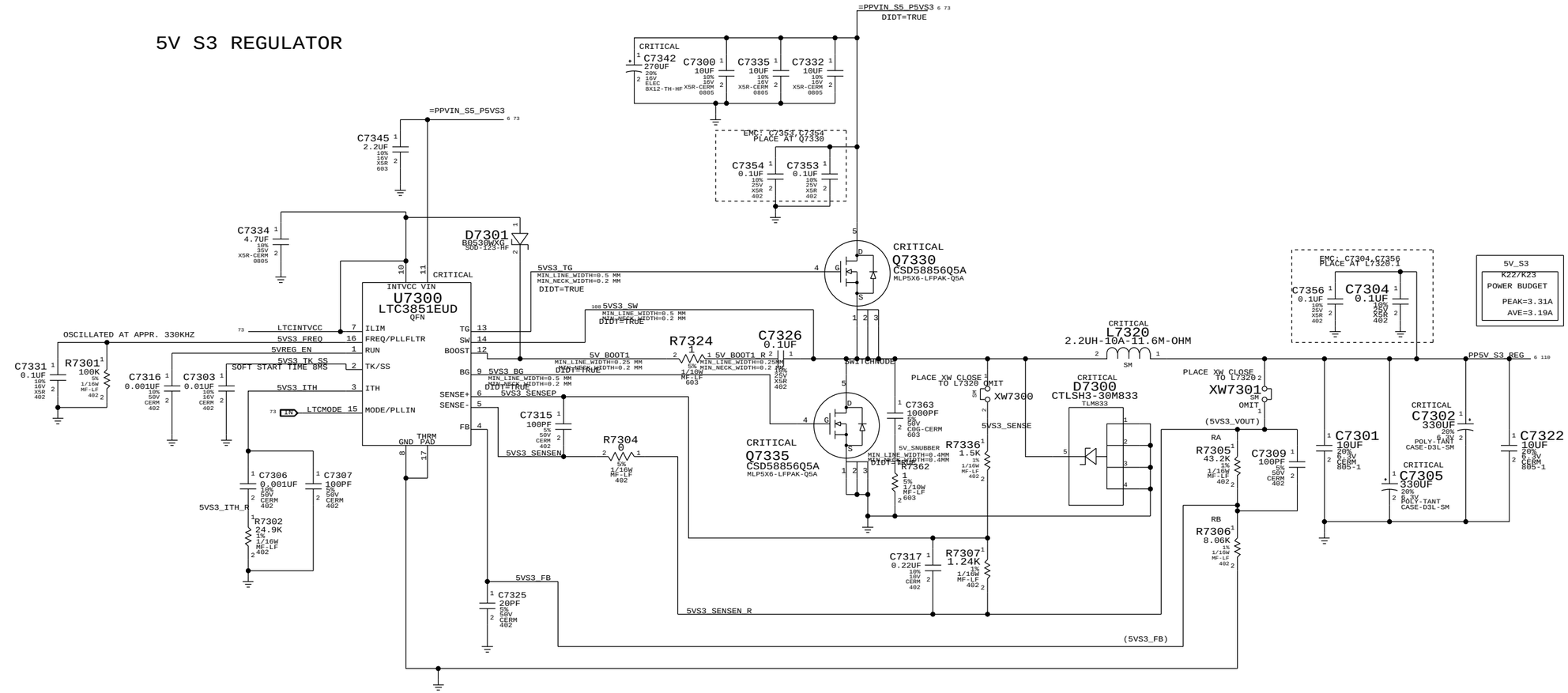
REVISION A.0.0

BRANCH

PAGE 72 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

5V S3 REGULATOR



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: 5V_S3 REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

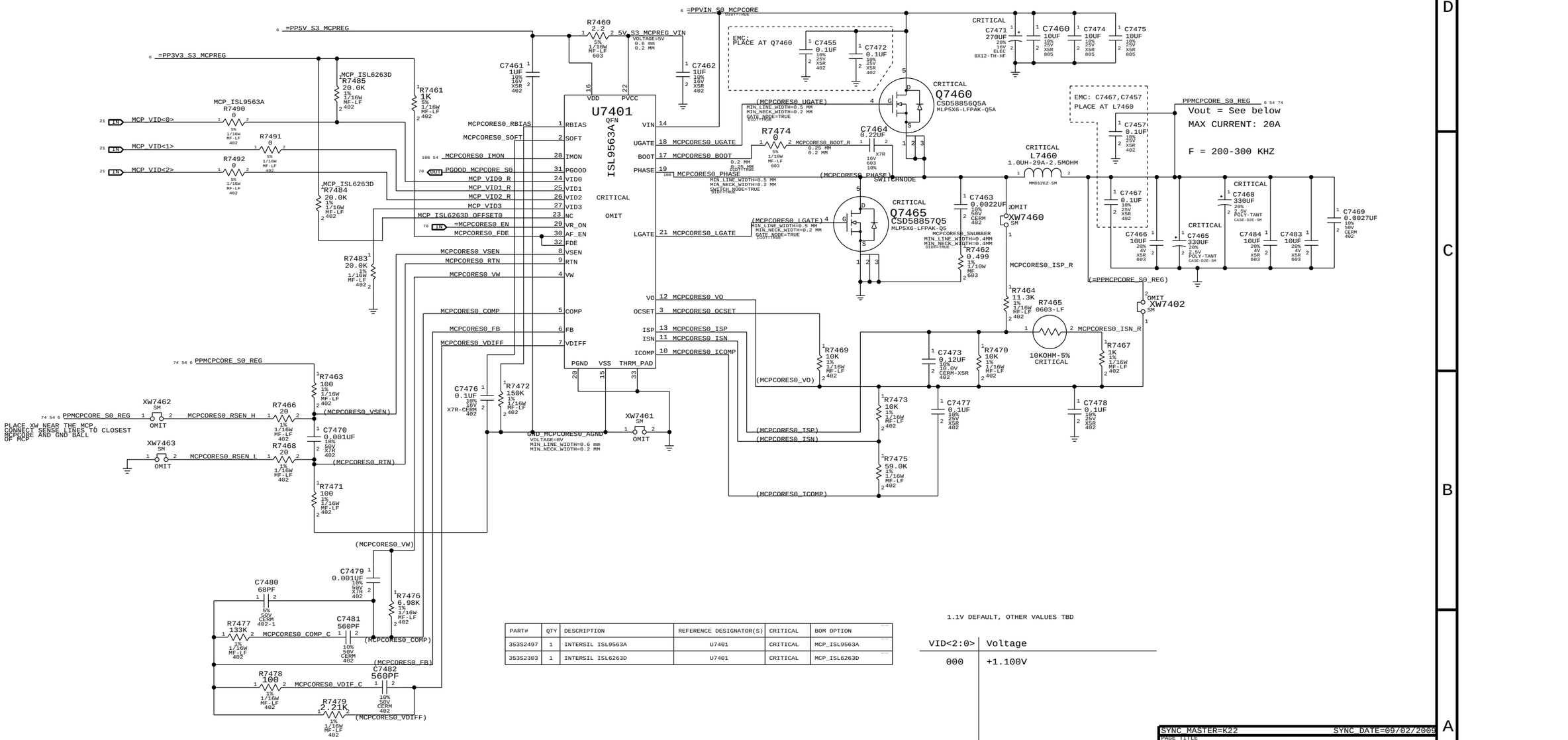
REVISION: A.0.0

BRANCH:

PAGE: 73 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP CORE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
353S2303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

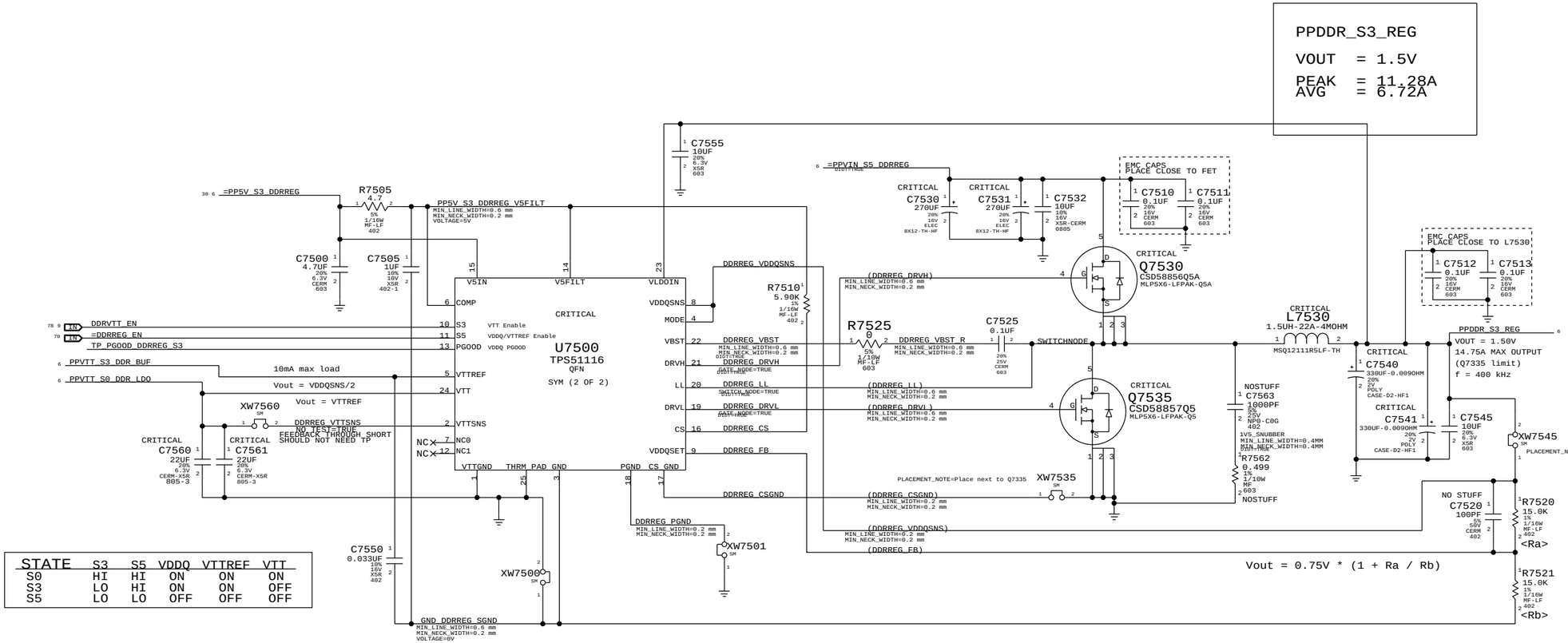
BRANCH:

PAGE: 74 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11.28A
AVG = 6.72A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

SYNC MASTER=K22 SYNC DATE=09/02/2009

PAGE TITLE: 1.5V DDR SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 75 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FSB VTT AND 3.3V S5 RAILS

INPUT POWER OF 12V_S0

INPUT POWER OF 12V_S5

Vout = 1.212V for Wolfdale
6.7A MAX OUTPUT
(R7614 LIMIT)
f = 200 kHz

Vout = 0.7V * (1 + Ra / Rb)

EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT. SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (PPVTT_S0) CONTROLLED SEPARATELY

SELECTS SWITCHING FREQUENCY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1078	1	IND,PWR,1.5UH,20%,9A,12mOHM	L7610	CRITICAL	

VTT_FSB_S0
K22/K23
POWER BUDGET
PEAK=5.28A
AVE=2.88A

SEL A3V3 S5
K22/K23
POWER BUDGET
PEAK=0.69A
AVE=0.46A

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: FSB VTT/3.3V S5 SUPPLIES

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 76 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

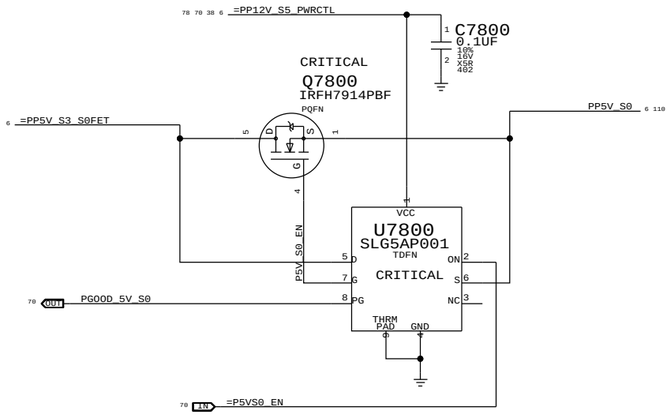
BRANCH

PAGE 77 OF 110

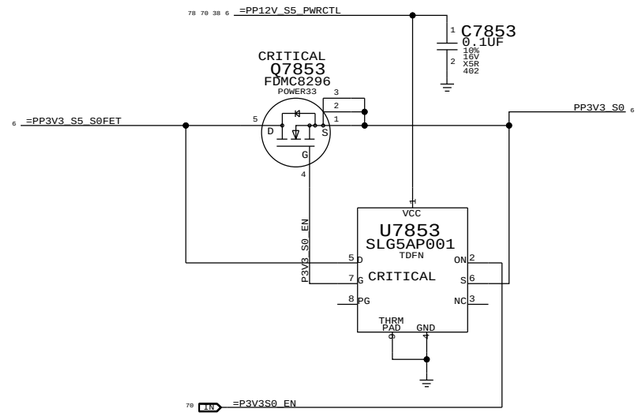
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

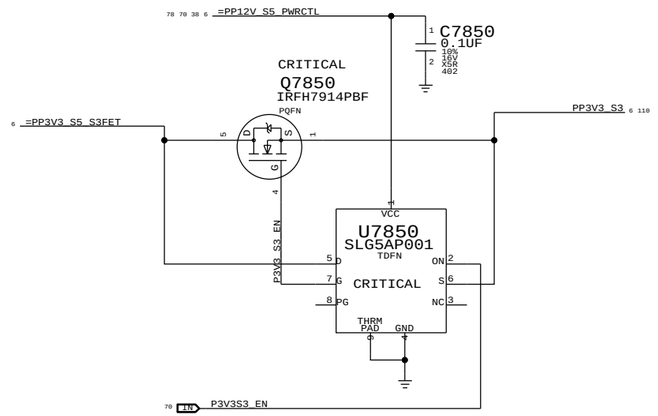
5V S0 FET



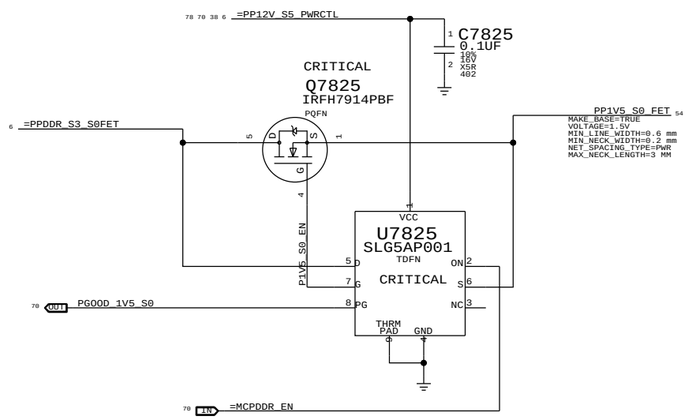
3.3V S0 FET



3.3V S3 FET

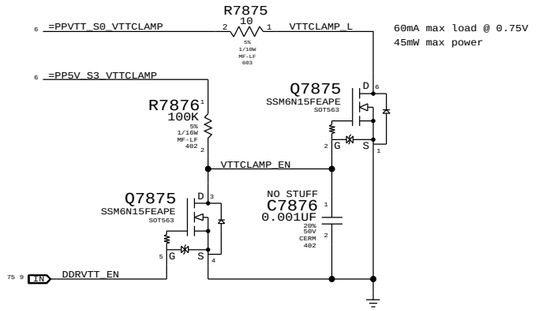


1.5V S0 FET



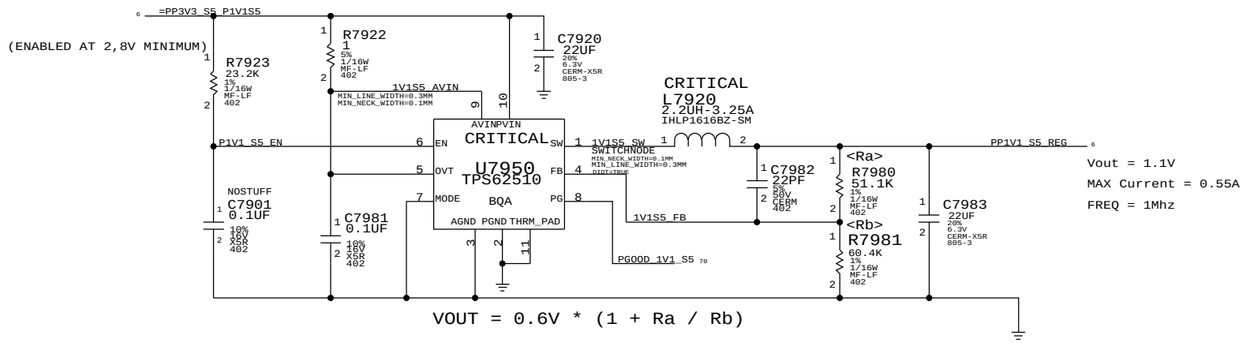
MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC_MASTER=K22	SYNC_DATE=09/02/2009
PAGE TITLE	S3 & S0 FETs
Apple Inc.	DRAWING NUMBER 051-7863 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 78 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP 1.1V_S5 AUXC SUPPLY



SYNC MASTER=K22	SYNC DATE=09/02/2009
PAGE TITLE: 1V1 S5 POWER SUPPLY	
Apple Inc.	DRAWING NUMBER: 051-7863 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 79 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 80 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 81 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 82 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 83 OF 110

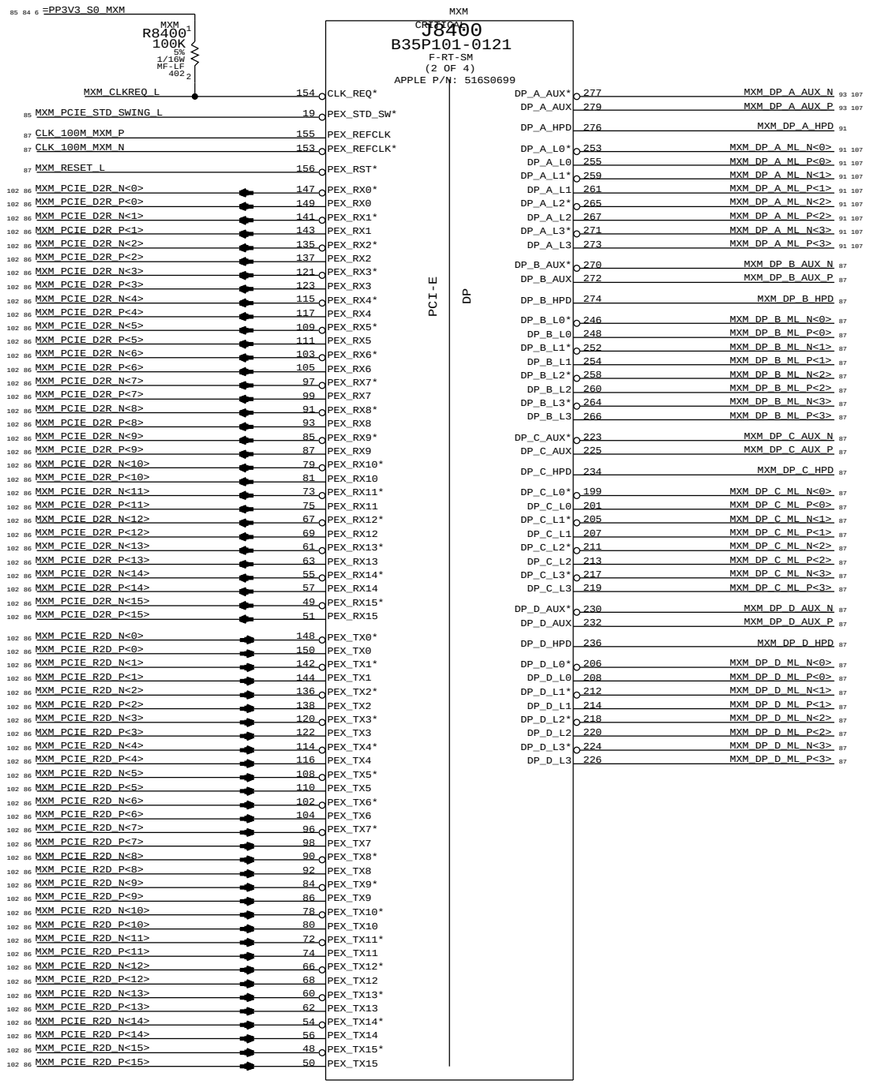
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 84 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

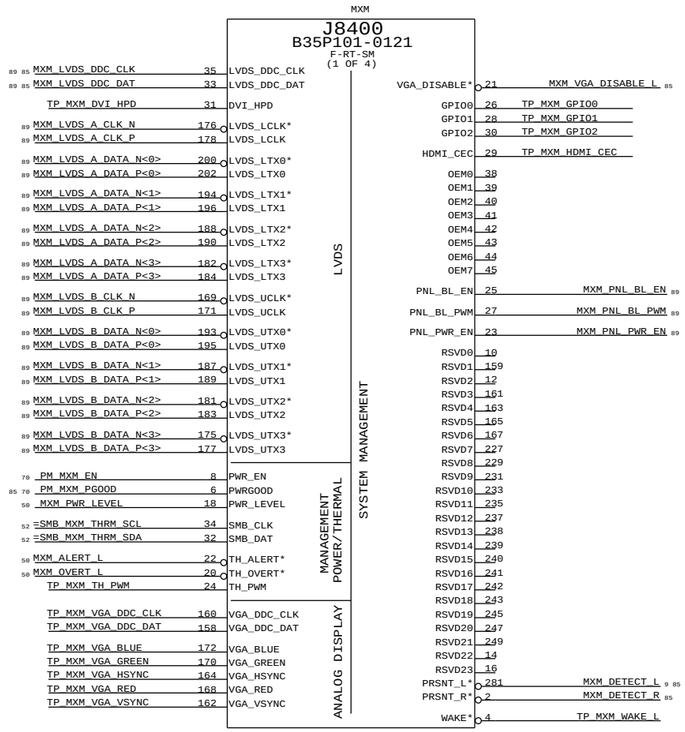
Page Notes

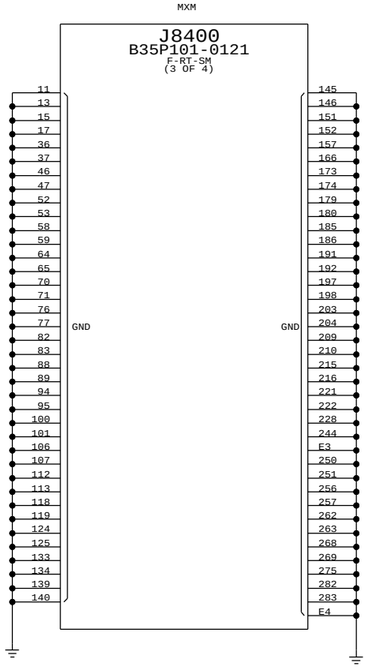
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =SMB_MXM_THRM_CLK
- =PM_MXM_PGOOD_PULLUP

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR





FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

FLOAT = LOW SWING
GND = HIGH SWING

R8510 0 MF-LF 5% 1/16W 402 NOSTUFF
MXM_VGA_DISABLE_L

R8504 0 MF-LF 5% 1/16W 402 MXM
MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM

R8500 100K MF-LF 5% 1/16W 402
MXM_DETECT_L
PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501 100K MF-LF 5% 1/16W 402
MXM_DETECT_R

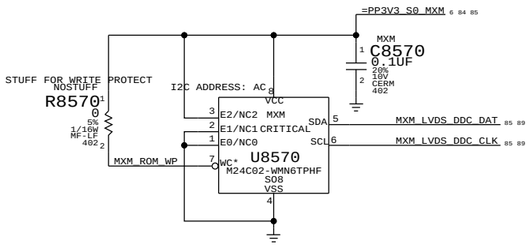
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503 10K MF-LF 5% 1/16W 402
PM_MXM_PGOOD

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MXM I/O

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 85 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MXM TX CAPS

102 9	IN	PEG_R2D_C_N<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT	84 102
102 9	IN	PEG_R2D_C_P<0>	MXM	C8601	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT	84 102
102 9	IN	PEG_R2D_C_P<1>	MXM	C8602	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT	84 102
102 9	IN	PEG_R2D_C_N<1>	MXM	C8603	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	OUT	84 102
102 9	IN	PEG_R2D_C_N<2>	MXM	C8604	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>	OUT	84 102
102 9	IN	PEG_R2D_C_P<2>	MXM	C8605	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>	OUT	84 102
102 9	IN	PEG_R2D_C_N<3>	MXM	C8606	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	OUT	84 102
102 9	IN	PEG_R2D_C_P<3>	MXM	C8607	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	OUT	84 102
102 9	IN	PEG_R2D_C_N<4>	MXM	C8608	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	OUT	84 102
102 9	IN	PEG_R2D_C_P<4>	MXM	C8609	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	OUT	84 102
102 9	IN	PEG_R2D_C_N<5>	MXM	C8610	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	OUT	84 102
102 9	IN	PEG_R2D_C_P<5>	MXM	C8611	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	OUT	84 102
102 9	IN	PEG_R2D_C_N<6>	MXM	C8612	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>	OUT	84 102
102 9	IN	PEG_R2D_C_P<6>	MXM	C8613	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>	OUT	84 102
102 9	IN	PEG_R2D_C_N<7>	MXM	C8614	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	OUT	84 102
102 9	IN	PEG_R2D_C_P<7>	MXM	C8615	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>	OUT	84 102
102 9	IN	PEG_R2D_C_N<8>	MXM	C8616	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>	OUT	84 102
102 9	IN	PEG_R2D_C_P<8>	MXM	C8617	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>	OUT	84 102
102 9	IN	PEG_R2D_C_N<9>	MXM	C8618	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>	OUT	84 102
102 9	IN	PEG_R2D_C_P<9>	MXM	C8619	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>	OUT	84 102
102 9	IN	PEG_R2D_C_N<10>	MXM	C8620	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>	OUT	84 102
102 9	IN	PEG_R2D_C_P<10>	MXM	C8621	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>	OUT	84 102
102 9	IN	PEG_R2D_C_P<11>	MXM	C8622	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>	OUT	84 102
102 9	IN	PEG_R2D_C_N<11>	MXM	C8623	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>	OUT	84 102
102 9	IN	PEG_R2D_C_N<12>	MXM	C8624	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>	OUT	84 102
102 9	IN	PEG_R2D_C_P<12>	MXM	C8625	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>	OUT	84 102
102 9	IN	PEG_R2D_C_N<13>	MXM	C8626	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>	OUT	84 102
102 9	IN	PEG_R2D_C_P<13>	MXM	C8627	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>	OUT	84 102
102 9	IN	PEG_R2D_C_N<14>	MXM	C8628	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>	OUT	84 102
102 9	IN	PEG_R2D_C_P<14>	MXM	C8629	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>	OUT	84 102
102 9	IN	PEG_R2D_C_N<15>	MXM	C8630	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>	OUT	84 102
102 9	IN	PEG_R2D_C_P<15>	MXM	C8631	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	OUT	84 102

MXM RX CAPS

102 84	IN	MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<0>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<2>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<3>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<3>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<4>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<11>	MXM	C8641	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<4>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<10>	MXM	C8642	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<5>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<10>	MXM	C8643	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<5>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<6>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<6>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<7>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<8>	MXM	C8647	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<7>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<8>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<9>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<9>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<5>	MXM	C8652	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<10>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<10>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<13>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<13>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT	9 102
102 84	IN	MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT	9 102

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 86 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP Connections

84 CLK_100M_MXM_P ── GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE) 9 102
84 CLK_100M_MXM_N ── GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE) 9 102
84 MXM_RESET_L ── PEG_RESET_L (MAKE_BASE=TRUE) 9

Unused LVDS Interfaces

18 LVDS_IG_A_CLK_P ── NC_LVDS_IG_A_CLK_P (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_CLK_N ── NC_LVDS_IG_A_CLK_N (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_P<0> ── NC_LVDS_IG_A_DATA_P<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_N<0> ── NC_LVDS_IG_A_DATA_N<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_P<1> ── NC_LVDS_IG_A_DATA_P<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_N<1> ── NC_LVDS_IG_A_DATA_N<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_P<2> ── NC_LVDS_IG_A_DATA_P<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_N<2> ── NC_LVDS_IG_A_DATA_N<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_P<3> ── NC_LVDS_IG_A_DATA_P<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_A_DATA_N<3> ── NC_LVDS_IG_A_DATA_N<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_CLK_P ── NC_LVDS_IG_B_CLK_P (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_CLK_N ── NC_LVDS_IG_B_CLK_N (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_P<0> ── NC_LVDS_IG_B_DATA_P<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_N<0> ── NC_LVDS_IG_B_DATA_N<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_P<1> ── NC_LVDS_IG_B_DATA_P<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_N<1> ── NC_LVDS_IG_B_DATA_N<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_P<2> ── NC_LVDS_IG_B_DATA_P<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_N<2> ── NC_LVDS_IG_B_DATA_N<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_P<3> ── NC_LVDS_IG_B_DATA_P<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_B_DATA_N<3> ── NC_LVDS_IG_B_DATA_N<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_DDC_CLK ── NC_LVDS_IG_DDC_CLK (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_DDC_DATA ── NC_LVDS_IG_DDC_DATA (MAKE_BASE=TRUE NO_TEST=TRUE)

Unused MXM Interfaces

85 MXM_LVDS_A_CLK_N ── NC_MXM_LVDS_A_CLK_N (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_CLK_P ── NC_MXM_LVDS_A_CLK_P (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_N<0> ── NC_MXM_LVDS_A_DATA_N<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_P<0> ── NC_MXM_LVDS_A_DATA_P<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_N<1> ── NC_MXM_LVDS_A_DATA_N<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_P<1> ── NC_MXM_LVDS_A_DATA_P<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_N<2> ── NC_MXM_LVDS_A_DATA_N<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_P<2> ── NC_MXM_LVDS_A_DATA_P<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_N<3> ── NC_MXM_LVDS_A_DATA_N<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_A_DATA_P<3> ── NC_MXM_LVDS_A_DATA_P<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_CLK_N ── NC_MXM_LVDS_B_CLK_N (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_CLK_P ── NC_MXM_LVDS_B_CLK_P (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_N<0> ── NC_MXM_LVDS_B_DATA_N<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_P<0> ── NC_MXM_LVDS_B_DATA_P<0> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_N<1> ── NC_MXM_LVDS_B_DATA_N<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_P<1> ── NC_MXM_LVDS_B_DATA_P<1> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_N<2> ── NC_MXM_LVDS_B_DATA_N<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_P<2> ── NC_MXM_LVDS_B_DATA_P<2> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_N<3> ── NC_MXM_LVDS_B_DATA_N<3> (MAKE_BASE=TRUE NO_TEST=TRUE)
85 MXM_LVDS_B_DATA_P<3> ── NC_MXM_LVDS_B_DATA_P<3> (MAKE_BASE=TRUE NO_TEST=TRUE)

Unused MXM DP Interfaces

84 MXM_DP_B_ML_P<0..3> ── NC_MXM_DP_B_ML_P<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_B_ML_N<0..3> ── NC_MXM_DP_B_ML_N<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_B_AUX_P ── NC_MXM_DP_B_AUX_P (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_B_AUX_N ── NC_MXM_DP_B_AUX_N (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_B_HPD ── NC_MXM_DP_B_HPD (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_D_ML_P<0..3> ── NC_MXM_DP_D_ML_P<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_D_ML_N<0..3> ── NC_MXM_DP_D_ML_N<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_D_AUX_P ── NC_MXM_DP_D_AUX_P (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_D_AUX_N ── NC_MXM_DP_D_AUX_N (MAKE_BASE=TRUE NO_TEST=TRUE)
84 MXM_DP_D_HPD ── NC_MXM_DP_D_HPD (MAKE_BASE=TRUE NO_TEST=TRUE)

Unused MCP Interfaces

18 LVDS_IG_BKL_ON ── NC_LVDS_IG_BKL_ON (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_BKL_PWM ── NC_LVDS_IG_BKL_PWM (MAKE_BASE=TRUE NO_TEST=TRUE)
18 LVDS_IG_PANEL_PWR ── NC_LVDS_IG_PANEL_PWR (MAKE_BASE=TRUE NO_TEST=TRUE)
18 =MCP_HDMI_TXD_P<0..2> ── NC_MCP_HDMI_TXD_P<0..2> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 =MCP_HDMI_TXD_N<0..2> ── NC_MCP_HDMI_TXD_N<0..2> (MAKE_BASE=TRUE NO_TEST=TRUE)
18 =MCP_HDMI_TXC_P ── NC_MCP_HDMI_TXC_P (MAKE_BASE=TRUE NO_TEST=TRUE)
18 =MCP_HDMI_TXC_N ── NC_MCP_HDMI_TXC_N (MAKE_BASE=TRUE NO_TEST=TRUE)

92 91 90 95 6 =PP3V3_S0_DP
R8700 2.7K 5% 1/16W MF-LF 2 402
R8701 2.7K 5% 1/16W MF-LF 2 402

18 =MCP_HDMI_DDC_CLK ── DP_IG_DDC_CLK (MAKE_BASE=TRUE)
18 =MCP_HDMI_DDC_DATA ── DP_IG_DDC_DATA (MAKE_BASE=TRUE)
18 =MCP_HDMI_HPD ── DP_IG_HPD

R8710 22K 5% 1/16W MF-LF 2 402

18 DP_IG_AUX_CH_P ── NC_DP_IG_AUX_CH_P (MAKE_BASE=TRUE NO_TEST=TRUE)
18 DP_IG_AUX_CH_N ── NC_DP_IG_AUX_CH_N (MAKE_BASE=TRUE NO_TEST=TRUE)

18 DP_IG_CA_DET
R8711 1M 5% 1/16W MF-LF 2 402

SYNC_MASTER=MARKVIDEO SYNC_DATE=03/12/2009
PAGE TITLE: Display: Aliases
Apple Inc.
DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 87 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K23_DAVE SYNC_DATE=01/05/2009

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 88 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 89 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

CRITICAL
J9002
20389-Y30E-01
F-RT-SM

NOSTUFF
R9050
0
5%
1/16W
MF-LF
402

NOSTUFF
R9051
0
5%
1/16W
MF-LF
402

52 =SMB_DP_TCON_SCL
52 =SMB_DP_TCON_SDA

I2C MASTER ON TCON
I2C_TCON_SCL
I2C_TCON_SDA

107 92 DP_INT_AUXCH_N
107 92 DP_INT_AUXCH_P

107 92 DP_INT_LINK_P<0>	C9040	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_P<0>	NO TEST
107 92 DP_INT_LINK_N<0>	C9041	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_N<0>	NO TEST
107 92 DP_INT_LINK_P<1>	C9042	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_P<1>	NO TEST
107 92 DP_INT_LINK_N<1>	C9043	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_N<1>	NO TEST
107 92 DP_INT_LINK_P<2>	C9044	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_P<2>	NO TEST
107 92 DP_INT_LINK_N<2>	C9045	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_N<2>	NO TEST
107 92 DP_INT_LINK_P<3>	C9046	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_P<3>	NO TEST
107 92 DP_INT_LINK_N<3>	C9047	0.1uF 10% 16V X5R 402	107 DP_INT_LINK_CONN_N<3>	NO TEST

95 SPDIF_DP_AUDIO_OUT
95 90 VIDEO_ON
92 DP_HPD_INT

PANEL POWER CONTROL

6 =PP12V_S0_LCD

R9000 100K 5% 1/16W MF-LF 402
R9001 29.4K 1% 1/16W MF-LF 402
R9002 100K 5% 1/16W MF-LF 402
C9000 0.1UF 10% 50V X7R 603-1

LCD_PANEL_PWR_L_DIV
LCD_PANEL_PWR_L_RC

CRITICAL
Q9000
FDC638P_G
SM

PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9000
FERR-250-OHM
SM

C9020 10UF 10% 16V X5R-CERM 0805
C9001 0.001uF 20% 50V CERM 402

PP12V_LCD_CONN
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

6 =PP3V3_S0_VIDEO

C9010 0.001uF 20% 50V CERM 402

PLACE NEAR J9002

NOSTUFF
R9071
0
5%
1/10W
MF-LF
603

95 LCD_PANEL_PWR
LCD_PANEL_PWR_G
LCD_PANEL_PWR_L

Q9001
2N7002
SOT23-HF1

95 90 VIDEO_ON
R9072
0
5%
1/10W
MF-LF
603

R9070 100K 5% 1/16W MF-LF 402

BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video
Options for GPU or MLB HW controlled backlight enable are included

92 91 90 87 95 6 =PP3V3_S0_DP

NOSTUFF
C9011
0.1UF
20%
10V
CERM
402

NOSTUFF
U9050
TC7SZ08AFEAPE
SOT665

95 90 VIDEO_ON
95 LCD_BKL_ON_MUX

LCD_BKL_MLB_EN

NOSTUFF
R9012
1K
5%
1/16W
MF-LF
402

95 BACKLIGHT_PWM

R9081
47
5%
1/16W
MF-LF
402

LCD_PWM_FILT

CRITICAL
L9050
FERR-250-OHM
SM

LCD_PWM

6 VIDEO_ON_L
used by diag LED

92 91 90 87 95 6 =PP3V3_S0_DP

C9005
22UF
20%
6.3V
CERM
805

U9500
74LVC14
TSSOP-HF

95 90 VIDEO_ON

D9000
SOT23
BAT54XG

VIDEO_ON_L_DLY

U9520
74AUP2G14GM
SOT886

R9009
19.1K
1%
1/10W
MF-LF
402

R9011
1K
5%
1/16W
MF-LF
402

LCD_BKL_ON_DLY
LCD_BKL_ON

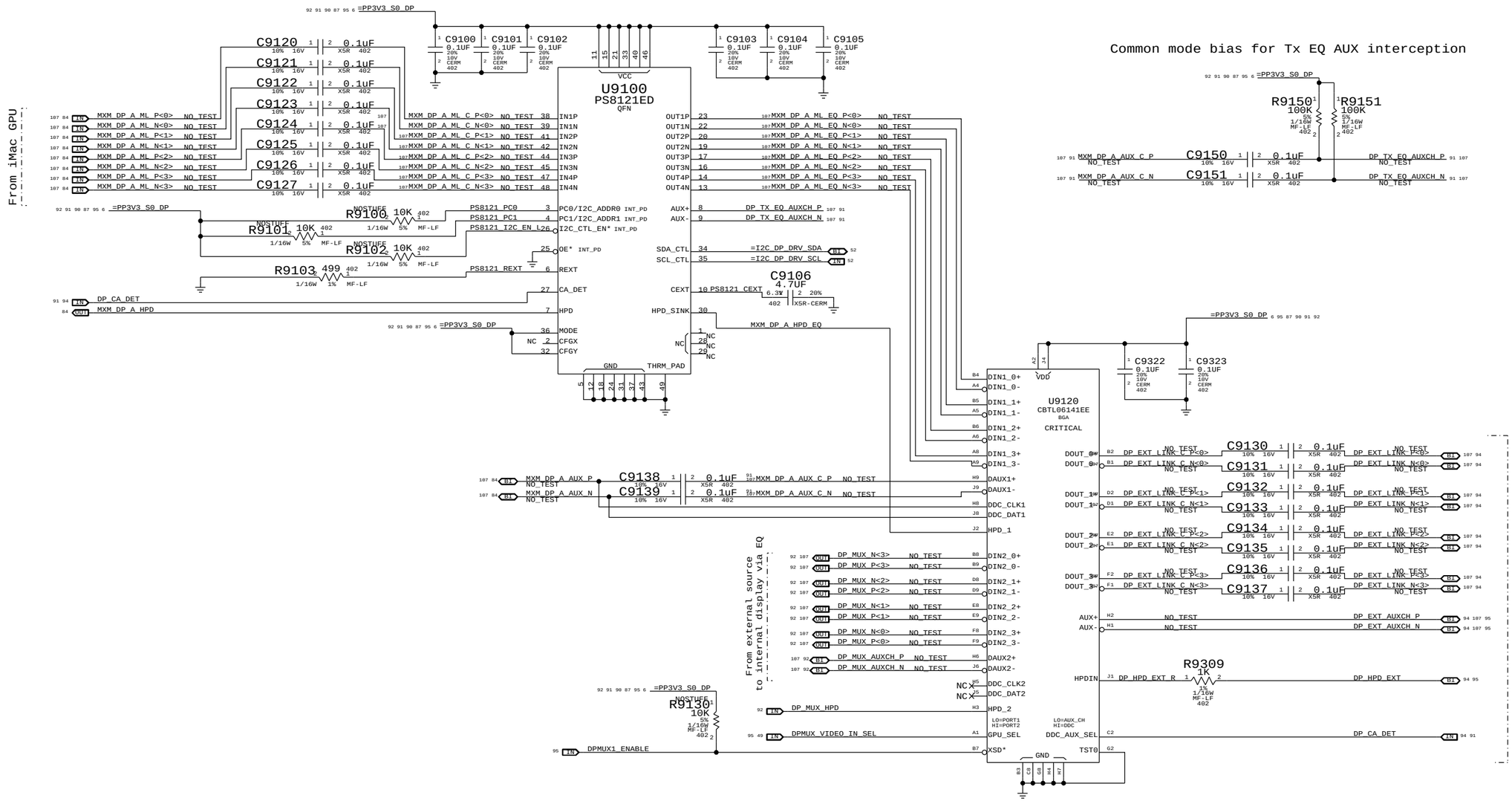
buffers are multiple parts, other parts are on csa 95

SYNC_MASTER=MARKVIDEO
SYNC_DATE=03/12/2009
PAGE TITLE
Display: Int DP Connector

Apple Inc.

DRAWING NUMBER 051-7863
SIZE D
REVISION A.0.0
BRANCH
PAGE 90 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

EQ & Re-Driver for DP source



DisplayPort Mux 1
Analog mux at External Connector

SYNC_MASTER=MARKVIDEO	SYNC_DATE=03/12/2009
PAGE TITLE: Display: BiDiVi Mux1	
Apple Inc.	DRAWING NUMBER: 051-7863 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 91 OF 110
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DisplayPort Equalizer & MUX 2

Note: INT_PD = Internal Pulldown on this pin of >=100 kOhms

=PP3V3_S0_DP

C9200 0.1UF 20% 10V CERM 402
C9201 0.1UF 20% 10V CERM 402
C9202 0.1UF 20% 10V CERM 402
C9203 0.1UF 20% 10V CERM 402
C9204 0.1UF 20% 10V CERM 402

U9200 PS8325 QFN CRITICAL

VDD: 4, 22, 38, 47, 62

From iMac GPU

C9240	MXM_DP_C_ML_P<0>	NO_TEST	MXM_DP_C_ML_C_P<0>
C9241	MXM_DP_C_ML_N<0>	NO_TEST	MXM_DP_C_ML_C_N<0>
C9242	MXM_DP_C_ML_P<1>	NO_TEST	MXM_DP_C_ML_C_P<1>
C9243	MXM_DP_C_ML_N<1>	NO_TEST	MXM_DP_C_ML_C_N<1>
C9244	MXM_DP_C_ML_P<2>	NO_TEST	MXM_DP_C_ML_C_P<2>
C9245	MXM_DP_C_ML_N<2>	NO_TEST	MXM_DP_C_ML_C_N<2>
C9246	MXM_DP_C_ML_P<3>	NO_TEST	MXM_DP_C_ML_C_P<3>
C9247	MXM_DP_C_ML_N<3>	NO_TEST	MXM_DP_C_ML_C_N<3>

0.1uF 10% 16V X5R 402

IN1_D0P	2	DP_D0P
IN1_D0N	3	DP_D0N
IN1_D1P	5	DP_D1P
IN1_D1N	6	DP_D1N
IN1_D2P	8	DP_D2P
IN1_D2N	9	DP_D2N
IN1_D3P	11	DP_D3P
IN1_D3N	12	DP_D3N
IN1_PEQ/SDA_CTL	68	=I2C_DP_EQLZ_SDA

DP_D0P	61	NO_TEST DP_INT_LINK_P<0>
DP_D0N	60	NO_TEST DP_INT_LINK_N<0>
DP_D1P	58	NO_TEST DP_INT_LINK_P<1>
DP_D1N	57	NO_TEST DP_INT_LINK_N<1>
DP_D2P	55	NO_TEST DP_INT_LINK_P<2>
DP_D2N	54	NO_TEST DP_INT_LINK_N<2>
DP_D3P	52	NO_TEST DP_INT_LINK_P<3>
DP_D3N	51	NO_TEST DP_INT_LINK_N<3>

To Internal display

From external input via MUX 1

IN2_D0P	14	DP_MUX_P<0>
IN2_D0N	15	DP_MUX_N<0>
IN2_D1P	17	DP_MUX_P<1>
IN2_D1N	18	DP_MUX_N<1>
IN2_D2P	20	DP_MUX_P<2>
IN2_D2N	21	DP_MUX_N<2>
IN2_D3P	23	DP_MUX_P<3>
IN2_D3N	24	DP_MUX_N<3>
IN2_PEQ/SCL_CTL	67	=I2C_DP_EQLZ_SCL

TMDS_CH0P	43	NC
TMDS_CH0N	42	NC
TMDS_CH1P	46	NC
TMDS_CH1N	45	NC
TMDS_CH2P	49	NC
TMDS_CH2N	48	NC
TMDS_CLKN	39	NC
TMDS_CLKP	40	NC

=PP3V3_S0_DP

R9221 1K 5% 1/16W MF-LF 402
R9215 1K 5% 1/16W MF-LF 402
R9220 1K 5% 1/16W MF-LF 402

DP_EQLZ_MODE0 → 64 MODE0
DP_EQLZ_MODE1 → 65 MODE1
DP_EQLZ_MODE2 → 69 MODE2

MODE[2..0] = 111 SELECTS I2C CONTROL MODE

R9222 4.99K 1% 1/16W MF-LF 402: DP_EQLZ_EXTR → 70 REXT

C9212 4.7UF 20% 6.3V X5R-CERM 402: CEXT 1 — DP_EQLZ_EXTC

see below

TMDS_SCL	NC	DP_AC_AUXP 30 NO_TEST DP_EQLZ_AUXCH_P
TMDS_SDA	NC	DP_AC_AUXN 31 NO_TEST DP_EQLZ_AUXCH_N

R9280 NOSTUFF 5% 1/16W MF-LF 402: DP_EQLZ_ADDR → 66 SW/I2C_ADDR (INT_PD)

To Internal display

From iMac GPU

C9248	MXM_DP_C_AUX_P	NO_TEST	MXM_DP_C_AUX_C_P
C9249	MXM_DP_C_AUX_N	NO_TEST	MXM_DP_C_AUX_C_N

0.1uF 10% 16V X5R 402

From external input via MUX 1

DP_MUX_AUXCH_P	NO_TEST	IN2_AUXP_SCL
DP_MUX_AUXCH_N	NO_TEST	IN2_AUXN_SDA

IN1_AUXP_SCL	28	DP_AUXP_SCL 32 NO_TEST DP_INT_AUXCH_P
IN1_AUXN_SDA	29	DP_AUXN_SDA 33 NO_TEST DP_INT_AUXCH_N

R9281 1M 5% 1/16W MF-LF 402: DP_EQLZ_CADET → 56 DP_CADET

INT_PDIN1_CADET → 7 NC
INT_PDIN2_CADET → 16 NC

From Internal display: DP_HPD_INT → 53 DP_HPD (INT_PD)

IN1_HPDX	10	MXM_DP_C_HPD → TO IMAC GPU
IN2_HPDX	19	DP_MUX_HPD → TO EXTERNAL SOURCE VIA MUX1

TMDS_HPD	NC	INT_PD
TMDS_PC0	NC	
TMDS_PC1	NC	
PIOINT_PD	NC	
PDINT_PD	NC	

GND: 13, 27, 36, 50, 63, 72, 73 — THRM_PAD

Pulls for AUX_CH from DisplayPort Mux #2

=PP3V3_S0_DP

R9212 100K 1% 1/16W MF-LF 402 → MXM_DP_C_AUX_C_N
R9213 100K 1% 1/16W MF-LF 402 → MXM_DP_C_AUX_C_P

AC caps for EQ AUX interception

C9290 0.1uF 10% 16V X5R 402: DP_EQLZ_AUXCH_P NO_TEST — DP_INT_AUXCH_P NO_TEST

C9291 0.1uF 10% 16V X5R 402: DP_EQLZ_AUXCH_N NO_TEST — DP_INT_AUXCH_N NO_TEST

SYNC_MASTER=MASTER	SYNC_DATE=N/A
PAGE TITLE	BIDIVI DP MUX2
Apple Inc.	DRAWING NUMBER 051-7863
	SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 92 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=K22 SYNC_DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

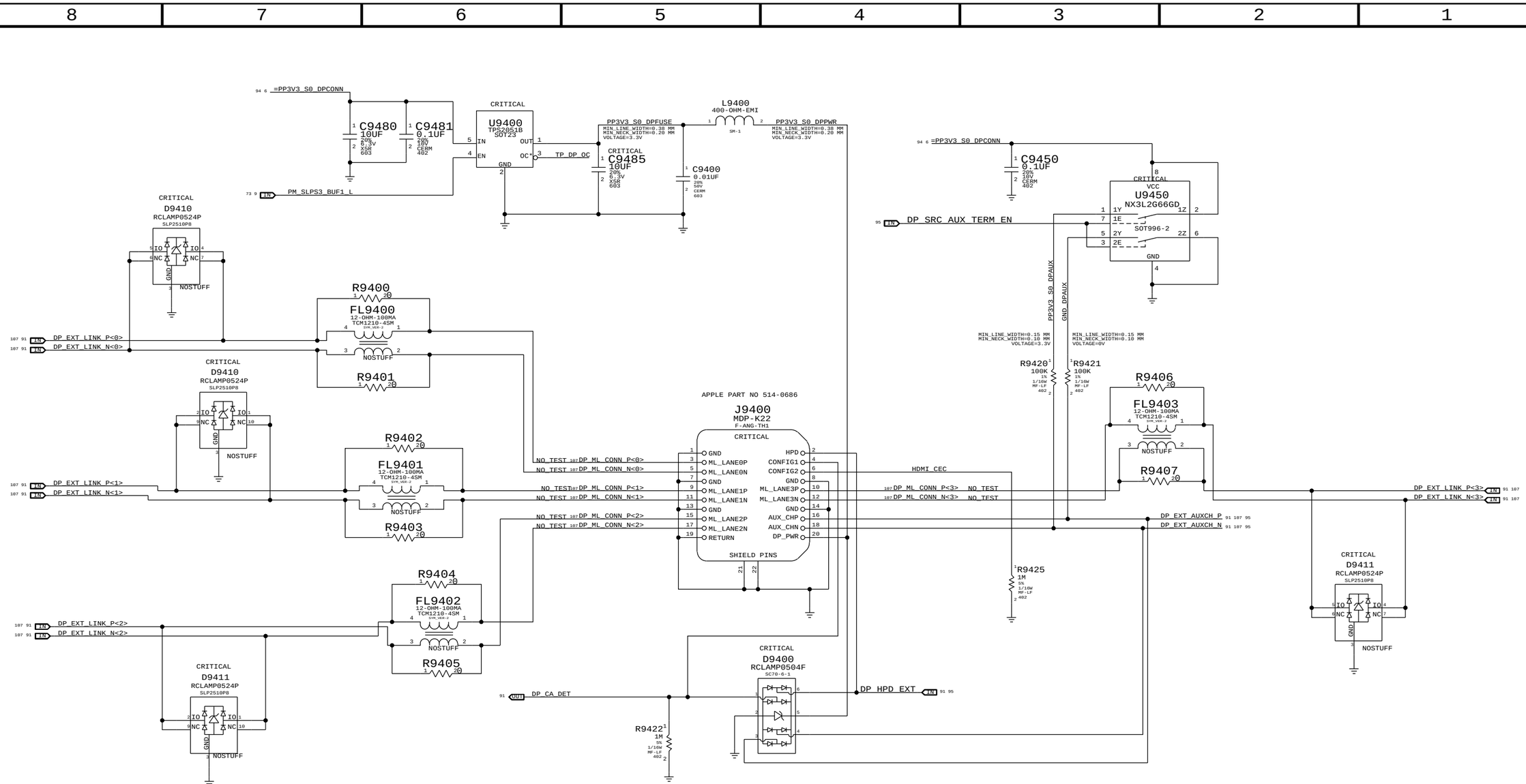
DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 93 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=MARKVIDEO SYNC_DATE=03/12/2009

PAGE TITLE

Display: Ext DP Connector

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

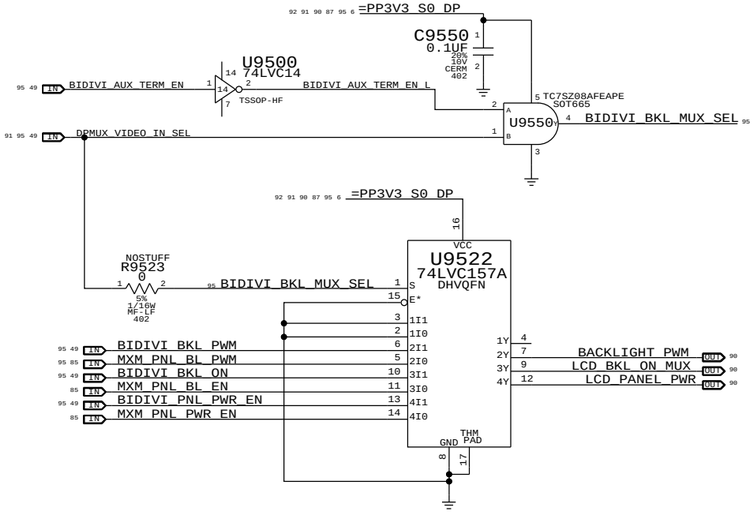
REVISION A.0.0

BRANCH

PAGE 94 OF 110

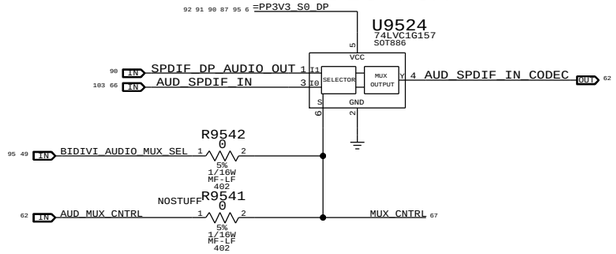
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PANEL/BACKLIGHT CONTROL MUX

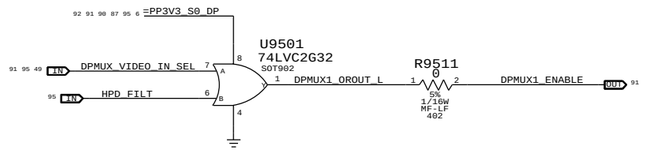


DisplayPort AUDIO MUX

PLACE NEAR U6201

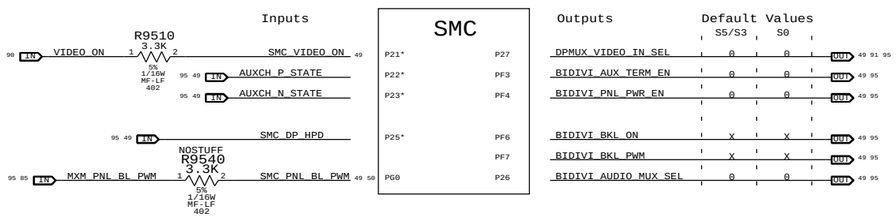


BiDiVi MUX Enable

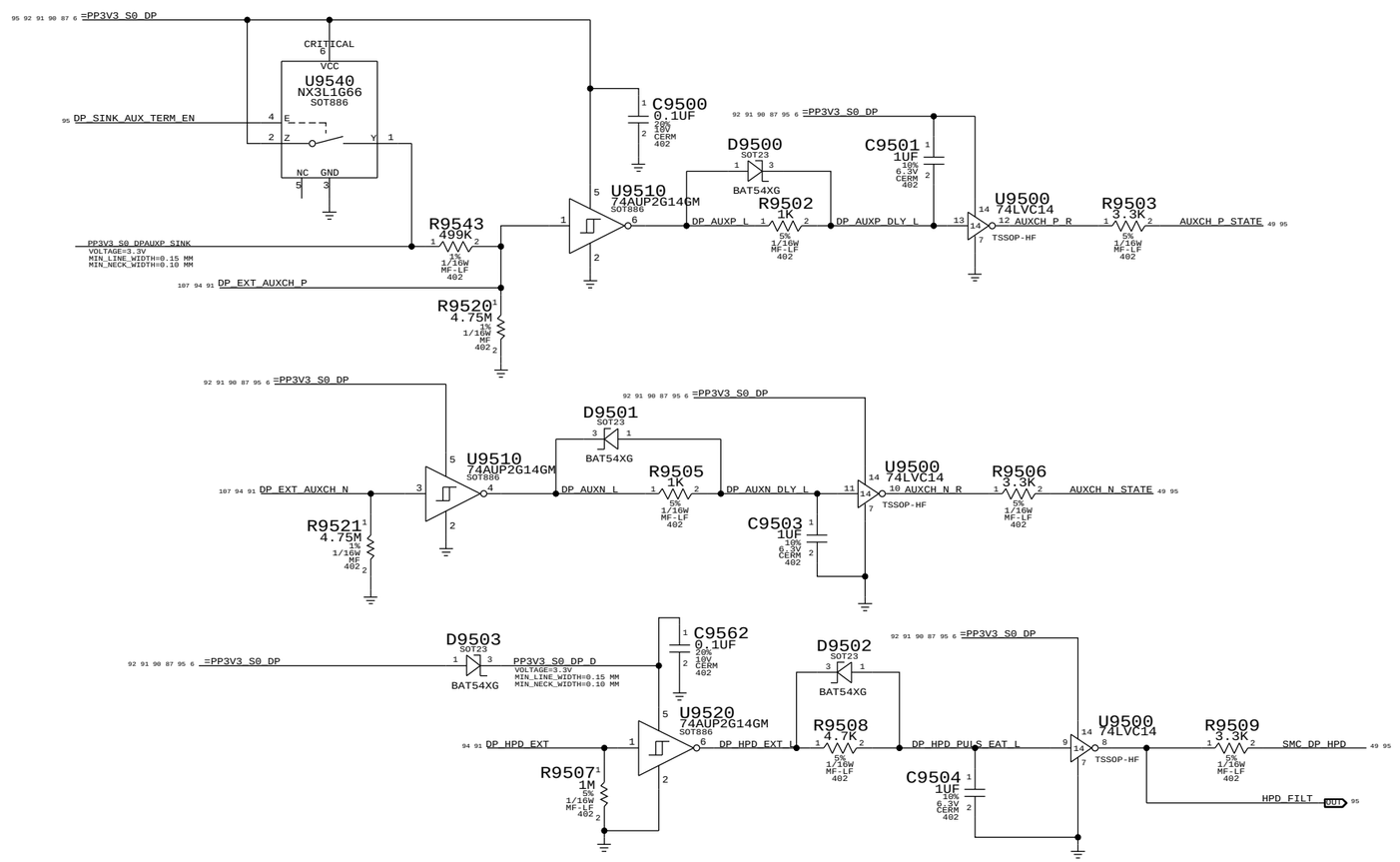


*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

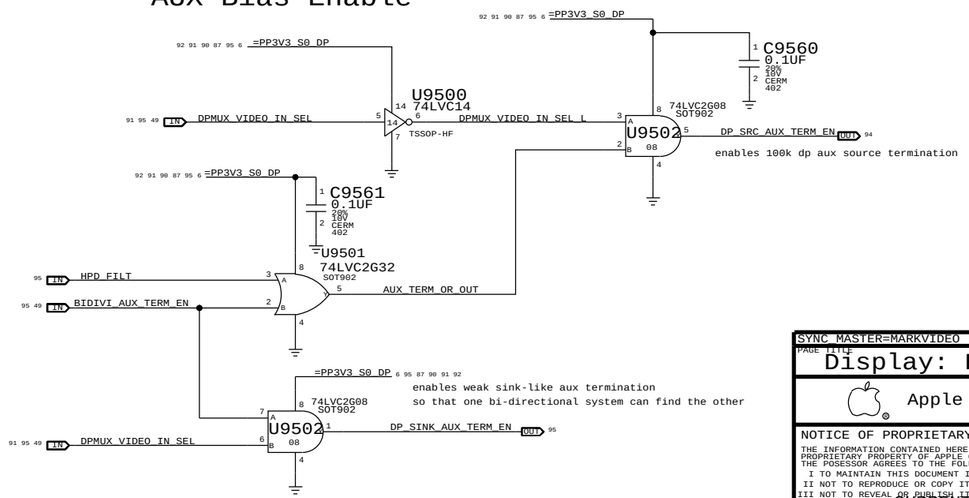
SMC Signals for BiDiVi



External AUX Channel and HPD Buffers & filters



AUX Bias Enable



SYNC_MASTER=MARKVIDEO SYNC_DATE=03/12/2009

PAGE TITLE: Display: BiDiVi Support

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 95 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 96 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 97 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 98 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8 7 6 5 4 3 2 1

D C B A

SYNC MASTER=K22 SYNC DATE=12/02/2008

PAGE TITLE

BLANK PAGE

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D

REVISION A.0.0

BRANCH

PAGE 99 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighther than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommmends each strobe/signal group is routed on the same layer.
Intel Design Guide recommmends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	Group 0	FSB_42S	FSB_DATA	FSB_D_L<15..0>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	Group 1	FSB_42S	FSB_DATA	FSB_D_L<31..16>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	Group 2	FSB_42S	FSB_DATA	FSB_D_L<47..32>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	Group 3	FSB_42S	FSB_DATA	FSB_D_L<63..48>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	Group 0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
		FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	Group 1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals		FSB_50S	FSB_1X	FSB_ADS_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ1_L	14
		FSB_50S	FSB_1X	FSB_BNR_L	10 14
		FSB_50S	FSB_1X	FSB_BPRI_L	10 14
		FSB_50S	FSB_1X	FSB_DBSY_L	10 14
		FSB_50S	FSB_1X	FSB_DEFER_L	10 14
		FSB_50S	FSB_1X	FSB_DRDY_L	10 14
		FSB_50S	FSB_1X	FSB_HIT_L	10 14
		FSB_50S	FSB_1X	FSB_HITM_L	10 14
		FSB_50S	FSB_1X	FSB_LOCK_L	10 14
		FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
		FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
		FSB_50S	FSB_1X	FSB_TRDY_L	10 14
		CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
		CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	11 14
		CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
		CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
		CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
		CPU_50S	CPU_AGTL	CPU_INTR	10 14
		CPU_50S	CPU_AGTL	CPU_NMI	10 14
		CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 14 50
		CPU_50S	CPU_AGTL	CPU_PWRGD	11 13 14
		CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
		CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
		CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 14 50
		CPU_50S	CPU_AGTL	FSB_CPUSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L	11 14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
		CPU_50S	CPU_AGTL	CPU_IERR_L	10
		CPU_50S	CPU_GTLREF	CPU_GTLREF0	10 11 29
		CPU_50S	CPU_GTLREF	CPU_GTLREF1	10 11 29
		CPU_27P4S	CPU_COMP	CPU_COMP<8>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<3>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<2>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<1>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<0>	11
		CPU_50S	CPU_ITP	CPU_XDP_TDI	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TDO	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TMS	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TCK	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TRST_L	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPM_L<5..0>	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPMB<3..0>	11 13
		CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<7..0>	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_P	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_N	12 71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_P	71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_N	71

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 100 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 16 31
	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 31
	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 16 32
	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 32
	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 33

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 33
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

SYNC_MASTER=K22 SYNC_DATE=09/02/2009
PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 101 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84 86
PCIE I/O				
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_N	34
	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 34
	PCIE_90D	PCIE	PCIE_FW_R2D_P	41
	PCIE_90D	PCIE	PCIE_FW_R2D_N	41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9 87
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9 87
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 41
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 41
SATA				
	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_HDD_R2D_P	45 110
	SATA_100D	SATA	SATA_HDD_R2D_N	45 110
	SATA_100D	SATA	SATA_HDD_D2R_P	20 45
	SATA_100D	SATA	SATA_HDD_D2R_N	20 45
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45 110
	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_ODD_R2D_P	45 110
	SATA_100D	SATA	SATA_ODD_R2D_N	45 110
	SATA_100D	SATA	SATA_ODD_D2R_P	20 45
	SATA_100D	SATA	SATA_ODD_D2R_N	20 45
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45 110
	MCP_SGS	SATA_TERMP	MCP_SATA_TERMP	20
MISC				
	MCP_SGS	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18 26
	MCP_SGS	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18 26
			PM_SLP_S3_L	9 21
			PM_SLP_S4_L	21 70

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MCP Constraints 1

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 102 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCI_55S	PCI	PCI_REQ0_L	19
	PCI_55S	PCI	PCI_REQ1_L	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
	LPC_55S	LPC	LPC_AD<3..0>	19 49 51
	LPC_55S	LPC	LPC_AD_R<3..0>	19
	LPC_55S	LPC	LPC_FRAME_L	19 49 51
	LPC_55S	LPC	LPC_FRAME_R_L	19
	LPC_55S	LPC	LPC_RESET_L	9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	9 19
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	9 49
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	9 51
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R	9 21
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK	9 49
	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
	USB_90D	USB	USB_EXTA_P	20 46
	USB_90D	USB	USB_EXTA_N	20 46
	USB_90D	USB	USB_PORT0_P	46
	USB_90D	USB	USB_PORT0_N	46
	USB_90D	USB	USB_EXTB_P	20 46
	USB_90D	USB	USB_EXTB_N	20 46
	USB_90D	USB	USB_PORT1_P	46
	USB_90D	USB	USB_PORT1_N	46
	USB_90D	USB	USB_EXTC_P	20 46
	USB_90D	USB	USB_EXTC_N	20 46
	USB_90D	USB	USB_PORT2_P	46
	USB_90D	USB	USB_PORT2_N	46
	USB_90D	USB	USB_EXTD_P	20 46
	USB_90D	USB	USB_EXTD_N	20 46
	USB_90D	USB	USB_D_MUXED_P	46
	USB_90D	USB	USB_D_MUXED_N	46
	USB_90D	USB	USB_PORT3_P	46
	USB_90D	USB	USB_PORT3_N	46
	USB_90D	USB	USB_CAMERA_P	20 47
	USB_90D	USB	USB_CAMERA_N	20 47
	USB_90D	USB	USB_CAMERA_L_P	47 110
	USB_90D	USB	USB_CAMERA_L_N	47 110
	USB_90D	USB	USB_BT_P	20 47
	USB_90D	USB	USB_BT_N	20 47
	USB_90D	USB	USB_BT_L_P	47 110
	USB_90D	USB	USB_BT_L_N	47 110
	USB_90D	USB	USB_IR_P	20 47
	USB_90D	USB	USB_IR_N	20 47
	USB_90D	USB	USB_IR_L_P	47 110
	USB_90D	USB	USB_IR_L_N	47 110
	USB_90D	USB	USB_SDCARD_P	20 47
	USB_90D	USB	USB_SDCARD_N	20 47
	USB_90D	USB	USB_SDCARD_L_P	47 110
	USB_90D	USB	USB_SDCARD_L_N	47 110
	MCP_55S	SPI	SPI_CLK_R	21 51 61
	MCP_55S	SPI	SPI_CLK	61
	MCP_55S	SPI	SPI_MOSI_R	21 51 61
	MCP_55S	SPI	SPI_MOSI	61
	MCP_55S	SPI	SPI_MISO	21 51 61
	MCP_55S	SPI	SPI_MISO_R	61
	MCP_55S	SPI	SPI_CS0_R_L	21 51
	MCP_55S	SPI	SPI_CS0_L	51
	HDA_55S	HDA	HDA_BIT_CLK	21 62
		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
	HDA_55S	HDA	HDA_RST_L	21 62
	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_SDOUT	21 62
	HDA_55S	HDA	HDA_SDOUT_R	21
	HDA_55S	HDA	HDA_SYNC	21 62
	HDA_55S	HDA	HDA_SYNC_R	21
	HDA_55S	HDA	HDA_SDIN0	21 62
	HDA_55S	HDA	AUD_SDI_R	62
		HDA	AUD_SPDIF_IN	9 66
		HDA	AUD_SPDIF_OUT	62 66
		HDA	AUD_SPDIF_CHIP	62
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT	21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN	21 28

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: MCP Constraints 2

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 103 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

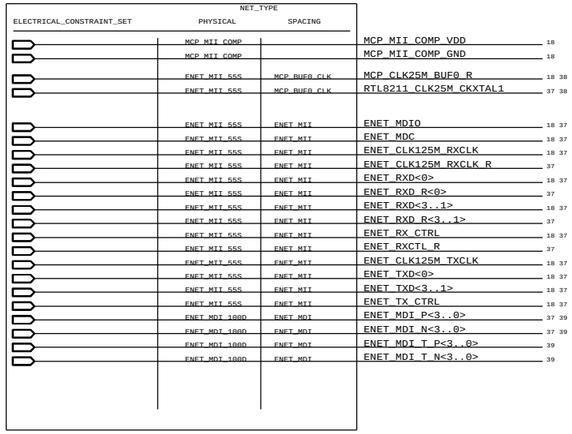
SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: Ethernet Constraints

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 104 OF 110

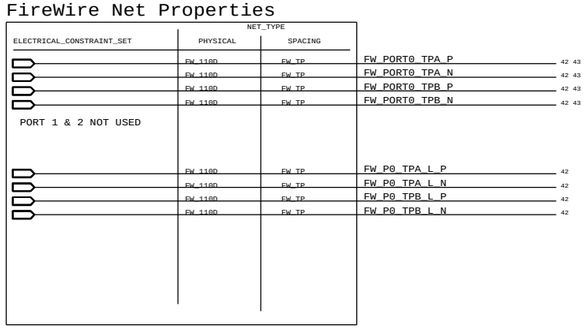
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties



SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: FireWire Constraints

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 105 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	52
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	52
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	52
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	52
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	52
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	52
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	52
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	52
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_55S	SMB	SMBUS_MCP_0_CLK	13 21 52
	SMB_55S	SMB	SMBUS_MCP_0_DATA	13 21 52

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 106 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08MM	=100_OHM_DIF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	3:1_SPACING
DISPLAYPORT	POWER	*	PWR_P2MM
DISPLAYPORT	GND	*	GND_P2MM

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
ASSINGED IN CONT. MGR.			
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_P<3..0> 84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_N<3..0> 84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0> 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0> 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0> 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0> 91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_P 84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_N 84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_C_P 91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_C_N 91
	DP_100D	DISPLAYPORT	DP_EXT_LINK_P<3..0> 91 94
	DP_100D	DISPLAYPORT	DP_EXT_LINK_N<3..0> 91 94
	DP_100D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0> 91
	DP_100D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0> 91
	DP_100D	DISPLAYPORT	DP_EXT_AUXCH_P 91 94 95
	DP_100D	DISPLAYPORT	DP_EXT_AUXCH_N 91 94 95
	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0> 94
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0> 94
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_P<3..0> 84 92
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_N<3..0> 84 92
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0> 92
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0> 92
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_P 84 92
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_N 84 92
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_C_P 92
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_C_N 92
	DP_100D	DISPLAYPORT	DP_INT_LINK_P<3..0> 92 90
	DP_100D	DISPLAYPORT	DP_INT_LINK_N<3..0> 92 90
	DP_100D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0> 90
	DP_100D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0> 90
	DP_100D	DISPLAYPORT	DP_INT_AUXCH_P 92 90
	DP_100D	DISPLAYPORT	DP_INT_AUXCH_N 92 90
	DP_100D	DISPLAYPORT	DP_MUX_P<3..0> 91 92
	DP_100D	DISPLAYPORT	DP_MUX_N<3..0> 91 92
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_P 91 92 107
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_N 91 92 107
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_P 91 92 107
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_N 91 92 107
	DP_100D	DISPLAYPORT	DP_TX_EQ_AUXCH_P 91
	DP_100D	DISPLAYPORT	DP_TX_EQ_AUXCH_N 91
	DP_100D	DISPLAYPORT	DP_EQLZ_AUXCH_P 92
	DP_100D	DISPLAYPORT	DP_EQLZ_AUXCH_N 92
	MCP_DV_COMP		MCP_HDMI_RSET 18 26
	MCP_DV_COMP		MCP_HDMI_VPROBE 18 26

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
Graphics Constraints

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 107 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6 30 31
		PPDDR_MEM	=PP1V5_S3_MEM_B	6 30 32
		SWITCHNODE	VR_CPU_SW1	72
		SWITCHNODE	VR_CPU_SW2	72
		SWITCHNODE	VR_CPU_SW3	72
		SWITCHNODE	1V8_SW	80
		SWITCHNODE	1V1S5_SW	79
		SWITCHNODE	PVTTS0_PHASE	76
		SWITCHNODE	3V3S5_SW	76
		SWITCHNODE	5VS3_SW	73
		SWITCHNODE	MCPCORES0_PHASE	74
	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55
	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55
	THERM_DIFF	THERMAL	CPU_THERMD_P	11 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	11 55
	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21 55
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54
	THERM_DIFF	THERMAL	SNS_LCD_P	55 110
	THERM_DIFF	THERMAL	SNS_LCD_N	55 110
	THERM_DIFF	THERMAL	SNS_ODD_P	55 110
	THERM_DIFF	THERMAL	SNS_ODD_N	55 110
	THERM_DIFF	THERMAL	SNS_CPU_H_P	55
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55
	THERM_DIFF	THERMAL	SNS_MCP_P	55
	THERM_DIFF	THERMAL	SNS_MCP_N	55
	THERM_DIFF	THERMAL	SNS_AMB_P	55 110
	THERM_DIFF	THERMAL	SNS_AMB_N	55 110
	THERM_DIFF	THERMAL	SNS_MXM_P	55
	THERM_DIFF	THERMAL	SNS_MXM_N	55
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	71
1215		THERMAL	SMC_CPU_ISENSE	49 53
1216		THERMAL	VR_CPU_IOUT	53 71
1217		THERMAL	VR_ISNS_CPU_P	53
1218		THERMAL	VR_ISNS_CPU_N	53
1219		THERMAL	SNS_PS_CPU_ISNS	53
1220		THERMAL	SMC_CPU_VSENSE	49 53
1221		THERMAL	CPU_VCC_SENSE	12 53
1222		THERMAL	SMC_GPU_VSENSE	49 53
1223		THERMAL	SMC_GPU_ISENSE	49 53
1224		THERMAL	SMC_1V5_S0_ISENSE	50 54
1225		THERMAL	SMC_1V5_S0_ISENSE_R	54
1226		THERMAL	SMC_1V5_S0_VSENSE	50 54
1227		THERMAL	SMC_MCP_CORE_ISENSE	50 54
1228		THERMAL	SMC_MCP_CORE_VSENSE	50 54
1229		THERMAL	MCPCORES0_IMON	54 74
1230		THERMAL	CPU_PECI_L	11 55
1231		THERMAL	SMB_PECI_L	55
1232		THERMAL	CPU_PECI_MCP	14 55
		THERMAL	HDD_OOB_TEMP_FILT	55
1233		THERMAL	HDD_OOB_TEMP	55
1234		THERMAL	HDD_OOB_TEMP_R	55
1235		THERMAL	SMC_HDD_OOB_TEMP	55

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE
K22/K23 SPECIFIC CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 108 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD_UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

SYNC_MASTER=K22 SYNC_DATE=09/02/2009

PAGE TITLE: K22/K23 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER: 051-7863 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 109 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

103 47	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
103 47	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

103 47	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
103 47	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

103 47	IN	USB_BT_L_P	FUNC_TEST=TRUE
103 47	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

103 47	IN	USB_IR_L_P	FUNC_TEST=TRUE
103 47	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

102 45	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
49 45	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

102 45	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

108 55	IN	SNS_LCD_P	FUNC_TEST=TRUE
108 55	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

108 55	IN	SNS_AMB_P	FUNC_TEST=TRUE
108 55	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

108 55	IN	SNS_ODD_P	FUNC_TEST=TRUE
108 55	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

56	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH0_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
56	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

57	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
57	IN	FAN_TACH2_L	FUNC_TEST=TRUE
57	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
57	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

56	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH1_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
56	IN	FAN_1_GND	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

66	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
66	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
66	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

	IN	AUD_SPKR_OUTLO2R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO2R_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1R_N	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

	IN	AUD_SPKR_OUTLO2L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO2L_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1L_N	FUNC_TEST=TRUE

		GND	16 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
78 6	IN	PP3V3_S3	2 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
73 6	IN	PP5V_S3_REG	2 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
78 6	IN	PP5V_S0		FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

SYNC MASTER=K22 SYNC DATE=09/02/2009

PAGE TITLE
K22/K23 ICT/FCT

Apple Inc.

DRAWING NUMBER 051-7863 SIZE D
REVISION A.0.0
BRANCH
PAGE 110 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>