SCHEM, FLYING CLOUD, MLB, K90i

"EVT3"  11/22/10

ALIASES RESOLVED

Schematic / PCB #'s

<table>
<thead>
<tr>
<th>Schematic / PCB #'s</th>
<th>DESCRIPTION</th>
<th>REFERENCE</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>3K1-MLB</td>
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<td>3K1-MLB</td>
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</table>

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APPD

DATE

SIZE

D

A

D
to low voltage signals for the processor
to convert the active high signal from Embedded DisplayPort sink device
Therefore, an inverting level shifter is required on the motherboard
even if internal Graphics is disabled since they are
Intel Doc 438297 Huron River SFF DG rev1.0 section 2.2.1 recommendation.
CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 3x 2.2uF, 2x 22uF, 4x 470uF

Note: The smallest 10mOhm available in the library are 0805s

CPU VCCIO/VCCP DECOUPLING

Intel recommendation (Section 6.4): 2x 1uF, 1x 330uF
VAKG DECOUPLING

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

PLACEMENT_NOTE (C1738-C1747):
Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

Intel recommendation (Section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

PLACEMENT_NOTE (C1748-C1756):

CPU VCCSA DECOUPLING

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

PLACEMENT_NOTE (C1763-C1771):

www.vinafix.vn
NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

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=MEM_A_DQ<52>

=MEM_A_DQ<49>

=MEM_A_DQ<55>

=MEM_A_DQ<45>

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=MEM_B_DQ<6>

=MEM_B_DQ<0>

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=MEM_B_DQ<5>

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=MEM_B_DQ<0>

=MEM_B_DQS_P<0>

=MEM_B_DQS_P<0>

=MEM_B_DQS_N<0>
must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

S0 to S3

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

<table>
<thead>
<tr>
<th>Step</th>
<th>ISOLATE_CPU_MEM_L</th>
<th>PLT_RESET_L</th>
<th>PM_SLP_S3_L</th>
<th>PM_SLP_S4_L</th>
<th>CPU_MEM_RESET_L</th>
<th>MEM_RESET_L</th>
<th>MEMVTT_EN</th>
<th>P1V5CPU_EN</th>
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</thead>
<tbody>
<tr>
<td>S0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>S1</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>S2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>S3</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

**1V5 S0 "PGOOD" for CPU**

MEMVTT Clamp

Ensures CKE signals are held low in S3

**CPU Memory S3 Support**

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DAC step size: 5mV / step @ output

+33μA - -33μA (- = sourced)

0.300V - 1.200V (+/- 450mV)

0.75V (DAC: 0x3A)

VOLTAGE=3.3V
MIN NECK WIDTH=0.2 mm
MIN LINE WIDTH=0.3 mm

PP3V3_S3_VREFMRGN_DAC

VREFMRGN

33

Page Notes

Signal aliases required by this page:

- =I2C_PCA9557D_SCL
- =I2C_VREFDACS_SDA

Circuitry.

VREFMRGN     - Stuffs VREF Margining

BOM options provided by this page:

- =I2C_PCA9557D_SCL
- =I2C_VREFDACS_SDA

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER QTY DESCRIPTION REFERENCE SHEET CRITICAL BOM OPTION
1164862 2 3NCpine VREFMRGN_DAC VREFMRGN_WK

DAC Channel:

A
B
C
C

Nominal value
0.75V (DAC: 0x3A)

Margined target:
0.300V - 1.200V (+/- 450mV)

DAC range:
0.000V - 1.000V (0x00 - 0x7F)

VRef current:
-3.3mA - +3.3mA (- = sourced)

DAC step size:
5mV / step @ output

DAC Channel:

A
B
C
C

Nominal value
1.5V (DAC: 0x3A)

Margined target:
1.999V - 1.001V (+/- 450mV)

DAC range:
0.000V - 1.000V (0x00 - 0x7F)

VRef current:
+3.3mA - -3.3mA (- = sourced)

DAC step size:
5mV / step @ output

DAC Channel:

A
B
C
C

Nominal value
1.267V (DAC: 0x8B)

Margined target:
1.054V - 1.442V (+/- 180mV)

DAC range:
0.000V - 1.000V (0x00 - 0x7F)

VRef current:
+4.06mA - -6.91mA (- = sourced)

DAC step size:
5mV / step @ output

DAC Channel:

A
B
C
C

Nominal value
8.59mV / step @ output

Margined target:
+33μA - -33μA (- = sourced)

DAC range:
0.000V - 3.300V (0x00 - 0xFF)

VRef current:
+6.0mA - -5.0mA (- = sourced)

DAC step size:
100K

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER QTY DESCRIPTION REFERENCE SHEET CRITICAL BOM OPTION
1164862 2 3NCpine VREFMRGN_DAC VREFMRGN_WK

DAC Channel:

A
B
C
C

Nominal value
0.75V (DAC: 0x3A)

Margined target:
0.300V - 1.200V (+/- 450mV)

DAC range:
0.000V - 1.000V (0x00 - 0x7F)

VRef current:
-3.3mA - +3.3mA (- = sourced)

DAC step size:
5mV / step @ output

DAC Channel:

A
B
C
C

Nominal value
1.5V (DAC: 0x3A)

Margined target:
1.999V - 1.001V (+/- 450mV)

DAC range:
0.000V - 1.000V (0x00 - 0x7F)

VRef current:
+3.3mA - -3.3mA (- = sourced)

DAC step size:
5mV / step @ output

DAC Channel:

A
B
C
C

Nominal value
1.267V (DAC: 0x8B)

Margined target:
1.054V - 1.442V (+/- 180mV)

DAC range:
0.000V - 1.000V (0x00 - 0x7F)

VRef current:
+4.06mA - -6.91mA (- = sourced)

DAC step size:
5mV / step @ output

DAC Channel:

A
B
C
C

Nominal value
8.59mV / step @ output

Margined target:
+33μA - -33μA (- = sourced)

DAC range:
0.000V - 3.300V (0x00 - 0xFF)

VRef current:
+6.0mA - -5.0mA (- = sourced)

DAC step size:
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

SD CARD CONNECTOR

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SYNC_DATE=05/26/2010
PAGE 35 OF 109

Apple Inc.
BOM options provided by this page:
- =PP3V3_T29_P3V3T29FET     (3.3V FET Input)
- =PP18V_T29_REG            (18V Boost Output)
- =PPVIN_SW_T29BST          (8-13V Boost Input)

Signal aliases required by this page:
- =PP1V05_T29
- =PP15V_T29
- =PP5V25_T29

Pull-up provided by SB page.
Open-Drain GPIO
Platform (PCIe) Reset

Supervisor & CLKREQ# Isolation

3.3V T29 Switch

1.05V T29 Switch

180PF CERM

Apple Inc.

T29 Power Support

Apple Inc.

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Page Notes

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FireWire Port Power Switch

FireWire PHY WAKE# Support

When PHY is powered, FW_WAKE# acts as legacy PME# signal.

Dual-purpose output:
1) FW_WAKE# (PME#) when PHY is powered.
2) 5K Pull-down when FW_PWR_EN is low.

Current source only active when FW_PWR_EN is low.
All FireWire devices require 5K pull-down on TPB pair.

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

To avoid an extra power supply, LSI FireWire PHY requires 1.0V.
1.0V is needed with a decr & regulator to reduce voltage.

Supervisor & CLKREQ# Isolation

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Most can detect as long as TPMA# signal is present.
Current source only active when TPMA# is low.
Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux

Left USB Port A

Left USB Port B

We can add protection to 5V if we want, but leaving NC for now
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designated as outputs require pull-ups.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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</thead>
<tbody>
<tr>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
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</tr>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

Unused pins have "SMC_Pxx" names. Unused
pins designated as outputs require pull-ups.
LPC+SPI Connector

SPI Bus Series Termination
Detect Fin Stack Temperature

BC846BMXXH
SOT732-3
Q5520

PLACE Q5520 on BOTTOM side close to finstack

Placement note:
Detect CPU Die Temperature

BC846BMXXH
SOT732-3
Q5510

PLACE Q5510 next to DDR/5V/3.3V supply on TOP side

Placement note:

Detect DDR/5V/3.3V Proximity Temperature

MF-LF
1/16W
402

R5520
0.0022uF

C5522

CPU Proximity/CPU Die/5V-3.3V Proximity

CERM
10V
20%

0.0022uF

R5521

C5512

Detect T29 Die Temperature

MF-LF
1/16W

10K
402
5%

R5522

PCH-T29 Proximity/FinStack

T29 Die

Write Address: 0x99
Read Address: 0x99

CRITICAL
Emc1412-A
www.vinafix.vn

Apple Inc.
Thermal Sensors

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SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys pressed with PSOC power to isolate when PSOC is not powered.
BOoster +18.5VDC FOR sENsors

booster Design consideration:
- Power consumption
- Drop line regulation
- Ripple to meet spec
- Startup time less than 2ms
- V5b2, V5b1, V5b1 booster

confirm if this can be connected to S3!!

keyboard backlight driver & detection

To detect keyboard backlight, SMC will tristate and read SMC SYS_KBDLED.
If LOW, keyboard backlight present.
If HIGH, keyboard backlight not present.
KB_BL always stuffed, stuff only grounded when KB BL flex connected.

KB_BL high indicates keyboard backlight not present.
KB_BL low indicates keyboard backlight present.

Booster Design Consideration:
- V5b3 for sensors
- Power consumption
- Drop line regulation
- Ripple to meet spec
- Startup time less than 2ms
- Power consumption

boosted +18.5VDC for sensors.

ckeyboard backlight driver & detection

- StartUp time less than 2ms
- 100-300 kHz clean spectrum
- Ripple to meet ERS
- DROop line regulation
- Power consumption

booster design consideration:
- +18.5VDC for sensors
- Power consumption
- Drop line regulation
- Ripple to meet spec
- Startup time less than 2ms
- V5b2, V5b1, V5b1 booster

convert if this can be connected to S3!!
NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when placed on top-side:

- +Z (up)
- +Y
- +X

Front of system

Circle indicates pin 1 location when placed in correct orientation:

BYPASS=U5920.14:13:8 mm

C5922

10k 1/16W MF-LF 5%

R5920

1

2

R5921

12

10k 1/16W MF-LF 5%

R5922

12

402

1/16W 5%

SYNC_MASTER=LINDA_K90I

SYNC_DATE=07/08/2010

Digital Accelerometer
LINE INPUT VOLTAGE DIVIDER

CODEC VIN = 2VRMS

PC HP = 3.6 HZ

FC LP = 43KHZ

VIN = 2VRMS, CODEC VIN = 1.14 VRMS

AUDIO: LINE INPUT FILTER

MIN_NECK_WIDTH=.1MM
MIN_LINE_WIDTH=.1MM
System Agent Power Supply

6A Max Output
f = 300 kHz

---

OUT
IN
FB
EN
PVCC
VCC
SREF
VO
OCSET
PGOOD
FSEL
RTN
PHASE
LGATE
UGATE
BOOT
PGND
GND
SET0
SET1
VID0
VID1

---

SYNC_DATE=08/19/2010
SYNC_MASTER=JACK_K90I

---

System Agent Supply

---

PPBUS_S5_HS_COMPUTING_ISNS
CPU_VCCSASENSE
DIDT=TRUE
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
VCCSAS0_LL
SWITCH_NODE=TRUE
DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VCCSAS0_DRVH
DIDT=TRUE
GATE_NODE=TRUE
DIDT=TRUE
PVCCSA_EN
VCCSAS0_FB
VCCSAS0_CS_N
VCCSAS0_CS_P
VCCSAS0_BOOT_RC
DIDT=TRUE
PPVCCSA_S0_REG_R
PPVCCSA_S0_CPU
VCCSAS0_SET0
VCCSAS0_SET1
VCCSAS0_VBST
VOLTAGE=1.05V
PP5V_S0
PVCCSA_PGOOD
VCCSAS0_OCSET
VCCSAS0_VO
VCCSAS0_SREF
VOLTAGE=5V
Need symbol to be re-drawn to clean up this page.
CPU VCCIO (1.05V S0) Regulator

Vout = 0.5V * (1 + Ra / Rb)

OCP = 22.695A

OCP = R7641 x 8.5uA / R7640

Vout = 0.5V * (1 + Ra / Rb)
FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY.
Some signals require 27.4-ohm single-ended impedance.

Most CPU signals with impedance requirements are 50-ohm single-ended.

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.
**Memory Bus Constraints**

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<thead>
<tr>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
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<tbody>
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<tr>
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<td>MEM_50S</td>
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<td>MEM_72D</td>
<td>MEM_40S</td>
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<td>MEM_37S</td>
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<tr>
<td>MEM_CTRL2MEM</td>
<td>MEM_CLK2MEM</td>
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<tr>
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**Memory Net Properties**

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**Memory Bus Spacing Group Assignments**

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**DDR3**

Memory Bus Spacing Group Assignments

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**Memory Net Properties**

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**Memory Constraints**

- DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
- CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
- DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

---

*Source: Apple Inc.*
Digital Video Signal Constraints

- DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

Digital Video Signal Constraints

- SATA_ICOMP
- SATA_90D
- LVDS

Table Spacing Rule Set

- ALLOW ROUTE = 90_OHM_DIFF
- 8_MIL = 85_OHM_DIFF

Table Spacing Rule Item

- MAXIMUM NECK LENGTH = 100_OHM_DIFF
- TOP, BOTTOM
- MAXIMUM NECK LENGTH
- LINE-TO-LINE SPACING = 3x_DIELECTRIC

Electrical Constraint Set

- I217
- I214
- PCH_CLK100M_SATA_N
- PCH_CLK100M_PCH_N
- USB_BRCRYPT_N
- USB_IR_P
- USB_CAMERA
- USB_CAMERA_N
- T29_A_RSVD_N
- USB_T29A_N
- USB_EXTB_N
- PCH_SATAICOMP
- SATA_HDD_D2R_RC_P
- SATA_ODD_D2R_P
- SATA_HDD_D2R_C_N
- SATA_HDD_D2R_P
- SATA_HDD_R2D_N
- NC_LVDS_IG_A_DATAN<3>
DisplayPort Signal Constraints

NOTE: DisplayPort physical/spacing constraints provided by chipset or GPU page.

T29 DP Connector Signal Constraints

PHYSICAL_RULE_SET

ELECTRICAL_CONSTRAINT_SET

SPACING_RULE_SET

T29/DP Net Properties

T29/IC Net Properties

T29/DP Net Properties

T29/IC Net Properties

T29 Constraints

www.vinafix.vn
<table>
<thead>
<tr>
<th>NET_TYPE</th>
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**SMC SMBus Net Properties**

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**SMC SMBus Charger Net Properties**

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**BGA**

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**DIFFPAIR PRIMARY GAP**

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**DIFFPAIR NECK GAP**

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**NOTE:** 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

**NOTE:** 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.