A standby circuit

The Apple power interface circuit principle J6900 Apple A1286 motherboard power connector, and a total of five pin. 1.2 feet to the adapter main power supply input; 3.4 foot as ground; 5 foot 1-wire signal line. U6900, the output signal of the 1-wire signal line overvoltage protector SYS ONEWIRE signal motherboard communications;

PPDCIN_G3H Input, after isolation MOS tube Q7080 internal body diode, the output PPDCIN_G3H_OR_PBUS;

Reverse-Current Protection

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085.
* Charges TOP FEED and Q7055.
PPDCIN_G3H_OR_PBUS Powered for U6990, U6990 output

Working Principle: input pin input voltage detection end, the inner part of the pressure, compared with Vref, electricity Pressure is normal, 1 foot high, 1 foot output low voltage is lower than the standard output. Then the application Role here is detection of PP3V42_G3H, when PP3V42_G3H voltage compliant After, U5000 to output high SMC_RESET_L to the EC. PP3V42_G3H ceded another road, powered to the U5020, U5020 output PP3V3_S5_AVREF_SMC_EC

NCP303LSNxxT1
Open Drain Output Configuration
PP3V42_G3H Voltage output, after the U5000 to detect, U5000 is a high-precision under voltage seized Measured, the internal principles are as follows:

PP3V42_G3H Ceded to provide power supply for the EC:
Apple A1286 notebook RTC battery does not exist. RTC power supply is directly PP3V42_G3H provide: Except:

In addition, PP3V42_G3H will also for the many signal provided on the pull
Two charge-discharge circuit

Apple machines, which the public side of the power supply is by the charge and discharge management chip in turn control MOS tube buck Change from, unlike the common notebook computer architecture (directly from the adapter output). So, Apple If the circuit which charge and discharge circuit using an adapter worked. A1286 them, the charge and discharge chip Model ISL6259 chip , itself several the the common 1 chip main power supply input , After two adapter voltage diode Input to the chip's 2 feet
DC-IN
Chip power supply input, there will be VDD voltage output available to chip peripheral circuitry required To;

2 adapter voltage detection, 3 feet ACIN Here is to design from the adapter input terminal connected to the partial pressure of the two resistors in series, to serve Chip ACIN provides a high level detection signal
3 when the voltage required, the output of the chips will ACOK signal.

Signal to the SMC_BC_ACOK signal sent to the EC, EC received, issued SMC_ADAPTER_EN PCH, notification the PCH now has access to the adapter: With
The protection of isolated two P-channel MOS transistor open:

To the back output PPDCIN_G3H_INRUSH voltage. Chip of 12 feet is a power supply input for internal the SM management module powered, 12-foot SM mode A reset signal of the block is the normal working hours, but also for high-level signal input:
Chip open the Q7080 and Q7085, the adapter output voltage to the back of the circuit,

After R7020 precision sampling resistor, the input to the high-end gate FET Q7030 D pole. In normal post-stage circuit, chip functional case, the chip will issue a square-wave driver for driving the two MOS transistor in turn turned to the back output voltage: PPBUS_G3H,
In Chip after chip internal two sets of current detection module, a detection adapter input The magnitude of the current, the output signal AMON feedback to the EC, the other is the size of the charging current is detected, the output Signal BMON feedback to the EC. And the charging and discharging of the battery, by the Q7055 control.
First to be a summary, Apple A1286 power-on timing, if the contents of the above to make a classification and scheduling Order, you can learn a rough picture of the following:

Namely: the first step is a standby circuit, the second step is a charge-discharge circuit, the third step, it is Next, we have to analyze the system power supply 3.3V and 5V power supply circuit. A1286 circuit, 3.3V and 5V control chip Model TPS51125, this chip in its His notebook which encountered more separate, and our extraordinary repair Forum Principles of analysis, we do not detail decomposed. Only said probably work order: 1 First, public-side power input:
Divided into a three-way, two-way FET power supply to the high-end door, another way for the chip to provide the main power supply input Into. 2 Next, open chip linear voltage signal: SMC_PM_G2_EN, sent to the chip 13 feet EN0, the description of this signal in the data sheet is grounded, the chip close linear voltage output Out resistance left floating or connected to GND, open linear output. 3

3 EC are powered, the output signal: SMC_PM_G2_EN chip 8-pin 17-pin output linear electrical Pressure:
To close both MOS tube, it requires the input of the corresponding turn-on signals, wherein, P3V3S5_EN letter Number is issued by the EC in standby:

Turn signals P5VS3_EN PCH trigger signal, issued SLP_S4 # signal RC delay Change:
So, Apple A1286 notebook in standby, 3.3V inductance 3.3V voltage; While the the 5V inductor standby voltage is 0V. In PP3V3_S5 voltage generated U7940 be PP3V3_S5 voltage detection voltage in line Requirements, and outputs a high level signal: RSMRST_PWRGD RSMRST_.
Four power-on trigger

The A1286 boot keys is connected to the keyboard, so through a keyboard interface to communicate with the motherboard is even Pick communication.

Boot the keyboard interface pin5 output trigger signal connected to R5710, Output signal SMC_ONOFF_L, hair High-low-high transition signals to the EC:

NOTE: P94 and P95 are short
EC after receiving the trigger signal, issued PWRBTN_L:

Sent to PCH PWRBTN # signal

*** Above picture is worth noting the signal: PM_BATLOW_L this signal to boot, must Is high, and this signal is EC issued directly. EC detection battery power issue This signal. If the battery is not sufficient to maintain the system starts, this signal will be EC drive Is low and the PCH is not triggered.
*** PCH received PWRBTN # signal, issued SLP_S3, #, SLP_S4 # signal (SLP_S5 # signal is used, SLP_S5 # signal when using the state of the battery, PCH is not received SMC_ADAPTER_EN Low, EC will not to issue P3V3_S5_EN to power the system, played standby to reduce battery power loss Consumption. After pressing the start button, pulled SLP_S5 #, SLP_S4 #, SLP_S3 #)

SLP_S4 # signal to open the memory supply, SLP_S3 # signal to open in addition to the memory power supply and CPU Powered groups supply. First we look at PM_SLP_S4_L signal control circuit:
The figure above the PM_SLP_S4_L signal open the power supply of the USB port.

PM_SLP_S4_L Signal returned to the EC.
PM_SLP_S4_L signal is connected to a pulldown resistor R5094, so that when the signal is not sent, the signal at At the low level state.

PM_SLP_S4_L signal conduction Q7812, pulled down Q7810G pole, Q7810 conduction to produce PP3V3_S3
PM_SLP_S4_L Signal after RC delay, generate signals: P5VS3_EN, DDRREG_EN. P5VS3_EN signal open the 5V voltage:

DDRREG_EN Open the memory 1.5V power supply

c7360, c7361 close to memory
PM_SLP_S3_L signal is issued, mainly to control the brightest

In this circuit, the PM_SLP_S3_L signal high conduction below the Q3205 above Q3205 (Q3205 packaged together by two NMOS)

1.5V S3/S0 FET
And MEMVTEN Signal is PM_SLP_S3_L Pulled, open PP0V75_S0_DDRVT2:

PM_SLP_S3_L Signal is issued, must be returned to the EC
PM_SLP_S3_L_R (PM_SLP_S3_L signal after resistance after conversion from) signal conduction following Q5315, the above Q5315G pole pulled down, PPBUS_G3H voltage after Q5315 (above) backwards. The surface output through a resistor in series partial pressure voltage detection signals to produce SMC_PBUS_VSENSE distributed EC.

PM_SLP_S3_L_R The signal conduction Q7812, Q7830 the conduction, PP3V3_S5 to the back output PP3V3_S0: PM_SLP_S3_L_R signal open PP5V_S0

3.3V S0 FET
PM_SLP_S3_L_R signal open PP5V_S0

PM_SLP_S3_L_R Signal to open the NIC
The signal of PM_SLP_S3_L open the J9400 port 5V powered:

Port Power Switch

In the above voltage generator, there will be a few road voltage the distributed switching control signal chip (GMUX) U9600:
U9600 Issue of graphics power (NV independence was powered chip) open letter EG_RAIL1_EN, EG_RAIL2_EN, EG_RAIL3_EN, EG_RAIL4_EN:
Respectively, open the brightest powered graphics chip needs:
Among them, EG_RAIL3_EN signal to the U8900, open graphics core power supply.

iN EN_RAIL Control of the brightest of these signals normally generated by the power supply, there will be corresponding power good letter The number PM_ALL_GPU_PGOOD output, including all the way back to the U9600 Hair.
Distributed to Q7995, to pull down CK505_27MHZ_EN_L signal sent to the clock chip, open graphics clock. The next action, that is, after each power good signal generator will go through U7980, power good signal:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP_SMC_EXCARD_PWR_EN</td>
<td>P12, P10</td>
</tr>
<tr>
<td>TP_SMC_RSTGATE_L</td>
<td>P11, P11</td>
</tr>
<tr>
<td>ALL_SYS_PWRGD</td>
<td>P12, P12</td>
</tr>
<tr>
<td>BSMRST_PWRGD</td>
<td>P13, P13</td>
</tr>
<tr>
<td>PM_BSMRST_L</td>
<td>P14</td>
</tr>
<tr>
<td>CPUIMVP_VR_ON</td>
<td>P15</td>
</tr>
<tr>
<td>PM_PWRTTN_L</td>
<td>P16</td>
</tr>
<tr>
<td>NC_ESTABLDO_EN</td>
<td>P17</td>
</tr>
<tr>
<td>TP_SMC_P24</td>
<td>P20, P21, P22, P23</td>
</tr>
</tbody>
</table>

U4900 After to get ALL_SYS_PWRGD signal, issued IMVP_VR_ON, open the CPU core power supply:
CPU core power supply generates a normal issue high level source: CPUIMVP_PGOOD:

Two high-level input signal with gate U2850 issued PM_PCH_PWRGD, issue PCH:
CPU power supply is normal, issued another signal, the low level of the clock enabled signal: CPUIMVP_CLK_EN_L, distributed clock chip:

CPU clock signal, issued by the CPU internal graphics module powered open Signal GFX_VR_EN:
Distributed to chip the U7500, chip get open signal, through the VID identification signal to communicate with the CPU, was Take the voltage information needed by the CPU:

The issue of a corresponding voltage. PCH in get above the power good signal will be issued reset signal PLT_RESET_L, reset each Equipment: