### BOM Variants (continued on CSA 6)

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### Part Numbers
- PCBA, 2.7G, 16G_HYN, VRAM_SAM, MLB_KEPLER, D2, DYW5
- PCBA, 2.6G, 8G_HYN, VRAM_SAM, MLB_KEPLER, D2, DRF4

### Module Parts

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### Programmables

- BASE_BOM, CPU_IVY: 2.3GHZ, FB_2G_SAMSUNG, EEEE:DY3W, DEVEL_BOM, RAM_2G_HYNIX_1600
- CRITICAL

### DRAM VREF Configs
- DRAM VREF: VREF=VCC_H, VREF=L, VREF=L, VREF=L

### DRAM SPD Straps

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### DEVELOPMENT/BASE BOM

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### Supplemental Information

- Panasonic alt to TDK
- Cyntec alt to Vishay
- Pericom eDP MUX

---

[www.vinafix.vn](http://www.vinafix.vn)
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*Note: All parts are critical.*

**Keeping for PRQ**

**Elipda DQ'd**

---

**BOM Variants (continued from CSA 5)**

**Bar Code Labels / EEEE #’s (continued from CSA 5)**
This connection is to support the same.

Intel is investigating processor driven VREF_DQ generation.
**VAXG DECOUPLING**

- Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
- Apple implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

**PLACEMENT_NOTE (C1734-C1735):**
- Place near inductors on bottom side.

**PLACEMENT_NOTE (C1726-C1731):**
- Place close to U1000 on bottom side

**PLACEMENT_NOTE (C1758-C1762):**
- CPU VCCSA DECOUPLING
- Local recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
- Apple implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

**CPU VCCSA DECOUPLING**

- Local recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
- Apple implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.

Note: TDO from CR is Push-Pull CMOS
PCH SIGNALS

XDP SIGNALS

PCB/SPP Signal Isolation Notes:
- Initially, stuff both 33 and 0 ohms and validate whether it is functional in that state, mix and match options.
- *Input* non-XDP signals require pull.
- *Output* PC/SPP signals require pull.

R2527, R253, R259s and R259s should be placed where signal path needs to switch between route from PCH to 2527S and path to non-XDP signal destination.

CPU Micro2-XDP

NOTE: This is not the standard XDP plane. Use with 921-0132 Adapter Flex to support optional debug.

CPU & PCH XDP
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISO|ATE_CPU_MEM L GPIO state during S3<->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE USE</th>
<th>CRITICAL</th>
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</table>

1V5 S0 "PGOOD" for CPU

MEMVTT Clamp
Ensures CKE signals are held low in S3

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.
NOTE: Must not enable more than two SO-DIMM margining buffers at once or Vref source may be overloaded.

Power alias required by this page:
- VREFCA_LDO_DAC
- VREFDQ_LDO_DAC
- VREFDQ_M1_DAC

Signal aliases required by this page:
- =PPDDR_S3_MEMVREF
- =PPVTT_S3_DDR_BUF
- =PP3V3_S3_VREFMRGN

NOTE: CPU DAC output step sizes:
- 7.69mV / step @ output
- +3.4mA - -3.4mA (- = sourced)
- 0.000V - 1.501V (0x00 - 0x74)
- 0.300V - 1.200V (+/- 450mV)
- 0.75V (DAC: 0x3A)

VREFCA:LDO_DAC
VREFDQ:LDO_DAC
VREFDQ:M1_M3
VREFDQ:M1_DAC

BI
IN
IN
IN

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0.75V
VOLTAGE=0.75V

RES,MTL FILM,332,1%,0402,SM,LF
RES,MTL FILM,0,5%,0402,SM,LF

CRITICAL
CRITICAL

NOTE: CPU DAC output step sizes:
- 7.69mV / step @ output
- +3.4mA - -3.4mA (- = sourced)
- 0.000V - 1.501V (0x00 - 0x74)
- 0.300V - 1.200V (+/- 450mV)
- 0.75V (DAC: 0x3A)

VREFCA:LDO_DAC
VREFDQ:LDO_DAC
VREFDQ:M1_M3
VREFDQ:M1_DAC

BI
IN
IN
IN

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0.75V
VOLTAGE=0.75V

RES,MTL FILM,332,1%,0402,SM,LF
RES,MTL FILM,0,5%,0402,SM,LF

CRITICAL
CRITICAL

NOTE: CPU DAC output step sizes:
- 7.69mV / step @ output
- +3.4mA - -3.4mA (- = sourced)
- 0.000V - 1.501V (0x00 - 0x74)
- 0.300V - 1.200V (+/- 450mV)
- 0.75V (DAC: 0x3A)

VREFCA:LDO_DAC
VREFDQ:LDO_DAC
VREFDQ:M1_M3
VREFDQ:M1_DAC

BI
IN
IN
IN

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0.75V
VOLTAGE=0.75V

RES,MTL FILM,332,1%,0402,SM,LF
RES,MTL FILM,0,5%,0402,SM,LF

CRITICAL
CRITICAL

NOTE: CPU DAC output step sizes:
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- 0.75V (DAC: 0x3A)

VREFCA:LDO_DAC
VREFDQ:LDO_DAC
VREFDQ:M1_M3
VREFDQ:M1_DAC

BI
IN
IN
IN

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0.75V
VOLTAGE=0.75V

RES,MTL FILM,332,1%,0402,SM,LF
RES,MTL FILM,0,5%,0402,SM,LF

CRITICAL
CRITICAL

NOTE: CPU DAC output step sizes:
- 7.69mV / step @ output
- +3.4mA - -3.4mA (- = sourced)
- 0.000V - 1.501V (0x00 - 0x74)
- 0.300V - 1.200V (+/- 450mV)
- 0.75V (DAC: 0x3A)

VREFCA:LDO_DAC
VREFDQ:LDO_DAC
VREFDQ:M1_M3
VREFDQ:M1_DAC

BI
IN
IN
IN

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0.75V
VOLTAGE=0.75V

RES,MTL FILM,332,1%,0402,SM,LF
RES,MTL FILM,0,5%,0402,SM,LF

CRITICAL
CRITICAL

NOTE: CPU DAC output step sizes:
- 7.69mV / step @ output
- +3.4mA - -3.4mA (- = sourced)
- 0.000V - 1.501V (0x00 - 0x74)
- 0.300V - 1.200V (+/- 450mV)
- 0.75V (DAC: 0x3A)

VREFCA:LDO_DAC
VREFDQ:LDO_DAC
VREFDQ:M1_M3
VREFDQ:M1_DAC

BI
IN
IN
IN

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0.75V
VOLTAGE=0.75V

RES,MTL FILM,332,1%,0402,SM,LF
RES,MTL FILM,0,5%,0402,SM,LF

CRITICAL
CRITICAL

NOTE: CPU DAC output step sizes:
- 7.69mV / step @ output
- +3.4mA - -3.4mA (- = sourced)
- 0.000V - 1.501V (0x00 - 0x74)
- 0.300V - 1.200V (+/- 450mV)
- 0.75V (DAC: 0x3A)
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
Note: All labels have "SMC," name. Unused pins designed as outputs can be left floating.
Unused pins designated as inputs require pull-ups.
Keyboard Backlight Driver & Detection

To detect keyboard backlight, one will

1. Assert and read SMC_SYS_KBDLED
2. IF HIGH, keyboard backlight not present
3. IF LOW, keyboard backlight present

To detect Keyboard backlight, SMC will

1. Read SMC_SYS_KBDLED
2. IF HIGH, keyboard backlight present
3. IF LOW, keyboard backlight not present
NOTE: If HOLD* is asserted, ROM will ignore SPI cycles.

SPI ROM

SPIROM_USE_MLB = PP3V3_SUS_ROM
SPI_MLB_MOSI
SPI_MLB_CS_L
SPI_WP_L
SPI_MLB_MISO
SPI_MLB_CLK

ROM will ignore SPI cycles.
### 1.8V S0 Regulator

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESC</th>
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**Expression:**

\[
V_{out} = 0.8V \times (1 + \frac{R_a}{R_b})
\]

### 1.05V SUS LDO

- Max Current = 4A
- Freq = 1 MHz

### 1.5V S0 Regulator

**Expression:**

\[
V_{out} = 0.8V \times (1 + \frac{R_a}{R_b})
\]

### 1.5V S0 LDO (RIO)

**Expression:**

\[
V_{out} = 0.8V \times (1 + \frac{R_a}{R_b})
\]

---

**Notes:**

- 1.5V S0 LDO (RIO) uses dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.
- Over 1.5V to compensate for flex loss.
- Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
- 70mA is required to support pull-ups. Alternative is strong voltage.
- Max Current = 0.5A

---

**Other Details:**

- **Part Number:** U7720
- **Description:** 1.05V SUS LDO
- **Reference:** C7741
- **Value:** 1UF
- **Voltage:** 6.3V
- **Tolerance:** 10%
- **QTY:** 2

---

**Misc Power Supplies**

Apple Inc. 051-9589 4.18.0

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---

**Reference:**

- **U7720**
- **MFG:** U7720
- **Vout:** 1.05V
- **THRM:** 0201-MUR
- **1.0UF**
- **6.3V**
- **MF-LF X5R 20%**
- **PART NUMBER:** 0201-MUR
- **DESCRIPTION:** 1.0UF
- **VOLTAGE:** 6.3V
- **TOLERANCE:** 10%
- **QTY:** 2

---

**General Notes:**

- **MIN LINE WIDTH:** 0.2 mm
- **MIN LINE WIDTH:** 0.6 mm
- **VOLTAGE:** 1.8V
- **MIN LINE WIDTH:** 0.4 mm

---

**References:**

- **1.8V S0 Regulator**
- **1.05V SUS LDO**
- **1.5V S0 Regulator**
- **1.5V S0 LDO (RIO)**
- **Misc Power Supplies**

---

**Additional Information:**

- **Figure:** PP1V8_S0_P1V5_LDO
- **Reference:** C7724
- **Value:** 1000PF
- **Voltage:** 70
- **NP0-C0G**

---

**Contact:**

www.vinafix.vn
3.3V/HV Power MUX

For 12V systems:

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<th>QTN</th>
<th>DESCRIPTION</th>
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Thunderbolt Connector B

- TBT: TX_1 (0-18.9V)
- TBT: TX_2 (0-18.9V)
- TBT: TX_3 (0-18.9V)
- TBT: TX_4 (0-18.9V)
- TBT: RX_1 (0-18.9V)
- TBT: RX_2 (0-18.9V)
- TBT: RX_3 (0-18.9V)
- TBT: RX_4 (0-18.9V)

4.16.0

051-5680 0

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CPU Rail Sequencing

Note: 1V8 may not be required for Kepler if there is no LVDS.

Power Sequencing EG/PCH S0

Place R9910 - R9917 close to U8000.
Place R9920 - R9927 close to U1000.

PCIE Test Structures (For Lab Use)

PEG_R2D_P<0> = P3V3GPU_MISC_EN
PEG_R2D_P<4> = P1V35FB_EN
PEG_R2D_P<7> = P3V3GPU_EN

PEG_D2R_P<0> = EG_RAIL1_EN
PEG_D2R_P<4> = EG_RAIL3_EN
PEG_D2R_P<7> = EG_RAIL5_EN
PEG_D2R_P<7> = P1V5S3RS0_RAMP_DONE
PEG_D2R_N<0> = TP_DDRREG_PGOOD
PEG_D2R_N<4> = TP_P1V5S3RS0_RAMP_DONE
PEG_D2R_N<7> = MAKE_BASE=TRUE

GPU_VCORE_EN = P1V05_GPU_EN
GPU_FB_PGOOD = P1V05_S0GPU_PGOOD
GPU_PGOOD3 = PP1V8_GPU_FET
GPU_PGOOD1 = PP3V3_S0_PWRCTL
GPU_PGOOD2 = PM_ALL_GPU_PGOOD
GPU_PGOOD4 = CPUIMVP_AXG_PGOOD

Note: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.
Some signals require 27.4-ohm single-ended impedance. Most CPU signals with impedance requirements are 50-ohm single-ended.
## Memory Bus Constraints

**MEM_DATA2DATA**
- DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

### DDR3 (Memory Down):
- **MEM_DATA2MEM**
- **MEM_CMD2MEM**
- **MEM_CMD2CMD**
- **MEM_CLK2MEM**
- **MEM_2OTHER**

### Memory Net Properties

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<tr>
<th>Layer</th>
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<td>LAYER</td>
<td>50_OHM_SE</td>
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<tr>
<td>LAYER</td>
<td>40_OHM_SE</td>
<td>25 MILS</td>
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### Memory Bus Spacing Group Assignments

**MEM_DATA2DATA**
- **MEM_DQS**
- **MEM_85D**
- **MEM_50S**
- **MEM_40S**

**MEM_37S**
- **MEM_DATA2DATA**

## DDR3 (Memory Down):
- DQ signals should be matched within 5.68m of associated DQS pair.
- DQS inter-pair matching should be within 7.12m, no inter-pair matching required.
- DQS to clock matching should be within 1.83m.
- Clock inter-pair matching should be within 5.68m.
- A/SP/CE signals should be matched within 4.58m.

### Memory Constraints

**SYNC_DATE=01/13/2012**

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### Physical Rule Set

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#### USB 2.0 Interface Constraints

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#### SATA Interface Constraints

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#### Digital Video Signal Constraints

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#### System Clock Signal Constraints

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**NOTE:** 25MHz system clocks very sensitive to noise.

### Spacing Rule Set

#### Clock Net Properties

**NOTE:** 25MHz system clocks very sensitive to noise.

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<tr>
<td>CR SFF Platform Design Guide V0.7, Table 4-211, 1X1</td>
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<tr>
<td>Layer</td>
<td>Min Width</td>
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<td>-----------</td>
</tr>
<tr>
<td>SMBUS_SMC_3_SDA</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_3_SCL</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_5_SDA</td>
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<td>SMBUS_SMC_5_SCL</td>
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</tr>
<tr>
<td>SMBUS_SMC_1_S0_SDA</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_1_S0_SCL</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_2_S3_SDA</td>
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<td>SMBUS_SMC_2_S3_SCL</td>
<td>0.1 MM</td>
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<tr>
<td>SMBUS_SMC_0_S0_SDA</td>
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</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>0.1 MM</td>
</tr>
</tbody>
</table>

**SMBus Charger Net Properties**

- **CHGR_CSI_P**
- **CHGR_CSI_N**
- **CHGR_CSO_P**
- **CHGR_CSO_N**
**Physical Rule Set**

- **GDDR5_45SE**
- **GDDR5_EDC**
- **HDMI_90D**
- **DP_85D**

**Line-to-line Spacing**
- **8x**
- **5x Dielectric**

**Weight**
- **45_OHM_SE**
- **90_OHM_DIFF**

**Maximum Neck Length**
- **80_OHM_DIFF**
- **90_OHM_DIFF**

**Minimum Neck Width**
- **80_OHM_DIFF**

**Spacing Rule Set**
- **GDDR5_EDC**
- **HDMI**

**Layer**
- **LAYER**
- **LAYER**

**Table Spacing Rule Item**

**Electrical Constraint Set**

**Digital Video Signal Constraints**

**Electrical Constraint Item**

**GDDR5 Frame Buffer Signal Constraints**

**Table Physical Rule Item**

**Sheet**

**Drawing Number**

**Size**

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### Memory Constraint Relaxations

Additional diffpair width/gap through BGA fanout areas (95-ohm diff)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Area Type</th>
<th>Diffpair</th>
<th>Neck Width</th>
<th>Gap Width</th>
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<td>BGA</td>
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### Project Specific Constraints

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