### Schematic / PCB #s

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### Alphas

#### SCHEM,MLB,M82

**Title:** SCHEM,MLB,M82  
**Date:** 11/14/2007

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**Acoustic Cap BOM Config Tables**

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<th>ICT_TEST</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>051-7230</td>
<td>ICT Test Points</td>
</tr>
</tbody>
</table>
**Functional Test Points**

**NB NO_TESTS**

- Functional Test and No-Tests
- Image of a block diagram with various test points labeled.

**Power Supply NO_TESTS**

- No Tests

**CLOCK NO_TESTS**

- No Tests

**LVDS NO_TESTS**

- No Tests

**REQUIRED NETS**

**NICE2HAVE NETS**

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**VIEW NO TESTS**

- True

**GET 1 OF 1**

- True

**GET 1 OF 1**

- True

**GET 1 OF 1**

- True
Mini-XDP Connector

**NOTES:** This is not the standard XDP pinout. Use with 920-0451 adapter board to support CPU, NB & SB debugging.

**NOTE:** This is not the standard XDP pinout.

Please avoid any obstructions.

---

**Direction of XDP module to edge of board**

These avoid any obstructions.

---

**Mini-XDP Connector**

**NOTES:** This is not the standard XDP pinout. Use with 920-0451 adapter board to support CPU, NB & SB debugging.

**NOTE:** This is not the standard XDP pinout.

Please avoid any obstructions.

---

**Direction of XDP module to edge of board**

These avoid any obstructions.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
TV_DCONSEL<0> to GND.
Follow instructions for LVDS and CRT & TV-Out Disable above.

NOTE: Must keep VDDC_TVDAC powered
VCCD_CRT, VCCD_QDAC and VCC_SYNC.

CRT & TV-Out Disable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.

TVDAC rails.  VCCA_TVx_DAC and VCCA_DAC_BG can
omit filtering components.  Unused DAC outputs
must remain powered, but can
Component: DACA, DACB & DACC
S-Video:   DACB & DACC only

LVDS Disable

Tie VCC_TX_LVDS and VCCA_LVDS to GND.

LVDS Disable / CRT Enable

Internal Graphics Signals

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Use only the parts recommended, except those noted above.
Follow instructions for LVDS and CRT & TV-Out Disable above.
Follow instructions for LVDS and CRT & TV-Out Disable above.
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omit filtering components.  Unused DAC outputs
must remain powered, but can
Component: DACA, DACB & DACC
S-Video:   DACB & DACC only

LVDS Disable

Tie VCC_TX_LVDS and VCCA_LVDS to GND.
Current numbers from Crestline EDS, doc #21749.

NB_VCCSM_LF7  NB_VCCSM_LF4  NB_VCCSM_LF2  NB_VCCSM_LF1

C1807  0.1UF  6.3V  X5R  10%  2
C1806  0.1UF  6.3V  X5R  2
C1805       X5R  20%  2
C1804  0.22UF  6.3V  X5R  CERM-X5R

76  C1802  16  5 mA (standby)  1700 mA (1 ch, 667MHz)  2700 mA (2 ch, 533MHz)

51  35  10%  21  32  18  31  14  21

5 mA (standby)  1700 mA (1 ch, 667MHz)  2700 mA (2 ch, 533MHz)

AW38  AW36  BL29  BK30  BJ29  BG29  BF30  BF28  BE31  BD28  BC31  BC29  BC27  BB32  BB30  BB28  BA31  BA29  BA27

NB Power 1

POER (TYP W)
U1400

100 mA (200 MHz)

PP1V05_S0

These connections can break without impacting part performance.

NCTF balls are Not Critical To Function
These connections can break without impacting part performance.

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SYNC_DATE=01/09/2007
Current numbers from Crestline EDS, doc #21749.

| Power | ALL | 87 | 76 | 28 | 28 | 150 mA | 250 mA | 100 mA | 0.4 mA | 100 mA | 27 | 60 mA | 60 mA | 40 mA | 40 mA | 40 mA | 10 mA | 50 mA | 5 mA | 35 mA |
|-------|-----|----|----|----|----|--------|--------|--------|--------|--------|-----|-------|-------|-------|-------|-------|-------|------|------|-----|------|
|       |     |    |    |    |    |        |        |        |        |        |     |       |       |       |       |       |       |      |      |     |      |
Platform Reset Connections

Unbuffered

Buffered

This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Place R2898 pads on bottom side near board edge

Silk: "SYS RST"

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### Clock Termination

**CPU Clocks**
- **CPU Clocks**
  - **CPU Host Clock (123/167MHz)**
  - **CPU Host Clock (222/293MHz)**
  - **CPU Host Clock (333/444MHz)**
- **CPU Port Clocks**
  - **CPU Port Clock (123/167MHz)**
  - **CPU Port Clock (222/293MHz)**
  - **CPU Port Clock (333/444MHz)**
- **CPU Internal Clocks**
  - **CPU Internal Clock (123/167MHz)**
  - **CPU Internal Clock (222/293MHz)**
  - **CPU Internal Clock (333/444MHz)**

**PLL Clocks**
- **PLL Clocks**
  - **PLL Clock (123/167MHz)**
  - **PLL Clock (222/293MHz)**
  - **PLL Clock (333/444MHz)**

**PCIE Clocks**
- **PCIE Clock (100MHz)**
  - **PCIE Clock (100MHz)**
  - **PCIE Clock (100MHz)**
  - **PCIE Clock (100MHz)**

**PCI Clocks**
- **PCI Clock (33MHz)**
  - **PCI Clock (33MHz)**
  - **PCI Clock (33MHz)**
  - **PCI Clock (33MHz)**

**Port Clocks**
- **Port Clocks**
  - **Port Clock (33MHz)**
  - **Port Clock (33MHz)**
  - **Port Clock (33MHz)**
  - **Port Clock (33MHz)**

**SMC Clocks**
- **SMC Clocks**
  - **SMC Clock (33MHz)**
  - **SMC Clock (33MHz)**
  - **SMC Clock (33MHz)**
  - **SMC Clock (33MHz)**

**Miscellaneous Clocks**
- **Miscellaneous Clocks**
  - **Miscellaneous Clock (33MHz)**
  - **Miscellaneous Clock (33MHz)**
  - **Miscellaneous Clock (33MHz)**
  - **Miscellaneous Clock (33MHz)**

---

### CPU Speed

**CPU Speed**
- **CPU Speed**
  - **CPU Speed**
  - **CPU Speed**
  - **CPU Speed**

**CPU Clock Settings**
- **CPU Clock Settings**
  - **CPU Clock Settings**
  - **CPU Clock Settings**
  - **CPU Clock Settings**

**CPU Speed**
- **CPU Speed**
  - **CPU Speed**
  - **CPU Speed**
  - **CPU Speed**

---

### PLL Clocks

**PLL Clocks**
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  - **PLL Clock**
  - **PLL Clock**
  - **PLL Clock**

---

### PCIE Clocks

**PCIE Clocks**
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  - **PCIE Clock**

---

### PCI Clocks

**PCI Clocks**
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  - **PCI Clock**
  - **PCI Clock**
  - **PCI Clock**

---

### Port Clocks

**Port Clocks**
- **Port Clocks**
  - **Port Clock**
  - **Port Clock**
  - **Port Clock**

---

### SMC Clocks

**SMC Clocks**
- **SMC Clocks**
  - **SMC Clock**
  - **SMC Clock**
  - **SMC Clock**

---

### Miscellaneous Clocks

**Miscellaneous Clocks**
- **Miscellaneous Clocks**
  - **Miscellaneous Clock**
  - **Miscellaneous Clock**
  - **Miscellaneous Clock**

---

**CPU Speed Settings**
- **CPU Speed Settings**
  - **CPU Speed Settings**
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---

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MEM CLOCK TERMINATION

Place one resistor at each end of Y split

--- MEM_CLK_P<4> ---
R3390  320   0.1UF  6.3V  10%
X5R        201
--- MEM_CLK_N<4> ---
R3391  320   0.1UF  6.3V  10%
X5R        201
--- MEM_CLK_P<4> ---
R3392  320   0.1UF  6.3V  10%
X5R        201
--- MEM_CLK_N<1> ---
R3393  320   0.1UF  6.3V  10%
X5R        201
--- MEM_CLK_P<4> ---
R3394  320   0.1UF  6.3V  10%
X5R        201
--- MEM_CLK_N<0> ---
R3395  320   0.1UF  6.3V  10%
X5R        201

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPT shown at the top of each group applies to every part below it

Memory Active Termination

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051-7230

TO PP0V9_S0_MEM_TERM
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APPROXIMATE CAP ARRANGEMENT

TWO 0402 CAPS ALONG PACKAGE EDGE

THREE 0603 CAPS SPREAD TO COVER ALL 8 PARTS

COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

COLUMN OF THREE CAPS BETWEEN PACKAGES

COLUMN OF THREE CAPS BETWEEN PACKAGES
Micro DVI, USB, to RIO Hatch Assembly

Audio Connector

516S0632

516S0350
3.3V GPIO54 is 5V tolerant.

C4400

20%

6.3V

10UF

X5R

C4400

20%

6.3V

10UF

X5R

R4401

1/20W

201

4.7K

1%

MF

R4400

1/20W

201

10K

5%

MF

R4402

5%

201

MF

100K

5%

5

1/20W

U4400

SC70

MC74VHC1G09

J4400

F-ST-SM

CRITICAL

AXK740327G

PATA HDD CONNECTOR

IDE_PDD<11>

IDE_PDD<13>

IDE_PDD<15>

IDE_PDD<14>

IDE_PDD<12>

IDE_PDD<10>

IDE_PDD<9>

IDE_PDD<8>

IDE_PDD<7>

IDE_PDD<6>

IDE_PDD<5>

IDE_PDD<4>

IDE_PDD<3>

IDE_PDD<2>

IDE_PDD<1>

IDE_PDD<0>

IDE_PDIORDY

IDE_PDIOW_L

IDE_PDDACK_L

IDE_PDDREQ

IDE_PDA<0>

IDE_PDA<1>

IDE_PDA<2>

IDE_PDD<16>

IDE_PDD<15>

IDE_PDD<14>

IDE_PDD<13>

IDE_PDD<12>

IDE_PDD<11>

IDE_PDD<10>

IDE_PDD<9>

IDE_PDD<8>

IDE_PDD<7>

IDE_PDD<6>

IDE_PDD<5>

IDE_PDD<4>

IDE_PDD<3>

IDE_PDD<2>

IDE_PDD<1>

IDE_PDD<0>

IDE_PDIORDY

IDE_IRQ14

IDE_RESET_L

IDE_RESET_BUF_L

IDE_PDD<18>

IDE_PDD<17>

IDE_PDD<16>

IDE_PDD<15>

IDE_PDD<14>

IDE_PDD<13>

IDE_PDD<12>

IDE_PDD<11>

IDE_PDD<10>

IDE_PDD<9>

IDE_PDD<8>

IDE_PDD<7>

IDE_PDD<6>

IDE_PDD<5>

IDE_PDD<4>

IDE_PDD<3>

IDE_PDD<2>

IDE_PDD<1>

IDE_PDD<0>

IDE_PDIORDY

IDE_IRQ14

IDE_PDD<16>

IDE_PDD<15>

IDE_PDD<14>

IDE_PDD<13>

IDE_PDD<12>

IDE_PDD<11>

IDE_PDD<10>

IDE_PDD<9>

IDE_PDD<8>

IDE_PDD<7>

IDE_PDD<6>

IDE_PDD<5>

IDE_PDD<4>

IDE_PDD<3>

IDE_PDD<2>

IDE_PDD<1>

IDE_PDD<0>

IDE_PDIORDY

IDE_IRQ14
USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT

CURRENT LIMIT TO 1.5A CONTINUOUS

USB/SMC MUX

USB EXTERNAL CONNECTORS

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IPD Connector

Inverted to drive SMC_RESET logic

Power Button Inverter

Inverted to drive SMC_RESET logic

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pins designed as outputs can be left floating.
near board edge
Silk: "SMC RST"
Place R5001 on bottom side near board edge

g5013 will pull down SMC/manual reset in the event of a keyboard SMC reset generated when left shift, option, and control and the power button is depressed.

Debug Power Button
SMC Crystal Circuit
SMC AVREF Supply
3.3V TO PBUS LEVEL SHIFTING

SMC 3.3V to 1.05V Level Shifting
SMC 1.05V to 3.3V Level Shifting

Battery Pack Status

R5011 CLOSE TO SB

R5011 will pull down SMC/manual reset in the event of a keyboard SMC reset generated when left shift, option, and control and the power button is depressed.
LPC+SPI Connector

Place R5101 close to J5100

Place halfway between SPIROM and J5100

Place R5102 close to J5100

Place within 0.5" of SB

51600573

SPI_CS MUX

Place halfway between SPIROM and J5100

Place within 0.5" of SB

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REV. 1184

A

D

C

B

A

LPC+SPI Debug Connector

PP3V42_G3H

PP3V3_S5

PCI_CLK33M_LPCPLUS

LPC_AD<2>

LPC_AD<3>

BOOTROM_OVR_EN_L

LPC_AD<0>

LPC_AD<1>

SPI_EXT_A_SI_R

PM_CLKRUN_L

SPI_SO

LPC_FRAME_L

SMC_TMS

DEBUG_RESET_L

SMC_TDO

SMC_TRST_L

SMC_MD1

SMC_TX_L

72

72

60

59

57

44

49

36

28

27

26

25

24

23

22

21

20

19

18

17

16

15

14

13

12

11

10

6

5

4

3

2

1

SMC_RX_L

SMC_NMI

SMC_TCK

SMC_TDI

FRANKCARD_GPIO

SPI_INT_CE_L<0>

SPI_CE_L<0>

SPI_EXT_CE_L<0>

PP5V_S0

51600573

72

60

59

57

44

49

36

28

27

26

25

24

23

22

21

20

19

18

17

16

15

14

13

12

11

10

6

5

4

3

2

1

BOOTROM_OVR_EN_L

SPI_CE_R_L<1>

SPI_A_SI_R

72

60

59

57

44

49

36

28

27

26

25

24

23

22

21

20

19

18

17

16

15

14

13

12

11

10

6

5

4

3

2

1

AM Raspberry

R5152

NO STUFF

201

5%

MF

1/20W

R5151

LPCPLUS

201

5%

MF

1/20W

20K

R5101

LPCPLUS

201

5%

1/20W

201

47

C5150

LPCPLUS

201

0.1UF

6.3V

10%

X5R

R5150

LPCPLUS

201

0.1UF

6.3V

10%

X5R
ACIN VOLTAGE SENSE

MAX 16.5V + 10% ACIN = 3.0V SMCPBUS_VSENSE

R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

SMC ACIN VSENSE

R5300 12.7K 1%

C5300 0.22UF 10%

SMC_PBUS_VSENSE

R5301 12.7K 1%

C5310 0.22UF 10%

GPU VOLTAGE SENSE

NOMINAL 8.4V PBUS = 3.0V SMCPBUS_VSENSE

R5310 and R5311 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

SMC GPU VSENSE

R5310 4.53K 1%

C5310 0.22UF 10%

PPBUS_G3H

PPVCORE_S0_NB_GFX

SMC_ACIN_VSENSE

GND_SMC_AVSS

GND_SMC_AVSS

SMC_PBUS_VSENSE

GND_SMC_AVSS

SMC_GPU_VSENSE

PPVDCIN_G3H_PRE

PBUS VOLTAGE SENSE

NOMINAL 8.4V PBUS = 3.0V SMCPBUS_VSENSE

R5350 and R5351 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

SMC PBUS VSENSE

C5350 0.22UF 10%

R5351 201 6.98K 1%

SMC_PBUS_VSENSE

C5350 6.3V CERM-X5R 10%

R5350 12.7K 1%

C5300 0.22UF 10%

R5300 27.4K 201 1%

R5301 5.36K 201 1%

SYNC_DATE=01/09/2007

SYNC_MASTER=M70

Apple Inc.
REMOTE TEMP AT HEAT SPREADER

APN: 518S0354

CPU THERMAL DIODE

LOCAL TEMP NEAR POWER SUPPLIES

(Write: 0x9E Read: 0x9F)

(Write: 0x90 Read: 0x91)
Sudden Motion Sensor (SMS)

I2C addresses:
- ADDR low => 0x30, 0x31
- ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

APN: 338S0354

---

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051-7230
SPI ROM

note: mux for CE_L<0> on debug connector page.

SPI_SO also driven by debug card

There is an option to connect SPI_INT_CE_L<0> directly to SPI_CE_L<0>

R618x close to U6100

There is a 10K pullup on SPI_INT_CE_L<0> at the mux output.

SPI ROM
**1.8V/0.9V POWER SUPPLY**

<table>
<thead>
<tr>
<th>State</th>
<th>PM_S4_STATE_B</th>
<th>PM_SLP_S3</th>
<th>PP1V8_S3</th>
<th>PP0V9_S0</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>HIGH</td>
<td>HIGH</td>
<td>1.8V</td>
<td>0.9V</td>
</tr>
<tr>
<td>S3</td>
<td>HIGH</td>
<td>LOW</td>
<td>1.8V</td>
<td>0.9V</td>
</tr>
<tr>
<td>S5/G3Hot</td>
<td>LOW</td>
<td>LOW</td>
<td>0.0V</td>
<td>0.0V</td>
</tr>
</tbody>
</table>

Vout = 0.75V * (1 + Ra / Rb)

**Placement Note:**
PLACE C7507, C7508 GND NEAR PIN 1

**Routing Note:**
put 6 vias under the thermal pad

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SYNC_MASTER=M70
SYNC_DATE=01/09/2007
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5V/3.3V POWER SUPPLY

State | SMC_PM_G2_EN | PP3V3_G3H | PP5V_S5 | PP3V3_S5
--- | --- | --- | --- | ---
G3H | LOW | 3.3V | 0.0V | 0.0V
SO/S3/S5 | HIGH | 3.3V | 5.0V | 3.3V

Vout = 1V * (1 + Ra / Rb)
5.106V = 1V * (1 + 20K / 4.87K)

Routing Note:
- Routing Note:
  - A dedicated trace to the output cap;

Placement Note:
- Placement Note:
  - Close to U7600 pin 19.

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051-7230
Supply needs to guarantee 3.31V delivered to SMC VRef generator.

P3V42G3H_SHDN_L in the event Q7730 will pull down

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

Vout = 1.25V * (1 + Ra / Rb)

Vout = 0.9V * (1 + Ra / (Rb + Rc))
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL

1.8V S3 RUN/SS CONTROL

5V S3 FET

1.8V S3 FET

3.3V S3 FET
SST8051 microcontroller for HDCP support
Place components near J4200 unless otherwise noted
ENA does not glitch during RESET.
Some signals require 27.4-ohm single-ended impedance.

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

Design Guide recommends FSB signals be routed only on internal layers.

All FSB signals with impedance requirements are 55-ohm single-ended.

Intel says to route with 7 mil spacing without 70_OHM_DIFF = 70_OHM_DIFF = 70_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which STANDARD

CPU Signal Constraints

NOTE: Some signals have 10 mils on the same layer. Design Guide recommends at least 25 mils. 100_OHM_DIFF

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET

SPACING_RULE_SET

FSB_ADDR2ADDR

FSB_DATA2DATA

FSB_ADDR

FSB_DATA

FSB_9MIL

FSB_4MIL

PHYSICAL

CPU / FSB Net Properties

Table 1: Native single-ended to single-ended signals.

Table 2: Native differential to single-ended signals.

Table 3: Native single-ended to differential signals.

Table 4: Native differential to differential signals.

CPU/FSB Constraints

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## Video Signal Constraints

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### Physical Rule Set

- **Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

#### 55-ohm +/- 15%

- From second termination resistor to connector.

#### LVDS signals

- 100-ohm +/- 20% differential impedance.

### Spacing Rule Set

- **Net Spacing Type 1**
- **Net Spacing Type 2**

---

---
### Disk Interface Constraints

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<tr>
<th>Layer</th>
<th>Pin Name</th>
<th>Scale</th>
<th>Size</th>
<th>Min. Pad Width</th>
<th>Min. Pad Length</th>
<th>Min. Spacing</th>
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### Internal Interface Constraints

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### USB 2.0 Interface Constraints

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### PCI Bus Constraints

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### Platform LAN (Nineveh) Constraints

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### Controller Link (AMT) Constraints

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**NOTICE OF PROPRIETARY PROPERTY**

**APPLE INC.**

**SYNC_DATE=01/30/2007**

**SB Constraints (2 of 2)**
### Clock Signal Constraints

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**NOTICE OF PROPRIETARY PROPERTY**

**SIZE OF PROPERTY**

**PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR**
### M82 Board-Specific Spacing & Physical Constraints

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### M82 Rule Definitions

**ISL10, ISL11, ISL13**

- **TOP, BOTTOM**
  - **LAYER**
  - **ALLOW ROUTE ON LAYER?**
    - **Y**
  - **MINIMUM LINE WIDTH**
    - **STANDARD**
  - **MINIMUM NECK WIDTH**
    - **STANDARD**
  - **MAXIMUM NECK LENGTH**
    - **STANDARD**
  - **DIFFPAIR PRIMARY GAP**
    - **STANDARD**
  - **DIFFPAIR NECK GAP**
    - **STANDARD**

**ISL2, ISL4, ISL5**

- **TOP, BOTTOM**
  - **LAYER**
  - **ALLOW ROUTE ON LAYER?**
    - **Y**
  - **MINIMUM LINE WIDTH**
    - **STANDARD**
  - **MINIMUM NECK WIDTH**
    - **STANDARD**
  - **MAXIMUM NECK LENGTH**
    - **STANDARD**
  - **DIFFPAIR PRIMARY GAP**
    - **STANDARD**
  - **DIFFPAIR NECK GAP**
    - **STANDARD**