3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Schematic / PCB #'s

8 7 6 5 4 2 1

8

1 SCHEM,MLB_LDO,K87051-8561 CRITICALSCH

37 (T27_MLB) (12/15/2009)

T27_MLB 02/16/2010

34 (K84_MLB) (10/03/2009)

MASTER MASTER

31 MASTER MASTER

26 T27_MLB 02/16/2010

23 T27_MLB 02/16/2010

22 T27_MLB 02/16/2010

21 T27_MLB 02/16/2010

19 T27_MLB 02/16/2010

18 T27_MLB 02/16/2010

16 T27_MLB 02/16/2010

15 T27_MLB 02/16/2010

14 T27_MLB 02/16/2010

12 T27_MLB 02/16/2010

10 T27_MLB 02/16/2010

9 T27_MLB 02/16/2010

5 (K84_MLB) (01/19/2009)

4 MASTER MASTER

3 MASTER MASTER

1 NA NA

K87 SMBus Connections

SMC

External USB Connectors

ETHERNET CONNECTOR

X16 WIRELESS CONNECTOR

FSB/DDR3 Vref Margining

SO-DIMM Pinswaps

DDR3 SO-DIMM Connector B

MCP Misc

MCP Graphics

MCP PCIe Interfaces

MCP Scratch

MCP Scratch

MCP Memory Interface

MCP Interface

MCP Power & Ground

MCES3 Memory Rail Gating

MCES9 GPX Core Rail Gating

MCF Standard Decoupling

MCF Graphics Support

SE Misc

DDR2 SO-DIMM Connector A

DDR3 SO-DIMM Connector B

SO-DIMM Finishes

EBB/EBB Used Machine

X16 WIRELESS CONNECTOR

Ethernet PHY

DATA Connectors

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SMC

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SMC Support

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K87 SMBus Connections
### Alternate Parts

- **514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR**
- **514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS**
- **353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE**

### Module Parts

**BOM Groups (project phase-dependent)**

- ONSEMI(NEW SPEC) AS ALTERNATE
- TOSHIBA AS ALTERNATE
- **353S2988 353S2987 ALL**
- MAGLAYERS AS ALTERNATE
- **128S0093**
- **152S0693**

**BOM Groups (always-present)**

- **K86_K87_DEBUG:PROD**
- **K86_K87_DEBUG:DEV**
- **K86_K87_DEVELOPMENT_PVT**
- **K86_K87_DEVELOPMENT_ONLY**
- **K86_SPECIFIC**
- **K86_K87_COMMON**
- **K87_SPECIFIC**

**K86_K87_DEBUG:PROD PROJECT_PHASE:PROD**

- **K86_K87_COMMON**
- **K87_SPECIFIC**

**BOM Option**

- **085-1799 K86_K87_DEVELOPMENT_PVTK87 MLB_LDO DEVELOPMENT BOM**

### Part Substitutions (differences with K6/K69)

- **826-4393 1 \[EEEE_DD17\] EEEE:DD17CRITICAL**
- **826-4393 LBL,P/N LABEL,PCB,28MM X 6 MM \[EEEE_DD19\] EEEE:DD19 CRITICAL**
- **RES,MTL FILM,1/16W,113 OHM,1,0402,SMD,LF CRITICAL**
- **826-4393 \[EEEE_DD16\] EEEE:DD16 CRITICAL**

### BOM Configuration

**K86/K87 BOARD STACK-UP**

<table>
<thead>
<tr>
<th>TOP</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>GROUND</td>
</tr>
<tr>
<td>3</td>
<td>SIGNAL(High Speed)</td>
</tr>
<tr>
<td>4</td>
<td>SIGNAL(High Speed)</td>
</tr>
<tr>
<td>5</td>
<td>GROUND</td>
</tr>
<tr>
<td>6</td>
<td>POWER</td>
</tr>
<tr>
<td>7</td>
<td>POWER</td>
</tr>
<tr>
<td>8</td>
<td>GROUND</td>
</tr>
<tr>
<td>9</td>
<td>SIGNAL(High Speed)</td>
</tr>
<tr>
<td>10</td>
<td>SIGNAL(High Speed)</td>
</tr>
<tr>
<td>11</td>
<td>GROUND</td>
</tr>
</tbody>
</table>

**BOTTOM**

- SIGNAL
Added BOM TABLE with LDO:FIXED, LDO:ADJ, and HTOL_SENSE:NO stuffing options

CSA 4: Added MCPHVDD:P2V5, LDO:FIXED, HTOL_SENSE:YES to BOM Group K86_K87_DEBUG:PROD

*** Resynced Audio pages with the following changes:
- Changed C9706 from 120pF to 220pF (131S2225)
- Changed C9705 from 8.2nF to 33nF (132S0131)
- Changed R9726 from 22k to 10k (114S0315) and removed NOSTUFF
- Added L4530, L4531 (APN 155S0137) to SIL connector pins

- pg. 67, no stuffed R6712 and R6713
- pg. 62, changed R6211 to 22 Ohms

CSA 37: Per <rdar://problem/7554342> K86/K87: Change L3720 to 152S1182

CSA 34: Changed U3440 from AP002 part to AP016 (343S0511) per <rdar://7459498> BOM: APN updates for FPF1009 and SAK parts

CSA 25: T27: Removed R2575 & R2580 per DG v1.3 (pg. 25). per <rdar://7459260> Design Guide v1.3 updates

CSA 18: T27: Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). <rdar://7416825> Ensure USB_EXTB is on ports 8-11 (NVRN-612340)

*** Resynced all synced pages and picked up the following (change notes from T27):
- Cosmetic cleanup
- Changed C7428 from 0.47uF => 0.33uF (132S0101) per Intersil
- Deleted net properties for =PP3V3_S3_WLAN
- =PP3V3_S0_PWRCTL'
- =PP5V_S0_HDD'

- REPLACED K84 MCP AND CPU PAGES WITH K6 PAGES

CSA 8: Added Toshiba(376S0908), Fairchild(376S0907) as an alternate to 376S0634.
C6900 changed to 2.2uF. 138S0592.

CSA 25: Added R2600 0ohm resistor to help layout change.

CSA 77: Deleted U7740 1.05V LDO circuit to free space for U2592 and current mirror circuit.

CSA 25: Changed U2594 power to 3V3_S0 from 3V42_G3H.

Per <rdar://7488543> K87/K86 Task Measure each power supply in mlb.

Per <rdar://7686179> K86/K87 schematic: Change audio jack part number for new connector cap

Per <rdar://7634730> K86/K87: add an RC on the LVDS_IG_BKL_PWM

U5400 changed from OPA348 to OPA330. C5434 changed to NOSTUFF

CSA 4: Added OLD_AUDIO_SWITCH BOM OPTION to K86_K87_COMMON1


Added C2599, R2597, R2596, U2593, Q2592, R2599, C2594, U2594, R2598, C2598 with BOMOPTION HTOL_SENSE:YES

CSA 93: Added C9303 3300pF cap on DP_CA_DET.

CSA 12: C1200, C1204, C1207, C1209, C1211, C1219, C1202, C1216 NOSTUFFED

CSA 97: R9725 changed to 200ohm, C9799 of 47pF added. R9726.1 connection moved to LVDS_IG_BKLPWM

CSA 73: Reestablished BOM in BOM table, 16.9K, (APN 114S0336)

CSA 65: Kept K86 and K87 pgs identical for CSA 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86.

CSA 4: T27: Change to GM1130A-0204-01 to 0705-0204-01, changed XDP_CON label change.

CSA 8: Fixed XDP_CON label change.

CSA 34: Added the following functional test points under the J5100 LPC+SPI CONN FUNC_TEST group
- PCBF: 820-2801
- BOM: 639-0680

CSA 45: Added passive deemphasis to SATA HDD D2R lines:
- C7428 = 0.22uF  10% (132S0102)
- R7417 from 5.36k => 6.34k, 1% (114S0296)

CSA 34: Deleted net properties for =PP3V3_S3_WLAN
- =PP3V3_S0_PWRCTL'
- =PP5V_S0_HDD'


C2599, R2597, R2596, U2593, Q2592, R2599, C2594, U2594, R2598, C2598 with BOMOPTION HTOL_SENSE:YES

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CSA 34: Deleted net properties for =PP3V3_S3_WLAN
- =PP3V3_S0_PWRCTL'
- =PP5V_S0_HDD'

Add R4585, R4586 (51.1 ohm, 1%, 114S0293) and OMITted

CSA 4: Added Toshiba(376S0908), Fairchild(376S0907) as an alternate to 376S0634.
C6900 changed to 2.2uF. 138S0592.

CSA 77: Deleted U7740 1.05V LDO circuit to free space for U2592 and current mirror circuit.

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Current numbers from Merom for Santa Rosa EMTS, doc #20905.

PEI ports are Gen2-capable. 1 RCs: x1, x1; 2 RCs: 4x, x2, x1, x1
PEI ports are Gen1-only; 2 RCs: x1, x1

If PEI[1:0] are not used, +VIO_PE_AVDD and +VIO_PE_DVDD can be GND
If PEI[3:0] and PEI[0:1] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND
If PEI[3:0] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

Currents:
- PCIe ports: 25 mA
- PCIe reset: 25 mA
- Other pins: 100 mA, 120 mA

Note: Diagrams and specific current values are shown, but detailed analysis requires understanding of the schematic and the specific application context.

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**PAGE TITLE:**
- MCP PCIe Interfaces

**SYNC_DATE:**
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- 051-8561 C.

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**SHIELDING:**
- SMD barriers are used to shield against EMI.

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DDC Mode Pull-downs
NOTE: If unused, pull-downs are required for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

GPIO Pull-Ups

NOTE: No Composite/S-Video/Component Video support on MCP89.

Connect +3.3V_RGBDAC pin to GND.

Okay to float all RGB_DAC signals.

NOTE: No Composite/S-Video/Component Video support on MCP89 A01.

HDA Output Caps

C1950
C1952
C1951
C1953

R1920
R1921

GPIO Pull-Ups/Downs

R1990
R1991
R1992
R1993
R1994
R1995
R1996
R1997
R1998

HDA_Sync
HDA_RST

Platform-Specific Connections

MCP HDA, LPC & Misc

MCP_CLK25M_XTALIN
MCP_CLK25M_XTALOUT

NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

NOTE: MCP89 does not support FWH, only LPC EDPs. So Apple designs will not use LPC for bootROM override.

**NOTE:** *SM* rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.

**POWER I**

<table>
<thead>
<tr>
<th>Unit</th>
<th>MCP89-A01</th>
<th>MCP89-A11</th>
</tr>
</thead>
<tbody>
<tr>
<td>1200 mA</td>
<td>+VIO_PE_DVDD0_2</td>
<td>+VIO_PE_DVDD1_2</td>
</tr>
<tr>
<td>1000 mA</td>
<td>+VIO_PE_DVDD2_2</td>
<td>+VIO_PE_DVDD3_2</td>
</tr>
<tr>
<td>800 mA</td>
<td>+VIO_PE_DVDD4_2</td>
<td>+VIO_PE_DVDD5_2</td>
</tr>
<tr>
<td>600 mA</td>
<td>+VIO_PE_DVDD6_2</td>
<td>+VIO_PE_DVDD7_2</td>
</tr>
<tr>
<td>400 mA</td>
<td>+VIO_PE_DVDD8_2</td>
<td>+VIO_PE_DVDD9_2</td>
</tr>
<tr>
<td>200 mA</td>
<td>+VIO_PE_DVDD10_2</td>
<td>+VIO_PE_DVDD11_2</td>
</tr>
</tbody>
</table>

**POWER II**

<table>
<thead>
<tr>
<th>Unit</th>
<th>MCP89-A01</th>
<th>MCP89-A11</th>
</tr>
</thead>
<tbody>
<tr>
<td>1200 mA</td>
<td>+VIO_PE_AVDD0_2</td>
<td>+VIO_PE_AVDD1_2</td>
</tr>
<tr>
<td>1000 mA</td>
<td>+VIO_PE_AVDD2_2</td>
<td>+VIO_PE_AVDD3_2</td>
</tr>
<tr>
<td>800 mA</td>
<td>+VIO_PE_AVDD4_2</td>
<td>+VIO_PE_AVDD5_2</td>
</tr>
<tr>
<td>600 mA</td>
<td>+VIO_PE_AVDD6_2</td>
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<td>+VIO_PE_AVDD9_2</td>
</tr>
<tr>
<td>200 mA</td>
<td>+VIO_PE_AVDD10_2</td>
<td>+VIO_PE_AVDD11_2</td>
</tr>
</tbody>
</table>

**NOTE:** VDD_COREA signals should NOT be used for remote sensing unless coreA/PU are powered by separate regulators.**

Use separate regulator sense point as close to coreA PU as possible.

=PP1V5R1V35_SW_MCP_MEM

Instead connect regulator sense point

(8 OF 11)

**MCP Power & Ground**

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Current numbers from MCP89 A01 Bring-Up Support document (MCP89_VDD_Bringup_Voltage_Apple.pdf, dated August 1, 2009). -8/65 KEP currents used.
Q2300 helps reduce input rail droop during Q2300 turn-on.

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1(Kohms)

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh. Clamps enable before MCP89_memVdd rail switched off. Clamps release after MCP89 MemVdd is up and CKEs are driven by MCP89.

Clamp settings: 1.5V, 10% ESR. 0.1µF each (IC-driven). Resistors on each CKE signal on DIMM. g2340/g2354 chosen for low output capacitance.

No Stubs on CKE signals!
NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

Max Ramp-Up Time: 1500 uS (ENABLE to 90%)

- Min Ramp-Up Time: 100 uS (10% to 90%)
- FET Ron <= 2.5 mOhms
- Gated Rail Savings: 860mW
Current #s from MCP89 A01 Bring-Up Support doc (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009)

8 8 20
MCP 3.3V AUX/USB Power
850 mA
MCP 0.9V AUX Core Power
8450 mA (0.85V)

C2520
4.7uF
C2540
4.7uF
C2510
2.2uF

C2521
6.3V
C2541
6.3V
C2511
20%

C2522
20%

C2523
X5R
20%

C2524
4V
C2542
4V
C2512
10V

CERM
CERM
CERM

CERM
CERM
CERM

MCP 3.3V/1.5V HDA Power
MCP 3.3V MAC PLL Power
MCP 1.05V SATA Analog Power
MCP 1.05V CPU/FSB/MEM PLL Power
MCP 1.05V SATA Digital Power
MCP CPU FSB (VTT) Power
MCP 1.05V CPU/FSB/VTT PLL Power
MCP 1.05V SATA/ATA PLL Power
MCP 3.3V DP & USB PLL Power
MCP 3.3V DP & USB PLL Power

=PP3V3_S0_MCP
=PP0V9_S5_MCP_VDD_AUXC
=PPVCORE_S0_MCP
=PP3V3_S5_MCP
=PP0V9_S5_MCP_VDD_AUXC
=PPVCORE_S0_MCP

=PP3V3_S0_MCP_HVDD
=PP1V05_S5_MCP_PLL_UF
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_PLL_UF

PP3V3_S0_MCP_HVDD
PP0V9_S5_MCP_VDD_AUXC
PPVCORE_S0_MCP

PP3V3_S0_MCP_PLL_DP_USB
PP3V3_S0_MCP_PLL_DP_USB

RES,0402,0,5%,1/16W

IC,LDO,TPS717,ADJ,150MA,3%,SC70,HFLF

MCPHVDD:P2V5

RES,0402,0,5%,1/16W

PLACEMENT Notes:

PAGE
BRANCH
DRAWING NUMBER SIZE
35 36 39 40
D
A
C
D

DO NOT PDF FROM TI7. DECODING CAN VALUES CHANGED.

Current #s from MCP89 A01 Bring-Up Support doc (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009)
DO NOT SYNC WITH K84. CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6.

DO NOT WITH KE6 CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6.
Configuration Settings:

- **TXDLY = 0** (No TXCLK Delay)
- **RXDLY = 0** (RXCLK transitions with data)
- **AN[1:0] = 11** (Full auto-negotiation)
- **PHYAD = 01** (PHY Address 00001)

*NOTE: RC (C3725 AND R3725) ARE NOT STUFFED.
ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.

If internal switcher is used, must place inductor within 5mm of U3710, and in 22µH ± 5% range. If internal switcher is not used, U3710 and R3720 can float.

*NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.*

**Configuration Note:**

- If internal switcher is used, must place inductor within 5mm of U3710, and in 22µH ± 5% range. If internal switcher is not used, U3710 and R3720 can float.

*NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.*
Transformers should be mirrored on opposite sides of the board.
SATA HDD

SATA ODD

ODD Power Control

Passive de-emphasis filter

Use 0-ohm resistors and 0.068UF caps if not using the 0-ohm resistors and BEMSTUFF caps.
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designated as outputs can be left floating, those designated as inputs require pull-ups.
NOTE: Internal pull-ups are to VIN, not V+. MR1* and MR2* must both be low to cause manual reset. Use no switches to support SMC reset via keyboard.

PLACE_NOTE=Place R5001 on BOTTOM side

SILK_PART=SMC_RST

R5001

SILK_PART=PWR_BTN

1%
**Battery (BMON) Current Sense, MUX & Filter**

- **Current Sensing**
- **Apple Inc.**

**MCP VCore Current Sense Filter**
- **Gain:** 100x
- **Scale:** 10A/V
- **Max Vout:** 2.48V

**MCP MEM VDD Current Sense / Filter**
- **Note:** Place near sense resistor across R7008 battery to PBUS (battery discharge)

**CPU VCore Load Side Current Sense / Filter**
- **Note:** Do not stuff R5415 and R7593 at the same time!

**DC-IN (AMON) Current Sense Filter**
- **Gain:** 36x
- **ISL6259 Gain:** 36x
- **INA213 Gain:** 50x

**Notes:**
- Place close to SMC
- Place close to SMC
- Place close to SMC
- Place close to SMC
- Place close to SMC
- Place close to SMC

**PLACEMENT_NOTE:** Place near sense resistor across R7008 battery to PBUS (battery discharge)

**PLACEMENT_NOTE:** Place close to SMC (For R and C)

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**PLACEMENT_NOTE:** Place close to SMC (For R and C)

**PLACEMENT>Note:** Do not stuff R5415 and R7593 at the same time!
**CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR**

- Internal diode in U5535 detects MCP proximity temperature.
- Internal diode in U5515 detects CPU proximity temperature.
- Internal diode in U5525 detects HDD temperature.

**MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR**

- Internal diode in U5535 detects MCP proximity temperature.
- Internal diode in U5515 detects CPU proximity temperature.
- Internal diode in U5525 detects HDD temperature.
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- Power consumption
- Drop line regulation
- Ripple to meet ERS
- Startup time less than 2ms
- DROOP LINE REGULATION
- 100-300 KHZ CLEAN SPECTRUM
- POWER CONSUMPTION

IPD Flex Connector

DO NOT SYNC FROM T27. REMOVED KEYBOARD BKLIGHT CIRCUIT

MIN_LINE_WIDTH=0.50MM
VOLTAGE=18.5V
MIN_NECK_WIDTH=0.20MM
PP18V5_S3

VOLTAGE=5V
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
PP5V_S3_P18V5S3_VIN

Z2_RESET
PSOC_F_CS_L
PICKB_L
PSOC_MISO
PSOC_MOSI
PSOC_SCLK
=I2C_TPAD_SDA
=I2C_TPAD_SCL

Z2_BOOST_EN
SWITCH_NODE=TRUE
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
P18V5S3_FB

Z2_CS_L
Z2_MOSI
Z2_MISO
Z2_SCLK
Z2_BOOST_EN
Z2_HOST_INTN

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DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923,C5924,C5925. ADDED PLACE NEARS
**NOTE:** SPI cycles are ignored if HOLD* is asserted.

- **SPI Frequency Select**
  - Frequency: SPI_MOSI, SPI_CLK
  - 25.0 MHz: 0 0
  - 31.2 MHz: 0 1
  - 41.7 MHz: 1 0
  - 62.5 MHz: 1 1

*NOTE: 25 & 31 MHz use FAST_READ command.*

**Components:**
- U6100: 32MBIT MX25L3205DM2I-12G SOP
- R6101: 3.3K 5% 1/16W MF-LF
- C6100: 20% 0.1UF CERM
- R6150: 10K 5% 1/16W MF-LF
- R6151: 10K 5% 1/16W MF-LF
- R6152: 10K 5% 1/16W MF-LF
- R6153: 10K 5% 1/16W MF-LF

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**Sheet:**
- Page 2 of 109
- Drawing Number: A-001
- Branch: R-008
- Revision: D
- Size: 47 of 76
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
RIN = 20K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
PC_VIN = 3.6 VDC
PC_VIN = 4.30VDC
VIN = 2V RMS, CODEC VIN = 1.14 VRMS

AUDIO: LINE INPUT FILTER

R6301
C6301
R6302
C6302
C6311
R6311
C6312
R6312
C6313
SATELLITE 796Hz < HPF FC < 936Hz
SUB 80 Hz < HPF FC < 94 Hz
GAIN 6DB (2V/V)
SPRKR AMP. INPUT REFERRED CLIP POINT = ~6dBFS
DO NOT SYNC WITH K84. R6900, C6960, SIGNAL NAMES CHANGED. HALL EFFECT CONNECTOR CHANGED.
1.05V ENET Switcher

1.05V S0 MCP PLL LDO

Vout = 0.6V * (1 + Ra / Rb)

1.8V S0 Switcher

1.8V S0 Switcher

MCP 0.9V S5 (AUXC) Switcher

Vout = 0.902V

Max Current = 1.5A

f = 1.6MHz

1.05V S0 MCP PLL LDO

Vout = 1.05V @ 800mA

Max Current = 0.3A

Vout = 1.902V

f = 1.6MHz

Notes:
- C7710 and C7715 have bypass property, should be added unless this pack is sync'd from Y27.
FOUR GROUND VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY.

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CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP.

---

LVDS CONNECTOR: 518S0650

CAMERA I/F

LED BKLT I/F

LVDS I/F

LVDS CONNECTOR

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm
VOLTAGE=5V
PP5V_S3_CAMERA_F

LVDS_IG_DDC_CLK=PP3V3_S0_LCD_DDC

MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.25 mm
VOLTAGE=3.3V
PP3V3_S0_LCD_DDC_F

LVDS_IG_A_CLK_F_P

LVDS_IG_A_CLK_F_N

LVDS_IG_A_CLK_N

USB_CAMERA_P

USB_CAMERA_N

PPVOUT_S0_LCDBKLT

PP3V3_S0_LCD_PANEL

MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.30 mm
VOLTAGE=3.3V
PP3V3_SW_LCD_PANEL_F

LVDS_IG_A_DATA_P<2>

LVDS_IG_A_DATA_N<2>

LVDS_IG_A_DATA_P<1>

LVDS_IG_A_DATA_N<1>

LVDS_IG_A_DATA_P<0>

LVDS_IG_A_DATA_N<0>

LED_RETURN_1

LED_RETURN_2

LED_RETURN_3

LED_RETURN_4

LED_RETURN_5

LED_RETURN_6

---

SYNC_DATE=(10/19/2009)
SYNC_MASTER=(K84_MLB)
13.3 Inch, K84 Panel (9 LEDs per string)

TARGET: ISET = 20mA, OVP = 35V

ISET = 153mA / <Riset>

TARGET: ISET = 20mA, OVP = 35V

1.0 ohm resistors for current measurement on LED strings.
MCP79 has internal 10k pull-up for these signals. MCP89 drives them low.

PPBUS_S0_LCDBKLT = PPBUS_S0_LCDBKLT_FUSED

PPBUS_S0_LCDBKLT_en_L

MIN_NECK_WIDTH = 0.25 mm
MIN_LINE_WIDTH = 0.4 mm
VOLTAGE = 12.6V

PPBUS_S0_LCDBKLT_PWR

BKLT_EN_L

MIN_NECK_WIDTH = 0.25 mm
MIN_LINE_WIDTH = 0.4 mm
VOLTAGE = 12.6V

PPBUS_S0_LCDBKLT_FUSED

PBUS_S0_LCDBKLT_EN_DIV

MCP79 has internal 10k pull-up for these signals. MCP89 drives them low.

PPBUS_S0_LCDBKLT = PPBUS_S0_LCDBKLT_FUSED

PPBUS_S0_LCDBKLT_en_L

MIN_NECK_WIDTH = 0.25 mm
MIN_LINE_WIDTH = 0.4 mm
VOLTAGE = 12.6V

PPBUS_S0_LCDBKLT_PWR

BKLT_EN_L

MIN_NECK_WIDTH = 0.25 mm
MIN_LINE_WIDTH = 0.4 mm
VOLTAGE = 12.6V

PPBUS_S0_LCDBKLT_FUSED

PBUS_S0_LCDBKLT_EN_DIV

LCD Backlight Support

Apple Inc.

SYNC_DATE = (10/19/2009)

SYNC_MAIN = (K84_MLB)
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Signals within each 4x group should be matched within 5 ps of strobe.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
No DQS to clock matching requirement.
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 3 ps.

**Memory Bus Constraints**

**Memory Bus Spacing Group Assignments**

**Memory Net Properties**

**MCP MEM COMP Signal Constraints**

**Please refer to the source documents for detailed information.**
NEED PCIe Gen1/Gen2 notes!

Analog PCIe Gen1/Gen2 notes!

**Digital Video Signal Constraints**

- Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

**SATA Interface Constraints**

- Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2.

**SATA Interface Constraints**

- Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6.
### Physical Constraints

#### MINIMUM LINE WIDTH
- **Allow Route**: Indicates the layers for which minimum line width constraints apply.
- **On Layer**: Specifies the layers related to the minimum line width constraints.

#### DIFFPAIR PRIMARY GAP

#### DIFFPAIR NECK GAP

#### ENET_MDI
- **?25 MIL**: Indicates a specific value for ENET_MDI, which is 25 mils.

#### ENET_MII
- **55_OHM_SE**: Indicates a specific value for ENET_MII, which is 55 ohm series termination.

#### ENET_MDI_100D

#### ENET_MII_55S

#### MCP_BUF0_CLK
- **=3:1_SPACING**: Indicates a specific spacing requirement for MCP_BUF0_CLK.

#### MCP_MII_COMP
- **=STANDARD**: Indicates a specific condition for MCP_MII_COMP.

#### MCP_CLK25M_BUF0

#### ENET_INTR_L

#### MCP_MII_COMP_GND

#### MCP_MII_COMP_VDD

#### ENET_PWRDWN_L

#### ENET_RXD_R<3..0>

#### ENET_TXD<3..1>

#### ENET_TXD<0>

#### ENET_TXD0

#### ENET_TX_CLK

#### ENET_CLK125M_TXCLK

#### ENET_RXCLK

#### ENET_PWRDWN_L

#### ENET_RESET_L

#### ENET_TX_CTRL

#### ENET_RX_CTRL

#### ENET_TXD

#### ENET_RXD

#### ENET_RXD<0>

#### ENET_RXD<3..1>

#### ENET_RXD_STRAP

#### MCP_RGMII (Ethernet) Constraints

#### MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

#### Ethernet Constraints

#### Alternate Source

**Source**: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

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### SMC SMBus Net Properties

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<tr>
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<th>Net_ID</th>
<th>Position</th>
<th>Voltage</th>
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<td>2</td>
<td>1.8</td>
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<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
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<td>3</td>
<td>1.8</td>
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<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
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### Misc Net Properties

#### Power Net Properties

#### Audio Net Properties

### MCP Fanout Constraint Relaxations

#### Graphics Net Properties
<table>
<thead>
<tr>
<th>BOARD LAYER</th>
<th>BOARD AREAS</th>
<th>PHYSICAL_RULE_SET</th>
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<tr>
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<td>ON LAYER?</td>
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<td>LAYER MINIMUM</td>
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<td>NECK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GAP</td>
</tr>
</tbody>
</table>

- ISL3, ISL4, ISL9, ISL10
- 50_OHM_SE
  - 0.115 MM TOP, BOTTOM
- 100_OHM_DIFF
  - 0.100 MM 0.224 MM
- 0.244 MM 0.115 MM 0.075 MM 0.075 MM
- 100_OHM_DIFF
  - 0.230 MM
- 0.091 MM 0.230 MM
- 0.091 MM TOP, BOTTOM

- Y
  - 12.7 MM
- MINIMUM LINE WIDTH
  - ALLOW ROUTE

- 0.112 MM 0.112 MM
- 0.220 MM
- 0.076 MM 0.076 MM
- 0.126 MM
- 40_OHM_SE
  - * 0.100 MM
- 50_OHM_SE
  - 0.090 MM TOP, BOTTOM
- 0.090 MM
- 0.222 MM 0.222 MM
- 0.310 MM TOP, BOTTOM
- 0.100 MM TOP, BOTTOM
- 0.165 MM

- 90_OHM_DIFF
  - 0.4 MM
- 1.5X_DIELECTRIC 0.095 MM
- 5X_DIELECTRIC
- 4X_DIELECTRIC
- 3X_DIELECTRIC
- 2X_DIELECTRIC

- 4:1_SPACING
  - 0.4 MM
- DEFAULT
  - 0.1 MM

- TOP, BOTTOM
  - 0.210 MM 3X_DIELECTRIC
  - 1.5X_DIELECTRIC 0.105 MM
  - 0.189 MM 2.5:1_SPACING
  - 0.252 MM
  - 0.315 MM

- 1.5X_DIELECTRIC
  - 0.105 MM
- TOP, BOTTOM
  - 0.280 MM 4X_DIELECTRIC
- TOP, BOTTOM
  - 0.350 MM 5X_DIELECTRIC

- 2BGA_P1MM
  - 0.189 MM
- 2BGA_P2MM
  - 0.189 MM
- BGA_P2MM
  - 0.350 MM

- 15.5.1
- 22.3
- 27P4_OHM_SE
  - 0.310 MM TOP, BOTTOM
- 0.100 MM TOP, BOTTOM

- 90_OHM_DIFF
  - 0.234 MM 0.095 MM

- CLK_PCIE
  - BGA_P1MM BGA_P2MM
- CLK_FSB
  - BGA_P1MM BGA_P2MM
- CLK_SLOW
  - BGA_P1MM
- MEM_CLK
  - BGA_P1MM
- MEM_40S STANDARDBGA_P1MM

- 1.5X_DIELECTRIC
  - 0.095 MM
- TOP, BOTTOM
  - 0.210 MM 3X_DIELECTRIC
- TOP, BOTTOM
  - 0.189 MM 2.5:1_SPACING
- TOP, BOTTOM
  - 0.252 MM
- TOP, BOTTOM
  - 0.315 MM