## K36C MLB SCHEMATIC

### APR/10/2009

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System Block Diagram

Drawn by: [Names]
Reviewed by: [Names]

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Description:

- **Intel CPU**: 2.66 GHz, Penryn
- **Nvidia MCP79**: U400
- **PCI-E**: J4300
- **FW Port**: J3400
- **Mini PCI-E**: J4200
- **O/S**: 2.8 GHz or 3.0 GHz
- **FSB**: 64-Bit, 640 MHz
- **DIMM's**: 2 UDIMMs, DDR2-800MHz
- **PCI**: 32-bit, 2.5 GT/s (up to four ports)
- **PCI-E**: 16-bit, 2.5 GT/s
- **HDMI Out**: LVDS, TMDS
- **Display**: 1536 x 864
- **Audio**: 88E1116
- **SMB**: J6950, J5751
- **Power Supply**: 76W
- **Power Sense**: J8000, J5800, J5900, J4810
- **Speaker**: J3900
- **Amps**: J4500, J4501
- **USB**: 800/1067/1333 MHz
- **DIMM**: XDP Conn
- **Intel CPU**: PG 25, 26
- **ODD**: PG 37
- **E-NET**: 88E1116
- **Minivalves**: 9216, 9217
- **LPC**: J5100
- **GPIOs**: PG 13
- **Audio**: PG 14, 15, 16, 17, 18
- **HDA**: PG 19
- **USB**: PG 44, 45
- **FAN Conn and Control**: J5601
- **Temp Sensor**: J5520
- **SPI**: J3100, 3200
- **Sync Master**: J36B
- **Sync Date**: 08/17/2008
- **System Block Diagram**: 051-8089
### BOM OPTION

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
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### ALTERNATES OPTION

<table>
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<tr>
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<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
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### BOARD STACK-UP AND CONSTRUCTION

#### Top
- 2: SIGNAL
- 3: GROUND
- 4: SIGNAL (High Speed)
- 5: SIGNAL (High Speed)
- 6: GROUND
- 7: POWER
- 8: SIGNAL (High Speed)
- 9: SIGNAL (High Speed)
- 10: GROUND
- 11: SIGNAL

#### Bottom
- SIGNAL
PAGE 39:
- C7560 FROM 128S0092 CHANGE TO 128S0218.
- Q7500 FROM 376S0512 CHANGE TO 376S0652.
- XW7400 ADD BOMOPTION OMIT.

PAGE 58:
- C7343 FROM 128S0073 CHANGE TO 128S0233.
- Q7321 FROM 376S0511 CHANGE TO 376S0651 (H-F)
- Q7320 FROM 376S0512 CHANGE TO 376S0652 (H-F)
- Q7260, Q7261 FROM 376S0512 CHANGE TO 376S0652 (H-F)

PAGE 60:
- 128S0222 (POLY, CASE-B2-SM)

PAGE 25:
- C7281, C7241, C7272 FROM 138S0555(603) CHANGE TO 138S0615(603-1)
- C2504-C2507 FROM 138S0578(402) CHANGE TO 138S0614(402-1)

PAGE 18:
- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.
- R0602 BOMOPTION FROM JTAG_1DEV CHANGE TO NO STUFF.

PAGE 6:
- REMOVE R9010, R9011

PAGE 46:
- ADD =RTL8211_ENSWRE LINK TO GND.

PAGE 9:
- ADD =PP3V3_S5_P3V3ENETFET LINK TO PP3V3_S5
- REMOVE ETHERNET CIRCUIT.

PAGE 63:

PAGE 50:
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE

PAGE 41:
- R4690 FROM NO STUFF CHANGE TO STUFF.

PAGE 39:
- L3401 FROM NO STUFF CHANGE TO STUFF.

PAGE 23:
- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.
- CHANGE XDP_TDO_CONN TO XDP_TDO
- =P3V3ENET_EN_L LINK TO PM_SLP_RMGT_L

PAGE 68:
- ADD =RTL8211_ENSWRE LINK TO GND.

PAGE 9:
- NET DPMUX_SEL_IG_L SYNC M97 NETNAME
- REMOVE J9001 PIN 20 AND PIN21 NET.

PAGE 66:
- REMOVE R7884 AND C7884

PAGE 57:
- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.

PAGE 43:
- ADD R5055 10KOHM LINK SMC_NB_MISC_ISENSE PULL DOWN TO GND.
- ADD R5054 10KOHM LINK SMC_GPU_ISENSE PULL DOWN TO GND.
- ADD SMC_SYS_KBDLED TO NC_SMC_SYS_KBDLED
- ADD ESTARLDO_EN TO NC_ESTARLDO_EN
- ADD ALS_GAIN TO NC_ALS_GAIN
- ADD SMC_RSTGATE_L TO TP_SMC_RSTGATE_L
- ADD SMC_EXCARD_PWR_EN TO TP_SMC_EXCARD_PWR_EN
- REMOVE NET DIMM_OVERTEMPA_L
- NET LVDSMUX_SEL_IG_L SYNC M97 NETNAME
- NET DPMUX_LOWPWR_L SYNC M97 NETNAME AUD_IPHS_SWITCH_EN

PAGE 19:
- NETNAME ENET_INTR_L CHANGE TO TP_ENET_INTR_L.

PAGE 18:
- ADD GMUX_JTAG_TMS AND GMUX_JTAG_TDI IN MISC NC MCP79 ALIASES.

PAGE 14:
- ADD =PP3V42_G3H_RTC_D LINK TO =PP3V42_G3H_REG

PAGE 8:
- R7011 CHANGE TO 9.31K OHM, 1%
- R7879 CHANGE TO 100K OHM.

PAGE 64:
- U7500 PIN TONSEL LINK TO GND DIRECTLY.
- U7500 PIN V5DRV1 LINK TO PP5V_S0_MCPREG_VCC.

PAGE 61:
- *****2008/08/21*****
- Revision History

PAGE 9:
- NET DPMUX_SEL_IG_L SYNC M97 NETNAME
- REMOVE J9001 PIN 20 AND PIN21 NET.

PAGE 66:
- REMOVE R7884 AND C7884

PAGE 28:
- ADD STANDOFF 860-0749 X 1
- ADD STANDOFF 860-0723 X 1
- ADD STANDOFF 860-0964 X 4

PAGE 15:
- ADD =PP3V42_G3H_RTC_D LINK TO =PP3V42_G3H_REG

PAGE 8:
- R7011 CHANGE TO 9.31K OHM, 1%
- R7879 CHANGE TO 100K OHM.

PAGE 64:
- U7500 PIN TONSEL LINK TO GND DIRECTLY.
- U7500 PIN V5DRV1 LINK TO PP5V_S0_MCPREG_VCC.

PAGE 61:
- *****2008/08/21*****
- Revision History
1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)

From XDP connector

U1000

CPU

To XDP connector

and/or level translator

From XDP connector

or via level translator

U1400

MCP
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
See with XDP-VS6 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

ABCD

1234

5678

9012

3456

7890

ABCD
HDA Output Caps

For EMI Reduction on HDA interface
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SYNC_MASTER=K36B_MLB
SYNC_DATE=08/17/2008

MCP79 A01 Silicon Support
HDCP ROM

- Open question on which package option(s) Nvidia can support.

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672
**RTC Power Sources**

- \( \text{C2870, C2871, C2872} \) - 100uF, X5R, 10V, 5%

**RTC Crystal**

- \( \text{C2810, C2811, C2812} \) - 12pF, CERM, 5%

- \( \text{C2816, C2817, C2818} \) - 12pF, CERM, 5%

**MCP 25MHz Crystal**

- \( \text{C2819, C2820, C2821} \) - 12pF, CERM, 5%

**Reset Button**

- \( \text{R2801, R2802, R2803} \) - 10K pull-up to 3.3V S0 inside MCP

**MCP S0 PWRGD**

- \( \text{C2826, C2827, C2828} \) - 10PF, CERM, 5%

**Platform Reset Connections**

- LPC Reset (Unbuffered)
  - \( \text{R2881, R2882, R2883, R2884, R2885} \)

- PCIE Reset (Unbuffered)
  - \( \text{R2891, R2892, R2893, R2894} \)

- LPC_CLK33M_LPCPLUS, LPC_CLK33M_SMC, LPC_CLK33M_SMC_LPCPLUS

**RTC Power Sources**

- \( \text{R2810, R2811, R2812} \) - 1UF, X5R, 10V, 5%

**RTC Crystal**

- \( \text{R2820, R2821, R2822} \) - 5%

**MCP 25MHz Crystal**

- \( \text{C2820, C2821, C2822} \) - 5%

**Reset Button**

- \( \text{R2825, R2826, R2827} \) - 5%

**MCP S0 PWRGD**

- \( \text{C2826, C2827, C2828} \) - 5%

**Platform Reset Connections**

- LPC Reset (Unbuffered)
  - \( \text{R2881, R2882, R2883, R2884, R2885} \)

- PCIE Reset (Unbuffered)
  - \( \text{R2891, R2892, R2893, R2894} \)

- LPC_CLK33M_LPCPLUS, LPC_CLK33M_SMC, LPC_CLK33M_SMC_LPCPLUS

**RTC Power Sources**

- \( \text{R2810, R2811, R2812} \) - 1UF, X5R, 10V, 5%

**RTC Crystal**

- \( \text{R2820, R2821, R2822} \) - 5%

**MCP 25MHz Crystal**

- \( \text{C2820, C2821, C2822} \) - 5%

**Reset Button**

- \( \text{R2825, R2826, R2827} \) - 5%

**MCP S0 PWRGD**

- \( \text{C2826, C2827, C2828} \) - 5%

**Platform Reset Connections**

- LPC Reset (Unbuffered)
  - \( \text{R2881, R2882, R2883, R2884, R2885} \)

- PCIE Reset (Unbuffered)
  - \( \text{R2891, R2892, R2893, R2894} \)

- LPC_CLK33M_LPCPLUS, LPC_CLK33M_SMC, LPC_CLK33M_SMC_LPCPLUS

**RTC Power Sources**

- \( \text{R2810, R2811, R2812} \) - 1UF, X5R, 10V, 5%

**RTC Crystal**

- \( \text{R2820, R2821, R2822} \) - 5%

**MCP 25MHz Crystal**

- \( \text{C2820, C2821, C2822} \) - 5%

**Reset Button**

- \( \text{R2825, R2826, R2827} \) - 5%

**MCP S0 PWRGD**

- \( \text{C2826, C2827, C2828} \) - 5%
Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE

- R2901 IN/UNIN
- R2902 IN/UNIN
- R2903 IN/UNIN
- R2904 IN/UNIN
- R2905 IN/UNIN
- R2906 IN/UNIN

Voltage divider resistor values at op-amp outputs not yet finalized.
The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.
One cap for each side of every RPAE, one cap for every two discrete resistors

MONOSOFT shown at the top of each group applies to every part below it.

LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM.
CONNECT TO M35 MODULE

OLD:51400404 (FOXCONN ONLY)
NEW:51400435 (FOXCONN & ACON)
**WLAN Enable Generation**

**NOTE:** S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

**WLAN Enable Generation**

**NOTE:** S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

**1.05V ENET FET**

**NOTE:** MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

**RTL8211 25MHz Clock**

**NOTE:** MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

**Ethernet & AirPort Support**

**NOTE:** Ethernet & AirPort Support

**Ethernet & AirPort Support**

**NOTE:** Ethernet & AirPort Support
PLACE ONE CAP EACH NEAR PINS 3 AND 6 OF T3901 AND T3902

- COPY THIS PAGE FROM K36 CSA.39
**Page Notes**

- Power aliases required by this page:
  - `=PPBUS_S5_FWPWRSW` (system supply for bus power)
  - `=PPBUS_S5_FW_FET` ...

- Signal aliases required by this page:
  - `=PP3V3_FW_LATEVG_ACTIVE`

- BOM options provided by this page:
  - (NONE)

---

**FireWire Port Power Switch**

Enable port power when machine is running or on AC.

**Late-VG Event Detection**

2.0V on late Vg event and port power is off

2.95V when port power is on

Enables port power when machine is running or on AC.

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**FireWire Port Power**

**SCALE REV.**

**SHT OF**

**SIZE**
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designated as inputs require pull-ups.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS and VSS are shorted, VSS could be spare.
ADD NC ALIASES FOR FAN1 SIGNALS
**CPU T-Diode Thermal Sensor**

- Detect CPU die temperature
- Detect heat-pipe temperature
- Detect fin-stack temperature
- Detect MCP die temperature

**MCP T-Diode Thermal Sensor**

- Internal diode in U5535 detects MCP proximity temperature
Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

SMS_Y_AXIS
SMS_Z_AXIS
SMS_SELFTEST
SMS_ONOFF_L SMS_PWRDN
MAKE_BASE=TRUE

SMS_INT_L = PP3V3_S5_SMC
SMS_X_AXIS = PP3V3_S3_SMS

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Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

+X Front of system
+Y
+Z (down)

Desired orientation when placed on board bottom-side:

+X Front of system
+Y
+Z (up)
25MHz IS SELECTED WITH R5164 AND R5144
ANY OF THE 4 FREQUENCIES CAN BE SELECTED
WITH R6190, R6191, R5164 AND R5144
1.8V/0.9V (DDR2) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

COPY THIS PAGE FROM K36 CSA.75

MAX CURRENT = 12A
PWM FREQ. = 400 KHZ
PUT ONE BULK CAP NEXT TO THE LOAD

=PP0V9_S0_REG
=PPVIN_S5_1V8S3_0V9S0
=PP1V8_S3_REG

+) 1V8S3_CS
()) 1V8S3_VBST
(() 1V8S3_VDDQSNS
\) 1V8S3_VTTSNS
\) VOUT = 0.75V * (1 + RA / RB)

C7307
22UF
603
X5R-CERM
6.3V 20%

XW7303
X5R
10V 10%
1UF
C7300

R7310
603X5R-CERM
6.3V 20%
10K
402 MF-LF 1/16W 1%

XW7302
XW7300

CRITICAL
U7300
TPS51116

CRITICAL
C7340
100PF 402CERM 50V 5%

R7307
330UF CASE-C2-SM1 POLY-TANT 2.5V 20%

R7308
1UF
402 X5R 25V 10%

C7341
CASE-D2E-SM POLY-TANT 2.5V 20%

R7300
10UF 6.3V 603 20%

R7321
28K 402 MF-LF 1/16W 1%

C7303
10UF 603 20%

R7311
22K 402 MF-LF 1/16W 1%

C7301
10UF 6.3V 603 20%

XW7301
XW7302

R7309
0.1uF 402 X5R 16V 10%

C7331
33UF 16V 20%

C7332
1UF 402 X5R 25V 10%

C7333
0.001UF 50V CERM 20%

C7334
330UF CASE-C2-SM1 POLY-TANT 2.5V 20%

C7335
0.001UF 50V CERM 20%

R7322
20K 402 MF-LF 1/16W 1%

R7312
10K

C7309
0.1uF 402 X5R 16V 10%

R7340
10.7K 402 MF-LF 1/16W 1%

R7323
1/16W 1%

R7324
1/16W 1%

R7341
1/16W 1%

R7342
1/16W 1%

CRITICAL
U7301
PWRPK-1212-8-HF

Q7320
CRITICAL
2.2UH-13A-5.6M-OHM
L7320

Q7321
CRITICAL

XW7300
SM-IHLP-1 1.0UH-13A-5.6M-OHM

CRITICAL
PWRPK-1212-8-HF

PIN 3 and Pin 25 of U7300.

Place XW7302 by Q7321.

Place XW7300 between

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=1 mm

PUT ONE BULK CAP NEXT TO THE LOAD

SM
ROUTING NOTE:

PUT 6 VIAS UNDER THE THERMAL PAD

CRITICAL

CRITICAL

CRITICAL

CRITICAL

CRITICAL

CRITICAL

CRITICAL

CRITICAL

CRITICAL

1.8V/0.9V DDR2 SUPPLY

STATE | PM_SLP_S4_L | PM_SLP_S3_L | PP1V8_S3 | PP0V9_S0
-----|-------------|-------------|----------|----------
S0   | HIGH       | HIGH       | 1.8V     | 0.9V     |
S3   | HIGH       | LOW        | 1.8V     | 0.0V     |
S1/G3HOT | LOW       | LOW        | 0.0V     | 0.0V     |

NO STUFF

NO STUFF

NO STUFF
FireWire 1.0V (Core) Supply

VOUT = 0.6V * (1 + Ra / Rb)

1.5V S0 SWITCH

VOUT = 0.6V * (1 + Ra / Rb)
Power Control Signals

5.0V (RIGHT AND LEFT), 3.3V AND 1.5V S0 RAILS MONITOR CIRCUIT

LAYOUT NOTE: ADD XW IF NEEDS TO SAVE SPACE FOR PIN2,10,1,9

Power Sequencing
### FSB (Front-Side Bus) Constraints

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<th>Source</th>
<th>MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4</th>
</tr>
</thead>
</table>

Some signals require 27.4-ohm single-ended impedance.

### CPU Signal Constraints

- **NOTE:** Intel Design Guide allows closer spacing if signal lengths can be shortened.
- **Design Guide recommends each strobe/signal group is routed on the same layer.**
- **Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.**
- **FSB 1X signals shown in signal table on right.**
- **Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.**
- **FSB 2X signals / groups shown in signal table on right.**
- **DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.**
- **DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.**
- **FSB 4X signals / groups shown in signal table on right.**
- **All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.**

### FSB Clock Constraints

- **SOURCE:** MCP79 Interface DG (DG-03328-001_v01), Section 2.2

Some signals with impedance requirements are not shown in single-ended.

FSB 2x signals / groups shown in signal table on right.

- Signals within each 2x group should be matched within 1ps. DSTB# should be matched +/- 300ps.
- FSB 2x signals shown in signal table on right.
- Signals within each 1x group should be matched to CPU clock, +/-1000 mils.
- Design Guide recommends each strobe/signal group is routed on the same layer.
- All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.
### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL_RULE_SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_DATA</td>
<td>MEM_DQS2MEM</td>
<td>MEM_DQS</td>
<td>MEM_DATA2MEM</td>
<td>MEM_CTRL2MEM</td>
<td>MEM_CLK2MEM</td>
</tr>
<tr>
<td>MEM_DQS</td>
<td>MEM_DQS2MEM</td>
<td>MEM_DQSN</td>
<td>MEM_2OTHER</td>
<td>MEM_CLK</td>
<td>MEM_CMD</td>
</tr>
</tbody>
</table>

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Layer</th>
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<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
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<td>MEM_DQS</td>
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<td>MEM_CTRL2MEM</td>
<td>MEM_CLK2MEM</td>
</tr>
<tr>
<td>MEM_DQS</td>
<td>MEM_DQS2MEM</td>
<td>MEM_DQSN</td>
<td>MEM_2OTHER</td>
<td>MEM_CLK</td>
<td>MEM_CMD</td>
</tr>
</tbody>
</table>

### Memory Net Properties

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<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL_RULE_SET</th>
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</thead>
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<tr>
<td>MEM_DQS</td>
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### MCP MEM COMP Signal Constraints

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<th>PHYSICAL_RULE_SET</th>
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<td>MEM_DQS2MEM</td>
<td>MEM_DQS</td>
<td>MEM_DATA2MEM</td>
<td>MEM_CTRL2MEM</td>
<td>MEM_CLK2MEM</td>
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<tr>
<td>MEM_DQS</td>
<td>MEM_DQS2MEM</td>
<td>MEM_DQSN</td>
<td>MEM_2OTHER</td>
<td>MEM_CLK</td>
<td>MEM_CMD</td>
</tr>
</tbody>
</table>

---

**No DQS to clock matching requirement.**

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
### SPI Interface Constraints

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<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>DiffPAIR Primary Gap</th>
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<tbody>
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### SMBus Interface Constraints

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### LPC Bus Constraints

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### USB 2.0 Interface Constraints

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### SIo Signal Constraints

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### MCP Constraints 2

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### MCP RMII (Ethernet) Constraints

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### 88E1116R (Ethernet Phy) Constraints

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</table>

**Source:**
- MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

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8 7 6 5 4 3 2 1

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**Ethernet Constraints**

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**Source:**
- MCP73 Interface DG (DG-02974-001_v01), Section 3.5.1
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A
| SMBus SMCm Bus Net Properties | | | | | |
|---|---|---|---|---|
| **NET** | **DESCRIPTION** | **TYPE** | **VALUE** |
| SMC_55S | SMBUS_SMC_MGMT_SDA | ST | 0.1 MM |
| SMC_55S | SMBUS_SMC_B_S0_SCL | ST | 0.1 MM |
| SMC_55S | SMBUS_SMC_B_S0_SDA | ST | 0.1 MM |
| SMC_55S | SMBUS_SMC_A_S3_SCL | ST | 0.1 MM |
| SMC_55S | SMBUS_SMC_A_S3_SDA | ST | 0.1 MM |

| SMBus Charger Net Properties | | | | | |
|---|---|---|---|---|
| **NET** | **DESCRIPTION** | **TYPE** | **VALUE** |
| SMC_55S | CHGR_CSI_P | ST | 0.1 MM |
| SMC_55S | CHGR_CSI_N | ST | 0.1 MM |
| SMC_55S | CHGR_CSO_P | ST | 0.1 MM |
| SMC_55S | CHGR_CSO_N | ST | 0.1 MM |

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### Table 1: Physical Constraints

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<tbody>
<tr>
<td>TOP</td>
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<td>0.230 mm</td>
<td>0.091 mm</td>
<td></td>
</tr>
<tr>
<td>BOTTOM</td>
<td>0.145 mm</td>
<td>0.230 mm</td>
<td>0.091 mm</td>
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</tbody>
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### Table 2: Spacing Rules

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<thead>
<tr>
<th>Rule Type</th>
<th>Min. Line Width</th>
<th>Allow Route</th>
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<tr>
<td>Layer 1</td>
<td>0.15 mm</td>
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<tr>
<td>Layer 2</td>
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<tr>
<td>Layer 3</td>
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<td>Layer 5</td>
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<tr>
<td>Layer 6</td>
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</tbody>
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### Table 3: Physical Rule Assignments

<table>
<thead>
<tr>
<th>Area Type</th>
<th>Net Spacing Type 1</th>
<th>Net Spacing Type 2</th>
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</thead>
<tbody>
<tr>
<td>BGA_P1MM</td>
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<td></td>
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<tr>
<td>BGA_P2MM</td>
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<tr>
<td>BGA_P3MM</td>
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</tbody>
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### Table 4: Spacing Assignments

<table>
<thead>
<tr>
<th>Assignment Type</th>
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<tbody>
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### Table 5: Physical Assignments

<table>
<thead>
<tr>
<th>Assignment Type</th>
<th>Assignments</th>
</tr>
</thead>
<tbody>
<tr>
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</table>