### BOMs

<table>
<thead>
<tr>
<th>PART</th>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>630-9210</td>
<td>PCBA, MLB, 1.8GHz, MI 2GB, MU CAP, M82</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>630-9209</td>
<td>PCBA, MLB, 1.8GHz, HY 2GB, TY CAP, M82</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>630-9208</td>
<td>PCBA, MLB, 1.8GHz, HY 2GB, MU CAP, M82</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Bar Code Label / EEE #'s

<table>
<thead>
<tr>
<th>LBL</th>
<th>P/N</th>
<th>LABEL TYPE</th>
<th>SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LBL</td>
<td>28MM X 6MM</td>
<td>PCB, 28MM X 6MM</td>
<td></td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART</th>
<th>DESCRIPTION</th>
<th>REFERENCE TYPE</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>101001</td>
<td>CPU, PRQ_1_8GHZ</td>
<td>CPU_1_8GHZ</td>
<td>CRITICAL</td>
<td>CPU_1_8GHZ</td>
</tr>
<tr>
<td>101011</td>
<td>CPU, PRQ_1_6GHZ</td>
<td>CPU_1_6GHZ</td>
<td>CRITICAL</td>
<td>CPU_1_6GHZ</td>
</tr>
<tr>
<td>101021</td>
<td>CPU, PRQ_1_8GHZ</td>
<td>CPU_1_8GHZ</td>
<td>CRITICAL</td>
<td>CPU_1_8GHZ</td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR</th>
<th>ORIENTATION</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
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<td>101001</td>
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<td>CPU_1_8GHZ</td>
<td>CRITICAL</td>
<td>CPU_1_8GHZ</td>
</tr>
<tr>
<td>101011</td>
<td>CPU, PRQ_1_6GHZ</td>
<td>CPU_1_6GHZ</td>
<td>CRITICAL</td>
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</tr>
<tr>
<td>101021</td>
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<td>CPU_1_8GHZ</td>
<td>CRITICAL</td>
<td>CPU_1_8GHZ</td>
</tr>
</tbody>
</table>

---

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### 1UF 0402 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>SAMSUNG</th>
<th>MURATA</th>
<th>TAIYO YUDEN</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFERENCE DC</td>
<td>CRITICAL</td>
<td>PART NUMBER</td>
</tr>
</tbody>
</table>

#### Critical Capacitors

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Vendor</th>
<th>Description</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2µF</td>
<td>Samsung</td>
<td>SS_CAP_2_2UF</td>
<td>138S0632</td>
</tr>
<tr>
<td>10µF</td>
<td>Samsung</td>
<td>SS_CAP_10UF</td>
<td>138S0633</td>
</tr>
</tbody>
</table>

### 2.2UF 0402 Capacitor Vendor Tables for Acoustics

#### Samsung

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Reference DC</th>
<th>Description</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2µF</td>
<td>SS_CAP_2_2UF</td>
<td>SS_CAP_2_2UF</td>
<td>138S0632</td>
</tr>
<tr>
<td>10µF</td>
<td>SS_CAP_10UF</td>
<td>SS_CAP_10UF</td>
<td>138S0633</td>
</tr>
</tbody>
</table>

#### Murata

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Reference DC</th>
<th>Description</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2µF</td>
<td>MU_CAP_2_2UF</td>
<td>MU_CAP_2_2UF</td>
<td>138S0634</td>
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<tr>
<td>10µF</td>
<td>MU_CAP_10UF</td>
<td>MU_CAP_10UF</td>
<td>138S0635</td>
</tr>
</tbody>
</table>

#### Taiyo Yuden

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Reference DC</th>
<th>Description</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2µF</td>
<td>TY_CAP_2_2UF</td>
<td>TY_CAP_2_2UF</td>
<td>138S0634</td>
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<tr>
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<td>TY_CAP_10UF</td>
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<td>138S0635</td>
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</table>

### 10UF 0603 Capacitor Vendor Tables for Acoustics

#### Samsung

<table>
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<tr>
<th>Capacitor Value</th>
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<tr>
<td>10µF</td>
<td>SS_CAP_10UF</td>
<td>SS_CAP_10UF</td>
<td>138S0633</td>
</tr>
<tr>
<td>10µF</td>
<td>MU_CAP_10UF</td>
<td>MU_CAP_10UF</td>
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</tr>
<tr>
<td>10µF</td>
<td>TY_CAP_10UF</td>
<td>TY_CAP_10UF</td>
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#### Murata

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>10µF</td>
<td>MU_CAP_10UF</td>
<td>MU_CAP_10UF</td>
<td>138S0635</td>
</tr>
<tr>
<td>10µF</td>
<td>MU_CAP_10UF</td>
<td>MU_CAP_10UF</td>
<td>138S0635</td>
</tr>
<tr>
<td>10µF</td>
<td>TY_CAP_10UF</td>
<td>TY_CAP_10UF</td>
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<table>
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<tbody>
<tr>
<td>10µF</td>
<td>TY_CAP_10UF</td>
<td>TY_CAP_10UF</td>
<td>138S0635</td>
</tr>
<tr>
<td>10µF</td>
<td>TY_CAP_10UF</td>
<td>TY_CAP_10UF</td>
<td>138S0635</td>
</tr>
</tbody>
</table>
**"S0, S0M" RAILS**

PP1V25_S0
PPVCORE_S0_NB_GFX

VOLTAGE=1.25V
MAKE_BASE=TRUE

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.4 mm

**"S5" RAILS**

PP1V25_S0
PPVCORE_S0_NB_GFX

VOLTAGE=1.25V
MAKE_BASE=TRUE

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

**"G3H" RAILS**

PP1V25_S0
PPVCORE_S0_NB_GFX

VOLTAGE=1.25V
MAKE_BASE=TRUE

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

**"S3" RAILS**

PP1V25_S0
PPVCORE_S0_NB_GFX

VOLTAGE=1.25V
MAKE_BASE=TRUE

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

**Power Rails**

APPLE INC. D 051-7230
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with XDP-100 adapter board to support DPM, GPM & debugging.

Direction of XDP module to edge of board:

Please avoid any obstructions.
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and Internal Graphics Disable
NOTE: Must keep VDDC_TVDAC powered
VCCD_CRT, VCCD_QDAC and VCC_SYNC.
Can tie the following rails to GND:
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, rails must be filtered except for VCCA_CRT.
All CRT/TVDAC rails must be powered. All
Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can
TV-Out Disable / CRT Enable
should connect to GND through 75-ohm resistors.
omit filtering components. Unused DAC outputs
Component: DACA, DACB & DACC
decoupling. Otherwise, tie VCCD_LVDS to GND also.
If SDVO is used, VCCD_LVDS must remain powered with proper

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Drawn by: [Name]
Checked by: [Name]
Printed by: [Name]

DDR2 Bypassing 1

For use by: [Department]

Omit:

C3400 6.3V 2.2UF 20%
C3401 6.3V 2.2UF 20%
C3402 6.3V 2.2UF 20%
C3403 6.3V 2.2UF 20%
C3404 6.3V 2.2UF 20%
C3405 6.3V 2.2UF 20%

C3410 6.3V 2.2UF 20%
C3411 6.3V 2.2UF 20%
C3412 6.3V 2.2UF 20%
C3413 6.3V 2.2UF 20%
C3414 6.3V 2.2UF 20%
C3415 6.3V 2.2UF 20%

C3420 6.3V 2.2UF 20%
C3421 6.3V 2.2UF 20%
C3422 6.3V 2.2UF 20%
C3423 6.3V 2.2UF 20%
C3424 6.3V 2.2UF 20%
C3425 6.3V 2.2UF 20%

C3430 6.3V 2.2UF 20%
C3431 6.3V 2.2UF 20%
C3432 6.3V 2.2UF 20%
C3433 6.3V 2.2UF 20%
C3434 6.3V 2.2UF 20%
C3435 6.3V 2.2UF 20%

C3440 6.3V 2.2UF 20%
C3441 6.3V 2.2UF 20%
C3442 6.3V 2.2UF 20%
C3443 6.3V 2.2UF 20%
C3444 6.3V 2.2UF 20%
C3445 6.3V 2.2UF 20%

C3450 6.3V 2.2UF 20%
C3451 6.3V 2.2UF 20%
C3452 6.3V 2.2UF 20%
C3453 6.3V 2.2UF 20%
C3454 6.3V 2.2UF 20%
C3455 6.3V 2.2UF 20%

C3490 6.3V 10UF X5R 603 20%
C3491 10UF 6.3V 20% X5R 603
C3492 10UF 6.3V 20% X5R 603

Two caps along package edge

Three caps spread to cover all 8 parts

APPROXIMATE CAP ARRANGEMENT
TWO 0402 CAPS ALONG PACKAGE EDGE

APPROXIMATE CAP ARRANGEMENT

3.3V, 10UF CERM

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APPLE INC.

REV. B.0.0

SIZE

SCALE

DRAWING NUMBER

DDR2 BYPASSING 2

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SYNC_MASTER=MEMORY

C3500 10UF CERM

C3510 2.2UF 0402-LF CERM

C3520 6.3V CERM

C3530 2.2UF 0402-LF CERM

C3540 6.3V CERM

C3550 2.2UF 0402-LF CERM

C3560 6.3V CERM

2 CAPS ALONG PACKAGE EDGE

COLUMN OF THREE CAPS BETWEEN PACKAGES
Micro DVI, USB, to RIO Hatch Assembly

Audio Connector

516S0632

516S0350
near board edge
Place R5001 on bottom side
Silk: "SMC_RST"

R5010
NOSTUFF
402
MF-LF
1/16W
5%

near board edge
Place on bottom side

40
Silk: "PWR_BTN"

R5000
NOSTUFF
402
5%

and the power button is depressed.
generated when left shift, option, and control
of a keyboard SMC Reset
SMC_MANUAL_RST_L in the event
Q5030 will pull down

R5011
CLOSE TO SB

SMC Reset Button / Brownout Detect

SMC 1.05V to 3.3V Level Shifting

SMC 3.3V to 1.05V Level Shifting

SMC AVREF Supply

SMC 3.3V to 1.05V Level Shifting

Battery Pack Status

3.3V to PBUS Level Shifting

SMC SUPPORT

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SMC 3.3V to 1.05V Level Shifting
Place R5101 close to J5100

Place halfway between SPIROM and J5100

Place R5102 close to J5100

Place within 0.5" of SB

5160573

Pullup to internal ROM on S5

SPI_CS MUX

Place halfway between SPIROM and J5100

Place within 0.5" of SB
ACIN VOLTAGE SENSE

- Maximum ACIN = 3.0V
- SMC_PBUS_VSENSE

R5300 and R5301 values chosen for RC filter @ 4.53Kohm

Thevenin Resistance

47k pullup on SMC support page

GPU VOLTAGE SENSE

SMC_GPU_VSENSE

R5310 and C5310 near SMC

PBUS VOLTAGE SENSE

SMC_PBUS_VSENSE

R5350 and C5350 near SMC

Voltage Sensors

Apple Inc.
REMOTE TEMP AT HEAT SPREADER

APN:518S0354

CPU THERMAL DIODE

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 6 MIL TRACK MOUNT AND 3 MIL SPACING BETWEEN THE traces.

LOCAL TEMP NEAR POWER SUPPLIES

(WRITE: 0x9E READ: 0x9F)

(WRITE: 0x90 READ: 0x91)
FAN CONNECTOR
SUDDEN MOTION SENSOR

APN: 338S0354

I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

---

APPLE INC.

501-7230

SYNC_MASTER=M76_MLB
SYNC_DATE=01/12/2007
RENDER VCORE POWER SUPPLY

NOTE: VID<4> is tied to GND

PWM FREQ. = 400kHz
MAX CURRENT = 13A (inductor limit)
1.5V/1.05V POWER SUPPLY

State | PM_SLP_S3_L | PP1V5_S0 | PP1V05_S0
-----|-------------|----------|----------
S0   | HIGH        | 1.5V     | 1.05V    | LOW     | 0.0V    | 0.00V  |
S3/S5/G3Hot | LOW    | 1.5V     | 1.05V   | LOW     | 0.0V    | 0.00V  |

Vout = 0.758V * (1 + Ra / Rb)

Routing Note:
- Use discharge path (VO1) should have a dedicated trace to the output cap; separate from the output voltage sensing trace.
- The discharge path (VO2) should have separate from the output voltage sensing trace.

Note: pu on PGOOD page

1.5V/1.05V Supplies

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APPLE INC.
5V/3.3V Supplies

5V/3.3V POWER SUPPLY

Vout = 1V * (1 + Ra / Rb)
5.106V = 1V * (1 + 20K / 4.87K)

Routing Note:
The discharge path (VO1) should have a dedicated trace to the output cap and separate from the output voltage sensing trace.

Routing Note:
The discharge path (VO2) should have a dedicated trace to the output cap and separate from the output voltage sensing trace.

State | SMC_PM_G2_EN | PPV3V3_G3H | PPV5_S5 | PPV3V2_S5
--- | --- | --- | --- | ---
G3H | LOW | 3.3V | 0.0V | 0.0V
50/53/55 | HIGH | 3.3V | 5.0V | 3.3V

PWM FREQ. = 280 kHz
MAX CURRENT = 6.0A
(inductor limited)
PPV_S5

PWM FREQ. = 430 kHz
MAX CURRENT = 7.8A
(OCF setting limited)
PPV3V2_S5

Part Number

Alternate for Part Number

BOM Option

Ref Des

Comments:

150UF
CRITICAL
POLY
6.3V
CASE-B2-HF
20%

Routing Note:
A dedicated trace to the output cap;
3.425V G3H SUPPLY

Supply needs to guarantee 3.3V delivered to SMC Vref generator. When left shift, option, and control and the power button is depressed, generated a SMC Reset Pulse (P3V42G3H_SHDN_L) in the event Q7730 will pull down Q7730.

1.25V S0 REGULATOR

Vout = 1.25V * (1 + Ra / Rb)

Vout = 1.2516V (3.0A max output)

(Switcher limit)
SST8051 microcontroller for HDCP support
LED Backlight Driver

- ENA does not glitch during RESET.
- PLT_RST_L input ensures backlight.

---

- IN
- IN
- IN

---

- LCDBKLT_PWM_UNBUF
- PP3V3_A_S0
- PPBUS_G3H
- PLT_RST_L
- LCDBKLT_PWREN

---

- R9766
- 1/20W
- 201
- MF
- 0.1UF
- 2
- 1
- 6.3V 10%
- X5R
- 201
- 2
- 1
- R9764
- 2
- 1
- 100K
- 201
- MF
- 1/20W
- 2
- 1
- R9762
- 10K
- 1/20W
- 201
- MF
- 1%
- LCDBKLT_SSTCMP_RC

---

- A
- U9740
- 5
- SOT665

---

- C9762
- 0.01UF
- 0.001UF
- C9763
- CERM
- 20%
- 402
- 402
- 50V
- 10%
- 2
- 1
- C9751
- 2
- C9760

---

- 1UF
- 25V 10%
- X5R
- 201
- 2
- 1
- VOLTAGE=0V
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.5 mm

---

- X5R
- 25V

---

- C9750
- 10UF
- X5R
- 201
- 2
- 1
- 10V
- 10%

---

- L9750
- NC
- NC
- NC

---

- U9750
- PPVOUT_S0_LCDBKLT_SW
- XW9750
- VIN
- QFN

---

- OZ9956ALN
- SWITCH_NODE=TRUE

---

- CRITICAL
- PD3S140XF
- D9750
- R9756
- 78.7K
- 1/20W
- 21
- 1M

---

- 1%
- MF
- 2
- 1
- 2
- 1
- 78.7K
- 1/20W
- 21
- 1M

---

- C9755
- 1
- 1206
- X7R-CERM
- 50V
- 10%
- 2
- 1
- C9756
- 2
- 1
- 50V
- 1206
- X7R-CERM
- 50V
- 10%

---

- C9757
- 4.7UF
- 1206
- X7R-CERM
- 50V
- 10%
- 2
- 1
- C9758
- 4.7UF
- 1206
- X7R-CERM
- 50V
- 10%

---

- C9771
- 1000PF
- X7R
- 16V
- 2
- 1
- C9772
- 1000PF
- X7R
- 16V
- 2
- 1
- C9773
- 4.7UF
- 1206
- X7R-CERM
- 50V
- 10%
- 2
- 1
- C9774
- 1000PF
- X7R
- 16V
- 2
- 1
- C9775
- 201
- 10%
- 2
- 1

---

- OVP Threshold: 37.9V

---

- R9776
- R9775
- R9774
- R9772
- R9771

---

- CRITICAL

---

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---

- SIZE
- SCALE
- NONE

---

- LED Backlight Driver

---

- 051-7230
- APPLE INC.
### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_4MIL</td>
<td>2.5 V ± 375 mV</td>
</tr>
<tr>
<td>FSB_5M5</td>
<td>2.5 V ± 250 mV</td>
</tr>
<tr>
<td>FSB_55S</td>
<td>±550 mV</td>
</tr>
<tr>
<td>FSB_70D</td>
<td>±700 mV</td>
</tr>
<tr>
<td>FSB_80S</td>
<td>±800 mV</td>
</tr>
<tr>
<td>FSB_100D</td>
<td>±1 V</td>
</tr>
<tr>
<td>FSB_120D</td>
<td>±1.2 V</td>
</tr>
<tr>
<td>FSB_150D</td>
<td>±1.5 V</td>
</tr>
<tr>
<td>FSB_180D</td>
<td>±1.8 V</td>
</tr>
<tr>
<td>FSB_220D</td>
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<tr>
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<td>FSB_70D</td>
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<tr>
<td>FSB_80S</td>
<td>±800 mV</td>
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<tr>
<td>FSB_100D</td>
<td>±1 V</td>
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<tr>
<td>FSB_120D</td>
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<tr>
<td>FSB_150D</td>
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<tr>
<td>FSB_180D</td>
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<td>FSB_250D</td>
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### CPU Signal Constraints

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Note: All data is for pin-to-pin tests.

### CPU / FSB Constraints

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</table>

Note: All data is for pin-to-pin tests.

### Design Guide

- Some signals require 27.4-ohm single-ended impedance.
- Design Guide recommends FSB signals be routed only on internal layers.
- Design Guide recommends each strobe/signal group be routed on the same layer.
- Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
- Design Guide does not indicate FSB spacing to other signals, assumed 1:1.
### PCI-Express / DMI Bus Constraints

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

LVDS signals are 100-ohm +/- 20% differential impedance.

- **PCIE_100D** = 100_OHM_DIFF = 100_OHM_DIFF = 100_OHM_DIFF
- **DMI_100D** = 100_OHM_DIFF = 100_OHM_DIFF = 100_OHM_DIFF

### Video Signal Constraints

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112); Sections 6.1 - 6.3.

**Note:** All signal and line spacing values vary by insertion.
- <15 µm: 15 µm from GMi to first transmission receiver.
- >15 µm: 15 µm from second transmission receiver to receiver.

### NB Constraints

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112); Sections 4.1 - 4.3.
### Disk Interface Constraints

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### HD Audio Interface Constraints

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### USB 2.0 Interface Constraints

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Apple Inc.

051-7230

Rev.

D.0.0.0

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### Controller Link (AMT) Constraints

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**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

### Platform LAN (Nineveh) Constraints

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**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

### PCI Bus Constraints

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**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

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**M82 Power and Ground Nets**

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**SCALE:** 051-7230

**SHEET:** OF

**REV.:** B.0.0

**APPLE INC.**
### M82 Board-Specific Spacing & Physical Constraints

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SYNC_MASTER = (MASTER)  
SYNC_DATE = (MASTER)