1. All resistance values are in ohms; 0.1 W max +/- 5%.

## Table of Contents

<table>
<thead>
<tr>
<th>Description</th>
<th>Reference</th>
<th>Part Number</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic/PCB #’s</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
K99 POWER SYSTEM ARCHITECTURE

Need to update!!!
<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>001-1022</td>
<td>1</td>
<td>K99_BOOMEDM1</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1023</td>
<td>1</td>
<td>K99_BOOMEDM2</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1024</td>
<td>1</td>
<td>K99_BOOMEDM3</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1025</td>
<td>1</td>
<td>K99_BOOMEDM4</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1026</td>
<td>1</td>
<td>K99_BOOMEDM5</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1027</td>
<td>1</td>
<td>K99_BOOMEDM6</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1028</td>
<td>1</td>
<td>K99_BOOMEDM7</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001-1029</td>
<td>1</td>
<td>K99_BOOMEDM8</td>
<td>MICRON_2GB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DRAM CFG CHART**

- **Part 1:**
  - PART NUMBER | QTY | DESCRIPTION | REFERENCE | CRITICAL | BOM OPTION
  - 001-1022    | 1   | K99_BOOMEDM1 | MICRON_2GB |          |            |
  - 001-1023    | 1   | K99_BOOMEDM2 | MICRON_2GB |          |            |
  - 001-1024    | 1   | K99_BOOMEDM3 | MICRON_2GB |          |            |
  - 001-1025    | 1   | K99_BOOMEDM4 | MICRON_2GB |          |            |
  - 001-1026    | 1   | K99_BOOMEDM5 | MICRON_2GB |          |            |
  - 001-1027    | 1   | K99_BOOMEDM6 | MICRON_2GB |          |            |
  - 001-1028    | 1   | K99_BOOMEDM7 | MICRON_2GB |          |            |
  - 001-1029    | 1   | K99_BOOMEDM8 | MICRON_2GB |          |            |

- **Part 2:**
  - PART NUMBER | QTY | DESCRIPTION | REFERENCE | CRITICAL | BOM OPTION
  - 001-1030    | 1   | K99_BOOMEDM9 | MICRON_2GB |          |            |
  - 001-1031    | 1   | K99_BOOMEDM10 | MICRON_2GB |          |            |
  - 001-1032    | 1   | K99_BOOMEDM11 | MICRON_2GB |          |            |
  - 001-1033    | 1   | K99_BOOMEDM12 | MICRON_2GB |          |            |
  - 001-1034    | 1   | K99_BOOMEDM13 | MICRON_2GB |          |            |
  - 001-1035    | 1   | K99_BOOMEDM14 | MICRON_2GB |          |            |
  - 001-1036    | 1   | K99_BOOMEDM15 | MICRON_2GB |          |            |
  - 001-1037    | 1   | K99_BOOMEDM16 | MICRON_2GB |          |            |

**NOT TO REPRODUCE OR COPY IT**

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<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>341T0262</td>
<td>1</td>
<td>CRITICAL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>341T0263</td>
<td>1</td>
<td>CRITICAL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>335S0610</td>
<td>1</td>
<td>U6100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>155S0329</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>155S0457</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>138S0673</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>138S0671</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>107S0075</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>104S0018</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>104S0023</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0586</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0516</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0874</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>K99_MISC</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

BOM Configuration

Apple Inc. 051-8379 4.4.0
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V TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
### CPU VCore HF and Bulk Decoupling

<table>
<thead>
<tr>
<th>Layout Note</th>
<th>Place opposite side of CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Critical</td>
<td>C1200</td>
</tr>
<tr>
<td>Critical</td>
<td>C1201</td>
</tr>
<tr>
<td>Critical</td>
<td>C1202</td>
</tr>
<tr>
<td>Critical</td>
<td>C1203</td>
</tr>
<tr>
<td>Critical</td>
<td>C1204</td>
</tr>
<tr>
<td>Critical</td>
<td>C1205</td>
</tr>
<tr>
<td>Critical</td>
<td>C1206</td>
</tr>
<tr>
<td>Critical</td>
<td>C1207</td>
</tr>
<tr>
<td>Critical</td>
<td>C1208</td>
</tr>
<tr>
<td>Critical</td>
<td>C1209</td>
</tr>
</tbody>
</table>

### CPU VCore VID Connections

<table>
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<tr>
<th>VCCA (CPU AVdd) Decoupling</th>
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<tbody>
<tr>
<td>Place C1290 close to CPU</td>
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</table>

<table>
<thead>
<tr>
<th>VCCP (CPU I/O) Decoupling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Place C1293 close to CPU</td>
</tr>
</tbody>
</table>

### CRITICAL Notes

- Place M1 on opposite side of CPU
- Place C1289-1290 close to CPU side
- Place C1291-1292 close to pin 84 of CPU0

**VCCP (CPU AVdd) DECOUPLING**

- Place C1290 close to CPU

**VCCP (CPU I/O) DECOUPLING**

- Place C1290 close to CPU

---

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**Drawing Number Size:**

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www.vinafix.vn
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with X60-0742 Adapter Flex to support chipset debug.

Direction of XDP adapter flex

Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.

NOTE: XDP pinout is not the standard.

Use with 920-0782 Adapter Flex to support chipset debug.

PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1

PE1 ports are Gen1-only. 2 RCs: x1, x1

+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[3:0] are not used, +VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

If PE0[4:5] and PE1[0:1] are not used, +VIO_PLL_HVDD can be GND

2 RCs: x1, x1


Connect RGMII_RESET* to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
Connect RGMII_MDC to 10K pull-down.
Connect RGMII_TXD<0:3> together to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXD2 to 10K pull-down.
Connect RGMII_RXD1 to 10K pull-down.
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
Connect RGMII_RXD<1> to 10K pull-down.
Connect RGMII_RXD<3> to 10K pull-down.
Connect RGMII_RXD<2> to 10K pull-down.
Connect RGMII_COMP_VDD to 10K pull-down.
Connect RGMII_COMP_GND to 10K pull-down.
Connect RGMII_TXD3 to 10K pull-down.
Connect RGMII_TXD2 to 10K pull-down.
Connect RGMII_TXD0 to 10K pull-down.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDC to 10K pull-down.
Connect RGMII_TXD<2> to 10K pull-down.
Connect RGMII_TXD<0> to 10K pull-down.
Connect RGMII_TXD<1> to 10K pull-down.
Connect RGMII_TXD<3> to 10K pull-down.
Connect RGMII_TXD<5> to 10K pull-down.
Connect RGMII_TXD<6> to 10K pull-down.
Connect RGMII_TXD<7> to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_COMP_VDD/_GND must remain connected as shown.
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_INTR/GPIO_35 to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_RXD2 to 10K pull-down.
Connect RGMII_RXD1 to 10K pull-down.
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
Connect RGMII_RXD<1> to 10K pull-down.
Connect RGMII_RXD<3> to 10K pull-down.
Connect RGMII_RXD<2> to 10K pull-down.
Connect RGMII_MDC to 10K pull-down.
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Connect RGMII_RXD1 to 10K pull-down.
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Connect RGMII_RXD<1> to 10K pull-down.
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Connect RGMII_RXD<2> to 10K pull-down.
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Connect RGMII_TXD3 to 10K pull-down.
Connect RGMII_TXD2 to 10K pull-down.
Connect RGMII_TXD0 to 10K pull-down.
Connect RGMII_VREF to 10K pull-down.
Current numbers from MCP89_A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

NOTE: "SW" rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless VDD_COREA/VDD_COREB are powered by separate regulators. Instead connect regulator sense point as close to COREB FET as possible.
Q2300 helps reduce input rail droop during Q2300 turn-on.

**MCP89 Memory Rail Gating**

- NO STUBS on CKE signals!

**DIMM CKE Clamps**

- CKE must be held low to keep memory in self-refresh.

Clamps enable after MCP89 MEMVDD rail switched off. Clamps release after MEMVDD rail is up and CKEs are driven by MCP89.

- NO STUBS on CKE signals!

- Approx. Ramp Time (EN to 1.35V, μS): 7.91 + 0.0678 * R1(Kohms)

- Gated Rail Savings: 120mW

**NV Requirements:**

- Min Ramp-Up Time: 20 μS (10% to 90%)
- Max Ramp-Up Time: 65 μS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

- Loading (G driven to VCC)

C2300 helps reduce input rail droop during Q2300 turn-on.

- NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

- Max Ramp-Up Time: 65 μS (ENABLE to 90%)

- Loading (G driven to VCC)

C2300 helps reduce input rail droop during Q2300 turn-on.
Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- Min Ramp-Up Time: 100 uS (10% to 90%)
- FET Ron <= 2.5 mOhms
- Gated Rail Savings: 860mW

C2400 helps reduce input rail drop during GFX fast-ramp:

Max Ramp-Up Time: 1500 uS (ENABLE to 90%)

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

C2405 helps reduce input rail drop during GFX fast-ramp:

Max Ramp-Up Time: 1500 uS (ENABLE to 90%)

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DRP BANK CONTROL
JEDEC recommends 30 Ohm term to VTT for CS, CKE, ODT and 36 Ohm for BA, A, RAS, CAS, WE.
**DCIN (AMON) Current Sense, RMUX & Filter**

- **ISL6259 Gain:** 20x
  - SENSE R: R7525, 1mOhm
  - MAX Vdiff = 24.8mV
  - From charger, SW6-1
  - Value: 20 mOhm
  - MAX VOUT: 1.24V
  - GAIN: 200x
  - Scale: 2.778A / V
  - Gain: 20x
  - SCALE: 1A / V
  - Gain: 36x

- **Battery (BMON) Current Sense, MUX & Filter**
  - GAIN: 36x
  - Scale: 2.778A / V
  - Gain: 50x
  - SCALE: 1A / V
  - Place close to SMC

- **Chipset Regulators High-Side Current Sense / Filter**
  - Place close to SMC

- **MCP MEM VDD Current Sense / Filter**
  - Place close to SMC

**VERIFY ALL RESISTOR AND GAINS**

**CPU VCore Load Side Current Sense / Filter**

**NOTE:** Do not stuff R5415 and R7593 at the same time!
FAN CONNECTOR

- PP5V_G0_FAN
- PP312_G0_FAN
- 5V GND
- FAN_RTL_TACH

R5660

100K

201

47K

1/20W 5%

2

R5661

5V DC TACH MOTOR CONTROL GND

2

1

R5665

J5600

FF14A-4C-R11DL-B-3H F-RT-SM

Q5660

SOD-VESM-HF SSM3K15FV

5180793

CRITICAL
IMVP6 CPU VCORE REGULATOR

OCP = 21.5MV / R7480 + 3.1A
VPMON = 90 X R7480 X VO X I0
18A @ 3V = 1.62V
LOAD LINE = R7480 X 6 / (500U X R7414)
NOTE: Pulled up to 5V on DP connector page.

FET spec'd for 1.5V Vgs operation.

Q9302
SIGNAL_MODEL=DP_AUXCH_FET
SSM6N37FEAPE
SOT563
CKPLUS_WAIVE=PdifPr_badTerm

Q9300
SIGNAL_MODEL=DP_AUXCH_FET
SSM6N37FEAPE
SOT563

C9301
3300PF
10%
10V
X7R

R9302
MF
1/20W
5%
201
22

External DisplayPort Support
SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

DP_EXT_AUX_CH_N
DP_CA_DET
DP_AUX_CH_C_P
DP_EXT_DDC_DATA
DP_CA_DET_RC
DP_AUX_CH_C_N
DP_EXT_DDC_CLK
DP_EXT_AUX_CH_P
Port Power Switch

Source resistance of > 5 MOhm. leakage of < 500 nA and gate to source resistance of ≥ 5 MΩ.

DP Source must pull-up to DP_PWR.
**CPU/FSB Constraints**

**FSB (Front-Side Bus) Constraints**

**CPU Net Properties**

**MCP FSB COMP Signal Constraints**

**FSB Clock Constraints**

**CPU Clock Constraints**

**Intel Design Guide** recommends FSB signals be routed only on internal layers.

**CPU Clock Constraints**

**CPU Signals**

**Intel Design Guide** recommends FSB signals be routed only on internal layers.

**Source:** MCP89 Interface DS (000-04625-001_v0.9), Section 2.1.4

**Intel Design Guide** recommends FSB signals be routed only on internal layers.

**Source:** Santa Rosa Platform DS, Rev 1.5 (#22294), Sections 4.2 & 4.3

**Intel Design Guide** recommends FSB signals be routed only on internal layers.

**Source:** Apple Inc.
Memory Constraints

**MCP_MEM_COMP Signal Constraints**

- CMD/CTRL signals should be matched within 150 ps.
- CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
- No DQS to clock matching requirement.

**MCP_MEM_COMP Signal Constraints**

- Memory Bus Spacing Group Assignments

  - MEM_70D = STANDARD
  - MEM_55S = STANDARD
  - MEM_2OTHER = 25 MIL
  - MEM_DATA = 70_OHM_DIFF
  - MEM_CMD = 70_OHM_DIFF
  - MEM_CTRL = 4:1_SPACING
  - MEM_CLK = 4:1_SPACING
  - MEM_A_DM = 2x_DIELECTRIC
  - MEM_DQ = 3:1_SPACING

**Memory Net Properties**

- Memory Bus Spacing Group Assignments

  - Table of Spacing Assignments

<table>
<thead>
<tr>
<th>Table Item</th>
<th>Table Item</th>
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<th>Table Item</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_DATA</td>
<td>MEM_CMD</td>
<td>MEM_CTRL</td>
<td>MEM_CLK</td>
<td>MEM_A_DM</td>
</tr>
<tr>
<td>MEM_DATA</td>
<td>MEM_CMD</td>
<td>MEM_CTRL</td>
<td>MEM_CLK</td>
<td>MEM_A_DM</td>
</tr>
<tr>
<td>MEM_DATA</td>
<td>MEM_CMD</td>
<td>MEM_CTRL</td>
<td>MEM_CLK</td>
<td>MEM_A_DM</td>
</tr>
<tr>
<td>MEM_DATA</td>
<td>MEM_CMD</td>
<td>MEM_CTRL</td>
<td>MEM_CLK</td>
<td>MEM_A_DM</td>
</tr>
</tbody>
</table>

**MCP_MEM_COMP GND**

- Memory Constraints

  - Apple Inc.
  - Sheet 051-8379 4.4.0

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NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

Digital Video Signal Constraints

SATA Interface Constraints

PCI-Express

SOURCE: MCP9 Interface DD (MCP9_IFPAB_v0.9), Section 2.3

MCP89 Net Properties

SOURCE: MCP9 Interface DD (MCP9_IFPAB_v0.9), Section 2.4.2

Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.

MCP9 Interface DD (MCP9_IFPAB_v0.9), Section 2.6

Max trace length: LVDS 10 inches, DP 8.5 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

Digital Video Signal Constraints

Analog Video Signal Constraints

MCP89 Net Properties

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
### SPI Interface Constraints

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

<table>
<thead>
<tr>
<th>NET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR</th>
<th>PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SIO Signal Constraints

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

<table>
<thead>
<tr>
<th>NET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR</th>
<th>PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### USB 2.0 Interface Constraints

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

<table>
<thead>
<tr>
<th>NET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR</th>
<th>PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### HD Audio Interface Constraints

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

<table>
<thead>
<tr>
<th>NET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR</th>
<th>PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SMBus Interface Constraints

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

<table>
<thead>
<tr>
<th>NET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR</th>
<th>PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### MCP89 Net Properties

<table>
<thead>
<tr>
<th>NET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR</th>
<th>PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table:**
- **LINE-TO-LINE SPACING:**
  - **LAYER:**
  - **SPACING RULE SET:**
  - **WEIGHT:**
- **MINIMUM LINE WIDTH:**
- **ALLOW ROUTE:**
- **TABLE PHYSICAL RULE ITEM:**
- **TABLE PHYSICAL RULE HEAD:**
- **TABLE PHYSICAL RULE ITEMS:**

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- **II:** Not to reproduce or copy it
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### SD Card Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraint Set</th>
<th>Min Width</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Diff-Pair Primary Gap</th>
<th>Diff-Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD_55S</td>
<td>SD INTERFACE</td>
<td>12 MIL</td>
<td>7.5 MIL</td>
<td>7.5 MIL</td>
<td>100 OHM DIFF</td>
<td>100 OHM DIFF</td>
</tr>
</tbody>
</table>

### RGMII Net Properties

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Min Width</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Diff-Pair Primary Gap</th>
<th>Diff-Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>RGMII</td>
<td>100 OHM</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
</tr>
</tbody>
</table>

### Ethernet Net Properties

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Min Width</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Diff-Pair Primary Gap</th>
<th>Diff-Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENET_MII</td>
<td>55 OHM</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
</tr>
</tbody>
</table>

### SD Card Net Properties

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Min Width</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Diff-Pair Primary Gap</th>
<th>Diff-Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD_INTERFACE</td>
<td>55 OHM</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
<td>55 OHM SE</td>
</tr>
<tr>
<td>NET_TYPE</td>
<td>NET_TYPE</td>
<td>PHYSICAL_SPACING</td>
<td>PHYSICAL_SPACING</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------------------------------</td>
<td>------------------------</td>
<td>------------------</td>
<td>------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SDA</td>
<td>SMBUS_SMC_BSA_SCL</td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>SMBUS_SMC_0_S0_SDA</td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_CSI_P</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_CSI_N</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_CSO_R_P</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_CSO_R_N</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_CSO_P</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMBUS_CSI_R_N</td>
<td></td>
<td>0.50</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SMC Constraints**

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10 OF 13

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### SD CARD READER LAYOUT RELAXATIONS

<table>
<thead>
<tr>
<th>Net</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Diff Pair</th>
<th>Primary Gap</th>
<th>Diff Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### MCP Fanout Constraint relaxations

<table>
<thead>
<tr>
<th>Net</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Diff Pair</th>
<th>Primary Gap</th>
<th>Diff Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Misc Net Properties

- **Net**
- **Position**
- **Properties**
  - **Electrical Constraint Set**
    - **Physical**
  - **Spacing**
  - **Net Type**

### Power Net Properties

- **Net**
- **Position**
- **Properties**
  - **Electrical Constraint Set**
    - **Physical**
  - **Spacing**
  - **Net Type**

### Graphics Net Properties

- **Net**
- **Position**
- **Properties**
  - **Electrical Constraint Set**
    - **Physical**
  - **Spacing**
  - **Net Type**

### Audio Net Properties

- **Net**
- **Position**
- **Properties**
  - **Electrical Constraint Set**
    - **Physical**
  - **Spacing**
  - **Net Type**

### Table of Spacing Assignments

<table>
<thead>
<tr>
<th>Net</th>
<th>Layer</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Diff Pair</th>
<th>Primary Gap</th>
<th>Diff Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS**

<table>
<thead>
<tr>
<th>TABLE BOARD_INFO</th>
<th>TABLE_Physical_rule_HEAD</th>
<th>TABLE_Physical_rule_ITEM</th>
</tr>
</thead>
</table>

**BOARDertime:**

- **8 7 5 4 2 1**

**K99 RULE DEFINITIONS**

- **Apple Inc.**

- **058-8379 - 1**

- **109 of 110**

-. 12 of 33

---

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<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>REFERENCE DES</th>
<th>OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>138S0632</td>
<td>10</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>CRITICAL</td>
<td>SS_CAP_2_2UF</td>
<td></td>
</tr>
<tr>
<td>138S0625</td>
<td>8</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>CRITICAL</td>
<td>SS_CAP_2_2UF</td>
<td></td>
</tr>
<tr>
<td>138S0629</td>
<td>10</td>
<td>CAP, 22UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641</td>
<td></td>
</tr>
<tr>
<td>138S0633</td>
<td>10</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>CRITICAL</td>
<td>C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939</td>
<td></td>
</tr>
<tr>
<td>138S0634</td>
<td>10</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>CRITICAL</td>
<td>C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296</td>
<td></td>
</tr>
</tbody>
</table>

**MURATA**

**TAIYO YUDEN**

---

**10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>REFERENCE DES</th>
<th>OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>138S0642</td>
<td>9</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>SS_CAP_10UF</td>
<td></td>
</tr>
<tr>
<td>138S0644</td>
<td>8</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>SS_CAP_10UF</td>
<td></td>
</tr>
<tr>
<td>138S0645</td>
<td>8</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>SS_CAP_10UF</td>
<td></td>
</tr>
</tbody>
</table>

---

**22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>REFERENCE DES</th>
<th>OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>138S0643</td>
<td>5</td>
<td>CAP, 22UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>SS_CAP_22UF</td>
<td></td>
</tr>
<tr>
<td>138S0645</td>
<td>5</td>
<td>CAP, 22UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>SS_CAP_22UF</td>
<td></td>
</tr>
<tr>
<td>138S0647</td>
<td>4</td>
<td>CAP, 22UF, 6.3V, 20%, 0603</td>
<td>CRITICAL</td>
<td>SS_CAP_22UF</td>
<td></td>
</tr>
</tbody>
</table>

---

**SS_CAP_2_2UF**

**SS_CAP_10UF**

**SS_CAP_22UF**

---

**DESCRIPTION REFERENCE DES BOM OPTION QTYPART NUMBER CRITICAL**

**DESCRIPTION REFERENCE DES BOM OPTION QTYPART NUMBER CRITICAL**

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**Acoustic Cap BOM Config Tables**

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