Table of Contents

1. Integration Issues to be Resolved
   - SMF
   - Front Flex Support
   - External USB Connectors
   - SATA Connectors
   - FireWire Ports
   - FireWire Port Power
   - Ethernet PHY (RTL8211CL)
   - SECUREDIGITAL CARD READER
   - SB Misc
   - MCP Graphics Support
   - MCP Standard Decoupling
   - MCP SATA & USB
   - eXtended Debug Port (MiniXDP)
   - CPU Decoupling
   - Signal Aliases

2. Revision History
   - Power Block Diagram
   - System Block Diagram
   - Contents Sync

3. All Capacitance Values are in Microfarads.
4. All Crystal & Oscillator Values are in Hertz.

5. Constraints
   - Ethernet
   - Memory
   - CPU/FSB
   - LCD Backlight Driver (MC34845)
   - DISPLAYPORT SUPPORT
   - POWER SEQUENCING
   - CPU VTT Power Supply
   - MCP CORE REGULATOR
   - AUDIO:SPEAKER AMP
   - AUDIO: HEADPHONE FILTER
   - AUDIO: LINE INPUT FILTER
   - AUDIO: CODEC/REGULATOR
   - DEBUG SENSORS AND ADC
   - WELLSPRING 2
   - WELLSPRING 1
   - Fan
   - Thermal Sensors
   - Current Sensing
   - K19i SMBus Connections

6. Metric
   - Size
   - Drawing Number
   - Date
   - MFG APPD
   - ENG APPD
   - NOTICE OF PROPRIETARY PROPERTY

7. SCALE
   - NOTED AS
   - X.XXX
   - DO NOT SCALE DRAWING
   - METRIC

8. Notice of Patent
   - a.k.a. K19i
   - 4/24/2009
   - PVT
   - a.k.a. K19
   - 4/2009

9. Apple Inc.
   - Master of Proprietary Property
   - OSL-7903-A
   - A
### BOM Variant

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>830-1771</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>128-1771</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BOM Groups

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>830-1771</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>D/F</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>27300K421</td>
<td></td>
<td>CPU_2_0GHZ</td>
<td></td>
<td>CRITICAL</td>
<td>PDC,SLGE3,PRQ,2.00,25W,1066,R0,3M,BGA</td>
</tr>
<tr>
<td>1337S3693</td>
<td></td>
<td>CPU_2_26GHZ</td>
<td></td>
<td>CRITICAL</td>
<td>PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA</td>
</tr>
</tbody>
</table>

### Programmable Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>D/F</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3641</td>
<td></td>
<td>CPU_2_53GHZ</td>
<td></td>
<td>CRITICAL</td>
<td>PDC,SL3BX,PRQ,2.5,35W,1066,C0,6M,BGA</td>
</tr>
<tr>
<td>1338S0694</td>
<td></td>
<td>U3700 CRITICAL</td>
<td></td>
<td>IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P</td>
<td></td>
</tr>
<tr>
<td>341S2460</td>
<td></td>
<td>IC,PRGRM,SMC EXTERNAL</td>
<td></td>
<td>SMC_PROG</td>
<td></td>
</tr>
</tbody>
</table>

### Development BOM

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>D/F</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>065-1771</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>D/F</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>152S0586</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0847</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0516</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0874</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0778</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0693</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Bar Code Label / EEE #

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>D/F</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>830-1771</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BOM Configuration

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>D/F</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>830-1771</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CHANGE C1240-C1243 AND C1260 FROM 128S0241 (9 MILLI-OHM) TO 128S0231 (6 MILLI-OHM)

REMOVE NO STUFF CAPS C1220 TO C1231

SYNC FROM T18

CPU Decoupling

VCCA (CPU AVdd) DECOUPLING
1x 10uF, 1x 0.1uF

VCCP (CPU I/O) DECOUPLING
1x 330uF, 1x 0.1uF 0602

PLACEMENT_NOTE= Place C1260 between CPU & NB.
1x 330uF, 6x 0.1uF 0402
1x 10uF, 1x 0.01uF

VCCA (CPU AVdd) DECOUPLING

PLACEMENT_NOTE= Place C1240-C1243:
Place inside socket cavity on secondary side.

PLACEMENT NOTE (C1200-C1219):
4X 330UF, 20X 22UF 0805

CPU Decoupling
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
See with XDP-300 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

NOTE: This is not the standard XDP pinout.
Please avoid any obstructions
on even-numbered side of J1300
Current numbers from email Ponnacha Kongetira provided 11/30/2007 4:04pm (no official document number).
RTC Power Source

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

System Reset Circuit

Platform Reset Connections

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

MCP S0 PWRGD & CPU_VLD

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. To maintain the Document in Confidence.
II. Not to reproduce or copy it.
III. Not to reveal or publish in whole or part.

PLACEMENT_NOTE=Place close to U1400

PLACEMENT_NOTE=Place R2897 on BOTTOM

SYNC_DATE=01/06/2009
SYNC_MASTER=WFERRY_K19I

REV.

D A B C
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e., not simultaneously) due to current limitation of TPS51116 regulator.
DDR3 RESET Support

Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

1. VDD MEM_RESET_L must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
2. PP3V3_S5 is used because MEM_RESET must be high before 1.5V starts to rise.

MCPCB Component List

- **R3300**: 10K ohm, 5%, 1/16W MF-LF
- **R3301**: 20K ohm, 5%, 1/16W MF-LF
- **R3309**: 1K ohm, 5%, 1/16W MF-LF
- **R3310**: 100K ohm, 5%, 1/16W MF-LF
- **C3300**: 0.1μF, 20%, CERM

**Notes:**
- DDR3 RESET Support
- PP3V3_S5 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
- PP1V5_S3 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
### 3.3V ENET FET

- **AP_PWR_EN AC_OR_S0_L**
- **SMC_ADAPTER_EN**
- **PM_SLP_S3_L**
- **PM_SLP_RMGT_L**

### 1.05V ENET FET

- **RTL8211_CLK25M_CKXTAL1**
- **P3V3ENET_SS**
- **P1V05ENET_EN_L**
- **P1V05ENET_SS**

### WLAN Enable Generation

- **WLAN Enable Generation**

### RTL8211 25MHz Clock

- **NOTE:** MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
- **Designs must ensure SMPS is powered whenever RMGT rails are, or use separate crystal.**

### Ethernet & AirPort Support

- **Ethernet & AirPort Support**

---

**NOTE:** MPCI can provide 32MHz clock, but clock runs whenever SMPS rails are powered. Designs must ensure SMPS is powered whenever SMPS rails are, or use separate crystal.
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II. NOT TO REPRODUCE OR COPY IT
III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

Transformers should be mirrored on opposite sides of the board.

Placement Note: Place one of 0.1uf cap close to each center tap pin of transformer.

---

Ethernet connector placement:

- ENET_MDI_P<0>
- ENET_MDI_N<0>
- ENET_MDI_P<1>
- ENET_MDI_N<1>
- ENET_MDI_P<2>
- ENET_MDI_N<2>
- ENET_MDI_P<3>
- ENET_MDI_N<3>

---

CRITICAL:

C3900
C3901
C3902
C3903

---

MIN_NECK_WIDTH = 0.25 mm
MIN_LINE_WIDTH = 0.6 mm
NOTE: FireWire TPA/TPB pairs are NOT
assumed that FireWire PHY page will
the necessary aliases to map the
FireWire (10/100) ports to proper
appropriate connections and to
properly terminate output signals.

Place close to FireWire PHY

Port "1" Bilingual (1394B)
- Port 1 Portable Power Class (0)
Configures PHY for:

Port Notes

Termination
Place close to FireWire PHY

Cable Power

Late-VG Protection Power

FireWire Ports

Apple Inc. D 031-7903 A
We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

Left USB Port B

Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

External USB Connectors
Alternate SPI ROM Support

SPI MUX BYPASS

LPC+SPI Connector

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: NOT TO REPRODUCE OR COPY IT; NOT TO REVEAL OR PUBLISH IN WHOLE OR PART; TO MAINTAIN THE DOCUMENT IN CONFIDENCE.
CPU Voltage Sense / Filter

MCP Voltage Sense / Filter

FBUS VOLTAGE SENSE ENABLE & FILTER

PLACEMENT_NOTE=Place near U1400 center

SMC_MCP_VSENSEMCPVSENSE_IN

PPBUS_G3H

PPBUS_G3HRS5_VSENSE

GBUS_VSENS_EN_L_DIV

PM_SLP_S3_L_BUF

VOLTAGE=18.5V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.20 mm

PLACEMENT_NOTE=Place near U1000 center
**CPU T-Diode Thermal Sensor**

- **INTERNAL DIODE IN U5515 DETECTS CPU PROXIMITY TEMPERATURE**
- **PLACEMENT NOTE:** PLACE U5515 NEAR CPU

**MCP T-Diode Thermal Sensor**

- **INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE**
- **PLACEMENT NOTE:** PLACE U5535 NEAR MCP

REPLACED 518S0521 WITH 518S0519
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

NOTICE OF PROPRIETARY PROPERTY
Analog SMS

R5921 pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC.

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation:

Sudden Motion Sensor (SMS)

SYNC_DATE=02/05/2009
SYNC_MASTER=K19_MLB
MAKE_BASE=TRUE
SMS_PWRDN
SMS_SELFTEST
PP3V3_S3
**Drawing Number:**

**Debug Sensors and ADC**

**Apple Inc.**

**COPYRIGHT & TRADEMARK NOTICE**

The information contained herein is the proprietary property of Apple Inc. The possession or use of this information in whole or in part by anyone other than Apple Inc. is strictly prohibited except with the express written consent of Apple Inc. No part of this information may be copied, reproduced or distributed in any manner without the express written consent of Apple Inc.

**1. Place NEAR Q4590:**

- **R6074:** 226K Ω, MF-LF, 1/16W, 1%
- **C6040:** 2.2μF, X5R, 6.3V, 20%

**2. Place NEAR U6050:**

- **U6050:** INA210
- **R6050:** 348K Ω
- **C6000:** 0.1μF, 10V, CERM
- **C6001:** 470PF

**3. Place RC NEAR U6000:**

- **R6033:** 1M Ω
- **R6021:** 681K Ω
- **R6051:** 47.0K Ω

**4. Place RC NEAR Q3450:**

- **R6041:** 1% 1/16W
- **C6040:** 2.2μF, X5R, 6.3V, 20%

**5. Place RC NEAR U6000:**

- **R6034:** 226K Ω
- **C6003:** 10μF, 603, 20%

**6. Place RC NEAR U6000:**

- **C6050:** 0.1μF, 10V, CERM

**Notes:**

- **DEBUG_ADC**
- **PLACEMENT_NOTE=PLACE NEAR Q4590**
- **PLACEMENT_NOTE=PLACE NEAR U6000**

**References:**

- **IN**
- **OUT**
- **IN-**
- **GND**
- **V+**
- **V-**
- **THRM**
- **CERM**
- **MF-LF**
- **1%**
- **1/16W**
- **50V10%**
- **50V**
- **50VCERM402**
- **1M**
- **2.2UF**
- **402**
- **6.3V10%**
- **X5R6.3V10%**
- **5%1/16W**
- **10%**
- **CERM402**
- **51**
- **51**
- **10V**
- **470PF**
- **ADC_SDA**
- **ADC_SCL**
- **ADC_VREF**
- **ADC_REFCOMP**
- **ADC_METHOD**
- **ADC_RANGE**
- **ADC_GAIN**
- **I2C_ADDRESS**
- **LSB**
- **DVDD**
- **AVDD**
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 Hz.
VIN = 2VRMS, CODEC VIN = 1.21 VRMS

FC = 8 Hz
NET RIN = 20K OHMS

AUDIO: LINE INPUT FILTER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

CRITICAL
3.3UF
CERM-X5R805-1
10%
10V
C6301
1 2

CRITICAL
3.3UF
CERM-X5R805-1
10%
10V
C6302
1 2

CRITICAL
3.3UF
CERM-X5R805-1
10%
10V
C6311
1 2

CRITICAL
3.3UF
CERM-X5R805-1
10%
10V
C6312
1 2

CRITICAL
NOSTUFF
15PF
CERM402
5%
50V
C6303
1 2

CRITICAL
NOSTUFF
15PF
CERM402
5%
50V
C6313
1 2

57 57
57

402MF-LF
1%
6.04K
1/16W
R6301
1 2

402MF-LF
1%
6.04K
1/16W
R6311
1 2

16.5K
402MF-LF
1/16W
1%
R6312
1

16.5K
402MF-LF
1/16W
1%
R6302
1

10
402
R6300
1 2
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER
3X MONO SPEAKER AMPLIFIERS (SSM2315)
APR: 35322500
GAIN = 6DB
1ST ORDER FC (LAR) = 120 Hz +/- 30%
1ST ORDER FC (SUB) = 50Hz +/- 30%

SPKRCONN_L_OUT_N
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRCONN_L_OUT_P
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRCONN_S_OUT_N
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRCONN_S_OUT_P
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRCONN_R_OUT_N
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRCONN_R_OUT_P
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRAMP_L_OUT_N
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRAMP_L_OUT_P
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRAMP_R_OUT_N
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

SPKRAMP_R_OUT_P
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM

AUD_GPIO_3
AUD_LO2_N_L AUD_LO2_P_L AUD_SPKRAMP_INP_L

PP5V_S3_AUDIO_AMP
FERR-1000-OHM
L6601
L6611
L6621
L6631

CRITICAL
R6601
R6611
R6621
R6631
R6630
R6620
R6632

CRITICAL
C6610
C6620
C6630
C6611
C6621
C6631
C6632

CRITICAL
C6613
C6622
C6633

CRITICAL
402X5R16V10%
CERM402
10V
10%

CRITICAL
402MF-LF
1/16W
5%

CRITICAL
402
16V
X5R
10%

CRITICAL
CERM402
10V
10%

CRITICAL
402
10%
X5R

CRITICAL
47UF
6.3V
20%

CRITICAL
100UF
47UF
6.3V
20%

CRITICAL
3X MONO SPEAKER AMPLIFIERS (SSM2315)

PLACE C6630 CLOSE TO VDD PIN
MagSafe DC Power Jack

1-Wire OverVoltage Protection

The chassis ground will otherwise float and not send transients onto ADAPTER_SENSE when AC is connected.

3.425V "G3Hot" Supply

Supply made to guarantee 3.42V delivered to SMC that generator

DC-In & Battery Connectors

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. NOT TO REPRODUCE OR COPY IT

APPLE INC.

SYNC_MASTER=K19_MLB
SYNC_DATE=03/18/2009

NOT TO MAINTAIN THE DOCUMENT IN CONFIDENCE
NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
NOT TO REPRODUCE OR COPY IT

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. NOT TO REPRODUCE OR COPY IT

APPLE INC.
The image contains a schematic diagram of a power supply and battery charger circuit. The diagram includes various components and connections, with labels for each part, such as resistors (R1, R2, R3, etc.), capacitors (C1, C2, C3, etc.), and power-related components like Q7000, Q7001, and Q7002. The diagram provides a detailed view of the circuitry, showing how different parts are connected and their functions within the system.
Vout = 1.052V

M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.
### COP Signal Constraints

- **FSB Clock Constraints**
  - Signals within each 4x group should be matched within 5 ps of strobe.
- **CPU Clock Constraints**
  - spacing in 1x dielectric between DATA#, DIVY signals, with 3x dielectric spacing to the DIVXs.
  - Design Guide recommends each strobe/signal group is routed on the same layer.

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Constraint</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_CPU_N</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB_CLK_CPU_P</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty()</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
<tr>
<td>FSB.isNullOrEmpty().</td>
<td>=50_OHM_SE</td>
<td>MCP_50S</td>
</tr>
</tbody>
</table>

### CPU / FSB Constraints

- **Signal Constraints**
  - Some signals require 27.4-ohm single-ended impedance.
  - Most CPU signals with impedance requirements are 55-ohm single-ended.

### Notes

- 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.
- 8 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.
- CPU/VCCSENSE signals are routed on 1x dielectric.
- MCP FSB Comp signals are routed on 2x dielectric.
- MCP FSB signals with impedance requirements are 55-ohm single-ended.

### Sources

- FSB Clock Constraints: Section 2.2
- CPU Signal Constraints: Sections 4.2 & 4.3
- CPU / FSB Net Properties: Section II.6
- CPU FSB Clock Constraints: Section II.6
- CPU FSB Net Properties: Section II.6
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
All DQS pairs should be matched within 100 ps of clocks.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

Use to support MEM_70D-style wildcards:

MEM_DATA, MEM_40S, MEM_A_DQ<47..40>, MEM_A_DQ<7..0>, MEM_A_DQS0, MEM_A_DQS1, MEM_A_DQS2, MEM_A_DQS3, MEM_A_DQS4, MEM_A_DQS5, MEM_A_DQS6, MEM_A_DQS7, MEM_B_A<14..0>, MEM_B_BA<2..0>, MEM_B_CAS_L, MEM_B_CNTL, MEM_B_CLK, MEM_B_DM<7>, MEM_B_DM<3>, MEM_B_DM<0>, MEM_B_DQ<47..40>, MEM_B_DQ<7..0>, MEM_B_DQS1, MEM_B_DQS2, MEM_B_DQS3, MEM_B_DQS_P<6>, MEM_B_DQS_N<5>, MEM_B_DQS_P<4>, MEM_B_DQS_N<2>, MEM_B_DQS_P<0>, MEM_B_DQ_BYTE0, MEM_B_DQ_BYTE1, MEM_B_DQ_BYTE2, MEM_B_DQ_BYTE3, MEM_B_DQ_BYTE4, MEM_B_DQ_BYTE5, MEM_B_DQ_BYTE6, MEM_B_DQ_BYTE7, MEM_B_DQS_P<2>, MEM_B_DQS_N<0>, MEM_B_DQS_P<1>, MEM_B_DQS_N<4>, MEM_B_DQS_P<5>, MEM_B_DQS_N<6>, MEM_B_DQS_P<7>, MEM_B_DQS_N<8>, MEM_B_DQS_P<9>, MEM_B_DQS_N<10>, MEM_B_DQS_P<11>, MEM_B_DQS_N<12>, MEM_B_DQS_P<13>, MEM_B_DQS_N<14>, MEM_B_DQS_P<15>, MEM_B_DQS_N<16>, MEM_B_DQS_P<17>, MEM_B_DQS_N<18>, MEM_B_DQS_P<19>, MEM_B_DQS_N<20>, MEM_B_DQS_P<21>, MEM_B_DQS_N<22>, MEM_B_DQS_P<23>, MEM_B_DQS_N<24>, MEM_B_DQS_P<25>, MEM_B_DQS_N<26>, MEM_B_DQS_P<27>, MEM_B_DQS_N<28>, MEM_B_DQS_P<29>, MEM_B_DQS_N<30>, MEM_B_DQS_P<31>, MEM_B_DQS_N<32>, MEM_B_DQS_P<33>, MEM_B_DQS_N<34>, MEM_B_DQS_P<35>, MEM_B_DQS_N<36>, MEM_B_DQS_P<37>, MEM_B_DQS_N<38>, MEM_B_DQS_P<38>, MEM_B_DQS_N<40>, MEM_B_DQS_P<41>, MEM_B_DQS_N<42>, MEM_B_DQS_P<43>, MEM_B_DQS_N<44>, MEM_B_DQS_P<45>, MEM_B_DQS_N<46>, MEM_B_DQS_P<47>, MEM_B_DQS_N<48>

Table of Spacing and Physical Rules

Source: MCP Interface DG (DG-03328-001_v0D), Section 2.3
## SATA Interface Constraints

Source: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

- Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

## Analog Video Signal Constraints

Source: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

- 75-ohm from output of three-pole filter to connector (if possible).
- 37.5-ohm from MCP to first termination resistor.

## Digital Video Signal Constraints

- LVDS interpair matching should be 5.0%. Pairs should be within 100 pS of clock length.
- DisplayPort/THS interpair matching should be 5.0%. Interpair matching should be within 100 pS.
- Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

Source: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.1.3 & 2.1.4.
### FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Pin 3</th>
<th>Pin 4</th>
<th>Pin 5</th>
<th>Pin 6</th>
<th>Pin 7</th>
<th>Pin 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 2</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

### FireWire Net Properties

<table>
<thead>
<tr>
<th>Port</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Pin 3</th>
<th>Pin 4</th>
<th>Pin 5</th>
<th>Pin 6</th>
<th>Pin 7</th>
<th>Pin 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 2</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

### FireWire Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Pin 3</th>
<th>Pin 4</th>
<th>Pin 5</th>
<th>Pin 6</th>
<th>Pin 7</th>
<th>Pin 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 2</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

---

**NOTICE OF PROPRIETARY PROPERTY**

The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it.
II. Not to reveal or publish in whole or part.
III. To maintain the document in confidence.

*The information contained herein is the proprietary property of Apple Computer, Inc.*
### SMC SMBus Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Physical SPACING</th>
<th>MINIMUM LINE WIDTH</th>
<th>ON LAYER?</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMB_55S SMBUS_SMC_A_S3_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SDA</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SDA</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
</tbody>
</table>

### SMCbus Charger Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Physical SPACING</th>
<th>MINIMUM LINE WIDTH</th>
<th>ON LAYER?</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSO_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>60</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
</tbody>
</table>

### SMC Constraints

- **Net Type**: SMBus Charger Net Properties
- **Physical SPACING**: 60
- **MINIMUM LINE WIDTH**: 0.1 MM
- **ON LAYER?**: STANDARD
- **MINIMUM NECK WIDTH**: 0.1 MM
- **MAXIMUM NECK LENGTH**: 0.1 MM
# K19i Board-Specific Physical & Spacing Constraints

## K19i PCB Rule Definitions

<table>
<thead>
<tr>
<th>Scale</th>
<th>NONE</th>
</tr>
</thead>
</table>

### TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, BOTTOM NO_TYPE, BGA |

<table>
<thead>
<tr>
<th>MM</th>
<th>15.2</th>
</tr>
</thead>
</table>

### Physical & Spacing Constraints

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>0.077</td>
<td>0.077</td>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>0.095</td>
<td>0.095</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

### Physical Rule Set

<table>
<thead>
<tr>
<th>Area Type</th>
<th>Spacing Rule Set</th>
<th>Net Spacing Type 1</th>
<th>Net Spacing Type 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA</td>
<td>BGA_P2MM_CLK_PCIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BGA</td>
<td>BGA_P2MM_CLK_PCIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BGA</td>
<td>BGA_P2MM_CLK_PCIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BGA</td>
<td>BGA_P2MM_CLK_PCIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BGA</td>
<td>BGA_P2MM_CLK_PCIE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Spacing Assignment

<table>
<thead>
<tr>
<th>Clock</th>
<th>Name 1</th>
<th>Name 2</th>
<th>Name 3</th>
<th>Name 4</th>
<th>Name 5</th>
<th>Name 6</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Notice of Proprietary Property**

The information contained herein is proprietary to Apple. It is to be used only for the purpose of working on behalf of Apple.