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### SCHEM,CORNHOLE,K19

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<td>02/21/2008108</td>
</tr>
<tr>
<td>3</td>
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</tr>
<tr>
<td>4</td>
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</tr>
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<td>5</td>
<td>SCHEM,CORNHOLE,K19</td>
<td>02/18/2008</td>
</tr>
<tr>
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<td>SCHEM,CORNHOLE,K19</td>
<td>02/18/2008</td>
</tr>
</tbody>
</table>

#### DATE

- **Thursday, 21 February 2008**

**MATERIAL/FINISH**

- **METRIC**

**APPD**

- **ENG**

**DATE**

- **REV**

**ZONE**

- **ECN**

**DESCRIPTION OF CHANGE**

- **REV**

**ECN**

- **DATE**

**DESCRIPTION OF CHANGE**

- **REV**

**ECN**

- **DATE**

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## Development BOM

<table>
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<th>PART NUMBER</th>
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</tr>
</thead>
<tbody>
<tr>
<td>630-9970</td>
<td>1</td>
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<td>2008-08-01</td>
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</tr>
<tr>
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</tbody>
</table>

## Module Parts

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</tr>
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CPU Decoupling & VID

PPCPUVTT_S0
PPVCCS0_CPU
PP1V8R1V5_S0_FET

CPU VCORE HF AND BULK DECOUPLING

VCCP (CPU I/O) DECOUPLING

VCCA (CPU AVdd) DECOUPLING

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I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II. NOT TO REPRODUCE OR COPY IT
III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
Mini-XDP Connector

NOTE: This is not the standard XDP pinout. See with XDP-XDP adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout
Current numbers from email Ponnacha Kongetira provided 11/30/2007 4:04pm (no official document number).
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

Minimum 1.025V for Gen2 support

OUT

IN

22 24 25 63 67

127 mA (A01, AVDD0 & 1)

43 mA (A01, DVDD0 & 1)

84 mA (A01)

402 MF-LF 1/16W 1%

TP_SATA_F_R2D_CN

TP_SATA_F_R2D_CP

TP_MCP_SATALED_L

TP_SATA_F_D2RN

TP_SATA_E_D2RP

NC_SATA_D_D2RN

TP_SATA_E_R2D_CN

TP_SATA_E_R2D_CP

NC_SATA_D_D2RN

TP_SATA_C_D2RN

SATA_ODD_D2R_P

SATA_ODD_D2R_N

SATA_ODD_R2D_C_N

SATA_ODD_R2D_C_P

SATA_HDD_D2R_P

SATA_HDD_D2R_N

SATA_HDD_R2D_C_N

If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
Current numbers from email Ponnacha Kongetira provided 11/30/2007 4:04pm (no official document number).
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

Apple: 1x 2.2uF 0402 (2.2 uF)

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

190 mA (A01, 1.8V)

16 mA (A01)

Apple: ???

206 mA (A01)

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)

NO STUFF

0.1UF

CERM402

20%

10V

2

1

C2620

NO STUFF

1K

MF-LF402

1%1/16W

2

1

R2630

NO STUFF

0.1UF

CERM402

20%

10V

2

1

C2640

30-OHM-1.7A

0402

21

L2640

4.7UF

X5R

402

20%

4V

2

1

C2615

4.7UF

CERM603

20%6.3V

2

1

C2640

30-OHM-1.7A

0402

21

L2640

0.1uF

CERM402

20%

10V

2

1

C2641

2.2UF

CERM402-LF

20%6.3V

2

1

C2616

NO STUFF

1K

MF-LF402

5%1/16W

2

1

R2651

2.2UF

CERM402-LF

20%6.3V

2

1

C2610

NO STUFF

1K

MF-LF402

1%1/16W

2

1

R2620

2.2UF

CERM402-LF

20%6.3V

2

1

C2610

NO TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_RGB_RED

NC_MCP_RGB_GREEN

NC_CRT_IG_B_COMP_PB

NC_MCP_CLK27M_XTALIN

NC_MCP_CLK27M_XTALOUT

MCP_IFPAB_VPROBE

MCP_HDMI_VPROBE

NC_MCP_TV_DAC_RSET

NC_MCP_TV_DAC_VREF

MCP_IFPAB_RSET

MCP_HDMI_RSET

PP1V8_S0

PPCPUVTT_S0

PP3V3_S0_MCP_VPLL

PP3V3_S0_MCP_DAC

VOLTAGE=3.3V

MIN_LINE_WIDTH=0.4 MM

MIN_NECK_WIDTH=0.2 MM

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_RGB_BLUE

NC_MCP_RGB_HSYNC

NC_MCP_RGB_VSYNC

NC_CRT_IG_R_C_PR

NC_CRT_IG_HSYNC

NC_CRT_IG_B_COMP_PB

NC_MCP_RGB_DAC_VREF

NC_MCP_CLK27M_XTALIN

NC_MCP_CLK27M_XTALOUT

NC_MCP_TV_DAC_RSET

NC_MCP_RGB_DAC_RSET

NC_MCP_RGB_DAC_VREF

NC_MCP_RGB_DAC_RSET

NC_MCP_RGB_DAC_VREF

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_RGB_BLUE

NC_MCP_RGB_HSYNC

NC_MCP_RGB_VSYNC

NC_CRT_IG_R_C_PR

NC_CRT_IG_HSYNC

NC_CRT_IG_B_COMP_PB

NC_MCP_RGB_DAC_VREF

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_CLK27M_XTALIN

NC_MCP_CLK27M_XTALOUT

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_TV_DAC_RSET

NC_MCP_RGB_DAC_VREF

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_RGB_DAC_RSET

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_RGB_BLUE

NC_MCP_RGB_HSYNC

NC_MCP_RGB_VSYNC

NC_CRT_IG_R_C_PR

NC_CRT_IG_HSYNC

NC_CRT_IG_B_COMP_PB

NC_MCP_RGB_DAC_VREF

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_CLK27M_XTALIN

NC_MCP_CLK27M_XTALOUT

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NC_MCP_RGB_DAC_RSET

NC_MCP_RGB_DAC_VREF

NO_TEST=TRUE

MAKE_BASE=TRUE

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MAKE_BASE=TRUE

NC_MCP_TV_DAC_RSET

NO_TEST=TRUE

MAKE_BASE=TRUE

NC_MCP_CLK27M_XTALIN
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for results in earlier ROMSIP and MCP FSB I/O interface initialization.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, PLACEMENT_NOTE=Place close to U1400

RTC Power Sources

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

Platform Reset Connections

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

Reset Button

SB Misc

Apple Inc.
DDR3 RESET Support

Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

- 3.3V is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
- 5% 1/16W MF-LF 100K R3305
- 5% 402 1/16W MF-LF 10K R3301
- 402 1/16W MF-LF 1K 5% R3310
- 402 5% 1/16W MF-LF 1K 5% R3310
- 402 0.1UF 20% Cerm C3300
- 402 1/16W MF-LF 20K 5% R3300
- 402 1/16W MF-LF 12 R3309
- 402 5% 1/16W MF-LF 12 R3309
- 402 1.5V S5 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

Ethernet & AirPort Support

NOTE: None can provide 3.3V power, but clock can otherwise RMGT rails are powered.

RTL8211 25MHz Clock

NOTE: None can provide 3.3V power, but clock can otherwise RMGT rails are powered.
Place one of 0.1uf cap close to each center tap pin of transformer

Transformers should be mirrored on opposite sides of the board

PLACEMENT_NOTE=Place on MDI lines so there are no stubs all 8 caps.
We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

Left USB Port B

Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

External USB Connectors
Unused pins designed as outputs can be left floating. Those designated as inputs require pull-ups.

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

PLACEMENT_NOTE: Place C4920 close to U4900 pins N14,N15

PLACEMENT NOTE= Place R4999 close to U4900 pins N14,N15

NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMI Interrupt can be active high or low, remove not accordingly. If SMI interrupt is not used, pull up to SMI rail.
Detect Right Fin Stack Temperature

Placement note: close to right fin stack
Place Q5501 on bottom side

Detect CPU Die Temperature
Place on top side under left heat pipe near CPU

CPU Proximity/CPU Die/Right Fin Stack

MCP Proximity/MCP Die/Battery Charger Proximity

Note: EMC1413 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe

Thermal Sensors

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NOTICE OF PROPRIETARY PROPERTY

DRAWING NUMBER

SHEET OF

SIZE

APPLE INC.

REV.

SCALE

A0.0051-7892

9749

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

FAN RT_PWM

SMC_FAN_0_TACH

PP5V_S0

PP3V3_S0

FAN_LT_TACH

SMC_FAN_0_CTL

FAN RT_PWM

SMC_FAN_0_TACH

PP5V_S0

PP3V3_S0

FAN_LT_TACH

SMC_FAN_0_CTL

CRITICAL 78171-0004
M-RT-SM

7 7

7 8 39 44 49 51 63 66 67 70

7

6 7 8 13 18 19 21 22 24 25 28

29 37 39 43 45 47 48 49 51 55

59 60 63 68 69 70 77

80 81 82 84 85 96

CRITICAL 78171-0004
M-RT-SM

7 7

7 8 39 44 49 51 63 66 67 70

7

6 7 8 13 18 19 21 22 24 25 28

29 37 39 43 45 47 48 49 51 55

59 60 63 68 69 70 77

80 81 82 84 85 96
BOM OPTION: KBDLED_YES

To detect Keyboard backlight, SMC will
LOW = keyboard backlight present
HIGH= keyboard backlight not present

BOOSTER +18.5VDC FOR SENSORS

IPD FLEX CONNECTOR

BOOSTER DESIGN CONFIGURATION:
- POWER CONVERSION
- SIGNAL TO GND
- GND TO GND
- START UP TIME LESS THAN ONE
- B5352,700/700,000 MICROSECOND

BOOSTER DESIGN CONSIDERATION:
- RIPPLE TO MEET ERS
- DROOP LINE REGULATION
- POWER CONSUMPTION

SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.50MM

KBDLED_ANODE
MIN_NECK_WIDTH=0.25 MM
MIN_LINE_WIDTH=0.25 MM

KBD BACKLIGHT CONNECTOR

F-RT-SM
APN 518S0612

CRITICAL
MM3243DRRE
APN 353S1364

VR5802
CTRL
6
CRITICAL

SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM

LED

WELLSPRING 2

KBD BACKLIGHT CONNECTOR

APPLE INC.
Analog SMS

R5921 Pull up SMS_PWRDN to turn off SMS when pin is not being driven by SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation:

---

Sync Master = Sensor
Sync Date = 08/14/2008

---

**Sudden Motion Sensor (SMS)**

---

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*Made in China*
Any of the 4 frequencies can be selected.

25 MHz is selected with R5190 and R5191.

Jumper to select 3.3 V or 5 V can be used with R6190, R6191, R5190 and R5191.
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 HZ
VIN = 2V RMS, CODEC VIN = 1.21 VRMS

CRITICAL
3.3UF CERM-X5R805-1 10V

CRITICAL
3.3UF CERM-X5R805-1 10V

CRITICAL
3.3UF CERM-X5R805-1 10V

CRITICAL
15PF CERM402 5% 50V

CRITICAL
1% 6.04K 1/16W

CRITICAL
16.5K 1% 402 1/16W

55 60
402MF-LF

AUD_LI_R_DIV
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_P_L
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_REF
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_GND
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_P_R
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_L_DIV
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_R
GND_AUDIO_CODEC
MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM
AUD_LI_L

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ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

OUT

IN

APPLE INC.

SCALE

REV.

A

D

C

B

A

D

C

B

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

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DRAWING NUMBER

SHEET OF

SIZE

DNC

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

R6501

C6504

100pF

100pF

CRITICAL

16V10%

402

X7R-CERM

0.1UF

2

1

MF-LF

5%1/16W

2

1

R6502

C6505

0.1UF

10%

16V

2

1

X7R-CERM

MF-LF

5%1/16W

2

1

R6512

C6510

0.0022UF

10%

50V

2

1

CERM402

MF-LF603

5%1/10W

21

R6501

C6501

0.0022UF

10%

50V

2

1

CERM402

0.1UF

5%

1/10W

21

R6501

C6501

CRITICAL

10%

50V

2

1

X7R-CERM

MF-LF

5%1/10W

21

R6511

C6511

CRITICAL

5%

1/10W

21

R6511

C6511

MF-LF

10%

1/10W

21

R6511

C6511

AUD_HP_PORT_R

AUD_HP_L

AUD_HP_ZOBEL_R

AUD_HP_ZOBEL_L

AUD_HP_R

GND_AUDIO_HP_AMP

AUD_HP_PORT_L

SYNC_MASTER=AUDIO

SYNC_DATE=03/16/2009
1.05V S0 PLL LDO

VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY

VOUT = 0.8V * (1 + RA / RB)
Critical BOM Option

C9704 SHOULD BE 47K IF RC FILTER IS USED

5% 1/16W 402

2

R9715 100K MF-LF 402 5% 1/16W 0 NO STUFF

R9714 100K MF-LF 402 5% 1/16W 0 NO STUFF

CRITICAL

NO STUFF

10UF X5R 805 25V 10%

PLACE XW9700 CLOSE TO C9712 AND C9713

SHT OF D

REV. A.0.0051-7892

DRAWING NUMBER

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APPLE INC.

MIN_LINE_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.4 MM
VOLTAGE=5V

CRITICAL

MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM
VOLTAGE=6V

CRITICAL

MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.20 MM
VOLTAGE=50V

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SYNC_MASTER=DDR SYNCE_DATE=12/12/2008
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps. DQ signals should be matched within 5 ps of associated DQS pair.

DDR3: All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ signals should be matched within 20 ps of associated DQS pair.
### SATA Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

- DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
- DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

### Digital Video Signal Constraints

- R/G/B signals should be matched as close as possible and < 10 inches.
- 50-ohm from first to second termination resistor.
- CRT signal single-ended impedance varies by location:
  - 20 MIL for CRT signals.
  - 100_OHM_DIFF for LVDS signals.
  - 90_OHM_DIFF for PCIE signals.

### Analog Video Signal Constraints

- Analog Video signals should be matched as close as possible and < 10 inches.
- 50-ohm from first to second termination resistor.
- CRT signals should be matched as close as possible and < 10 inches.
- CRT signals should be matched as close as possible and < 10 inches.

---

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## FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Net Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
<th>Diff Pair Primary Gap</th>
<th>Diff Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## FireWire Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Spacing</th>
<th>Min Line Width</th>
<th>Allow Route</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## SD CARD INTERFACE CONSTRAINTS

- SD_DATA
- SD_CLK
- SD_CMD
- SD_D<0>
- SD_D<1>
- SD_D<2>
- SD_D<3>
- SD_D<4>
- SD_D<5>
- SD_D<6>
- SD_D<7>

## SD CARD NET PROPERTIES

<table>
<thead>
<tr>
<th>Property</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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Rev. A

Apple Inc.
### Graphics, SATA Constraint Relaxations
Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

### Memory Constraint Relaxations

#### Table: Physical Rule Set

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table: Spacing Rule Item

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table: Physical Rule Item

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table: Spacing Assignment Item

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Project Specific Constraints

#### Table: Physical Assignment Item

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Project Specific Net Properties

#### Table: Physical Rule Head

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table: Spacing Rule Head

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table: Spacing Assignment Head

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PCB Electrical Properties

#### Table: Electrical Constraint Set

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### PCB Rule Definitions

**NOTE:** From T18 MLB, changed to reflect M99 stackup.

**SCALE**

- **NONE**

**DREWING NUMBER**

- **97 97**

**REV.**

- **A.0.0051-7892**

---

### A

#### PCB Rule Definitions

- **NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

**LINE-TO-LINE SPACING**

- **LAYERS**
- **SPACING_RULE_SET**
- **WEIGHT**

---

### B

#### PCB Rule Definitions

- **NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

**LINE-TO-LINE SPACING**

- **LAYERS**
- **SPACING_RULE_SET**
- **WEIGHT**

---

### C

#### PCB Rule Definitions

- **NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

**LINE-TO-LINE SPACING**

- **LAYERS**
- **SPACING_RULE_SET**
- **WEIGHT**

---

### D

#### PCB Rule Definitions

- **NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

**LINE-TO-LINE SPACING**

- **LAYERS**
- **SPACING_RULE_SET**
- **WEIGHT**

---

### Table: Board-Specific Spacing & Physical Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.089 mm</td>
<td>0.220 mm</td>
<td>0.089 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.080 mm</td>
<td>0.200 mm</td>
<td>0.080 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0.115 mm</td>
<td>0.230 mm</td>
<td>0.115 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0.102 mm</td>
<td>0.220 mm</td>
<td>0.102 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.076 mm</td>
<td></td>
<td>0.076 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0.077 mm</td>
<td>0.330 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>0.330 mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.090 mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>0.095 mm</td>
<td>0.165 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>0.135 mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>0.150 mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>0.180 mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** From T18 MLB, changed to reflect M99 stackup.