3. All crystals & oscillator values are in Hertz.
System Block diagram can be found on Kismet

PATH: KISMET > K70/72 > BLOCK DIAGRAMS > K72 BLOCK DIAGRAM
### BOM Variants

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>376S0975</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>377S0147</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### Bar Code Labels / IEEE #'s

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>PART #</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>376S0975</td>
<td>LABEL,M8,20</td>
<td>377S0147</td>
<td>LABEL,M8,20</td>
</tr>
</tbody>
</table>

### CPU SOCKET

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### CPU SOCKET ALTERNATES

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### D8 SCHEMATIC / PCB #'S

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### D8 ALTERNATES

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### BOM Groups

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### CPUs

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### ASICs

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### Programable Parts

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### VRAM Module Parts

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### BOM Configuration

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0620</td>
<td>LABEL,M8,20</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>
CPU Heatsink
4MM PLATED HOLES (998-4158)

GPU HEATSINK MOUNTING FEATURES
(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)

Rear Cover
988-5034 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)

Rear Cover
860-1487 (PCB STANDOFF)

SSD STANDOFF
A02: 860-1461

SYNC_DATE=08/27/2012
Holes/PD parts
WWW.VINAFIX.VN
VAXG DECOUPLING

INTEL RECOMMENDATION 4X22UF 0805, 3X 4.7UF
PLACE INSIDE SOCKET CAVITY.

C1704: 22UF 20% 6.3V X5R-CERM
C1705: 22UF 20% 6.3V X5R-CERM
C1706: 22UF 20% 6.3V X5R-CERM
C1707: 22UF 20% 6.3V X5R-CERM
C1708: 22UF 20% 6.3V X5R-CERM
C1709: 22UF 20% 6.3V X5R-CERM

PLACE C1710 AT BALL U1800.AB1
PLACE C1711 AT BALL U1800.AC2

R1720 6.3V 10% 603 X5R-CERM
R1730 6.3V 10% 603 X5R-CERM
R1740 6.3V 10% 603 X5R-CERM

SYNC_MASTER=D8_MLB
SYNC_DATE=08/27/2012

VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.4MM
MAKE_BASE=TRUE

VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.4MM
MAKE_BASE=TRUE

PPCPUAXG_S0_REG=PPVAXG_S0_CPU
PP1V05_S0_PCH_VCC_ADPLL_F=PP1V05_S0_PCH_VCC_ADPLLB_F
PP3V3_S0_PCH_VCCA_DAC_F=PP3V3_S0_PCH_VCC_ADAC
- Unused GPIOs 0 & 15 not isolated.
- 'Output' PCH/XDP signals require pulls.
- MXM_GOOD not isolated as only LED is affected.

- Needs to split between route from PCH to J2550 connect to appropriate non-XDP signals on PCB.
MEM_RESET_L Generator

The circuits below handle MEMVTT power during S0->S3->S0 transitions, as well as isolating the CPU’s PM_SLP_S3_L output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behaviour of signals.

WHEN HIGH: MEM_RESET_L NOT ISOLATED.
WHEN LOW: MEM_RESET_L IS ISOLATED.

MEM_RESET_L = 1ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L (Block CPU from driving MEM_RESET_L in S3)

WHEN LOW: MEM_RESET_L IS ISOLATED.
WHEN HIGH: MEM_RESET_L NOT ISOLATED.

MEM_RESET_L Generator

With optional delay from 1V5 S0 PGODX

PM_PGOOD pull-up to CPU VTT rail is on CPU page

MEMVTT_EN Generator

Enables MEMVTT when PCH drives CPU PWRGD.

CPU does not drive MEM_CKE until VCCORE activated but CPU 1V5 (VDDQ) leaks into it. Clamping MEMVTT will keep the MEM_CKE low until CPU actively controls it.

MEMVTT Clamp actively holds MEMVTT rail low until MEMVTT is enabled.

MEMVTT = CPU_PWRGD * PM_SLP_S3_L (VTT is enabled when PCH tells CPU to enable VCCORE)

MEMVTT Clamp

Ensures CREK signals are held low in S3 and in S0 before CPU PWRGD
HDD Out-of-Band Temp Sensing

Temperature read from SATA power connector pin 11

HDD 12V_S0 FET (max 2.8A, ave 0.6A)

HDD 5V_S0 FET (max 0.7A, ave 0.3A)

REMOVE R5413 AND SHORT R5412 AFTER HDD_PWR_EN WORKS

NOTICE OF PROPRIETARY PROPERTY:
I. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
III. NOT TO REPRODUCE OR COPY IT

HDD/SSD Temp Sense
Note:
The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors).

Note:

It is assumed there is a pull-up to
5V/12V inside the fan, otherwise
the SMC does not see any significant
voltage on the SMC pin. Then my definition of the mode of Q5610 is
at common and the SMC sinks current
when Q5610 is on.

This resembles an open-drain if
there is a pull-up, going to a 5V-12V
PWM input:

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors):

The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors).

Note:

It is assumed there is a pull-up to
5V/12V inside the fan, otherwise
the SMC does not see any significant
voltage on the SMC pin. Then my definition of the mode of Q5610 is
at common and the SMC sinks current
when Q5610 is on.

This resembles an open-drain if
there is a pull-up, going to a 5V-12V
PWM input:

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors):

The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors):

The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors):

The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors):

The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.

See: RADAR: 10565825- D7: Need schematic and PCB file of fan (All Vendors):

The circuit for the PWM input to
the fan acts as a non-inverting
level-shifter to protect the SMC.
If Q5610 turns on, there would be 5V/12V
inside the fan, otherwise, this is simply a pass-FET.

FET input.

Otherwise, this is simply a pass-FET.
APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

PLACE XW6110 NEAR U6101, BETWEEN PINS 2 & 5

PLACE U6100 AS CLOSE TO PIN 9 AS POSSIBLE

WARNING: This document contains proprietary information. The possession of this document does not convey any rights to the information contained herein. The information in this document is protected by copyright laws and other intellectual property laws. The information in this document may not be copied, reproduced, distributed, transmitted, displayed, published, broadcast, or otherwise used, in whole or in part, without the prior written permission of the owner. USE OF THIS DOCUMENT IS SUBJECT TO CERTAIN ADDITIONAL LIMITATIONS AS SET FORTH IN THE LICENSE AGREEMENT WHICH IS AVAILABLE AT WWW.QDZBWX.COM/LEGAL.
IPHS HS Detect Debounce CKT

AUDIO CONNECTOR DETECT STATES

<table>
<thead>
<tr>
<th>PIN</th>
<th>NCH</th>
<th>SDP</th>
<th>RSAH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

LI Insert Detect (DETECT A)

TBT/DP Audio Enable

AUDIO: Detects/Grounding

Apple Inc.

The information contained herein is the proprietary property of Apple Inc.

Notice of Proprietary Property:

All rights reserved.

The possessor agrees to the following:

I. To maintain this document in confidence
II. Not to reproduce or copy it
III. Not to reveal or publish it in whole or part

Page 12 of 144

Apple Inc.

051-9505 1.3.0.0

04/28/09

Access Request No.

www.qdzbxw.com

www.vinafix.vn
S5 3V3 Soft Enable

S4 5V Enable

S0 12V Enable

S0 5V and TBT Enable

Parallel Enable PGood combinator

S0 Platform Parallel Sequence Enable

CPU/PCR Sequencing

S4 3V3 Enable

S4 USB Enable

S3 1V5 Reg (S0/S3) Enable

Rail definitions

Platform: All processor use Core and core-Graphics (1.5 V, 1.8 V, 2.0 V, 3.3 V, 5.0 V, PCH Core/PLL/VRM) 

Notes on sequencing requirements:

1. No hard specification on platform rails.
2. VIN sequencing taking in S0 S3V3 and 1V5.
3. VIN 1V5 must ramp before VIN 1V8 and VIN 3V3 must ramp before VIN 1V5.
4. VIN 1V8 must ramp before VIN 1V5 and VIN 3V3 must ramp within 50 ms of each other.
Resume Reset

Intel Core 2007 Intel: Bay P2G, Section 2.2.3.

Noise:
The Intel 870G2 design does not support deep 0 volt mode to both SSTR0 and SSTR1 output signals together.

Requirement:
Power on:
Assumed at least 10 ms after all regulated volt power is valid
Power off or loss of AC:
Transition is 0.1% or less before U7000/3 drops to 2.5V
To allow PCH to detect regulated volt in battery without some minute loading.

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for resume operation.

SMC guarantees RSMRST# if PCH in power good and SSTR0/1/PWRGD signal in assertion condition, input exists 1 or 1.3 V.

SMC guarantees RSMRST# if PCH[PWRGD] signal in assertion condition, input exists 1 or 1.3 V.

Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for resume operation via PBCH_PGW.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough in normal operation via PM_DSW_PWRGD.

Asserted at least 10 ms after allsuspend well power is validated.

1. Do not reproduce or copy it.
2. Do not reveal or publish it in whole or part.
3. To maintain this document in confidence.
3.3V S5 Regulator
Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: 7 A (design)/ 6.6 A (budget)
OC trip point: 1.9 (non)/ 1.7 A (min)
Switching freq: 350 kHz

5V S4 Regulator
Max avg current: 10 A (design)/ 6.98 A (budget)
Max peak current: 7 A (design)/ 6.9 A (budget)
OC trip point: 1.9 (non)/ 1.9 A (min)
Switching freq: 350 kHz

VReg 3.3V S5/5V S4
Apple Inc. 05-03-00
NOTICE OF PROPRIETARY PROPERTY:
PROPRIETARY PROPERTY OF APPLE INC.
NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
PAGE TITLE III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
DRAWING NUMBER SHEET
051-9505 S 11 OF 144 71 OF 123
www.qdzbwx.com
www.vinafix.vn
3.425V "G3Hot" Regulator

Max avg current: 0.04 A (WORLD)
Max peak current: 0.10 A (WORLD)
OC trip point: ? A (nom) / ? A (min)
Switching freq: 7 kHz

D8: CONTROLLER CHANGE FOR 3.42V SMC SUPPLY  RDAR://11003901
D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42 G3H REGULATOR  RDAR://11132734
Dual-Port Host DDC Crossbar

U9300

C9300 20%
CERM 10V
0.1UF 402

U9300

TS3DS10224 QFN

Critical

SYNC_DATE=08/27/2012
SYNCH_MASTER=D8_MLB=PP3V3_S0_DP
DP_TBTPA_DDC_DATA
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
DP_TBTPA_DDC_CLK
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA
DP_TBTSNK0_DDC_DATA
DP_TBTSNK0_DDC_CLK
TBT_DDC_XBAR_EN_L

NOTICE OF PROPRIETARY PROPERTY:
I. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
III. NOT TO REPRODUCE OR COPY IT

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.

Apple Inc.

www.qdzbwx.com

www.vinafix.vn
For 12V systems:

- **IHVS0/S3  1120mA  1090mA  1170mA (12W minimum)**

**CRITICAL**

- **POLY-TANT**
- **100UF**

- **TBT_A_D2R_P<0>**
- **DP_TBTPA_ML_C_N<3>**

**114S0338**

**V3P3 must be S4 to support wake from Thunderbolt devices.**

- **20%=PPHV_SW_TBTAPWRSW**

**CRITICAL**

- **C9480**
- **IN**
- **2**
- **0.1UF**
- **10%**

- **C9474**
- **C9475**
- **RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF**

- **R9452**
- **1/20W**

- **R9410,R9413**
- **22.6K**
- **1%**

- **R9411**
- **36.5K**
- **402**

- **R9426**
- **R9427**
- **1M**
- **10K**
- **MF**
- **201**
- **1/20W**

- **R9429**
- **100K**
- **201**

**NOTE:** Polarity swapped for layout!

**I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE**

**II NOT TO REPRODUCE OR COPY IT**
K6X BACKLIGHT CONTROL SUPPORT

Backlight Control

Y2 is simply an inverted version of A, with no delay. On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video.

U9500 OUTPUT Y2 IS A NON-INVERTED, DELAYED VERSION OF INPUT A. The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.

VIDEO_ON = PP3V3_S0_DP

Internal DP Support
GPU NVVDD DECOUPLING I (EDP) = 95A

PLACE UNDER GPU

PLACE UNDER GPU

PLACE UNDER GPU

PLACE NEAR GPU W/ 35MM FROM GPU CENTER
GPU FBVDD/Q DECOUPLING I (EDP PEAK) = 26A

PLACE UNDER GPU

PLACE UNDER GPU

PLACE UNDER GPU

PLACE UNDER GPU

PAGE NOTES

Page Title

INSTRUCTIONS

1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

2. SYNC_MASTER = D8_YAN

3. PROPRIETARY PROPERTY OF APPLE INC.

4. NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.

5. BOM options provided by this page:
   - 2
   - NOSTUFF
   - 4.7UF
   - X6S
   - 0402
   - 6.3V
   - 10UF
   - X6S
   - 0201

6. Power aliases required by this page:
   - (NONE)

7. Signal aliases required by this page:
   - (NONE)
GPU SP_PLLVDD/VID_PLLVDD 47MA+41MA

GPU GPC_PLLAVDD/LXS_PLLVDD/FB_DLL_AVDD 52MA+39MA+50MA

GPU GPU_FB_PLL_AVDD 120MA X 4 = 480MA
### General Physical Rule Definitions

<table>
<thead>
<tr>
<th>Description</th>
<th>Min (mil)</th>
<th>Max (mil)</th>
<th>Min (mils)</th>
<th>Max (mils)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100_ohm_diff</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>90_ohm_diff</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>50_ohm_se</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>42_ohm_se</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>34_ohm_se</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>* Y</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Compensation Physical Rule Definition

- **Min Width**
  - Min Width (mil): 0.1 MM
  - Min Width (mils): 0.1 MM

### General Spacing Definitions

- **Min Width**
  - Min Width (mil): 0.1 MM
  - Min Width (mils): 0.1 MM

### Board Stack-up

- **Top Signal**: 0.5 oz (Cu plated)
- **Signal**: 1 oz
- **Prepreg**: 0.076 MM
- **Prepreg**: 0.380 MM

---

**Note**: The information contained herein is the property of Apple Inc. The possession agrees to the following:

- All rights reserved.
- To maintain this document in confidence.
- Not to reveal or publish it in whole or part.

**SYNC_DATE** = 08/27/2012
### DDR3 Specifications

#### DDR3-specific Physical Rules

<table>
<thead>
<tr>
<th>Line</th>
<th>Rule</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR_CLK_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
<tr>
<td>DDR_DQS_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
<tr>
<td>DDR_CMD_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
<tr>
<td>DDR_CTRL_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
</tbody>
</table>

#### DDR3-specific Spacing Definitions

<table>
<thead>
<tr>
<th>Line</th>
<th>Rule</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR_CLK_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
<tr>
<td>DDR_DQS_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
<tr>
<td>DDR_CMD_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
<tr>
<td>DDR_CTRL_PHY</td>
<td>2.0 MM</td>
<td>E09015:2004.103.100290.1001</td>
</tr>
</tbody>
</table>

### DDR3 Constraints

**Note:**

- To meet these rules, the spacing must be applied to the net.
- DDR3 must have a weight greater than DDR_BL2BL.
- DDR3 draws about 25 ma per pin with equal spacing on the DDR of the pin. The worst coupling mechanism is capacitive: 0.05 mm spacing is used for worst case. DDR3 does not require coupling between channels. DDR3 must be placed on top and bottom layers only.
- Creation of capacitor, inductance, and resistance is not recommended to use DDR3, as it is not designed to be used in this context.
- DDR3 must be used to fit the design to fit the DDR3 standard.
### DMI-Specific Physical Rules

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### CPU Misc. / FDI

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### XDP-Specific Physical Rules

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Chipset Test Interface

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Physical Net Type to Rule Map**

- **SPACING_RULE_SET**
  - NET_SPACING_TYPE1: NET_SPACING_TYPE2

**Physical Net Type to Rule Map**

- **DMI_85DDMI_PHY**
  - XDP_CLK_ISO
  - COMP_FDI

**Electrical Constraint Set**

- **PCIE_REF_CLK**
  - 10 mils

**Electrical Constraint Set**

- **CPU_MON**
  - 15.75 mils

**Electrical Constraint Set**

- **I258**
  - 20 mils

**Electrical Constraint Set**

- **I266**
  - 20 mils

**Electrical Constraint Set**

- **I254**
  - 20 mils

**Electrical Constraint Set**

- **I247**
  - 20 mils

**Electrical Constraint Set**

- **I248**
  - 20 mils

---

**CPU Misc.**

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU Misc.**

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU Misc.**

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU Misc.**

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Name</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDP_S2N</td>
<td>XDP-sdk</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
<td>0.3 mm</td>
<td>1.5 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### SMBus

**SMBus-specific Physical Rules**

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Layer</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Physical Net Type to Rule Map**

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Layer</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Sensor

**Sensor-specific Physical Rules**

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Layer</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Physical Net Type to Rule Map**

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Layer</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Constraints

**Sensor-specific Spacing Definitions**

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Layer</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SMBus-specific Spacing Definitions**

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Layer</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## CPU Core Phases

<table>
<thead>
<tr>
<th>Signal Bus</th>
<th>Mechanical</th>
<th>Operating</th>
<th>Voltage</th>
<th>DC/DC</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Phase 1
- Local Ground Input Bus
- Input Bus

### Phase 2
- I1179
- I1178
- I1176
- I1171
- I1164
- I1161
- I1160
- I1159
- I1158
- I1155
- I1156
- I1152

### Phase 3
- I1149
- I1146
- I1147
- I1143
- I1141
- I1138

### Phase 4
- I896
- I894
- I893
- I891
- I887
- I885
- I884

---

## CPU AXS Phase and Core Controller

<table>
<thead>
<tr>
<th>Electrical Connector</th>
<th>Mechanical</th>
<th>Operating</th>
<th>Voltage</th>
<th>DC/DC</th>
<th>Status</th>
</tr>
</thead>
</table>

### Phase 1
- PPCPUAXG_S0_SENSE
- ISENAXG_P

### Phase 2
- CPU_VIDSCLK
- REG_CPUCORE_IMON

### Phase 3
- REG_CPUCORE_FB
- CPU_AXG_FB_R_1

### Phase 4
- REG_CPUCORE_VSEN
- REG_CPUCORE_FDVID
- REG_ISENAXG_P

---

## Electrical Constraints

- ISNS_CPU_CORE
- ISNS_CPU_AXG
- POWER_PHY
- VR_CTL_PHY
- VR_VID
- VR_SWITCH
- SNS_DIFF_PHY
- VR_LGATE
- SENSE
- POWER
- 1.1V
- 12V

---

## CPU VReg Constraints

- Apple Inc. 129-3664 6.1.0.0 129 of 144 109 of 123

---

**Caption:**

- PAGE TITLE
- PAGE
- BRANCH
- DRAWING NUMBER
- SIZE
- SYNC_DATE=08/27/2012
### Platform VReg Constraints

**Apple Inc.**

**SYNC_DATE=08/27/2012**

**NOTE:** This document contains information that is the property of Apple Inc. and is provided for the sole purpose of facilitating communication between Apple Inc. and its licensees. Any unauthorised reproduction or disclosure of this document, or any portion thereof, is strictly prohibited.

---

### 3.3V S5/5V S4

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Output Bus</th>
<th>FET Switched</th>
<th>Input Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td></td>
<td></td>
<td>5V S3</td>
</tr>
</tbody>
</table>

### 1.8V S0

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Output Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8V</td>
<td></td>
</tr>
</tbody>
</table>

### 12V S5

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Output Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V</td>
<td></td>
</tr>
</tbody>
</table>

---

### VDDQ S3 (1.5V)/VTT S5

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Output Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5V</td>
<td></td>
</tr>
</tbody>
</table>

---

### Voltage Spacing

- **3.3V:** 3.3V
- **1.8V:** 1.8V
- **12V:** 12V
- **0.75V:** 0.75V

---

### Physical Layout

- **3.3V S5/5V S4**
- **1.8V S0**
- **12V S5**
- **VDDQ S3 (1.5V)/VTT S5**

---

### Platform VReg Constraints

**Apple Inc.**

**SYNC_DATE=08/27/2012**

**NOTE:** This document contains information that is the property of Apple Inc. and is provided for the sole purpose of facilitating communication between Apple Inc. and its licensees. Any unauthorised reproduction or disclosure of this document, or any portion thereof, is strictly prohibited.
### DisplayPort

**Electrical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Physical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

### TBT/DP Constraints

**TBT IC Net Properties**

<table>
<thead>
<tr>
<th>Electrical Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Physical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**TBT/DP Constraints**

**Apple Inc.**

**NOTICE OF PROPRIETARY PROPERTY:**

No disclosure of Technology or design is being made which may infringe upon the rights of others. Information contained herein is the proprietary property of Apple Inc. and is subject to Apple’s rights under copyright, patent, trade secret, and other laws. It is being furnished to you for the sole purpose of allowing you to use Apple products in accordance with the terms of your Apple contract. You agree not to use, disclose, reproduce, or copy this information or any other part of Apple’s proprietary property without express written consent of Apple. Any use of this information, other than in accordance with your Apple contract, is prohibited.

**SYNC DATE:** 08/27/2012

**DRAWING NUMBER:** 124578

---

**DisplayPort**

**Electrical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Physical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Thunderbolt**

**Electrical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Physical Constraint Set**

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_C_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_EG_AUX_N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DP_INT_SPDIF_AUDIO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Thunderbolt-specific Spacing Definitions**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Spacing</th>
<th>Maximum Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>75 mm</td>
<td>90 mm</td>
</tr>
<tr>
<td>B</td>
<td>36 mm</td>
<td>75 mm</td>
</tr>
<tr>
<td>C</td>
<td>79 mm</td>
<td>36 mm</td>
</tr>
</tbody>
</table>

**DISPLAYPORT AUX CHANNEL INTRA-PAIR MATCHING SHOULD BE 5 PS.**

**SPACING RULE SET**

<table>
<thead>
<tr>
<th>Line-1</th>
<th>Line-2</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>7</td>
<td>6</td>
</tr>
</tbody>
</table>

**LINE-TO-LINE SPACING ON LAYER**

**SPACING RULE ITEM**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Minimum Line Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>55 _OHM_SE</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>85 _OHM_DIFF</td>
<td></td>
</tr>
</tbody>
</table>

---

**NO_TEST=TRUE**

---

**Bill Comolli's TBD Routing Notes**

---

**Table of Spacing Assignment Items**

<table>
<thead>
<tr>
<th>Table ID</th>
<th>Layer</th>
<th>Minimum Spacing</th>
<th>Maximum Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>89</td>
<td>A</td>
<td>75 mm</td>
<td>90 mm</td>
</tr>
<tr>
<td>88</td>
<td>B</td>
<td>36 mm</td>
<td>75 mm</td>
</tr>
<tr>
<td>87</td>
<td>C</td>
<td>79 mm</td>
<td>36 mm</td>
</tr>
</tbody>
</table>

---

**Table of Physical Rule Items**

<table>
<thead>
<tr>
<th>Rule ID</th>
<th>Layer</th>
<th>Minimum Spacing</th>
<th>Maximum Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>86</td>
<td>A</td>
<td>55 _OHM_SE</td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>B</td>
<td>85 _OHM_DIFF</td>
<td></td>
</tr>
</tbody>
</table>

---

**Table of Spacing Rule Items**

<table>
<thead>
<tr>
<th>Table ID</th>
<th>Layer</th>
<th>Minimum Spacing</th>
<th>Maximum Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>84</td>
<td>A</td>
<td>75 mm</td>
<td>90 mm</td>
</tr>
<tr>
<td>83</td>
<td>B</td>
<td>36 mm</td>
<td>75 mm</td>
</tr>
<tr>
<td>82</td>
<td>C</td>
<td>79 mm</td>
<td>36 mm</td>
</tr>
</tbody>
</table>
### GDDR5 Specific Physical Rules

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Rule Map</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output net</td>
<td>Input net</td>
</tr>
<tr>
<td>Output net</td>
<td>Input net</td>
</tr>
</tbody>
</table>

#### Table: Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

<table>
<thead>
<tr>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
<tr>
<td>3:1</td>
<td>2:1</td>
<td>2:1</td>
</tr>
</tbody>
</table>

#### Table: Electrical Constraint Set

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Dynamic Bus Inversion: ADDRay</td>
<td>0x80</td>
</tr>
<tr>
<td>Data Dynamic Bus Inversion: DBRay</td>
<td>0x80</td>
</tr>
<tr>
<td>Error Detection: EDRay</td>
<td>0x80</td>
</tr>
<tr>
<td>Clock, CKE, CLO, WAY, CKey, CKey</td>
<td>0x80</td>
</tr>
<tr>
<td>Forwarded Clock: WSRRay</td>
<td>0x80</td>
</tr>
</tbody>
</table>

#### Table: Physical Spacing

<table>
<thead>
<tr>
<th>Physical Spacing</th>
<th>Min Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock, CKE, CLO, WAY, CKey, CKey</td>
<td>3:1</td>
</tr>
<tr>
<td>Forwarded Clock: WSRRay</td>
<td>3:1</td>
</tr>
</tbody>
</table>

---

**GDDR5 Frame Buffer A**

**GDDR5 Frame Buffer B**

**GDDR5/GPU Constraints**
<table>
<thead>
<tr>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMCISNS_*</td>
<td>SMCISNS_*</td>
<td>SMCISNS_*</td>
<td>SMCISNS_*</td>
</tr>
<tr>
<td>SMCV3NS_*</td>
<td>SMCV3NS_*</td>
<td>SMCV3NS_*</td>
<td>SMCV3NS_*</td>
</tr>
<tr>
<td>SMC_*</td>
<td>SMC_*</td>
<td>SMC_*</td>
<td>SMC_*</td>
</tr>
<tr>
<td>SPI_*</td>
<td>SPI_*</td>
<td>SPI_*</td>
<td>SPI_*</td>
</tr>
<tr>
<td>SSD_*</td>
<td>SSD_*</td>
<td>SSD_*</td>
<td>SSD_*</td>
</tr>
<tr>
<td>SYS_*</td>
<td>SYS_*</td>
<td>SYS_*</td>
<td>SYS_*</td>
</tr>
<tr>
<td>UVP_*</td>
<td>UVP_*</td>
<td>UVP_*</td>
<td>UVP_*</td>
</tr>
</tbody>
</table>

**AUTO-CONSTRAINS GENERATED Fri 04/06/12 07:46:02 PM**