1. All resistance values are in ohms, 0.1 watt +/- 5%.

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</tr>
<tr>
<td>48</td>
<td>I/O Reader Connector</td>
</tr>
</tbody>
</table>

### Sync

<table>
<thead>
<tr>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>49</td>
</tr>
<tr>
<td>50</td>
</tr>
<tr>
<td>51</td>
</tr>
<tr>
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<tr>
<td>89</td>
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<td>90</td>
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<tr>
<td>91</td>
</tr>
</tbody>
</table>
For EMC
EMC Spring (870-1577); Near DIMMs

DIMM CONNECTOR NUTS

Nuts (805-9582)

CPU Heatsink
4mm Plated Holes (998-0850)

PCH HEAT SINK

MOUNTING ANCHORS (511-0057)

Rear Cover
Standoffs (860-1255)

Backer Plate
Nuts (835-0269)

Holes

SYNC_MASTER=K74_MASTER
SYNC_DATE=N/A
The POSSESSOR AGREES TO THE FOLLOWING:

[Diagram and text related to the processor agreement and related components]

[Diagram and text related to the processor agreement and related components]
BOM GROUP

INTEL RECOMMENDATION 178 220F 0805

INTEL RECOMMENDATION 9X22UF 0805

2x 22uF 0805, 5x 1uF 0402

2X 22UF 0805, 7X 10UF 0805

330UF-0.0045OHM

VTT (CPU Uncore) DECOUPLING

2x 220F 0805, 7x 100F 0805 INTEL RECOMMENDATION 9X22UF 0805

Place at edge of socket.

Place under socket cavity on secondary side.

Memory (CPU VCCDDR) DECOUPLING

2x 220F 0805, 1x 1UF 0402

PLL (CPU VCCSFR) DECOUPLING

1x 220F 0805, 1x 4.7UF 0603, 1x 2.2UF 0402, 2x 1UF 0402

Instead call out appropriate BOM GROUP defined in tables above.

NOTE: BOM Configurations should not call out CPUPOCn, n=3-5, BOM OPTIONS directly. Instead call out appropriate BOM GROUP defined in tables above.
PLACEMENT_NOTE=Place R2501 close to R2500 to minimize stubs.
LVD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

MEM RESET ISOLATION

CPU_RESET_L    ISOLATE_L   MEM_RESET_L
0           3.3V         0
0           3.3V         0
1.5V        3.3V         1.5V
0           0            1.5V

S5
S0
S5
S0
S3
S0
S5
S0

DDR3 RESET Support

MEM RESET ISOLATION

CPU_RESET_L

CPU_RESET_L    CPU_RESET_L    CPU_RESET_L
0           3.3V         0
0           3.3V         0
1.5V        3.3V         1.5V
0           0            1.5V

S5
S0
S5
S0
S3
S0
S5
S0

DDR3 RESET

SYNC_DATE=01/06/2010
SYNC_MASTER=MATT
RTC Power Sources

Fault protection for RTC battery.

NOTE: R2800 and D2800 form the double.

unused PCH 25MHz crystal

Reset Button

Platform Reset Connections

Unbuffered

Recipient uses to move longer track due to Sustained

Buffered

Apple Inc.

CHIPSET SUPPORT
Power Sources:
FW_PHY0 nets are OHCI/PCIe power, and the
multi-part systems must come from bus power.
FWXIO_PHY nets are PHY power, and for

For all multi-part systems, all IC power should
be tied together and powered by either the

(Snoop Enable, for FireBug)
12 VOLTS
7 WATTS MAX PER PORT

IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V

PLACE CLOSE TO COMPARATOR

CRITICAL BOM OPTION

CRITICAL
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as inputs can be left floating, unused designated as inputs require pull-ups.
SMC Reset "Button", Supervisor & AVREF Supply

SMC Crystal Circuit

MEM_EVENT

POWER BUTTON

SILK_PART=SMC
RESET

SMC_SUPPORT

Apple Inc.

SMC Support

www.vinafix.vn
HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING

Drive active = valid signal protocol
Drive asleep = HDD drives HDD_OOB_TEMP low
Must pull high to 2.5V for compatibility with all drives

Drive disconnected = pulled high

LOW: -0.3V TO 0.5V
HIGH: 2.0V TO 3.6V

HDD TEMP SENSE
SYNC_MASTER=K74_MASTER
SYNC_DATE=N/A

=PP3V3_S0_SMC_LS
=PP3V3_S0_SMC_LS
=PP12V_S0_SENSE
HDD_OOB_1V60_REF
HDD_OOB_TEMP_R
HDD_OOB_TEMP_FILT

518S0698

Drive temp sensing level shifting

May pull high to 2.5V for compatibility with all drives

www.vinafix.vn
IBEX PEAK CORE REG 1.05V  OUTPUT = PP1V05_S0_REG

VOUT = 0.75*( 1+R7615/R7616) = 1.05V

IBEX PEAK CORE REG 1.05V  OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG

VOUT  = 1.05V
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

\[ V_{out} = 1.25V \times \left(1 + \frac{R_a}{R_b}\right) \]

\[ R_a = 348K \quad \text{and} \quad R_b = 200K \]

\[ C7901 = 22pF \quad \text{X5R-CERM} \]

\[ R7902 = 348K \quad \text{402} \quad 1\% \quad \text{1/16W} \]

\[ L7900 = 33UH \quad \text{CDPH4D19FHF-SM} \]

\[ C7902 = 22UF \quad \text{X5R} \quad 6.3V \]

\[ U7900 = \text{LT3470A DFN} \]

\[ C7900 = 0.22UF \quad \text{X5R} \quad 402 \quad 20\% \quad 6.3V \]

\[ R7901 = 402 \quad MF-LF \quad 1/16W \quad 1\% \quad 200K \]

\[ C7910 = 25V \quad 10\% \quad \text{X5R} \quad 805 \]

\[ V_{out} = 3.425 \quad \text{(Switcher limit)} \]
### PAGE NOTES

Signal aliases required by this page
- PP5V_S0_MXM

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### MXM TX CAPS

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<th>Component</th>
<th>Value</th>
<th>Location</th>
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</thead>
<tbody>
<tr>
<td>C8605</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8606</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8607</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8608</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8609</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
</tbody>
</table>

### MXM RX CAPS

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8610</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8611</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8612</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8613</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8614</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
</tbody>
</table>

### MXM PCIe Caps

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8620</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8621</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8622</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8623</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
<tr>
<td>C8624</td>
<td>0.1UF</td>
<td>DIM P150</td>
</tr>
</tbody>
</table>

---

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### Unused MXM Interfaces

<table>
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<th>Description</th>
</tr>
</thead>
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<tr>
<td>MXM_LVDS_B_DATA_N&lt;0&gt;</td>
<td>Unused MXM DP Interfaces</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_CLK_N</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_CLK_P</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_CLK_N</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_CLK_P</td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Interface Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;0&gt;</td>
<td>Unused MXM DP Interfaces</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_CLK_N</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_B_CLK_P</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_N&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_DATA_P&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_CLK_N</td>
<td></td>
</tr>
<tr>
<td>MXM_LVDS_A_CLK_P</td>
<td></td>
</tr>
</tbody>
</table>

### Unused MXM Control Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC_MXM_LVDS_B_CLK_P</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_P&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_P&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_P&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_P&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_CLK_P</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_CLK_N</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_N&lt;0&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_N&lt;1&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_N&lt;2&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
<tr>
<td>NC_MXM_LVDS_B_DATA_N&lt;3&gt;</td>
<td></td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td></td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td></td>
</tr>
</tbody>
</table>

### DISPLAY AUDIO MUX NOT USED - SEND SPDIF TO CODEC

- **AUD_SPDIF_IN_CODEC**
- **TP_DP_INT_SPDIF_AUDIO**
- **DP_INT_SPDIF_AUDIO**

---

**Page Notes**: Unused aliases required by this page:

- **Display: Aliases**
- **Signal aliases required by this page**
- **Unused MXM DP Interfaces**
- **Unused MXM Interfaces**
- **Unused MXM CONTROL SIGNALS**

**Page Title**: Page Notes

**Branch**: 3

**Revision**: D

**Drawing Number**: 051-8337 A.0.0

**Size**: 21 OF 110

**Sheet**: 3

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**Display: Aliases**

- **MXM_LVDS_B_DATA_N<0>**
- **MXM_LVDS_B_DATA_P<0>**
- **MXM_LVDS_B_DATA_N<1>**
- **MXM_LVDS_B_DATA_P<1>**
- **MXM_LVDS_B_DATA_N<2>**
- **MXM_LVDS_B_DATA_P<2>**
- **MXM_LVDS_B_DATA_N<3>**
- **MXM_LVDS_B_DATA_P<3>**
- **MXM_LVDS_B_CLK_N**
- **MXM_LVDS_B_CLK_P**
- **MXM_LVDS_A_DATA_N<0>**
- **MXM_LVDS_A_DATA_P<0>**
- **MXM_LVDS_A_DATA_N<1>**
- **MXM_LVDS_A_DATA_P<1>**
- **MXM_LVDS_A_DATA_N<2>**
- **MXM_LVDS_A_DATA_P<2>**
- **MXM_LVDS_A_DATA_N<3>**
- **MXM_LVDS_A_DATA_P<3>**
- **MXM_LVDS_A_CLK_N**
- **MXM_LVDS_A_CLK_P**

---

**Display Options**: Provided by this page:

- **(NONE)**

**Power Aliases**: Required by this page:

- **(NONE)**

---

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### Memory Bus Constraints

<table>
<thead>
<tr>
<th>NET_NAME</th>
<th>NET_TYPE</th>
<th>LAYER</th>
<th>MEM_DQ_EVEN</th>
<th>MEM_DQ_EVEN2DQ_EVEN</th>
<th>MEM_DQ_EVEN2DQ_ODD</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_DQ_EVEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_EVEN2DQ_EVEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_EVEN2DQ_ODD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>NET_NAME</th>
<th>NET_TYPE</th>
<th>LAYER</th>
<th>MEM_DQ_EVEN</th>
<th>MEM_DQ_EVEN2DQ_EVEN</th>
<th>MEM_DQ_EVEN2DQ_ODD</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_DQ_EVEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_EVEN2DQ_EVEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_EVEN2DQ_ODD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Memory Net Properties

<table>
<thead>
<tr>
<th>NET_NAME</th>
<th>NET_TYPE</th>
<th>LAYER</th>
<th>MEM_DQ_EVEN</th>
<th>MEM_DQ_EVEN2DQ_EVEN</th>
<th>MEM_DQ_EVEN2DQ_ODD</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_DQ_EVEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_EVEN2DQ_EVEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_EVEN2DQ_ODD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Memory Power Properties

- **Memory Power Properties**
  - **MINIMUM LINE WIDTH**
    - MEM_DQ_EVEN: 35_OHM_SE
    - MEM_DQ_EVEN2DQ_EVEN: 39_OHM_SE
  - **MINIMUM NECK WIDTH**
    - MEM_DQ_EVEN: 0.2 MM
  - **MAXIMUM NECK LENGTH**
    - MEM_DQ_EVEN: 70_OHM_DIFF
  - **STANDARD**
    - **TABLE_SPACING_RULE_ITEM**
      - AREA_TYPE = STANDARD
    - **TABLE_SPACING_ASSIGNMENT_ITEM**
      - AREA_TYPE = STANDARD

---

**Memory Constraints**

Apple Inc.

051-8337

A.0.0

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### HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>NET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>PHYSICAL_RULE_SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDA</td>
<td>SMB</td>
<td>SMB</td>
<td>SMB</td>
<td>SMB</td>
<td>SMB</td>
<td>SMB</td>
<td>SMB</td>
<td>SMB</td>
</tr>
</tbody>
</table>

#### PHYSICAL RULE SET

- **SPACING RULE SET**
  - **CLK_PCH_55S**
  - **SMB_55S**
  - **CLK_PCI_55S**
  - **CLK_LPC**

#### LAYER

- **XTAL**
  - **HDA**
  - **SMB**
  - **LPC**

#### SPI annually

- **LINE-TO-LINE SPACING**
  - **ON LAYER?**
    - **=100_OHM_DIFF**
    - **=55_OHM_SE**

- **ALLOW ROUTE ON LAYER?**
  - **=2x_DIELECTRIC**
  - **=4X_DIELECTRIC**

- **MINIMUM LINE WIDTH**
  - **=55_OHM_SE**
  - **=2X_DIELECTRIC**

- **MINIMUM NECK WIDTH**
  - **=100_OHM_DIFF**
  - **=55_OHM_SE**

- **MAXIMUM NECK LENGTH**
  - **=2X_DIELECTRIC**
  - **=4X_DIELECTRIC**

- **DIFFPAIR PRIMARY GAP**
  - **=90_OHM_DIFF**
  - **=STANDARD**

- **DIFFPAIR NECK GAP**
  - **=STANDARD**
  - **=100_OHM_DIFF**

- **DIFFPAIR_secondary GAP**
  - **=55_OHM_SE**

#### PHYSICAL RULE HEAD

- **TABLE_PHYSICAL_RULE_HEAD**
  - **TABLE_PHYSICAL_RULE_ITEM**
    - **TABLE_PHYSICAL_RULE_HEAD**
      - **TABLE_PHYSICAL_RULE_ITEM**

#### SPACING RULE HEAD

- **TABLE_SPACING_RULE_HEAD**
  - **TABLE_SPACING_RULE_ITEM**
    - **TABLE_SPACING_RULE_ITEM**
      - **TABLE_SPACING_RULE_ITEM**

---

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- **85 OF 92**

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CAESAR II (ETHERNET) CONSTRAINTS

CAESAR IV (SD) CONSTRAINTS

FireWire Interface Constraints

AUDIO CONSTRAINTS

AUDIO NET PROPERTIES
### PM NET PROPERTIES

**Net Type**: PM, RESET, EN, PGOOD

#### Net Spacing

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Net Spacing Type 1</th>
<th>Net Spacing Type 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM_VTT</td>
<td>3:1 Spacing</td>
<td>2:1 Spacing</td>
</tr>
</tbody>
</table>

#### Physically Assigned Items

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Net Type</th>
<th>Net Type</th>
<th>Net Type</th>
<th>Net Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM_GND</td>
<td>PM_GND</td>
<td>PM_GND</td>
<td>PM_GND</td>
<td>PM_GND</td>
</tr>
</tbody>
</table>

#### Spacing Rule Set

- 3:1 Spacing
- 2:1 Spacing

---

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**Sync Master:** K74_MASTER

**Sync Date:** N/A

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**Branch:** 109 of 110

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**Sync Date:** N/A

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