

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K60 MLB

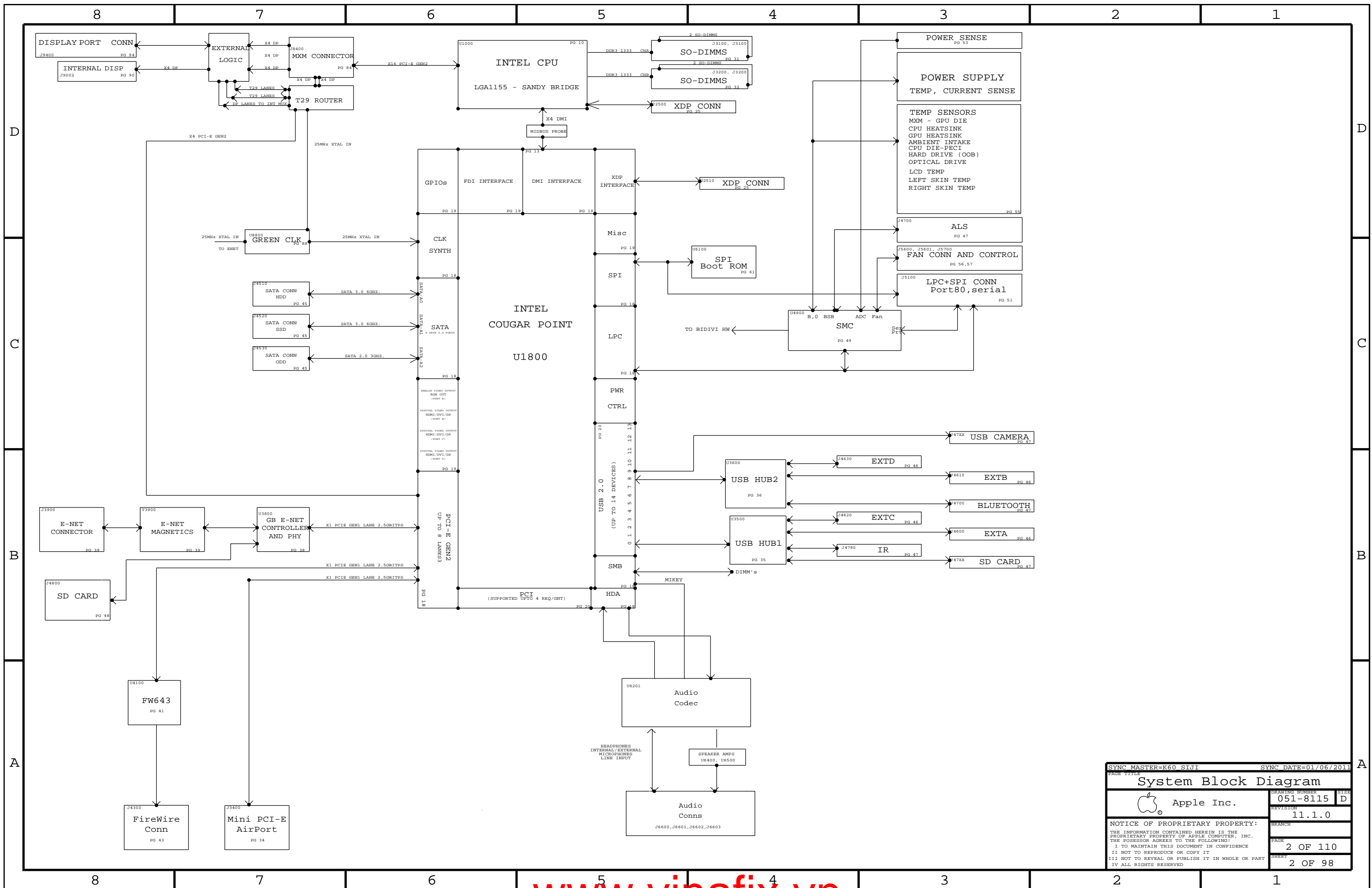
REV	ECN	DESCRIPTION OF REVISION	DATE
		APPD	2011-02-08

LAST_MODIFIED=Tue Feb 8 14:39:56 2011

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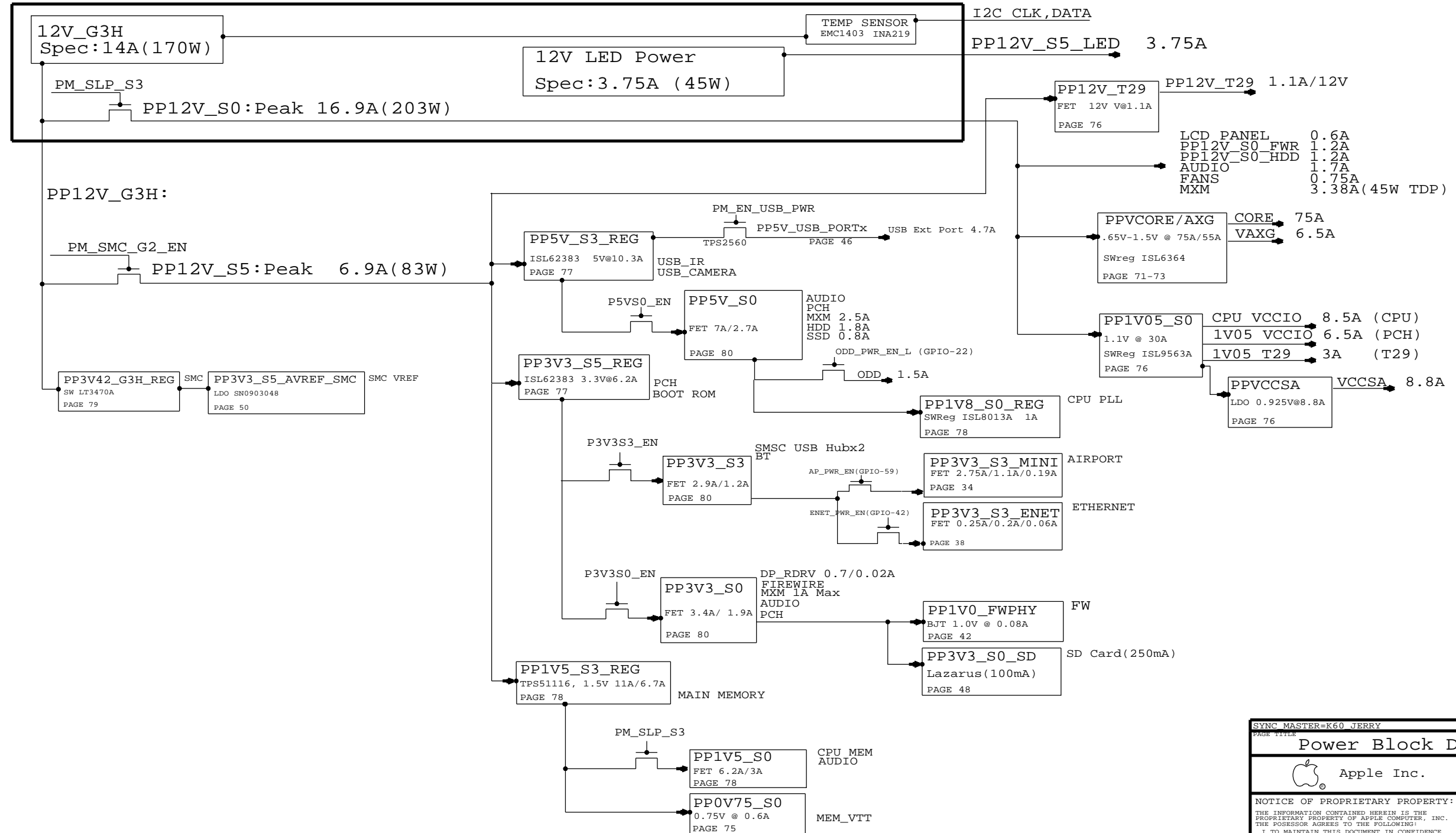
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DRAWING TITLE		SCH, K60, MLB	
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	REVISION	11.1.0	
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SYNC MASTER=K60 SIJI		SYNC DATE=01/06/2011	
System Block Diagram			
Apple Inc.		DRAWING NUMBER	051-8115
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AC/DC POWER SUPPLY (Spec:215W)



SYNC MASTER=K60_JERRY		SYNC DATE=01/06/2011
Power Block Diagram		
Apple Inc.	DRAWING NUMBER 051-8115	SIZE D
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	BRANCH	SHEET 3 OF 98

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-0801	PCBA,MLB,DEV,K60	DEVELOPMENT,DEV_GROUP
639-1767	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1820	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1821	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-2160	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2159	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2161	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2118	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2122	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2119	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2132	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2133	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2134	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_LV5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE,HUB_USX2061,PRODUCTION,VAXG,SSD
BASIC2	AP,BT,IR,T29
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_LV5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51180071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
51180073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2452	SUB ASSY,CPU SOCKET,K60,TYCO	TYCO_SOCKET
085-2453	SUB ASSY,CPU SOCKET,K60,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2452	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2453	085-2452		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33784088	1	IC,CONGAR POINT,SL74F,8D82268,PRQ,B3	U1800	CRITICAL	
35383055	1	IC,P13VEDP212,X2 DP MIX,QFN	U9390	CRITICAL	
33880753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
34380534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW: 33580807	1	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL	
RAW: 33580539	1	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL	
33880945	1	T29 ROUTER, IC ASSP	U9700	CRITICAL	T29
34170257	1	IC,T29,SERIAL EEPROM	U9790	CRITICAL	T29
RAW: 33783997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29
RAW: 33580709	1	IC,MXM SYS ROM,24C02	U8570	CRITICAL	
RAW: 33880878	1	IC,SMC,K60	U4900	CRITICAL	K60

CPU


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33784043	1	SNB,S8008,PRQ,D2,2.5,65W,4+1.6M,LGA	CPU	CRITICAL	2P5GHZ_SNB_CPU_PRQ
33784062	1	SNB,S8009,PRQ,D2,2.7,65W,4+1.6M,LGA	CPU	CRITICAL	2P7GHZ_SNB_CPU_PRQ
33784061	1	SNB,S8008,PRQ,D2,2.8,65W,4+1.8M,LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU_PRQ

K60 PARTS

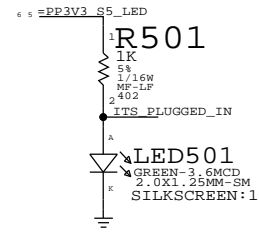
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8115	1	SCH,MLB,K60	SCH1		K60
820-2641	1	PCBF,MLB,K60	MLB1		K60

K60 ALTERNATE PARTS

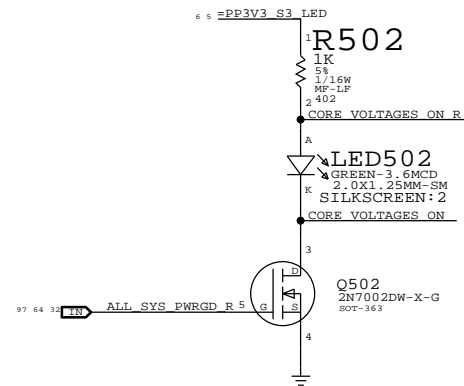
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293			330UF
371S0679	371S0652			PIN DIODE
377S0107	377S0066			USB DIODE
376S0972	376S0612			ROHM TRA-BJT

SYNC MASTER=K60 AARON		SYNC DATE=N/A	
BOM Configuration			
 Apple Inc.		DRAWING NUMBER	051-8115
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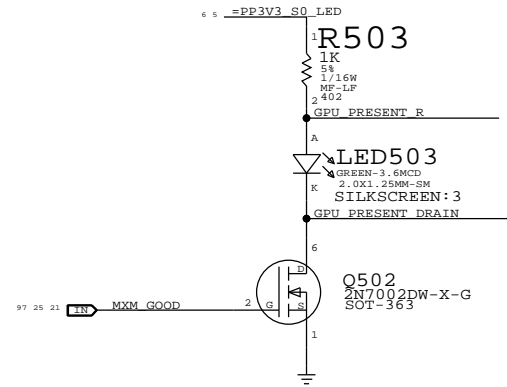
S5 Led



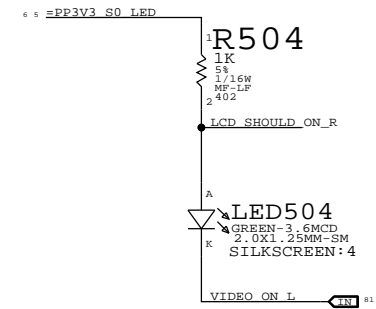
ALL_SYS_PWRGD Led



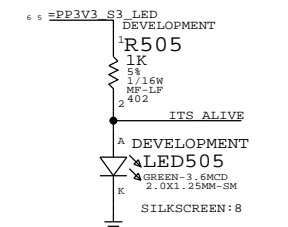
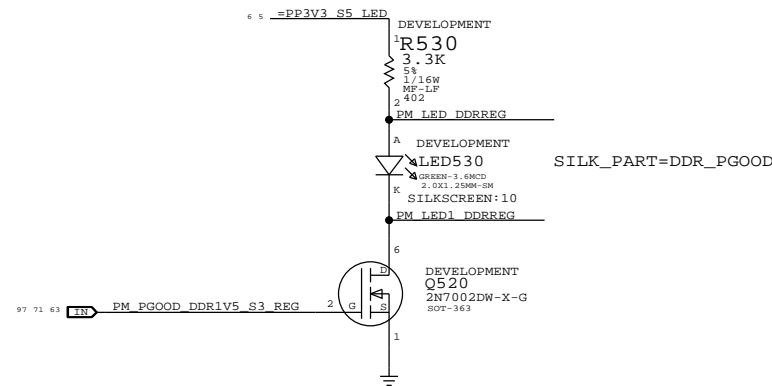
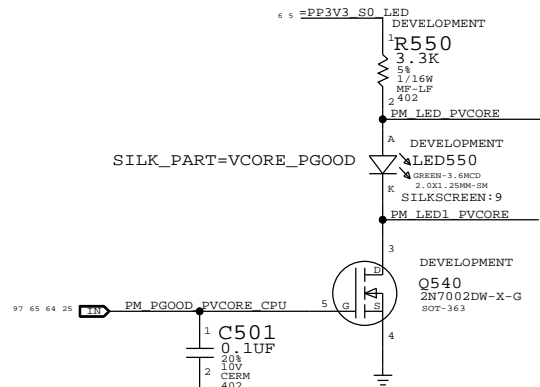
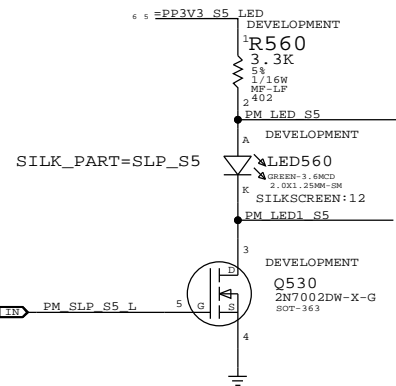
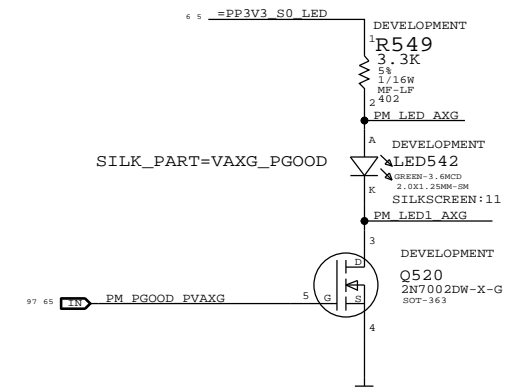
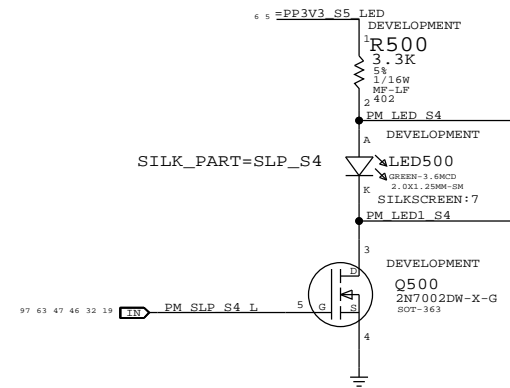
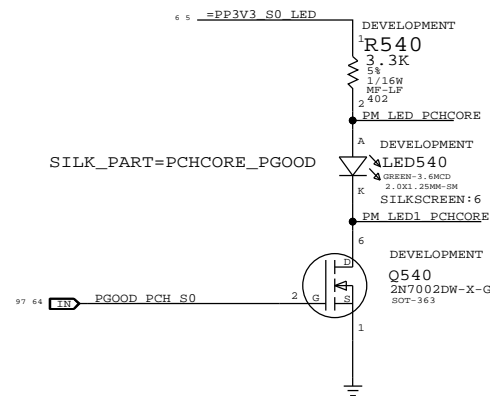
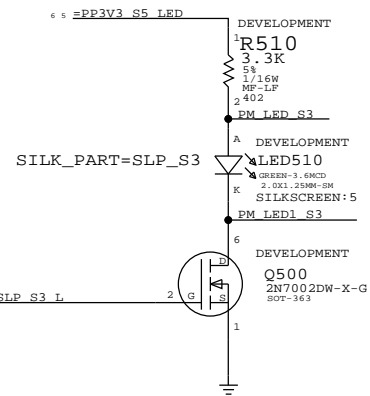
MXM PWR GOOD Led



VIDEO ON Led

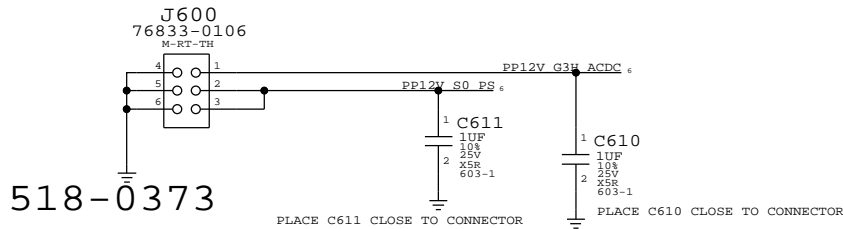


PROTO DEBUG LEDS ARE SHOWN BELOW



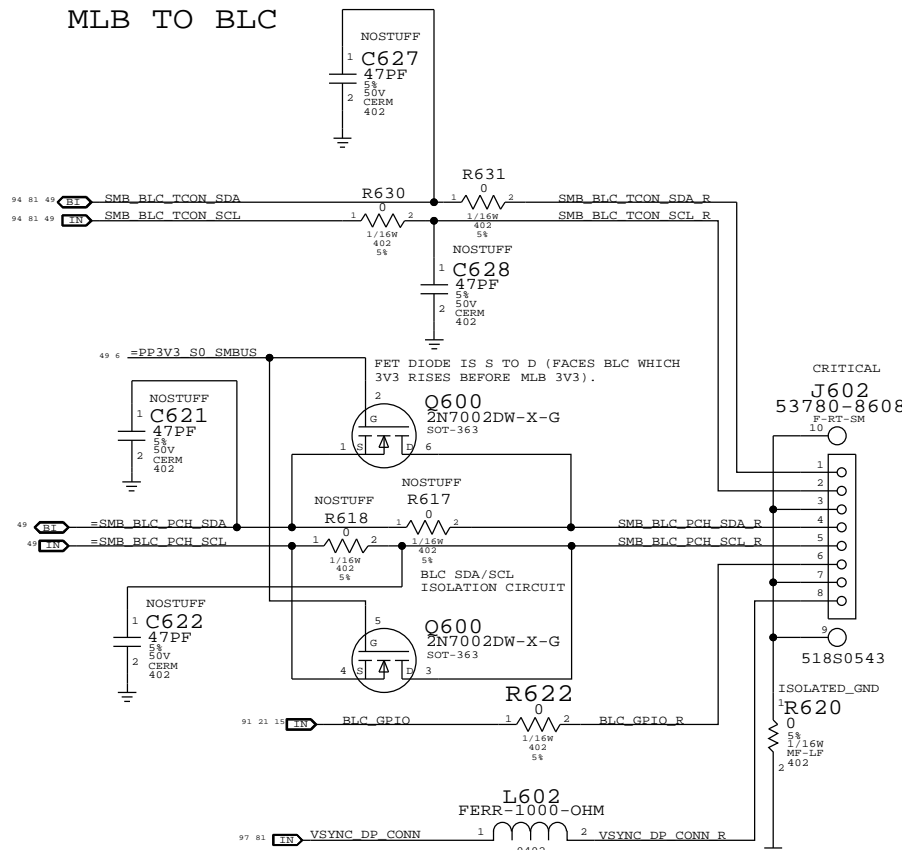
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DEBUG LEDS			
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POWER SUPPLY TO MLB

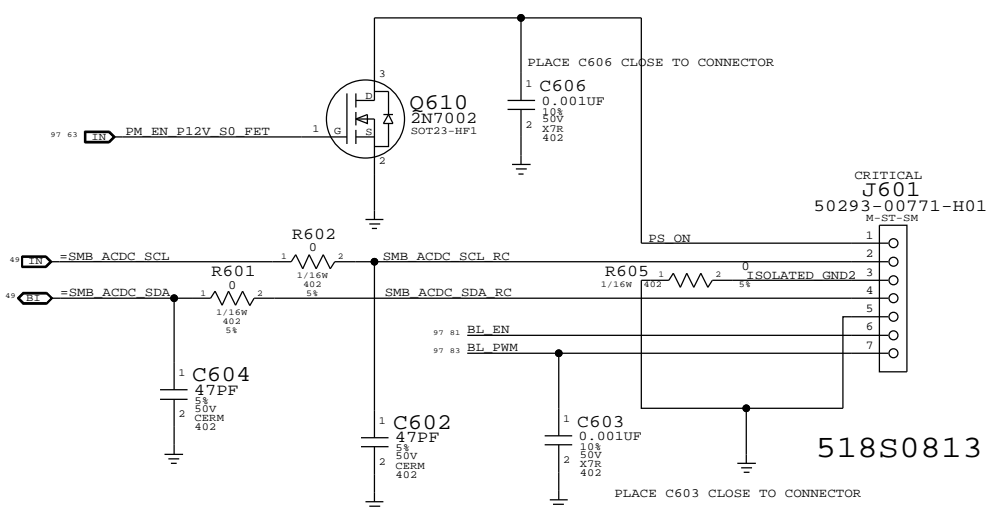


518-0373

MLB TO BLC



MLB TO PS



- List of power rail aliases including PP0V75 S0, PPVTT S0 DDR, PFCORE S0 CPU, PPVAG S0 REG, PPV05 S0, PPV05 S0 PCH, PPV05 S0 CPU MEM, PP3V3 S0, PP1V5 S3, and PP5V S3.

"S0" RAILS ONLY ON IN RUN

- List of "S0" rail aliases including PP1V8 S0, PP5V S0, and PP12V S0.

"S3" RAILS ON IN RUN AND SLEEP

- List of "S3" rail aliases including PP1V5 S3, PP3V3 S3, and PP5V S3.

"S5" RAILS ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

- List of "S5" rail aliases including PP3V3 S5, PP5V S5, and PP12V S5.

"G3H" RAILS ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

- List of "G3H" rail aliases including PP3V42 G3H, PP12V G3H, and PP3V3 S0 T29.

T29 RAILS

- List of T29 rail aliases including PP3V3 S0 T29 and PP1V05 S0 T29.

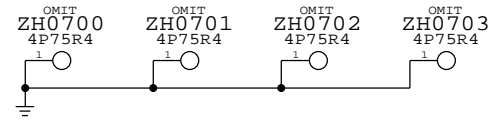
GND RAILS

- List of GND rail aliases including GND.

Table with metadata: SYNC MASTER=K60 MARK, SYNC DATE=12/30/2010, Power Conn / Alias, Apple Inc., DRAWING NUMBER 051-8115, SIZE D, REVISION 11.1.0, PAGE 6 OF 110, SHEET 6 OF 98.

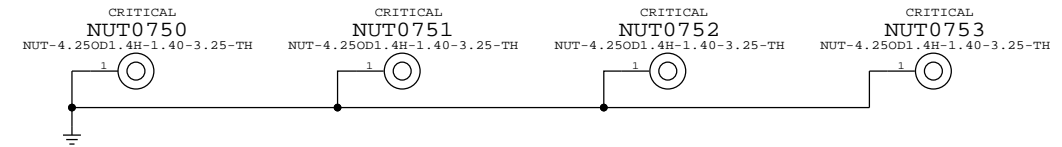
CPU Heatsink

4mm Plated Holes (998-0850)



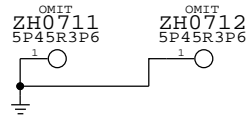
DIMM CONNECTOR NUTS

Nuts (805-9582)



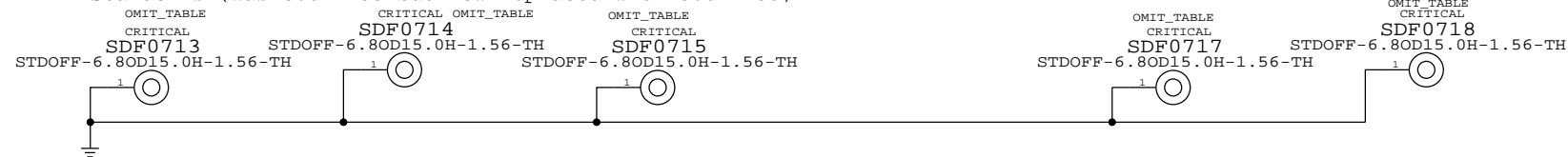
PCH HEATSINK

MOUNTING HOLES (998-0873, 998-0976)



Rear Cover

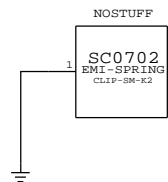
Standoffs (was 860-1255 but now replaced with 860-1430)



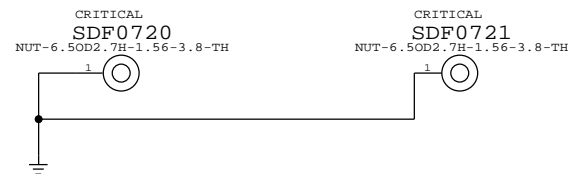
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	5	STANDOFF,MLB,K60/K62	SDF0713,SDF0714,SDF0715,SDF0717,SDF0718	

For EMC

EMC Spring (870-1577); Near DIMMs



MXM STANDOFFS (835-0272)



SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
Holes			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8115	D
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UNUSED CPU SIGNALS

TP CPU RSVD<16..1> == NC CPU RSVD<16..1>
TP CPU RSVD<46..19> == NC CPU RSVD<46..19>

NC ON UNUSED PCIE ALIASES

TP PCIE CLK100M PE5P == NC PCIE CLK100M PE5P
TP PCIE CLK100M PE5N == NC PCIE CLK100M PE5N
TP PCIE CLK100M PE6P == NC PCIE CLK100M PE6P
TP PCIE CLK100M PE6N == NC PCIE CLK100M PE6N
TP PCIE CLK100M PE7P == NC PCIE CLK100M PE7P
TP PCIE CLK100M PE7N == NC PCIE CLK100M PE7N
TP PE RX N<3..0> == NC PE RXN<3..0>
TP PE RX P<3..0> == NC PE RXP<3..0>
TP PE TX N<3..0> == NC PE TXN<3..0>
TP PE TX P<3..0> == NC PE TXP<3..0>
TP PCIE D2R PERN4 == NC PCIE D2R PERN4
TP PCIE D2R PERP4 == NC PCIE D2R PERP4
TP PCIE R2D PETN4 == NC PCIE R2D PETN4
TP PCIE R2D PETP4 == NC PCIE R2D PETP4
TP PCIE CLK100M PE4P == NC PCIE CLK100M PE4P
TP PCIE CLK100M PE4N == NC PCIE CLK100M PE4N

NC ON UNUSED PCI ALIASES

TP PCI AD<31..0> == NC PCI AD<31..0>
TP PCI C BE L<3..0> == NC PCI C BE L<3..0>
TP PCI PAR == NC PCI PAR
TP PCI RESET L == NC PCI RESET L
TP LPC DREQ0 L == NC LPC DREQ0 L

NC ON UNUSED MEM ALIASES

TP MEM A DO CB<7..0> == NC MEM A DO CB<7..0>
TP MEM A DOS N<8> == NC MEM A DOSN<8>
TP MEM A DOS P<8> == NC MEM A DOSP<8>
TP MEM B DO CB<7..0> == NC MEM B DO CB<7..0>
TP MEM B DOS N<8> == NC MEM B DOSN<8>
TP MEM B DOS P<8> == NC MEM B DOSP<8>

NC ON UNUSED MISC ALIASES

TP HDA SDIN1 == NC HDA SDIN1
TP HDA SDIN2 == NC HDA SDIN2
TP HDA SDIN3 == NC HDA SDIN3
TP PCH PWM0 == NC PCH PWM0
TP PCH PWM1 == NC PCH PWM1
TP PCH PWM2 == NC PCH PWM2
TP PCH PWM3 == NC PCH PWM3
TP PCH SST == NC PCH SST
TP PCH CL CLK1 == NC PCH CL CLK1
TP PCH CL DATA1 == NC PCH CL DATA1
TP PCH CL RST1 == NC PCH CL RST1

NC ON UNUSED DISPLAY ALIASES

TP CRT IG DDC CLK == NC CRT IG DDC CLK
TP CRT IG DDC DATA == NC CRT IG DDC DATA
TP CRT IG RED == NC CRT IG RED
TP CRT IG GREEN == NC CRT IG GREEN
TP CRT IG BLUE == NC CRT IG BLUE
TP CRT IG HSYNC == NC CRT IG HSYNC
TP CRT IG VSYNC == NC CRT IG VSYNC
TP DP IG B MLN<3..0> == NC DP IG B MLN<3..0>
TP DP IG B MLP<3..0> == NC DP IG B MLP<3..0>
TP DP IG B AUX N == NC DP IG B AUXN
TP DP IG B AUX P == NC DP IG B AUXP
TP DP IG B HPD == NC DP IG B HPD
TP DP IG B DDC CLK == NC DP IG B DDC CLK
TP DP IG B DDC DATA == NC DP IG B DDC DATA
TP DP IG C MLN<3..0> == NC DP IG C MLN<3..0>
TP DP IG C MLP<3..0> == NC DP IG C MLP<3..0>
TP DP IG C AUX N == NC DP IG C AUXN
TP DP IG C AUX P == NC DP IG C AUXP
TP DP IG C HPD == NC DP IG C HPD
TP DP IG C CTRL CLK == NC DP IG C CTRL CLK
TP DP IG C CTRL DATA == NC DP IG C CTRL DATA
TP DP IG D MLN<3..0> == NC DP IG D MLN<3..0>
TP DP IG D MLP<3..0> == NC DP IG D MLP<3..0>
TP DP IG D AUXN == NC DP IG D AUXN
TP DP IG D AUXP == NC DP IG D AUXP
TP DP IG D HPD == NC DP IG D HPD
TP DP IG D CTRL CLK == NC DP IG D CTRL CLK
TP DP IG D CTRL DATA == NC DP IG D CTRL DATA
TP SDVO TVCLKINN == NC SDVO TVCLKINN
TP SDVO TVCLKINP == NC SDVO TVCLKINP
TP SDVO STALLN == NC SDVO STALLN
TP SDVO STALLP == NC SDVO STALLP
TP SDVO INTN == NC SDVO INTN
TP SDVO INTP == NC SDVO INTP
TP PCH L BKLCTCTL == NC PCH L BKLCTCTL
TP PCH L BKLITEN == NC PCH L BKLITEN
TP PCH L VDD EN == NC PCH L VDD EN
TP PCH CLKOUT DPN == NC PCH CLKOUT DPN
TP PCH CLKOUT DPP == NC PCH CLKOUT DPP

NC ON UNUSED FDI ALIASES

TP CPU FDI TX N<7..0> == NC CPU FDI TXN<7..0>
TP CPU FDI TX P<7..0> == NC CPU FDI TXP<7..0>
TP PCH FDI RX N<7..0> == NC PCH FDI RXN<7..0>
TP PCH FDI RX P<7..0> == NC PCH FDI RXP<7..0>

NC ON UNUSED SATA ALIASES

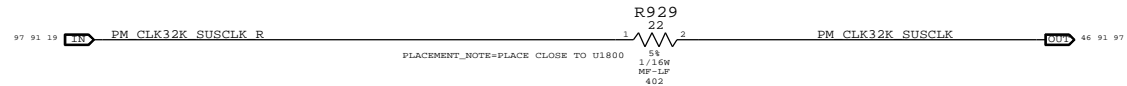
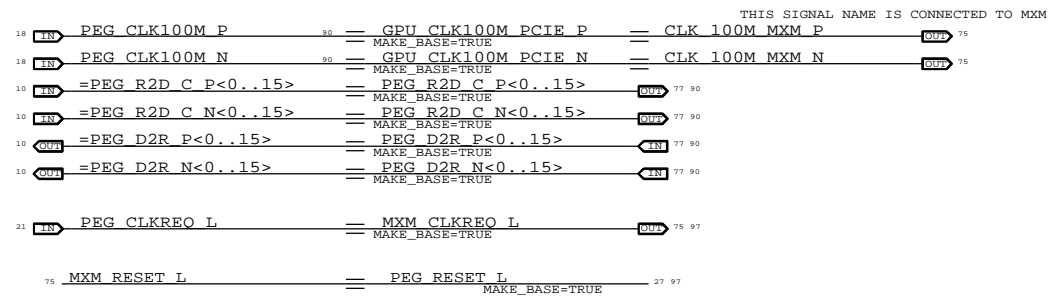
TP SATA D D2RN == NC SATA D D2RN
TP SATA D D2RP == NC SATA D D2RP
TP SATA D R2D CN == NC SATA D R2D CN
TP SATA D R2D CP == NC SATA D R2D CP
TP SATA E D2RN == NC SATA E D2RN
TP SATA E D2RP == NC SATA E D2RP
TP SATA E R2D CN == NC SATA E R2D CN
TP SATA E R2D CP == NC SATA E R2D CP
TP SATA F D2RN == NC SATA F D2RN
TP SATA F D2RP == NC SATA F D2RP
TP SATA F R2D CN == NC SATA F R2D CN
TP SATA F R2D CP == NC SATA F R2D CP

NC ON UNUSED USB ALIASES

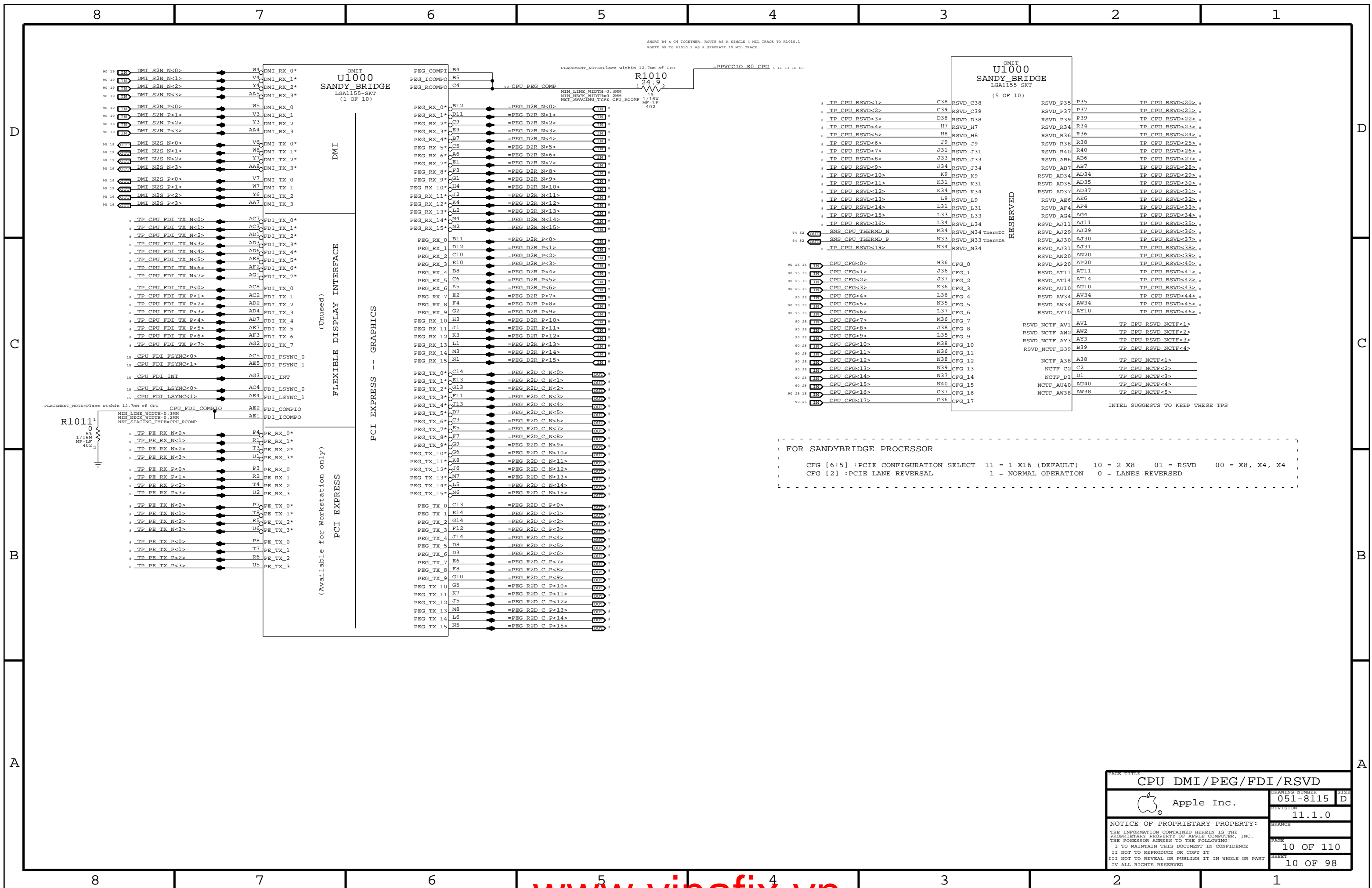
TP USB 1N == NC USB 1N
TP USB 1P == NC USB 1P
TP USB 2N == NC USB 2N
TP USB 2P == NC USB 2P
TP USB 3N == NC USB 3N
TP USB 3P == NC USB 3P
TP USB 4N == NC USB 4N
TP USB 4P == NC USB 4P
TP USB 5N == NC USB 5N
TP USB 5P == NC USB 5P
TP USB 6N == NC USB 6N
TP USB 6P == NC USB 6P
TP USB 7N == NC USB 7N
TP USB 7P == NC USB 7P
TP USB 10N == NC USB 10N
TP USB 10P == NC USB 10P
TP USB 11N == NC USB 11N
TP USB 11P == NC USB 11P
TP USB 12N == NC USB 12N
TP USB 12P == NC USB 12P
TP USB 13N == NC USB 13N
TP USB 13P == NC USB 13P

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UNUSED SIGNAL ALIAS
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PEG Slot Support



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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
 ROUTE B5 TO R1010.1 AS A SEPARATE 10 MIL TRACE.

PLACEMENT_NOTE=Place within 12.7MM of CPU
 =PEVCCIO S0 CPU 6 11 13 16 65

R1010
 24.9
 1/16W MF-LP 402

MIN_LINE_WIDTH=0.3MM
 MIN_NECK_WIDTH=0.2MM
 NET_SPACING_TYPR=CPU_RCOMP

OMIT
 U1000
 SANDY BRIDGE
 LGA1155-SKT
 (5 OF 10)

TP CPU RSVD<1>	C38	RSVD_C38	RSVD_P35	P35	TP CPU RSVD<20>
TP CPU RSVD<2>	C39	RSVD_C39	RSVD_P37	P37	TP CPU RSVD<21>
TP CPU RSVD<3>	D38	RSVD_D38	RSVD_P39	P39	TP CPU RSVD<22>
TP CPU RSVD<4>	H7	RSVD_H7	RSVD_R34	R34	TP CPU RSVD<23>
TP CPU RSVD<5>	H8	RSVD_H8	RSVD_R36	R36	TP CPU RSVD<24>
TP CPU RSVD<6>	J9	RSVD_J9	RSVD_R38	R38	TP CPU RSVD<25>
TP CPU RSVD<7>	J31	RSVD_J31	RSVD_R40	R40	TP CPU RSVD<26>
TP CPU RSVD<8>	J33	RSVD_J33	RSVD_AB6	AB6	TP CPU RSVD<27>
TP CPU RSVD<9>	J34	RSVD_J34	RSVD_AB7	AB7	TP CPU RSVD<28>
TP CPU RSVD<10>	K9	RSVD_K9	RSVD_AD34	AD34	TP CPU RSVD<29>
TP CPU RSVD<11>	K31	RSVD_K31	RSVD_AD35	AD35	TP CPU RSVD<30>
TP CPU RSVD<12>	K34	RSVD_K34	RSVD_AD37	AD37	TP CPU RSVD<31>
TP CPU RSVD<13>	L9	RSVD_L9	RSVD_AE6	AE6	TP CPU RSVD<32>
TP CPU RSVD<14>	L31	RSVD_L31	RSVD_AF4	AF4	TP CPU RSVD<33>
TP CPU RSVD<15>	L33	RSVD_L33	RSVD_AG4	AG4	TP CPU RSVD<34>
TP CPU RSVD<16>	L34	RSVD_L34	RSVD_AJ11	AJ11	TP CPU RSVD<35>
SNS CPU THERMD N	M34	RSVD_M34 ThermoDA	RSVD_AJ29	AJ29	TP CPU RSVD<36>
SNS CPU THERMD P	N33	RSVD_N33 ThermoDA	RSVD_AJ30	AJ30	TP CPU RSVD<37>
TP CPU RSVD<19>	N34	RSVD_N34	RSVD_AJ31	AJ31	TP CPU RSVD<38>
CPU_CFG<0>	H36	CFG_0	RSVD_AN20	AN20	TP CPU RSVD<39>
CPU_CFG<1>	J36	CFG_1	RSVD_AP20	AP20	TP CPU RSVD<40>
CPU_CFG<2>	J37	CFG_2	RSVD_AT11	AT11	TP CPU RSVD<41>
CPU_CFG<3>	K36	CFG_3	RSVD_AT14	AT14	TP CPU RSVD<42>
CPU_CFG<4>	L36	CFG_4	RSVD_AU10	AU10	TP CPU RSVD<43>
CPU_CFG<5>	N35	CFG_5	RSVD_AV34	AV34	TP CPU RSVD<44>
CPU_CFG<6>	L37	CFG_6	RSVD_AW34	AW34	TP CPU RSVD<45>
CPU_CFG<7>	M36	CFG_7	RSVD_AY10	AY10	TP CPU RSVD<46>
CPU_CFG<8>	J38	CFG_8	RSVD_NCTF_AV1	AV1	TP CPU RSVD NCTF<1>
CPU_CFG<9>	L35	CFG_9	RSVD_NCTF_AV2	AW2	TP CPU RSVD NCTF<2>
CPU_CFG<10>	M38	CFG_10	RSVD_NCTF_AV3	AY3	TP CPU RSVD NCTF<3>
CPU_CFG<11>	N36	CFG_11	RSVD_NCTF_B39	B39	TP CPU RSVD NCTF<4>
CPU_CFG<12>	N38	CFG_12	NCTF_A38	A38	TP CPU NCTF<1>
CPU_CFG<13>	N39	CFG_13	NCTF_C2	C2	TP CPU NCTF<2>
CPU_CFG<14>	N37	CFG_14	NCTF_D1	D1	TP CPU NCTF<3>
CPU_CFG<15>	N40	CFG_15	NCTF_AU40	AU40	TP CPU NCTF<4>
CPU_CFG<16>	G37	CFG_16	NCTF_AW38	AW38	TP CPU NCTF<5>
CPU_CFG<17>	G36	CFG_17			

RESERVED

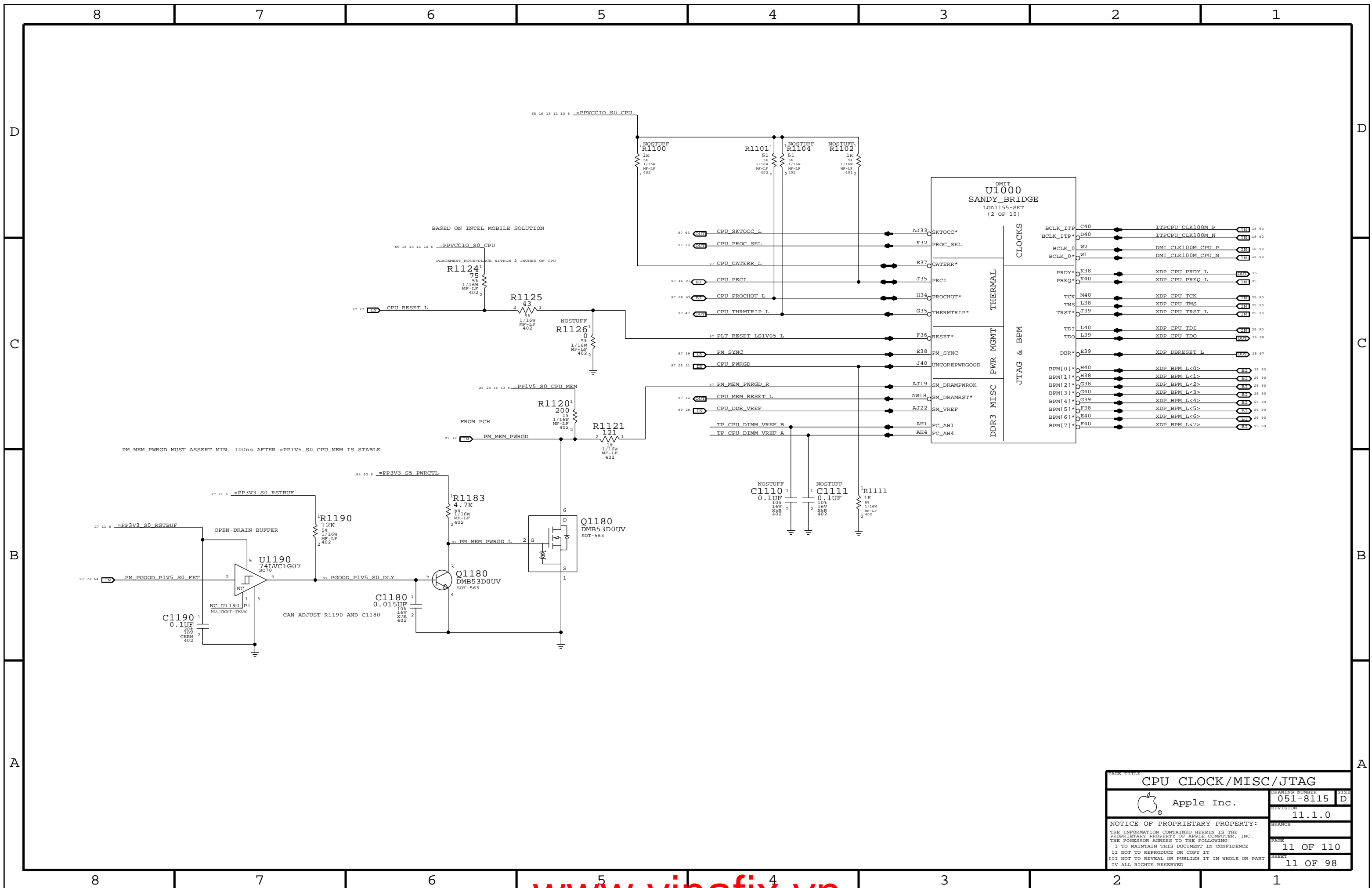
INTEL SUGGESTS TO KEEP THESE TPS

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4

CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE		CPU DMI/PEG/FDI/RSVD	
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CPU CLOCK/MISC/JTAG		
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D

C

B

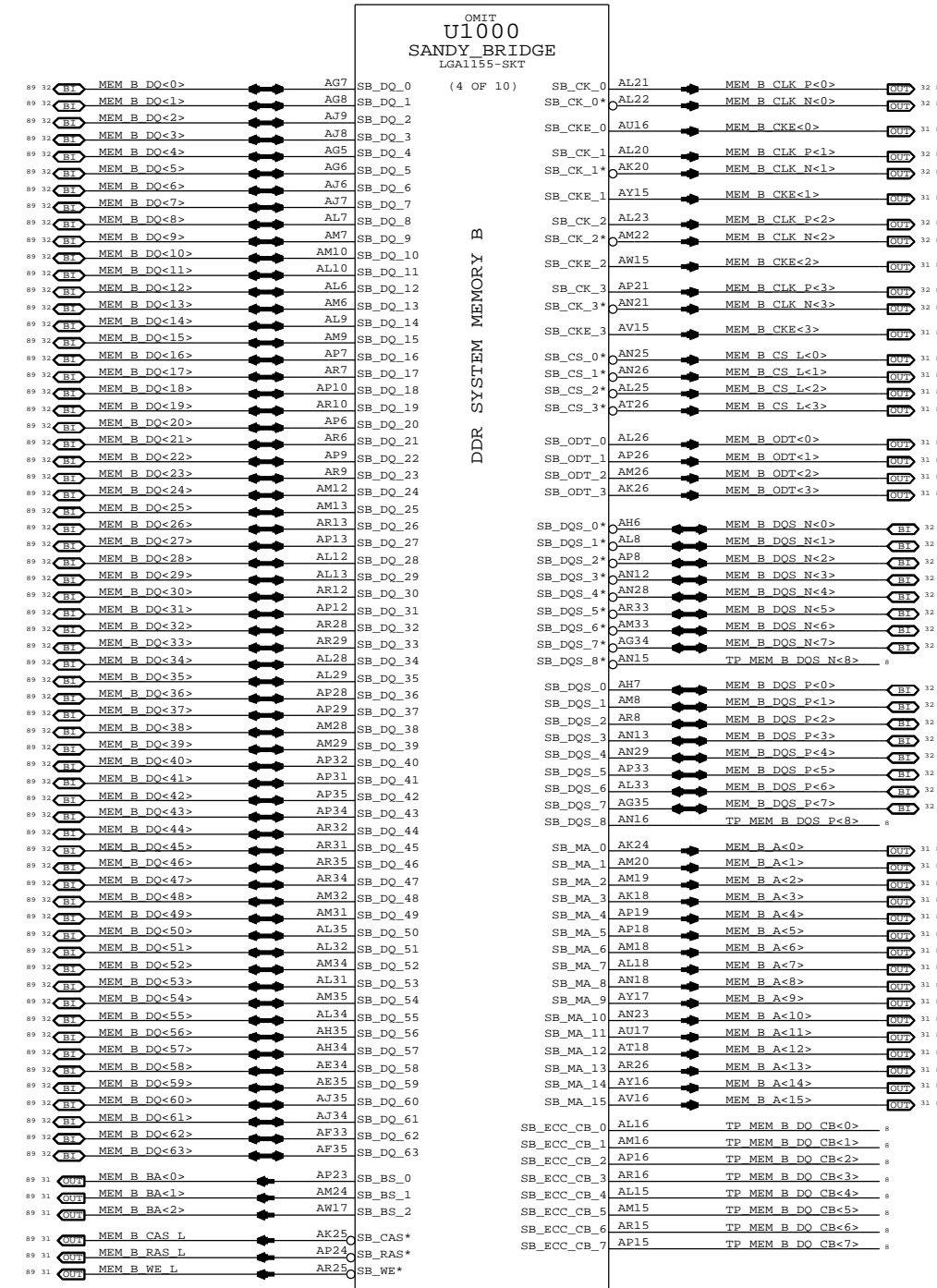
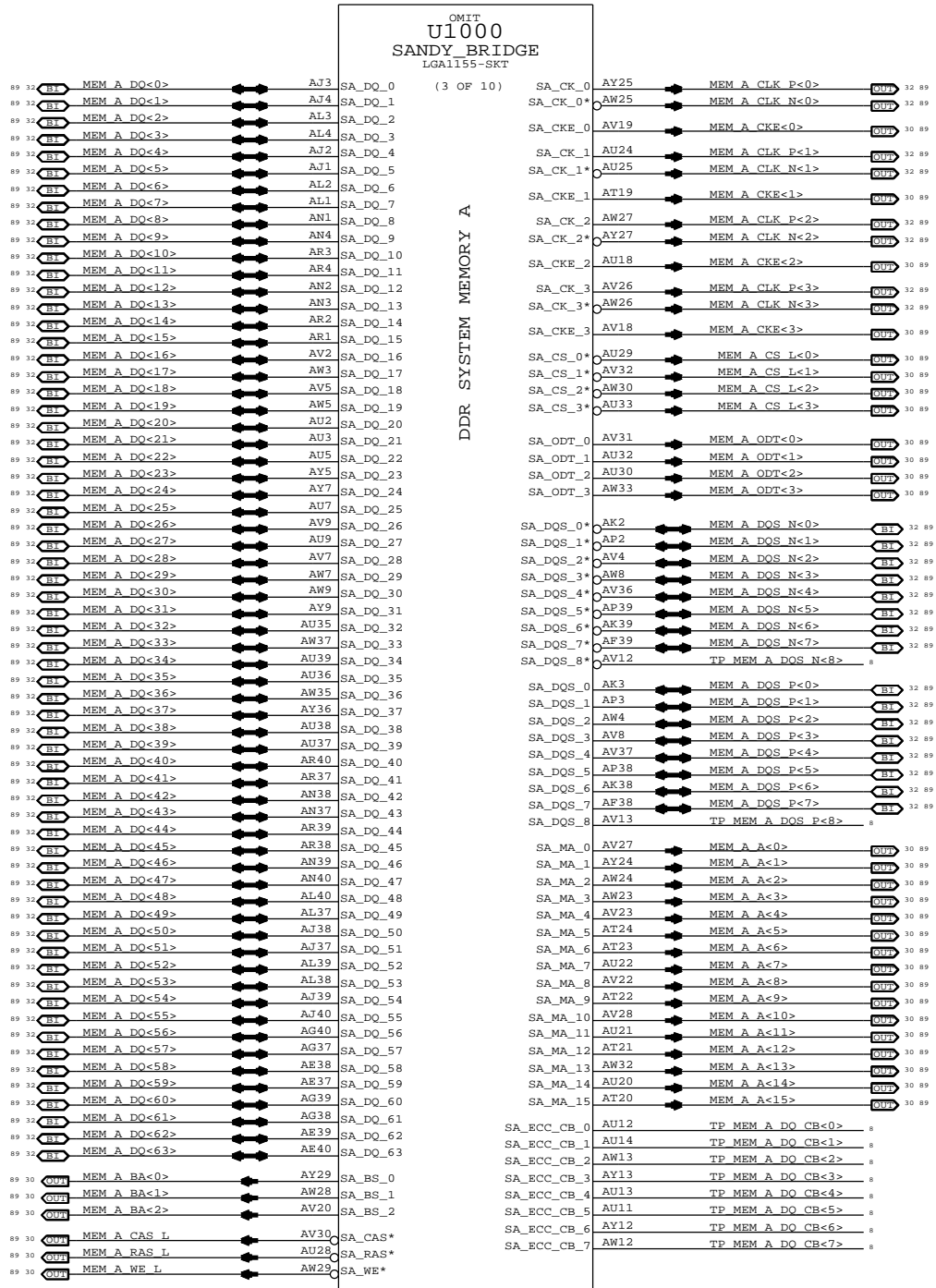
A

D

C

B

A



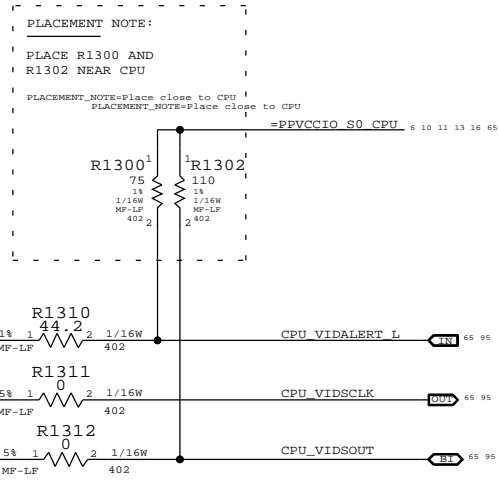
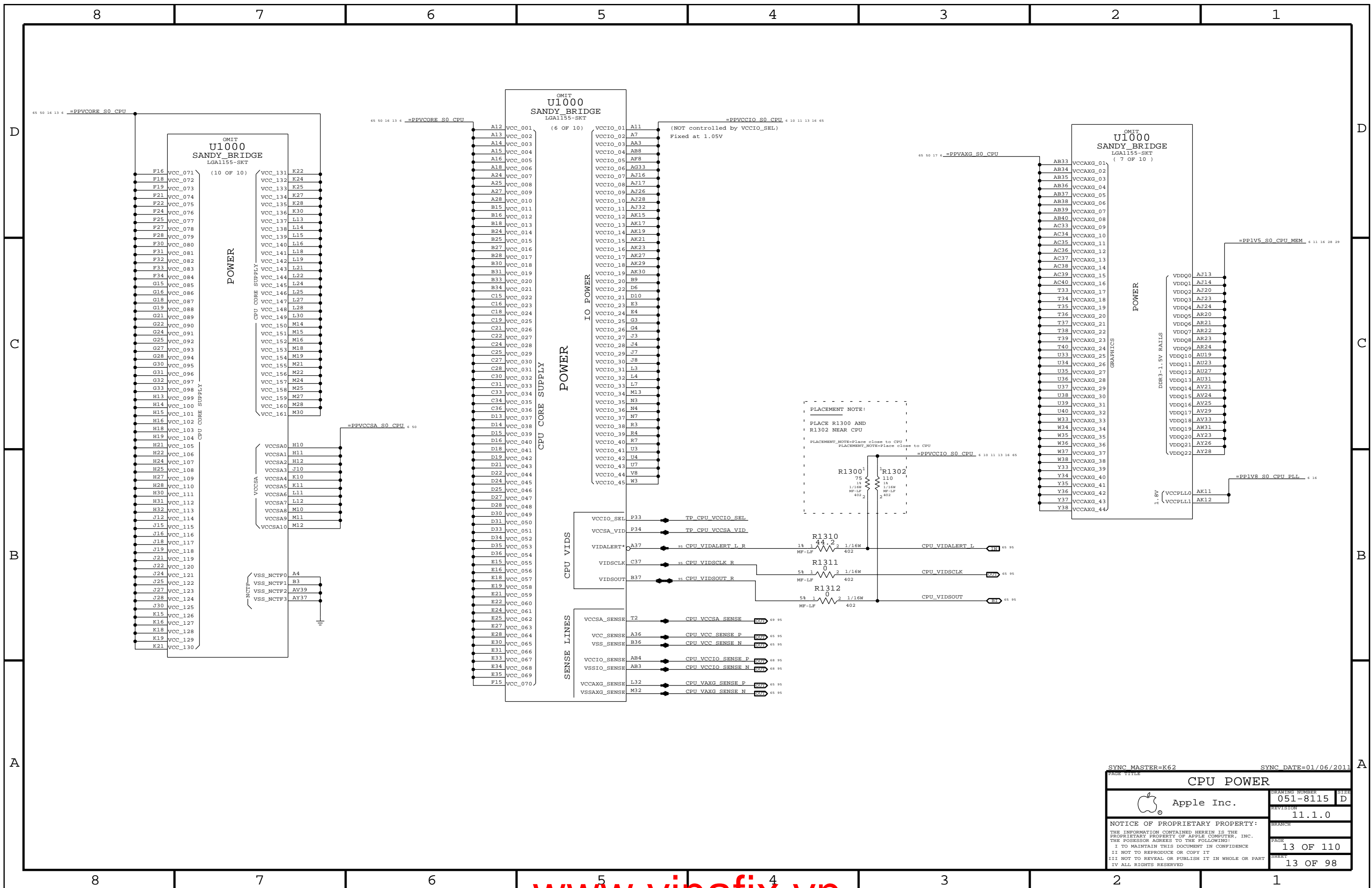
CPU DDR3 INTERFACES

Apple Inc.

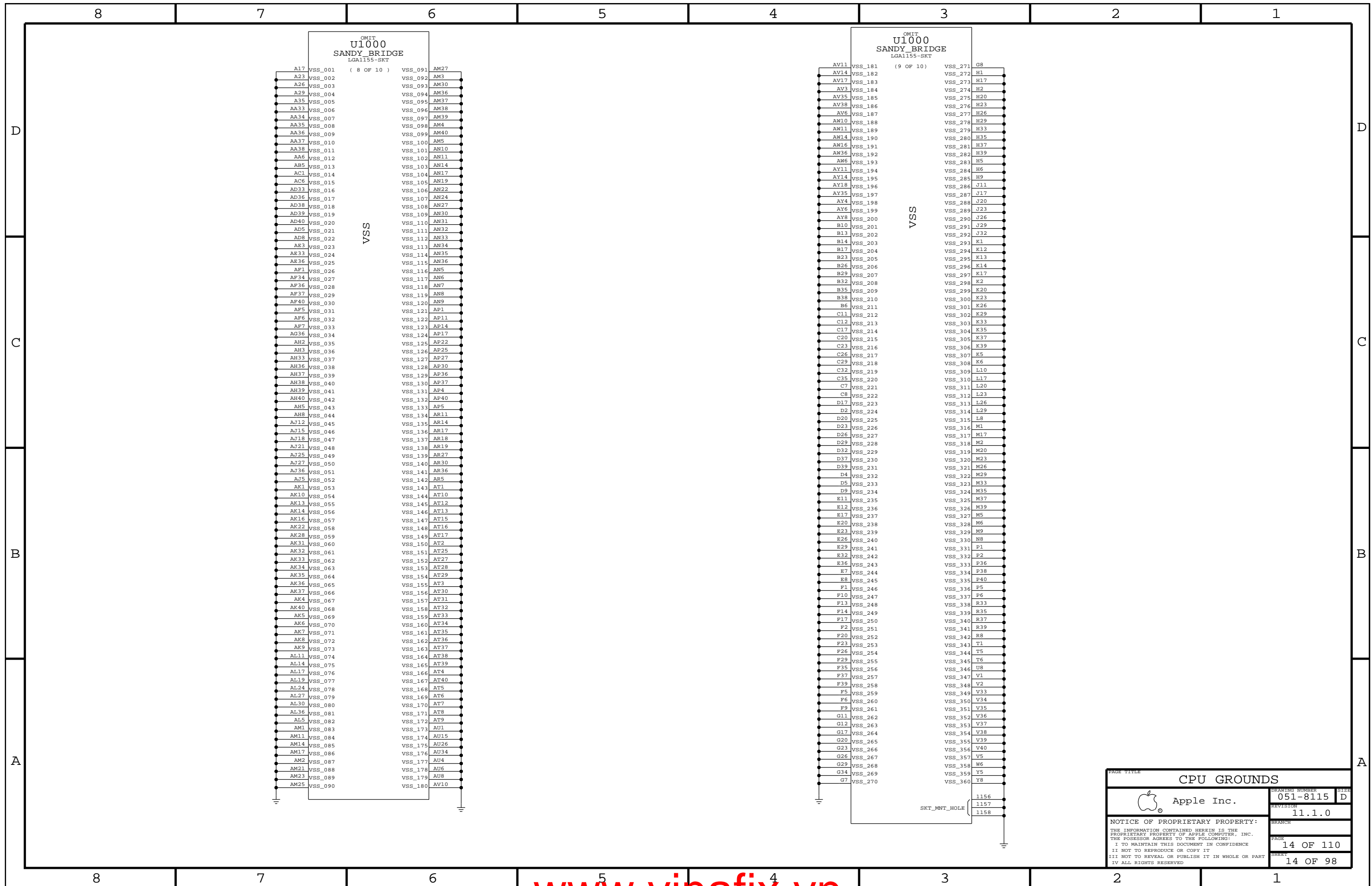
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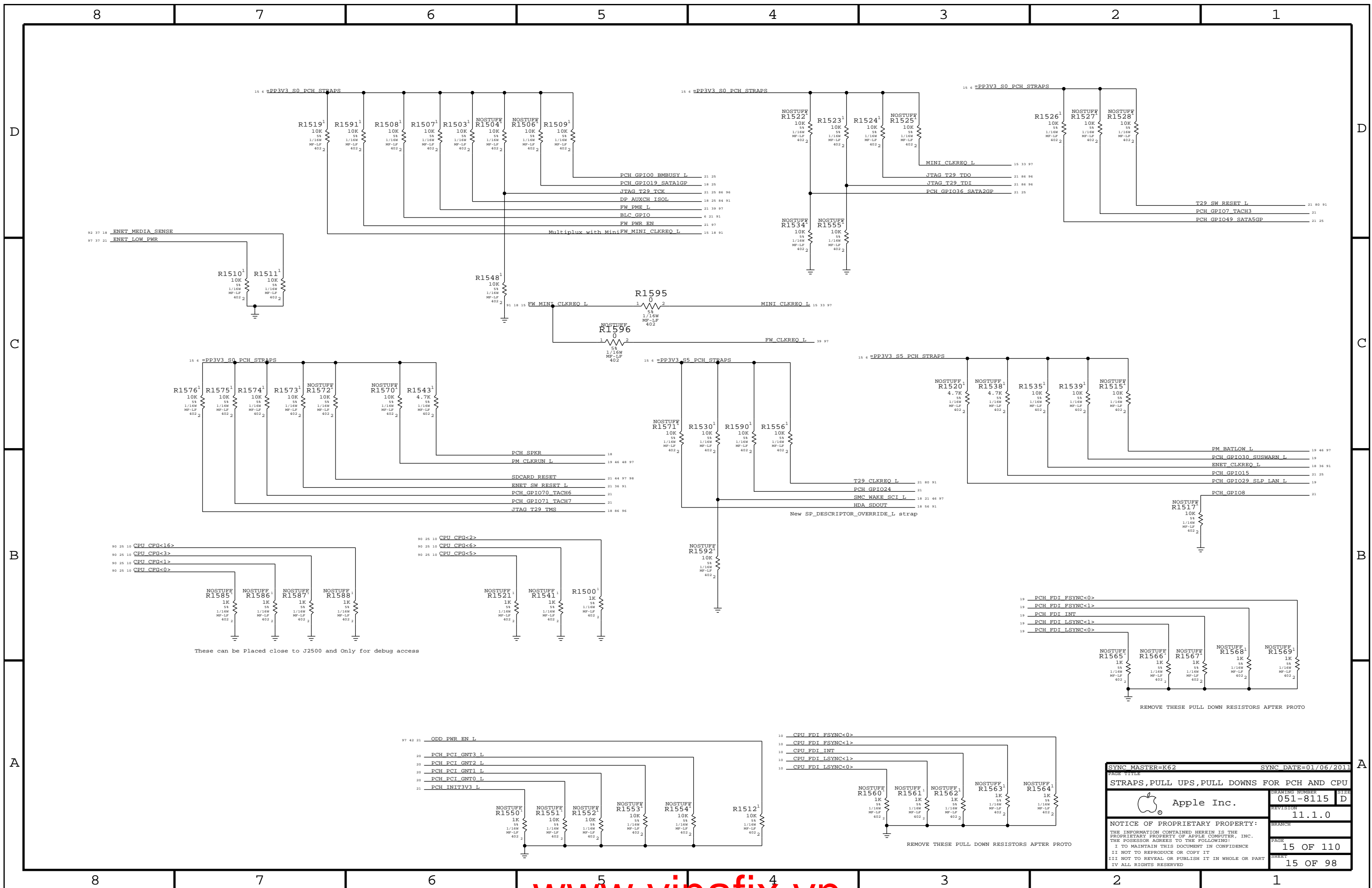
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CPU POWER		051-8115		D
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CPU GROUNDS		
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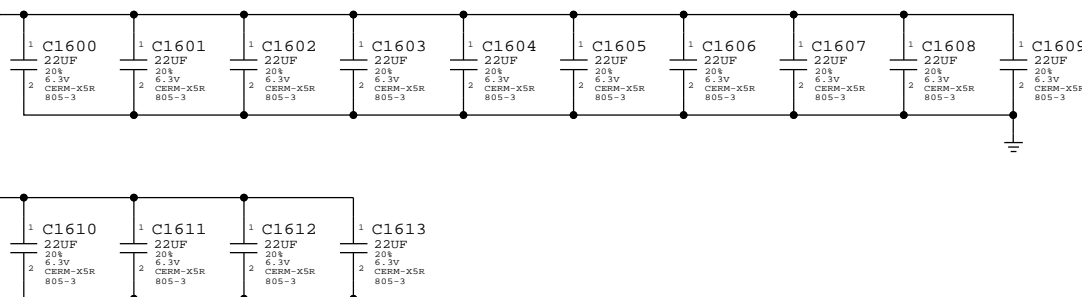
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PAGE TITLE STRAPS, PULL UPS, PULL DOWNS FOR PCH AND CPU			
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CPU VCORE DECOUPLING

14x 22uF,0805 INTEL RECOMMENDATION 18X 22uF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

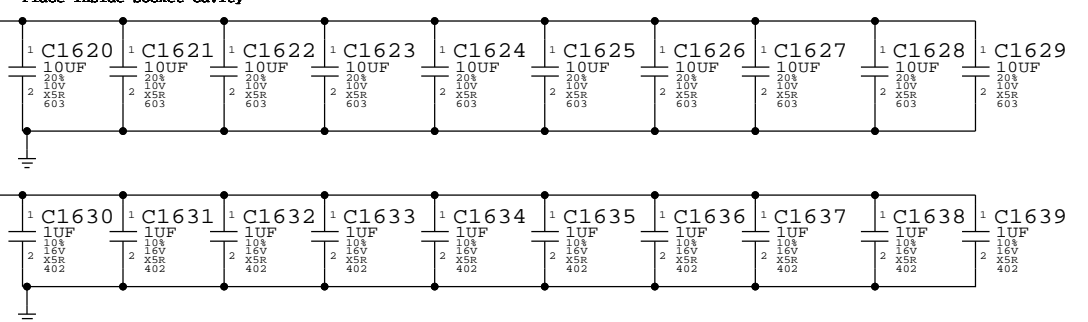
Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 72

10x 10uF and 10x 1uF CAPACITORS

Place inside socket cavity

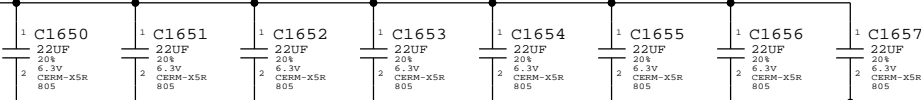


CPU VCCIO DECOUPLING

8X 22uF 0805, 6X 10uF 0805 INTEL RECOMMENDATION 9X22uF 0805,16X 0805 placeholders

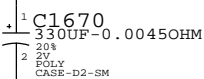
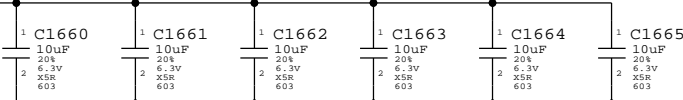
PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.



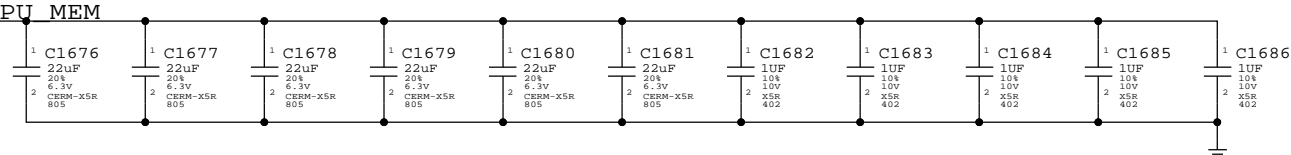
PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.



Memory (CPU VCCDDR) DECOUPLING

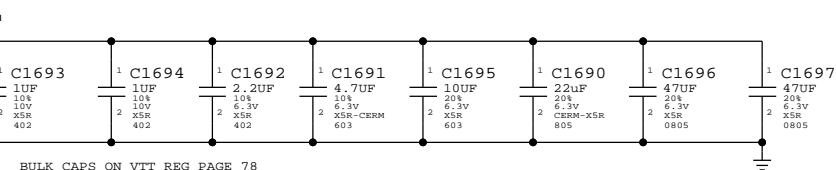
6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805



Note: VCCSA decoupling is on regulator page

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805



BULK CAPS ON VTT REG PAGE 78

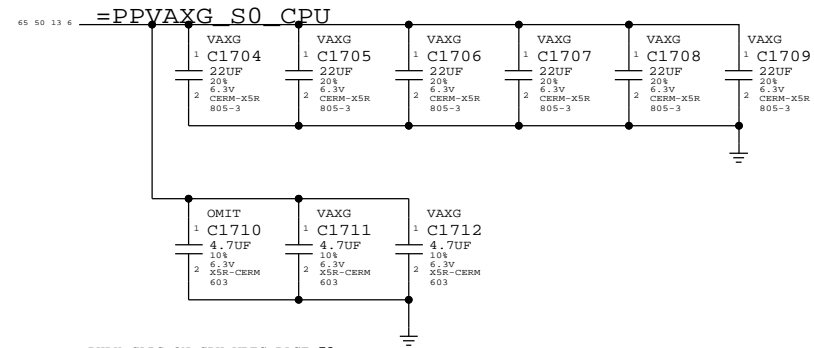
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CPU NON-GFX DECOUPLING		051-8115		D
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VAXG DECOUPLING

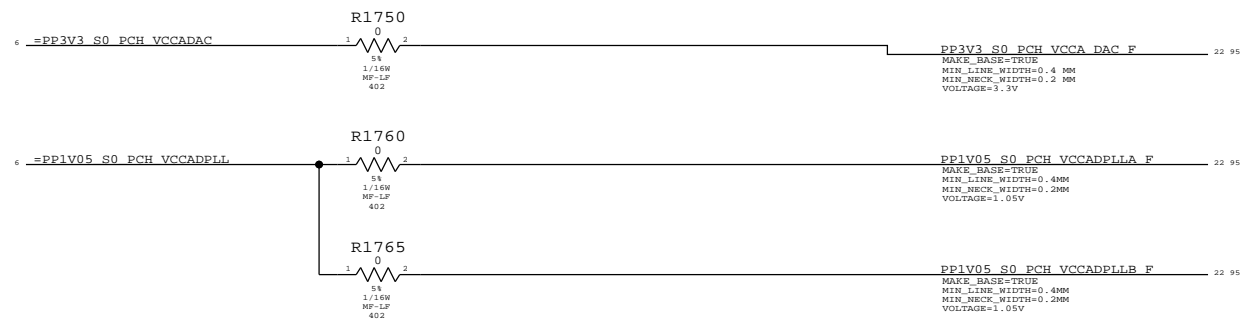
INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity

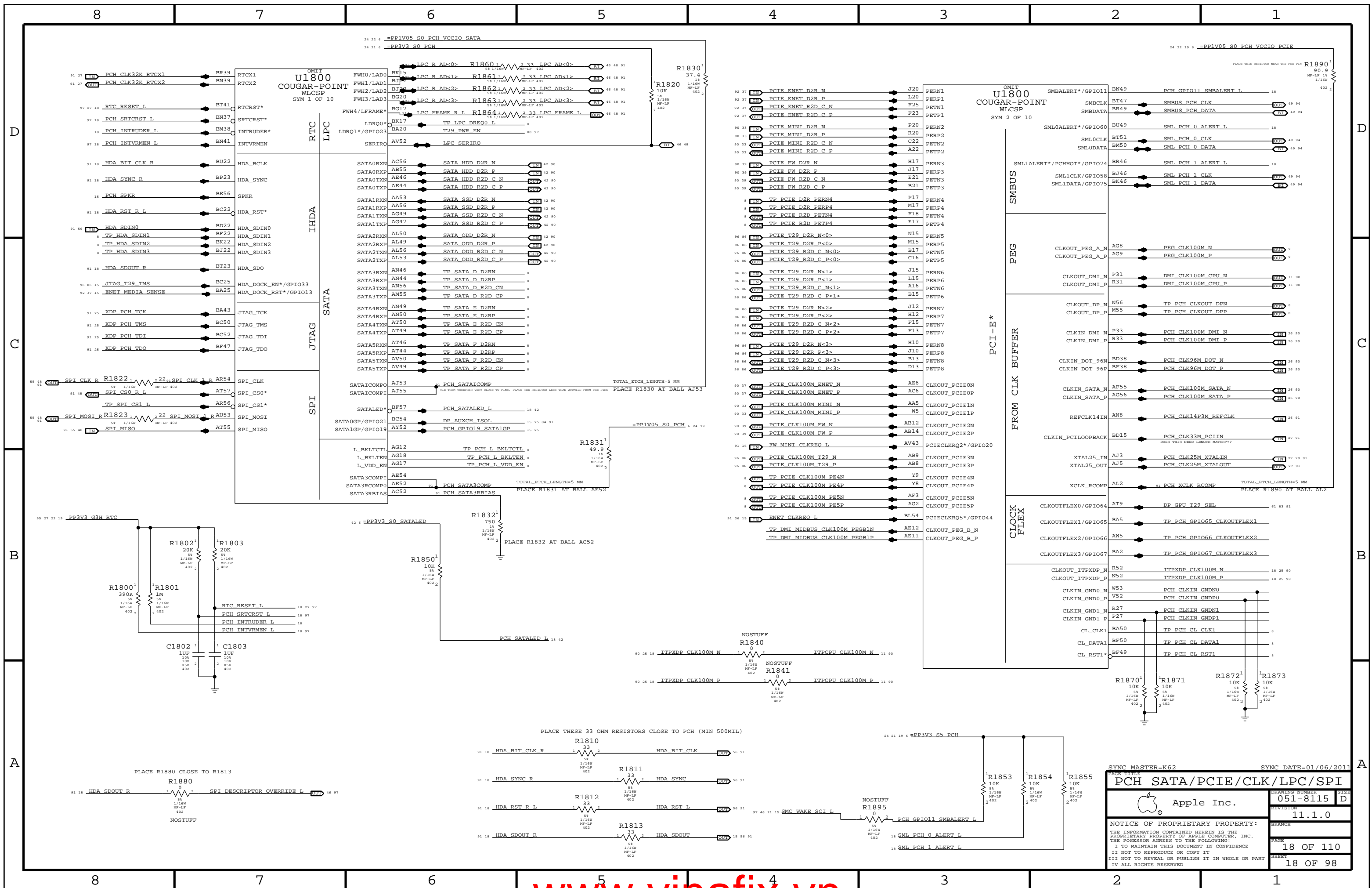


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13880586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
11380022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG



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GFX DECOUPLING & PCH PWR ALIAS		051-8115	D
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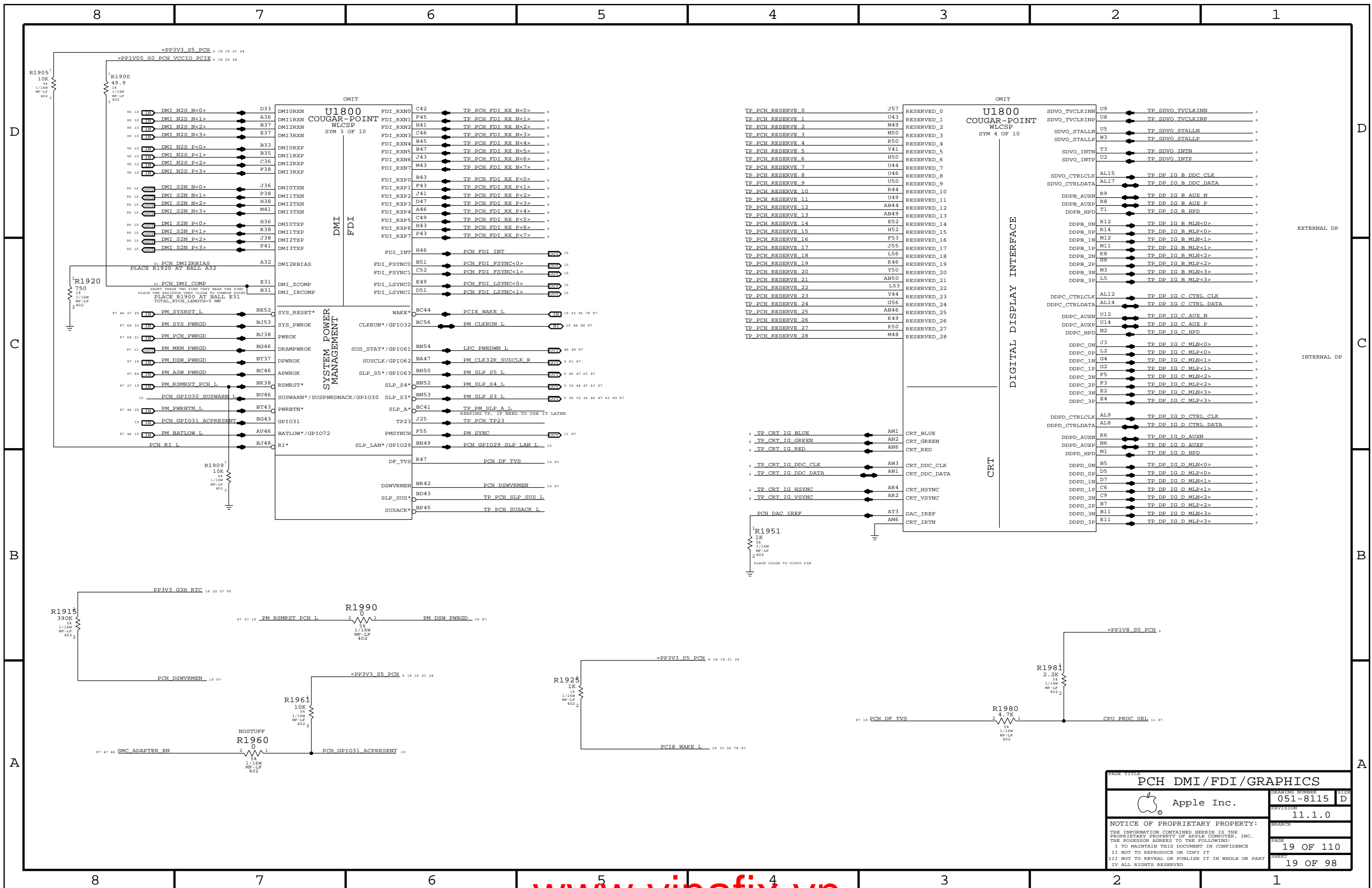
PCH SATA/PCIE/CLK/LPC/SPI

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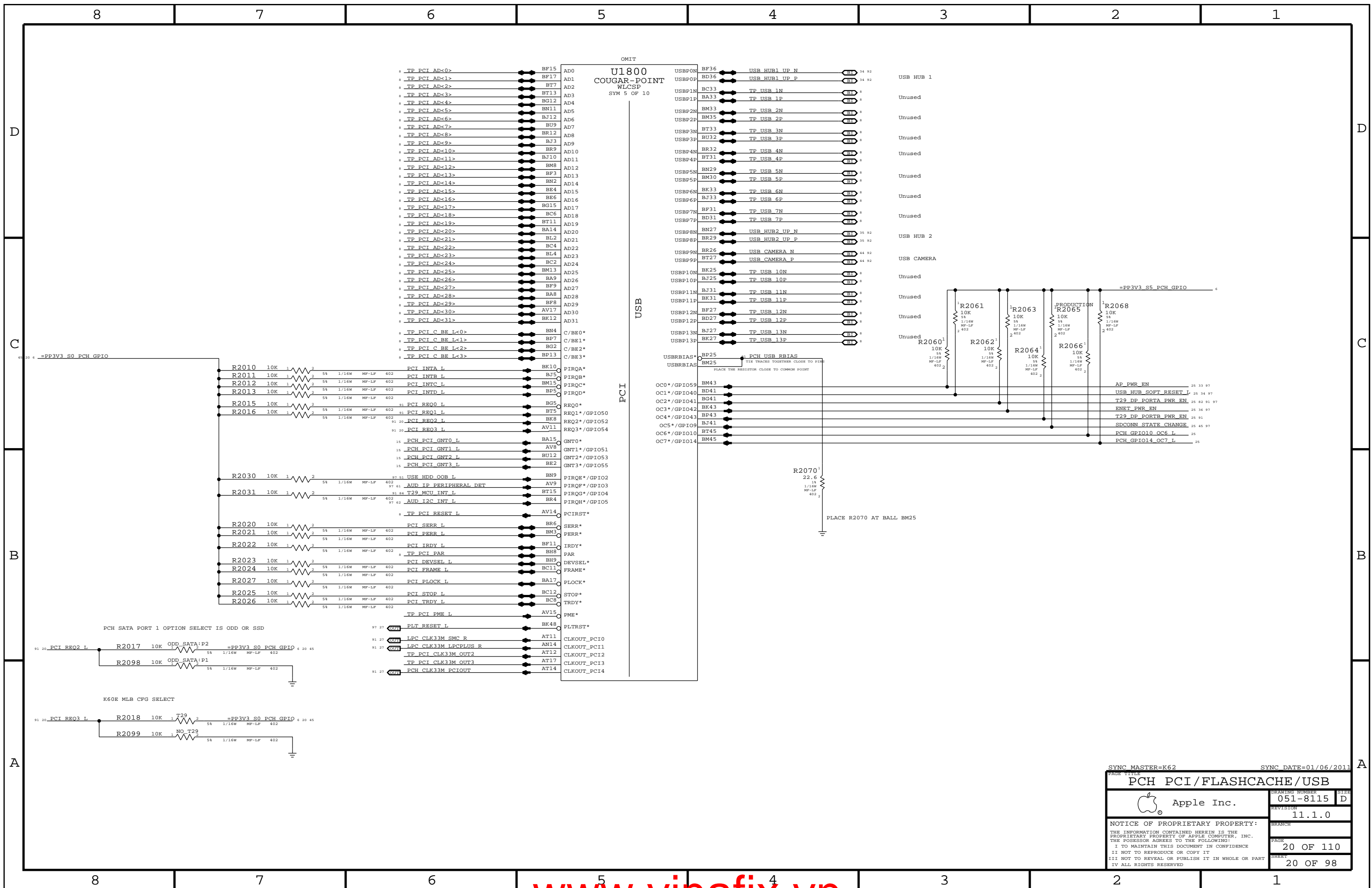
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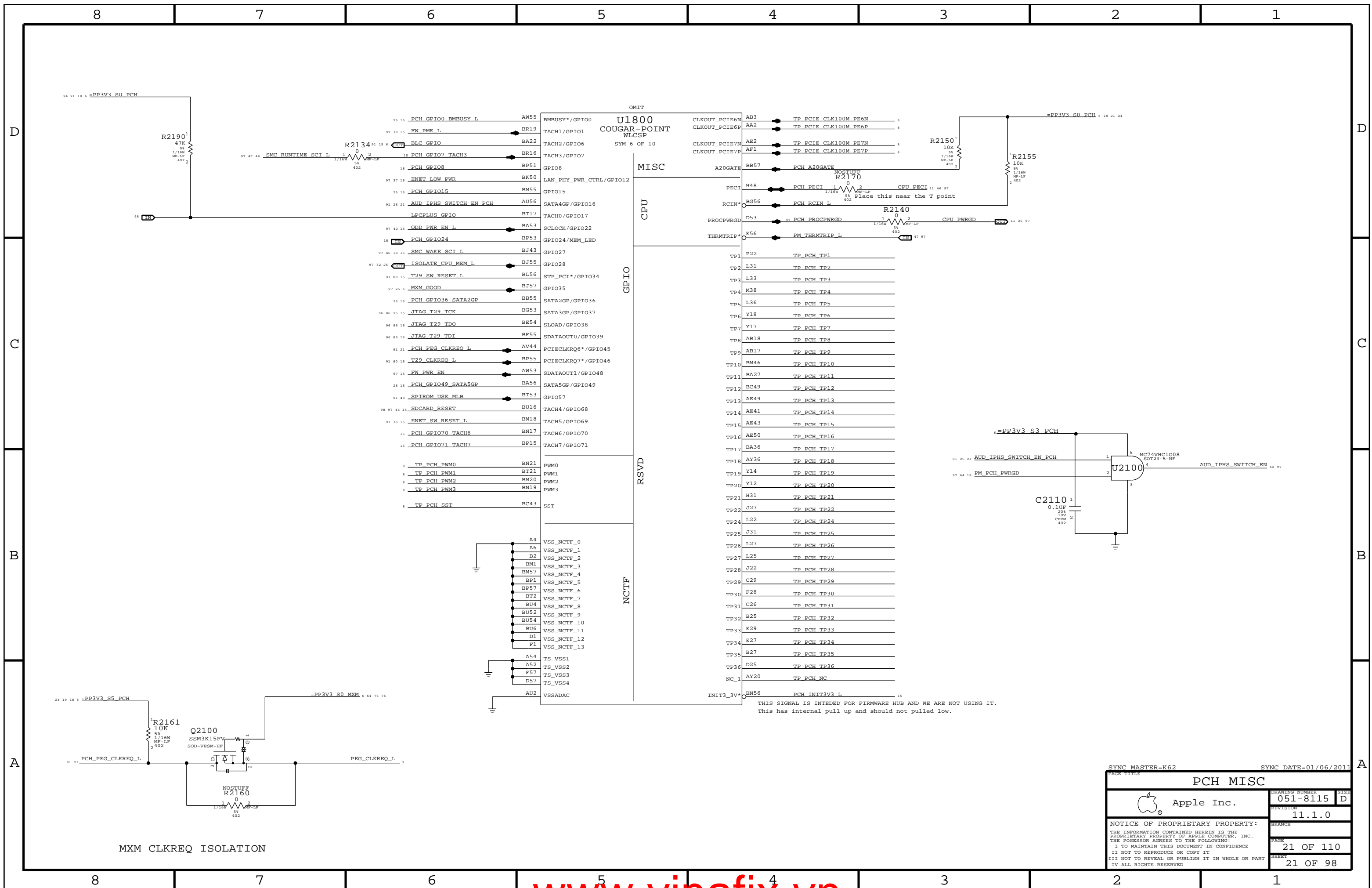


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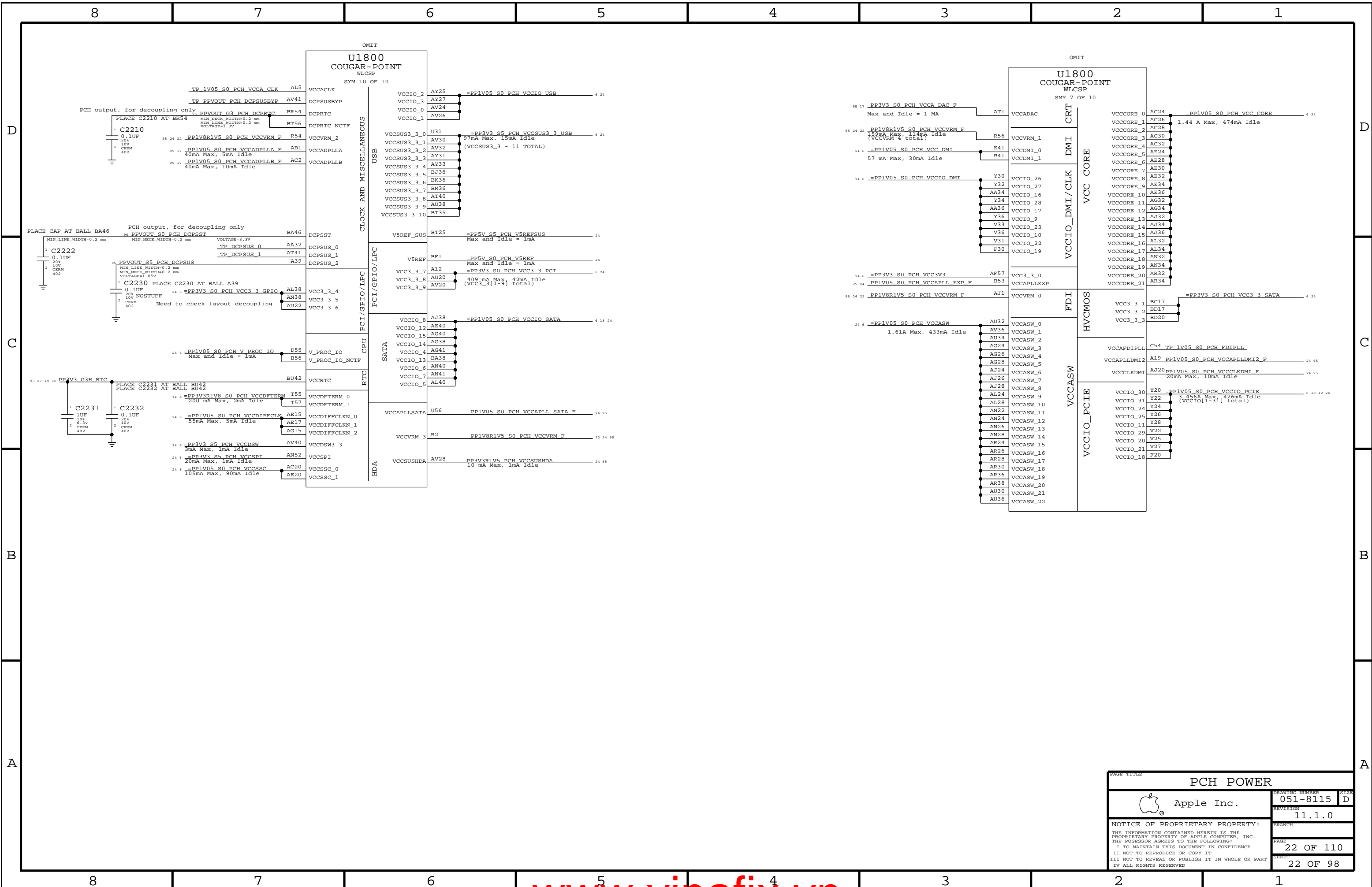
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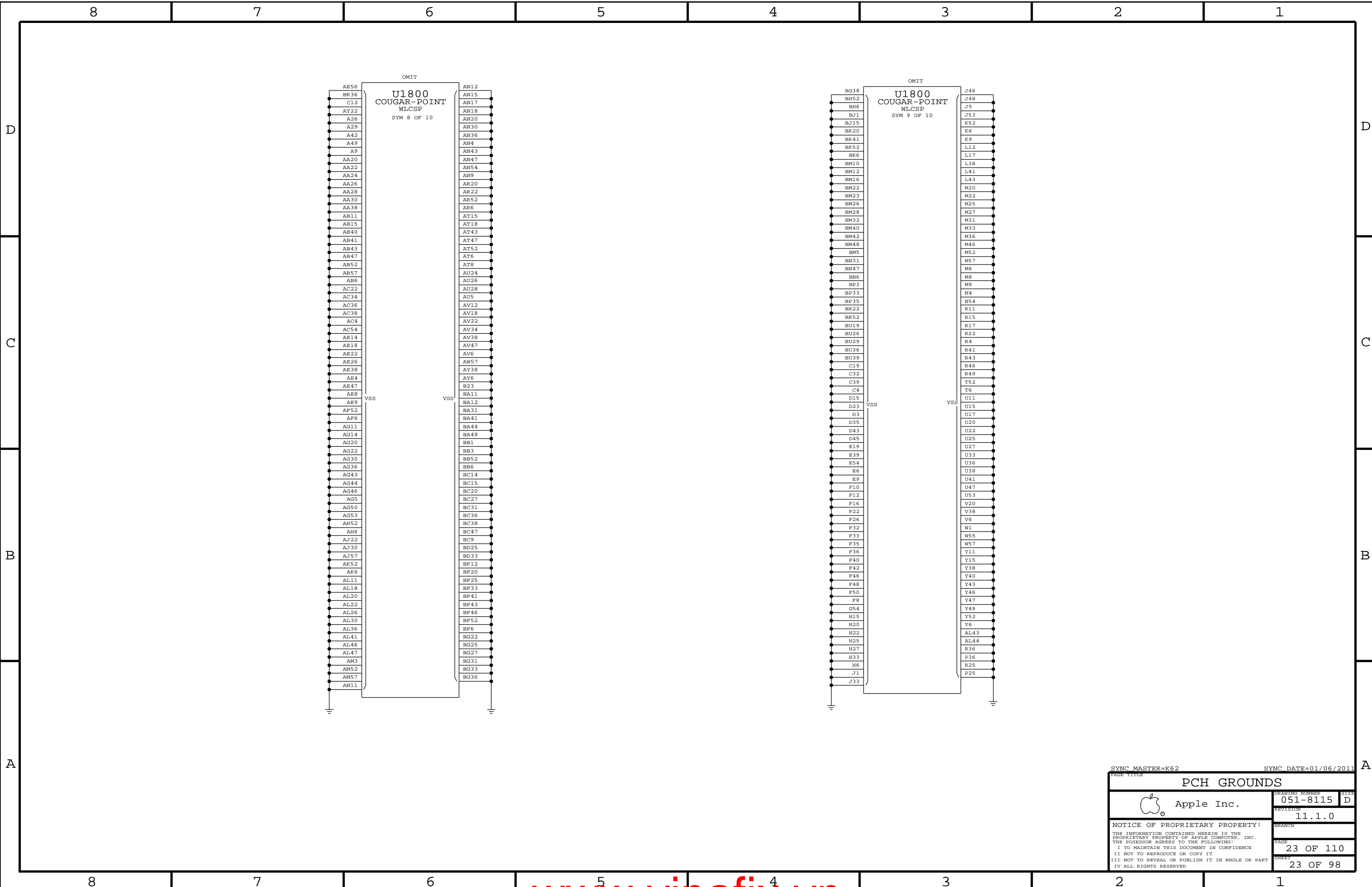


MXM CLKREQ ISOLATION

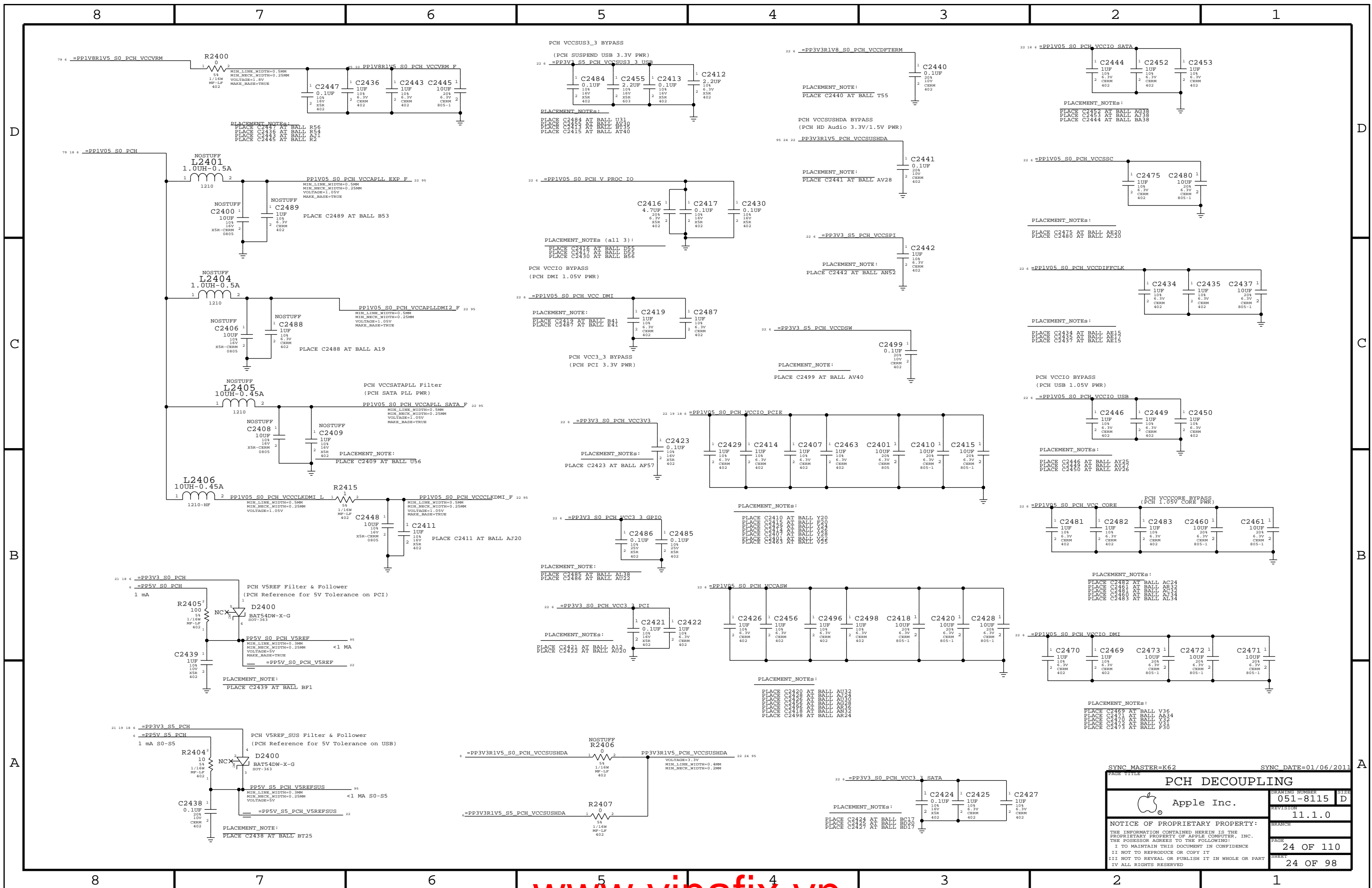
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PCH MISC			
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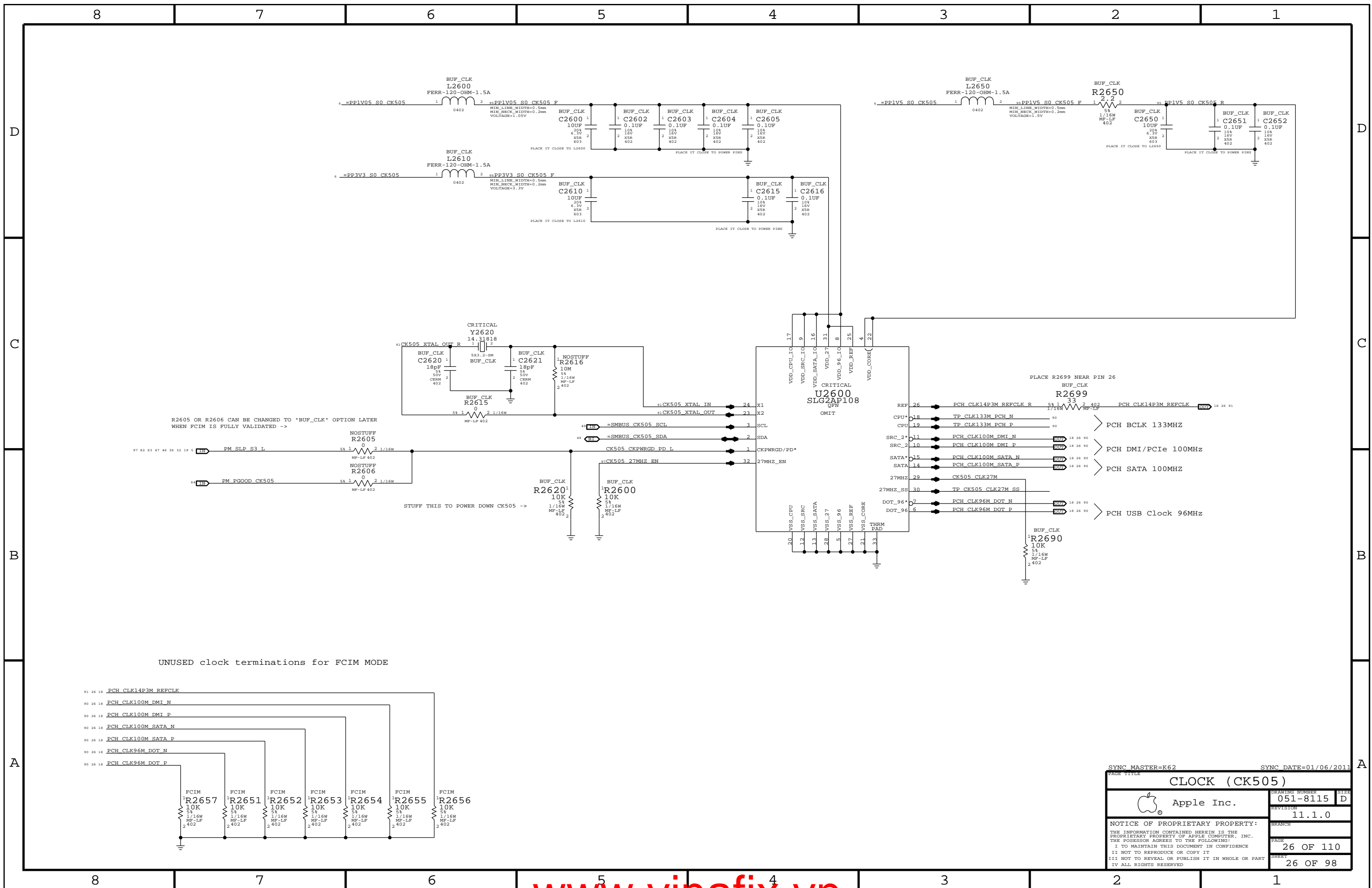


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PCH DECOUPLING

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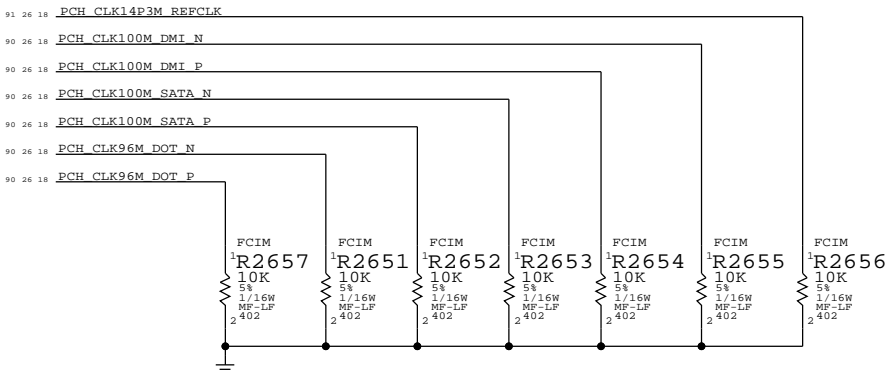
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R2605 OR R2606 CAN BE CHANGED TO "BUF_CLK" OPTION LATER WHEN FCIM IS FULLY VALIDATED ->

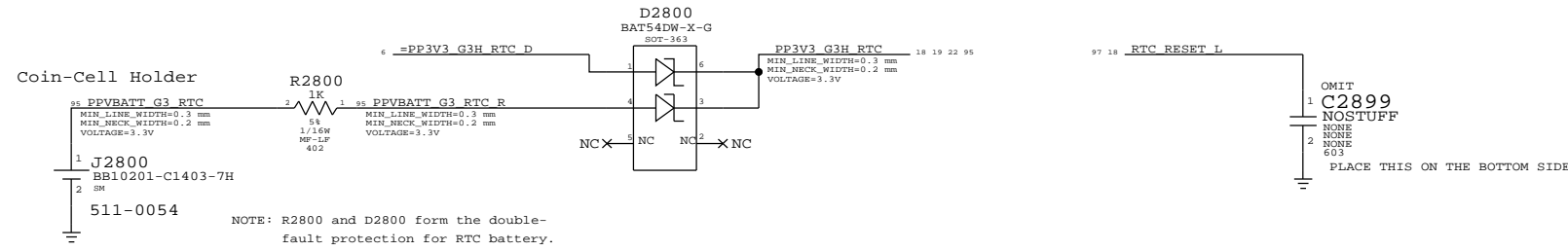
STUFF THIS TO POWER DOWN CK505 ->

UNUSED clock terminations for FCIM MODE

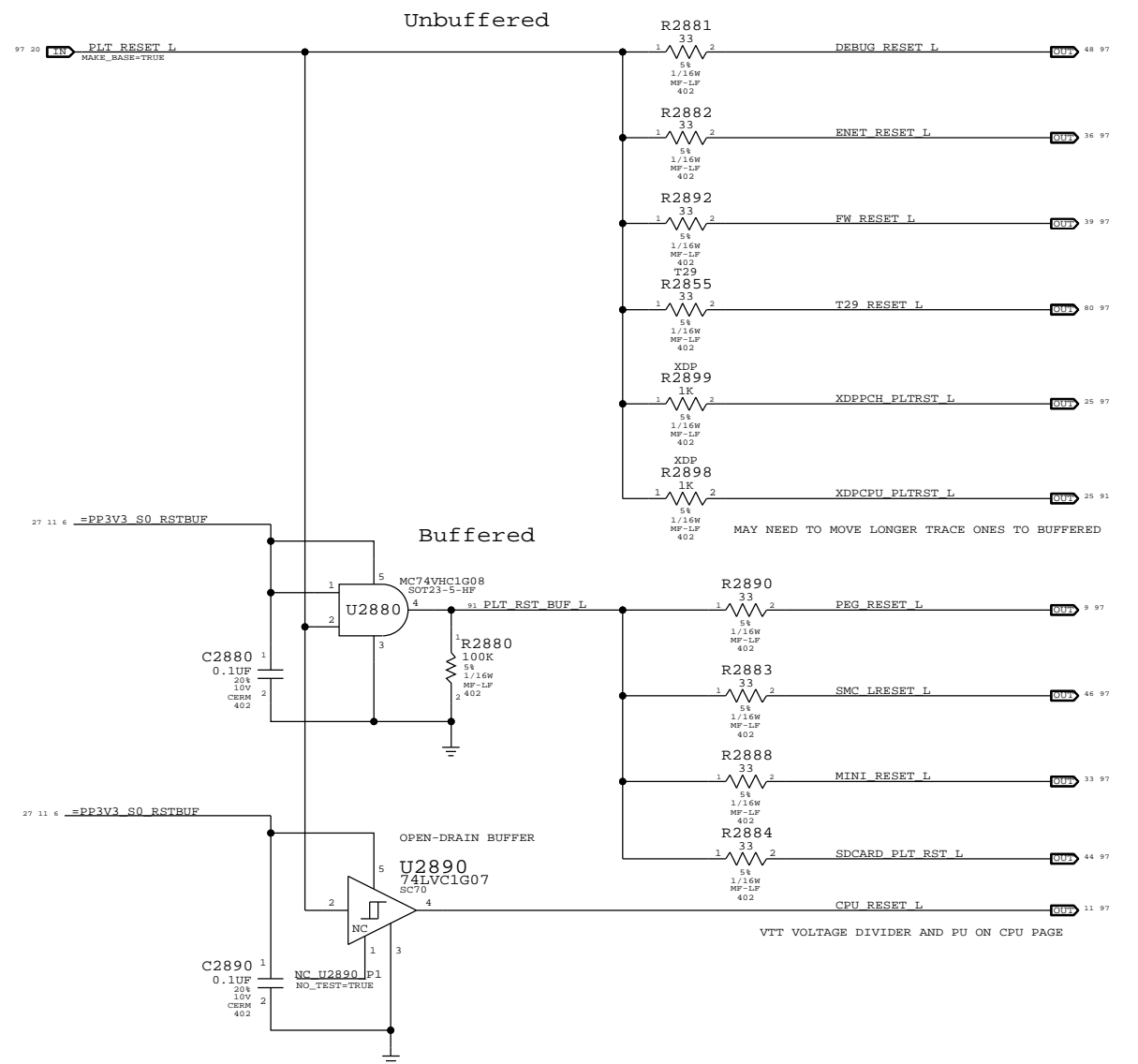


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CLOCK (CK505)			
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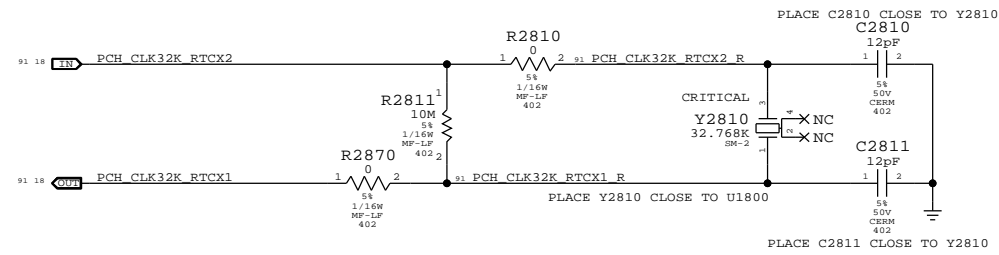
RTC Power Sources



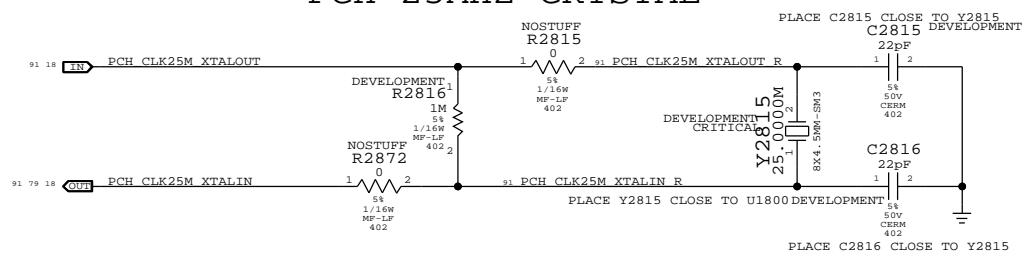
Platform Reset Connections



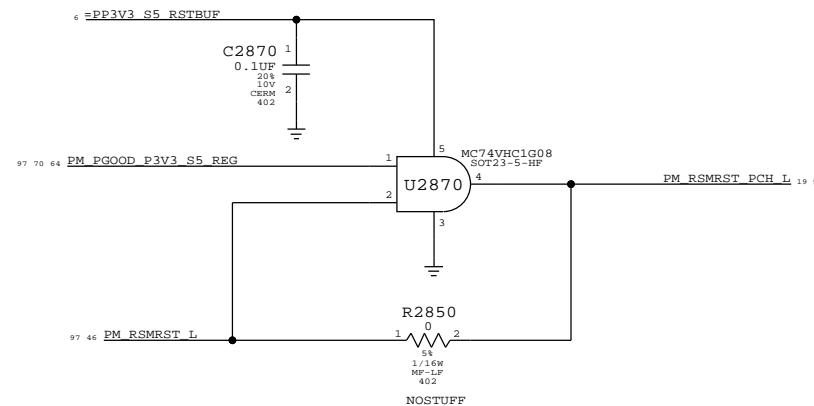
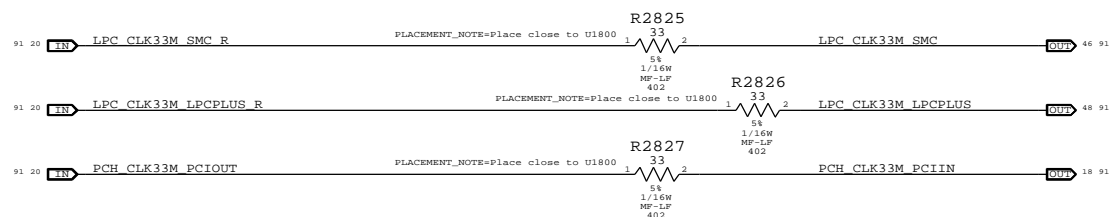
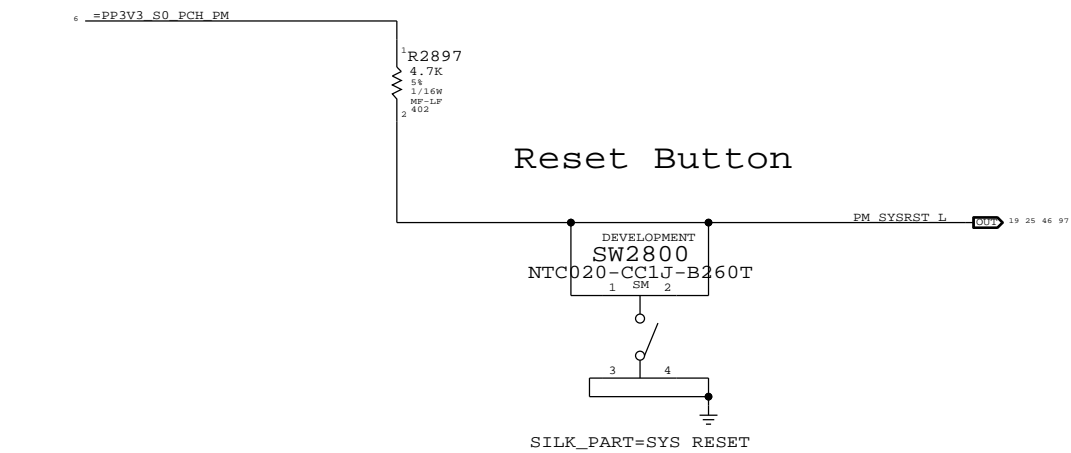
PCH RTC Crystal



PCH 25MHZ CRYSTAL

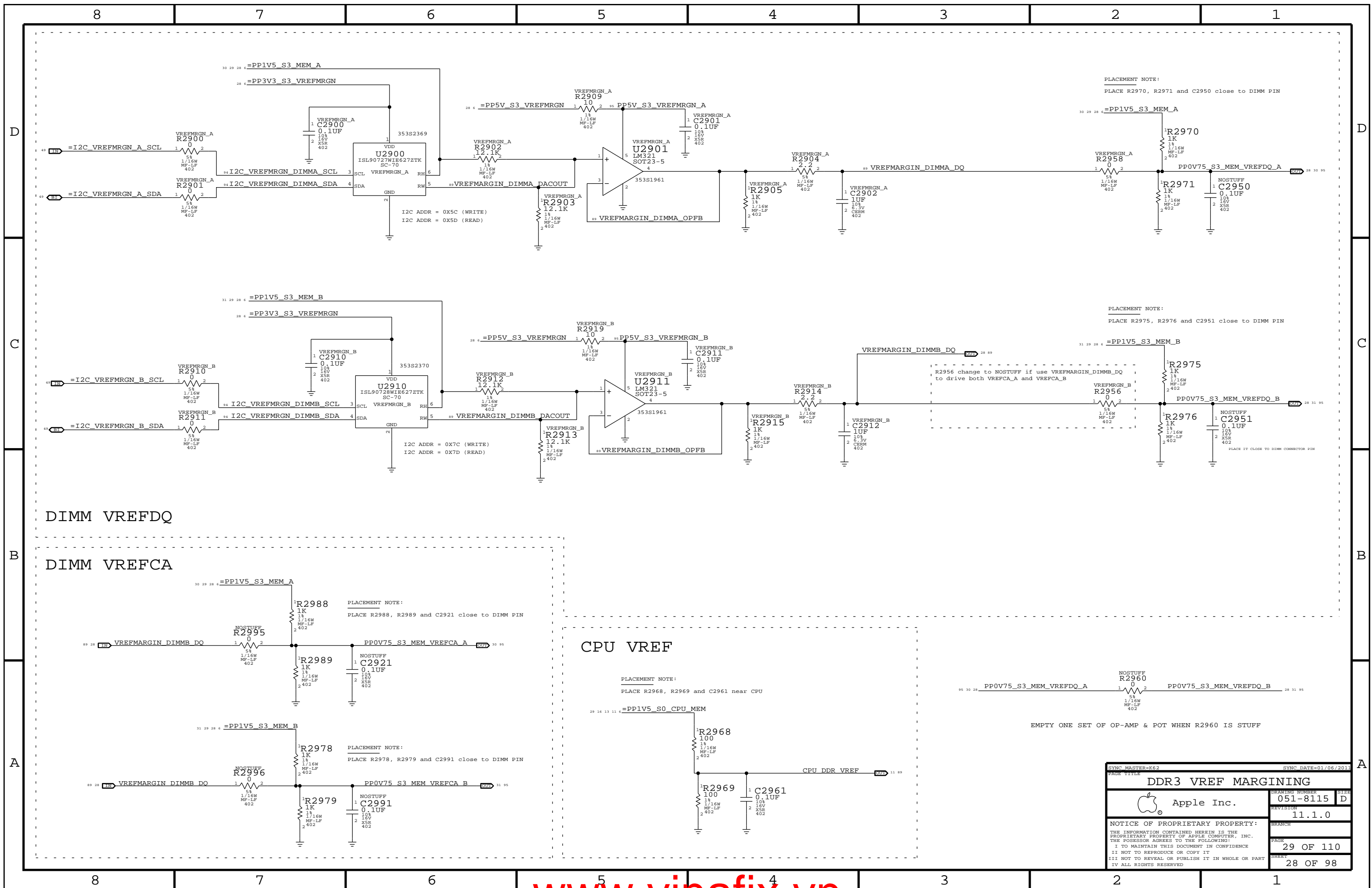


Reset Button



SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
 SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
 SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
 PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

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CHIPSET SUPPORT					
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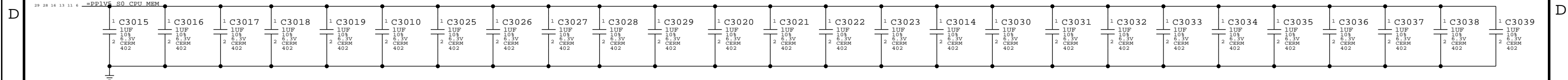
2

1

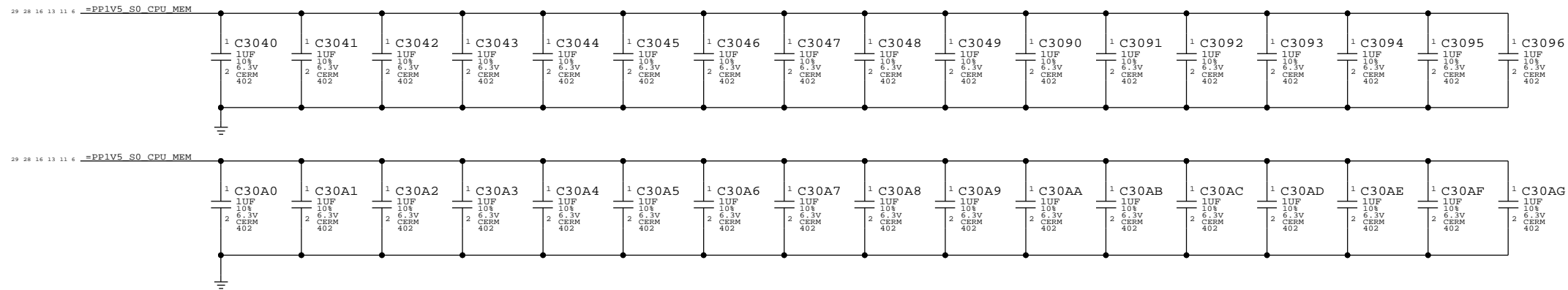
DIMM A (CLOSER TO CPU)

CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM

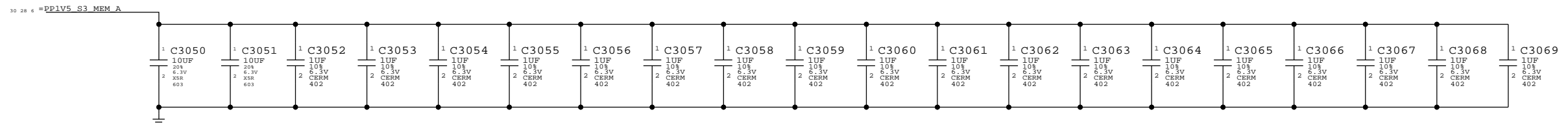
DIMM B (FURTHER FROM CPU)



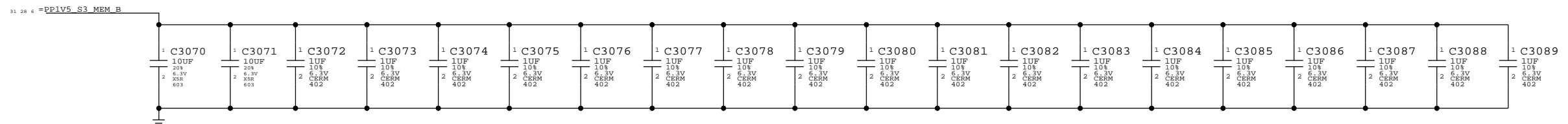
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



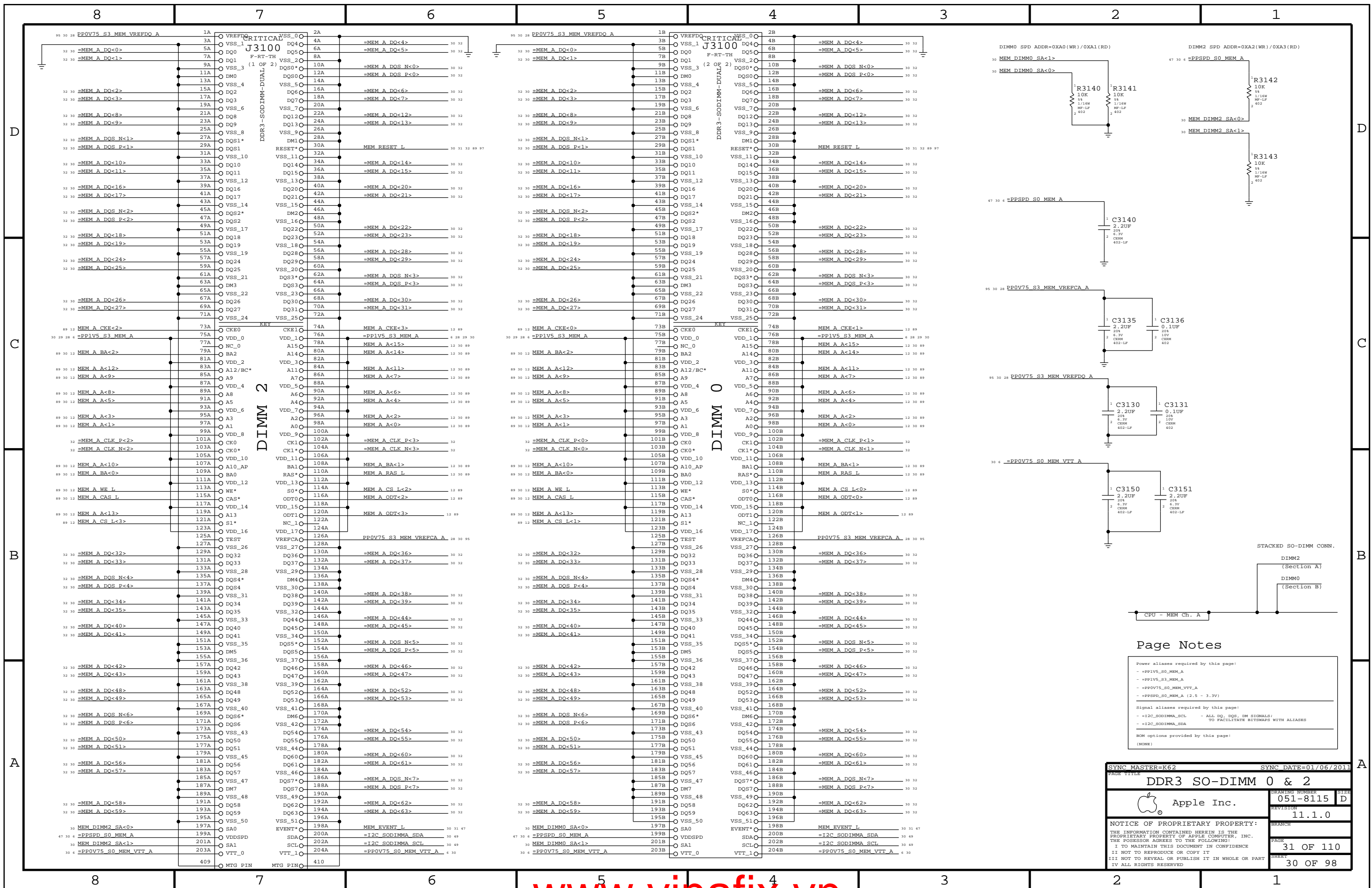
DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



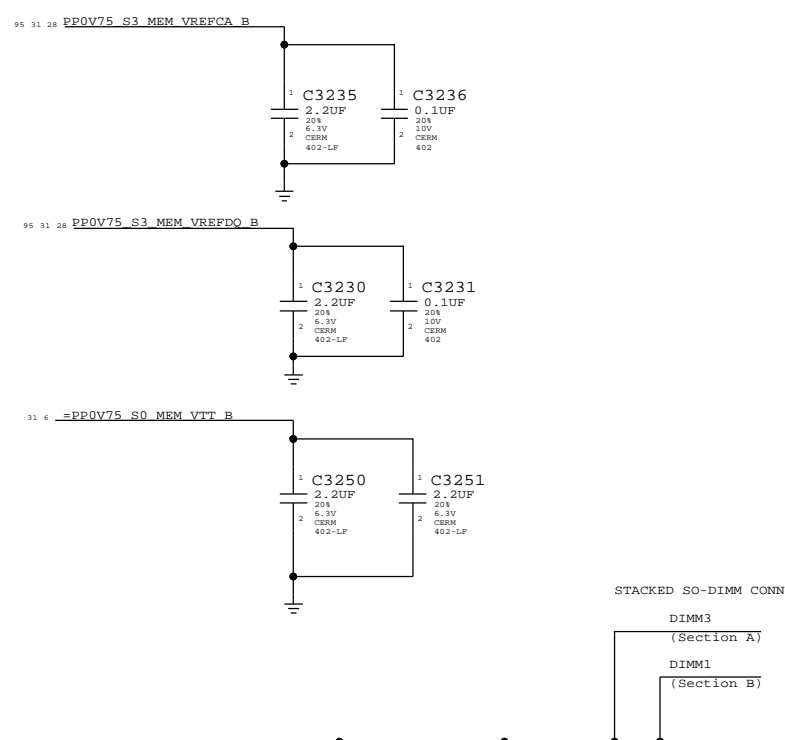
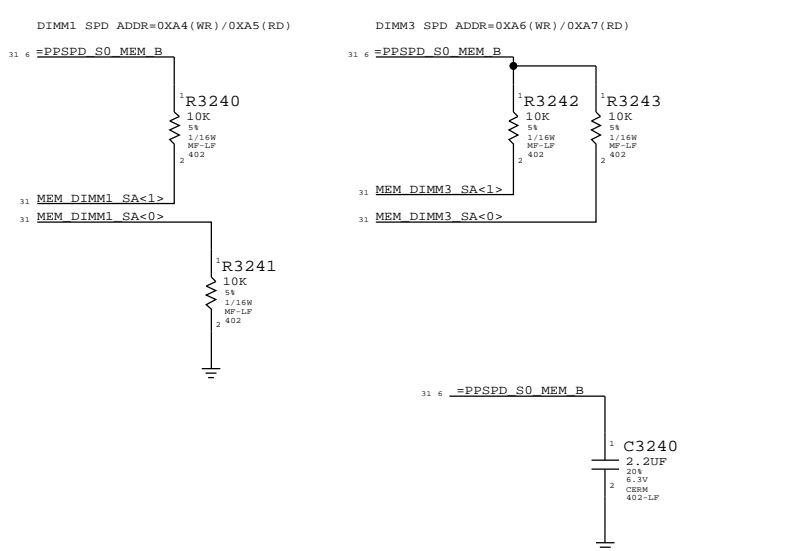
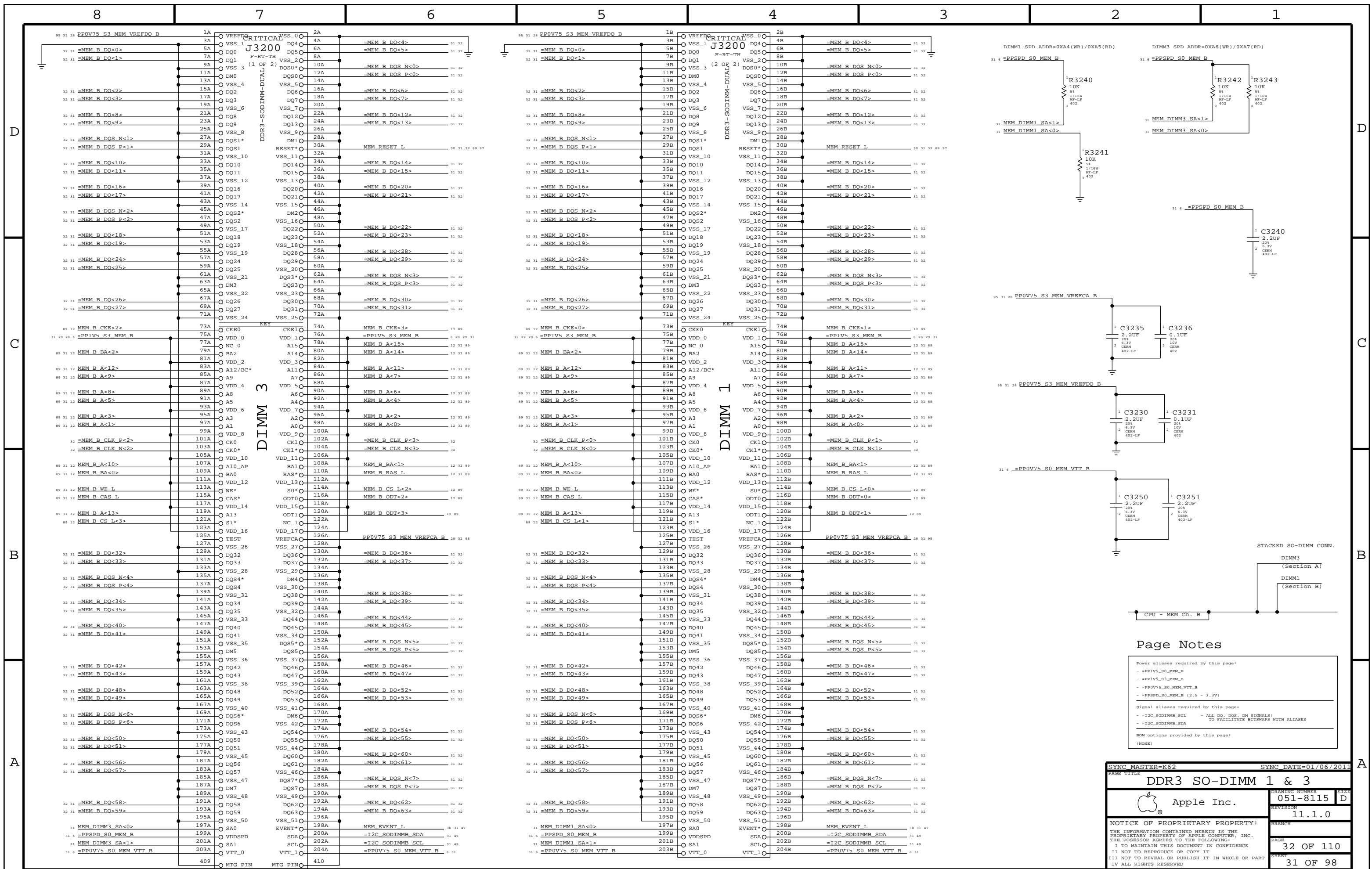
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MEMORY CAPS			
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Page Notes

- Power aliases required by this page:
- =PP1V5_S0_MEM_A
 - =PP1V5_S3_MEM_A
 - =PP0V75_S0_MEM_VTT_A
 - =PPSPD_S0_MEM_A (2.5 - 3.3V)
- Signal aliases required by this page:
- =I2C_SODIMMA_SCL - ALL DQ, DQS, DM SIGNALS TO FACILITATE BITSTREAMS WITH ALIASES
 - =I2C_SODIMMA_SDA
- MEM options provided by this page:
- (NONE)

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Page Notes

Power aliases required by this page:
 - *PP1V5_S0_MEM_B
 - *PP1V5_S3_MEM_B
 - *PP0V75_S0_MEM_VTT_B
 - *PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
 - *I2C_SODIMM_SCL - ALL DQ, DQS, DM SIGNALS;
 - *I2C_SODIMM_SDA TO FACILITATE BITSNAPS WITH ALIASES

MEM options provided by this page:
 (NONE)

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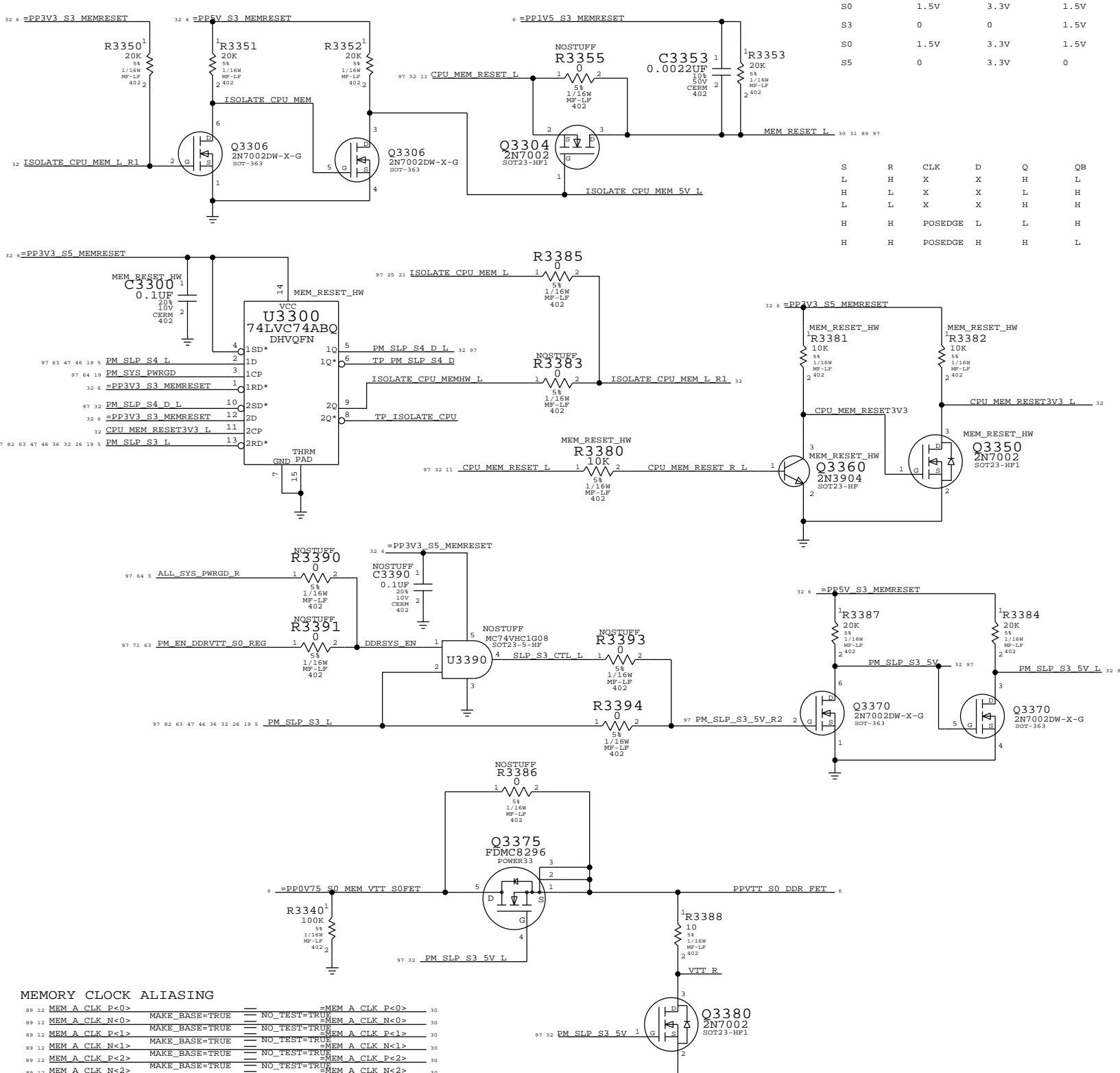
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CPU CHANNEL A DQS 0 -> DIMM A DQS 7		CPU CHANNEL B DQS 0 -> DIMM B DQS 7	
MEM A DQS N<0>	MAKE_BASE=TRUE	MEM B DQS N<0>	MAKE_BASE=TRUE
MEM A DQS P<0>	MAKE_BASE=TRUE	MEM B DQS P<0>	MAKE_BASE=TRUE
MEM A DQ<7>	MAKE_BASE=TRUE	MEM B DQ<7>	MAKE_BASE=TRUE
MEM A DQ<6>	MAKE_BASE=TRUE	MEM B DQ<6>	MAKE_BASE=TRUE
MEM A DQ<5>	MAKE_BASE=TRUE	MEM B DQ<5>	MAKE_BASE=TRUE
MEM A DQ<4>	MAKE_BASE=TRUE	MEM B DQ<4>	MAKE_BASE=TRUE
MEM A DQ<3>	MAKE_BASE=TRUE	MEM B DQ<3>	MAKE_BASE=TRUE
MEM A DQ<2>	MAKE_BASE=TRUE	MEM B DQ<2>	MAKE_BASE=TRUE
MEM A DQ<1>	MAKE_BASE=TRUE	MEM B DQ<1>	MAKE_BASE=TRUE
MEM A DQ<0>	MAKE_BASE=TRUE	MEM B DQ<0>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 1 -> DIMM A DQS 6		CPU CHANNEL B DQS 1 -> DIMM B DQS 6	
MEM A DQS N<1>	MAKE_BASE=TRUE	MEM B DQS N<1>	MAKE_BASE=TRUE
MEM A DQS P<1>	MAKE_BASE=TRUE	MEM B DQS P<1>	MAKE_BASE=TRUE
MEM A DQ<15>	MAKE_BASE=TRUE	MEM B DQ<15>	MAKE_BASE=TRUE
MEM A DQ<14>	MAKE_BASE=TRUE	MEM B DQ<14>	MAKE_BASE=TRUE
MEM A DQ<13>	MAKE_BASE=TRUE	MEM B DQ<13>	MAKE_BASE=TRUE
MEM A DQ<12>	MAKE_BASE=TRUE	MEM B DQ<12>	MAKE_BASE=TRUE
MEM A DQ<11>	MAKE_BASE=TRUE	MEM B DQ<11>	MAKE_BASE=TRUE
MEM A DQ<10>	MAKE_BASE=TRUE	MEM B DQ<10>	MAKE_BASE=TRUE
MEM A DQ<9>	MAKE_BASE=TRUE	MEM B DQ<9>	MAKE_BASE=TRUE
MEM A DQ<8>	MAKE_BASE=TRUE	MEM B DQ<8>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 2 -> DIMM A DQS 5		CPU CHANNEL B DQS 2 -> DIMM B DQS 5	
MEM A DQS N<2>	MAKE_BASE=TRUE	MEM B DQS N<2>	MAKE_BASE=TRUE
MEM A DQS P<2>	MAKE_BASE=TRUE	MEM B DQS P<2>	MAKE_BASE=TRUE
MEM A DQ<23>	MAKE_BASE=TRUE	MEM B DQ<23>	MAKE_BASE=TRUE
MEM A DQ<22>	MAKE_BASE=TRUE	MEM B DQ<22>	MAKE_BASE=TRUE
MEM A DQ<21>	MAKE_BASE=TRUE	MEM B DQ<21>	MAKE_BASE=TRUE
MEM A DQ<20>	MAKE_BASE=TRUE	MEM B DQ<20>	MAKE_BASE=TRUE
MEM A DQ<19>	MAKE_BASE=TRUE	MEM B DQ<19>	MAKE_BASE=TRUE
MEM A DQ<18>	MAKE_BASE=TRUE	MEM B DQ<18>	MAKE_BASE=TRUE
MEM A DQ<17>	MAKE_BASE=TRUE	MEM B DQ<17>	MAKE_BASE=TRUE
MEM A DQ<16>	MAKE_BASE=TRUE	MEM B DQ<16>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 3 -> DIMM A DQS 4		CPU CHANNEL B DQS 3 -> DIMM B DQS 4	
MEM A DQS N<3>	MAKE_BASE=TRUE	MEM B DQS N<3>	MAKE_BASE=TRUE
MEM A DQS P<3>	MAKE_BASE=TRUE	MEM B DQS P<3>	MAKE_BASE=TRUE
MEM A DQ<31>	MAKE_BASE=TRUE	MEM B DQ<31>	MAKE_BASE=TRUE
MEM A DQ<30>	MAKE_BASE=TRUE	MEM B DQ<30>	MAKE_BASE=TRUE
MEM A DQ<29>	MAKE_BASE=TRUE	MEM B DQ<29>	MAKE_BASE=TRUE
MEM A DQ<28>	MAKE_BASE=TRUE	MEM B DQ<28>	MAKE_BASE=TRUE
MEM A DQ<27>	MAKE_BASE=TRUE	MEM B DQ<27>	MAKE_BASE=TRUE
MEM A DQ<26>	MAKE_BASE=TRUE	MEM B DQ<26>	MAKE_BASE=TRUE
MEM A DQ<25>	MAKE_BASE=TRUE	MEM B DQ<25>	MAKE_BASE=TRUE
MEM A DQ<24>	MAKE_BASE=TRUE	MEM B DQ<24>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 4 -> DIMM A DQS 3		CPU CHANNEL B DQS 4 -> DIMM B DQS 3	
MEM A DQS N<4>	MAKE_BASE=TRUE	MEM B DQS N<4>	MAKE_BASE=TRUE
MEM A DQS P<4>	MAKE_BASE=TRUE	MEM B DQS P<4>	MAKE_BASE=TRUE
MEM A DQ<39>	MAKE_BASE=TRUE	MEM B DQ<39>	MAKE_BASE=TRUE
MEM A DQ<38>	MAKE_BASE=TRUE	MEM B DQ<38>	MAKE_BASE=TRUE
MEM A DQ<37>	MAKE_BASE=TRUE	MEM B DQ<37>	MAKE_BASE=TRUE
MEM A DQ<36>	MAKE_BASE=TRUE	MEM B DQ<36>	MAKE_BASE=TRUE
MEM A DQ<35>	MAKE_BASE=TRUE	MEM B DQ<35>	MAKE_BASE=TRUE
MEM A DQ<34>	MAKE_BASE=TRUE	MEM B DQ<34>	MAKE_BASE=TRUE
MEM A DQ<33>	MAKE_BASE=TRUE	MEM B DQ<33>	MAKE_BASE=TRUE
MEM A DQ<32>	MAKE_BASE=TRUE	MEM B DQ<32>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 5 -> DIMM A DQS 2		CPU CHANNEL B DQS 5 -> DIMM B DQS 2	
MEM A DQS N<5>	MAKE_BASE=TRUE	MEM B DQS N<5>	MAKE_BASE=TRUE
MEM A DQS P<5>	MAKE_BASE=TRUE	MEM B DQS P<5>	MAKE_BASE=TRUE
MEM A DQ<47>	MAKE_BASE=TRUE	MEM B DQ<47>	MAKE_BASE=TRUE
MEM A DQ<46>	MAKE_BASE=TRUE	MEM B DQ<46>	MAKE_BASE=TRUE
MEM A DQ<45>	MAKE_BASE=TRUE	MEM B DQ<45>	MAKE_BASE=TRUE
MEM A DQ<44>	MAKE_BASE=TRUE	MEM B DQ<44>	MAKE_BASE=TRUE
MEM A DQ<43>	MAKE_BASE=TRUE	MEM B DQ<43>	MAKE_BASE=TRUE
MEM A DQ<42>	MAKE_BASE=TRUE	MEM B DQ<42>	MAKE_BASE=TRUE
MEM A DQ<41>	MAKE_BASE=TRUE	MEM B DQ<41>	MAKE_BASE=TRUE
MEM A DQ<40>	MAKE_BASE=TRUE	MEM B DQ<40>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 6 -> DIMM A DQS 1		CPU CHANNEL B DQS 6 -> DIMM B DQS 1	
MEM A DQS N<6>	MAKE_BASE=TRUE	MEM B DQS N<6>	MAKE_BASE=TRUE
MEM A DQS P<6>	MAKE_BASE=TRUE	MEM B DQS P<6>	MAKE_BASE=TRUE
MEM A DQ<55>	MAKE_BASE=TRUE	MEM B DQ<55>	MAKE_BASE=TRUE
MEM A DQ<54>	MAKE_BASE=TRUE	MEM B DQ<54>	MAKE_BASE=TRUE
MEM A DQ<53>	MAKE_BASE=TRUE	MEM B DQ<53>	MAKE_BASE=TRUE
MEM A DQ<52>	MAKE_BASE=TRUE	MEM B DQ<52>	MAKE_BASE=TRUE
MEM A DQ<51>	MAKE_BASE=TRUE	MEM B DQ<51>	MAKE_BASE=TRUE
MEM A DQ<50>	MAKE_BASE=TRUE	MEM B DQ<50>	MAKE_BASE=TRUE
MEM A DQ<49>	MAKE_BASE=TRUE	MEM B DQ<49>	MAKE_BASE=TRUE
MEM A DQ<48>	MAKE_BASE=TRUE	MEM B DQ<48>	MAKE_BASE=TRUE
CPU CHANNEL A DQS 7 -> DIMM A DQS 0		CPU CHANNEL B DQS 7 -> DIMM B DQS 0	
MEM A DQS N<7>	MAKE_BASE=TRUE	MEM B DQS N<7>	MAKE_BASE=TRUE
MEM A DQS P<7>	MAKE_BASE=TRUE	MEM B DQS P<7>	MAKE_BASE=TRUE
MEM A DQ<63>	MAKE_BASE=TRUE	MEM B DQ<63>	MAKE_BASE=TRUE
MEM A DQ<62>	MAKE_BASE=TRUE	MEM B DQ<62>	MAKE_BASE=TRUE
MEM A DQ<61>	MAKE_BASE=TRUE	MEM B DQ<61>	MAKE_BASE=TRUE
MEM A DQ<60>	MAKE_BASE=TRUE	MEM B DQ<60>	MAKE_BASE=TRUE
MEM A DQ<59>	MAKE_BASE=TRUE	MEM B DQ<59>	MAKE_BASE=TRUE
MEM A DQ<58>	MAKE_BASE=TRUE	MEM B DQ<58>	MAKE_BASE=TRUE
MEM A DQ<57>	MAKE_BASE=TRUE	MEM B DQ<57>	MAKE_BASE=TRUE
MEM A DQ<56>	MAKE_BASE=TRUE	MEM B DQ<56>	MAKE_BASE=TRUE

DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.



MEMORY CLOCK ALIASING

MEM A CLK P<0>	MAKE_BASE=TRUE	MEM A CLK P<0>	NO_TEST=TRUE
MEM A CLK N<0>	MAKE_BASE=TRUE	MEM A CLK N<0>	NO_TEST=TRUE
MEM A CLK P<1>	MAKE_BASE=TRUE	MEM A CLK P<1>	NO_TEST=TRUE
MEM A CLK N<1>	MAKE_BASE=TRUE	MEM A CLK N<1>	NO_TEST=TRUE
MEM A CLK P<2>	MAKE_BASE=TRUE	MEM A CLK P<2>	NO_TEST=TRUE
MEM A CLK N<2>	MAKE_BASE=TRUE	MEM A CLK N<2>	NO_TEST=TRUE
MEM A CLK P<3>	MAKE_BASE=TRUE	MEM A CLK P<3>	NO_TEST=TRUE
MEM A CLK N<3>	MAKE_BASE=TRUE	MEM A CLK N<3>	NO_TEST=TRUE
MEM B CLK P<0>	MAKE_BASE=TRUE	MEM B CLK P<0>	NO_TEST=TRUE
MEM B CLK N<0>	MAKE_BASE=TRUE	MEM B CLK N<0>	NO_TEST=TRUE
MEM B CLK P<1>	MAKE_BASE=TRUE	MEM B CLK P<1>	NO_TEST=TRUE
MEM B CLK N<1>	MAKE_BASE=TRUE	MEM B CLK N<1>	NO_TEST=TRUE
MEM B CLK P<2>	MAKE_BASE=TRUE	MEM B CLK P<2>	NO_TEST=TRUE
MEM B CLK N<2>	MAKE_BASE=TRUE	MEM B CLK N<2>	NO_TEST=TRUE
MEM B CLK P<3>	MAKE_BASE=TRUE	MEM B CLK P<3>	NO_TEST=TRUE
MEM B CLK N<3>	MAKE_BASE=TRUE	MEM B CLK N<3>	NO_TEST=TRUE

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	L	L
H	L	X	X	L	H
L	L	X	X	L	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	L	L

SYNC MASTER=K62 SYNC DATE=01/06/2011

DDR3 SUPPORT AND BITSWAPS

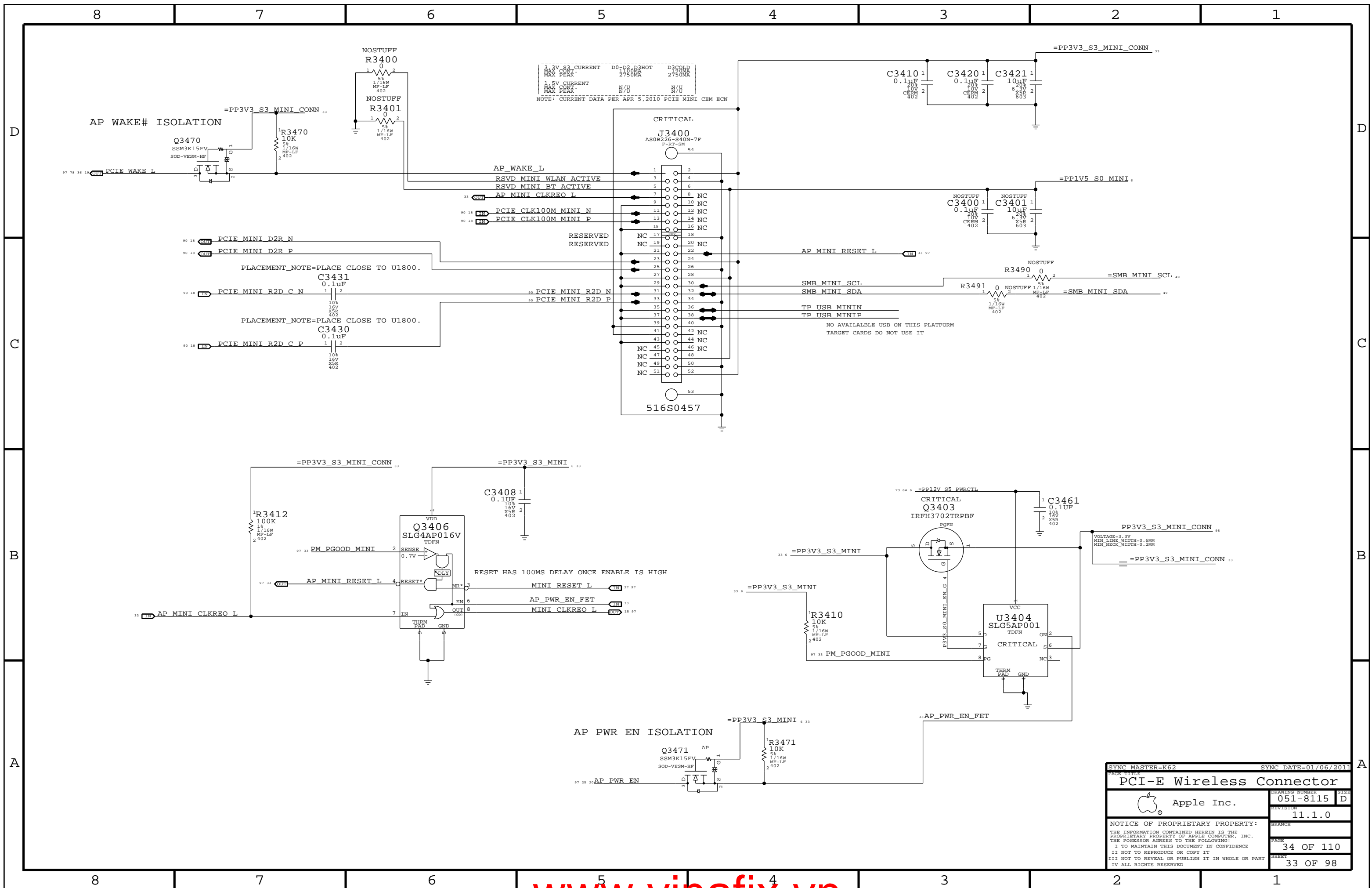
Apple Inc.

051-8115

11.1.0

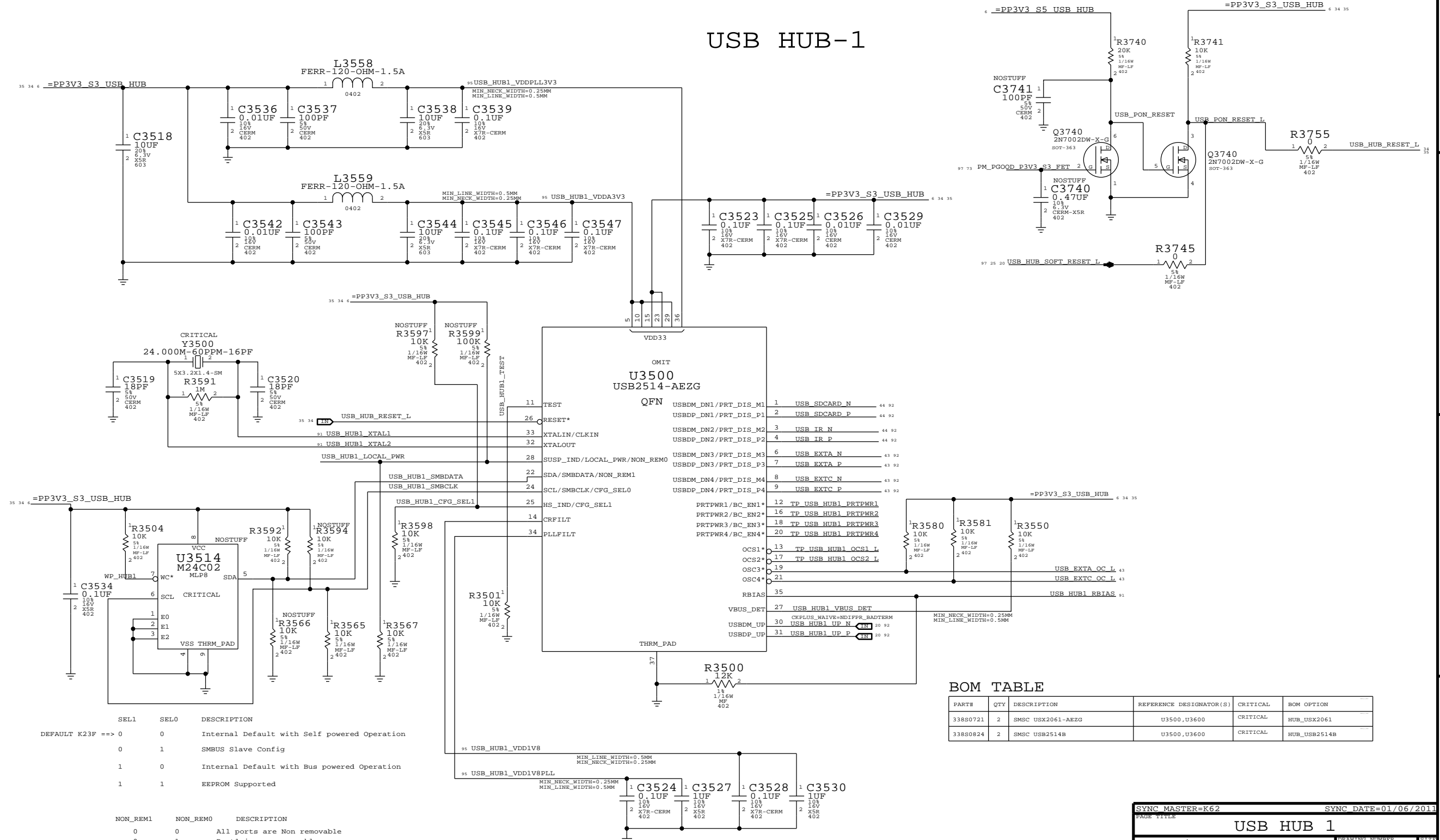
33 OF 110

32 OF 98



SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE PCI-E Wireless Connector			
DRAWING NUMBER 051-8115		SIZE D	
REVISION 11.1.0		BRANCH	
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PAGE 34 OF 110		SHEET 33 OF 98	

USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REMO	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

SYNC MASTER=K62 SYNC DATE=01/06/2011

USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

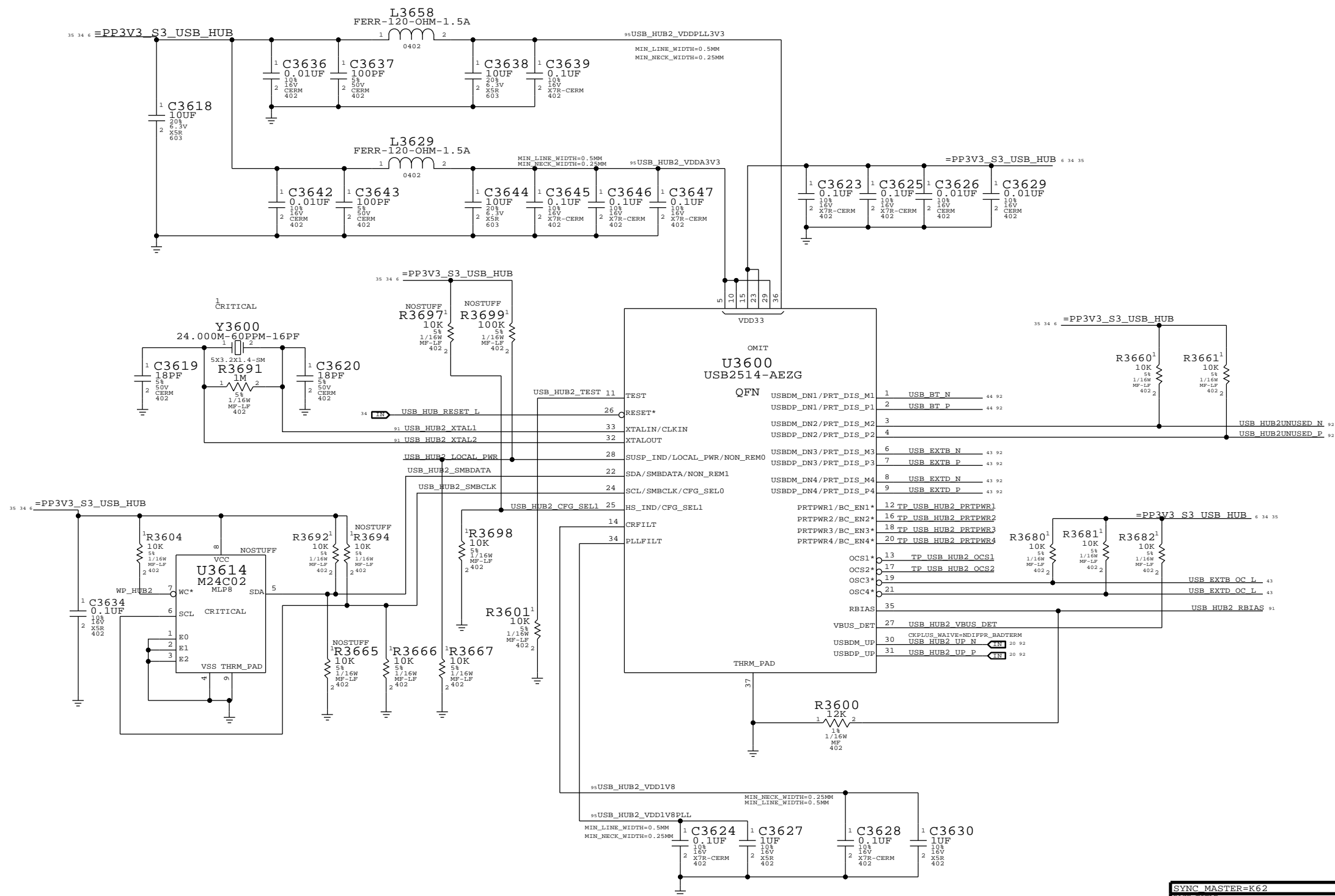
BRANCH:

PAGE: 35 OF 110

SHEET: 34 OF 98

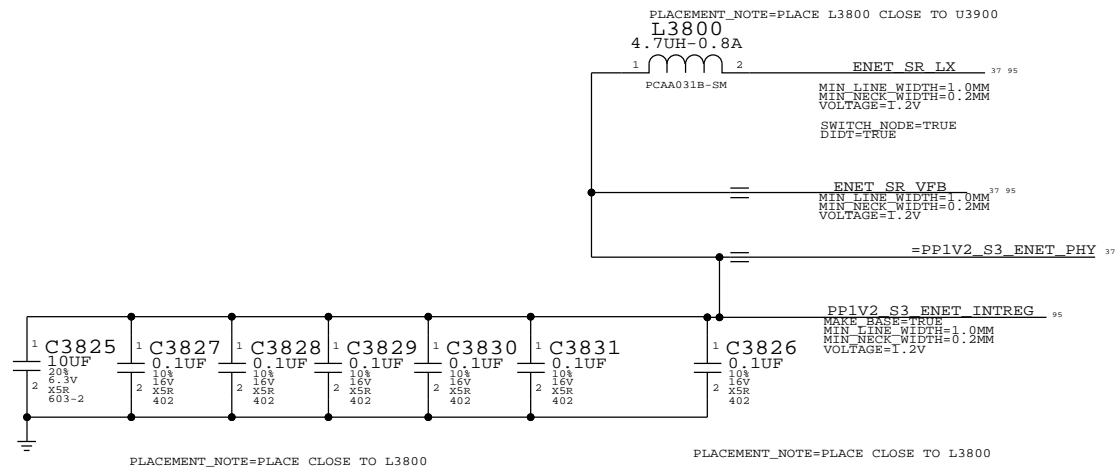
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USB HUB-2

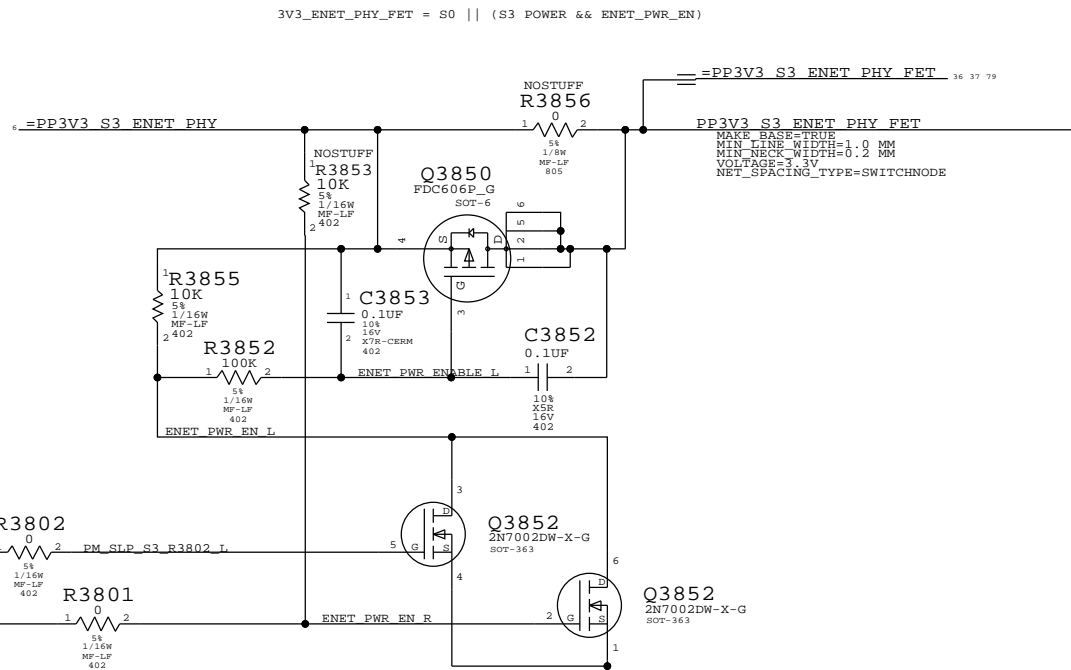


SYNC MASTER=K62		SYNC DATE=01/06/2011	
USB HUB 2			
Apple Inc.		DRAWING NUMBER	051-8115
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		PAGE	36 OF 110
		SHEET	35 OF 98

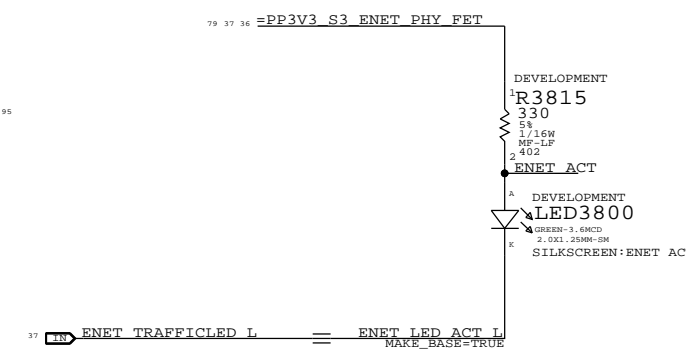
CAESAR IV 1.2V INT.VR CMPTS



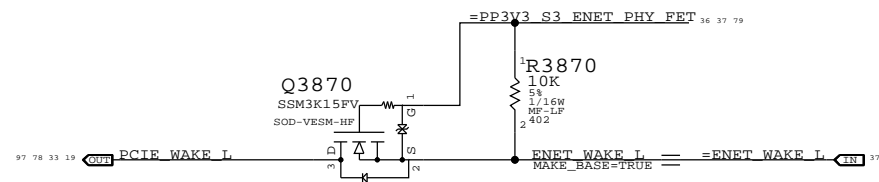
CAESAR IV POWER ENABLE CIRCUIT



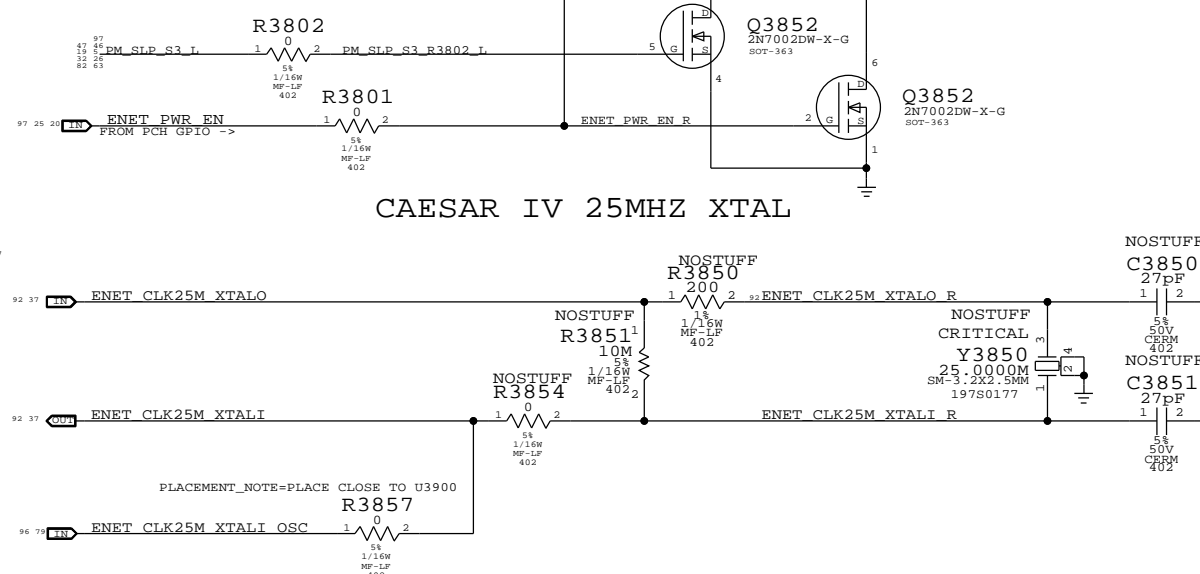
CAESAR IV ACTIVITY LED



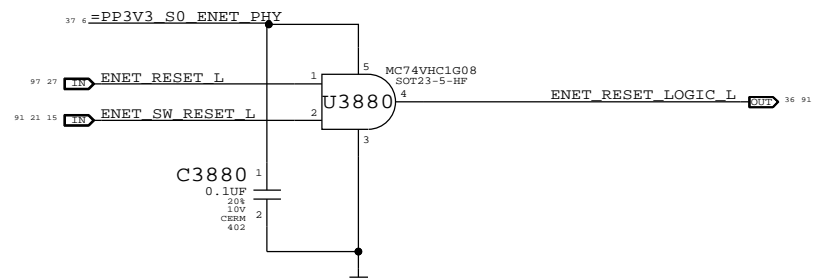
CAESAR IV WAKE# ISOLATION



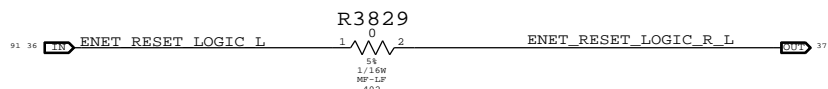
CAESAR IV 25MHZ XTAL



CAESAR IV SW RESET GATING

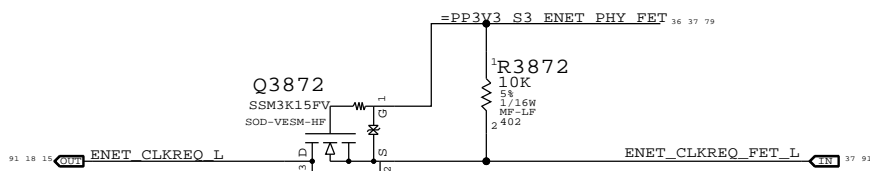


CAESAR IV RESET CONNECTION

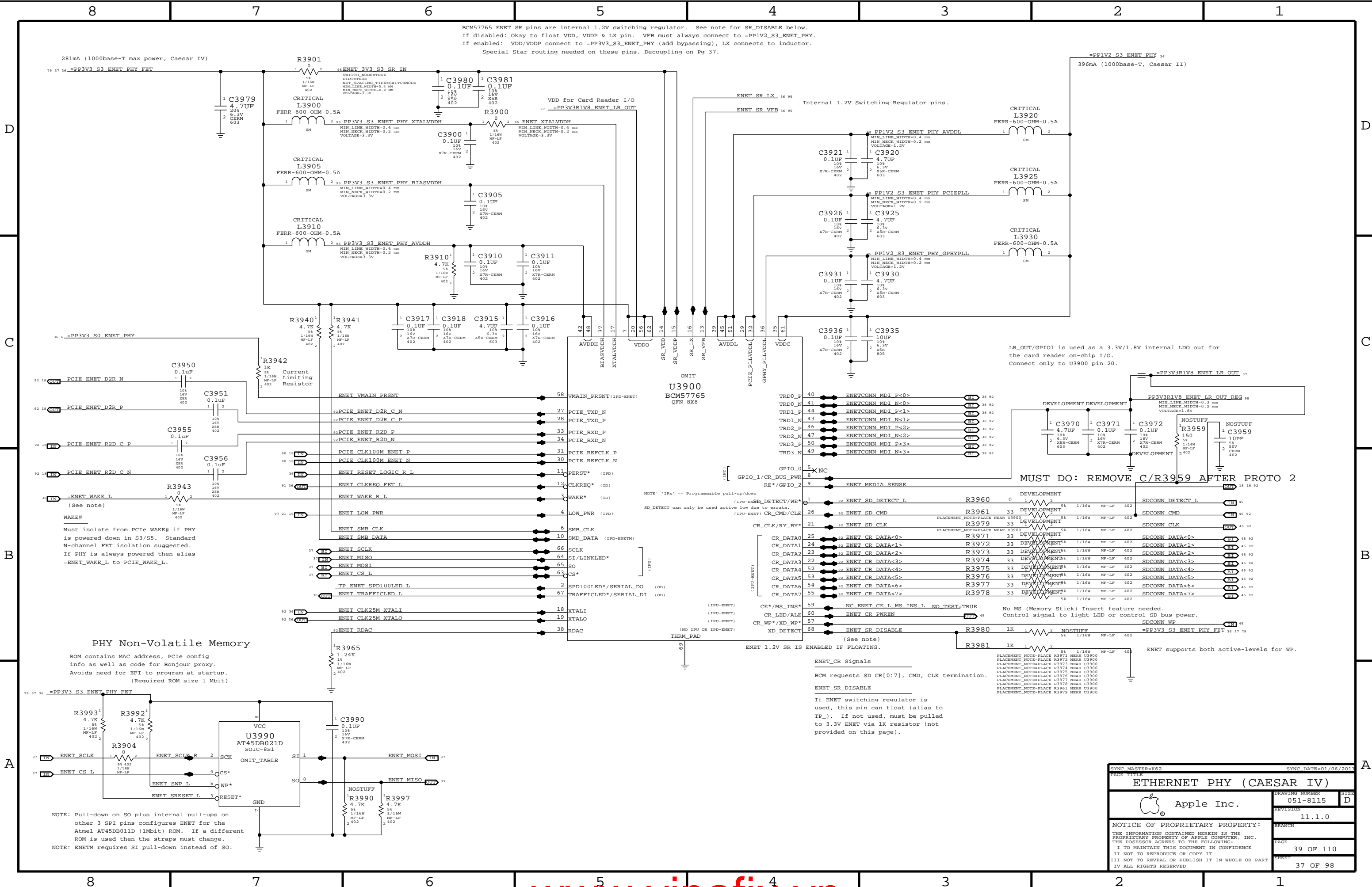


CAESAR IV STRAPS (NONE)

CAESAR IV CLKREQ ISOLATION



SYNC MASTER=K62		SYNC DATE=01/06/2011	
CAESAR IV SUPPORT			
Apple Inc.	DRAWING NUMBER	051-8115	SIZE
	REVISION	11.1.0	D
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		SHEET	36 OF 98



BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
 If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
 If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
 Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)
 =PP3V3_S3_ENET_PHY_FET

=PP1V2_S3_ENET_PHY 36
 396mA (1000base-T, Caesar II)

=PP3V3_S0_ENET_PHY

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIe_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EPI to program at startup. (Required ROM size 1 Mbit)

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
 NOTE: ENETM requires SI pull-down instead of SO.

Internal 1.2V Switching Regulator pins.

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O. Connect only to U3900 pin 20.

MUST DO: REMOVE C/R3959 AFTER PROTO 2

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

ENET supports both active-levels for WP.

No MS (Memory Stick) Insert feature needed. Control signal to light LED or control SD bus power.

ENET SD DETECT L

ENET SD CMD

ENET SD CLK

ENET CR DATA<0>

ENET CR DATA<1>

ENET CR DATA<2>

ENET CR DATA<3>

ENET CR DATA<4>

ENET CR DATA<5>

ENET CR DATA<6>

ENET CR DATA<7>

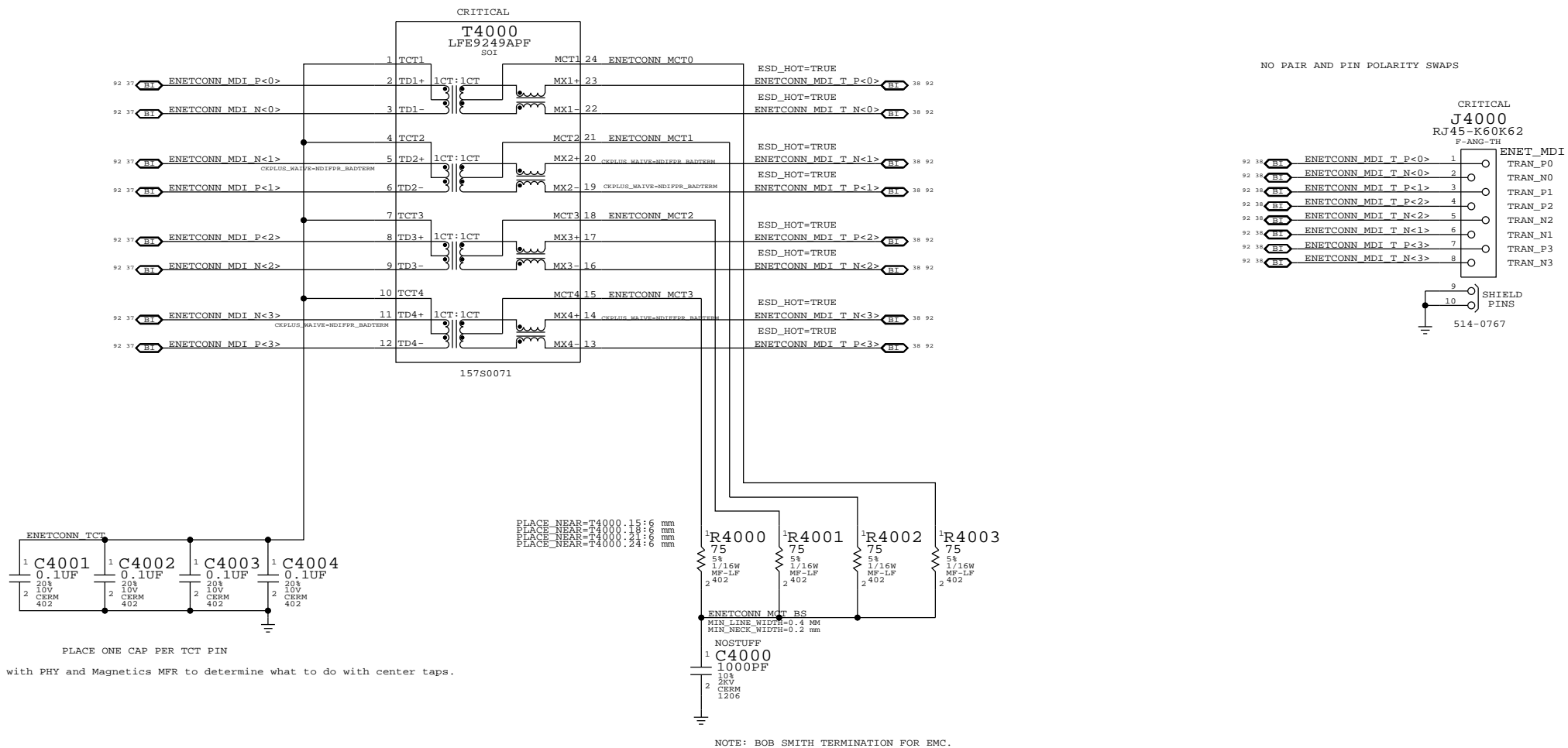
ENET CE L MS INS L NO_TEST=TRUE

ENET CR PWRDN

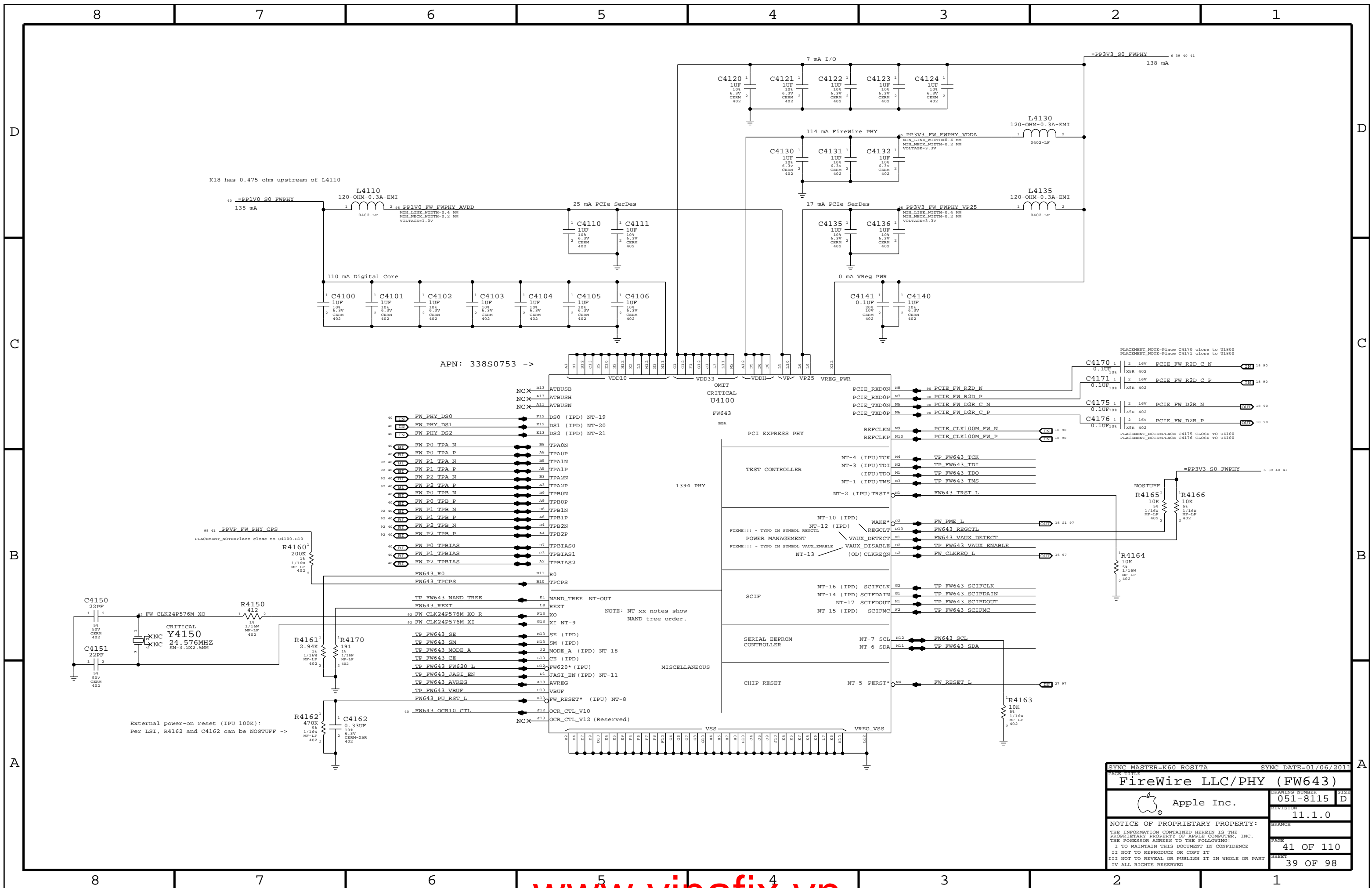
ENET SR_DISABLE

SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE			
ETHERNET PHY (CAESAR IV)			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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THIS PAGE DIFFERENT BETWEEN K60 and K62.



SYNC MASTER=K60 MARK		SYNC DATE=01/06/2011	
Ethernet Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	11.1.0
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APN: 338S0753 ->

External power-on reset (IPU 100K):
Per LSI, R4162 and C4162 can be NOSTUFF ->

PLACEMENT_NOTE=Place C4170 close to U1800
PLACEMENT_NOTE=Place C4171 close to U1800

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

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PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

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PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

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PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
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PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

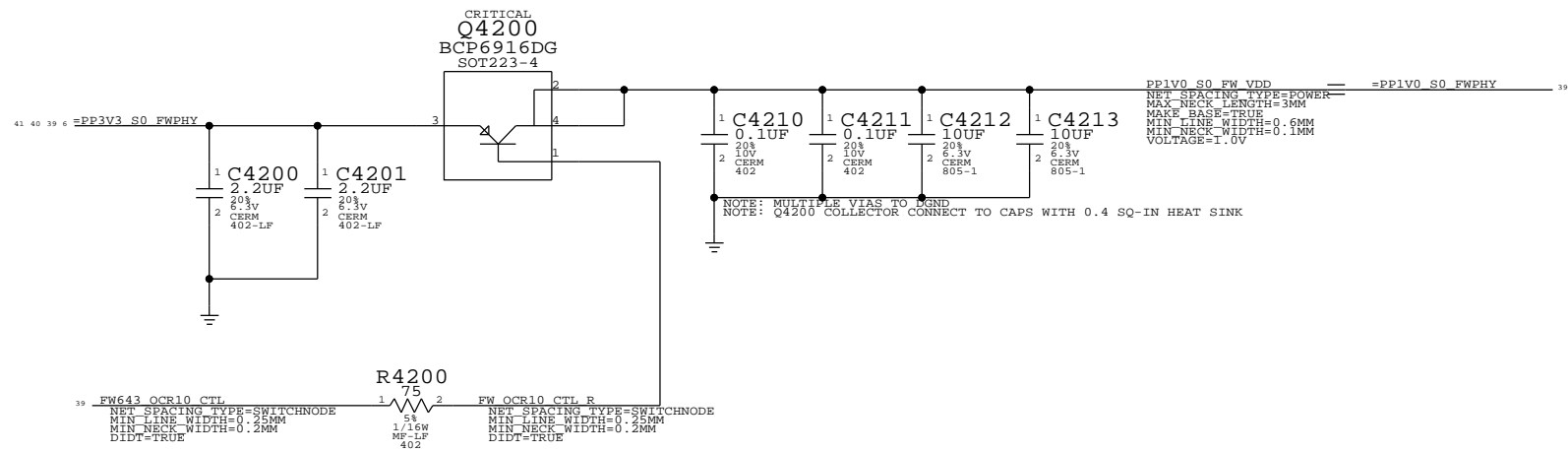
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PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

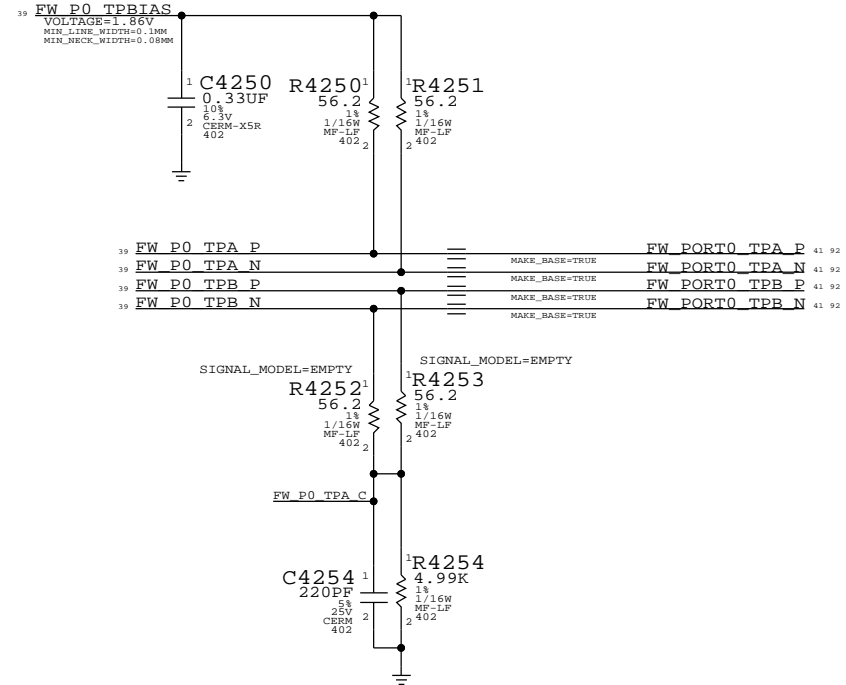
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PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100

SYNC MASTER=K60 ROSITA		SYNC DATE=01/06/2011	
PAGE TITLE			
FireWire LLC/PHY (FW643)			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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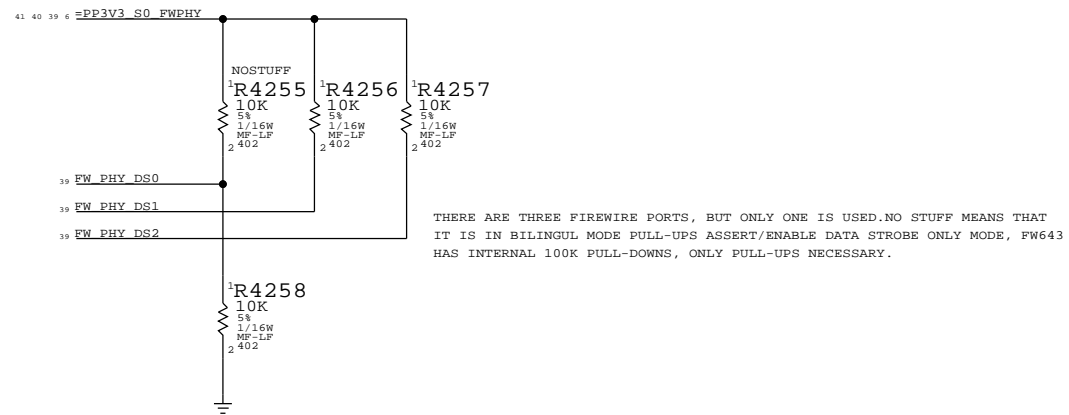
FW643 1.0V GENERATION



Termination
Place close to FireWire PHY



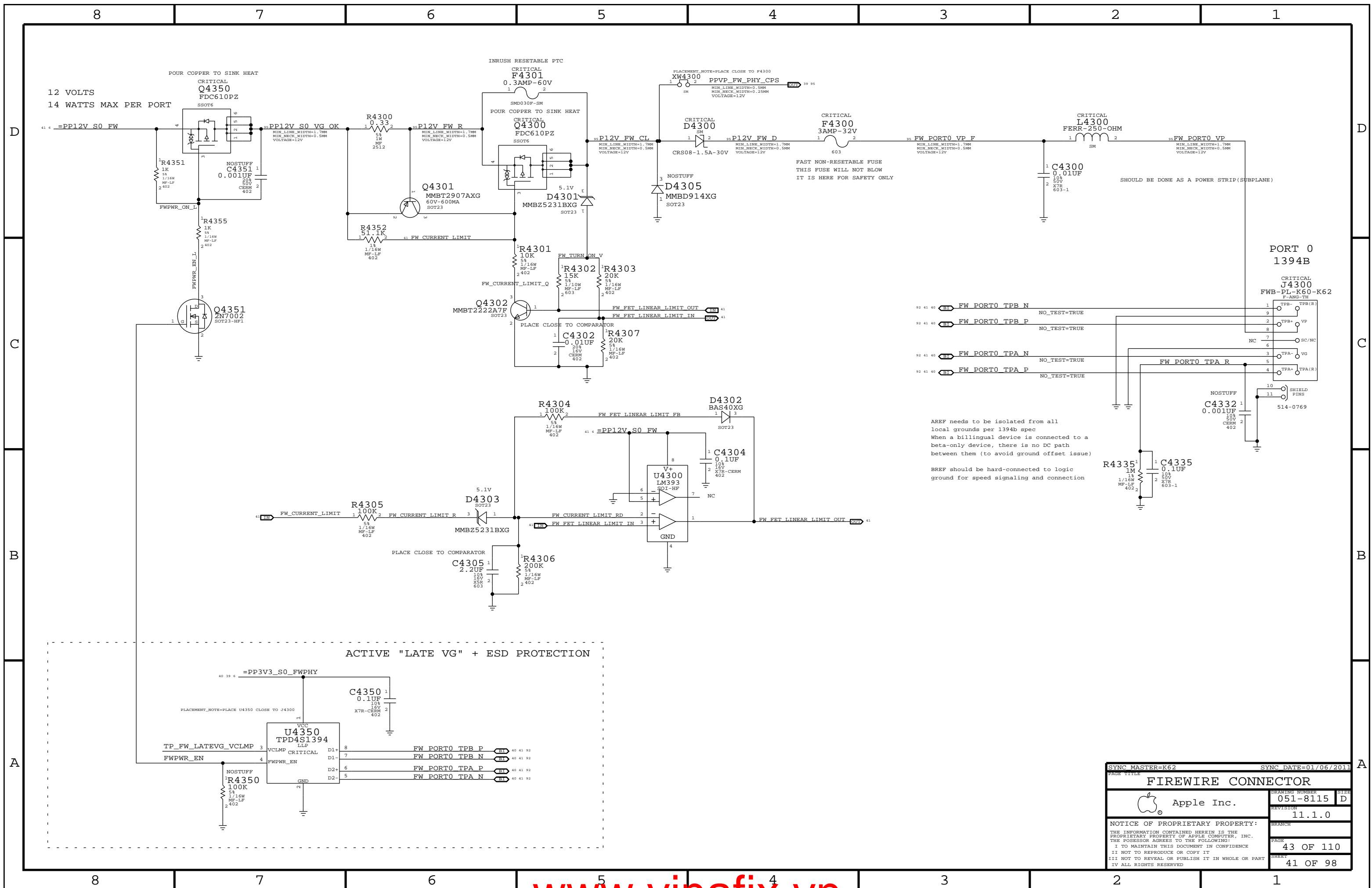
1394 PHY DATA/STROBE OPTIONS



2ND & 3RD TPA/TPB PAIR UNUSED

- 39 FW_P1_TPBIAIS == NC_FW_PORT1_TPBIAIS
 - 39 FW_P1_TPA_P == NC_FW_PORT1_TPA_P
 - 39 FW_P1_TPA_N == NC_FW_PORT1_TPA_N
 - 39 FW_P1_TPB_P == NC_FW_PORT1_TPB_P
 - 39 FW_P1_TPB_N == NC_FW_PORT1_TPB_N
 - 39 FW_P2_TPBIAIS == NC_FW_PORT2_TPBIAIS
 - 39 FW_P2_TPA_P == NC_FW_PORT2_TPA_P
 - 39 FW_P2_TPA_N == NC_FW_PORT2_TPA_N
 - 39 FW_P2_TPB_P == NC_FW_PORT2_TPB_P
 - 39 FW_P2_TPB_N == NC_FW_PORT2_TPB_N
- NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

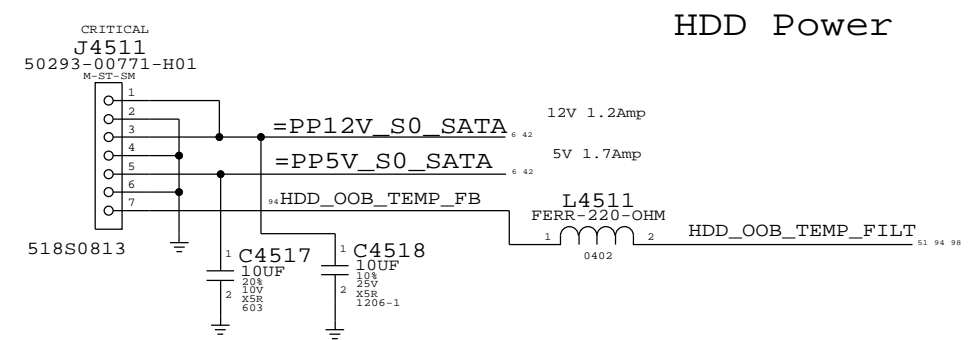
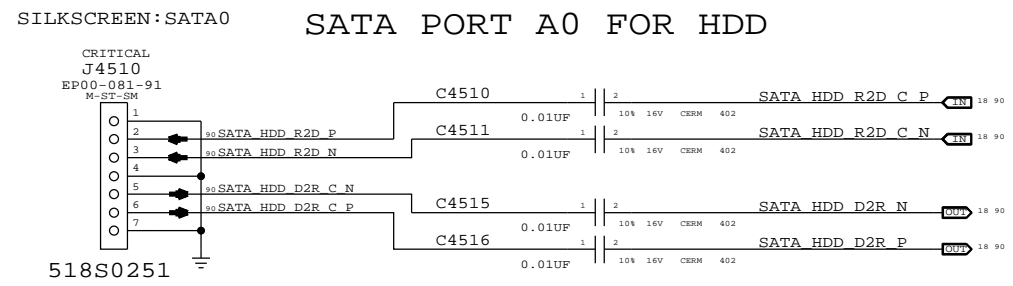
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PAGE TITLE FireWire: 1394B MISC			
DRAWING NUMBER 051-8115		SIZE D	
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FW PORT0 TPA N NO_TEST=TRUE
 FW PORT0 TPA P NO_TEST=TRUE
 FW PORT0 TPA N NO_TEST=TRUE
 FW PORT0 TPA P NO_TEST=TRUE

AREF needs to be isolated from all local grounds per 1394b spec. When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue).
 BREF should be hard-connected to logic ground for speed signaling and connection.

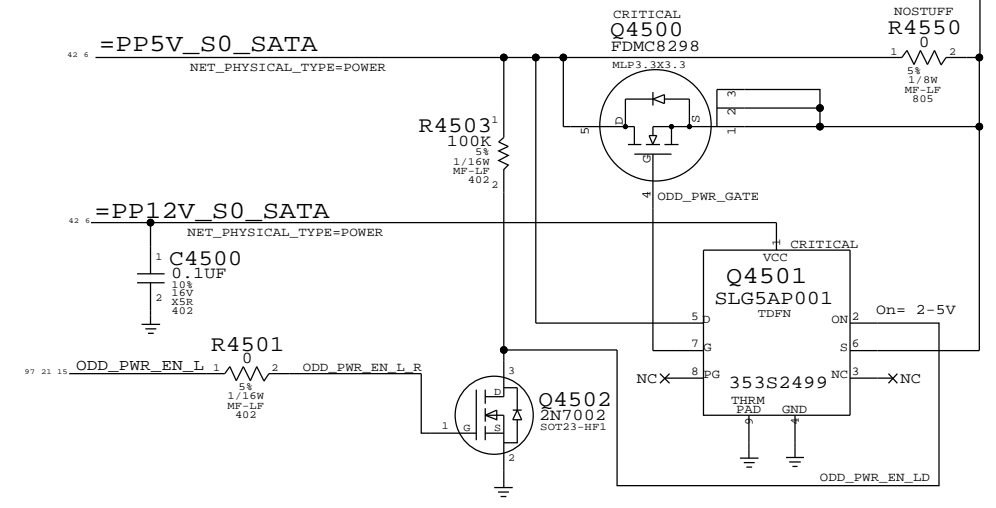
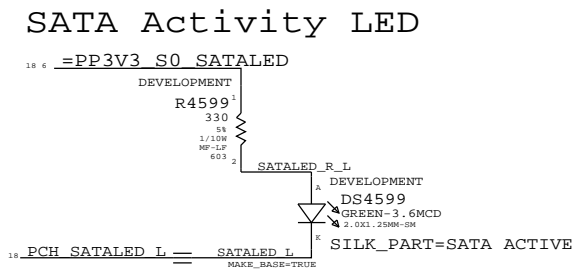
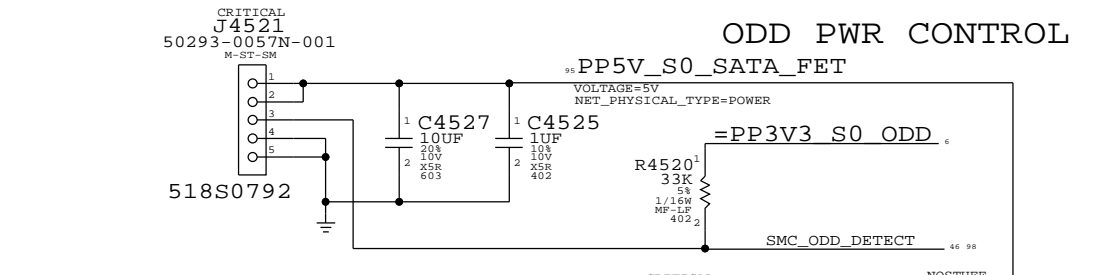
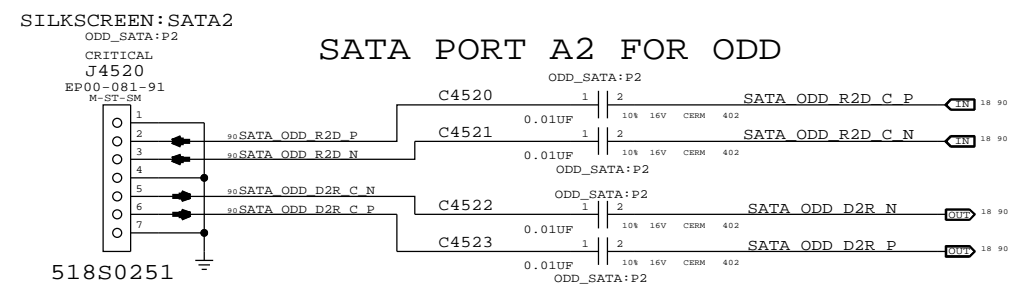
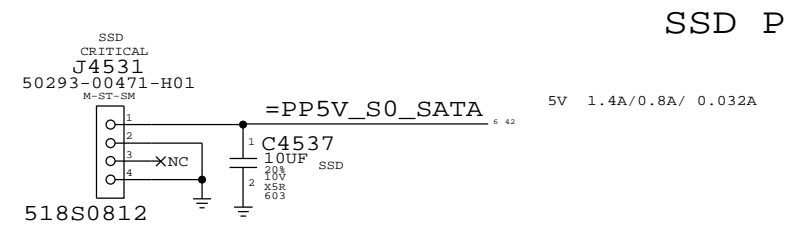
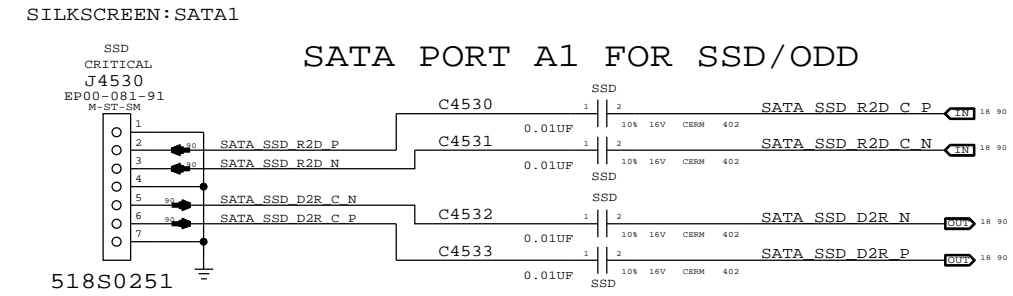
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PAGE TITLE			
FIREWIRE CONNECTOR			
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	REVISION	11.1.0	
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BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

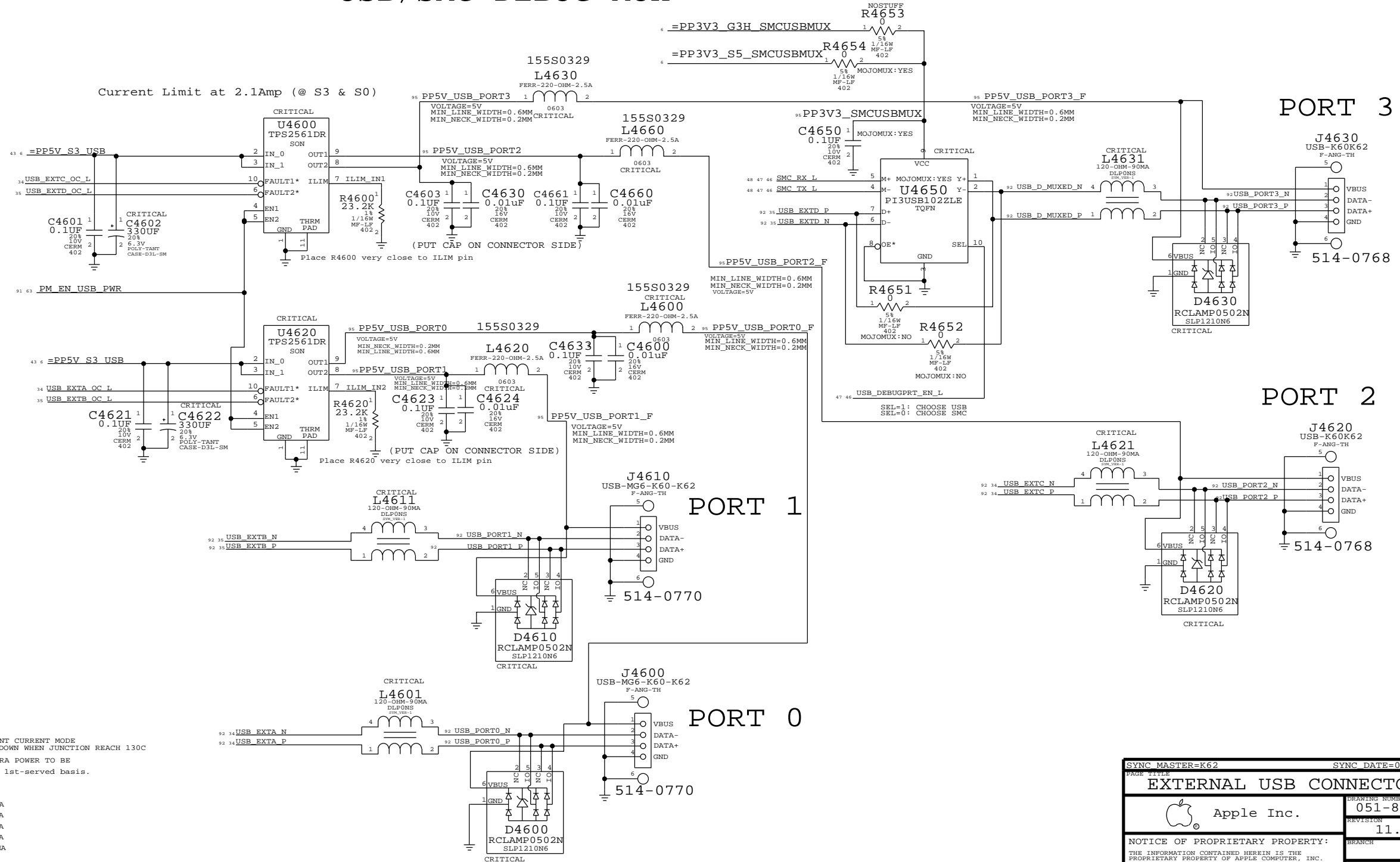
A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.
K60E should stuff S_P1_ODD=YES because it has no SSD option.



SYNC MASTER=K60 JERRY		SYNC DATE=01/06/2011	
SATA Connectors			
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USB/SMC DEBUG MUX ADDED AT EVT & SWITCH TO S5 RAIL



USB PORT POWER:
EACH PORT IS HARDWARE Capable of :
STATE MAX MIN (WITHIN THE TOLERANCE)
S0, S3 2.7A 2.1A -- PER PORT

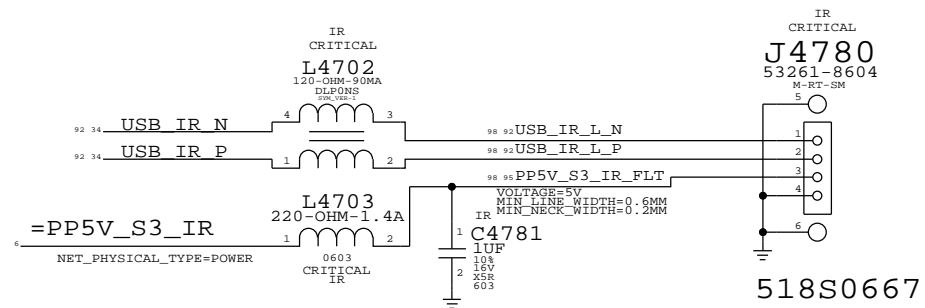
WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALLOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

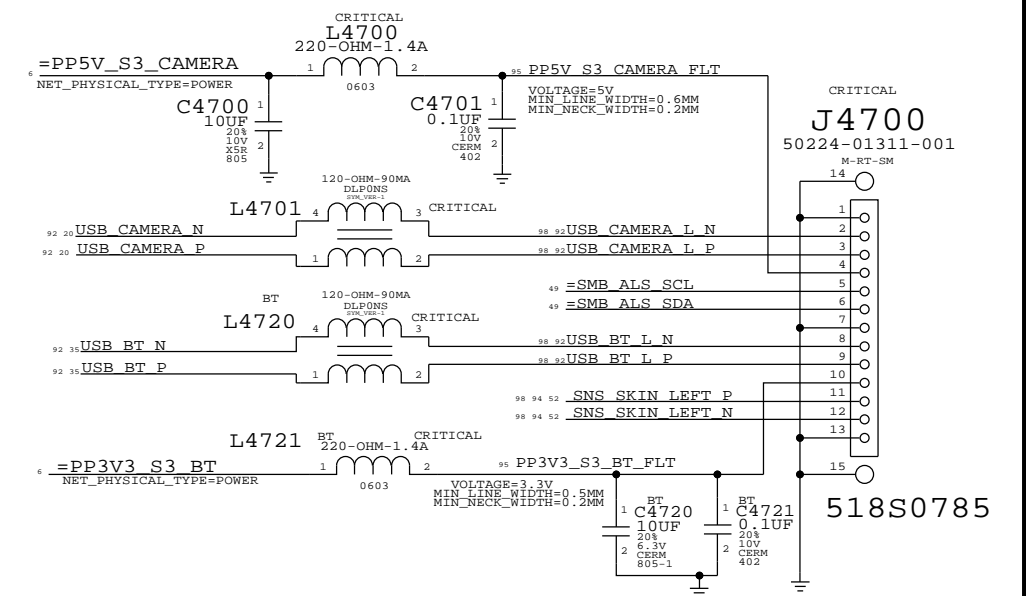
EXAMPLE: Port 1 - iPad fast charging = 2100mA
Port 2 - Wired Keyboard = 1100mA
Port 3 - iPhone fast charging = 1000mA
PORT 4 - USB 2.0 500MA = 500MA
TOTAL: 4700MA

SYNC MASTER=K62		SYNC DATE=01/06/2011	
EXTERNAL USB CONNECTORS			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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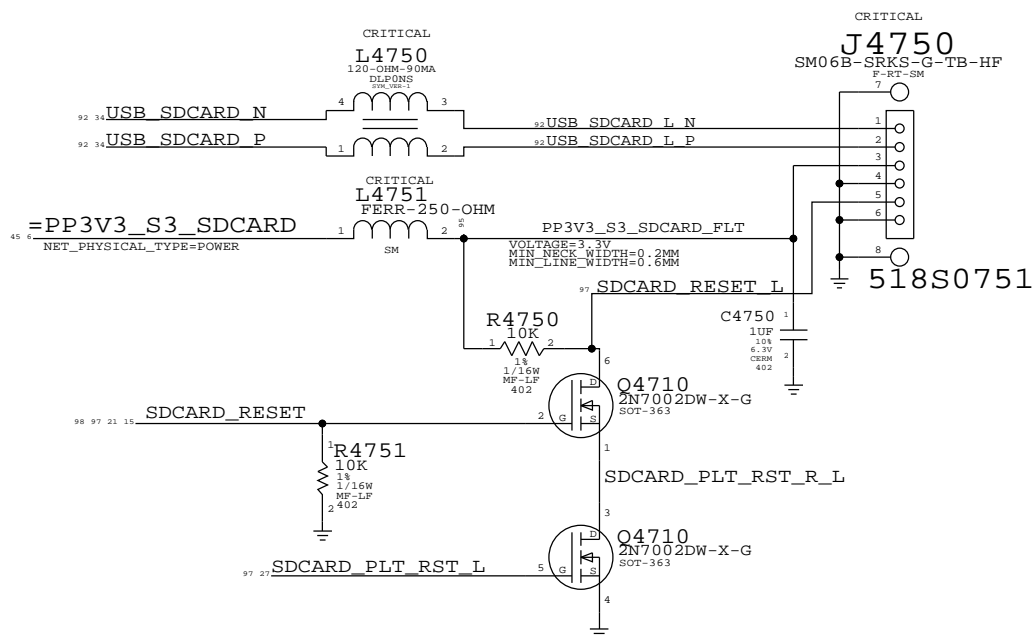
IR RECEIVER CONNECTOR



CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



SD Card Reader Board (Lazarus)

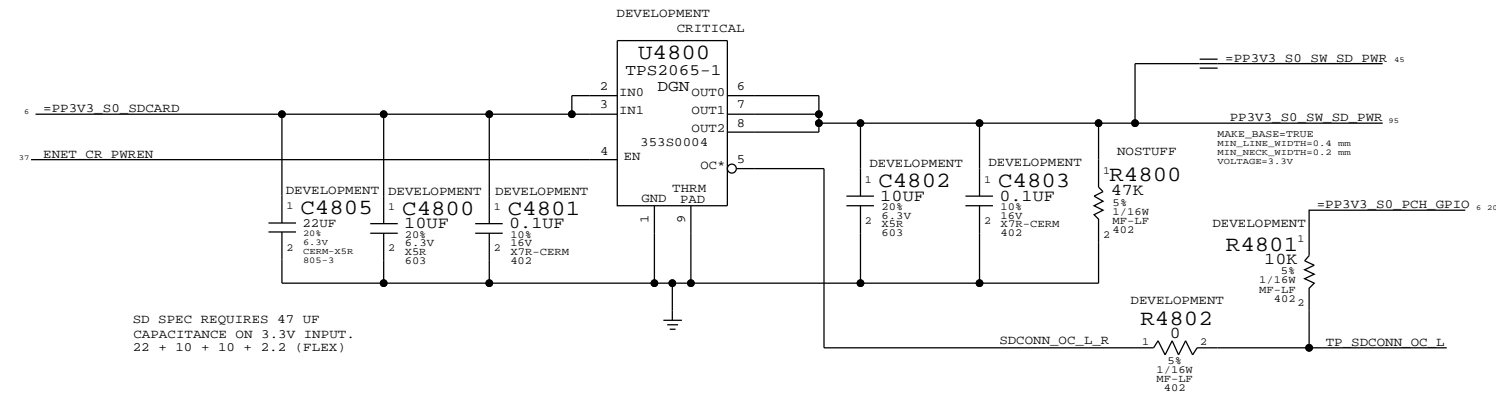


Skin Temp sense at upper Left Screen corner

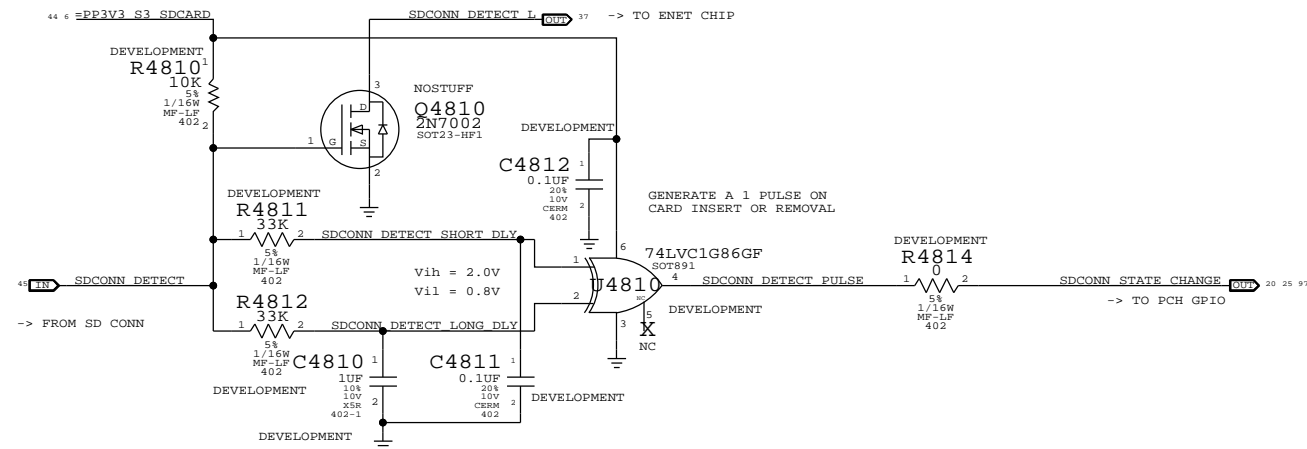
SYNC MASTER=K62		SYNC DATE=01/06/2011	
Internal USB Connections			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

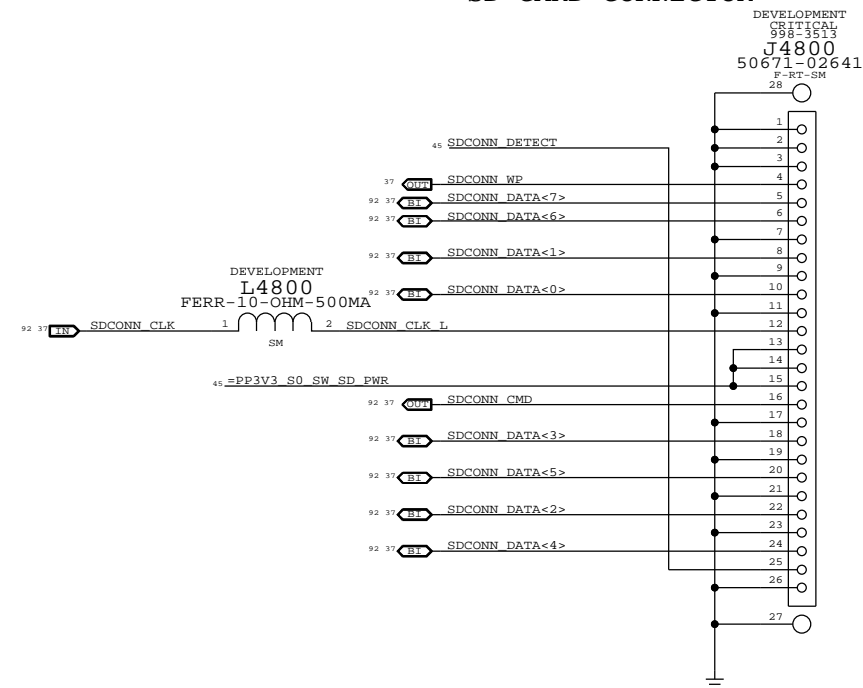
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.



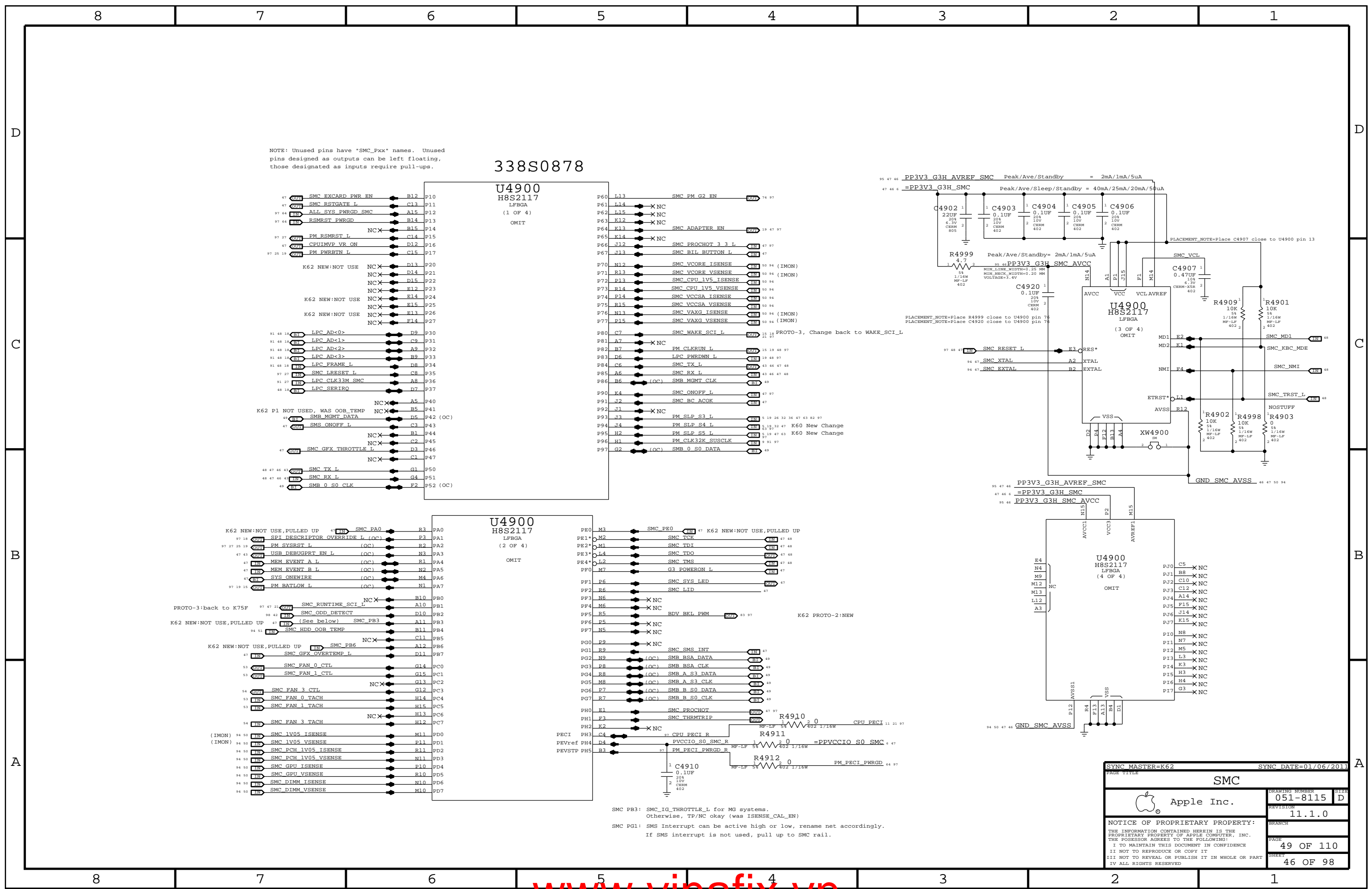
SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR

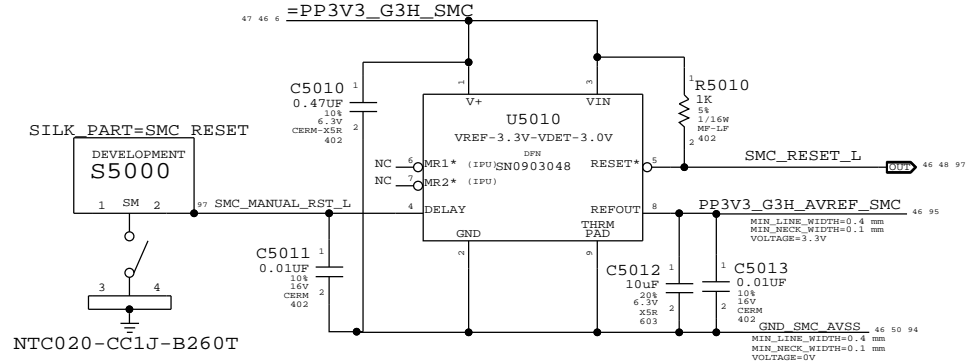


SYNC MASTER=K62		SYNC DATE=01/06/2011	
SD READER CONNECTOR			
Apple Inc.		DRAWING NUMBER	051-8115
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		PAGE	48 OF 110
		SHEET	45 OF 98



SYNC MASTER=K62		SYNC DATE=01/06/2011	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		11.1.0	
		BRANCH	
		PAGE	
		49 OF 110	
		SHEET	
		46 OF 98	

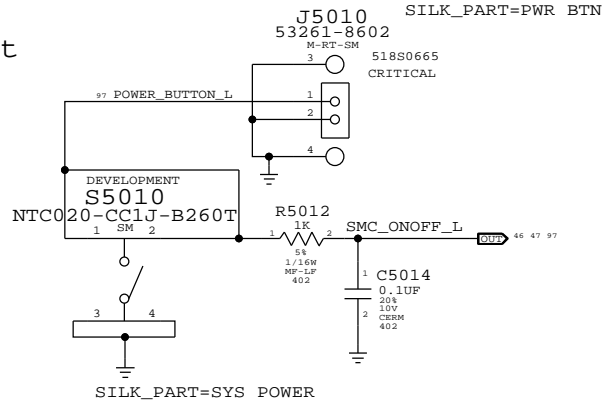
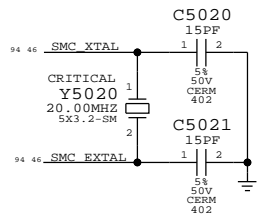
SMC Reset "Button", Supervisor & AVREF Supply



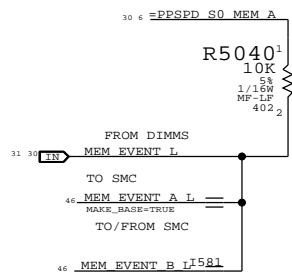
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

POWER BUTTON

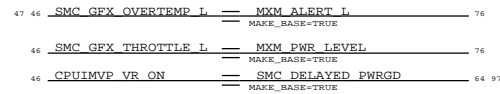
SMC Crystal Circuit



MEM_EVENT

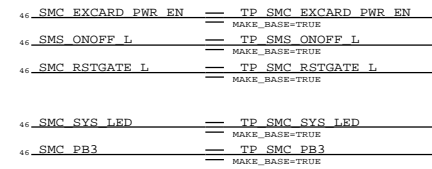


MISC. SIGNAL ALIASES

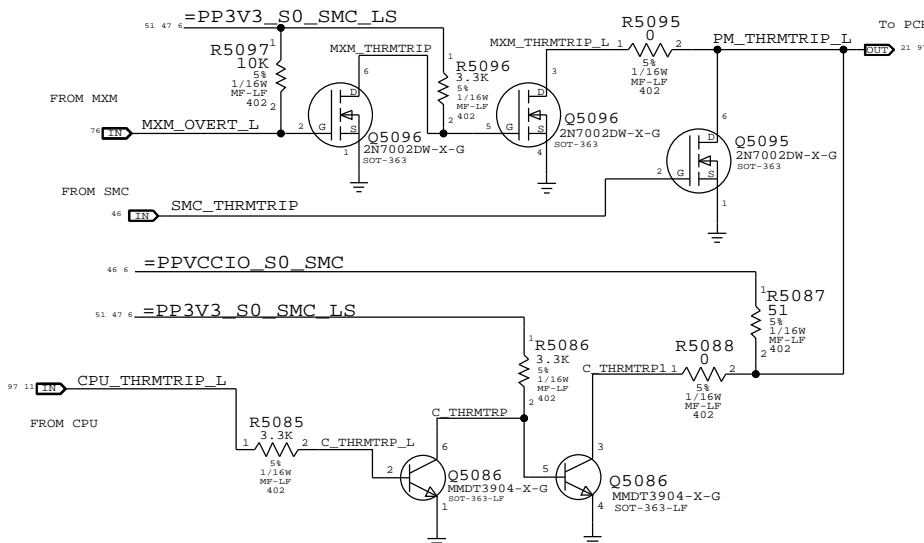


UNUSED PORT 7 ANALOG SENSORS

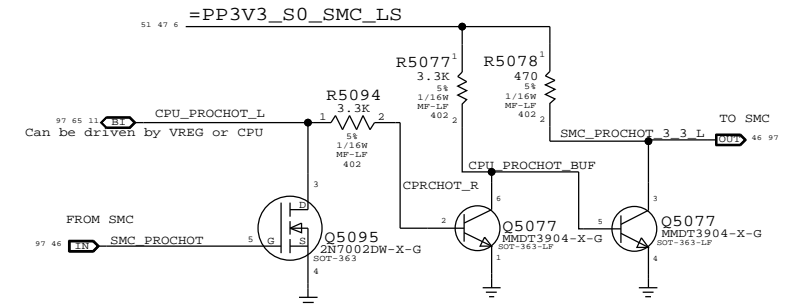
UNUSED TP/NC ALIASES



SMC & MXM THERMTRIP LEVEL SHIFTING

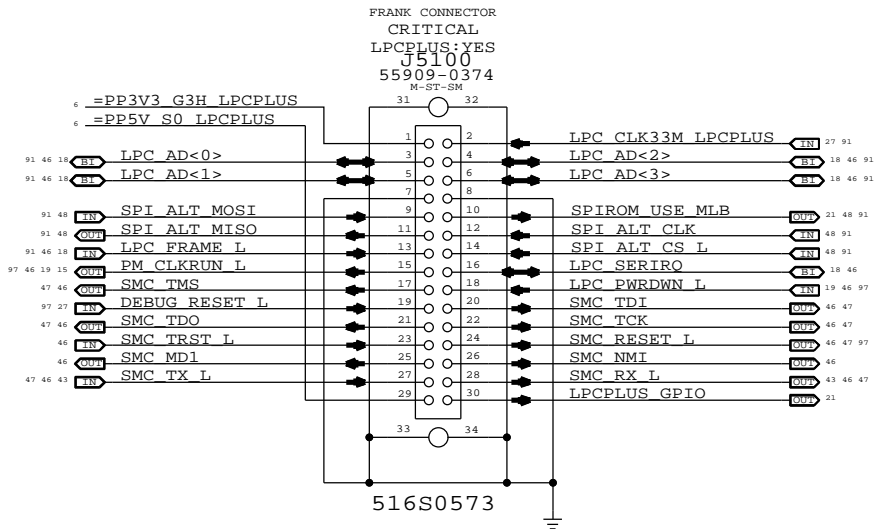


SMC PROCHOT 3.3V LEVEL SHIFTING

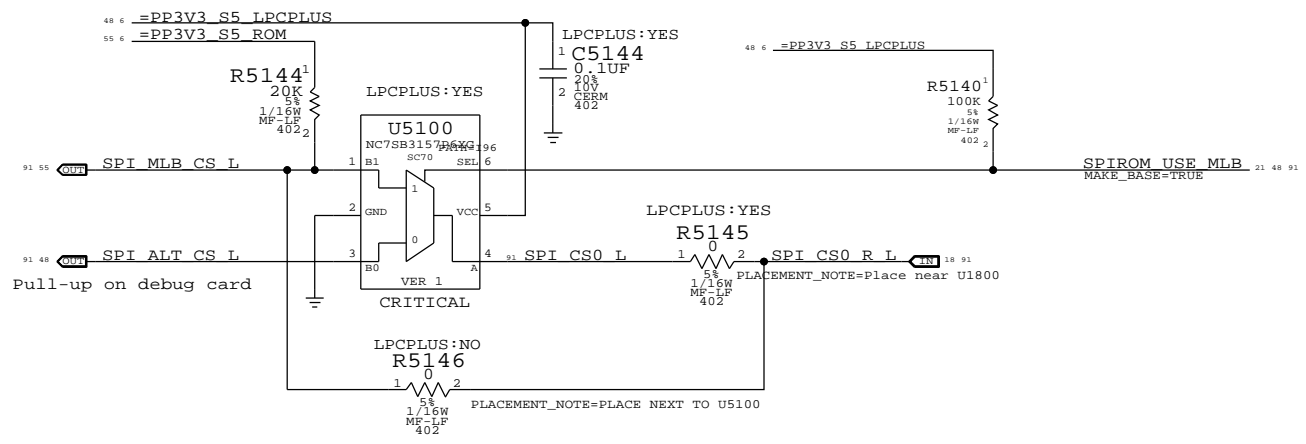


SYNC MASTER=K62		SYNC DATE=01/06/2011	
SMC Support			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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		PAGE	50 OF 110
		SHEET	47 OF 98

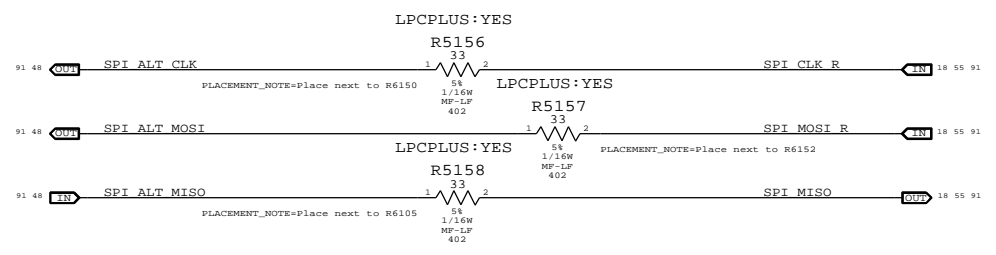
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC MASTER=K62 AARON		SYNC DATE=11/30/2009	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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		SHEET	48 OF 98

PCH "SMBUS" CONNECTIONS

PCH "SML 0" CONNECTIONS

SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)

SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

DISPLAY TCON TO SPTX OR O2M BLC

SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

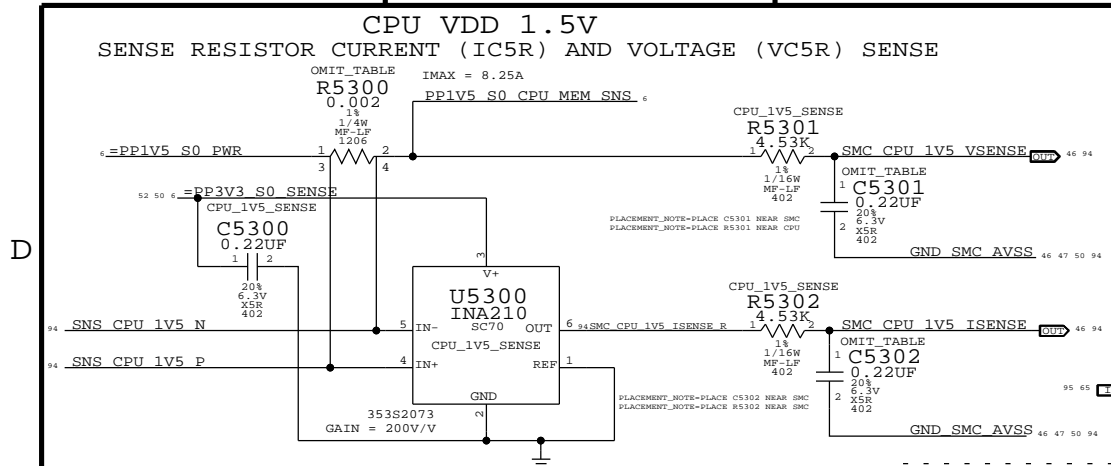
T29 I2C CONNECTIONS

I2C BUS PULL-UP RAIL MUST REFLECT WHEN USB POWER (VBUS) IS VALID.

PCH "SML 1" CONNECTIONS

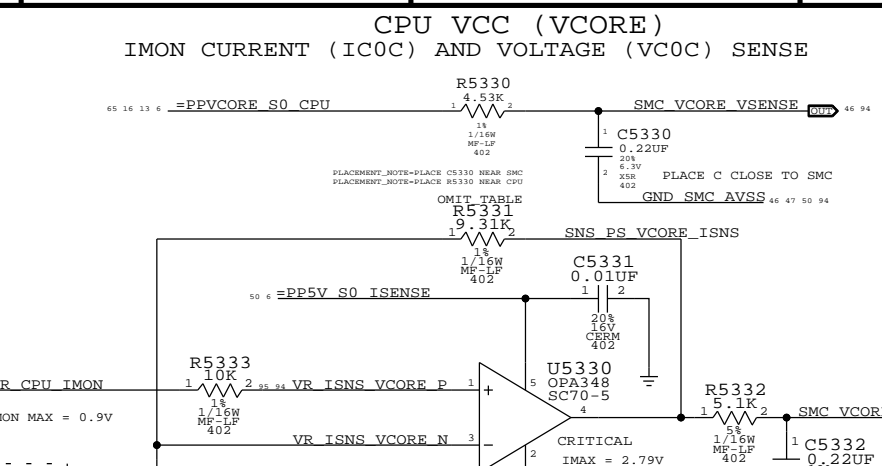
Also reserve 0x56 and 0x32 per spec

SYNC MASTER=K60 MARK		SYNC DATE=01/06/2011	
SMBUS CONNECTIONS			
Apple Inc.		DRAWING NUMBER	051-8115
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		PAGE	52 OF 110
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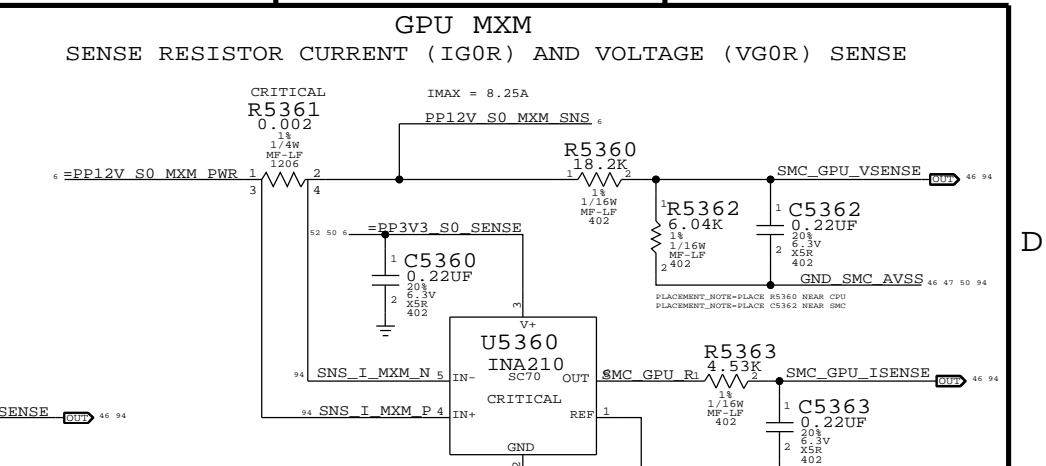
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5300	CPU_V5_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5300	NO_CPU_V5_SENSE
132S0080	2	CAP, 0.22UF, 402	C5301, C5302	CPU_V5_SENSE
116S0004	2	RES, 0 OHM, 402	C5301, C5302	NO_CPU_V5_SENSE

NOTE: THE NO IV05 PCH SENSE, NO CPU VCCSA SENSE, AND NO CPU VCCS SENSE OPTIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.



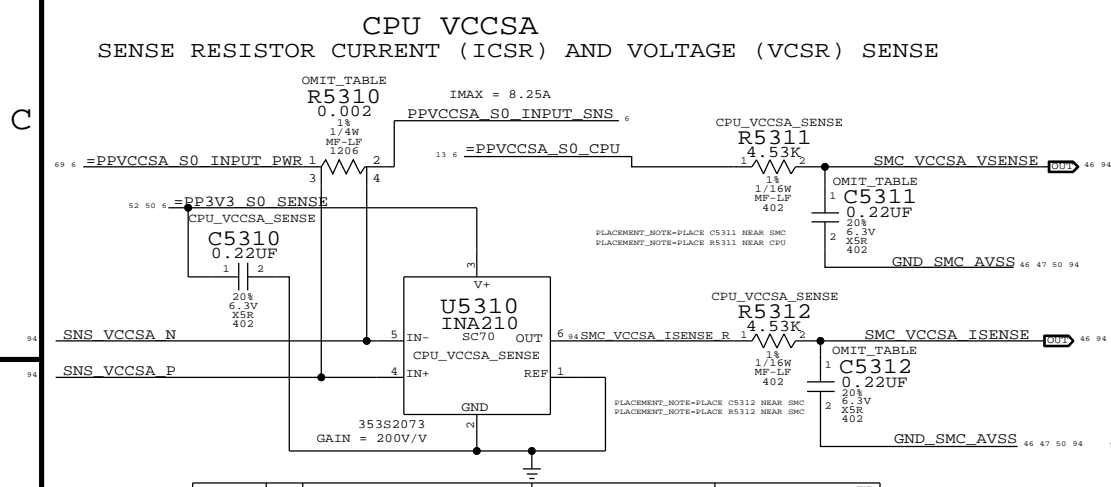
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES, MTL FILM, 1/16W, 9.31K, 0402	R5331	CPUVCORE-3PH
114S0345	1	RES, MTL FILM, 1/16W, 21K, 0402	R5331	CPUVCORE-4PH

CRITICAL IMAX = 2.79V



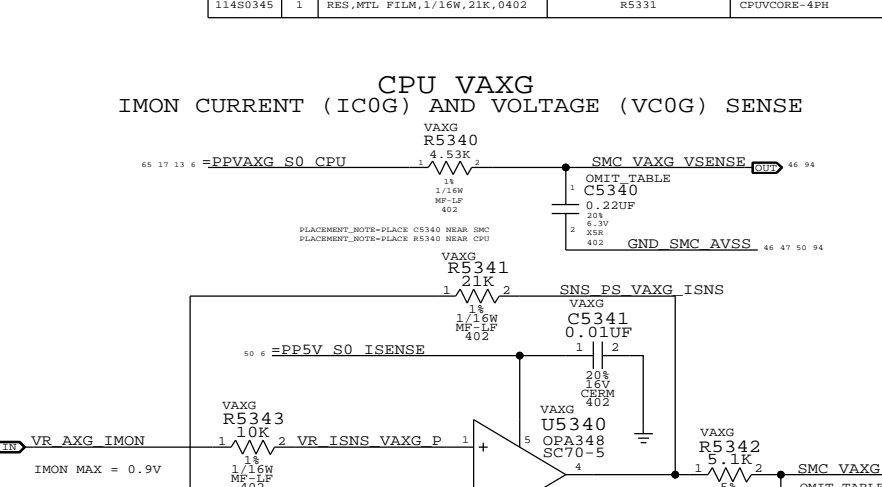
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP, 0.22UF, 402	C5362, C5372	DIMM_V5_SENSE
116S0004	2	RES, 0 OHM, 402	C5371, C5372	PRODUCTION

CRITICAL IMAX = 8.25A



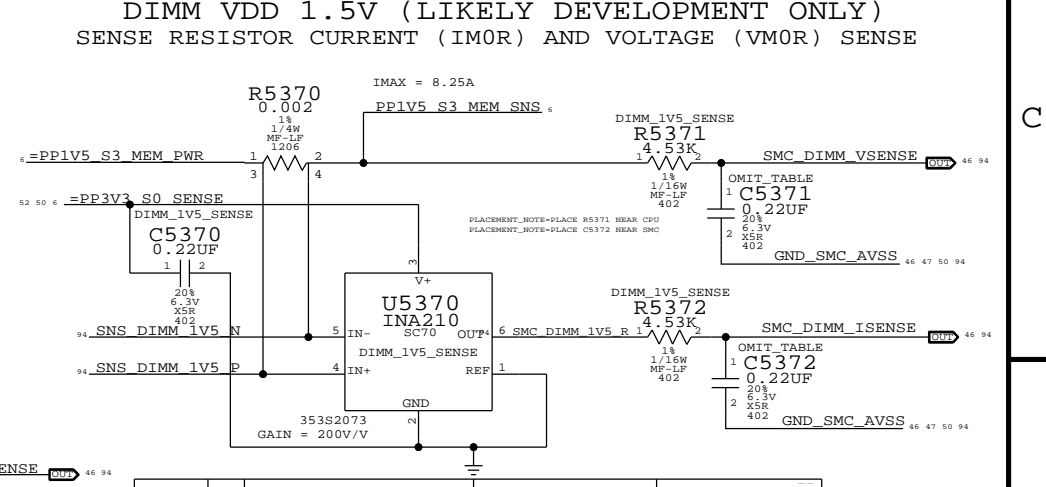
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP, 0.22UF, 402	C5311, C5312	CPU_VCCSA_SENSE
116S0004	2	RES, 0 OHM, 402	C5311, C5312	NO_CPU_VCCSA_SENSE

CRITICAL IMAX = 8.25A



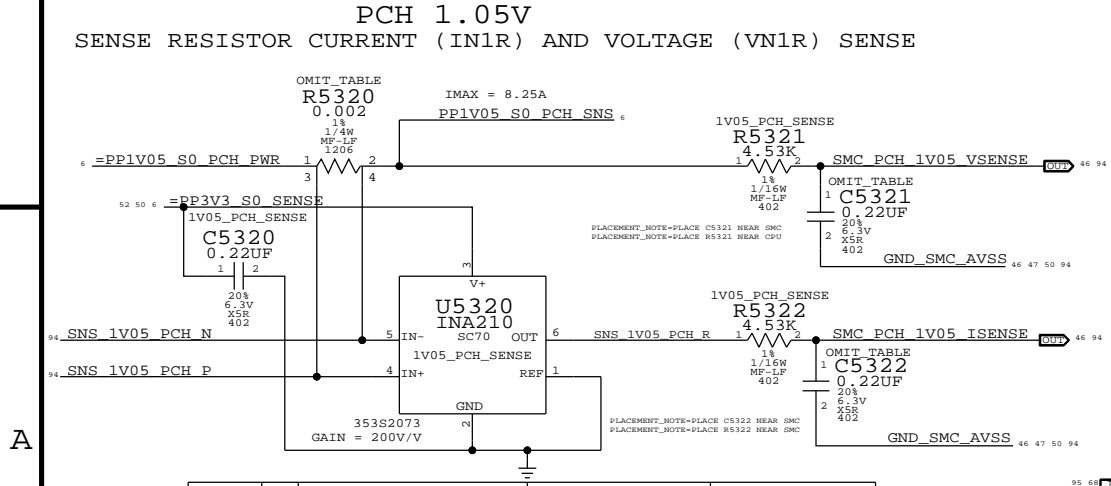
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP, 0.22UF, 402	C5340, C5342	VAXG
116S0004	2	RES, 0 OHM, 402	C5340, C5342	NO_VAXG

CRITICAL IMAX = 2.79V



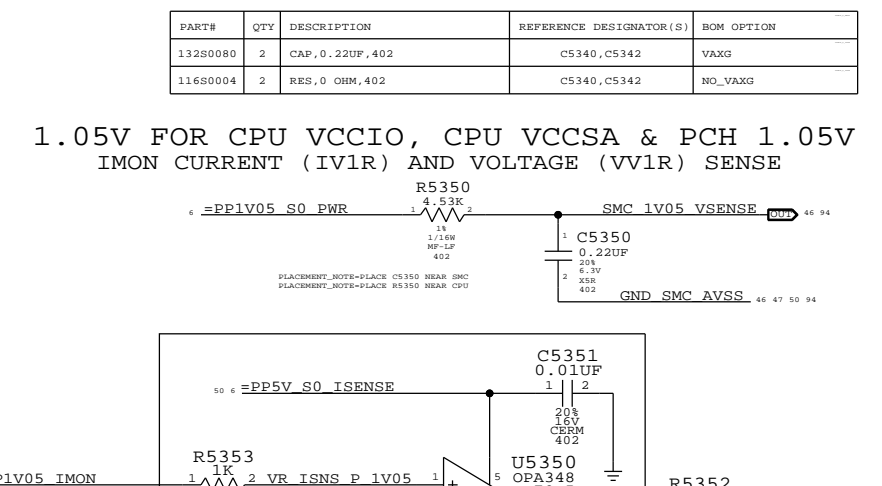
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP, 0.22UF, 402	C5371, C5372	DIMM_V5_SENSE
116S0004	2	RES, 0 OHM, 402	C5371, C5372	PRODUCTION

CRITICAL IMAX = 8.25A



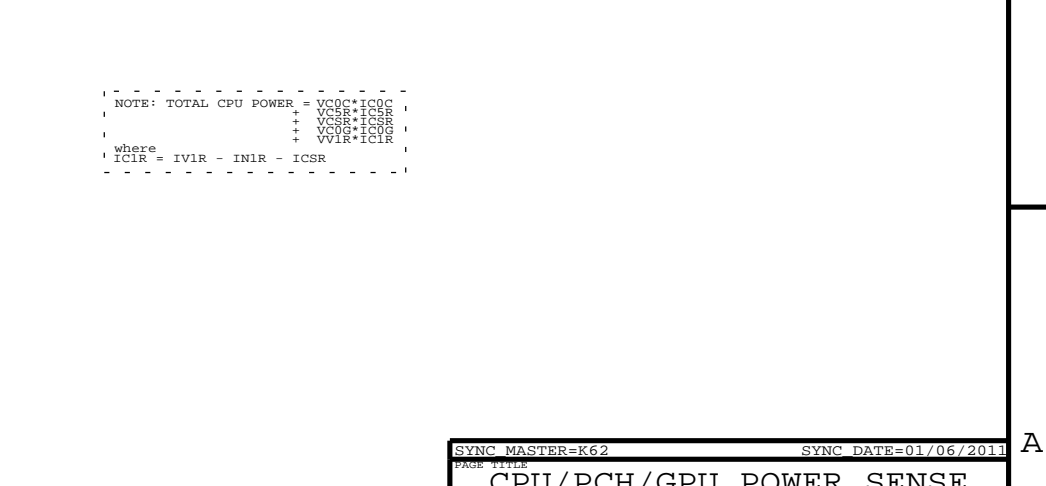
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5320	1V05_PCH_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP, 0.22UF, 402	C5321, C5322	1V05_PCH_SENSE
116S0004	2	RES, 0 OHM, 402	C5321, C5322	NO_1V05_PCH_SENSE

CRITICAL IMAX = 8.25A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP, 0.22UF, 402	C5351, C5352	1V05_PCH_SENSE
116S0004	2	RES, 0 OHM, 402	C5351, C5352	NO_1V05_PCH_SENSE

CRITICAL IMAX = 2.7V



CRITICAL IMAX = 2.7V

CRITICAL IMAX = 2.7V

SYNC MASTER=K62 SYNC DATE=01/06/2011

CPU/PCH/GPU POWER SENSE

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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PAGE: 53 OF 110 SHEET: 50 OF 98

D

D

C

C

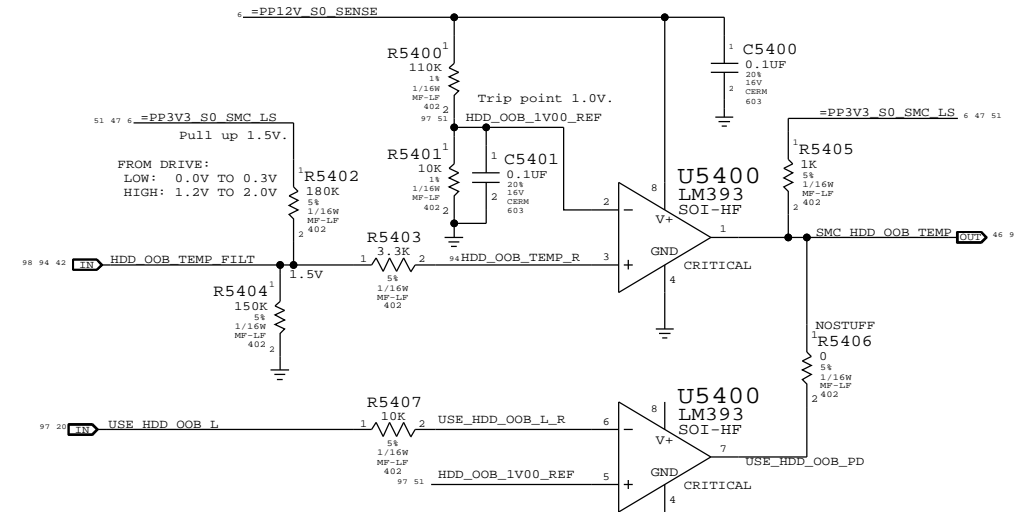
B

B

A

A

HDD OOB TEMPERATURE SENSING

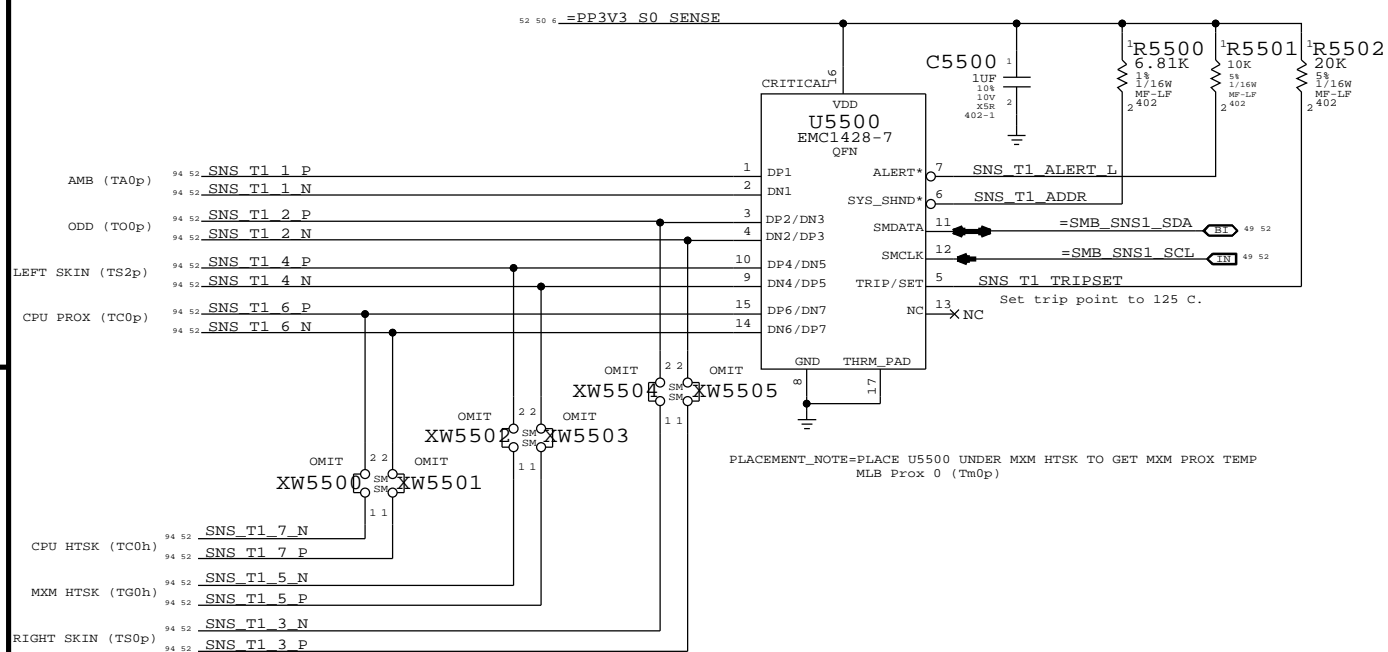


DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
 DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
 DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
 THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
 AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
 BOTH FUNCTIONS NOT USED.

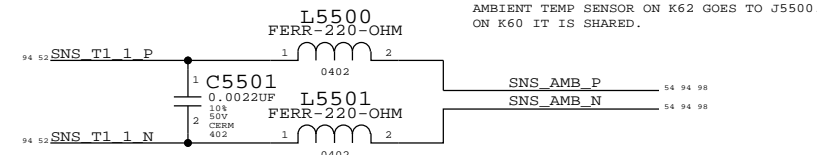
SYNC MASTER=K62		SYNC DATE=01/06/2011	
HDD OOB SENSE			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8115	D
		REVISION	
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SNS T1: PRODUCTION TEMP SENSOR IC

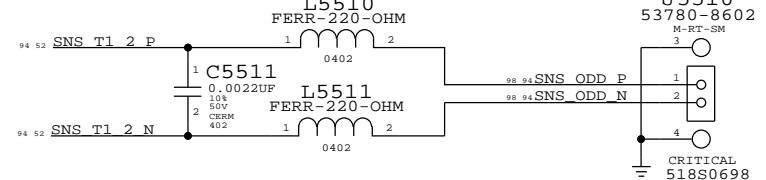


EMCL428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

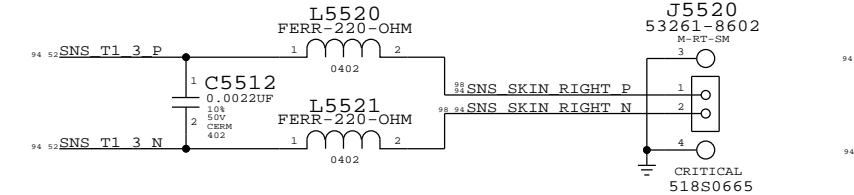
AMBIENT TEMP SENSOR



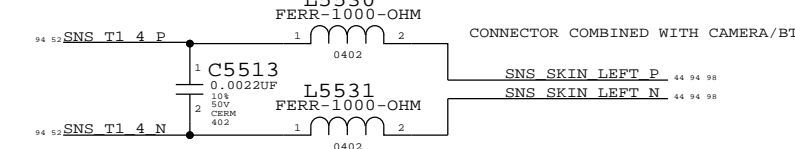
ODD TEMP SENSOR



RIGHT SKIN TEMP SENSOR

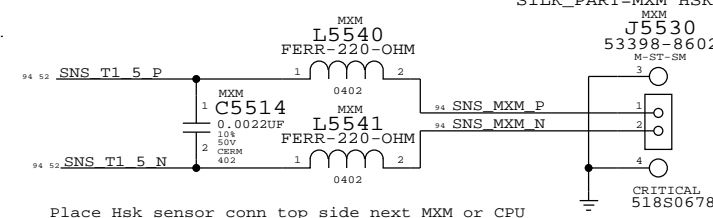


LEFT SKIN TEMP SENSOR

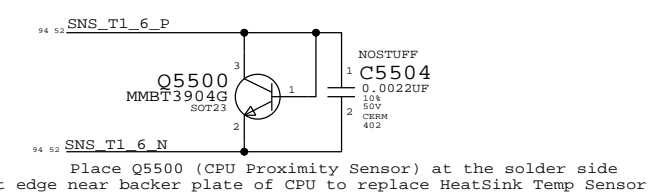


THIS PAGE DIFFERENT BETWEEN K60 AND K62.

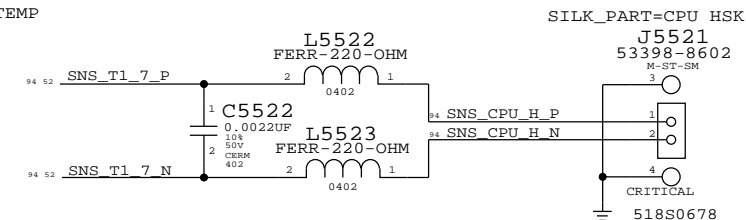
MXM HTSK TEMP SENSOR



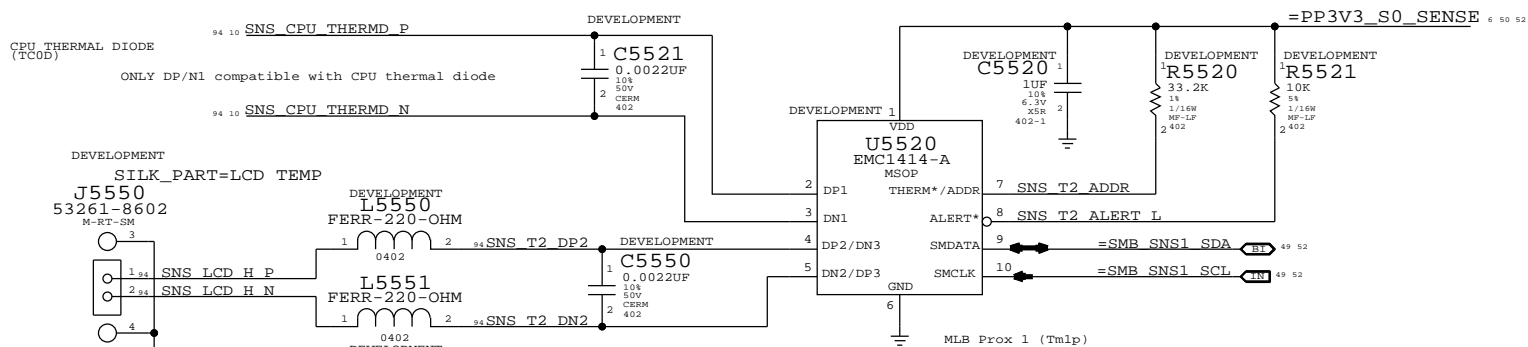
CPU PROXIMITY TEMP SENSOR



CPU HTSK TEMP SENSOR

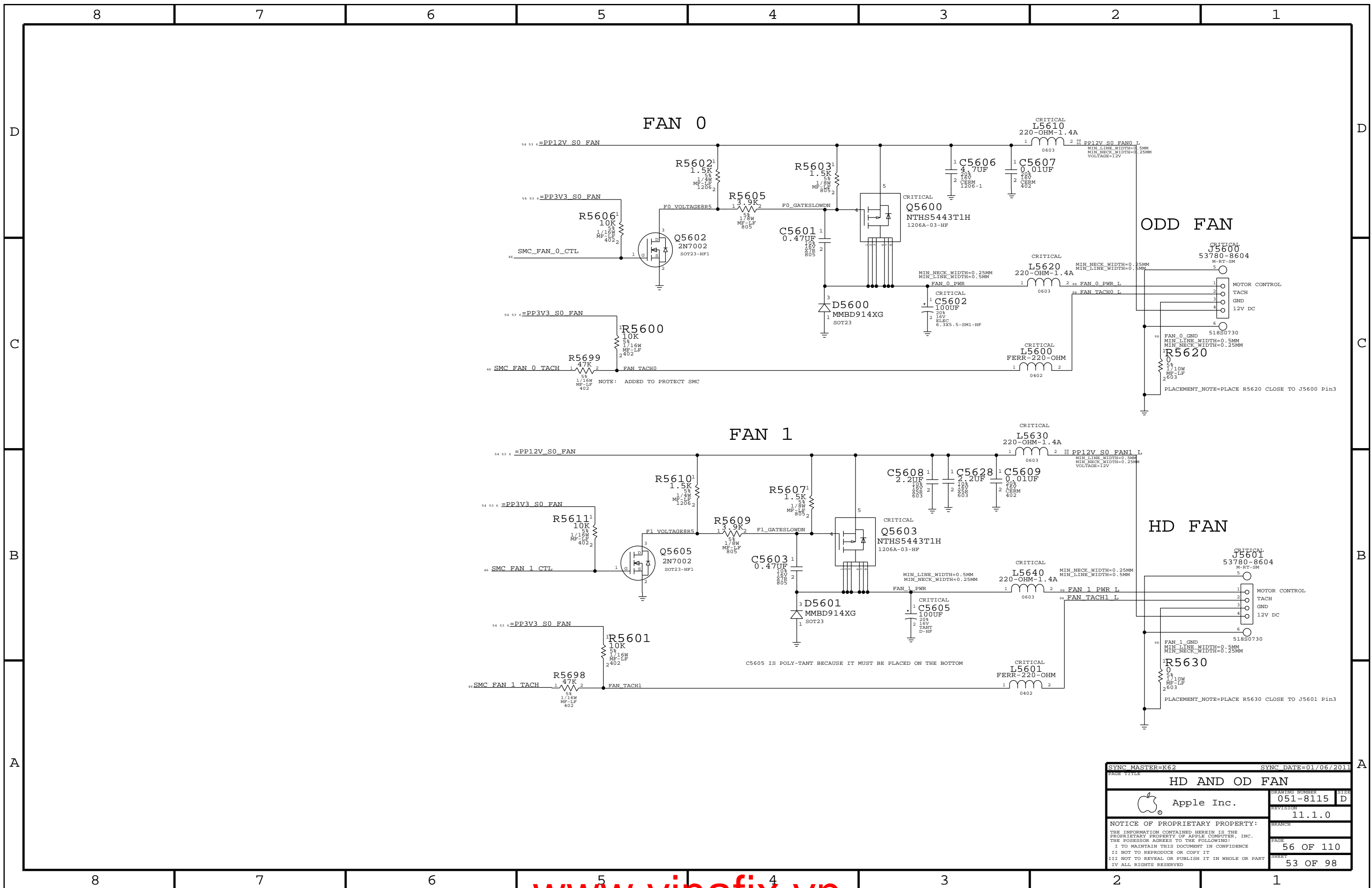


SNS T2: DEVELOPMENT TEMP SENSOR IC

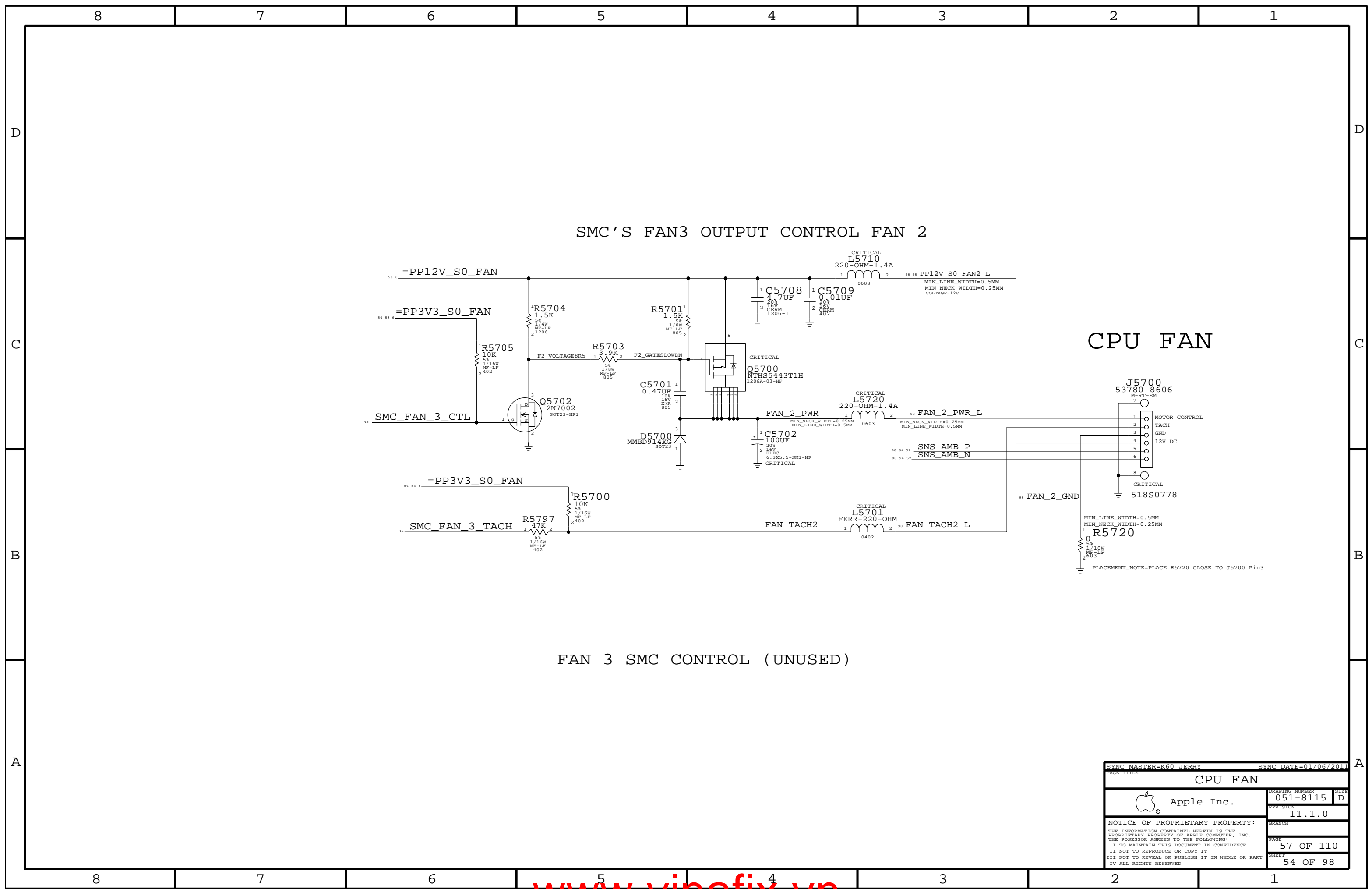


EMCL414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

PAGE TITLE		SYNC DATE=01/06/2011	
TEMP SENSORS			
Apple Inc.	DRAWING NUMBER	051-8115	SIZE D
	REVISION	11.1.0	
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SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE			
HD AND OD FAN			
		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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		PAGE	56 OF 110
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		SIZE	D

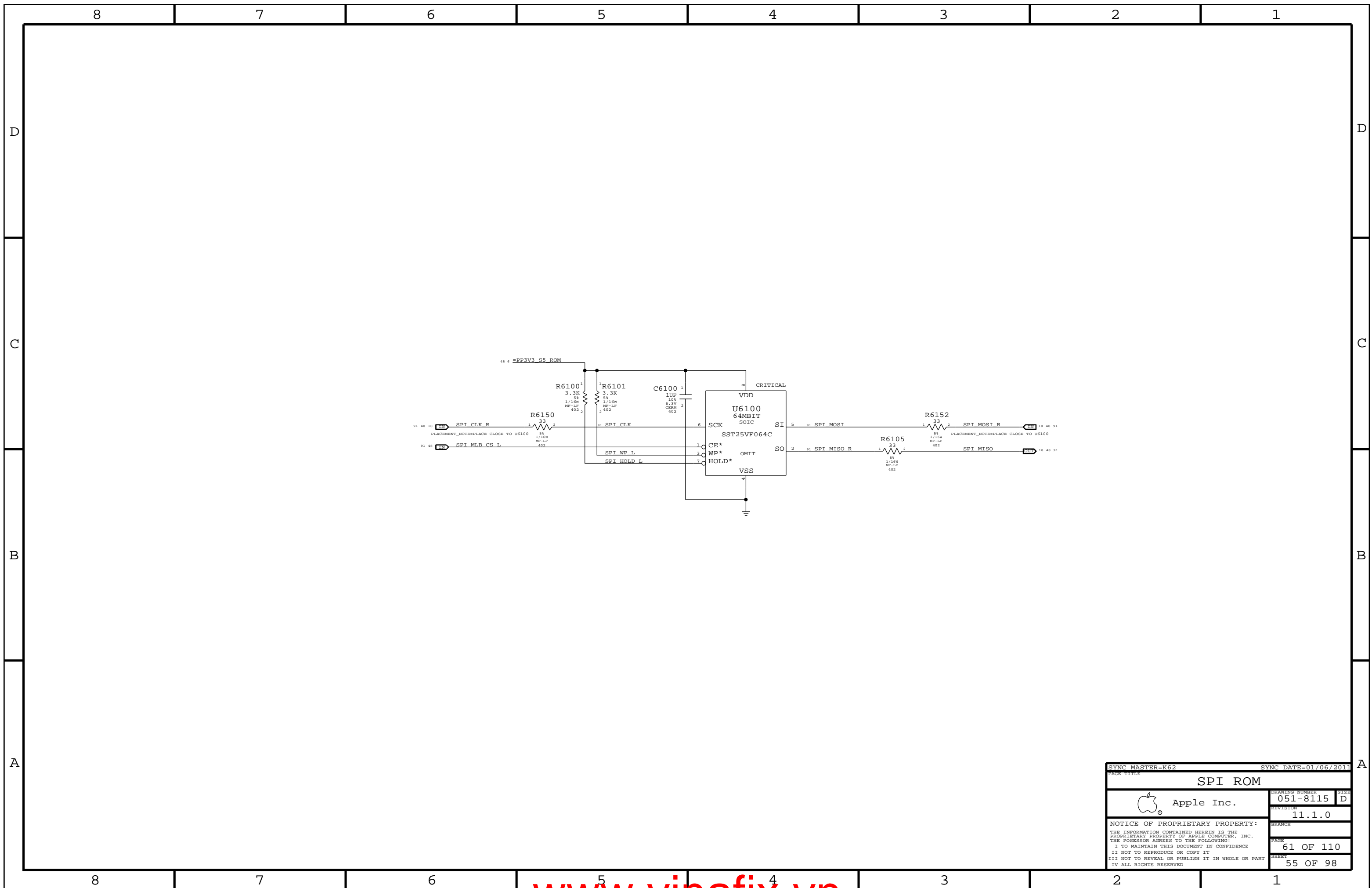


SMC'S FAN3 OUTPUT CONTROL FAN 2

CPU FAN

FAN 3 SMC CONTROL (UNUSED)

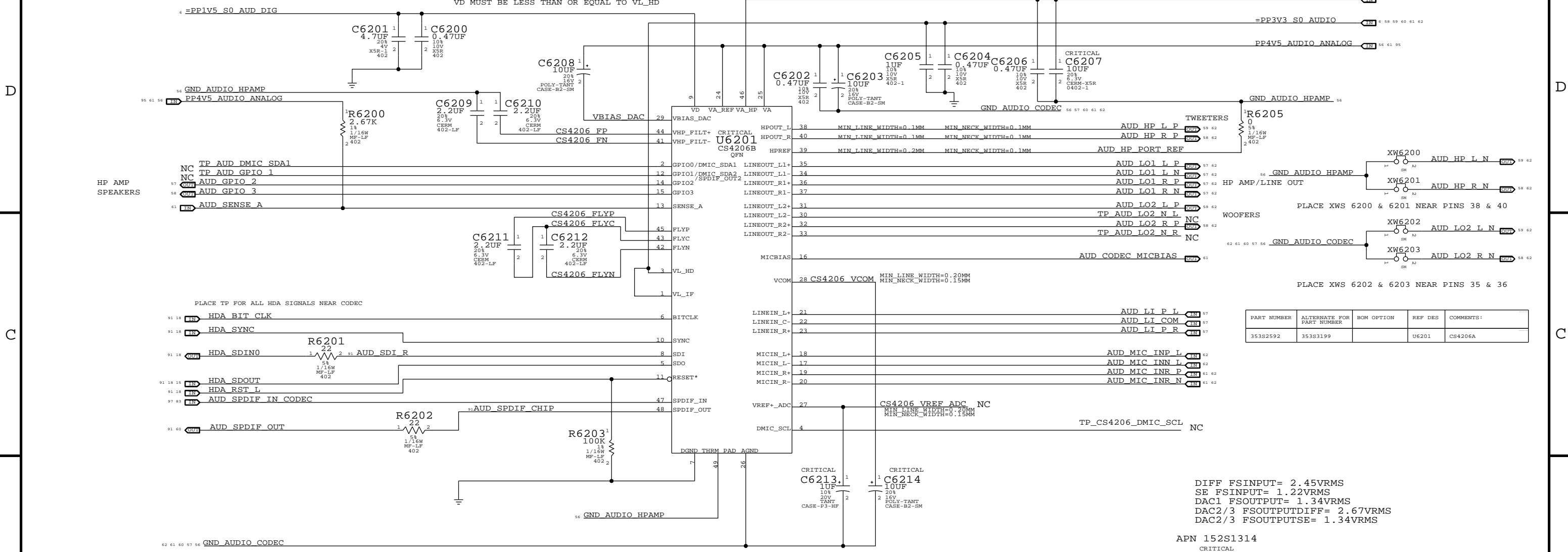
SYNC MASTER=K60_JERRY		SYNC DATE=01/06/2011	
PAGE TITLE CPU FAN			
DRAWING NUMBER 051-8115		SIZE D	
REVISION 11.1.0		BRANCH	
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SYNC_MASTER=K62		SYNC_DATE=01/06/2011	
PAGE TITLE			
SPI ROM			
		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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AUDIO CODEC

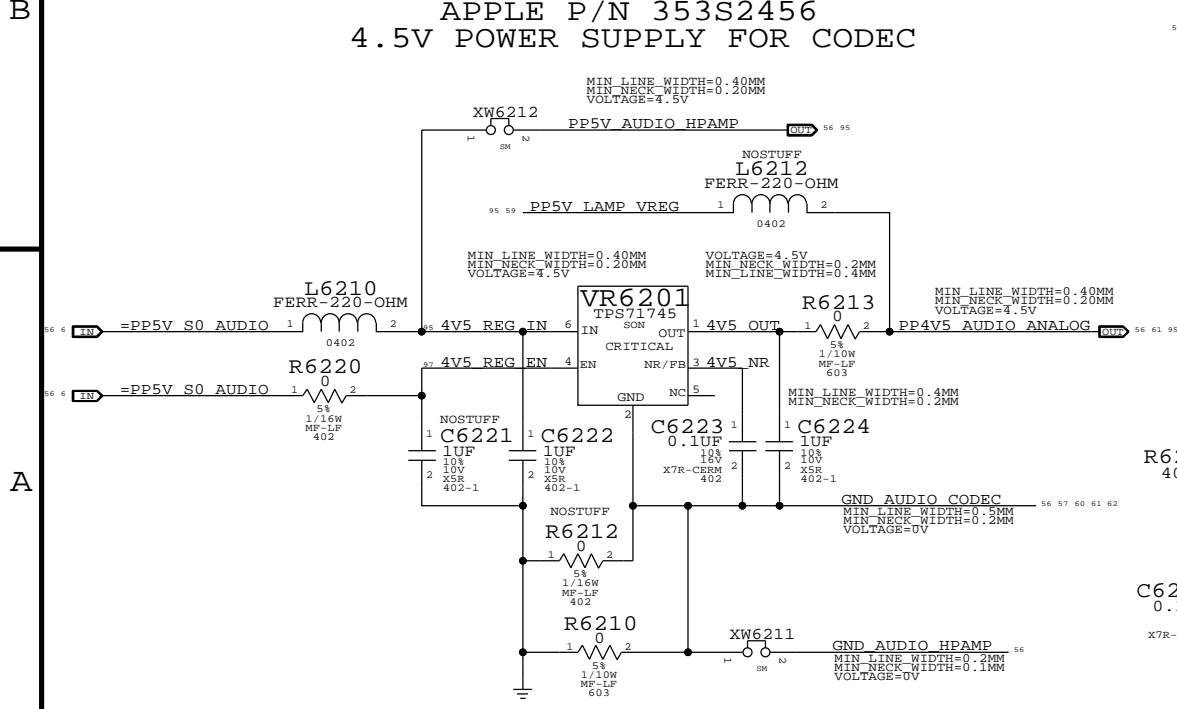
APPLE P/N 353S2592
PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE
VD MUST BE LESS THAN OR EQUAL TO VL_HD



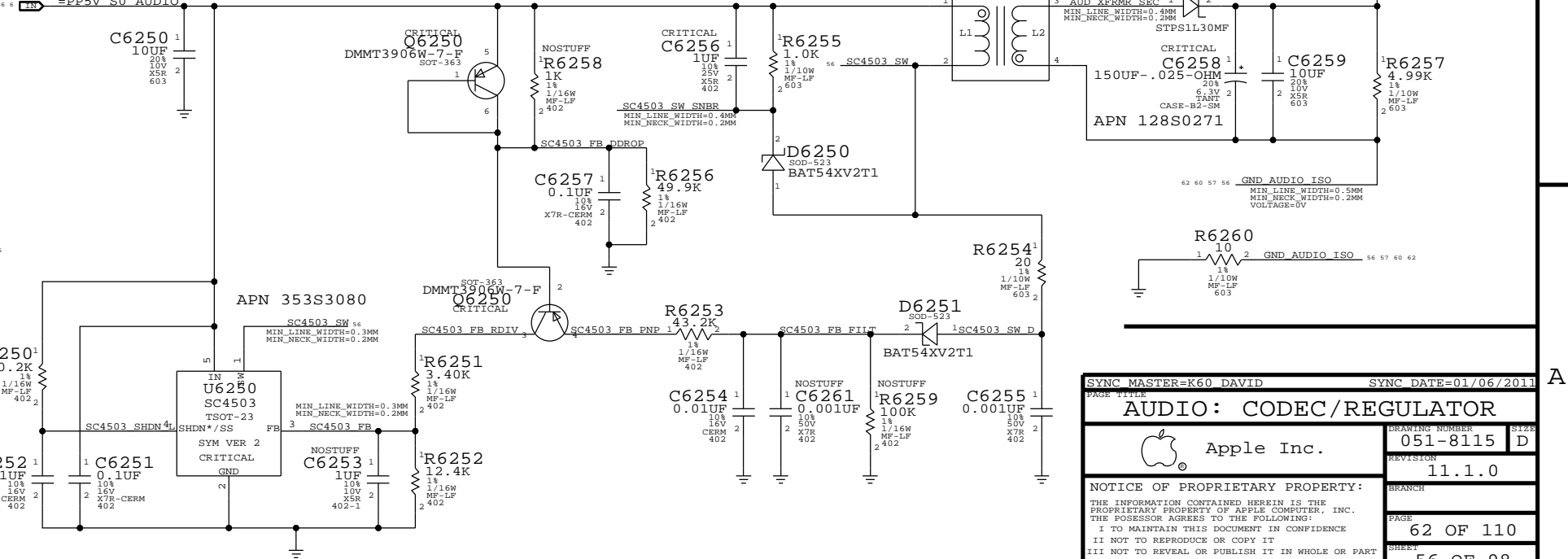
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S2592	353S3199		U6201	CS4206A

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

APPLE P/N 353S2456 4.5V POWER SUPPLY FOR CODEC



ISOLATED 5 V POWER SUPPLY FOR HP AMP



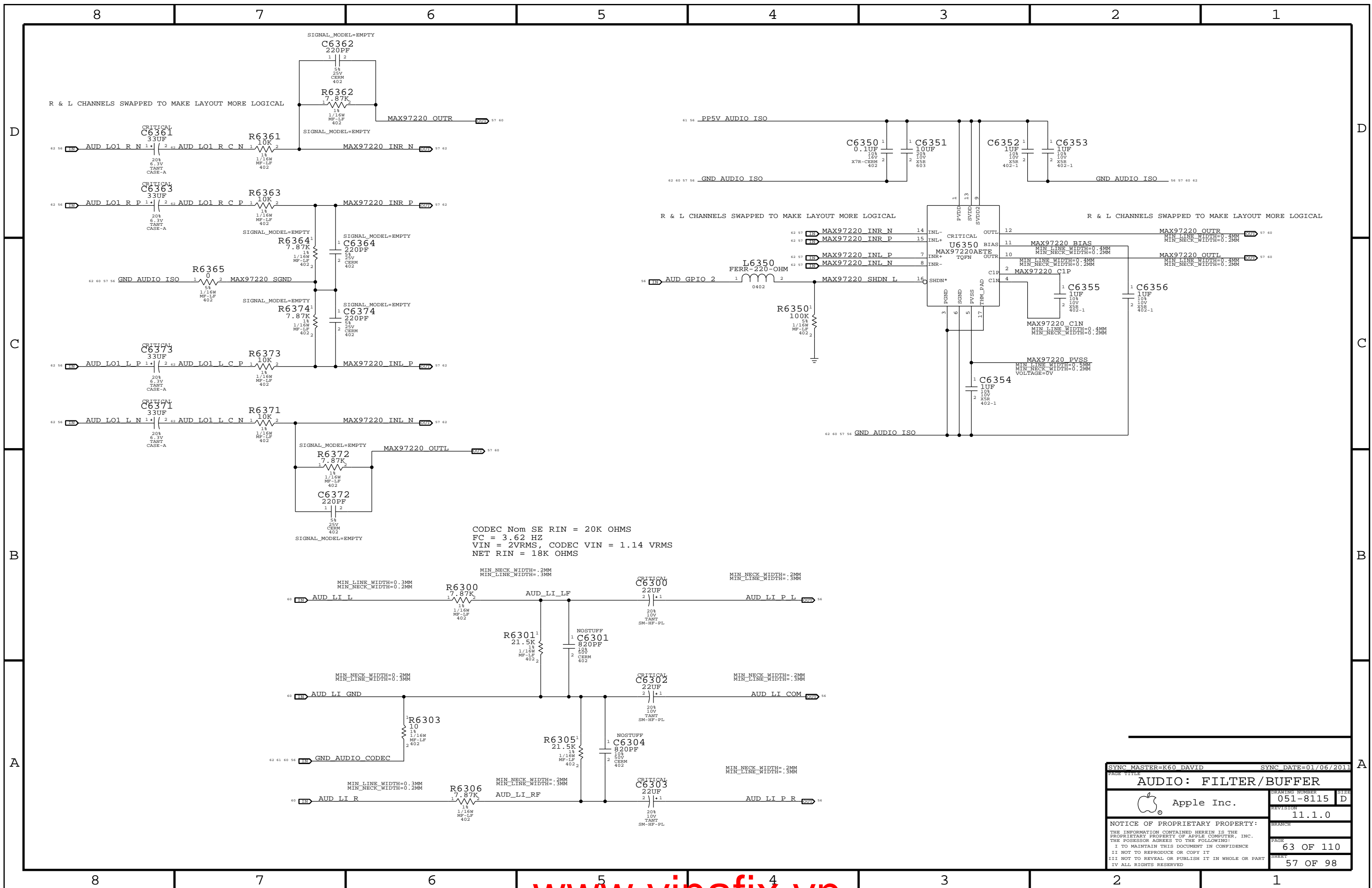
SYNC MASTER=K60 DAVID SYNC DATE=01/06/2011

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
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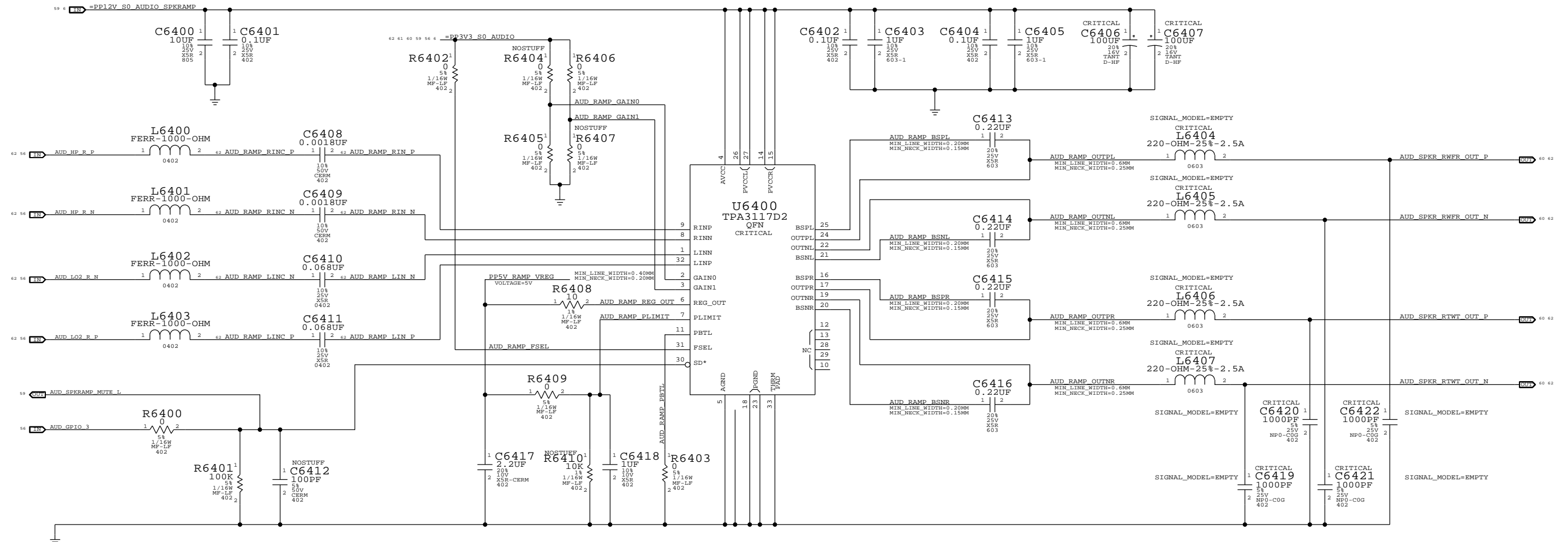


CODEC Nom SE RIN = 20K OHMS
 FC = 3.62 HZ
 VIN = 2VRMS, CODEC VIN = 1.14 VRMS
 NET RIN = 18K OHMS

PAGE TITLE		SYNC DATE=01/06/2011	
AUDIO: FILTER/BUFFER			
Apple Inc.	DRAWING NUMBER	051-8115	SIZE D
	REVISION	11.1.0	
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

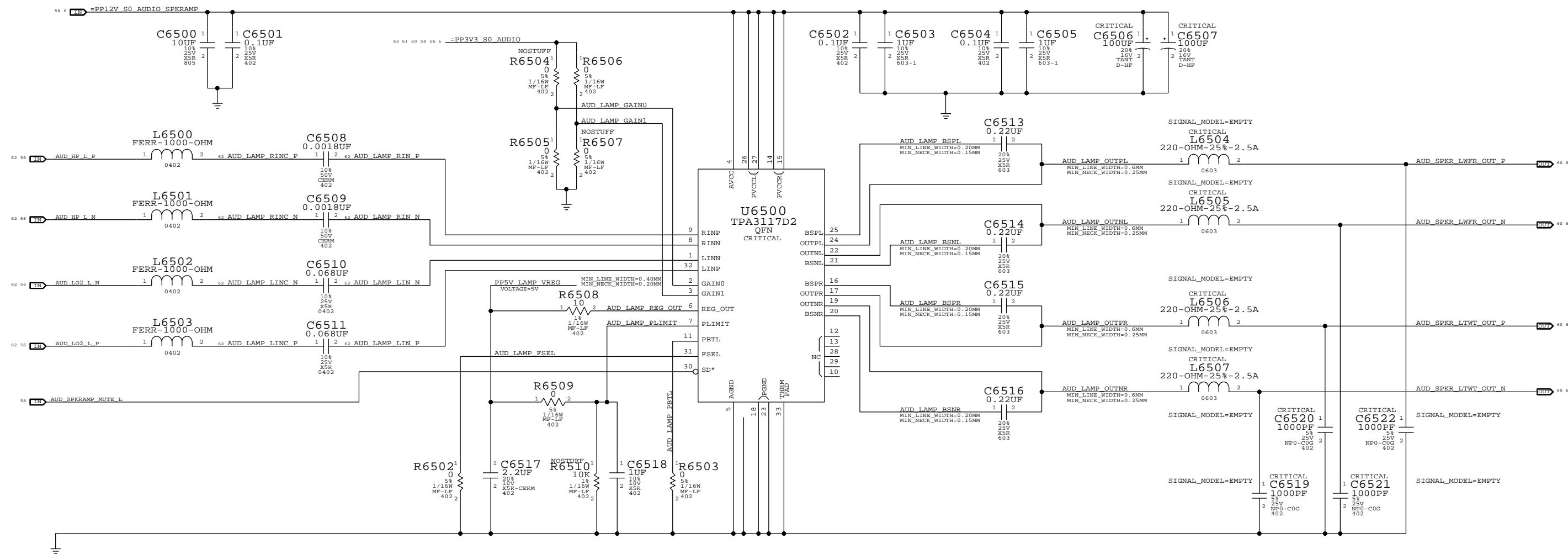
R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC MASTER=K60 DAVID		SYNC DATE=01/06/2011	
AUDIO: SPEAKER AMP_1			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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		PAGE	64 OF 110
		SHEET	58 OF 98
		SIZE	D

LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC MASTER=K60 DAVID		SYNC DATE=01/06/2011	
AUDIO: SPEAKER AMP			
Apple Inc.		DRAWING NUMBER	051-8115
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		PAGE	65 OF 110
		SHEET	59 OF 98

8

7

6

5

4

3

2

1

INTERNAL MIC CON

APPLE P/N 518S0677

SPEAKER CABLE CONNECTORS

APPLE P/N 518S0748
APPLE P/N 518S0656

PROPERTIES FOR ALL SPKR NETS

CRITICAL

PROPERTIES FOR ALL SPKR NETS

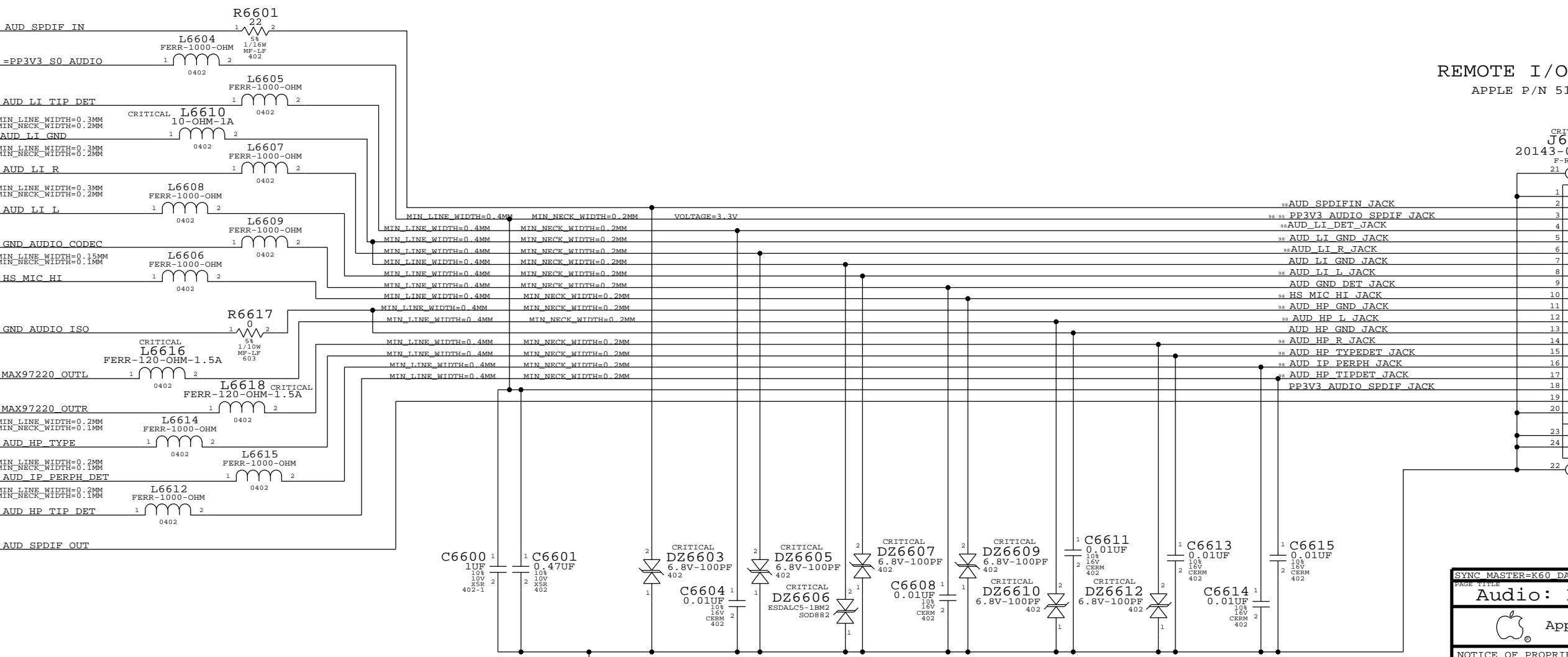
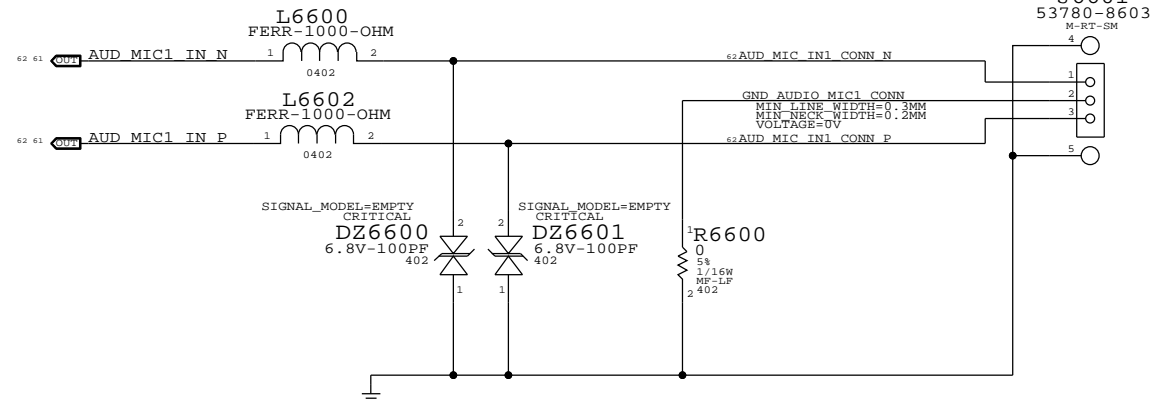
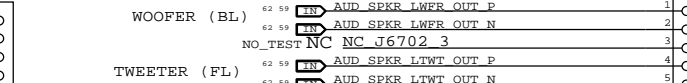
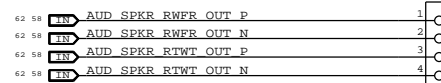
CRITICAL

J6602
78048-0473
M-RT-SM

J6603
78048-0573
M-RT-SM

WOOFER (BR)
TWEETER (FR)

WOOFER (BL)
TWEETER (FL)



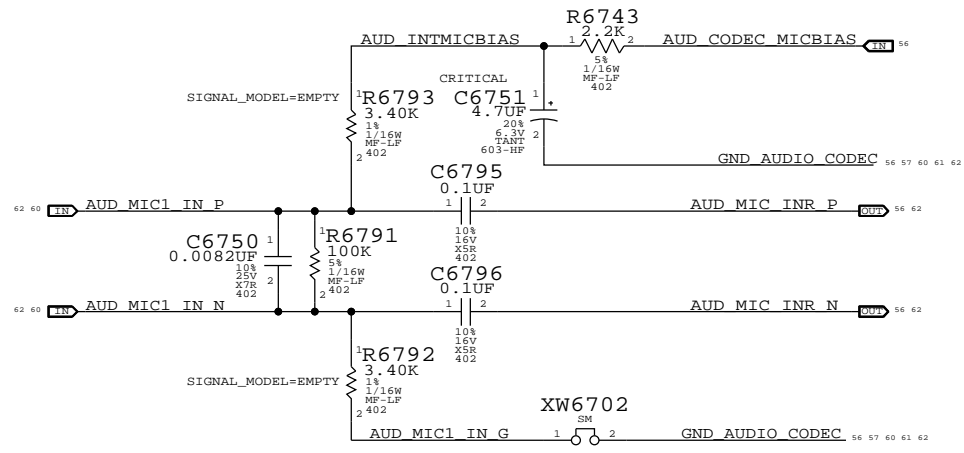
REMOTE I/O CONNECTOR

APPLE P/N 518S0723

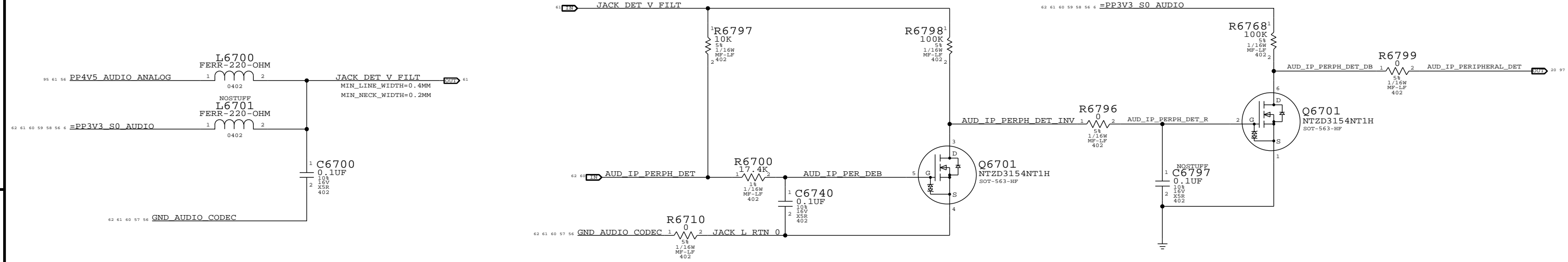
J6600
20143-020E-20F
F-RT-SM

PAGE TITLE		SYNC DATE=01/06/2011	
Audio: MLB to I/O Conn.		DRAWING NUMBER	051-8115
Apple Inc.		REVISION	11.1.0
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Internal Microphone Impedance Matching



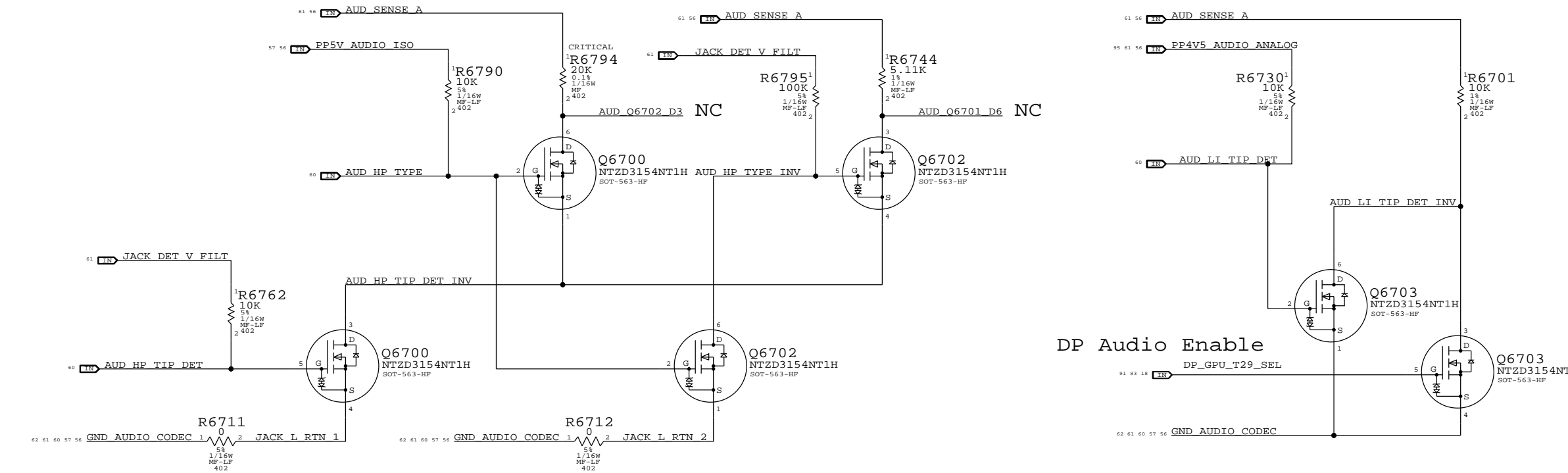
IPHS HS Detect Debounce CKT



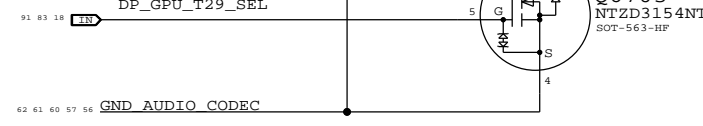
Digital Out (DETECT B)

Headphone Out (DETECT D)

LI Insert Detect (DETECT C)



DP Audio Enable



SYNC MASTER=K60 DAVID		SYNC DATE=11/24/2010	
PAGE TITLE AUDIO: Detects/Grounding			
DRAWING NUMBER 051-8115		SIZE D	
REVISION 11.1.0		BRANCH	
PAGE 67 OF 110		SHEET 61 OF 98	
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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640

CODEC OUTPUT SIGNAL PATHS					
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

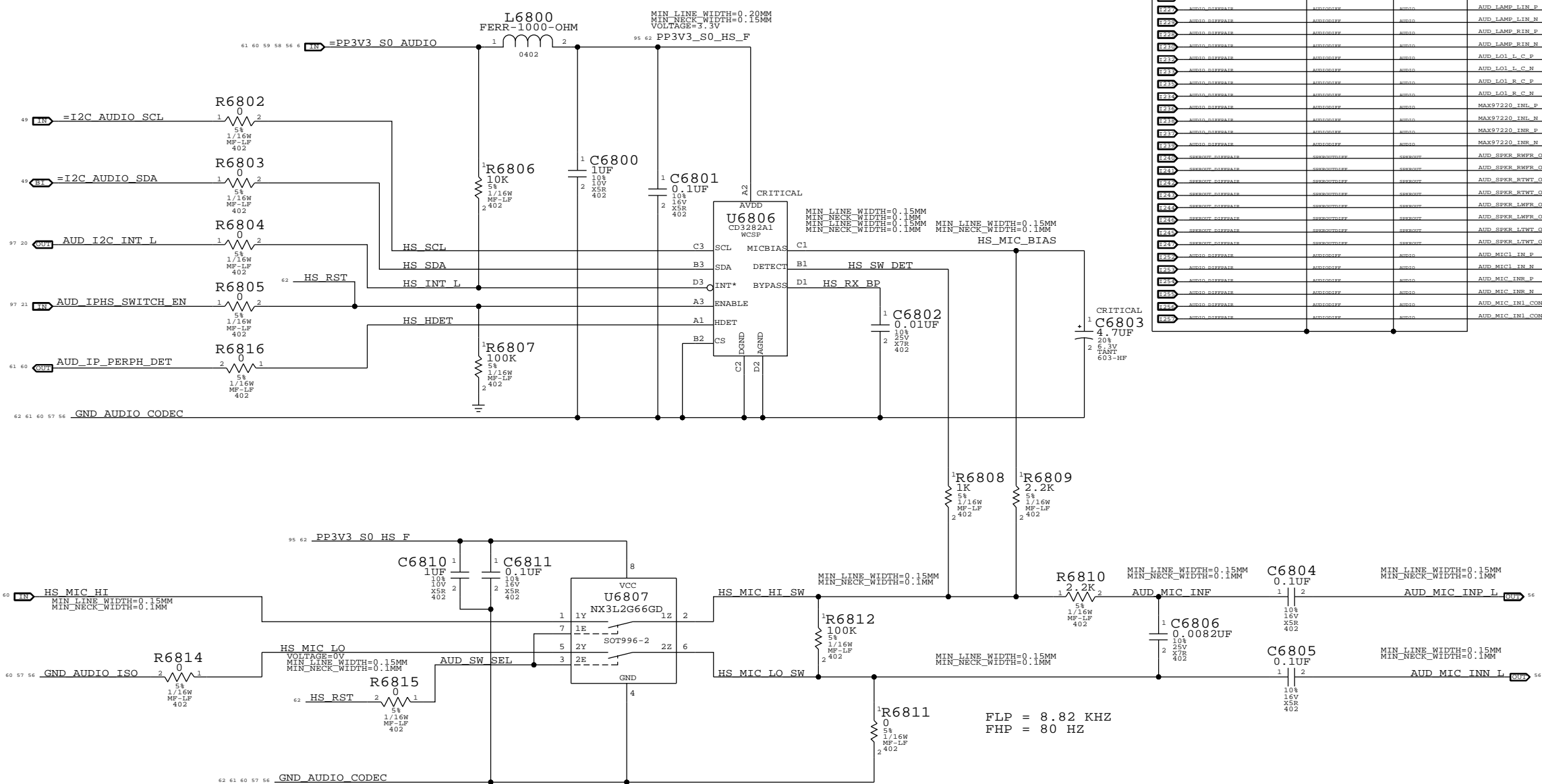
CODEC INPUT SIGNAL PATHS					
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT	
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)	
SPDIF IN	0X07 (7)	0x0F (15)	N/A	N/A	
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A	
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (RCVR INT)	COUGAR POINT GPIO 3 (PERIPH DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIODIFF	*	0.1 MM	?
SPKROUTDIFF	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

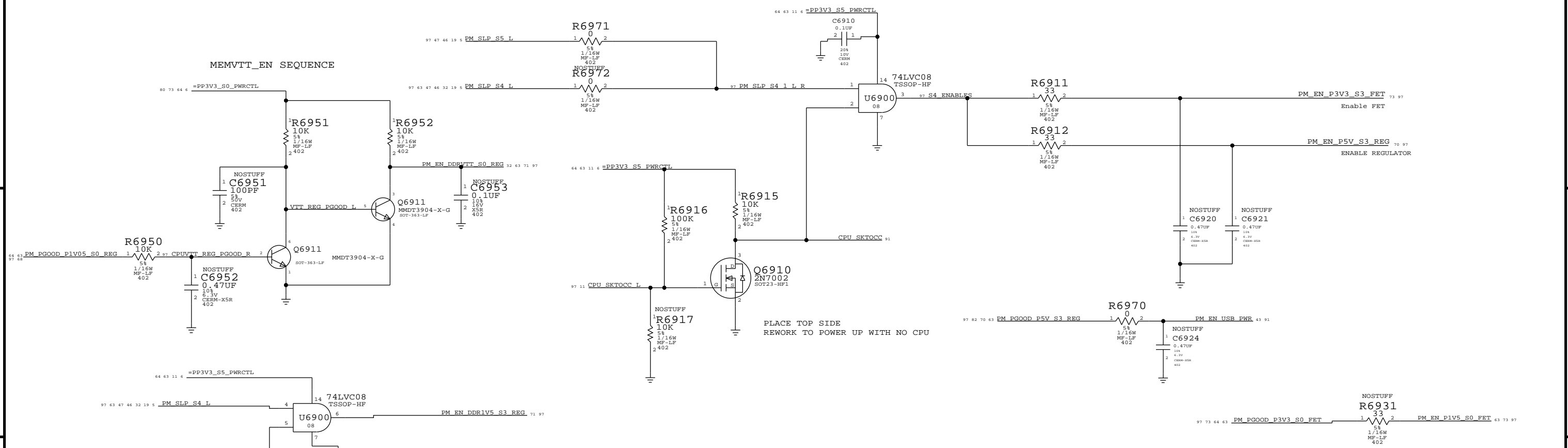
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
DIFF	AUDIODIFF	AUDIODIFF	AUD_HP_L_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_HP_L_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_HP_R_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_HP_R_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_L_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_L_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_R_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_R_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO2_L_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO2_L_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO2_R_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO2_R_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_LINC_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_LINC_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_RINC_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_RINC_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_LIN_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_LIN_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_RIN_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_RAMP_RIN_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_LINC_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_LINC_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_RINC_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_RINC_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_LIN_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_LIN_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_RIN_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LAMP_RIN_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_L_C_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_L_C_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_R_C_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_LO1_R_C_N
DIFF	AUDIODIFF	AUDIODIFF	MAX97220_INL_P
DIFF	AUDIODIFF	AUDIODIFF	MAX97220_INL_N
DIFF	AUDIODIFF	AUDIODIFF	MAX97220_INR_P
DIFF	AUDIODIFF	AUDIODIFF	MAX97220_INR_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_RWFR_OUT_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_RWFR_OUT_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_RTWT_OUT_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_RTWT_OUT_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_LWFR_OUT_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_LWFR_OUT_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_LTWT_OUT_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_SPKR_LTWT_OUT_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_MIC1_IN_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_MIC1_IN_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_MIC_INR_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_MIC_INR_N
DIFF	AUDIODIFF	AUDIODIFF	AUD_MIC_IN1_CONN_P
DIFF	AUDIODIFF	AUDIODIFF	AUD_MIC_IN1_CONN_N



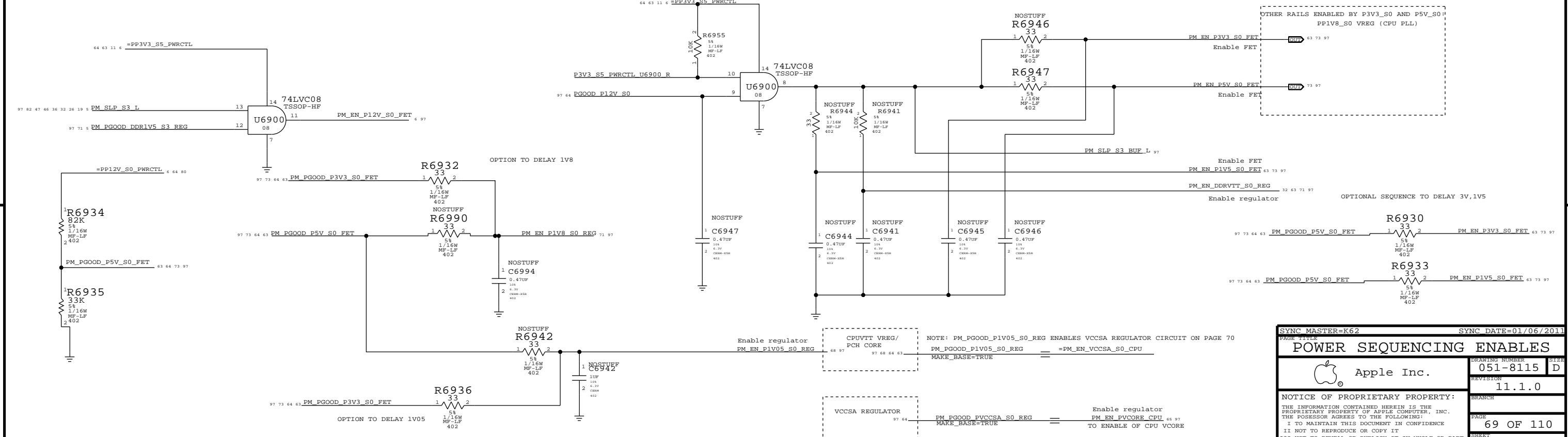
FLP = 8.82 KHZ
FHP = 80 HZ

PAGE TITLE		SYNC MASTER=K60 DAVID		SYNC DATE=01/06/2011	
AUDIO: Mikey			DRAWING NUMBER	051-8115	SIZE
Apple Inc.			REVISION	11.1.0	
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			PAGE	68 OF 110	
			SHEET	62 OF 98	

SLP_S4 ENABLES

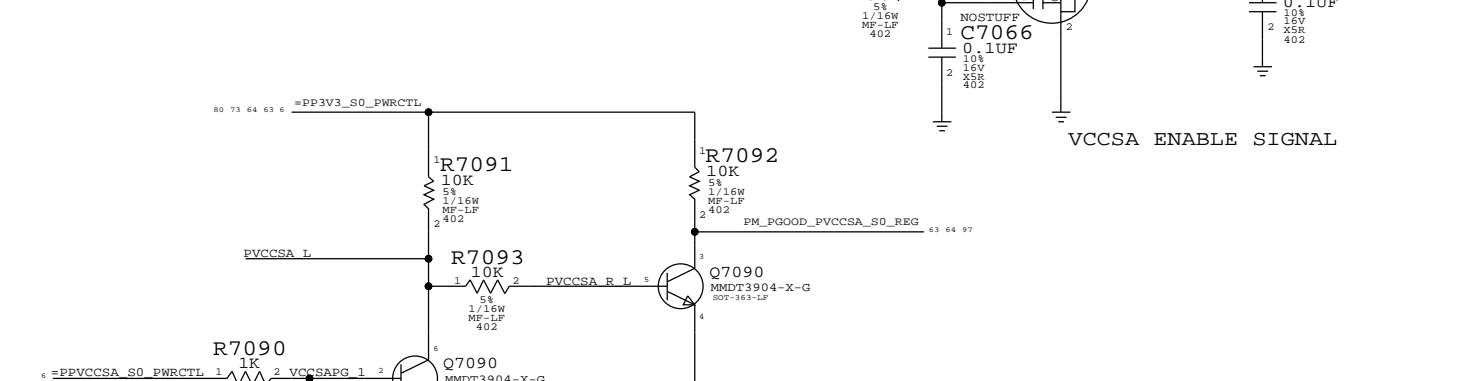
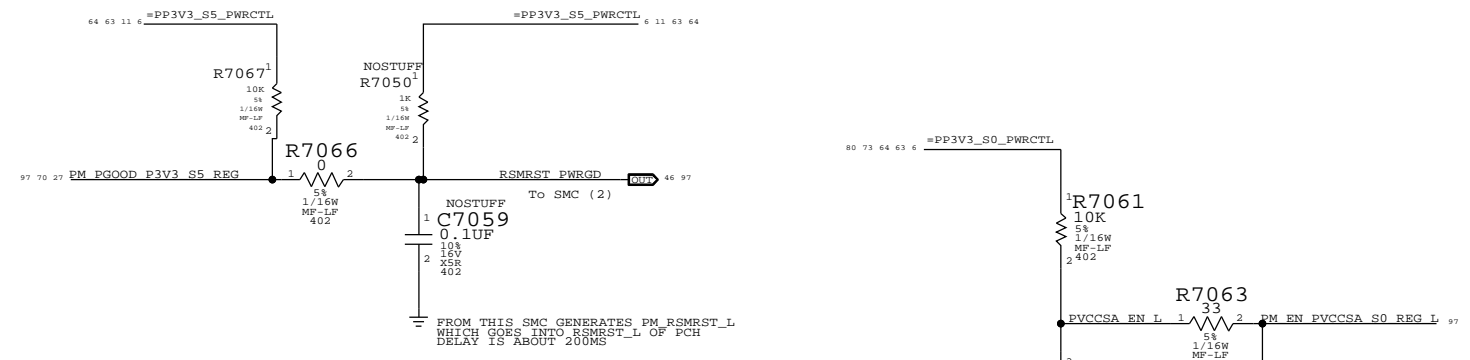
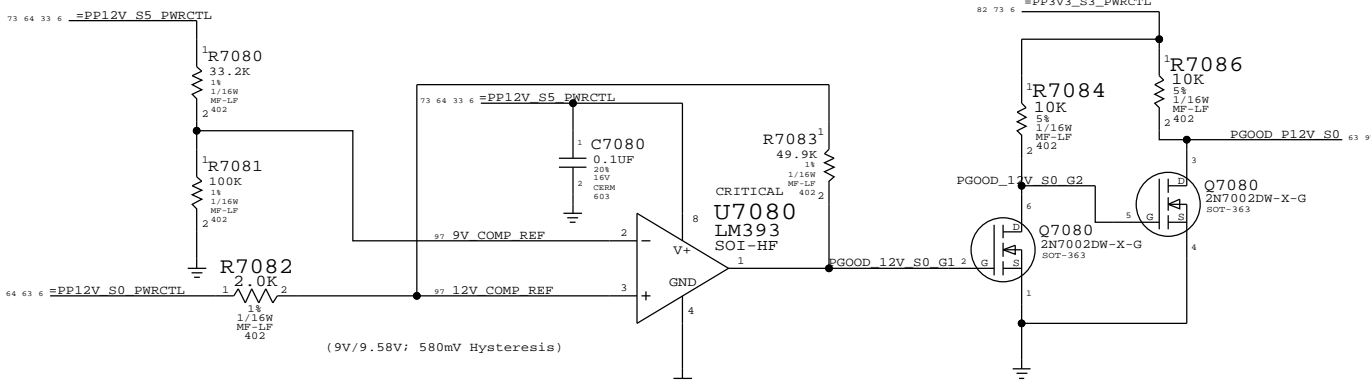
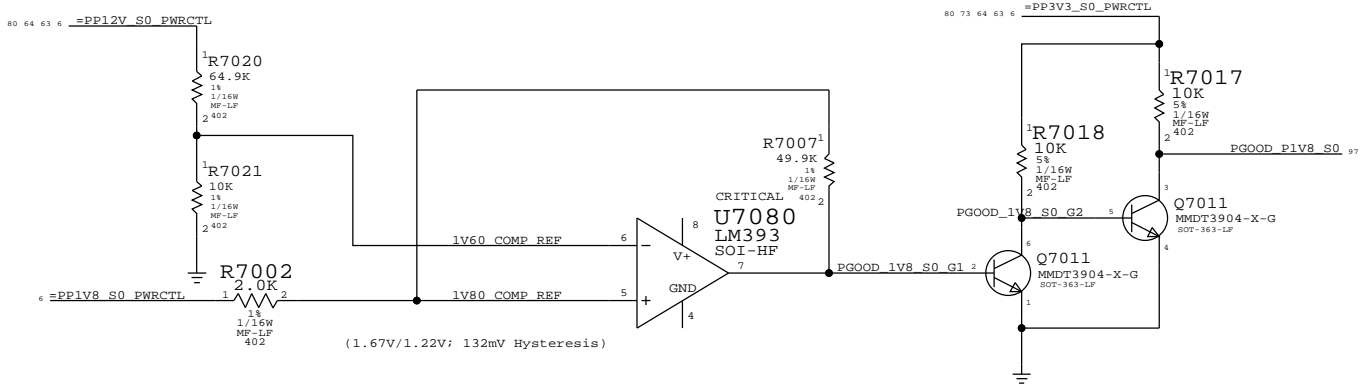


SLP_S3 ENABLES

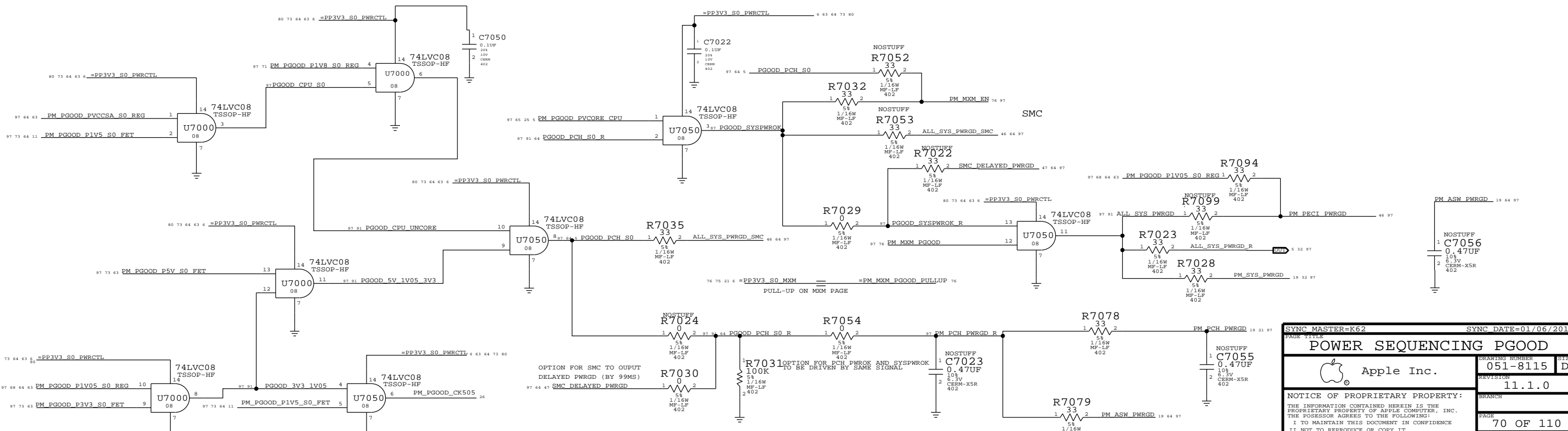


SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE POWER SEQUENCING ENABLES			
Apple Inc.		DRAWING NUMBER 051-8115	SIZE D
		REVISION 11.1.0	
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PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0



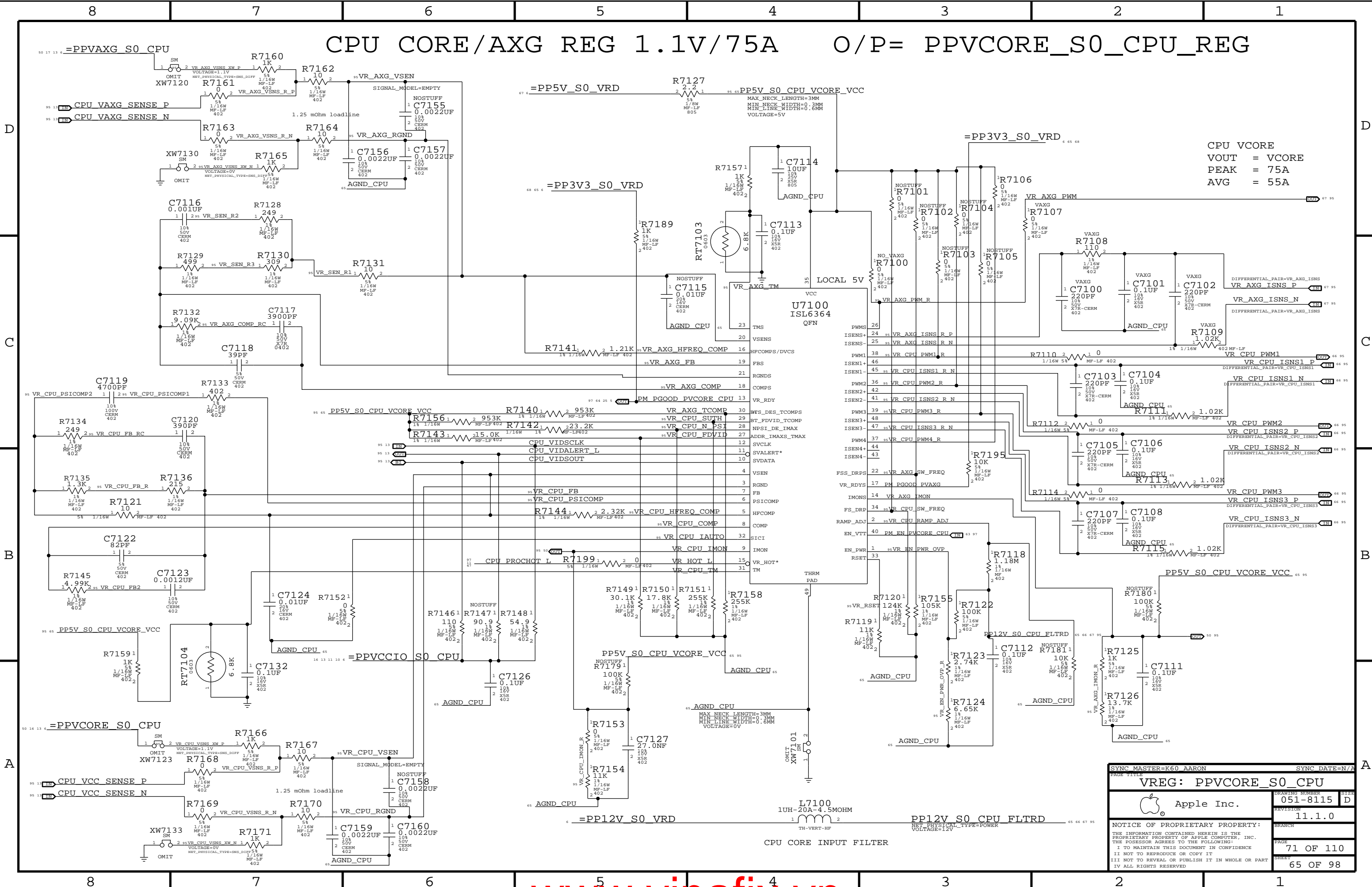
S0 RAILS PGOOD



ALL_SYS_PWRGD CIRCUIT

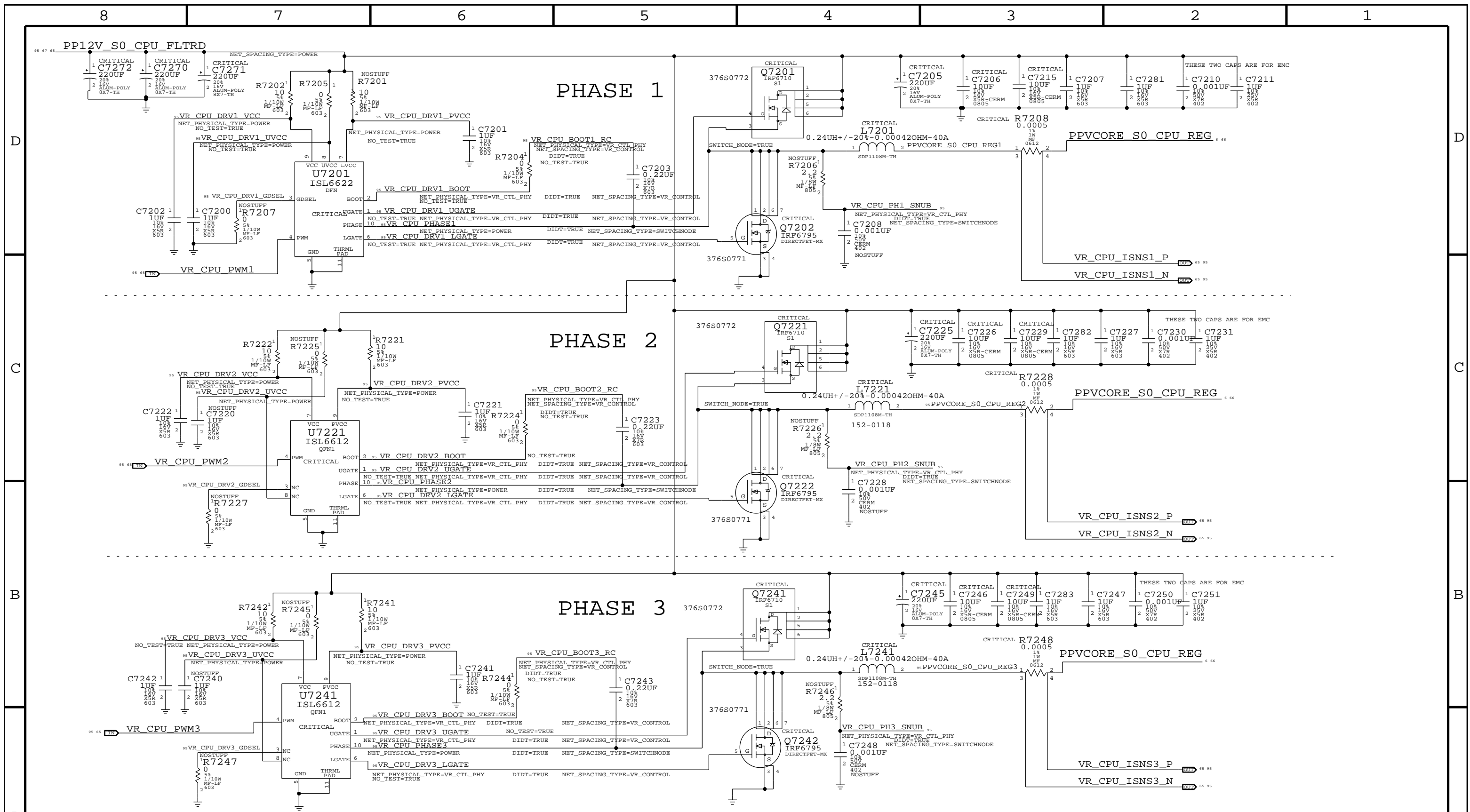
PAGE TITLE		PAGE NUMBER		PAGE SIZE	
POWER SEQUENCING PGOOD		051-8115		D	
Apple Inc.		REVISION		11.1.0	
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CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG

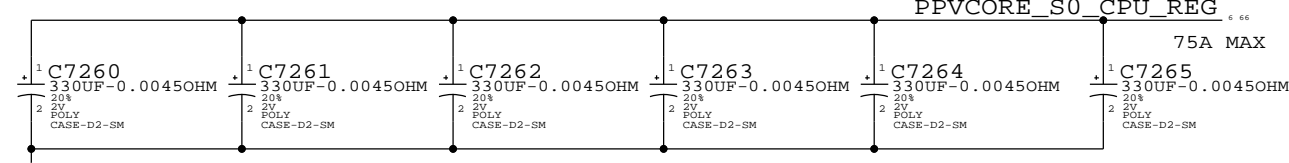


CPU VCORE
 VOUT = VCORE
 PEAK = 75A
 AVG = 55A

SYNC MASTER=K60 AARON		SYNC DATE=N/A	
VREG: PPVCORE_S0_CPU			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8115	D
		REVISION	
		11.1.0	
		BRANCH	
		PAGE	
		71 OF 110	
		SHEET	
		65 OF 98	
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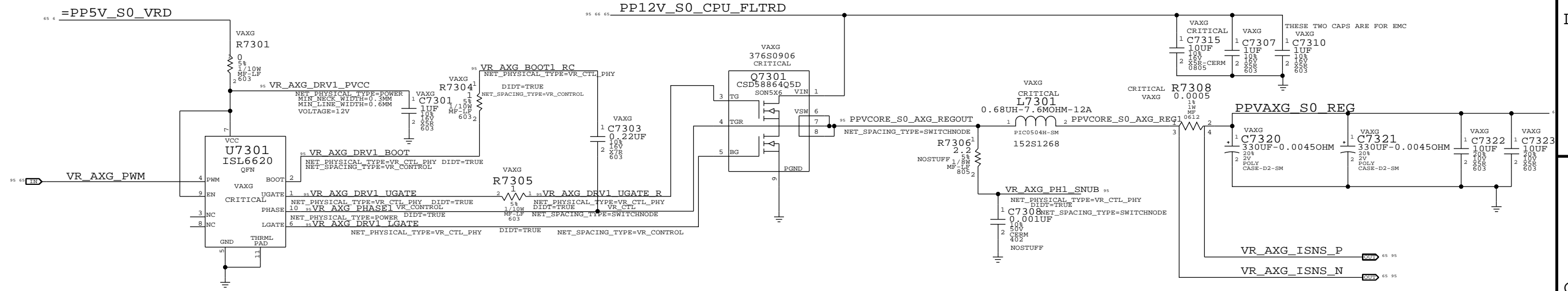


OUTPUT BULK DECOUPLING: 128S0209



SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE			
VREG: CPU CORE - PHASES 1-3			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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AXG PHASE (MAX 15A)



SYNC MASTER=K60 AARON		SYNC DATE=N/A	
PAGE TITLE VREG:AXG PHASE/CORE - CAPS			
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	REVISION	11.1.0	
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			PAGE 73 OF 110
			SHEET 67 OF 98

1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG

8 7 6 5 4 3 2 1

D

D

C

C

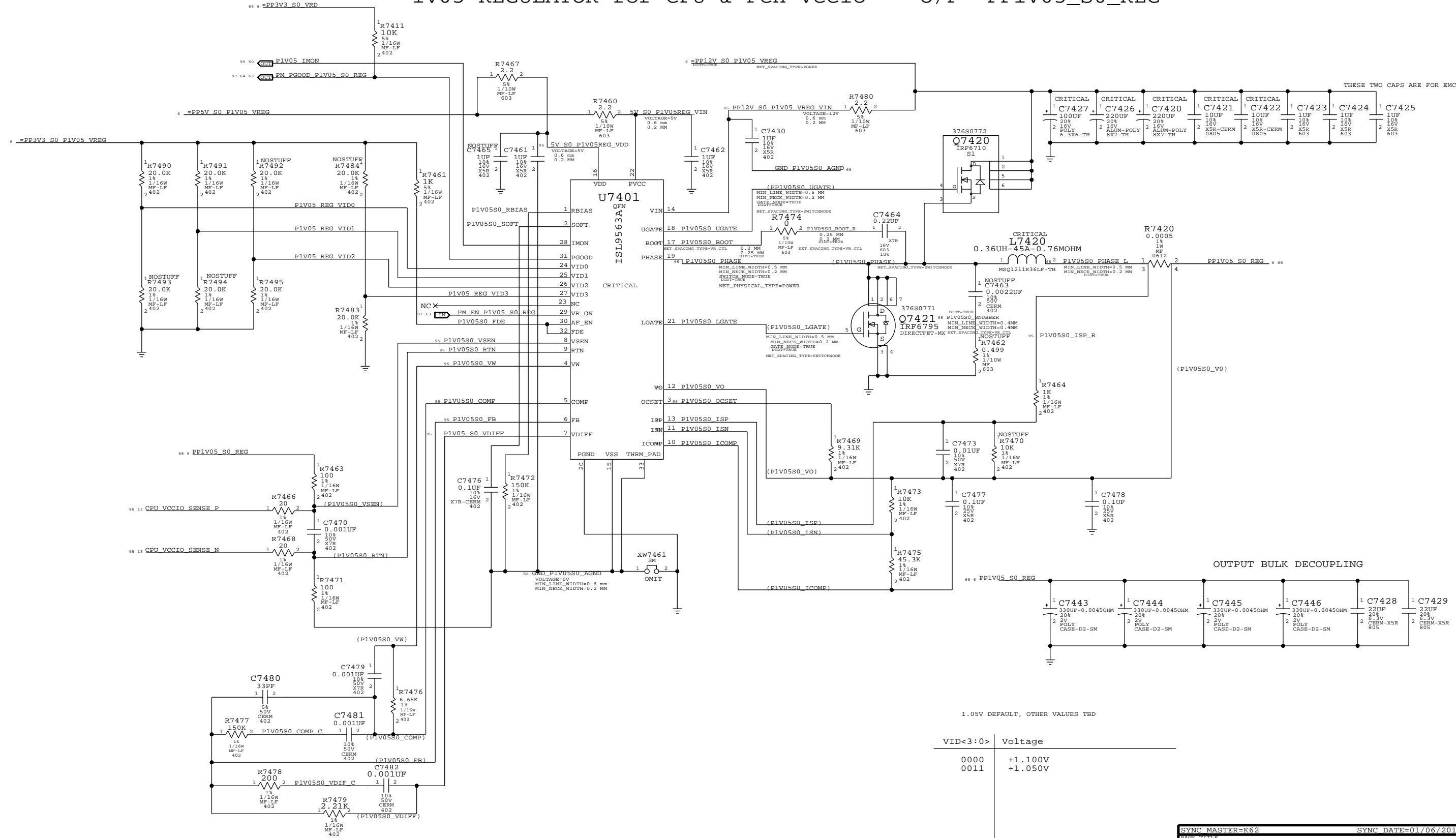
B

B

A

A

8 7 6 5 4 3 2 1

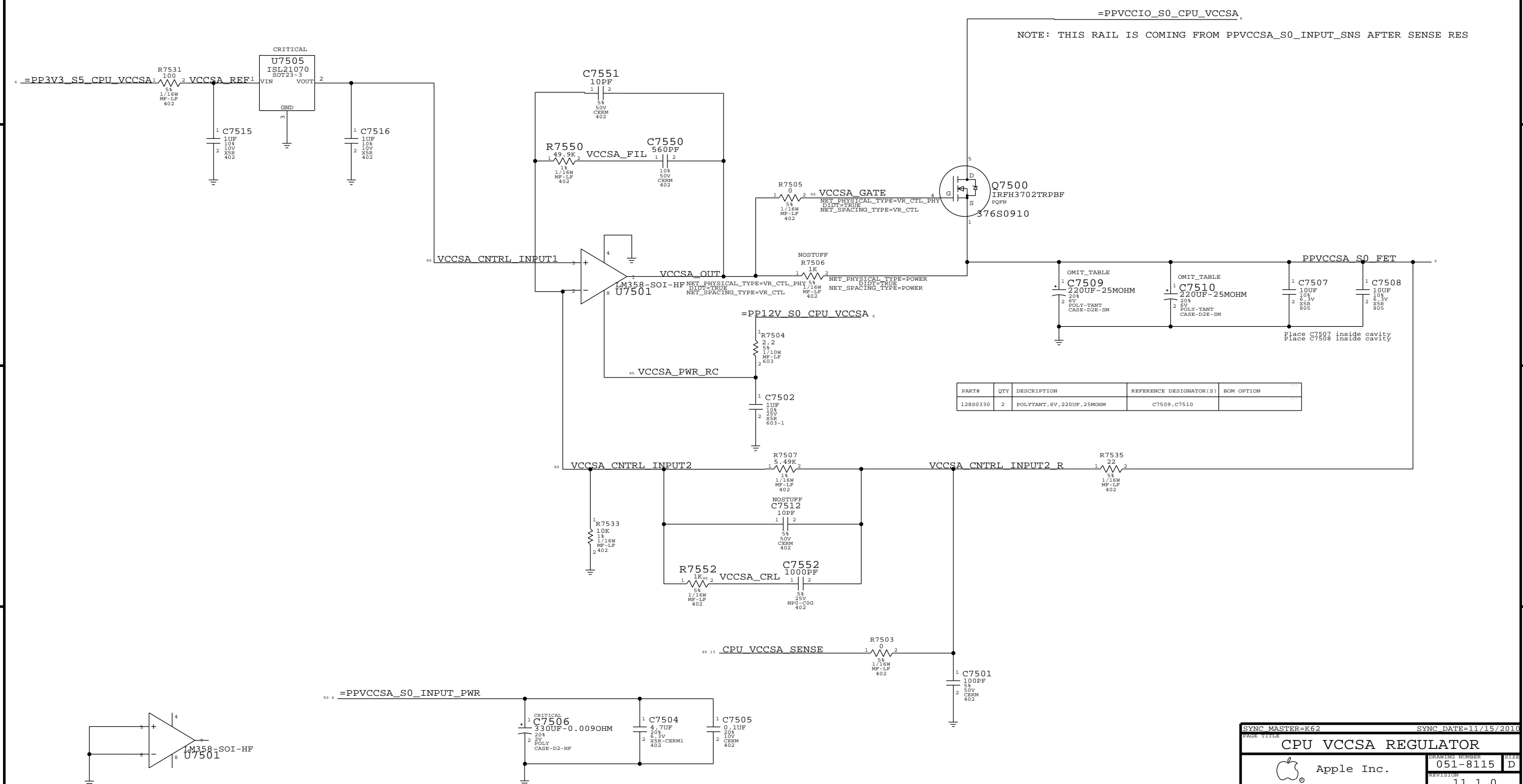


1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

SYNC MASTER=K62		SYNC DATE=01/06/2011	
1V05 REGULATOR			
Apple Inc.		DRAWING NUMBER	051-8115
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CPU VCCSA 0.925V (8.8A MAX)



NOTE: THIS RAIL IS COMING FROM PPVCCSA_S0_INPUT_SNS AFTER SENSE RES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT, 6V, 220UF, 25MOHM	C7509, C7510	

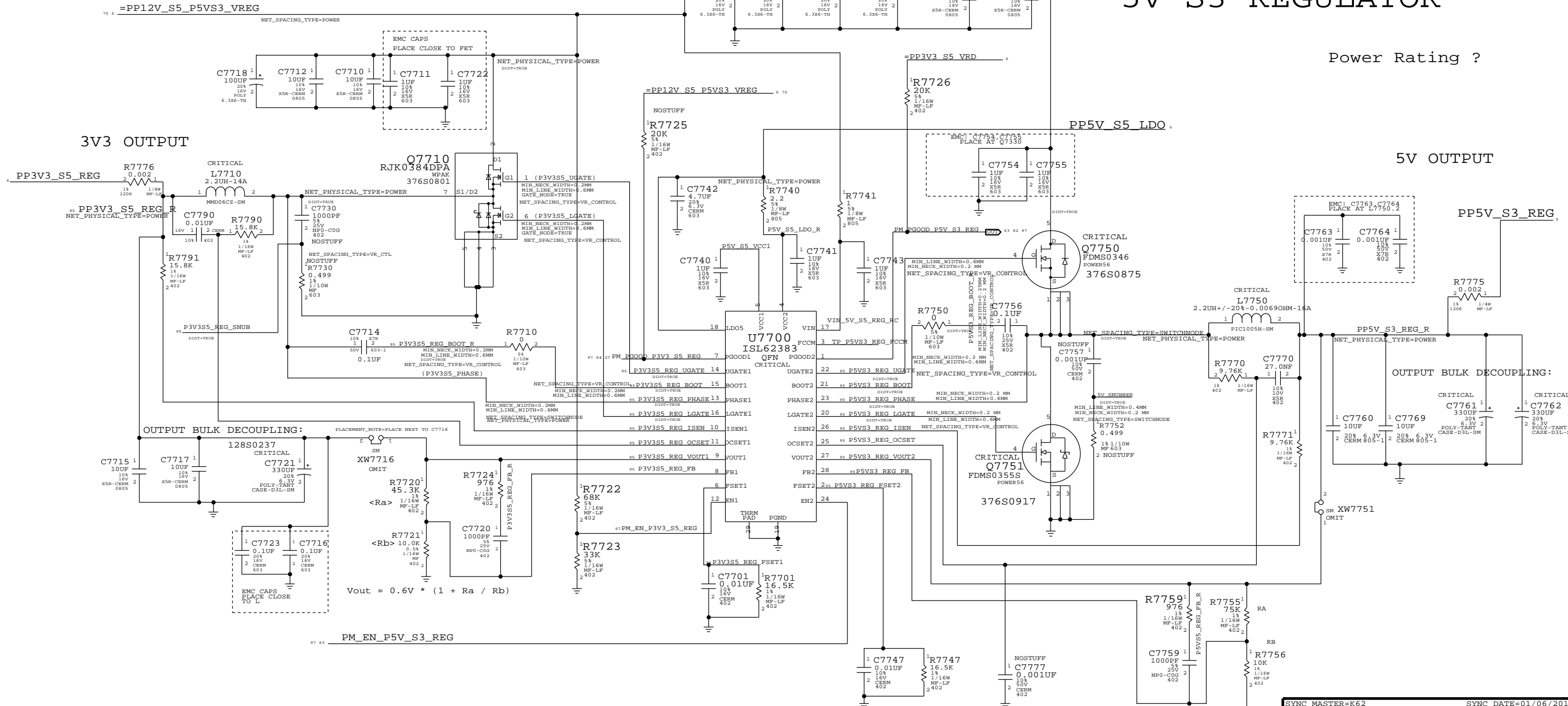
Place C7507 inside cavity
Place C7508 inside cavity

NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

SYNC MASTER=K62		SYNC DATE=11/15/2010	
CPU VCCSA REGULATOR			
Apple Inc.		DRAWING NUMBER	051-8115
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		PAGE	75 OF 110
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3V3 S5 REGULATOR

5V S3 REGULATOR



Power Rating ?

5V OUTPUT

3V3 OUTPUT

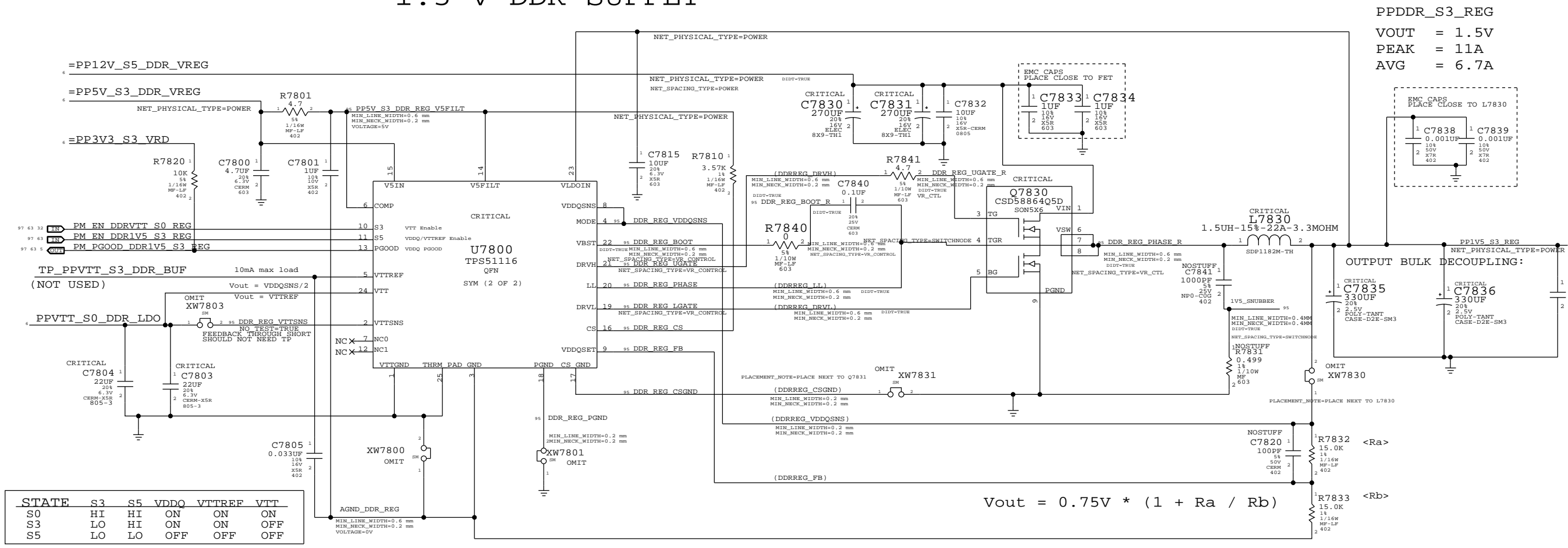
OUTPUT BULK DECOUPLING:

OUTPUT BULK DECOUPLING:

$$V_{out} = 0.6V * (1 + R_a / R_b)$$

PAGE TITLE		SYNC DATE=01/06/2011	
5V_S3 / 3V3_S5 VREGS		DRAWING NUMBER	051-8115
Apple Inc.		REVISION	11.1.0
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1.5 V DDR SUPPLY

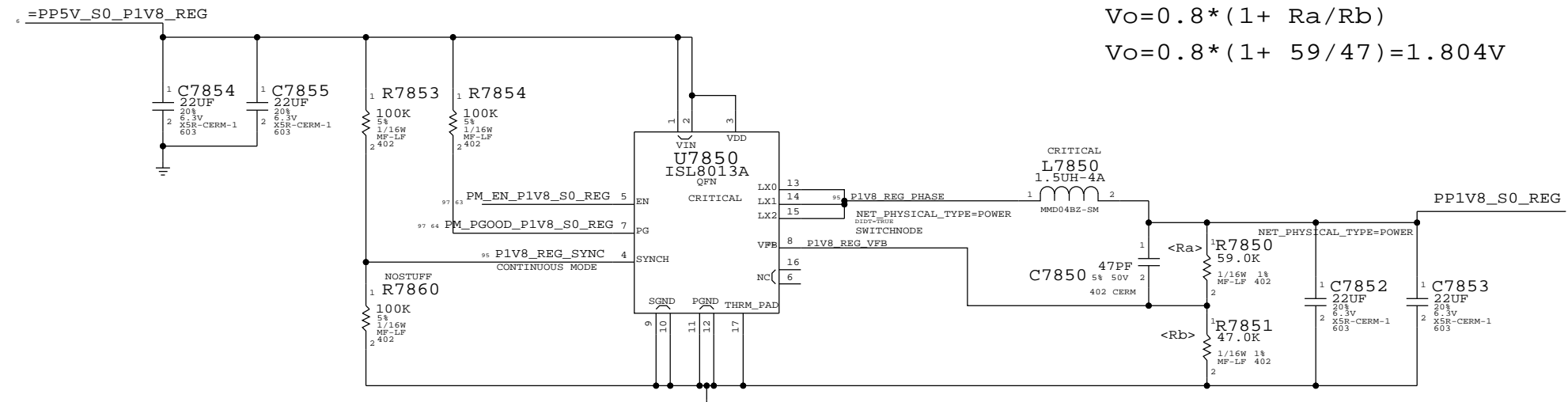


1.8 V SUPPLY

1A Average current

$V_o = 0.8 * (1 + R_a / R_b)$

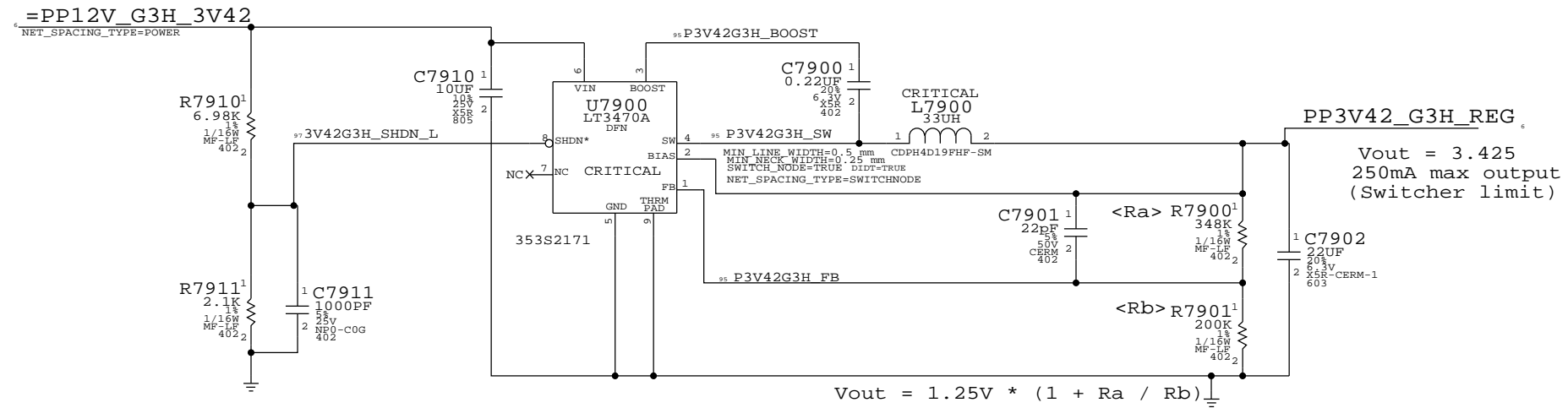
$V_o = 0.8 * (1 + 59 / 47) = 1.804V$



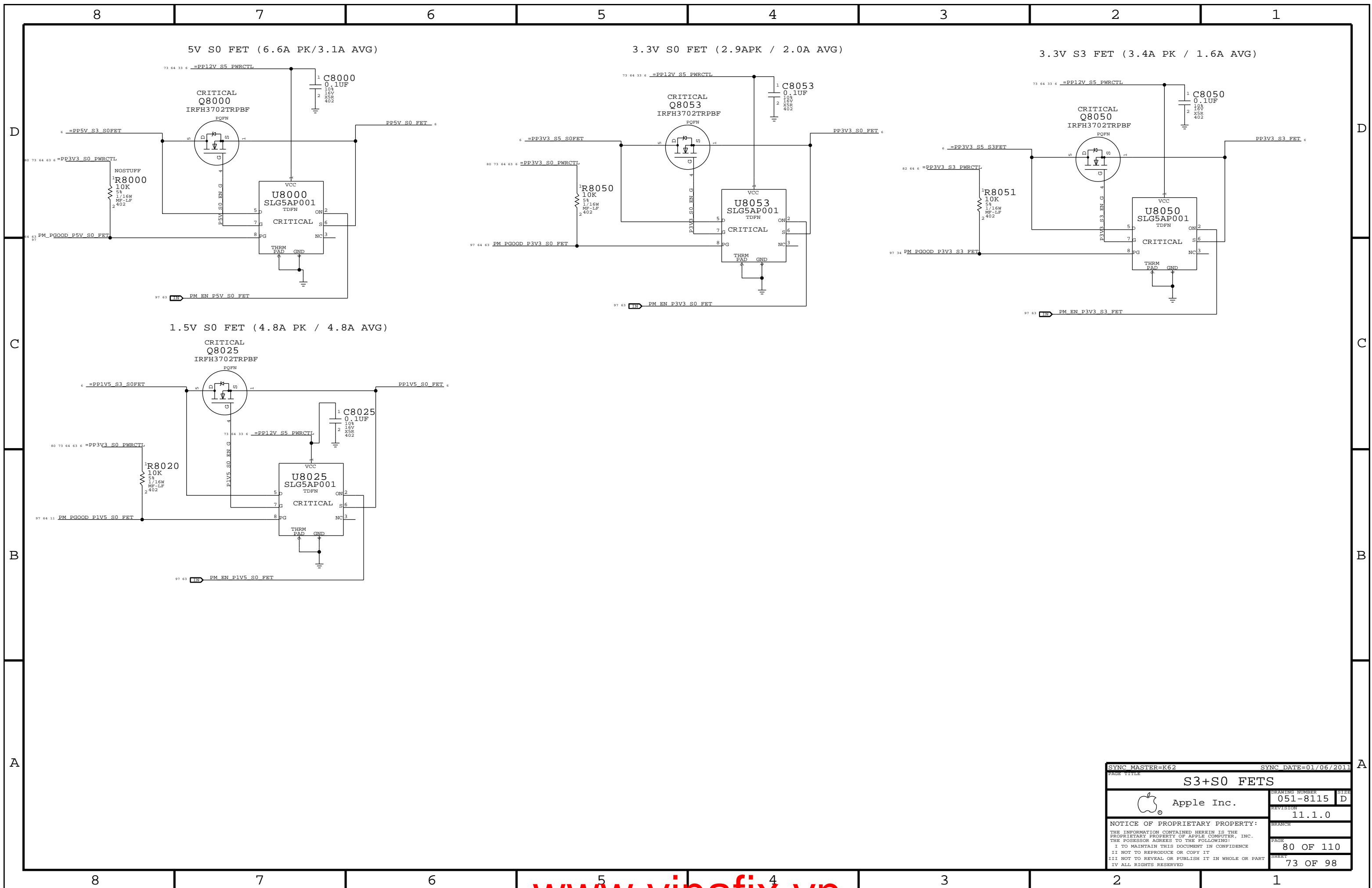
SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE			
1.5V / 1.8V VREGS			
Apple Inc.		DRAWING NUMBER	051-8115
		REVISION	11.1.0
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3.425V "G3Hot" Supply

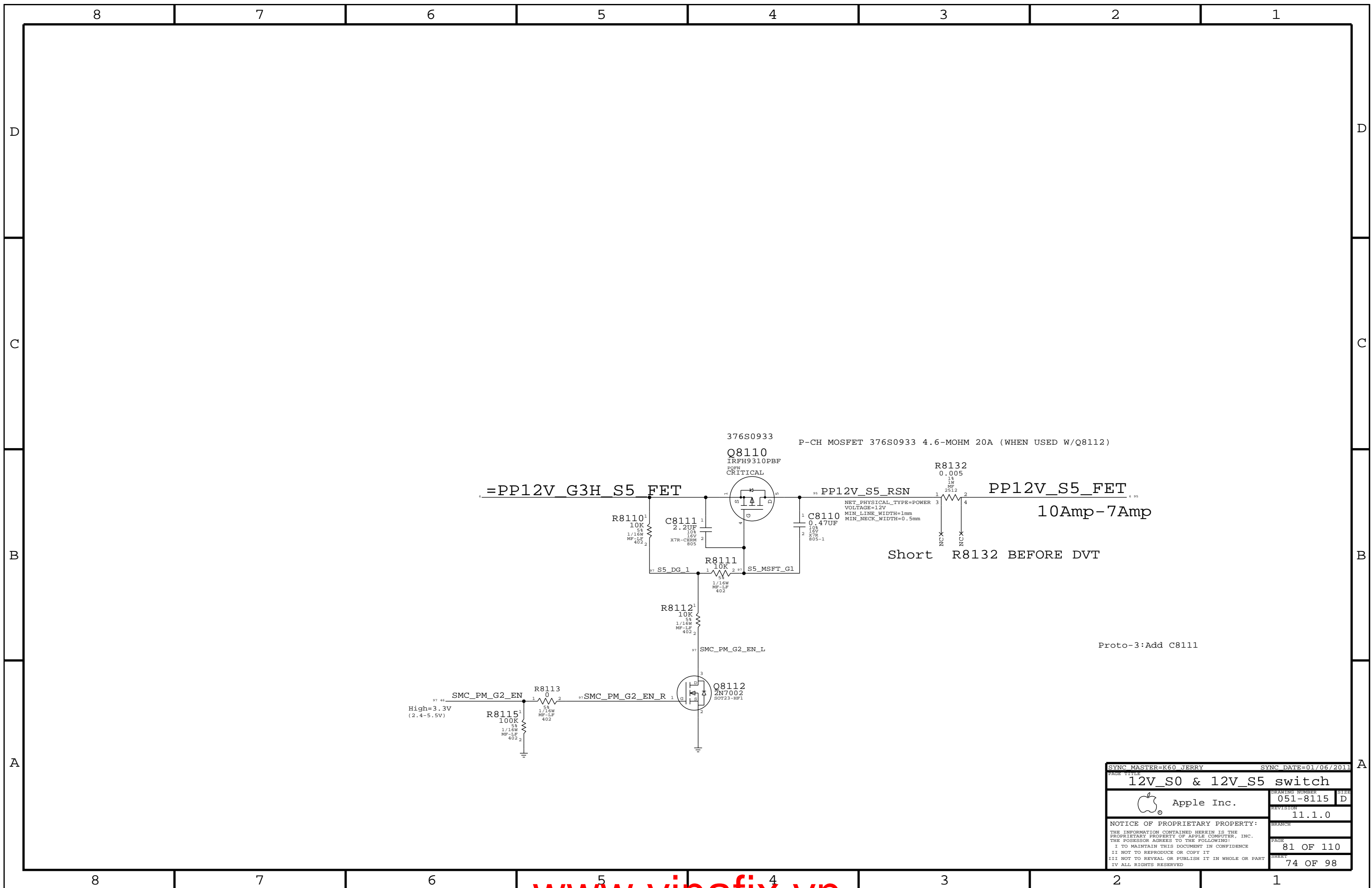
Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC MASTER=K62		SYNC DATE=01/06/2011	
3.42 G3HOT SUPPLY			
DRAWING NUMBER		SIZE	
051-8115		D	
REVISION		BRANCH	
11.1.0			
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S3+S0 FETS			
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		11.1.0	
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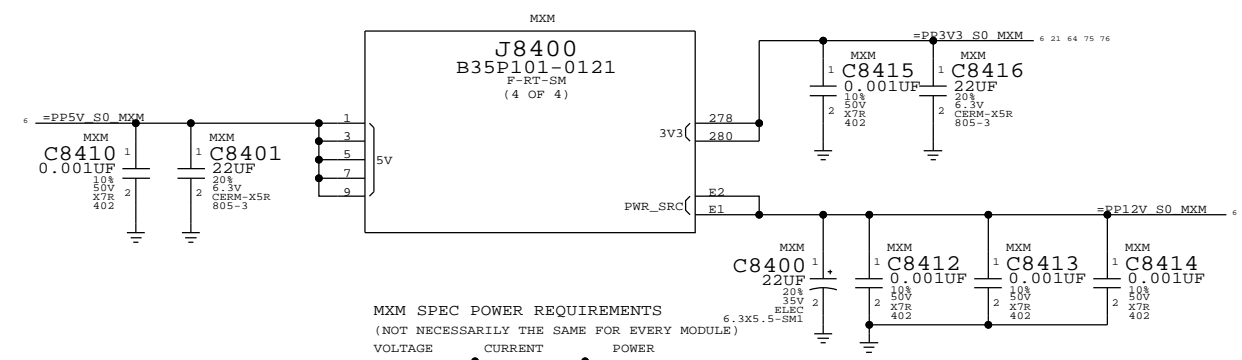
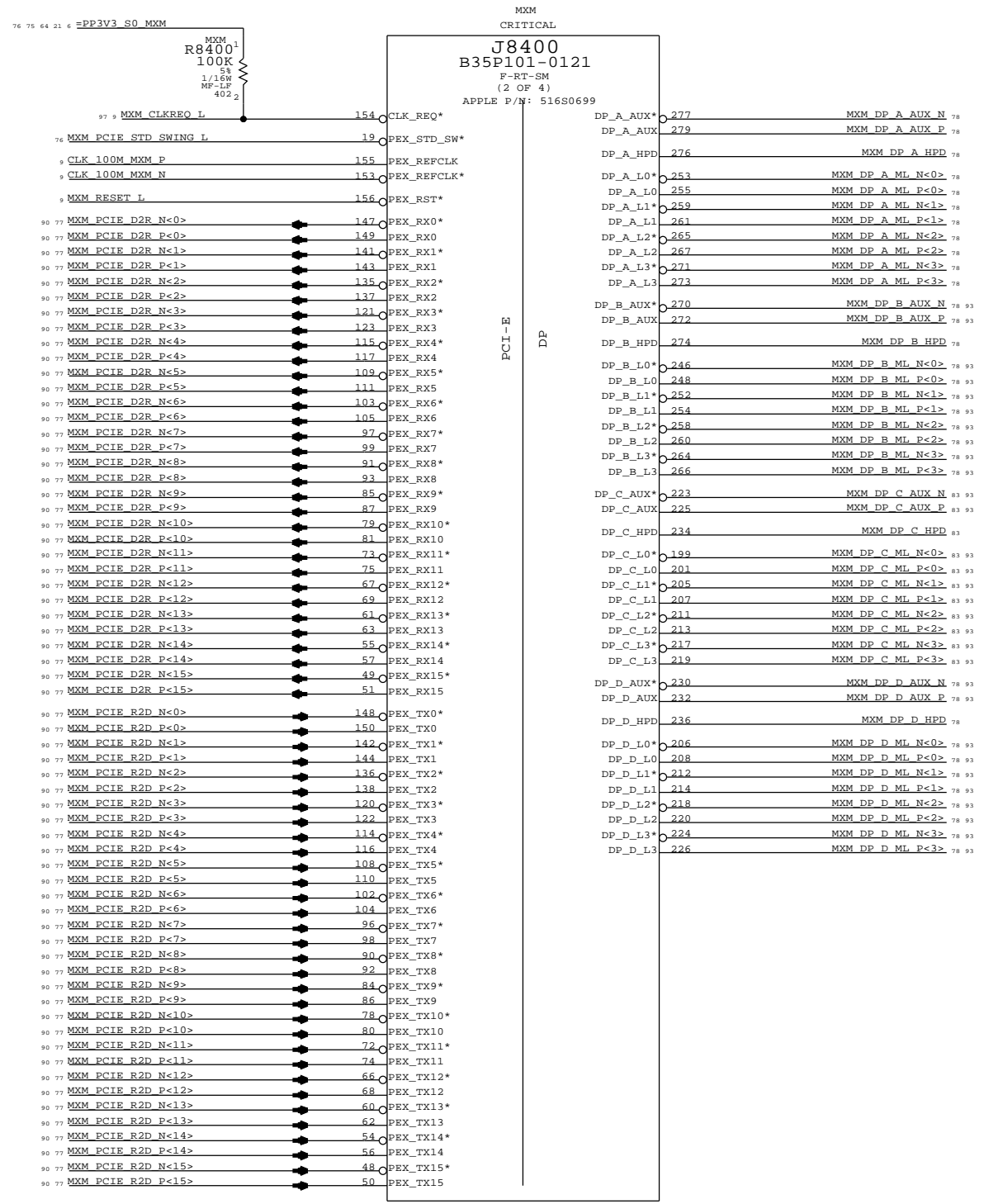
SYNC MASTER=K60_JERRY		SYNC DATE=01/06/2011	
PAGE TITLE 12V_S0 & 12V_S5 switch			
DRAWING NUMBER 051-8115		SIZE D	
REVISION 11.1.0		BRANCH	
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Page Notes

Power aliases required by this page:
 - =PP3V3_S0_MXM
 - =PP5V_S0_MXM
 - =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - MXM



MXM SPEC POWER REQUIREMENTS
 (NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER: 051-8115
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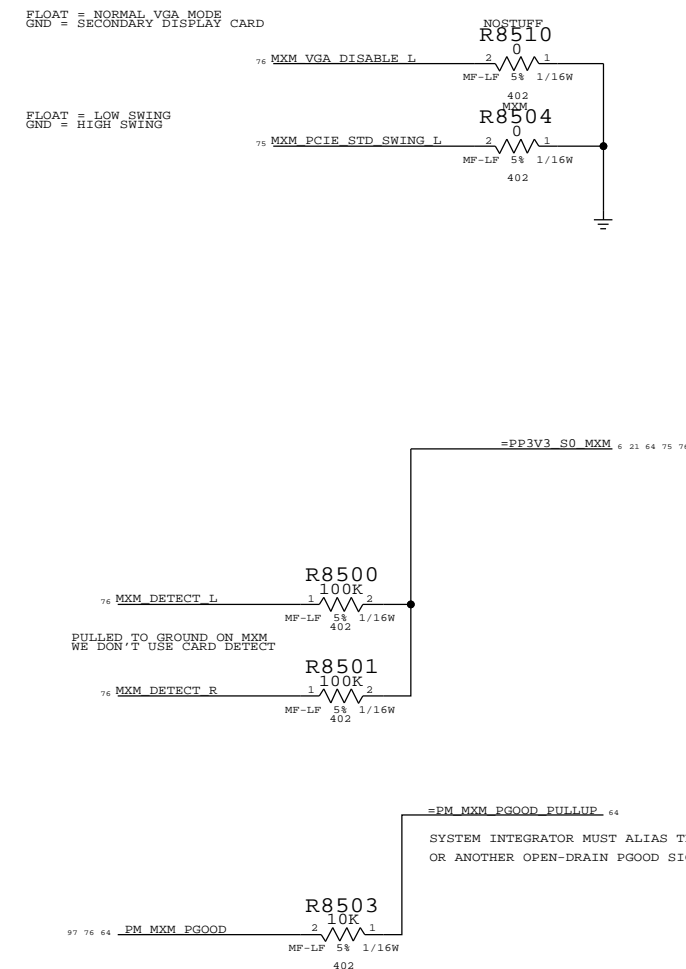
Page Notes

Power aliases required by this page:
 - =PP3V3_S0_MXM

Signal aliases required by this page:
 - =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
 - =SMB_MXM_THRM_CLK

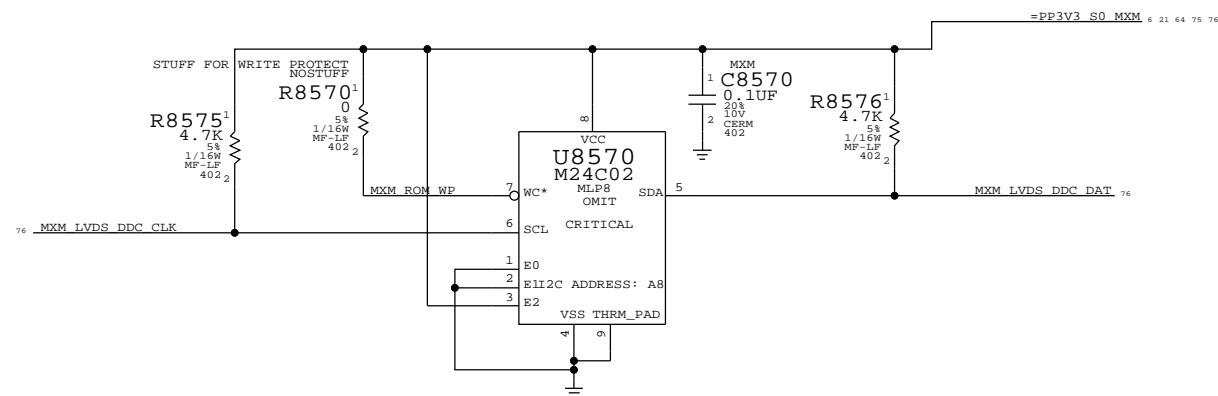
BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400




PAGE TITLE		SYNC DATE=N/A	
MXM I/O			
Apple Inc.	DRAWING NUMBER	051-8115	SIZE
	REVISION	11.1.0	
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MXM TX CAPS

90	150	PEG_R2D_C_P<0>	MXM C8600 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	90 75
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90	150	PEG_R2D_C_P<1>	MXM C8603 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	90 75
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MXM RX CAPS

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SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE			
MXM PCIE CAPS			
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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

75 MXM DP A ML P<0..3> == DP EXTA ML C P<0..3> 84 93
 MAKE_BASE=TRUE NO_TEST=TRUE
 75 MXM DP A ML N<0..3> == DP EXTA ML C N<0..3> 84 93
 MAKE_BASE=TRUE NO_TEST=TRUE
 75 MXM DP A AUX P == DP EXTA AUXCH C P 78 84 93
 MAKE_BASE=TRUE NO_TEST=TRUE
 75 MXM DP A AUX N == DP EXTA AUXCH C N 78 84 93
 MAKE_BASE=TRUE NO_TEST=TRUE
 75 MXM DP A HPD == DP EXTA HPD 84
 MAKE_BASE=TRUE NO_TEST=TRUE

T29 CONN POWER CONTROL ALIAS

95 84 PP3V3_SW_DPAEWR == PP3V3_SW_DPAEWR 6
 97 36 13 19 PCIE_WAKE_L == T29_WAKE_L 84

Unused MXM Interfaces

93 76 MXM LVDS A CLK N == NC MXM LVDS A CLK N
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 76 MXM LVDS A CLK P == NC MXM LVDS A CLK P
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 76 MXM LVDS A DATA N<3..0> == NC MXM LVDS A DATA N<3..0>
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 76 MXM LVDS A DATA P<3..0> == NC MXM LVDS A DATA P<3..0>
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 93 76 MXM LVDS B CLK N == NC MXM LVDS B CLK N
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 76 MXM LVDS B CLK P == NC MXM LVDS B CLK P
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 76 MXM LVDS B DATA N<3..0> == NC MXM LVDS B DATA N<3..0>
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 76 MXM LVDS B DATA P<3..0> == NC MXM LVDS B DATA P<3..0>
 MAKE_BASE=TRUE NO_TEST=TRUE

T29 MXM DP ALIAS

93 75 MXM DP D ML P<0..3> == DP T29SNK0 ML C P<0..3> 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP D ML N<0..3> == DP T29SNK0 ML C N<0..3> 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP D AUX P == DP T29SNK0 AUXCH C P 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP D AUX N == DP T29SNK0 AUXCH C N 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 75 MXM DP D HPD == DP T29SNK0 HPD 86
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP B ML P<0..3> == DP T29SNK1 ML C P<0..3> 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP B ML N<0..3> == DP T29SNK1 ML C N<0..3> 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP B AUX P == DP T29SNK1 AUXCH C P 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 93 75 MXM DP B AUX N == DP T29SNK1 AUXCH C N 86 96
 MAKE_BASE=TRUE NO_TEST=TRUE
 75 MXM DP B HPD == DP T29SNK1 HPD 86
 MAKE_BASE=TRUE NO_TEST=TRUE

Unused T29 Interfaces

96 86 T29 D2R N<2..3> == NC T29 D2R N<2..3>
 MAKE_BASE=TRUE NO_TEST=TRUE
 96 86 T29 D2R P<2..3> == NC T29 D2R P<2..3>
 MAKE_BASE=TRUE NO_TEST=TRUE
 96 86 T29 R2D C N<2..3> == NC T29 R2D C N<2..3>
 MAKE_BASE=TRUE NO_TEST=TRUE
 96 86 T29 R2D C P<2..3> == NC T29 R2D C P<2..3>
 MAKE_BASE=TRUE NO_TEST=TRUE
 86 T29 LSEO<3> == T29 LSEO LSEO1 == T29 LSEO<3> 86
 MAKE_BASE=TRUE NO_TEST=TRUE
 86 T29 LSEO<2> == T29 LSEO LSEO2 == T29 LSEO<2> 86
 MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED MXM CONTROL SIGNALS

76 MXM PNL BL EN == NC MXM PNL BL EN
 MAKE_BASE=TRUE NO_TEST=TRUE
 76 MXM PNL PWR EN == NC MXM PNL PWR EN
 MAKE_BASE=TRUE NO_TEST=TRUE

DDC/AUX ALIAS

93 84 78 DP EXTA AUXCH C P == DP EXTA DDC CLK 84
 MAKE_BASE=TRUE
 93 84 78 DP EXTA AUXCH C N == DP EXTA DDC DATA 84
 MAKE_BASE=TRUE

SYNC MASTER=K60 AARON		SYNC DATE=07/18/2010	
PAGE TITLE			
DP ALIAS AND CONTROL			
DRAWING NUMBER		SIZE	
051-8115		D	
REVISION		BRANCH	
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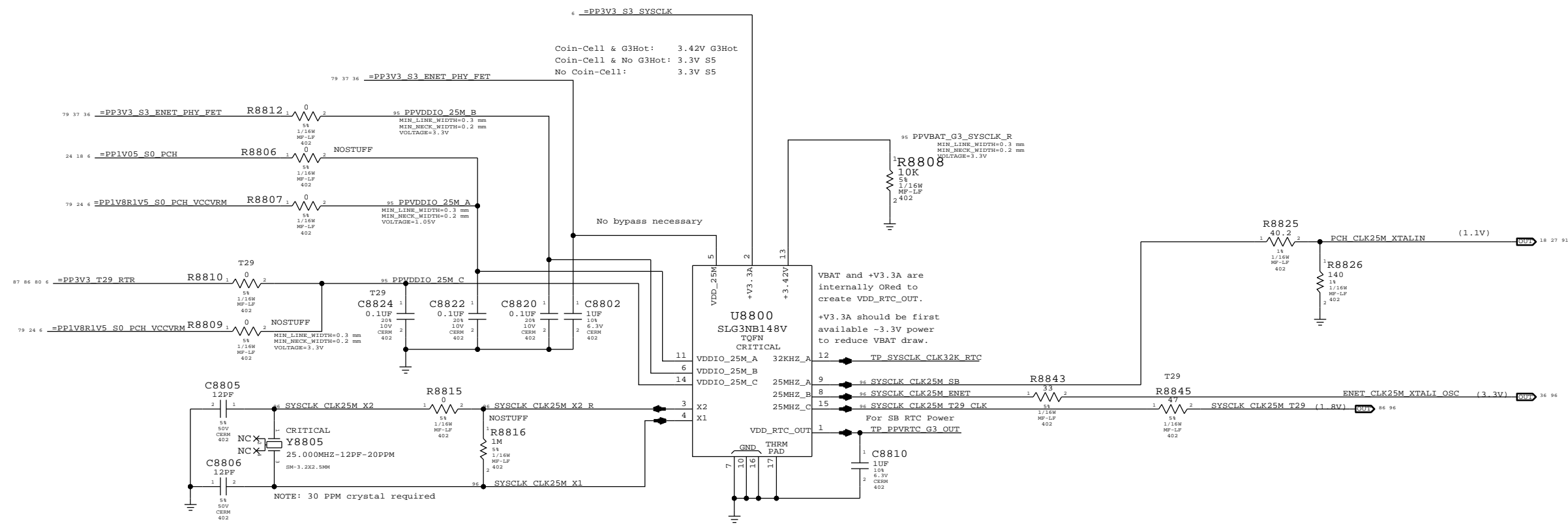
GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
 +V3.3A: Alias as appropriate (see note below)
 VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)
 VDDIO_25M_A: SB power rail for XTAL circuit.
 VDDIO_25M_B: Ethernet power rail for XTAL circuit.
 VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
 For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
 For Caesar-IV (BCMS7765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

System RTC Power Source & 32kHz / 25MHz Clock Generator



SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE: GREEN CLOCK			
DRAWING NUMBER: 051-8115		SIZE: D	
REVISION: 11.1.0		BRANCH:	
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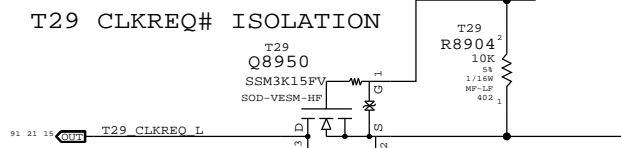
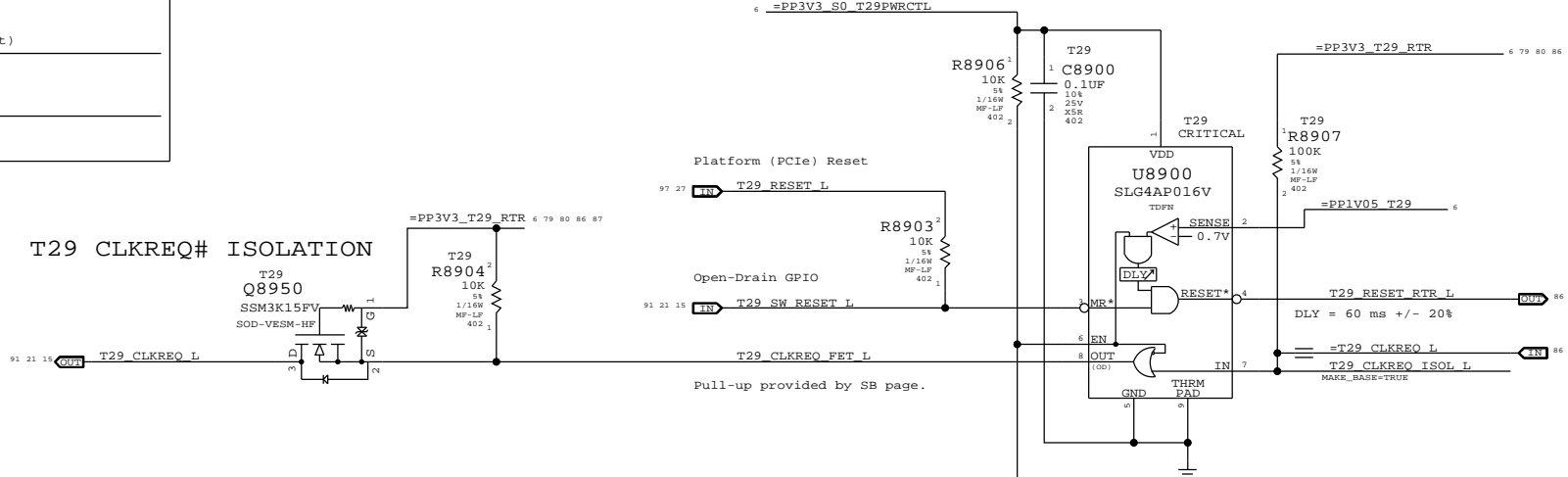
Page Notes

Power aliases required by this page:
 - =PP3V3_T29_P3V3T29FET (3.3V FET Input)
 - =PP3V3_T29_FET (3.3V FET Output)
 - =PP3V3_S0_T29PWRCTL
 - =PP1V05_T29_P1V05T29FET (1.05V FET Input)
 - =PP1V05_T29_FET (1.05V FET Output)

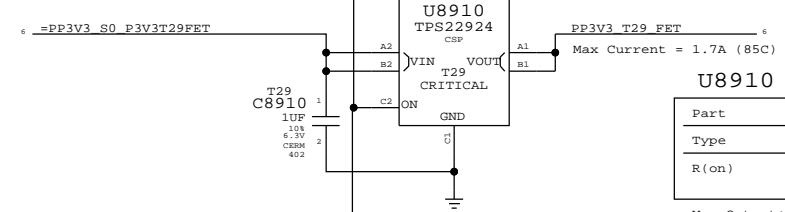
Signal aliases required by this page:
 - =T29_CLKREQ_L
 - T29_RESET_L

BOM options provided by this page:
 (NONE)

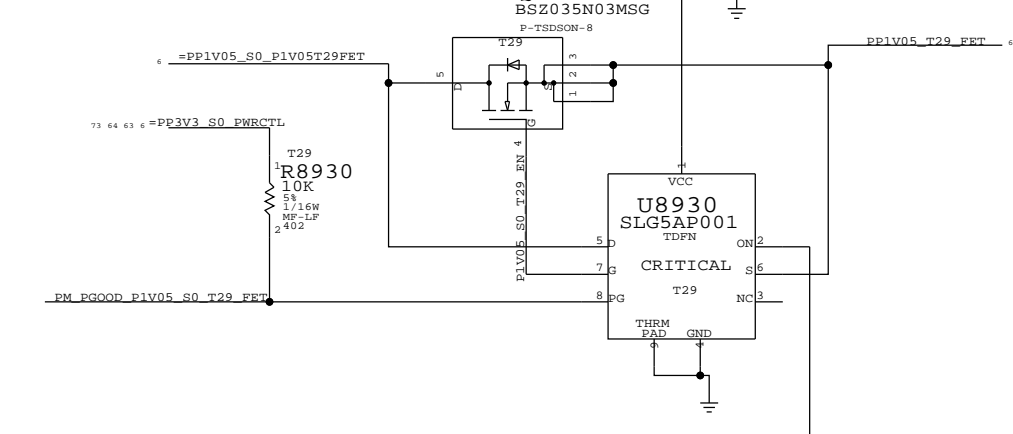
Supervisor & CLKREQ# Isolation



3.3V T29 Switch



1.05V T29 Switch



SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE: T29 POWER			
Apple Inc.		DRAWING NUMBER: 051-8115	SIZE: D
		REVISION: 11.1.0	
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Page Notes

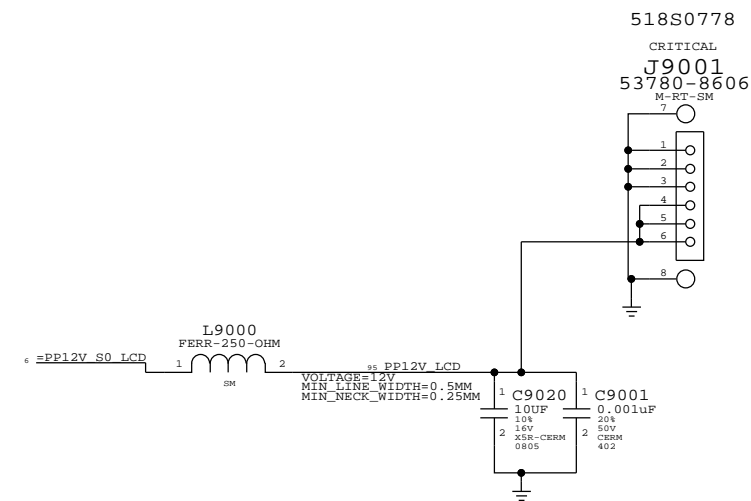
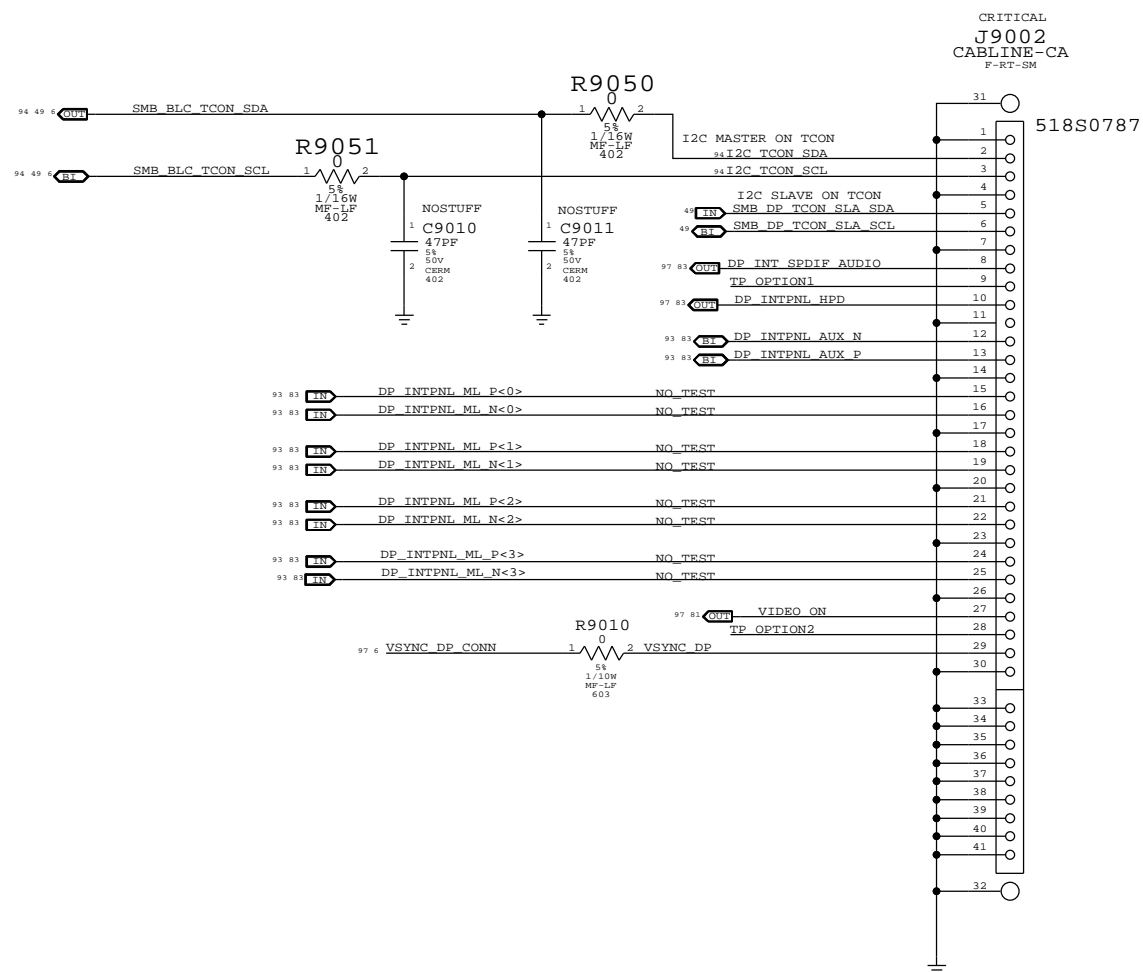
Power aliases required by this page:
 - =PP12V_S0_LCD
 - =PP3V3_S0_VIDEO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

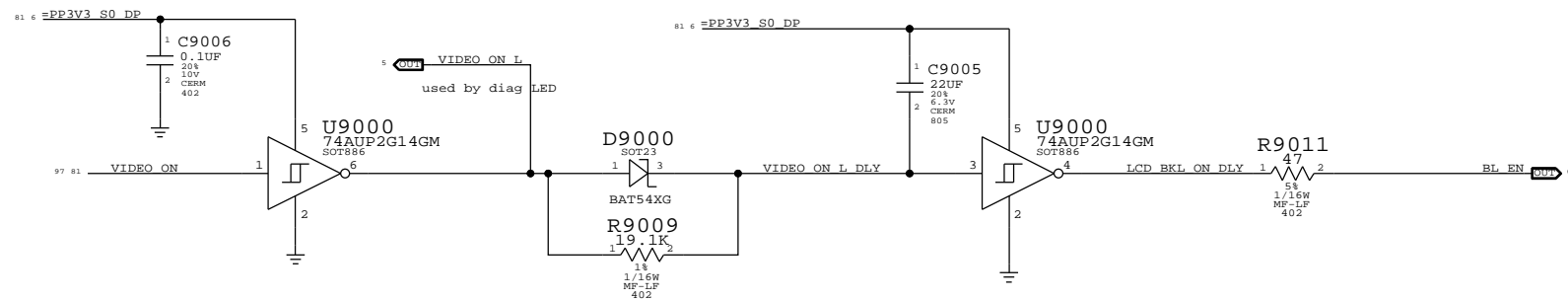
INTERNAL DP INTERFACE

INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

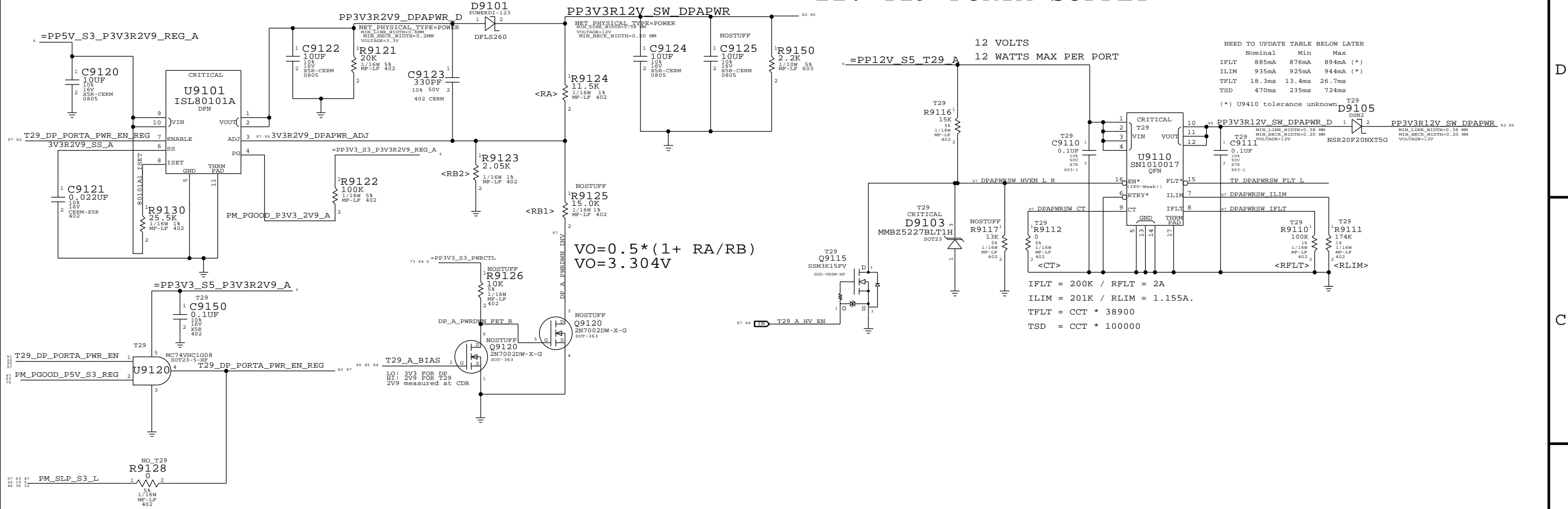
guarantee backlight is
 only on when Panel has valid video



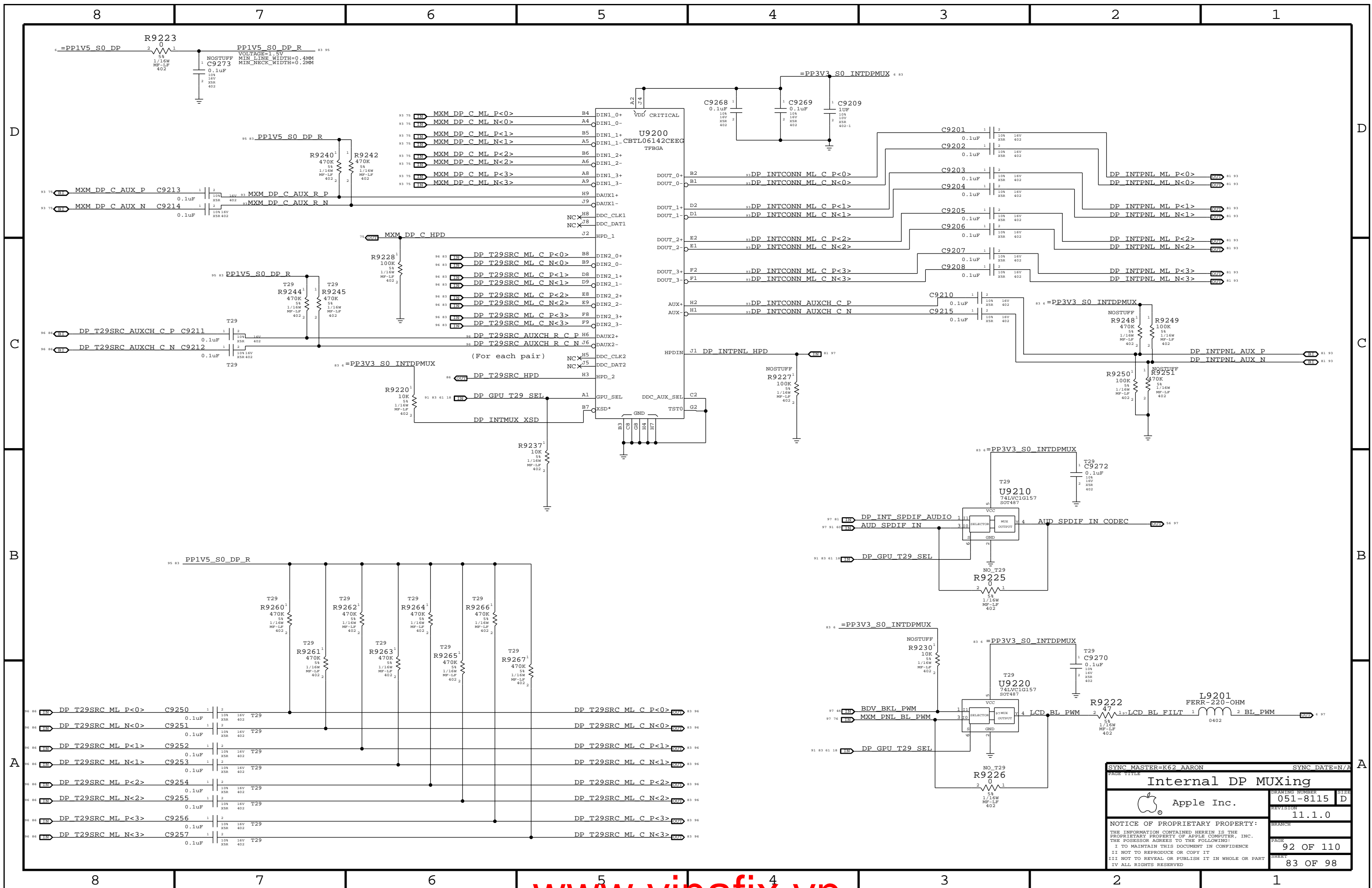
PAGE TITLE		SYNC DATE=01/06/2011	
Display: Int DP Connector		DRAWING NUMBER	SIZE
Apple Inc.		051-8115	D
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3V3 (DP) / 2V9 (T29) PORTA SUPPLY

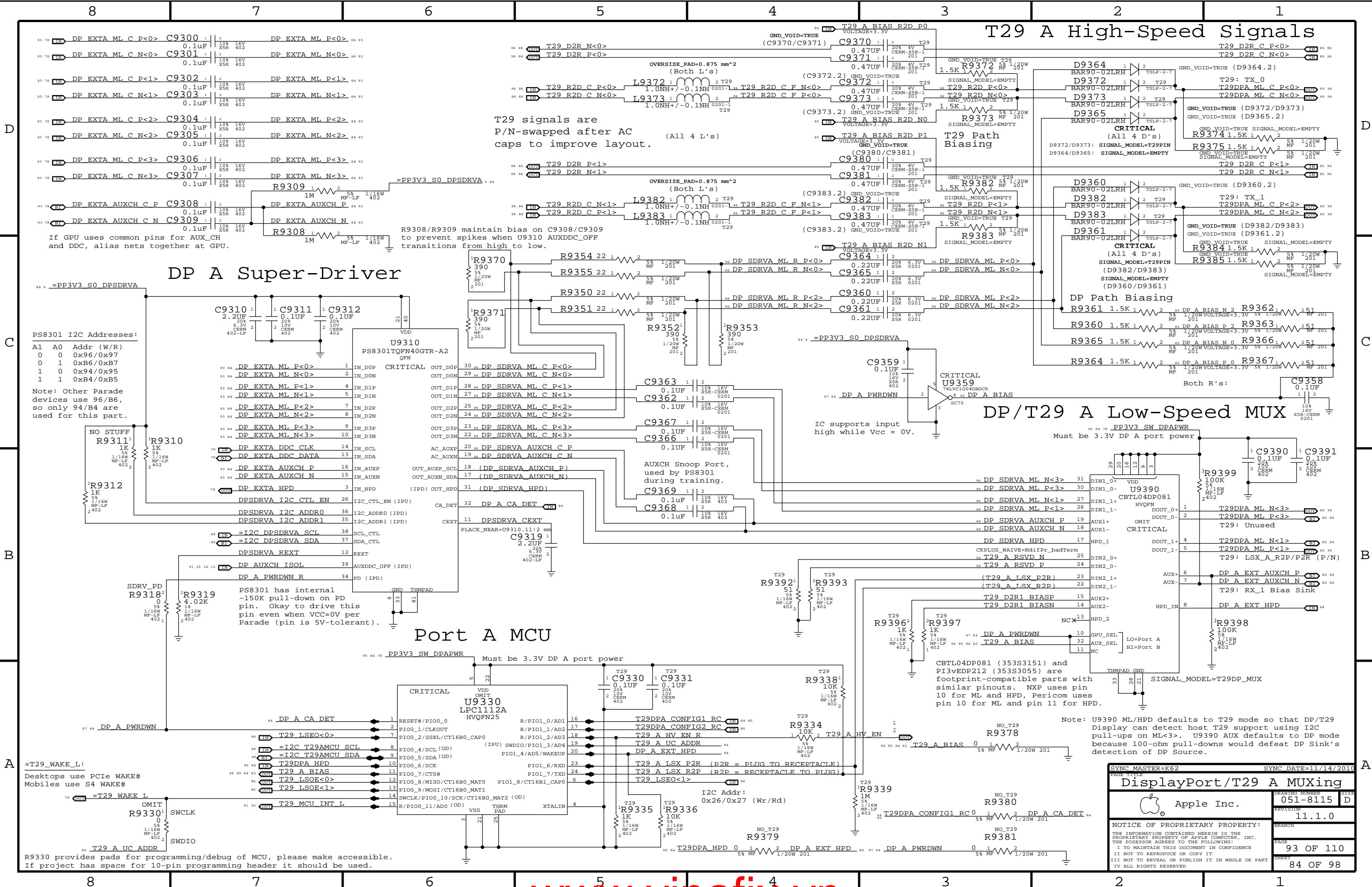
12V T29 PORTA SUPPLY



SYNC MASTER=K62		SYNC DATE=11/14/2010	
PAGE TITLE 2V9/3V3/12V POWER SWITCH			
DRAWING NUMBER 051-8115		SIZE D	
REVISION 11.1.0		BRANCH	
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SYNC MASTER=K62 AARON		SYNC DATE=N/A	
Internal DP MUXing			
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		SHEET	83 OF 98



DP A Super-Driver

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

T29 signals are P/N-swapped after AC caps to improve layout. (All 4 L's)

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

AUXCH Snoop Port, used by PS8301 during training.

DP/T29 A Low-Speed MUX

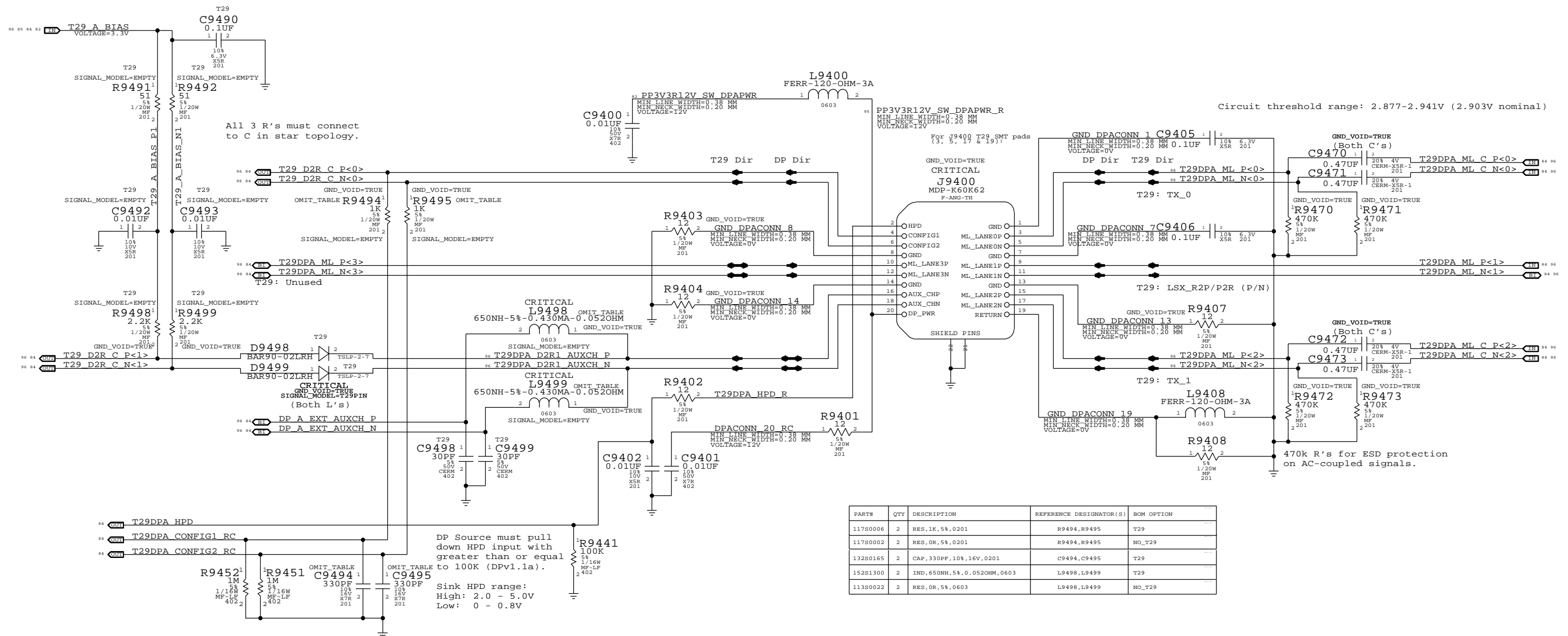
Must be 3.3V DP A port power

Port A MCU

Must be 3.3V DP A port power

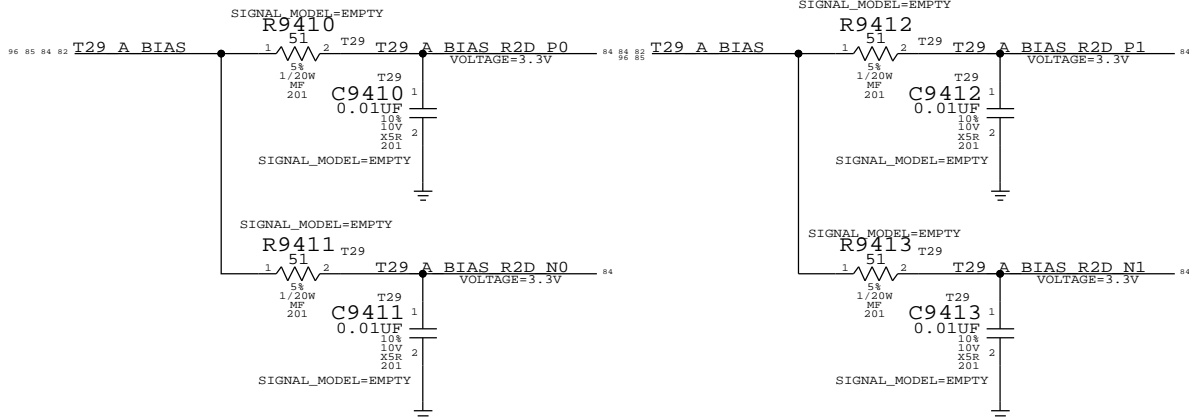
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DisplayPort/T29 A MUXing			
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DisplayPort/T29 A Connector

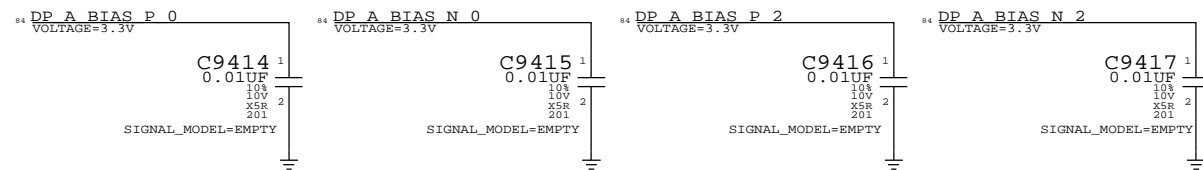


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11780006	2	RES,1K,5%,0201	R9494,R9495	T29
11780002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
11380022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

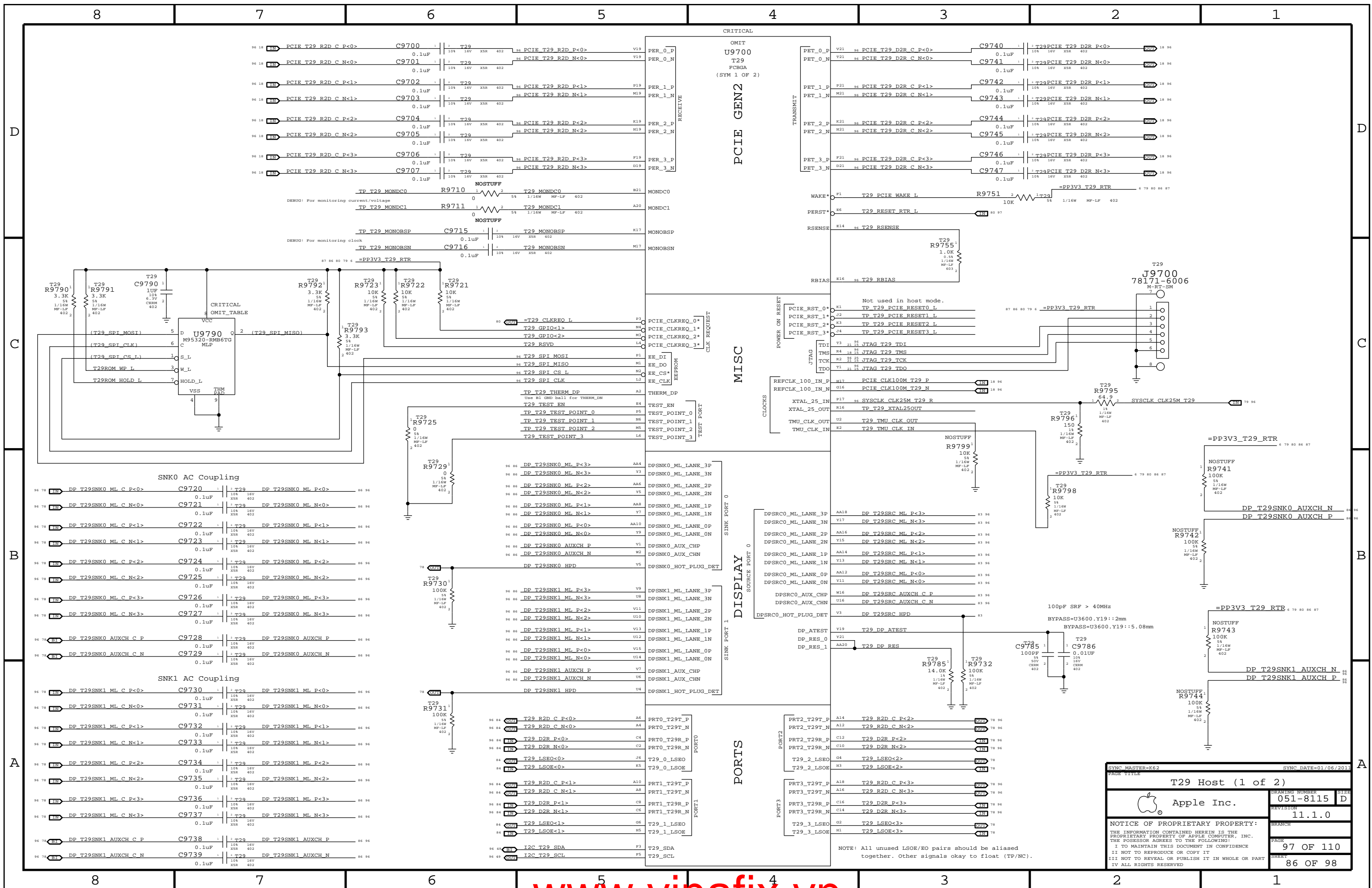
T29 BIAS RC



DP BIAS CAPS



SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
DisplayPort/T29 A Connector			
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T29 Host (1 of 2)

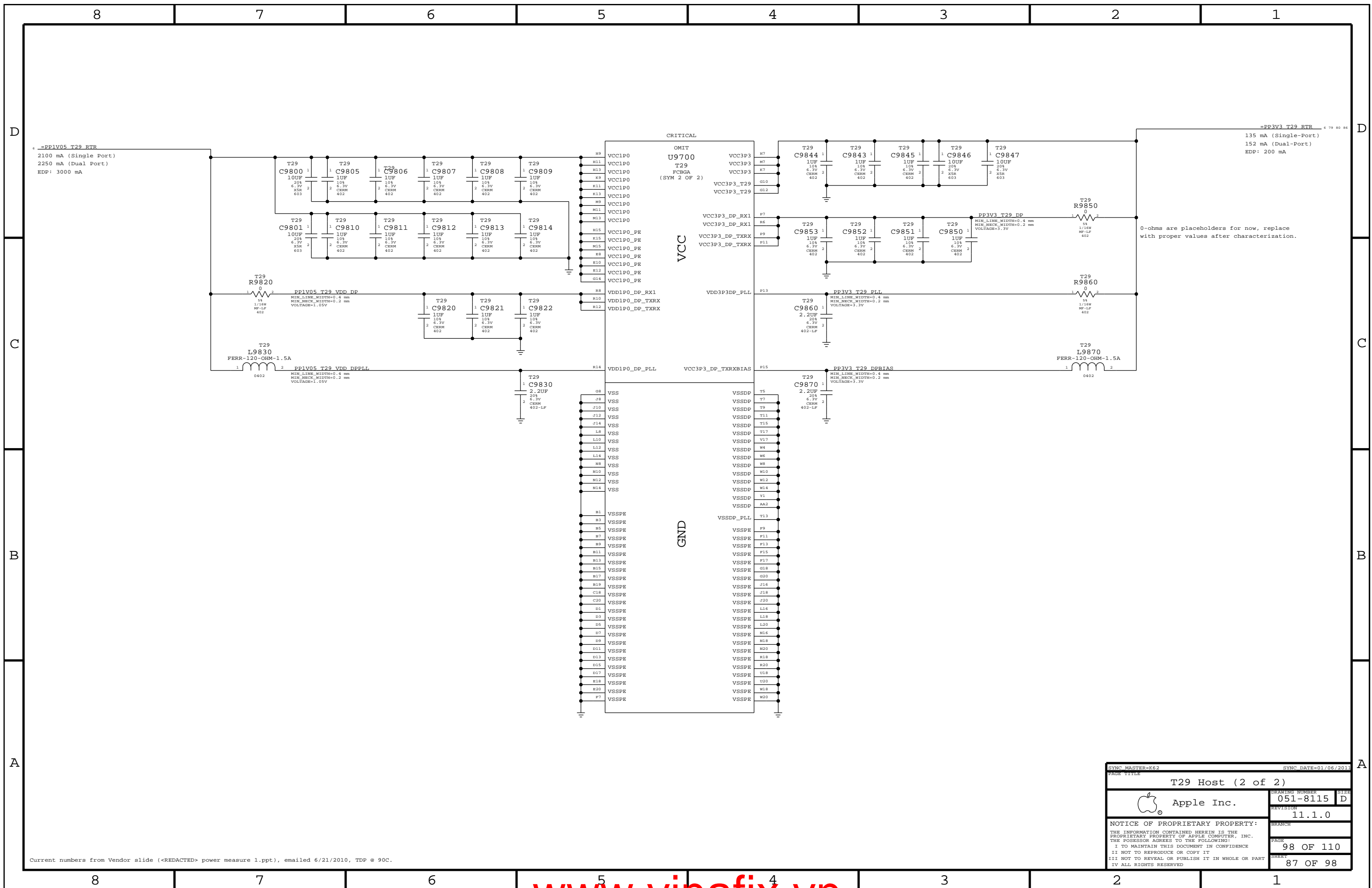
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Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=K62		SYNC DATE=01/06/2011	
T29 Host (2 of 2)			
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K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE, BGA, BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	TOP, BOTTOM	Y	0.21 MM	0.090 MM	=STANDARD		
34_OHM_SE	*	Y	0.19 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP, BOTTOM	Y	0.175 MM	0.090 MM	=STANDARD		
39_OHM_SE	*	Y	0.159 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP, BOTTOM	Y	0.151 MM	0.090 MM	=STANDARD		
42_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68_OHM_DIFF	ISL3, ISL6	Y	0.16 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM
68_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL6	Y	0.099 MM	0.085 MM	12 MM	0.2 MM	0.1 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL6	Y	0.081 MM	0.081 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
3.5:1_SPACING	*	0.35 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P1P5MM	*	0.15 MM	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
*	*	BGA	BGA_P1MM
MEK_CLK	*	BGA	BGA_P1P5MM
CLK_PCIE	*	BGA	BGA_P1MM
CLK_LPC	*	BGA	BGA_P1MM
CLK_PCI	*	BGA	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CONTROL	*	*	SWITCHNODE
VR_CONTROL	VR_CONTROL	*	STANDARD
VR_CONTROL	SWITCHNODE	*	STANDARD
VR_CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.155 MM	?
2X_DIELECTRIC	TOP, BOTTOM	0.145 MM	?
3X_DIELECTRIC	*	0.230 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.215 MM	?
4X_DIELECTRIC	*	0.305 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.285 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.355 MM	?
7X_DIELECTRIC	*	0.532 MM	?
7X_DIELECTRIC	TOP, BOTTOM	0.497 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC MASTER=K62		SYNC DATE=01/06/2011	
PAGE TITLE K60/K62 RULE DEFINITIONS			
DRAWING NUMBER 051-8115		SIZE D	
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Memory Bus Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include MEM_50S, MEM_42S, MEM_39S, MEM_34S, MEM_68D, MEM_42S_D.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include MEM_CLK2MEM, MEM_CTRL2CTRL, MEM_CTRL2MEM, MEM_CMD2CMD, MEM_CMD2MEM, MEM_DQ_SAMEBYTE, MEM_DQ_DIFFBYTE, MEM_DATA2MEM, MEM_DQS2MEM, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_CLK, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_CMD, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_CTRL, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQS, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTES, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTES, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTES, MEM_2OTHER.

Memory Bus Spacing Group Assignments

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTE0, MEM_CTRL, MEM_DATA2MEM, MEM_CMD, MEM_DATA2MEM, MEM_DQ_SAMEBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTE1, MEM_CTRL, MEM_DATA2MEM, MEM_CMD, MEM_DATA2MEM, MEM_DQ_SAMEBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTE2, MEM_CTRL, MEM_DATA2MEM, MEM_CMD, MEM_DATA2MEM, MEM_DQ_SAMEBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTE3, MEM_CTRL, MEM_DATA2MEM, MEM_CMD, MEM_DATA2MEM, MEM_DQ_SAMEBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQ_BYTE4, MEM_CTRL, MEM_DATA2MEM, MEM_CMD, MEM_DATA2MEM, MEM_DQ_SAMEBYTE, MEM_DQ_DIFFBYTE, MEM_DQ_DIFFBYTE, MEM_2OTHER.

Memory Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, VOLTAGE. Rows include MEM A CLK P<3..0>, MEM A CLK N<3..0>, MEM A CKE<3..0>, MEM A CS L<3..0>, MEM A ODT<3..0>, MEM A A<15..0>, MEM A BA<2..0>, MEM A RAS L, MEM A CAS L, MEM A WE L, MEM A DQ<7..0>, MEM A DQ<15..8>, MEM A DQ<23..16>, MEM A DQ<31..24>, MEM A DQ<39..32>, MEM A DQ<47..40>, MEM A DQ<55..48>, MEM A DQ<63..56>, MEM A DQS P<0>, MEM A DQS N<0>, MEM A DQS P<1>, MEM A DQS N<1>, MEM A DQS P<2>, MEM A DQS N<2>, MEM A DQS P<3>, MEM A DQS N<3>, MEM A DQS P<4>, MEM A DQS N<4>, MEM A DQS P<5>, MEM A DQS N<5>, MEM A DQS P<6>, MEM A DQS N<6>, MEM A DQS P<7>, MEM A DQS N<7>, MEM RESET L.

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, VOLTAGE. Rows include MEM B CLK P<3..0>, MEM B CLK N<3..0>, MEM B CKE<3..0>, MEM B CS L<3..0>, MEM B ODT<3..0>, MEM B A<15..0>, MEM B BA<2..0>, MEM B RAS L, MEM B CAS L, MEM B WE L, MEM B DQ<7..0>, MEM B DQ<15..8>, MEM B DQ<23..16>, MEM B DQ<31..24>, MEM B DQ<39..32>, MEM B DQ<47..40>, MEM B DQ<55..48>, MEM B DQ<63..56>, MEM B DQS P<0>, MEM B DQS N<0>, MEM B DQS P<1>, MEM B DQS N<1>, MEM B DQS P<2>, MEM B DQS N<2>, MEM B DQS P<3>, MEM B DQS N<3>, MEM B DQS P<4>, MEM B DQS N<4>, MEM B DQS P<5>, MEM B DQS N<5>, MEM B DQS P<6>, MEM B DQS N<6>, MEM B DQS P<7>, MEM B DQS N<7>.

MEMORY MISC PROPERTIES

Table with 4 columns: VOLTAGE, PHYSICAL, SPACING, VOLTAGE. Rows include CPU DIMM VREF A, CPU DIMM VREF B, CPU DDR VREF, VREFMARGIN DIMMA DACOUT, VREFMARGIN DIMMA OPFB, CPU DIMM VREF A SW, VREFMARGIN DIMMB DACOUT, VREFMARGIN DIMMB OPFB, CPU DIMM VREF B SW.

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row: MEM_POWER_WIDTH, *, Y, 0.500 MM, 0.250 MM, =STANDARD, =STANDARD, =STANDARD.

Table with 6 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET, SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows: MEM_POWER_PHY, *, MEM_POWER_WIDTH, MEM_POWER, *, =3:1_SPACING, ?.

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4:1_SPACING	?
CLK_PCIE	*	0.5 MM	?				

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6:1_SPACING	?	SATA	TOP,BOTTOM	=6:1_SPACING	?

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
SATA			
HDD	SATA_90D	SATA	SATA SSD R2D C P 18 42
HDD	SATA_90D	SATA	SATA SSD R2D C N 18 42
HDD	SATA_90D	SATA	SATA SSD R2D P 42
HDD	SATA_90D	SATA	SATA SSD R2D N 42
HDD	SATA_90D	SATA	SATA SSD D2R P 18 42
HDD	SATA_90D	SATA	SATA SSD D2R N 18 42
HDD	SATA_90D	SATA	SATA SSD D2R C P 42
HDD	SATA_90D	SATA	SATA SSD D2R C N 42
PCIE			
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 R2D P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 R2D N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 R2D C P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 R2D C N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 D2R P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 D2R N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 D2R C P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 1 D2R C N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 R2D P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 R2D N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 R2D C P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 R2D C N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 D2R P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 D2R N
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 D2R C P
HDD	PCI_E_85D	PCI_E	PCI_E USB3 2 D2R C N
CPU ITP			
HDD	CPU_50S	CPU_ITP	XDP_BPM L<7..0> 11 26
HDD	CPU_50S	CPU_ITP	CPU_CFG<17..0> 10 15 25
HDD	CPU_50S	CPU_ITP	XDP_OBSDATA B<3..0> 26
HDD	CPU_50S	CPU_ITP	XDP_CPU_CFG<0> 26
HDD	CPU_50S	CPU_ITP	XDP_CPU_TDO 11 26
HDD	CPU_50S	CPU_ITP	XDP_CPU_TDI 11 26
HDD	CPU_50S	CPU_ITP	XDP_CPU_TMS 11 26
HDD	CPU_50S	CPU_ITP	XDP_CPU_TCK 11 26
HDD	CPU_50S	CPU_ITP	XDP_CPU_TRST L 11 26
CPU_MISC			
HDD	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP 10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING																																																																																																																																																																																																																																																																																																
PCIE GRAPHICS																																																																																																																																																																																																																																																																																																			
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HDD	PCI_E_85D	PCI_E	MMX_PCIE_D2R N<7..0> 75 77	PCIE I/O				HDD	PCI_E_85D	PCI_E	PCI_E MINI_R2D P 33	HDD	PCI_E_85D	PCI_E	PCI_E MINI_R2D N 33	HDD	PCI_E_85D	PCI_E	PCI_E MINI_R2D C P 18 33	HDD	PCI_E_85D	PCI_E	PCI_E MINI_R2D C N 18 33	HDD	PCI_E_85D	PCI_E	PCI_E MINI_D2R P 18 33	HDD	PCI_E_85D	PCI_E	PCI_E MINI_D2R N 18 33	PCIE FW				HDD	PCI_E_85D	PCI_E	PCI_E FW_R2D P 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_R2D N 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_R2D C P 18 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_R2D C N 18 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_D2R P 18 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_D2R N 18 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_D2R C P 39	HDD	PCI_E_85D	PCI_E	PCI_E FW_D2R C N 39	DMI				HDD	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M N	HDD	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M P	HDD	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU N 11 18	HDD	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU P 11 18	HDD	PCI_E_85D	PCI_E	DMI_S2N P<3..0> 10 19	HDD	PCI_E_85D	PCI_E	DMI_S2N N<3..0> 10 19	HDD	PCI_E_85D	PCI_E	DMI_N2S P<3..0> 10 19	HDD	PCI_E_85D	PCI_E	DMI_N2S N<3..0> 10 19	PCIE REF CLOCKS				HDD	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE P 9	HDD	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE N 9	HDD	CLK_PCIE_90D	CLK_PCIE	PCI_E_CLK100M_MINI P 18 33	HDD	CLK_PCIE_90D	CLK_PCIE	PCI_E_CLK100M_MINI N 18 33	HDD	CLK_PCIE_90D	CLK_PCIE	PCI_E_CLK100M_FW P 18 39	HDD	CLK_PCIE_90D	CLK_PCIE	PCI_E_CLK100M_FW N 18 39	HDD	ENET_100D	ENET_MII	PCI_E_CLK100M_ENET P 18 37	HDD	ENET_100D	ENET_MII	PCI_E_CLK100M_ENET N 18 37	SATA				HDD	SATA_90D	SATA	SATA_HDD_R2D C P 18 42	HDD	SATA_90D	SATA	SATA_HDD_R2D C N 18 42	HDD	SATA_90D	SATA	SATA_HDD_R2D P 42	HDD	SATA_90D	SATA	SATA_HDD_R2D N 42	HDD	SATA_90D	SATA	SATA_HDD_D2R P 18 42	HDD	SATA_90D	SATA	SATA_HDD_D2R N 18 42	HDD	SATA_90D	SATA	SATA_HDD_D2R C P 42	HDD	SATA_90D	SATA	SATA_HDD_D2R C N 42	HDD	SATA_90D	SATA	SATA_ODD_R2D C P 18 42	HDD	SATA_90D	SATA	SATA_ODD_R2D C N 18 42	HDD	SATA_90D	SATA	SATA_ODD_R2D P 42	HDD	SATA_90D	SATA	SATA_ODD_R2D N 42	HDD	SATA_90D	SATA	SATA_ODD_D2R P 18 42	HDD	SATA_90D	SATA	SATA_ODD_D2R N 18 42	HDD	SATA_90D	SATA	SATA_ODD_D2R C P 42	HDD	SATA_90D	SATA	SATA_ODD_D2R C N 42	CLOCKS				HDD	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI P 18 26	HDD	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI N 18 26	HDD	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT P 18 26	HDD	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT N 18 26	HDD	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA P 18 26	HDD	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA N 18 26	HDD	CLK_PCIE_90D	CLK_PCIE	ITEXDP_CLK100M N 18 25	HDD	CLK_PCIE_90D	CLK_PCIE	ITEXDP_CLK100M P 18 25	HDD	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M N 11 18	HDD	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M P 11 18	HDD	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M P 25	HDD	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M N 25	UNUSED CLOCKS				HDD	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH N 26	HDD	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH P 26	UNUSED PCIE				HDD	PCI_E_85D	PCI_E	MMX_PCIE_R2D P<8..15> 75 77	HDD	PCI_E_85D	PCI_E	MMX_PCIE_R2D N<8..15> 75 77	HDD	PCI_E_85D	PCI_E	MMX_PCIE_D2R P<8..15> 75 77	HDD	PCI_E_85D	PCI_E	MMX_PCIE_D2R N<8..15> 75 77
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HDD	CLK_PCIE_90D	CLK_PCIE	ITEXDP_CLK100M N 18 25																																																																																																																																																																																																																																																																																																
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HDD	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M P 25																																																																																																																																																																																																																																																																																																
HDD	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M N 25																																																																																																																																																																																																																																																																																																
UNUSED CLOCKS																																																																																																																																																																																																																																																																																																			
HDD	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH N 26																																																																																																																																																																																																																																																																																																
HDD	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH P 26																																																																																																																																																																																																																																																																																																
UNUSED PCIE																																																																																																																																																																																																																																																																																																			
HDD	PCI_E_85D	PCI_E	MMX_PCIE_R2D P<8..15> 75 77																																																																																																																																																																																																																																																																																																
HDD	PCI_E_85D	PCI_E	MMX_PCIE_R2D N<8..15> 75 77																																																																																																																																																																																																																																																																																																
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HDD	PCI_E_85D	PCI_E	MMX_PCIE_D2R N<8..15> 75 77																																																																																																																																																																																																																																																																																																

SYNC_MASTER=K62		SYNC_DATE=01/06/2011	
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PCIE/DMI/FDI/SATA CONSTRAINTS		DRAWING NUMBER	SIZE
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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2X_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2X_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

PHYSICAL	NET_TYPE	SPACING	
R332	PM	T29 CLKREQ L	15 21 80
R333	PM	FW MINI CLKREQ L	15 18
R334	PM	BLC GPIO	6 15 21
R335	PM	T29 SW RESET L	15 21 80
R336	PM	ENET CLKREQ L	15 18 36
R337	PM	DP GPU T29_SEL	18 61 83
R338	PM	T29 MCU INT L	20 84
R339	PM	T29 DP PORTA PWR EN	20 25 82 97
R340	PM	T29 DP PORTB PWR EN	20 25
R341	PM	DP AUXCH ISOL	15 18 25 84
R342	PM	PLT RST BUF L	27
R343	PM	XDFCPU PLTREST L	25 27
R344	PM	PCH_PEG_CLKREQ L	21
R345	PM	ENET SW RESET L	15 21 36
R346	PM	CPU SKTOCC	63
R347	PM	PM EN USB PWR	43 63

PHYSICAL	NET_TYPE	SPACING	
R348	PM	ENET RESET LOGIC L	36
R349	PM	ENET RESET FET L	
R350	PM	ENET CLKREQ FET L	36 37
R351	PM	PGOOD 5V 1V05 3V3	64 97
R352	PM	PGOOD CPU CORE	64 97
R353	PM	ALL SYS PWBGD	64 97
R354	PM	PGOOD 3V3 1V05	64 97
R355	PM	PGOOD PCH S0 R	64 97
R356	PM	AUD IPHS SWITCH EN PCH	21 25

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
	PCI_55S	PCI	PCI REQ0 L	20
	PCI_55S	PCI	PCI REQ1 L	20
	PCI_55S	PCI	PCI REQ2 L	20
	PCI_55S	PCI	PCI REQ3 L	20
	CLK_PCI_55S	CLK_PCI	PCH CLK33M PCIOUT	20 27
	CLK_PCI_55S	CLK_PCI	PCH CLK33M PCIIN	18 27
	LPC_55S	LPC	LPC AD<3..0>	18 46 48
	LPC_55S	LPC	LPC FRAME L	18 46 48
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	20 27
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	27 46
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	27 48
	CLK_LPC_55S	PM	PM CLK32K SUSCLK R	9 19 97
	CLK_LPC_55S	PM	PM CLK32K SUSCLK	9 46 97
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS R	20 27
	LPC_55S	LPC	LPC R AD<3..0>	18
	LPC_55S	LPC	LPC FRAME R L	18
	SPI_55S	SPI	SPI CLK 1 R	18
	SPI_55S	SPI	SPI MOSI 1 R	18
	CLK_XTAL	XTAL	USB HUB2 XTAL1	35
	CLK_XTAL	XTAL	USB HUB2 XTAL2	35
	CLK_XTAL	XTAL	PCH CLK32K RTCX1 R	27
	CLK_XTAL	XTAL	PCH CLK32K RTCX2 R	27
	CLK_XTAL	XTAL	PCH CLK32K RTCX1	18 27 91
	CLK_XTAL	XTAL	PCH CLK32K RTCX2	18 27 91
	CLK_XTAL	XTAL	PCH CLK32K RTCX1	18 27 91
	CLK_XTAL	XTAL	PCH CLK32K RTCX2	18 27 91
	CLK_XTAL	XTAL	CK505 XTAL IN	26
	CLK_XTAL	XTAL	CK505 XTAL OUT	26
	CLK_XTAL	XTAL	CK505 XTAL OUT R	26
	CLK_PCH_55S	CLK_PCH	PCH CLK14P3M REFCLK	18 26

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
	SET_55S	SET	SPI CLK R	18 48 55
	SET_55S	SET	SPI CLK	55
	SET_55S	SET	SPI MOSI R	18 48 55
	SET_55S	SET	SPI MOSI	55
	SET_55S	SET	SPI MISO	18 48 55
	SET_55S	SET	SPI MISO R	55
	SET_55S	SET	SPI CS0 R L	18 48
	SET_55S	SET	SPI CS0 L	48
	SET_55S	SET	SPI MLB CS L	48 55
	SET_55S	SET	SPI ALT CS L	48
	SET_55S	SET	SPIROM USE MLB	21 48
	SET_55S	SET	SPI ALT MOSI	48
	SET_55S	SET	SPI ALT MISO	48
	SET_55S	SET	SPI ALT CLK	48
	HDA_55S	HDA	HDA BIT CLK	18 56
	HDA_55S	HDA	HDA BIT CLK R	18
	HDA_55S	HDA	HDA RST L	18 56
	HDA_55S	HDA	HDA RST R L	18
	HDA_55S	HDA	HDA SDOUT	15 18 56
	HDA_55S	HDA	HDA SDOUT R	18
	HDA_55S	HDA	HDA SYNC	18 56
	HDA_55S	HDA	HDA SYNC R	18
	HDA_55S	HDA	HDA SDIN0	18 56
	HDA_55S	HDA	AUD SDI R	56
		PM	AUD SPDIF IN	60 83 97
		HDA	AUD SPDIF OUT	56 60
		HDA	AUD SPDIF CHIP	56
	HDA_55S	HDA	AUD SPKR OUTLO1L NOUT	98
	HDA_55S	HDA	AUD SPKR OUTLO1L POUT	98
	HDA_55S	HDA	AUD SPKR OUTLO1R NOUT	98
	HDA_55S	HDA	AUD SPKR OUTLO1R POUT	98
	HDA_55S	HDA	AUD SPKR OUTLO2L NOUT	98
	HDA_55S	HDA	AUD SPKR OUTLO2L POUT	98
	HDA_55S	HDA	AUD SPKR OUTLO2R NOUT	98
	HDA_55S	HDA	AUD SPKR OUTLO2R POUT	98
	CLK_XTAL	XTAL	PCH CLK25M XTALOUT R	27
	CLK_XTAL	XTAL	PCH CLK25M XTALIN R	27
	CLK_XTAL	XTAL	PCH CLK25M XTALOUT	18 27
	CLK_XTAL	XTAL	PCH CLK25M XTALIN	18 27 91
	PCH_55S	COMP_PCH	PCH USB RBIAS	20
	PCH_55S	COMP_PCH	PCH SATA3COMP	18
	PCH_55S	COMP_PCH	PCH XCLK RCOMP	18
	PCH_55S	COMP_PCH	PCH DMI COMP	18
	PCH_55S	COMP_PCH	PCH SATA1COMP	18
	CLK_XTAL	XTAL	USB HUB1 XTAL1	34
	CLK_XTAL	XTAL	USB HUB1 XTAL2	34
	PCH_55S	COMP_PCH	USB HUB1 RBIAS	34
	PCH_55S	ITP_PCH	XDP PCH TCK	18 25
	PCH_55S	ITP_PCH	XDP PCH TMS	18 25
	PCH_55S	ITP_PCH	XDP PCH TDI	18 25
	PCH_55S	ITP_PCH	XDP PCH TDO	18 25
	PCH_55S	COMP_PCH	PCH DMI2BIAS	18
	PCH_55S	COMP_PCH	PCH SATA3BIAS	18
	PCH_55S	COMP_PCH	USB HUB2 RBIAS	35

SYNC MASTER=K62 SYNC DATE=01/06/2011

IBEX PEAK CONSTRAINTS

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE: BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_2OTHER	*	=50MIL_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL_SPACING	*	1.27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_DIFF_T	*	*	ENET_2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USR_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3:1_SPACING	?	USB	TOP,BOTTOM	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
ENET_50S	ENET_SE	ENET RDAC	37
CLK_RCH_55S	XTAL	ENET_CLK25M XTALI	36 37
CLK_RCH_55S	XTAL	ENET_CLK25M XTALO	36 37
CLK_RCH_55S	XTAL	ENET_CLK25M XTALO_R	36
ENET_100D	ENET_DIFF	ENETCONN MDI P<3..0>	37 38
ENET_100D	ENET_DIFF	ENETCONN MDI N<3..0>	37 38
ENET_100D	ENET_DIFF_T	ENETCONN MDI T P<3..0>	38
ENET_100D	ENET_DIFF_T	ENETCONN MDI T N<3..0>	38
PCIE_85D	ENET_MII	PCIE ENET R2D P	37
PCIE_85D	ENET_MII	PCIE ENET R2D N	37
PCIE_85D	ENET_MII	PCIE ENET D2R P	18 37
PCIE_85D	ENET_MII	PCIE ENET D2R N	18 37
PCIE_85D	ENET_MII	PCIE ENET R2D C P	18 37
PCIE_85D	ENET_MII	PCIE ENET R2D C N	18 37
PCIE_85D	ENET_MII	PCIE ENET D2R C P	37
PCIE_85D	ENET_MII	PCIE ENET D2R C N	37
SD_50S	SN	ENET SD CMD	37
SD_50S	SN	SDCONN CMD	37 45
SD_50S	SN	SDCONN CLK	37 45
SD_50S	SN	ENET SD CLK	37
SD_50S	SN	SDCONN DATA<7..0>	37 45
SD_50S	SN	ENET_CR DATA<7..0>	37
SD_50S	SN	ENET MEDIA SENSE	15 18 37
SD_50S	SN	ENET MEDIA SENSE R	
SD_50S	SN	ENET SD DETECT L	37
SD_50S	SN	SDCONN DETECT BUF L	97

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
USR_90D	USR	USB EXTRA P	34 43
USR_90D	USR	USB EXTRA N	34 43
USR_90D	USR	USB PORT0 P	43
USR_90D	USR	USB PORT0 N	43
USR_90D	USR	USB EXTR P	35 43
USR_90D	USR	USB EXTR N	35 43
USR_90D	USR	USB PORT1 P	43
USR_90D	USR	USB PORT1 N	43
USR_90D	USR	USB EXTC P	34 43
USR_90D	USR	USB EXTC N	34 43
USR_90D	USR	USB PORT2 P	43
USR_90D	USR	USB PORT2 N	43
USR_90D	USR	USB EXT D P	35 43
USR_90D	USR	USB EXT D N	35 43
USR_90D	USR	USB D MIXED P	43
USR_90D	USR	USB D MIXED N	43
USR_90D	USR	USB PORT3 P	43
USR_90D	USR	USB PORT3 N	43
USR_90D	USR	USB CAMERA P	20 44
USR_90D	USR	USB CAMERA L P	20 44
USR_90D	USR	USB CAMERA L N	44 98
USR_90D	USR	USB BT P	35 44
USR_90D	USR	USB BT N	35 44
USR_90D	USR	USB BT L P	44 98
USR_90D	USR	USB BT L N	44 98
USR_90D	USR	USR IR P	34 44
USR_90D	USR	USR IR N	34 44
USR_90D	USR	USR IR L P	44 98
USR_90D	USR	USR IR L N	44 98
USR_90D	USR	USR SDCARD P	34 44
USR_90D	USR	USR SDCARD N	34 44
USR_90D	USR	USR SDCARD L P	44
USR_90D	USR	USR SDCARD L N	44
USR_90D	USR	USB HUB1 UP P	20 34
USR_90D	USR	USB HUB1 UP N	20 34
USR_90D	USR	USB HUB2 UP P	20 35
USR_90D	USR	USB HUB2 UP N	20 35
USR_90D	USR	USB HUB2UNUSED P	35
USR_90D	USR	USB HUB2UNUSED N	35

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
FW_110D	FW_TP	FW CLK24P576M XO	39
FW_110D	FW_TP	FW CLK24P576M XO R	39
FW_110D	FW_TP	FW CLK24P576M XI	39
FW_110D	FW_TP	FW PORT0 TPA P	40 41
FW_110D	FW_TP	FW PORT0 TPA N	40 41
FW_110D	FW_TP	FW PORT0 TPB P	40 41
FW_110D	FW_TP	FW PORT0 TPB N	40 41
FW_110D	FW_TP	FW P1 TPA P	39 40
FW_110D	FW_TP	FW P1 TPA N	39 40
FW_110D	FW_TP	FW P2 TPA P	39 40
FW_110D	FW_TP	FW P2 TPA N	39 40
FW_110D	FW_TP	FW P1 TPB P	39 40
FW_110D	FW_TP	FW P1 TPB N	39 40
FW_110D	FW_TP	FW P2 TPB P	39 40
FW_110D	FW_TP	FW P2 TPB N	39 40

SYNC MASTER=K62 SYNC DATE=01/06/2011

USB/ENET/SD/FW/AUD CONSTRAINTS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET
 ASSIGNED IN CONT. MGR. NET_TYPE

PHYSICAL	SPACING	NET	TYPE
DP_85D	DISPLAYPORT	DP INTCONN ML C P<3..0>	83
DP_85D	DISPLAYPORT	DP INTCONN ML C N<3..0>	83
DP_85D	DISPLAYPORT	DP INTCONN AUXCH C P	83
DP_85D	DISPLAYPORT	DP INTCONN AUXCH C N	83
DP_85D	DISPLAYPORT	DP INTPNL ML P<3..0>	81 83
DP_85D	DISPLAYPORT	DP INTPNL ML N<3..0>	81 83
DP_85D	DISPLAYPORT	DP INTPNL AUX P	81 83
DP_85D	DISPLAYPORT	DP INTPNL AUX N	81 83
DP_85D	DISPLAYPORT	DP EXTA ML P<3..0>	84
DP_85D	DISPLAYPORT	DP EXTA ML N<3..0>	84
DP_85D	DISPLAYPORT	DP EXTA AUXCH P	84
DP_85D	DISPLAYPORT	DP EXTA AUXCH N	84
DP_85D	DISPLAYPORT	DP EXTA ML C P<3..0>	78 84
DP_85D	DISPLAYPORT	DP EXTA ML C N<3..0>	78 84
DP_85D	DISPLAYPORT	DP EXTA AUXCH C P	78 84
DP_85D	DISPLAYPORT	DP EXTA AUXCH C N	78 84
DP_85D	DISPLAYPORT	DP EXTB ML P<3..0>	83
DP_85D	DISPLAYPORT	DP EXTB ML N<3..0>	83
DP_85D	DISPLAYPORT	DP EXTB AUXCH P	83
DP_85D	DISPLAYPORT	DP EXTB AUXCH N	83
DP_85D	DISPLAYPORT	DP EXTB ML C P<3..0>	75 78
DP_85D	DISPLAYPORT	DP EXTB ML C N<3..0>	75 78
DP_85D	DISPLAYPORT	DP EXTB AUXCH C P	75 78
DP_85D	DISPLAYPORT	DP EXTB AUXCH C N	75 78
DP_85D	DISPLAYPORT	MXM DP B ML P<3..0>	75 78
DP_85D	DISPLAYPORT	MXM DP B ML N<3..0>	75 78
DP_85D	DISPLAYPORT	MXM DP B AUX P	75 78
DP_85D	DISPLAYPORT	MXM DP B AUX N	75 78
DP_85D	DISPLAYPORT	MXM DP C ML P<3..0>	75 83
DP_85D	DISPLAYPORT	MXM DP C ML N<3..0>	75 83
DP_85D	DISPLAYPORT	MXM DP C AUX P	75 83
DP_85D	DISPLAYPORT	MXM DP C AUX N	75 83
DP_85D	DISPLAYPORT	MXM DP C AUX R P	83
DP_85D	DISPLAYPORT	MXM DP C AUX R N	83
DP_85D	DISPLAYPORT	MXM DP D ML P<3..0>	75 78
DP_85D	DISPLAYPORT	MXM DP D ML N<3..0>	75 78
DP_85D	DISPLAYPORT	MXM DP D AUX P	75 78
DP_85D	DISPLAYPORT	MXM DP D AUX N	75 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

DP_85D	DISPLAYPORT	MXM LVDS A CLK P	76 78
DP_85D	DISPLAYPORT	MXM LVDS A CLK N	76 78
DP_85D	DISPLAYPORT	MXM LVDS B CLK P	76 78
DP_85D	DISPLAYPORT	MXM LVDS B CLK N	76 78
DP_85D	DISPLAYPORT	MXM LVDS A DATA P<3..0>	76 78
DP_85D	DISPLAYPORT	MXM LVDS A DATA N<3..0>	76 78
DP_85D	DISPLAYPORT	MXM LVDS B DATA P<3..0>	76 78
DP_85D	DISPLAYPORT	MXM LVDS B DATA N<3..0>	76 78

D
C
B
A

D
C
B
A

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

GRAPHICS CONSTRAINTS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_555	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPER1	NET_SPACING_TYPER2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
	SMB_555	SMB		SMBUS SMC A S3 SCL	49
	SMB_555	SMB		SMBUS SMC A S3 SDA	49
	SMB_555	SMB		SMBUS SMC B S0 SCL	49
	SMB_555	SMB		SMBUS SMC B S0 SDA	49
	SMB_555	SMB		SMBUS SMC 0 S0 SCL	49
	SMB_555	SMB		SMBUS SMC 0 S0 SDA	49
	SMB_555	SMB		SMBUS SMC BSA SCL	49
	SMB_555	SMB		SMBUS SMC BSA SDA	49
	SMB_555	SMB		SMBUS SMC MGMT SCL	49 94
	SMB_555	SMB		SMBUS SMC MGMT SDA	49 94
	SMB_555	SMB		SMBUS SMC MGMT SCL	49 94
	SMB_555	SMB		SMBUS SMC MGMT SDA	49 94
	SMB_555	SMB		SMBUS PCH CLK	18 49
	SMB_555	SMB		SMBUS PCH DATA	18 49
	SMB_555	SMB		SML PCH 0 CLK	18 49
	SMB_555	SMB		SML PCH 0 DATA	18 49
	SMB_555	SMB		SML PCH 1 CLK	18 49
	SMB_555	SMB		SML PCH 1 DATA	18 49
	CLK_XTAL	XTAL		SMC_XTAL	46 47
	CLK_XTAL	XTAL		SMC_XTAL	46 47
	SMB_555	SMB		I2C VREFMRGN DIMMA SCL	28
	SMB_555	SMB		I2C VREFMRGN DIMMA SDA	28
	SMB_555	SMB		I2C VREFMRGN DIMMB SCL	28
	SMB_555	SMB		I2C VREFMRGN DIMMB SDA	28
	SMB_555	SMB		SMB_BLC TCON SCL	6 49 81
	SMB_555	SMB		SMB_BLC TCON SDA	6 49 81
	SMB_555	SMB		I2C TCON SCL	81
	SMB_555	SMB		I2C TCON SDA	81
	SMB_555	SMB		SMB_BLC PCH SCL R	6
	SMB_555	SMB		SMB_BLC PCH SDA R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
	THERM_DIFF	THERMAL		SNS T1 1 P	52
	THERM_DIFF	THERMAL		SNS T1 1 N	52
	THERM_DIFF	THERMAL		SNS T2 DP2	52
	THERM_DIFF	THERMAL		SNS T2 DN2	52
	THERM_DIFF	THERMAL		SNS T1 2 P	52
	THERM_DIFF	THERMAL		SNS T1 2 N	52
	THERM_DIFF	THERMAL		SNS T1 3 P	52
	THERM_DIFF	THERMAL		SNS T1 3 N	52
	THERM_DIFF	THERMAL		SNS T1 4 P	52
	THERM_DIFF	THERMAL		SNS T1 4 N	52
	THERM_DIFF	THERMAL		SNS T1 5 P	52
	THERM_DIFF	THERMAL		SNS T1 5 N	52
	THERM_DIFF	THERMAL		SNS T1 6 P	52
	THERM_DIFF	THERMAL		SNS T1 6 N	52
	THERM_DIFF	THERMAL		SNS T1 7 P	52
	THERM_DIFF	THERMAL		SNS T1 7 N	52
	THERM_DIFF	THERMAL		SNS CPU THERMD P	10 52
	THERM_DIFF	THERMAL		SNS CPU THERMD N	10 52
	THERM_DIFF	THERMAL		SNS LCD H P	52
	THERM_DIFF	THERMAL		SNS LCD H N	52
	THERM_DIFF	THERMAL		SNS ODD P	52 98
	THERM_DIFF	THERMAL		SNS ODD N	52 98
	THERM_DIFF	THERMAL		SNS CPU H P	52
	THERM_DIFF	THERMAL		SNS CPU H N	52
	THERM_DIFF	THERMAL		SNS SKIN RIGHT P	52 98
	THERM_DIFF	THERMAL		SNS SKIN RIGHT N	52 98
	THERM_DIFF	THERMAL		SNS SKIN LEFT P	44 52 98
	THERM_DIFF	THERMAL		SNS SKIN LEFT N	44 52 98
	THERM_DIFF	THERMAL		SNS AMB P	52 54 98
	THERM_DIFF	THERMAL		SNS AMB N	52 54 98
	THERM_DIFF	THERMAL		SNS MXM P	52
	THERM_DIFF	THERMAL		SNS MXM N	52
	THERMAL			HDD OOB TEMP FLT	42 51 98
	THERMAL			HDD OOB TEMP FB	42
	THERMAL			HDD OOB TEMP R	51
	THERMAL			SMC HDD OOB TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
	THERM_DIFF	THERMAL		SNS I MXM P	50
	THERM_DIFF	THERMAL		SNS I MXM N	50
	THERM_DIFF	THERMAL		SNS DIMM 1V5 P	50
	THERM_DIFF	THERMAL		SNS DIMM 1V5 N	50
	SNS_DIFF	THERMAL		VR ISNS VCORE P	50 95
	SNS_DIFF	THERMAL		VR ISNS VCORE N	50 95
	SNS_DIFF	THERMAL		VR ISNS VAXG P	50 95
	SNS_DIFF	THERMAL		VR ISNS VAXG N	50 95
	SNS_DIFF	THERMAL		VR ISNS 1V05 P	95
	SNS_DIFF	THERMAL		VR ISNS 1V05 N	95
	THERM_DIFF	THERMAL		SNS CPU 1V5 P	50
	THERM_DIFF	THERMAL		SNS CPU 1V5 N	50
	THERM_DIFF	THERMAL		SNS VCCSA P	50
	THERM_DIFF	THERMAL		SNS VCCSA N	50
	THERM_DIFF	THERMAL		SNS 1V05 PCH P	50
	THERM_DIFF	THERMAL		SNS 1V05 PCH N	50
	THERMAL			GND SMC AVSS	46 47 50 94
	THERMAL			SMC CPU 1V5 ISENSE	46 50
	THERMAL			SMC CPU 1V5 ISENSE R	50
	THERMAL			SMC CPU 1V5 VSENSE	46 50
	THERMAL			GND SMC AVSS	46 47 50 94
	THERMAL			SMC DIMM ISENSE	46 50
	THERMAL			SMC DIMM 1V5 R	50
	THERMAL			SMC DIMM VSENSE	46 50
	THERMAL			GND SMC AVSS	46 47 50 94
	THERMAL			SMC VCCSA ISENSE	46 50
	THERMAL			SMC VCCSA ISENSE R	50
	THERMAL			SMC VCCSA VSENSE	46 50
	THERMAL			GND SMC AVSS	46 47 50 94
	THERMAL			SMC PCH 1V05 ISENSE	46 50
	THERMAL			SMC VAXG VSENSE	46 50
	THERMAL			SMC PCH 1V05 VSENSE	46 50
	THERMAL			GND SMC AVSS	46 47 50 94
	THERMAL			SMC 1V05 ISENSE	46 50
	THERMAL			SMC VAXG ISENSE	46 50
	THERMAL			SMC 1V05 VSENSE	46 50
	THERMAL			SMC GPU ISENSE	46 50
	THERMAL			SMC GPU VSENSE	46 50
	THERMAL			SMC VCORE ISENSE	46 50
	THERMAL			SMC VCORE VSENSE	46 50
	THERMAL			SMC CPU VSENSE	

SYNC MASTER=K62 SYNC DATE=01/06/2011

SMC Constraints

Apple Inc.

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Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include SWITCHNODE, POWER, GND, and *.

POWER NET PROPERTIES

SENSING NET PROPERTIES

VR CTRL NET PROPERTIES

VR CTRL NET PROPERTIES

POWER NET PROPERTIES

Table with 4 columns: NET_TYPE, PHYSICAL, SPACING, VOLTAGE. Lists various power nets like PP12V_S0_MXM, PP12V_SLG1, PP3V3R12V_SW_DPAPWR_1, etc.

Table with 4 columns: NET_TYPE, PHYSICAL, SPACING, VOLTAGE. Lists various sensing nets like PP12V_S0_MXM, PP12V_SLG1, PP3V3R12V_SW_DPAPWR_1, etc.

Table with 4 columns: NET_TYPE, PHYSICAL, SPACING. Lists various sensing nets like VR_CPU_ISNS1_P, VR_CPU_ISNS1_R_N, etc.

Table with 4 columns: NET_TYPE, PHYSICAL, SPACING. Lists various VR control nets like VR_CPU_P1_SNUB, VR_CPU_P2_SNUB, etc.

Table with 4 columns: NET_TYPE, PHYSICAL, SPACING. Lists various VR control nets like VR_CTL_PHY, VR_CTL_SW, etc.

Table with 4 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET, SPACING_RULE_SET. Lists physical and spacing rules.

VR VID NET PROPERTIES

Table with 4 columns: NET_TYPE, PHYSICAL, SPACING. Lists various VR VID nets like CPU_VIDCLK_R, CPU_VIDALERT_L_R, etc.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Lists spacing rules for VR_CTL_VIDS.

POWER CONSTRAINTS header with Apple logo, drawing number 051-8115, revision 11.1.0, and a notice of proprietary property.

T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?	T29	TOP,BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_XTAL_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2X_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
NO_TEST=TRUE	T29_90D	T29	T29_R2D C P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_R2D C N<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_D2R C P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_D2R C N<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_R2D P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_R2D N<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_D2R P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_D2R N<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_R2D C F P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29_R2D C F N<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPA ML P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPA ML N<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPB ML P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPB ML N<3..0>
NO_TEST=TRUE	T29_90D	T29	DP A EXT AUXCH P
NO_TEST=TRUE	T29_90D	T29	DP A EXT AUXCH N
NO_TEST=TRUE	T29_90D	T29	DP SDRVA AUXCH C P
NO_TEST=TRUE	T29_90D	T29	DP SDRVA AUXCH C N
NO_TEST=TRUE	T29_90D	T29	DP SDRVB AUXCH C P
NO_TEST=TRUE	T29_90D	T29	DP SDRVB AUXCH C N
NO_TEST=TRUE	T29_90D	T29	DP B EXT AUXCH P
NO_TEST=TRUE	T29_90D	T29	DP B EXT AUXCH N
NO_TEST=TRUE	T29_90D	T29	T29DPA D2R1 AUXCH P
NO_TEST=TRUE	T29_90D	T29	T29DPA D2R1 AUXCH N
NO_TEST=TRUE	T29_90D	T29	T29DPB D2R3 AUXCH P
NO_TEST=TRUE	T29_90D	T29	T29DPB D2R3 AUXCH N
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C N<0>
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C P<0>
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C N<2>
NO_TEST=TRUE	T29_90D	T29	T29DPA ML C P<2>
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C N<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C P<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C N<2>
NO_TEST=TRUE	T29_90D	T29	T29DPB ML C P<2>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 R2D P<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 R2D N<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 D2R P<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 D2R N<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML P<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC ML N<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0>
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH R C P
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH R C N
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA AUXCH P
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA AUXCH N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB AUXCH P
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB AUXCH N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML C P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML C N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML R P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVA ML R N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML C P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML C N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML R P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP SDRVB ML R N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 A RSVD N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 A RSVD P
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 B RSVD N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29 B RSVD P

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
T29_SPI_55S	T29_SPI	T29_SPI	JTAG T29 TDI
T29_SPI_55S	T29_SPI	T29_SPI	JTAG T29 TMS
T29_SPI_55S	T29_SPI	T29_SPI	JTAG T29 TCK
T29_SPI_55S	T29_SPI	T29_SPI	JTAG T29 TDO
T29_SPI_55S	T29_SPI	T29_SPI	T29_SPI MOSI
T29_SPI_55S	T29_SPI	T29_SPI	T29_SPI MISO
T29_SPI_55S	T29_SPI	T29_SPI	T29_SPI CS L
T29_SPI_55S	T29_SPI	T29_SPI	T29_SPI CLK
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M T29
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M T29 R
T29_SMB_55S	T29_SMB	T29_SMB	I2C T29 SDA
T29_SMB_55S	T29_SMB	T29_SMB	I2C T29 SCL
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M SB
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M ENET
CLK_25M_55S	CLK_25M	CLK_25M	ENET CLK25M XTALI OSC
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M T29 CLK
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M T29
CLK_25M_55S	CLK_25M	CLK_25M	SYSCLK CLK25M T29 R
T29_XTAL_100D	T29_XTAL	T29_XTAL	SYSCLK CLK25M X2
T29_XTAL_100D	T29_XTAL	T29_XTAL	SYSCLK CLK25M X2 R
T29_XTAL_100D	T29_XTAL	T29_XTAL	SYSCLK CLK25M X1
T29_COMP	T29_COMP	T29_COMP	T29 RBIAS
T29_COMP	T29_COMP	T29_COMP	T29 A BIAS
T29_COMP	T29_COMP	T29_COMP	T29 B BIAS
T29_COMP	T29_COMP	T29_COMP	DP A BIAS

SYNC MASTER=K62 SYNC DATE=01/06/2011

T29 CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE			
PHYSICAL	SPACING		
PM		4V5_REG_EN	56
PM		3V42G3H_SHDN_L	72
PM		ALL_SYS_PWRGD_R	5 32 64
PM		ALL_SYS_PWRGD_SMC	46 64
PM		AP_PWR_EN	30 26 33
PM		AP_MINI_RESET_L	33
PM		AUD_I2C_INT_L	20 62
PM		AUD_IP_PERIPHERAL_DET	20 61
PM		AUD_IPHS_SWITCH_EN	21 62
PM		AUD_SPDIF_IN	60 83 91
PM		AUD_SPDIF_IN_CODEC	56 83
PM		BDV_BKL_PWM	46 83 97
PM		BL_PWM	6 83
PM		BL_EN	6 83
PM		BDV_BKL_PWM	46 83 97
PM		CK505_27MHZ_EN	26
PM		CPUVTT_REG_EN	
PM_VTT		CPUVTT_REG_PGOOD_R	63
PM		CPU_MEM_RESET_L	11 32
PM		CPU_PECI_R	46
PM_VTT		CPU_PWRGD	11 21 25
PM		CPU_RESET_L	11 27
PM		CPU_SKTOCC_L	11 63
PM		CPU_CATERR_L	11
PM		CPU_PECI	11 21 46
PM		CPU_PROCHOT_L	11 47 65
PM		CPU_THRMTRIP_L	11 47
PM		CPU_PROC_SEL	11 19
PM		DEBUG_RESET_L	27 48
PM		DDRVTN_EN	81 83
PM		DP_INT_SPDIF_AUDIO	81 83
PM		DP_INTENL_HPD	81 83
PM		3V3R2V9_DPAEWR_ADJ	82 96
PM		DP_A_PWRDN	82
PM		DP_A_PWRDN_FET_R	82
PM		DP_A_PWRDN_INV	82
PM		DPAPWRSG_HVEN_L_R	82
PM		DPAPWRSG_CT	82
PM		DPAPWRSG_ILIM	82
PM		DPAPWRSG_ILIT	82
PM		T29_A_HV_EN	82 84
PM		3V3R2V9_DPBWR ADJ	82 84
PM		DP_B_PWRDN	82
PM		DP_B_PWRDN_FET_R	82
PM		DP_B_PWRDN_INV	82
PM		DPBWRSG_HVEN_L_R	82
PM		DPBWRSG_CT	82
PM		DPBWRSG_ILIM	82
PM		DPBWRSG_ILIT	82
PM		T29_B_HV_EN	18 80 97
PM		T29_PWR_EN	18 80 97
PM		T29_RESET_RTR_L	80 86
PM		LCD_BLK_ON_DLY	83
PM		LCD_BLK_PWM	83
PM		MXM_PNL_BLK_PWM	76 83

NET_TYPE			
PHYSICAL	SPACING		
PM		ENET_PWR_EN	30 25 36
PM		ENET_LOW_PMR	15 21 37
PM		FW_RESET_L	27 39
PM		ENET_RESET_L	27 36
PM		FW_PME_L	15 21 39
PM		FW_PWR_EN	15 21
PM		FW_CLKREQ_L	15 39
PM		ISOLATE_CPU_MEM_L	21 25 32
PM		LPC_PWRDN_L	19 46 48
PM		MEM_RESET_L	30 31 32 89
PM		MINI_CLKREQ_L	15 33
PM		MINI_RESET_L	27 33
PM		MXM_CLKREQ_L	9 75
PM		MXM_GOOD	5 21 25
PM		ODD_PWR_EN_L	15 21 42
PM		RTC_RESET_L	18 27 97
PM		RSRST_PWRGD	46 64
PM		RTC_RESET_L	18 27 97
PM		S4_ENABLES	63
PM		SDCONN_STATE_RST_L	
PM		SDCONN_DETECT_BUF_L	92
PM		SDCONN_STATE_CHANGE	20 26 48
PM		SDCARD_RESET	15 21 44 98
PM		SDCARD_RESET_L	44
PM		SDCARD_PLT_RST_L	27 44
PM		SDCARD_PLT_RST_L_R	
PM		SMC_PM_G2_EN	46 74
PM		SMC_PM_G2_EN_R	74
PM		SMC_PM_G2_EN_L	74
PM		S5_DG_1	74
PM		S5_MSFT_G1	74
PM		USE_HDD_OOB_L	20 51
PM		HDD_OOB_1V00_REF	51
PM		SMC_ADAPTER_EN	19 46 47
PM		SMC_RUNTIME_SCI_L	21 46 47
PM		SMC_WAKE_SCI_L	15 18 21 46
PM		SMC_DELAYED_PWRGD	47 64
PM		SMC_LRESET_L	27 46
PM		SMC_RESET_L	46 47 48
PM		SMC_PROCHOT	46 47
PM		SMC_PROCHOT_3_3_L	46 47
PM		SMC_ONOFF_L	46 47
PM		SMC_MANUAL_RST_L	47
PM		SPI_DESCRIPTOR_OVERRIDE_L	18 46
PM		T29_PWR_EN	18 80 97
PM		T29_RESET_L	27 80
PM		T29_DP_PORTA_PWR_EN	20 25 82 91
PM		T29_DP_PORTA_PWR_EN_REG	82
PM_VTT		XDP_CPUPWRGD	
PM_VTT		XDP_DBRESET_L	11 25
PM_VTT		XDP_PWRGD	
PM		XDPPCH_PLTRST_L	25 27
PM		USB_HUB_SOFT_RESET_L	20 25 34
PM		VSYNC_DP_CONN	6 81
PM		VSYNC_DP	81
PM		VIDEO_ON	81
PM		VTT_REG_PGOOD_L	63

NET_TYPE			
PHYSICAL	SPACING		
PM		PLT_RESET_L	20 27
PM_VTT		PLT_RESET_LS1V05_L	11
PM		PM_BATLOW_L	15 19 46
PM		PM_CLK32K_SUSCLK	9 46 91
PM		PM_CLK32K_SUSCLK_R	9 19 91
PM		PM_CLKRUN_L	15 19 46 48
PM		PM_PWRBTN_L	19 25 46
PM		PM_RSMRST_L	27 46
PM		PM_RSMRST_PCH_L	19 27
PM		PCH_SRTCST_L	18
PM		PCH_INTVRMEN_L	18
PM		PCH_DSWVRMEN	19
PM		PCH_DF_TVS	19
PM		PCH_PROCPWRGD	21
PM		PCIE_WAKE_L	19 33 36 78
PM		PM_DSW_PWRGD	19
PM		PM_ASW_PWRGD	19 64
PM		PM_MEM_PWRGD_R	11
PM		PM_EN_DDR1V5_S3_REG	63 71
PM		PM_EN_DDRVTT_S0_REG	32 63 71
PM		PM_EN_P12V_S0_FET	6 63
PM		PM_EN_P1V05_S0_REG	63 68
PM		PM_EN_P1V05_S3_REG	
PM		PM_EN_P1V5_S0_FET	63 73
PM		PM_EN_P1V8_S0_REG	63 71
PM		PM_EN_P3V3_S0_FET	63 73
PM		PM_EN_P3V3_S3_FET	63 73
PM		PM_EN_P3V3_S5_REG	70
PM		PM_EN_P5V_S0_FET	63 73
PM		PM_EN_P5V_S3_REG	63 70
PM		PM_EN_PVCCSA_S0_REG_L	64
PM		PM_EN_VCCSA_S0_CPU	
PM		PM_EN_PVCCORE_CPU	63 65
PM_VTT		PM_MEM_PWRGD	11 19 97
PM		PM_MXM_EN	64 76
PM		PM_PCH_PWRGD_R	64
PM		PM_PECI_PWRGD	46 64
PM		PM_PECI_PWRGD_R	46
PM		PM_PGOOD_DDR1V5_S3_REG	5 63 71
PM		PM_PGOOD_P1V05_S0_REG	63 64 68
PM		PM_PGOOD_P1V5_S0_FET	11 64 73
PM		PM_PGOOD_P1V8_S0_REG	64 71
PM		PM_PGOOD_P3V3_S0_FET	63 64 73
PM		PM_PGOOD_P3V3_S3_FET	34 73
PM		PM_PGOOD_P3V3_S5_REG	27 64 70
PM		PM_PGOOD_P5V_S0_FET	63 64 73
PM		PM_PGOOD_MINI	33
PM		PM_PGOOD_PVCCORE_CPU	5 25 64 65
PM		PM_PGOOD_PVCCSA_S0_REG	63 64
PM		PM_PGOOD_P5V_S3_REG	63 70 82
PM		PM_PGOOD_PVAXG	5 65
PM_VTT		PM_MEM_PWRGD	11 19 97
PM		PM_MEM_PWRGD_L	11
PM		PM_MXM_PGOOD	64 76
PM		PM_PCH_PWRGD	19 21 64
PM		PM_SLP_S3_5V	32
PM		PM_SLP_S3_5V_L	32
PM		PM_SLP_S3_5V_R2	32
PM		PM_SLP_S3_L	5 19 26 32 36 46 47 63 82
PM		PM_SLP_S4_L	5 19 32 46 47 63 97
PM		PM_SLP_S5_L	5 19 46 47 63
PM_VTT		PM_SYNC	11 19
PM		PM_SYSRST_L	19 25 27 46
PM		PM_SYS_PWRGD	19 32 64
PM_VTT		PM_THRMTRIP_L	21 47
PM		PM_SLP_S3_BUF_L	63
PM		PM_SLP_S4_1_L_R	63
PM		PM_SLP_S4_D_L	32
PM		PM_SLP_S4_L	5 19 32 46 47 63 97
PM		PGOOD_P1V5_S0_DLY	11
PM		PGOOD_1V8_S0_G1	64
PM		PGOOD_1V8_S0_G2	64
PM		PGOOD_P12V_S0	63 64
PM		PGOOD_P1V8_S0	64
PM		PGOOD_PCH_S0	5 64
PM		PGOOD_PCH_S0_R	64 91
PM		PGOOD_SYSPWRK	64
PM		PGOOD_SYSPWRK_R	64
PM		POWER_BUTTON_L	47
PM		PEG_RESET_L	9 27
PM		PGOOD_CPU_S0	64
PM		PGOOD_CPU_UNCORE	64 91
PM		PGOOD_5V_1V05_3V3	64 91
PM		PGOOD_3V3_1V05	64 91
PM		PGOOD_12V_S0_G1	64
PM		PGOOD_12V_S0_G2	64
PM		9V_COMP_REF	64
PM		12V_COMP_REF	64
PM		ALL_SYS_PWRGD	64 91

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

95 4 **IN** PP5V_S3 MIN_ALLOWED_TPS=1 FUNC_TEST=TRUE
 92 44 **IN** USB_CAMERA_L_P FUNC_TEST=TRUE
 92 44 **IN** USB_CAMERA_L_N FUNC_TEST=TRUE
 92 44 **IN** USB_BT_L_P FUNC_TEST=TRUE
 92 44 **IN** USB_BT_L_N FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
 1 PP3V3_S3 TESTPOINT NEAR J4700
 6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

97 44 21 15 **IN** SD_CARD_RESET FUNC_TEST=TRUE
 1 PP3V3_S3 Testpoint near J4750
 2 Ground Testpoints near J4750

J4780 IR BOARD

92 44 **IN** USB_IR_L_P FUNC_TEST=TRUE
 92 44 **IN** USB_IR_L_N FUNC_TEST=TRUE
 95 44 **IN** PP5V_S3_IR_FLT FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42 **IN** SMC_ODD_DETECT FUNC_TEST=TRUE
 1 PP5V_S0 Testpoint near J4520
 1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

94 52 **IN** SNS_ODD_P FUNC_TEST=TRUE
 94 52 **IN** SNS_ODD_N FUNC_TEST=TRUE

J5600 ODD FAN

53 **IN** FAN_0_PWR_L FUNC_TEST=TRUE
 53 **IN** FAN_TACH0_L FUNC_TEST=TRUE
 95 53 **IN** PP12V_S0_FAN0_L FUNC_TEST=TRUE
 53 **IN** FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

54 **IN** FAN_2_PWR_L FUNC_TEST=TRUE
 54 **IN** FAN_TACH2_L FUNC_TEST=TRUE
 95 54 **IN** PP12V_S0_FAN2_L FUNC_TEST=TRUE
 54 **IN** FAN_2_GND FUNC_TEST=TRUE

94 54 52 **IN** SNS_AMB_P FUNC_TEST=TRUE
 94 54 52 **IN** SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53 **IN** FAN_1_PWR_L FUNC_TEST=TRUE
 53 **IN** FAN_TACH1_L FUNC_TEST=TRUE
 95 53 **IN** PP12V_S0_FAN1_L FUNC_TEST=TRUE
 53 **IN** FAN_1_GND FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

94 51 42 **IN** HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

94 52 44 **IN** SNS_SKIN_LEFT_P FUNC_TEST=TRUE
 94 52 44 **IN** SNS_SKIN_LEFT_N FUNC_TEST=TRUE

94 52 **IN** SNS_SKIN_RIGHT_P FUNC_TEST=TRUE
 94 52 **IN** SNS_SKIN_RIGHT_N FUNC_TEST=TRUE

J6602 AUDIO RIGHT SPEAKER

91 **IN** AUD_SPKR_OUTLO2R_POUHNC_TEST=TRUE
 91 **IN** AUD_SPKR_OUTLO2R_NOUHNC_TEST=TRUE
 91 **IN** AUD_SPKR_OUTLO1R_POUHNC_TEST=TRUE
 91 **IN** AUD_SPKR_OUTLO1R_NOUHNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

91 **IN** AUD_SPKR_OUTLO2L_POUHNC_TEST=TRUE
 91 **IN** AUD_SPKR_OUTLO2L_NOUHNC_TEST=TRUE
 91 **IN** AUD_SPKR_OUTLO1L_POUHNC_TEST=TRUE
 91 **IN** AUD_SPKR_OUTLO1L_NOUHNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

95 60 **IN** PP3V3_AUDIO_SPDIF_JACKHNC_TEST=TRUE
 2 TP'S
 MIN_ALLOWED_TPS=2

60 **IN** AUD_LI_DET_JACK FUNC_TEST=TRUE

60 **IN** AUD_LI_R_JACK FUNC_TEST=TRUE
 60 **IN** AUD_LI_GND_JACK FUNC_TEST=TRUE
 60 **IN** AUD_LI_L_JACK FUNC_TEST=TRUE

60 **IN** HS_MIC_HI_JACK FUNC_TEST=TRUE

60 **IN** AUD_HP_L_JACK FUNC_TEST=TRUE

60 **IN** AUD_HP_GND_JACK FUNC_TEST=TRUE

60 **IN** AUD_HP_R_JACK FUNC_TEST=TRUE

60 **IN** AUD_HP_TYDEDET_JACK FUNC_TEST=TRUE

60 **IN** AUD_IP_PERPH_JACK FUNC_TEST=TRUE

60 **IN** AUD_HP_TIPDET_JACK FUNC_TEST=TRUE

60 **IN** AUD_SPDIFIN_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

91 **IN** GND 17 TP'S
 MIN_ALLOWED_TPS=17

95 6 **IN** PP3V3_S3 2 TP'S
 MIN_ALLOWED_TPS=2

95 6 **IN** PP5V_S0
 MIN_ALLOWED_TPS=1

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