



# P72/73 (JUN 04 /2002)

BOMOPTION	P72 OASIS	P72 OASIS	P73 OASIS	P72 MIRAGE	P72 MIRAGE	P73 MIRAGE
	GOOD	BETTER	BEST	GOOD	BETTER	BEST
DD1X	X	X	X	X	X	X
DD2X						
600MHZ	X			X		
700MHZ		X	X		X	X
OASIS	X	X	X			
MIRAGE				X	X	X
MID OR HIGH RANGE NO PWRSTEP	X	X	X	X	X	X
HIGH_PLL_RANGE_NO_PWRSTEP						
MID OR HIGH RANGE PWRSTEP						
HIGH PLL PANGE PWRSTEP						
LOW PLL RANGE						
LOW OR MID PLL RANGE	X	X	X	X	X	X
FIREWIRE	X	X	X	X	X	X
NO FIREWIRE						
PWRSTEP						
NO PWRSTEP	X	X	X	X	X	X
100MHZ	X	X	X	X	X	X
66MHZ						
3SBAT	X	X		X	X	
4SBAT			X			X
SWCHG						
HWCHG	X	X	X	X	X	X
OASIS_600	X					
OASIS_700		X	X			
MIRAGE_600				X		
MIRAGE_700					X	X
INTUSB	X	X	X	X	X	X
NON PRODUCTION						
SLOW_CHRG	X	X		X	X	
FAST_CHRG			X			X
128M	X	X	X	X	X	X
256M						
TBEN						

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P. LEADER	APPROVED BY	CHECKED BY	PREPARED BY

PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
REV	1.C	1.0	1.B	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.B	1.B	1.0	1.0	1.0	1.0	1.C	1.0	1.0	1.0	1.0	1.0	1.0
DATE	0604	0312	0522	0312	0312	0312	0312	0312	0312	0312	0312	0312	0312	0522	0522	0312	0312	0312	0604	0312	0312	0312	0312	0312	0312	0312
27	28	29	30	31	32	33	34	35	36	37	38	39	39	41	42	43	44	45	46	47	48	49	50	51	52	53
1.0	1.B	1.0	1.0	1.0	1.0	1.A	1.0	1.B	1.0	1.0	1.B	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.C	1.0	1.0	1.0	1.0	1.0
0312	0502	0312	0312	0312	0312	0402	0312	0522	0312	0312	0522	0312	0312	0312	0312	0312	0312	0312	0312	0312	0604	0312	0312	0312	0312	0312

P/N:820-1320  
RFA # 222273  
ATC P/N:KK0U22701110U02  
ATC DRAWING NO.: U227-1-3-08

COVER PAGE (CONTENTS)

DESCRIPTION:  
iBook MLB & SCHEMATIC

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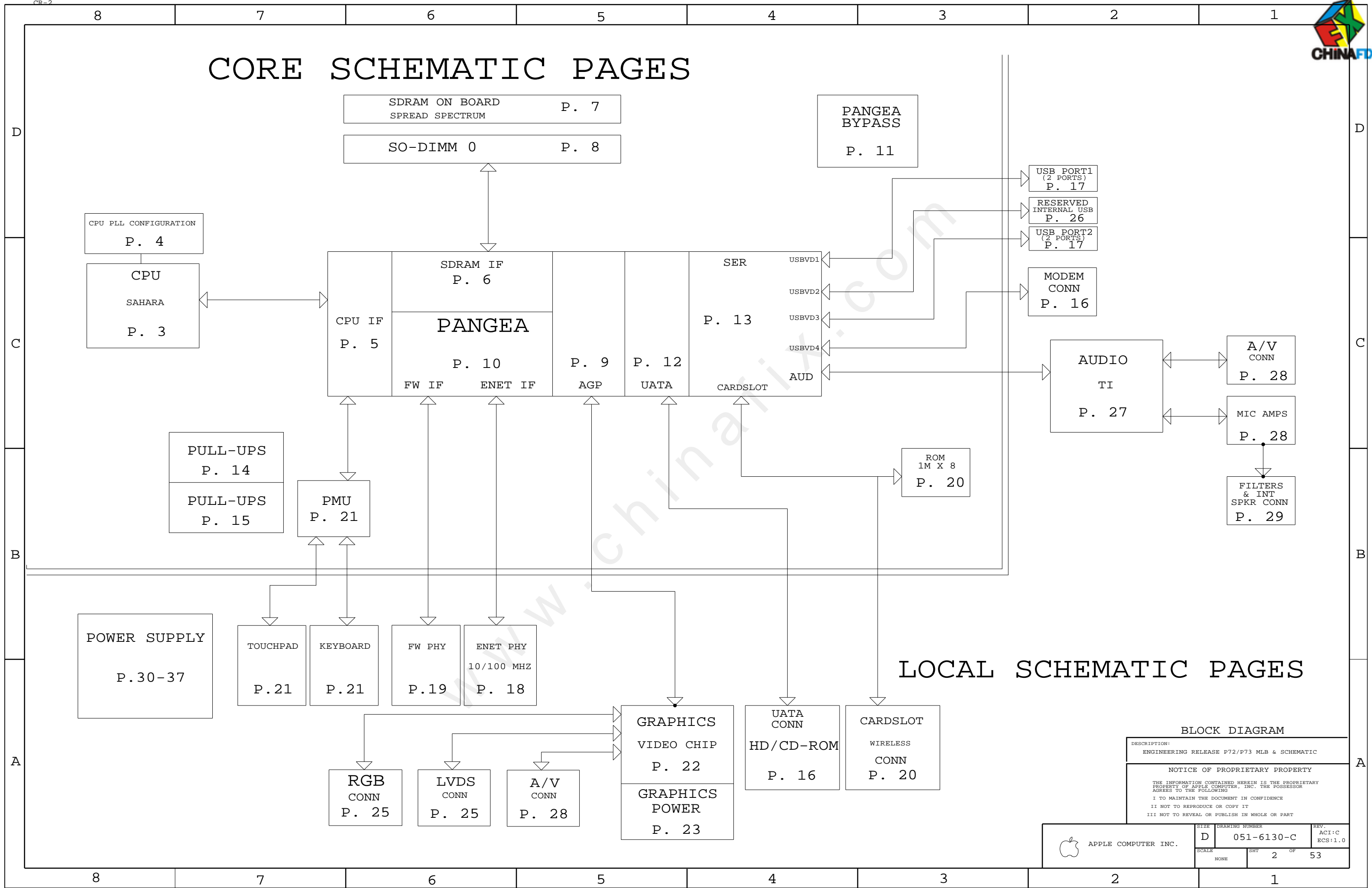
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		D	051-6130-C	ACI:C ECS:1.C
	SCALE	NONE	SHT	1 OF 53

# CORE SCHEMATIC PAGES



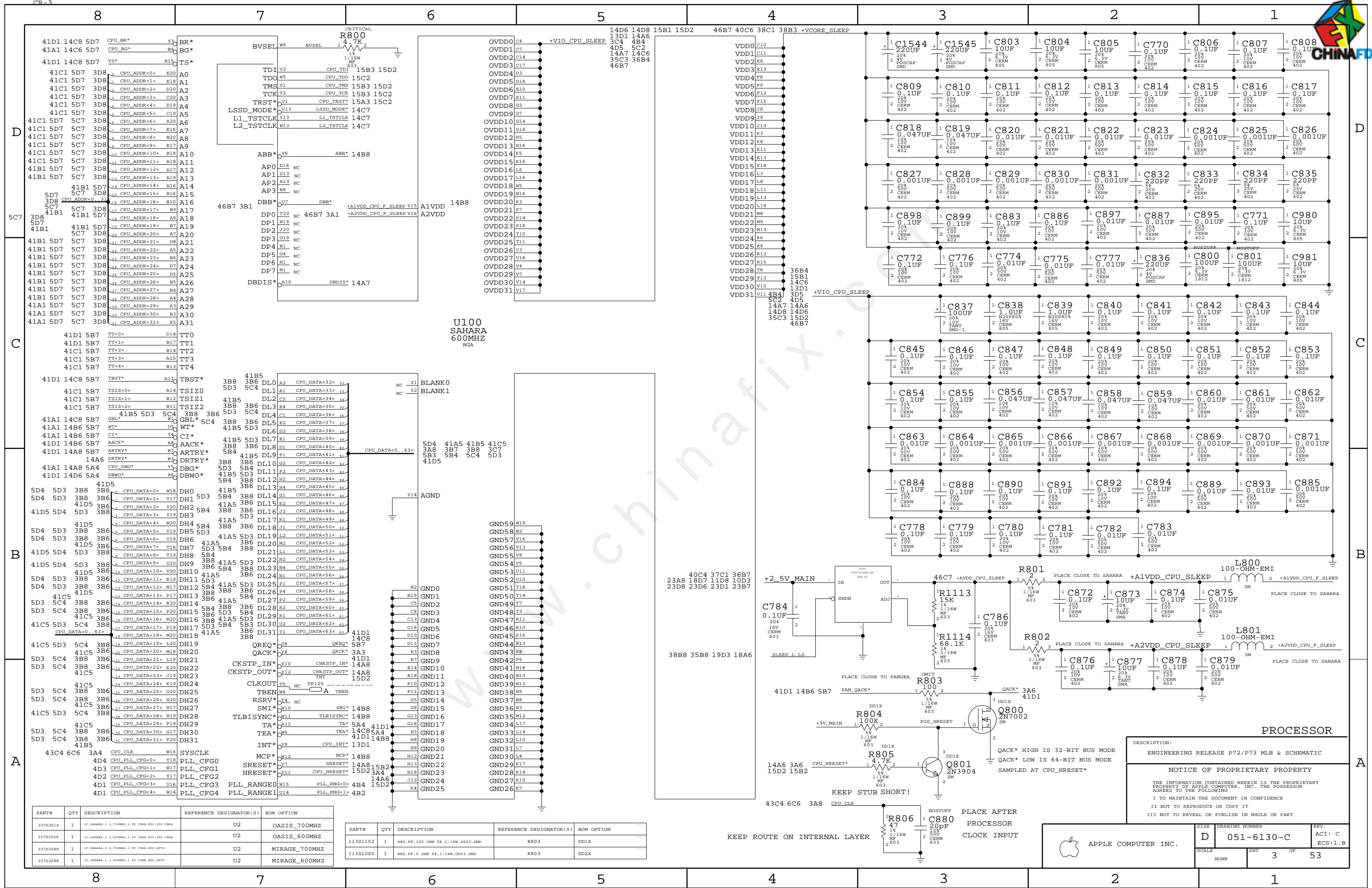
## LOCAL SCHEMATIC PAGES

**BLOCK DIAGRAM**

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ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

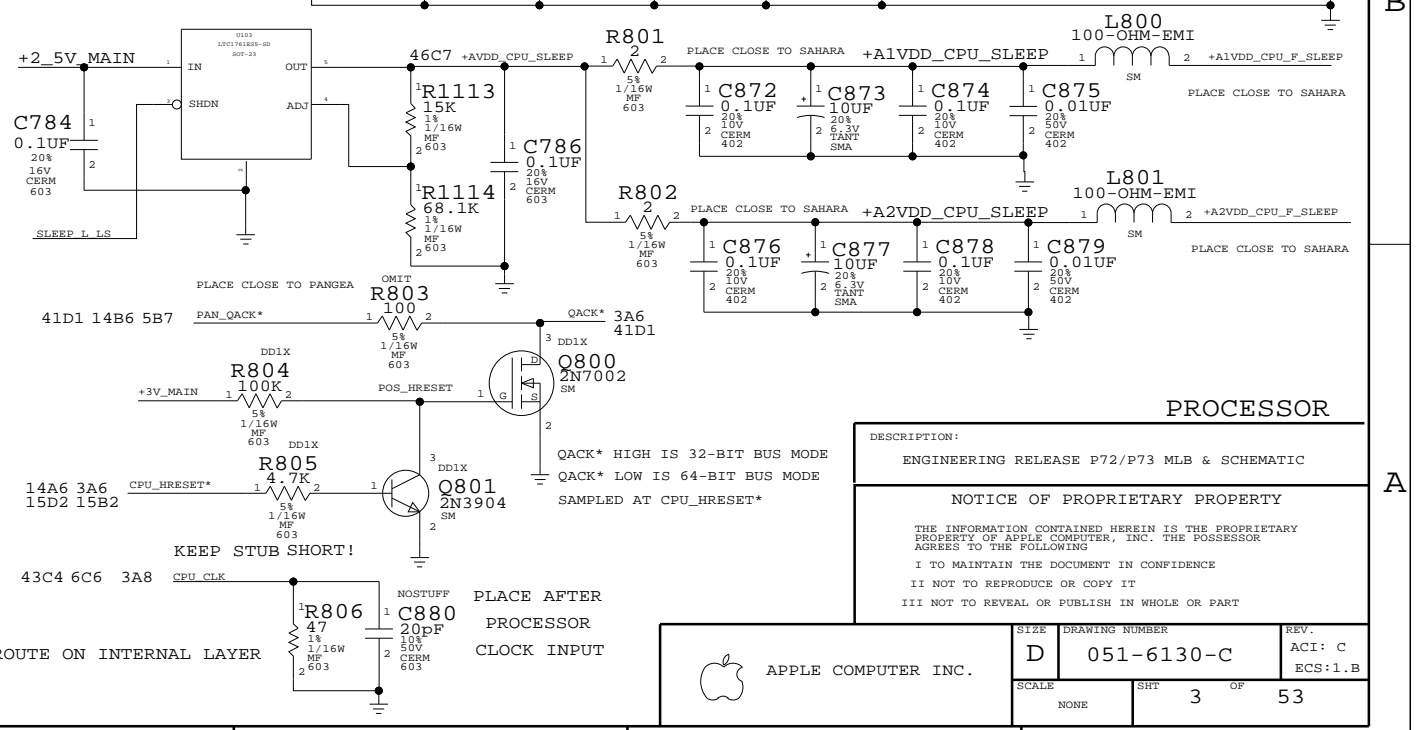
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	SCALE NONE	SHEET 2 OF 53	



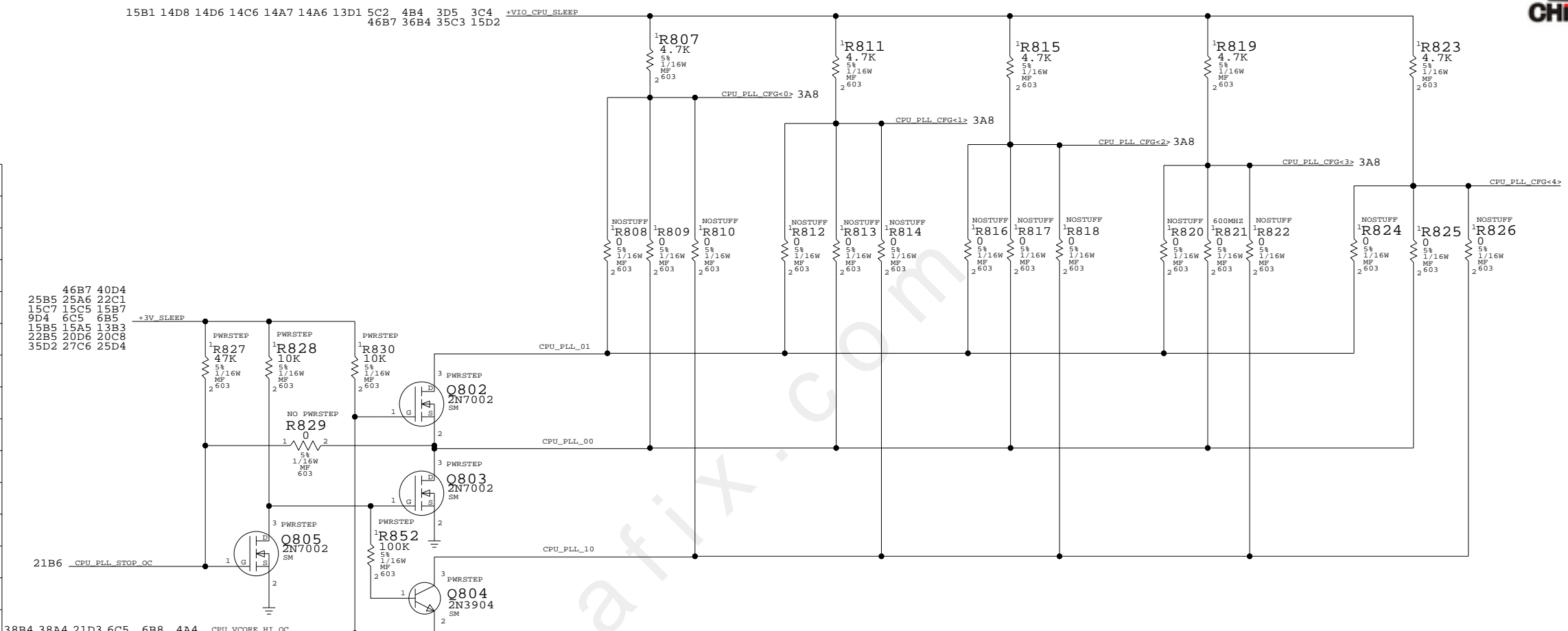
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
33782514	1	IC,SAHARA,1.2,700MHZ,1.5V CORE,85C,292 CPGA	U2	OASIS_700MHZ
33782509	1	IC,SAHARA,1.2,600MHZ,1.5V CORE,85C,292 CPGA	U2	OASIS_600MHZ
33782589	1	IC,SAHARA,1.2,700MHZ,1.5V CORE,85C,SF70	U2	MIRAGE_700MHZ
33782588	1	IC,SAHARA,1.2,600MHZ,1.5V CORE,85C,SF70	U2	MIRAGE_600MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11351102	1	RES,FF,100 OHM 5%,1/16W,0603,SMD	R803	DD1X
11351000	1	RES,FF,0 OHM 5%,1/16W,0603,SMD	R803	DD2X



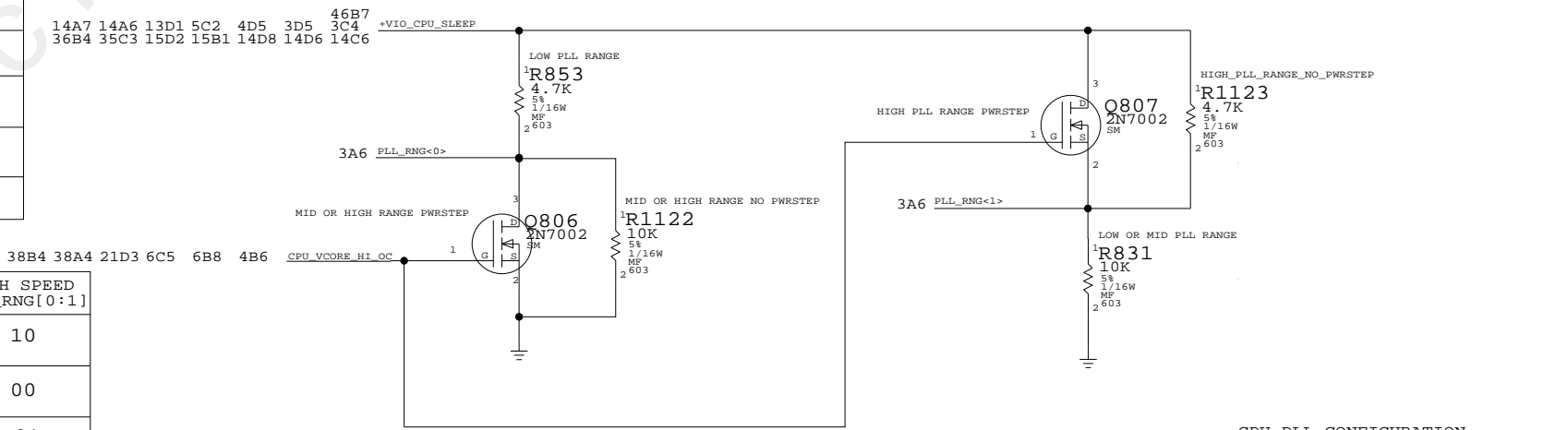
STATE ENCODING	CPU_VCORE_HI_OC	CPU_PLL_STOP_OC
HIGH SPEED	1	0
LOW SPEED	0	0
PLL OFF	X	1

BUS SPEED		66	100
CPU_PLL_CFG[0:4]	CORE:BUS RATIO		
00000	OFF		
00001	OFF		
00010	PLL BYPASS		
00011	PLL BYPASS		
00100	2.0:1	N/A	N/A
00101	2.5:1	N/A	N/A
00110	3.0:1	N/A	N/A
00111	3.5:1	N/A	N/A
01000	4.0:1	N/A	N/A
01001	4.5:1	N/A	N/A
01010	5.0:1	N/A	500
01011	5.5:1	N/A	550
01100	6.0:1	N/A	600
01101	6.5:1	N/A	650
01110	7.0:1	N/A	700
01111	7.5:1	500	750
10000	8.0:1	533	800
10001	8.5:1	567	850
10010	9.0:1	600	900
10011	9.5:1	633	950
10100	10.0:1	667	1000
10101	11.0:1	733	N/A
10110	12.0:1	800	N/A
10111	13.0:1	867	N/A
11000	14.0:1	933	N/A
11001	15.0:1	1000	N/A
11010	16.0:1	N/A	N/A
11011	17.0:1	N/A	N/A
11100	18.0:1	N/A	N/A
11101	19.0:1	N/A	N/A
11110	20.0:1	N/A	N/A
11111	OFF		



PLL_RNG[0:1]	PLL FREQUENCY RANGE
00	500-750 MHZ
01	750-1200 MHZ
10	UP TO 500 MHZ
11	RESERVED

SYSTEM	LOW SPEED PLL_RNG[0:1]	HIGH SPEED PLL_RNG[0:1]
LOW RANGE ONLY	10	10
LOW TO MID RANGE	10	00
LOW TO HIGH RANGE	10	01



**CPU PLL CONFIGURATION**

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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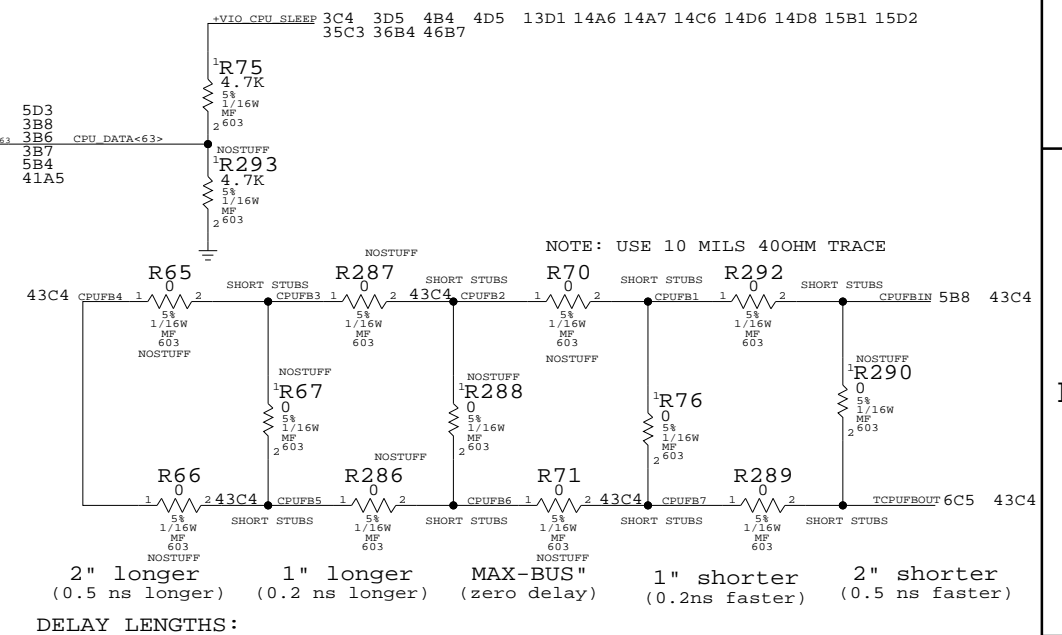
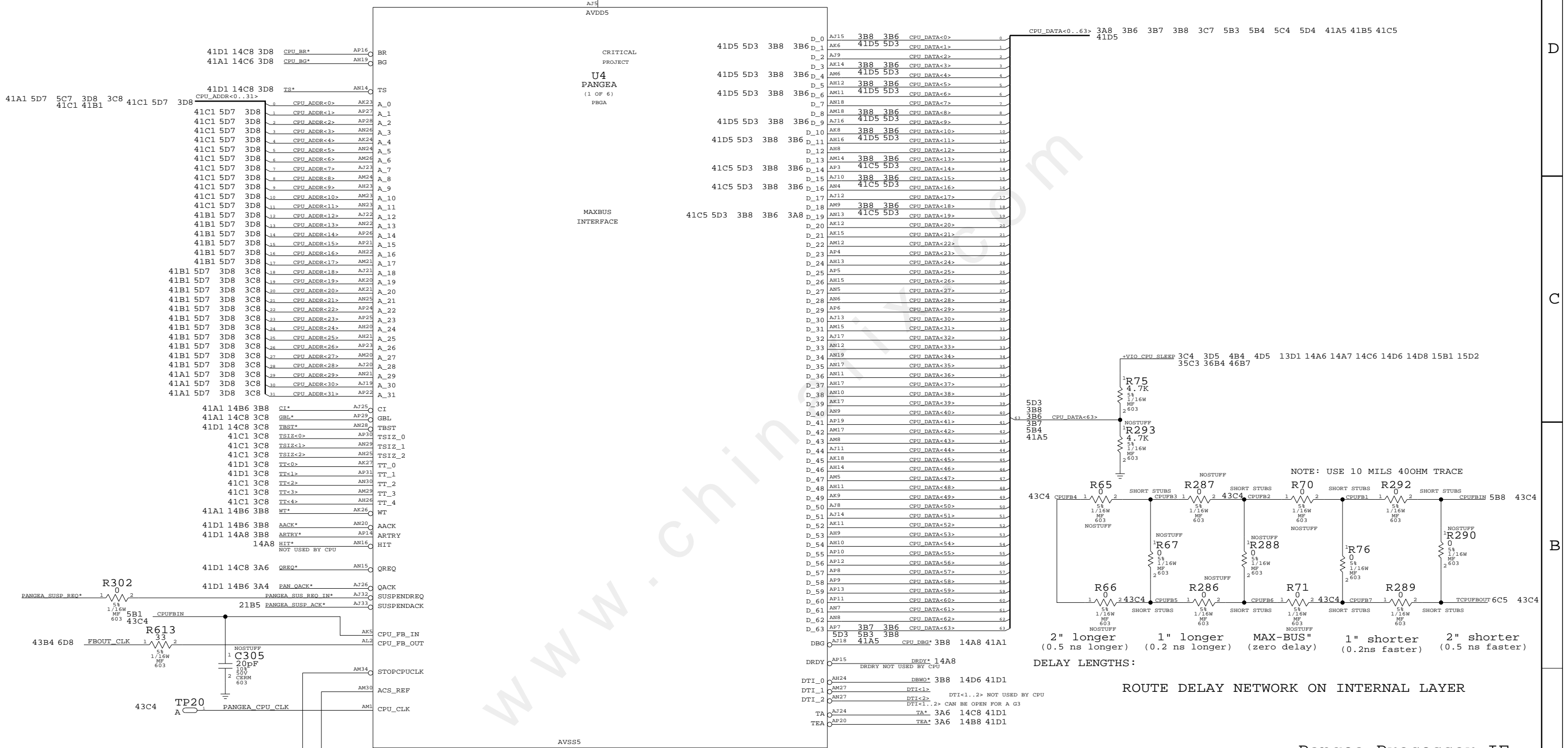
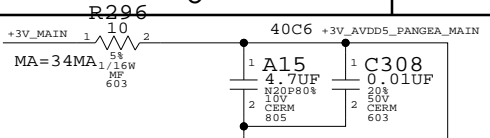




8 7 6 5 4 3 2 1

PANGEA CORE

22B1 16D4 15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3  
 8D6 8D4 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 3A4  
 13B8 13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7  
 21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4  
 46B7 40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4



2" longer (0.5 ns longer)    1" longer (0.2 ns longer)    MAX-BUS" (zero delay)    1" shorter (0.2ns faster)    2" shorter (0.5 ns faster)

DELAY LENGTHS:

ROUTE DELAY NETWORK ON INTERNAL LAYER

Pangea Processor IF

DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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PARTH	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380557	1	RFA-127675, PANGEA, PBGA-34X34-700	U4	PROJECT	

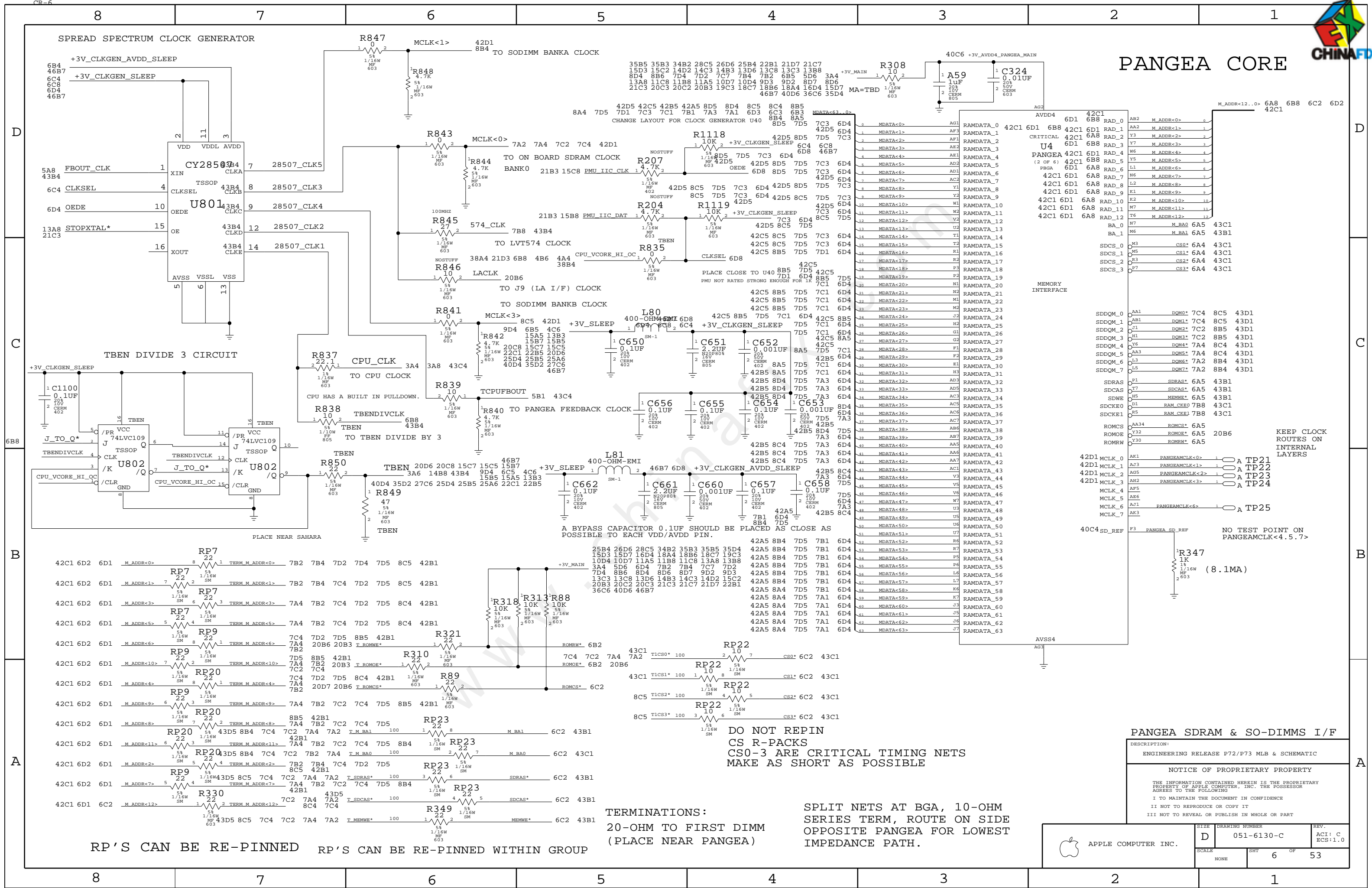
APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-6130-C	REV.	ACI: C ECS: 1.0
SCALE	NONE	SHT	5 OF	53	

8 7 6 5 4 3 2 1



# PANGEA CORE



**DO NOT REPIN CS R-PACKS CS0-3 ARE CRITICAL TIMING NETS MAKE AS SHORT AS POSSIBLE**

**TERMINATIONS: 20-OHM TO FIRST DIMM (PLACE NEAR PANGEA)**

**SPLIT NETS AT BGA, 10-OHM SERIES TERM, ROUTE ON SIDE OPPOSITE PANGEA FOR LOWEST IMPEDANCE PATH.**

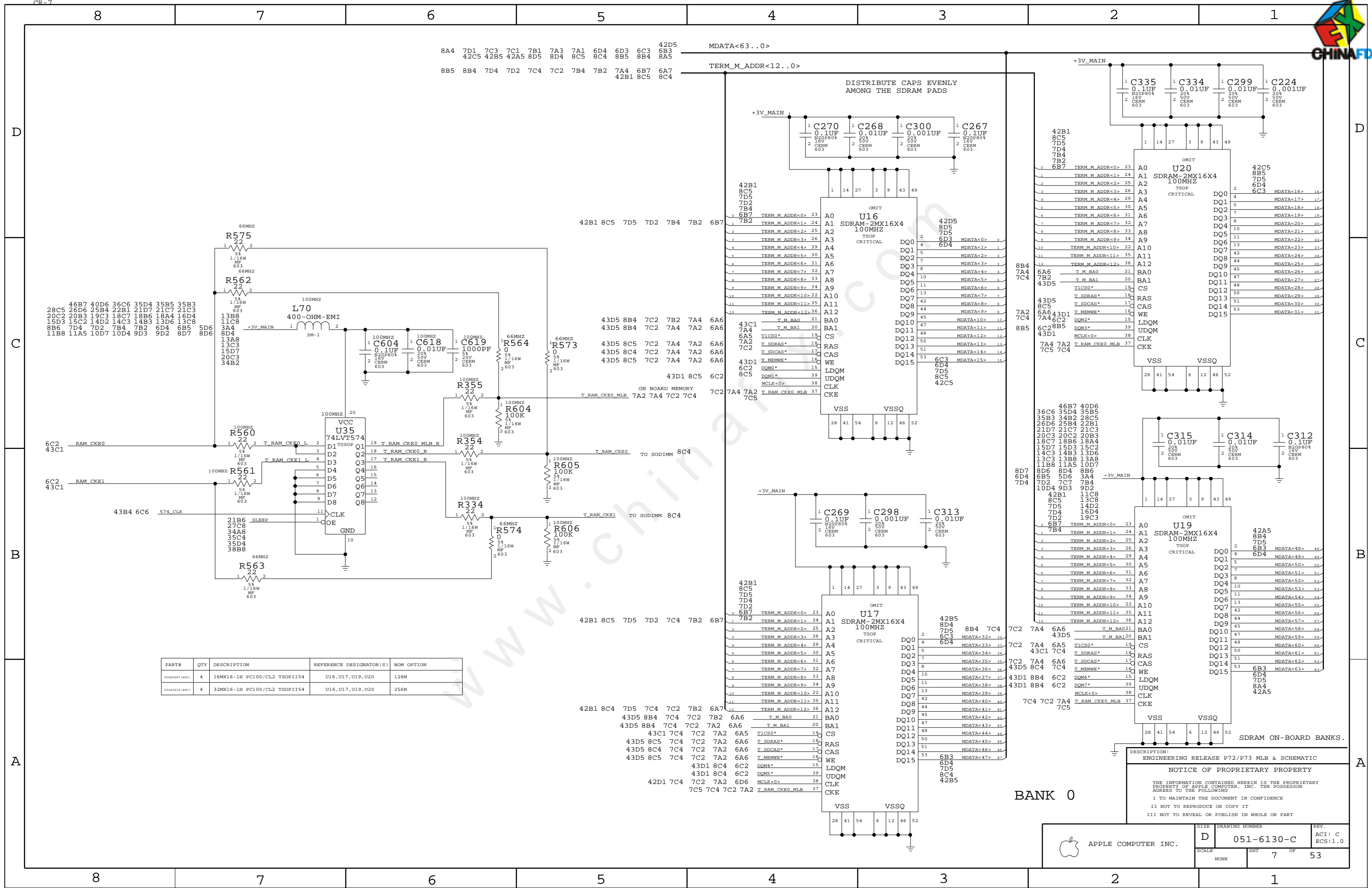
RP'S CAN BE RE-PINNED RP'S CAN BE RE-PINNED WITHIN GROUP

### PANGEA SDRAM & SO-DIMMS I/F

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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	SCALE	NONE	SHT	6 OF	53	ECS:1.0



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
838800071(ANCI)	4	16MX16-1H PC100/CL2 TSOPII54	U16,U17,U19,U20	128M
838802101(ANCI)	4	32MX16-1H PC100/CL2 TSOPII54	U16,U17,U19,U20	256M

DESCRIPTION:  
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SCALE	SHT	7	OF 53
NONE			

BANK 0

SDRAM ON-BOARD BANKS.



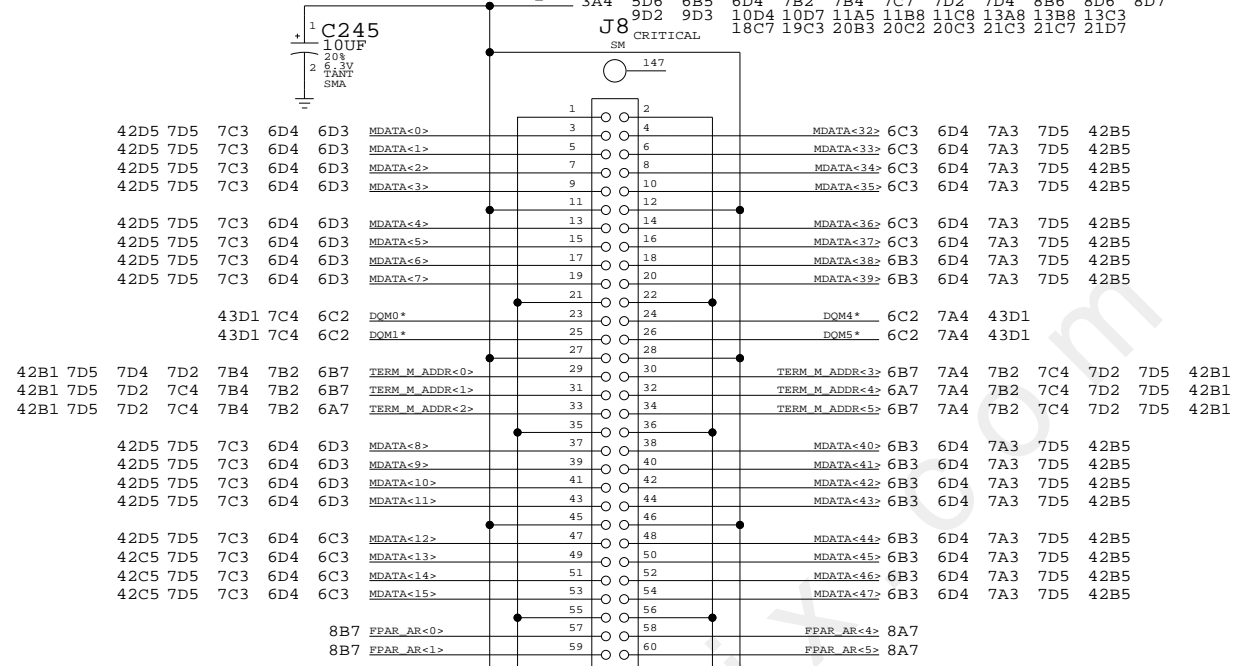
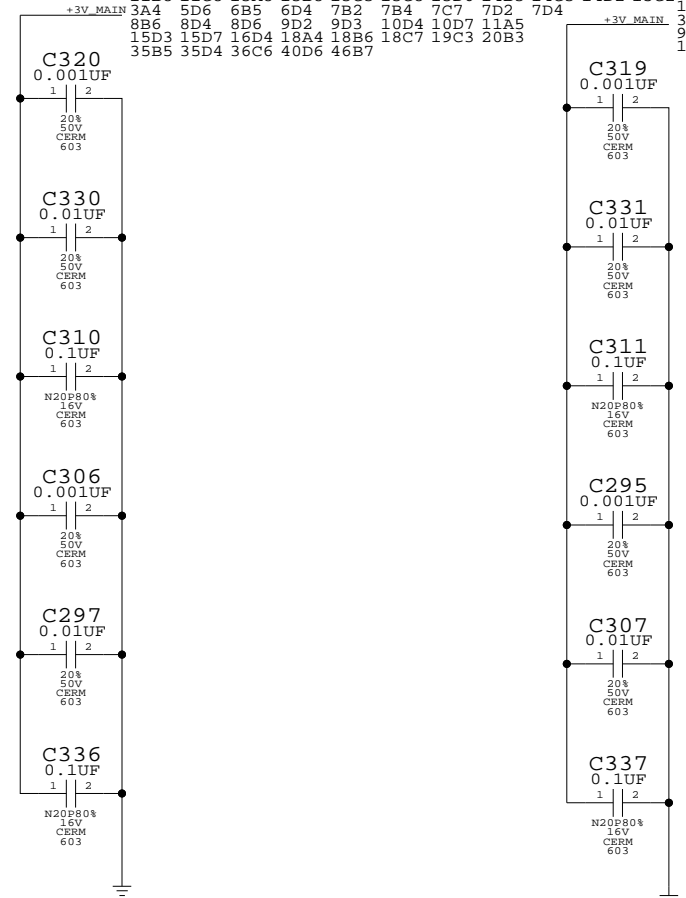


20C2 20C3 21C3 21C7 21D7 22B1 25B4 26D6 28C5 34B2 35B3  
 11B8 11C8 13A8 13B8 13C3 13C8 13D6 14B3 14C3 14D2 15C2 34B2 35B3  
 3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D7  
 8B6 8D4 8D6 9D2 9D3 10D4 10D7 11A5  
 15D3 15D7 16D4 18A4 18B6 18C7 19C3 20B3  
 35B5 35D4 36C6 40D6 46B7

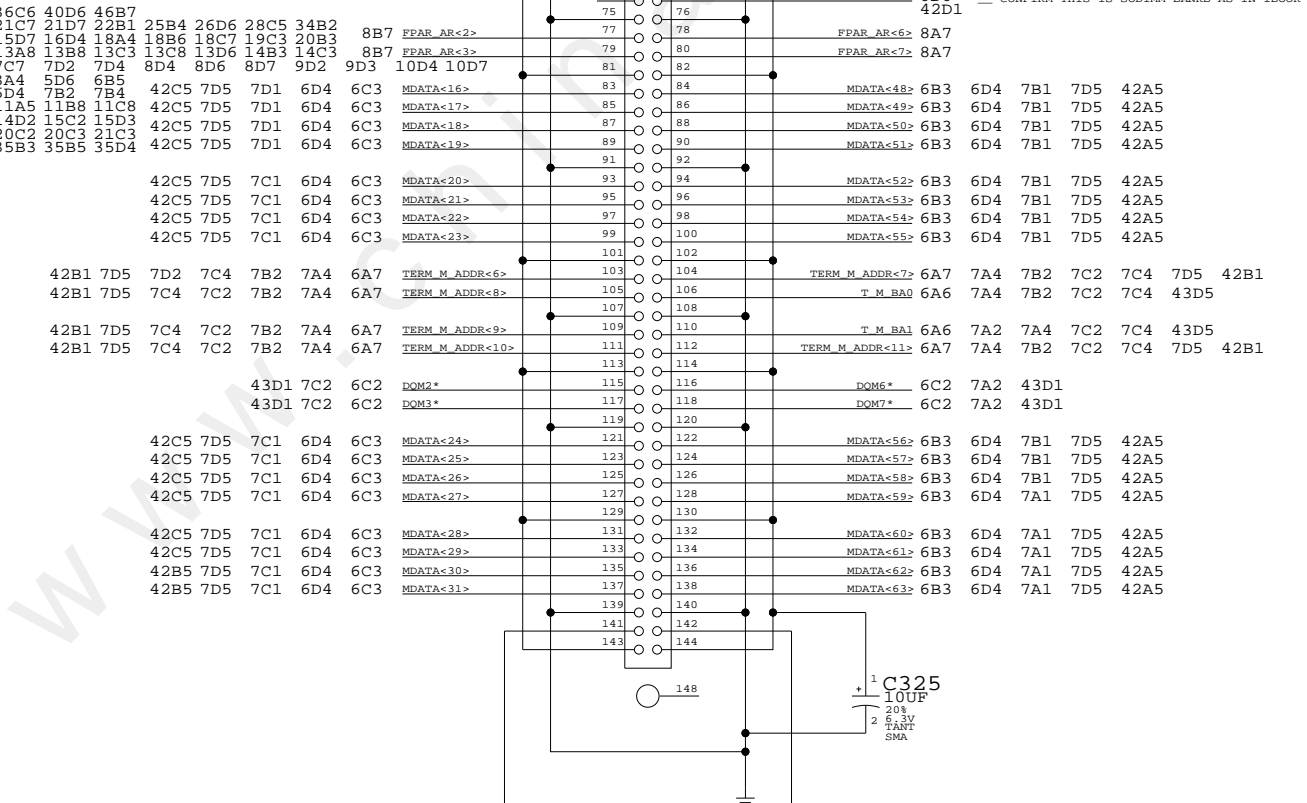
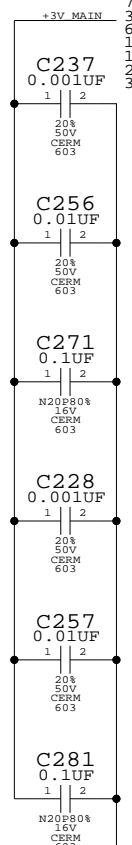
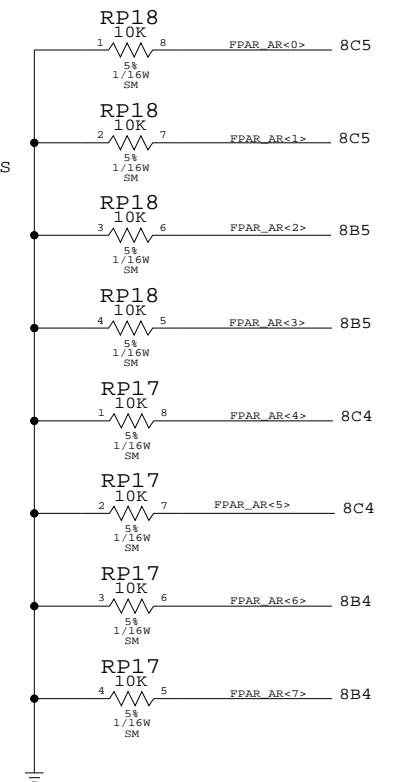
3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D7  
 9D2 9D3 10D4 10D7 11A5 11B8 11C8 13A8 13B8 13C3 13C8  
 19C3 20B3 20C2 20C3 21C3 21C7 21D7 22B1 25B4 26D6 28C5

PUT EACH 10UF GAP AT EACH END  
 AND HIGH-FREQUENCY BYPASS DISTRIBUTED  
 ALONG SODIMM

22B1 25B4 26D6 28C5 34B2 35B3 35B5 35D4 36C6 40D6 46B7  
 13C8 13D6 14B3 14C3 14D2 15C2 15D3 15D7 16D4 18A4 18B6  
 3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D6 8D7  
 9D2 9D3 10D4 10D7 11A5 11B8 11C8 13A8 13B8 13C3 13C8  
 18C7 19C3 20B3 20C2 20C3 21C3 21C7 21D7



PULL-DOWN UNUSED PARITY BITS



RP'S CAN BE RE-PINED  
 OR TURNED INTO DISCRETES  
 BY PCB DESIGNS.

IIC ALSO USED FOR 15D8 10B7 UNI\_IIC\_DAT  
 SODIMM DEBUG PORT 15D8 10B7 UNI\_IIC\_CLK

SO-DIMM CONNECTOR

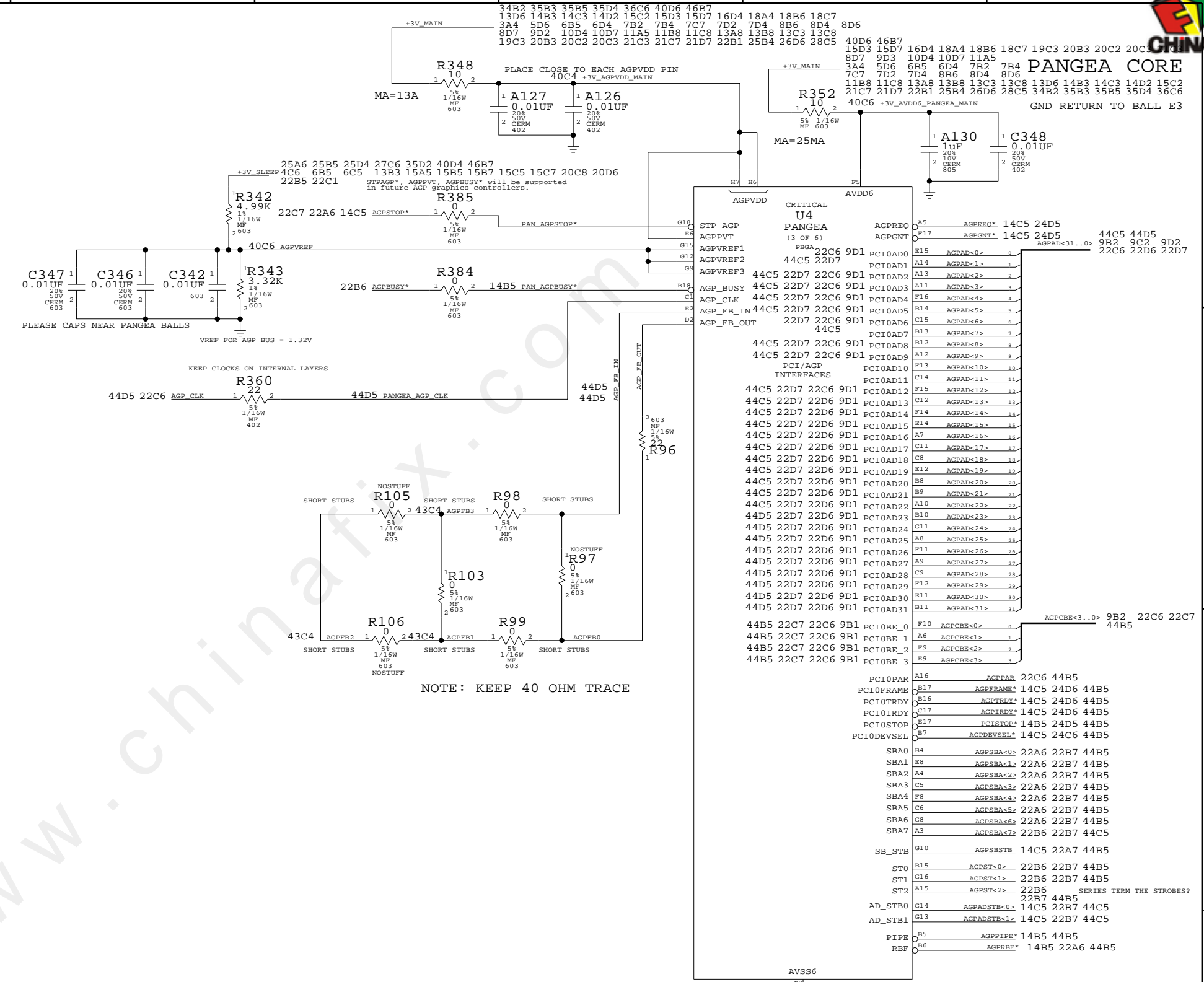
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SCALE	NONE	SHT	8 OF 53





1. WHAT IS THE PURPOSE OF SINGNAL AGPPVT?
2. CHECK WITH BILL C. FOR AGPVREF DIVIDERS - SCALE FOR LESS LEAKAGE.

**PANGEA AGP IF**

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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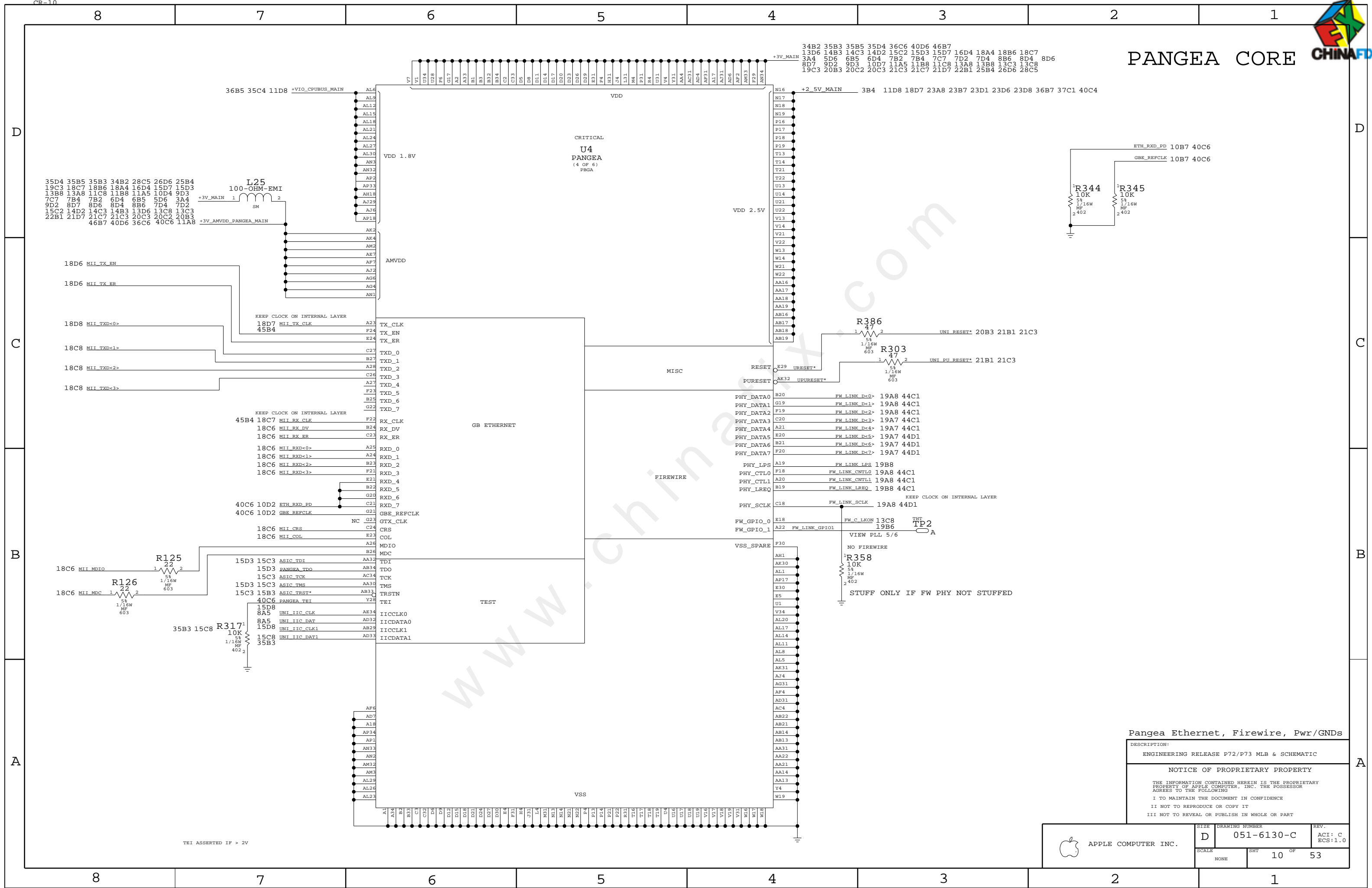
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SCALE	SHT	9 OF	53
NONE			



# PANGEA CORE



Pangea Ethernet, Firewire, Pwr/GNDs

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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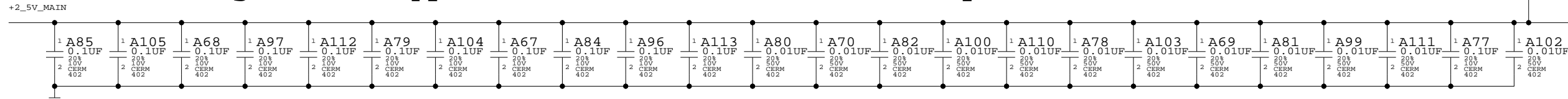
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	SCALE	SHT 10 OF 53	ACI: C ECS:1.0

TEI ASSERTED IF > 2V

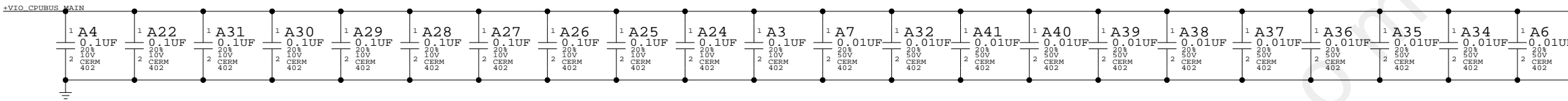


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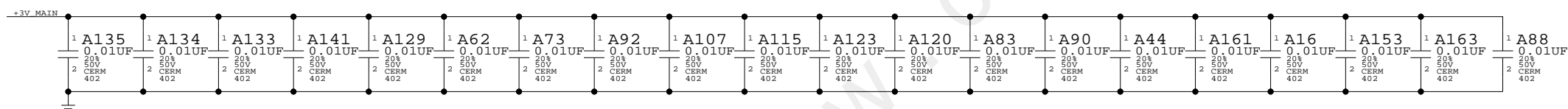
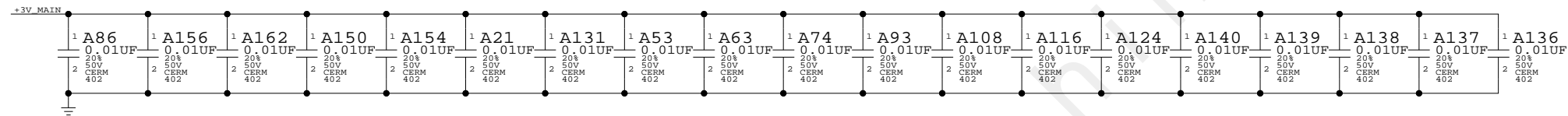
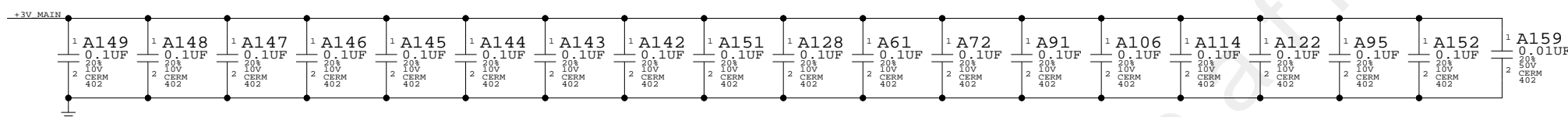
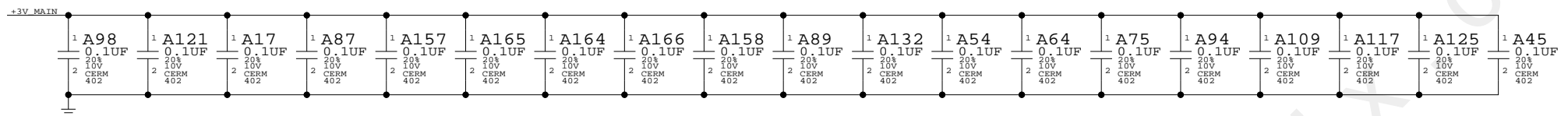
## Pangea Core Bypass -- 16 0.01uF across each pair, 8 0.001uF on corners



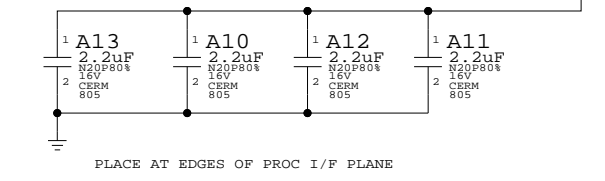
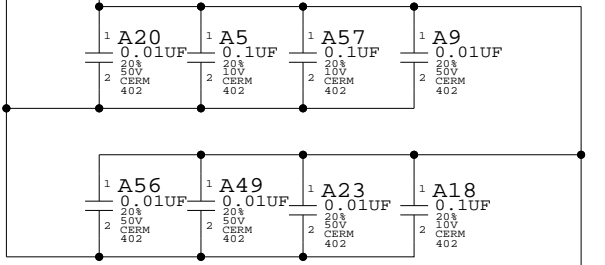
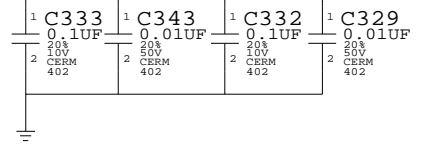
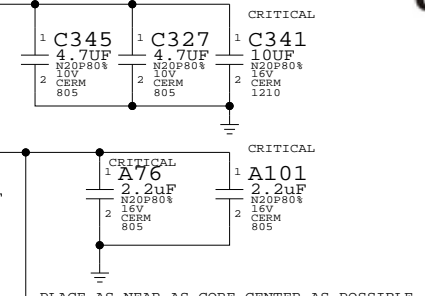
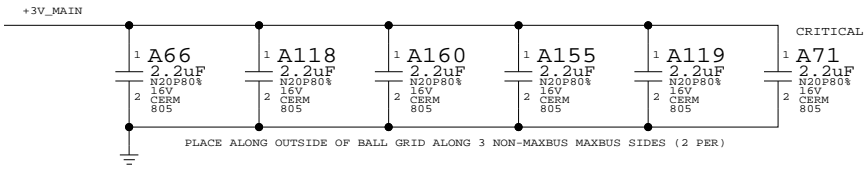
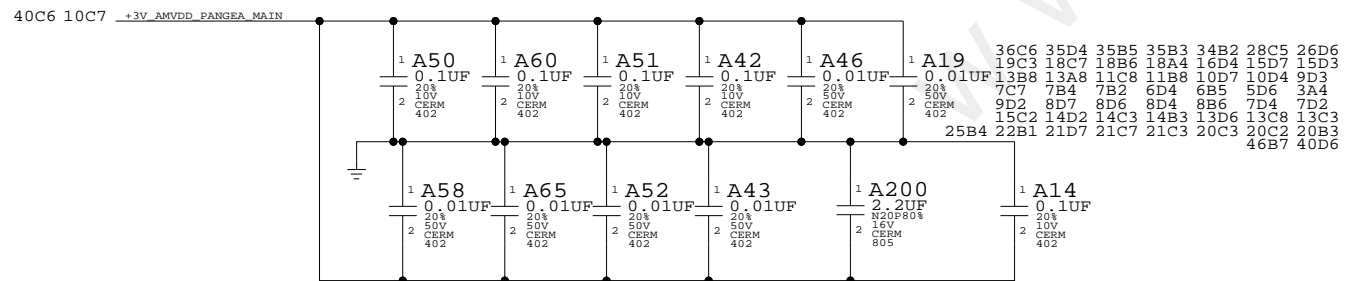
## Pangea Processor I/F Bypass -- two per power/ground pair



## Pangea I/O Ring Bypass -- two per power/ground pair



## Pangea AMVDD Bypass (one pair per pin)



## Pangea Bypass

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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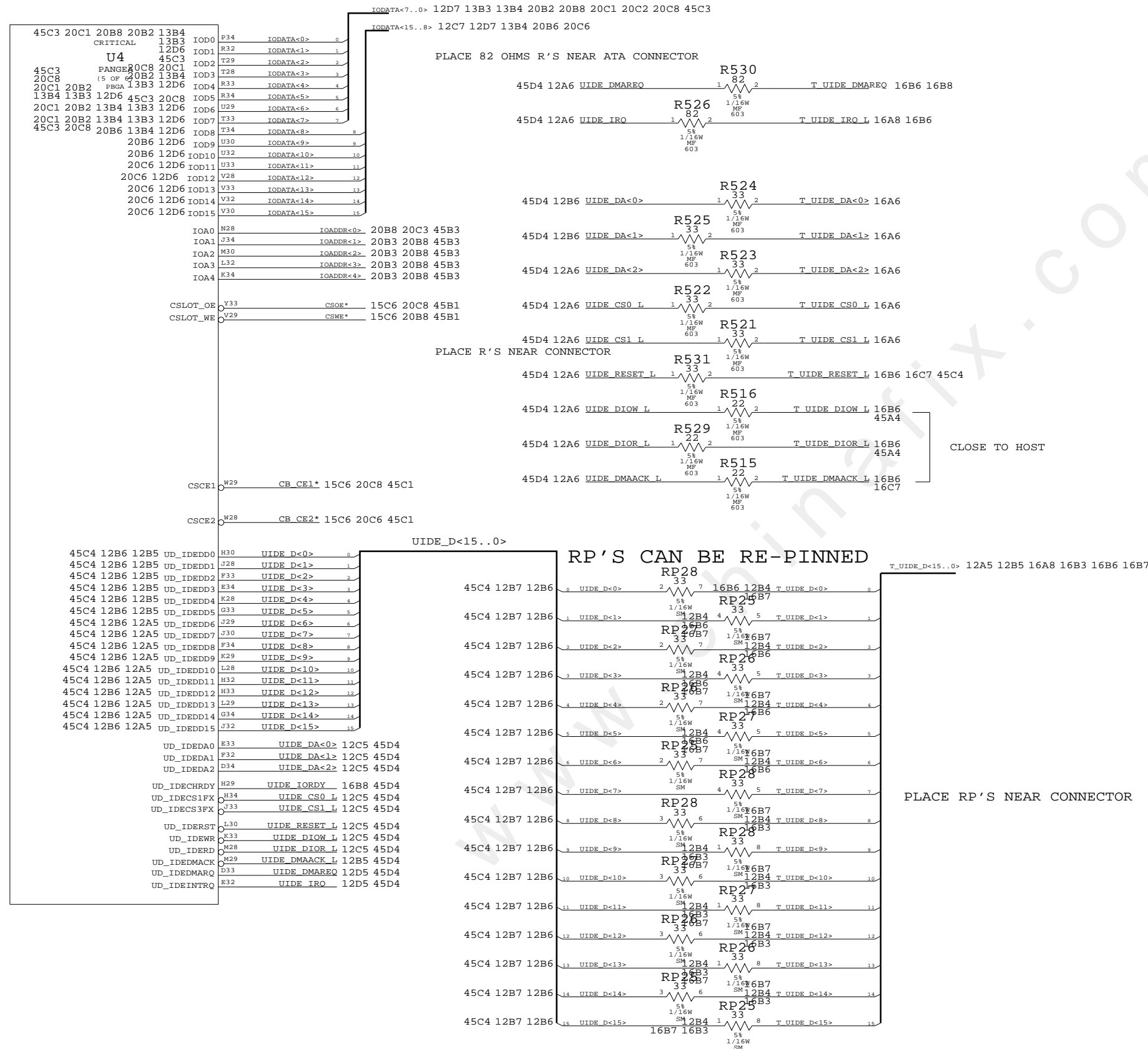
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-6130-C	REV.	ACI: C
	SCALE	NONE	SHT	11	OF	53





# PANGEA CORE



## PANGEA ATA BUS

DESCRIPTION:  
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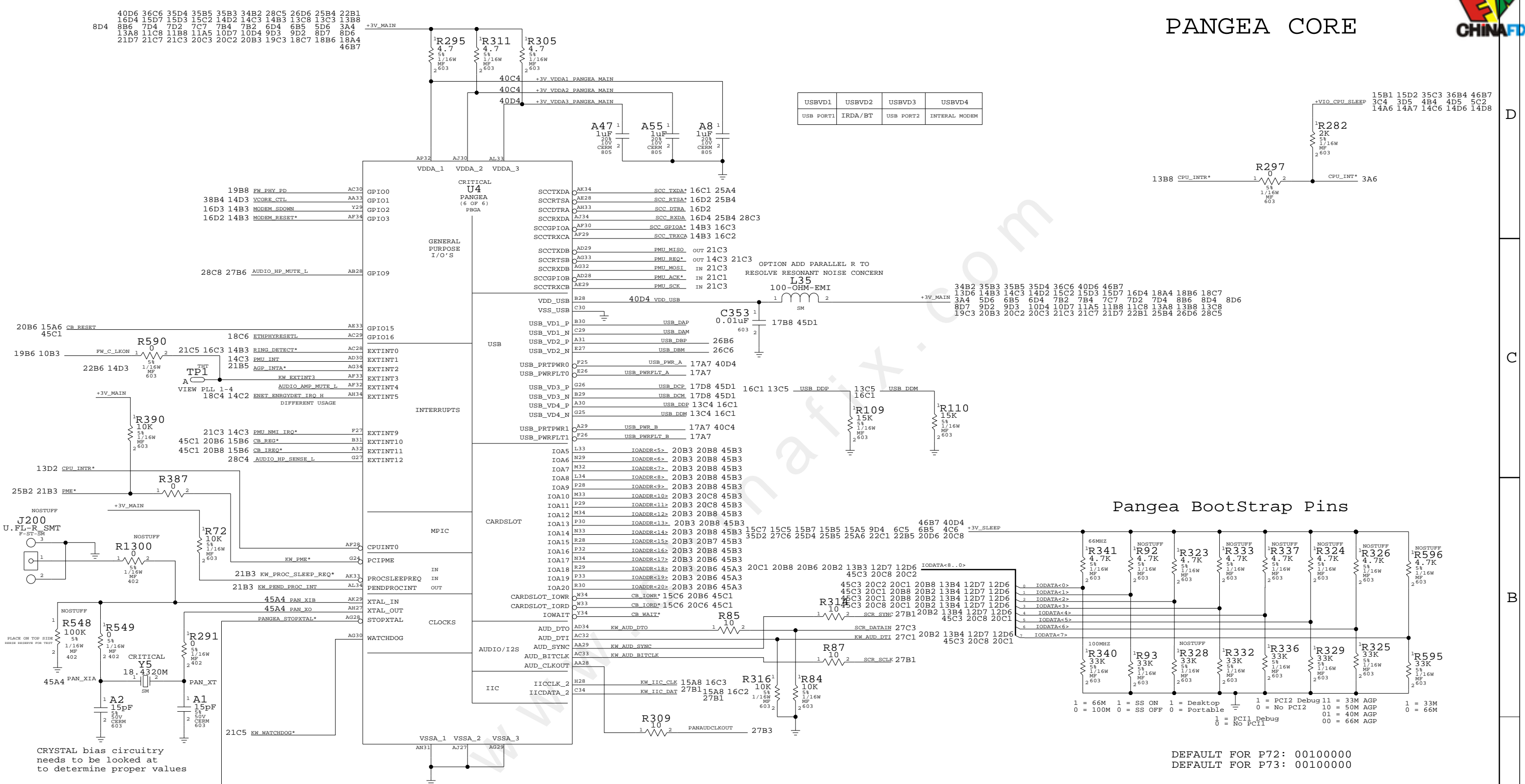
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	12 OF	53
NONE			



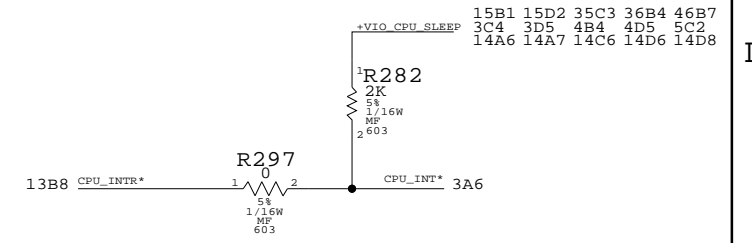
# PANGEA CORE

D  
C  
B  
A

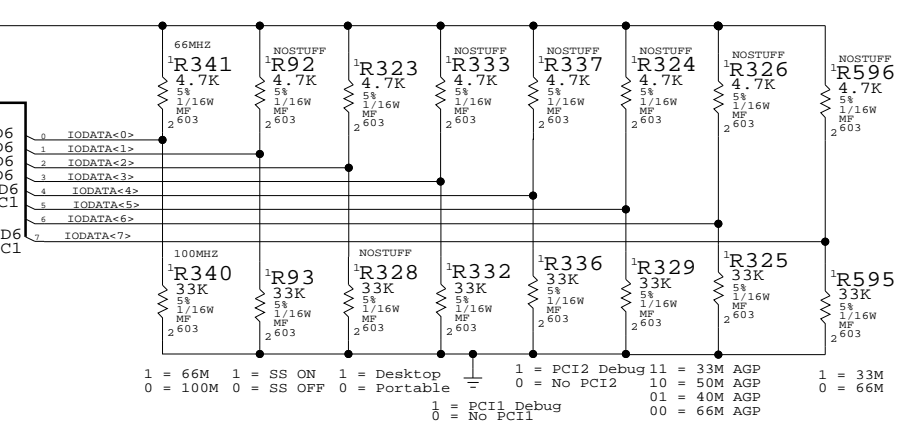
D  
C  
B  
A



USBVD1	USBVD2	USBVD3	USBVD4
USB PORT1	IRDA/BT	USB PORT2	INTERNAL MODEM



## Pangea Boot Strap Pins



DEFAULT FOR P72: 00100000  
 DEFAULT FOR P73: 00100000

CRYSTAL bias circuitry needs to be looked at to determine proper values

### PANGEA SER/AUD/USB, BOOTSTRAPS

DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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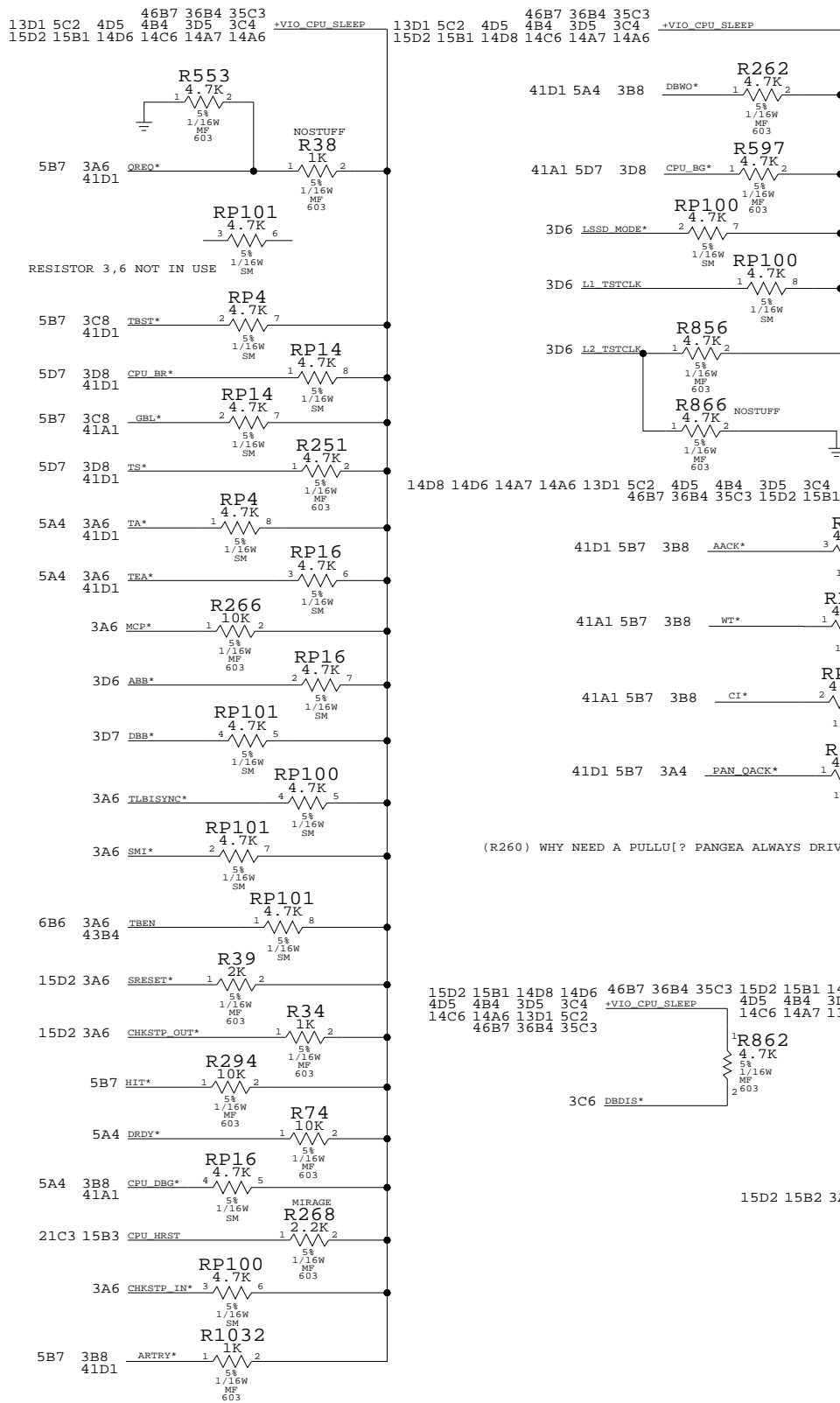
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	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	OF	REV.
NONE	13	53	

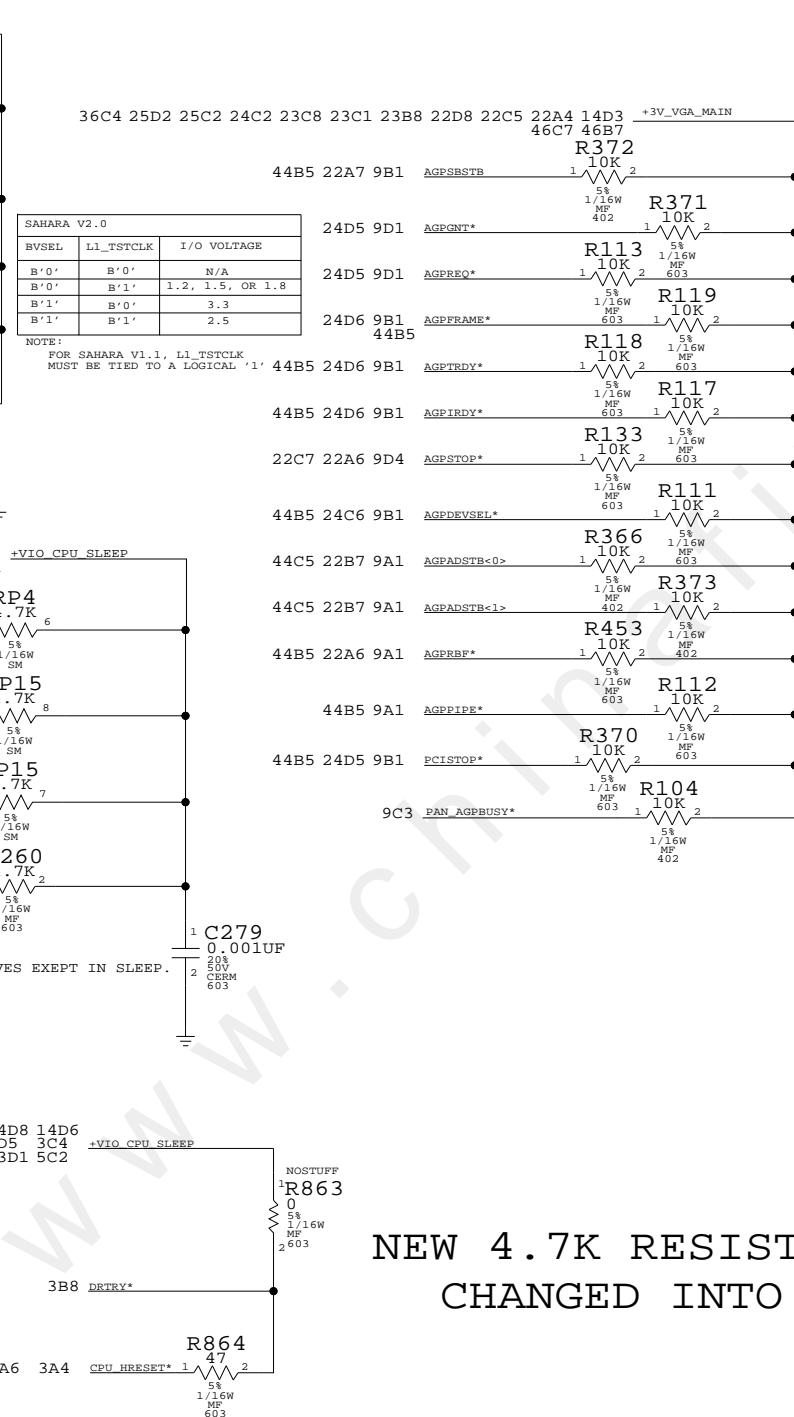
# PANGEA PULLUPS/PULLDOWNS

TO LOCATE UNUSED RPAK PINS REFERE TO COMPONENT LOCATIO CREF TABLE ON PAGE 49

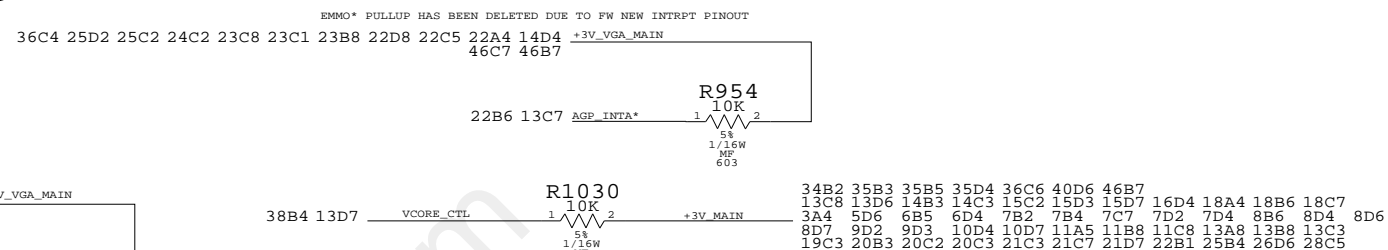
## MAXBUS PULLS



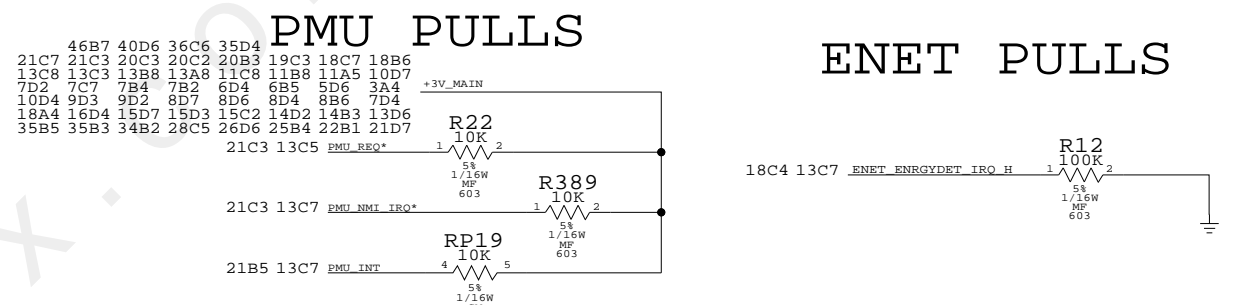
## AGP PULLS



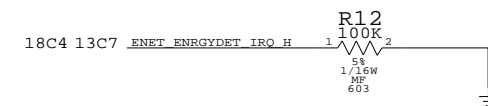
## GPIO PULLS



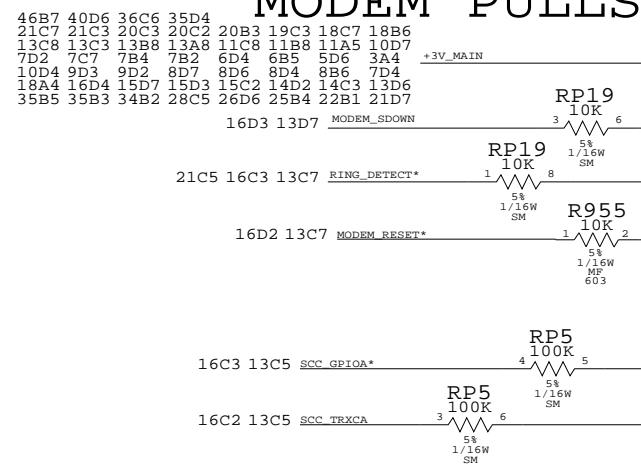
## PMU PULLS



## ENET PULLS



## MODEM PULLS



NEW 4.7K RESISTORS CAN BE CHANGED INTO R-PACKS

R-PACKS CAN BE RE-PINNED

PULL-UP/PULL-DOWN (1)

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ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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SCALE	NONE	SHT	14 OF 53



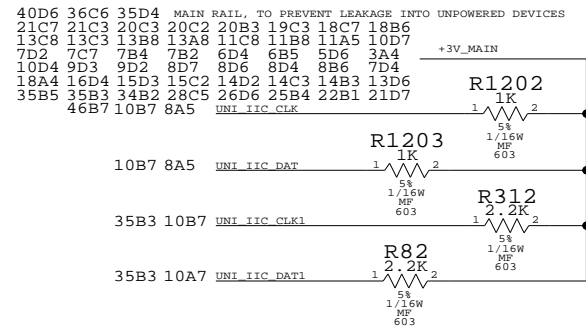


TO LOCATE UNUSED RPAK PINS REFERE TO COMPONENT LOCATIO CREF TABLLE ON PAGE49

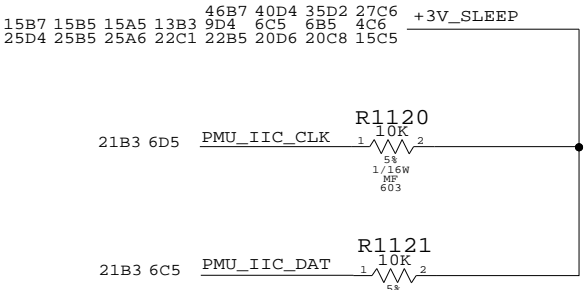
### IIC BUS PULLUPS

### CARDSLOT BUS PULLS

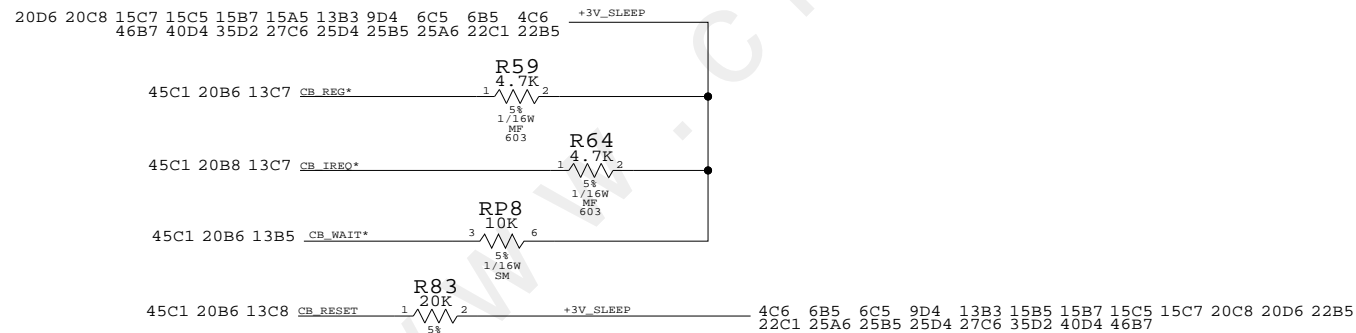
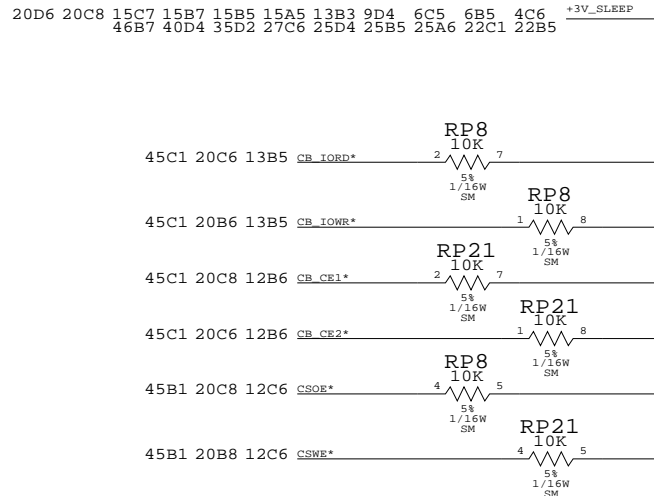
### JTAG PULLS



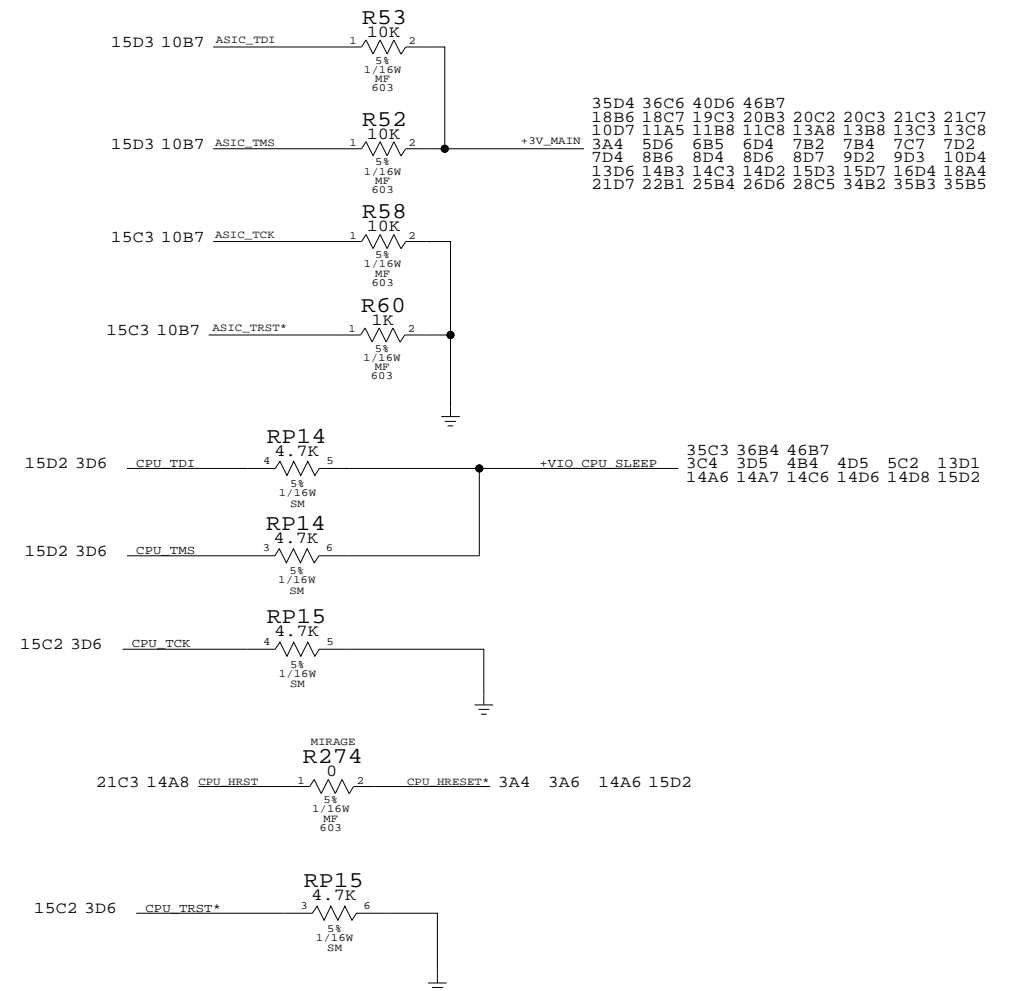
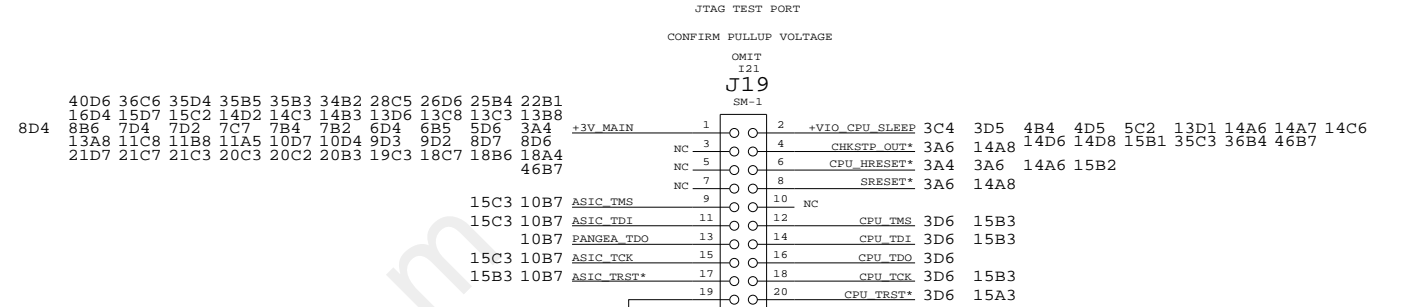
PMU NOT RATED STRONG ENOUGH FOR 1K



PMU PULL UP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
630-3999	1	PCBA, BOOTBANGER, P72	J19	OASIS
511S0018	1	CONN, POPT, STR 20-P .8MM PITCH	J19	NONPRODUCTION



PULL-UP/PULL DOWN(2)

DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

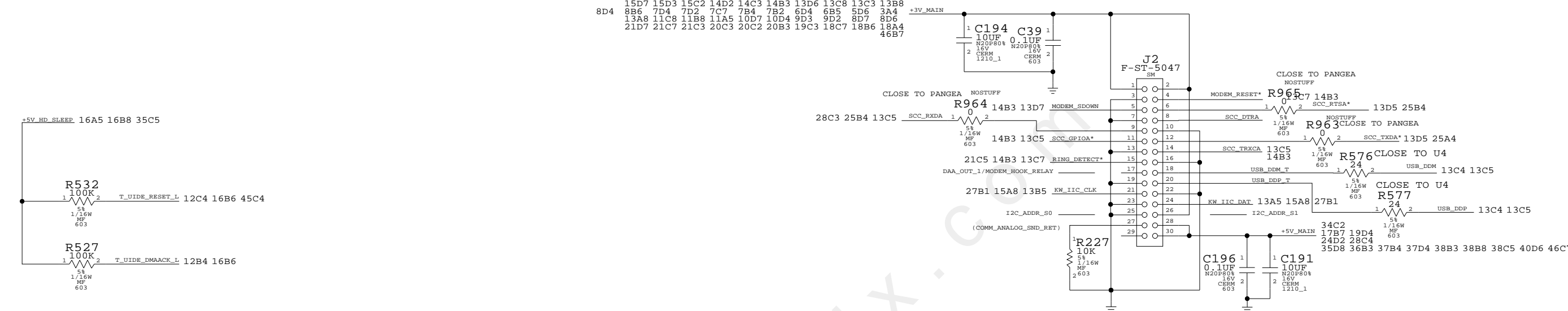
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SCALE	NONE	SHT	15 OF 53

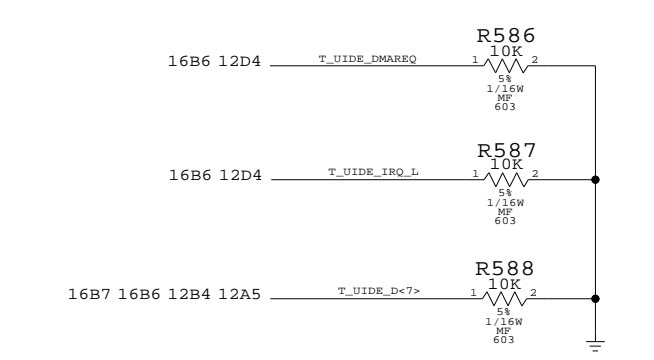
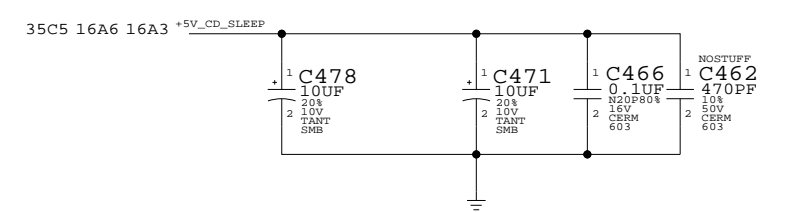
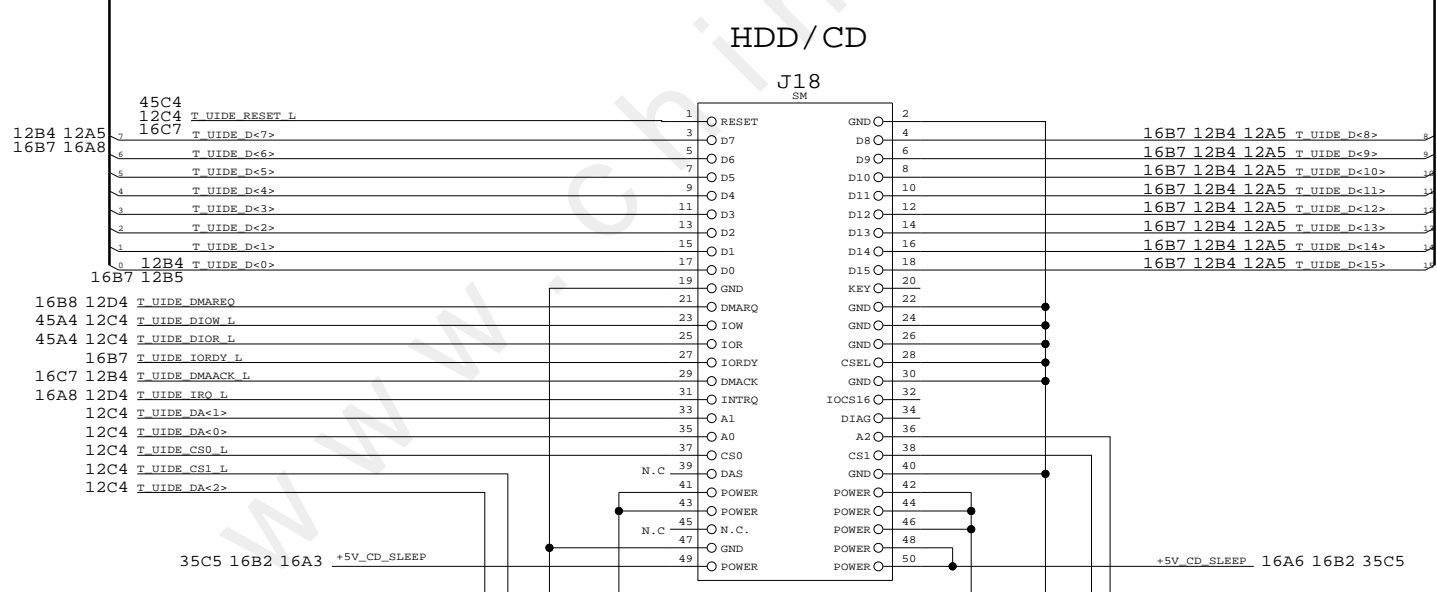
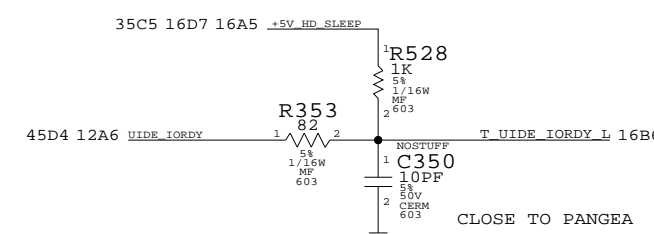
# MICRO DASH AND MINI-SPRING MODEM BOARD CONNECTOR

40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4 22B1  
 15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8  
 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4  
 13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6  
 21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4  
 46B7



## RJ-11 SHIELD

16B6 16B3 16A8 12B5 12B4 12A5 T\_UIDE\_D<15..0>



INTERNAL HD AND CD-ROM CONNECTORS  
 MICRO DASH AND MINI SPRING MODEM BOARD CONNECTOR

DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

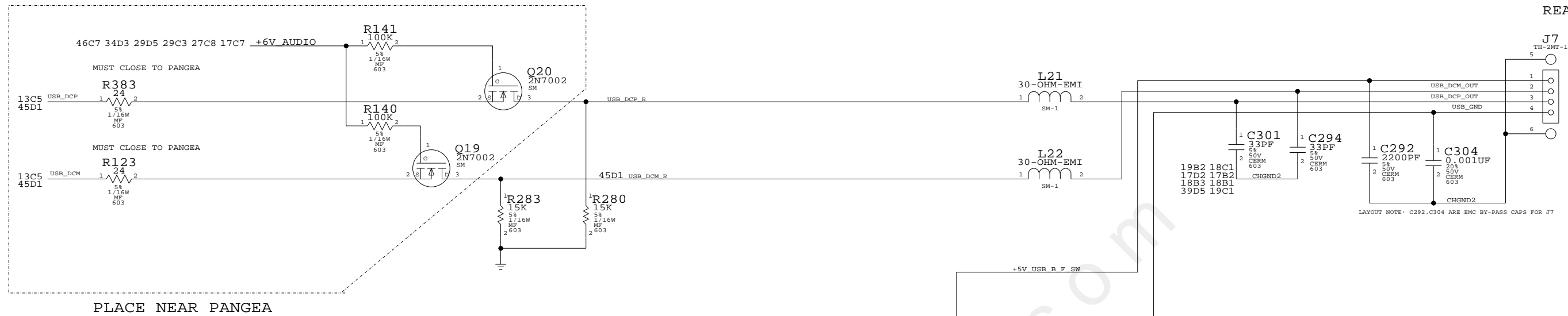
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SCALE	SHT	OF	
NONE	16	53	

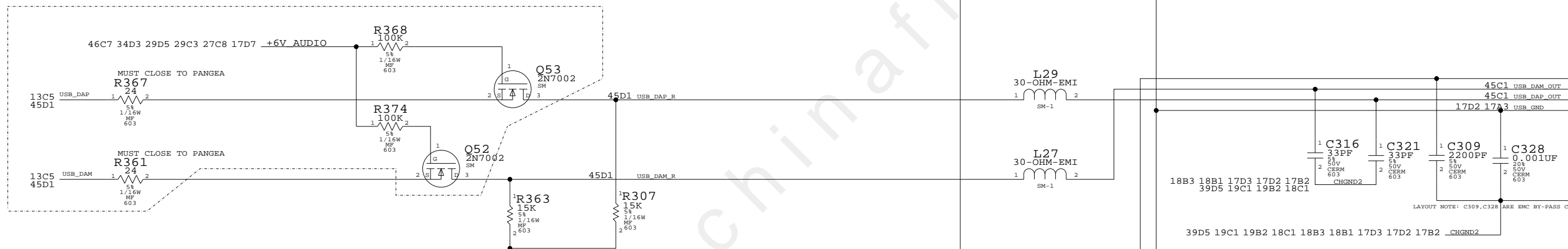
8 7 6 5 4 3 2 1

REAR

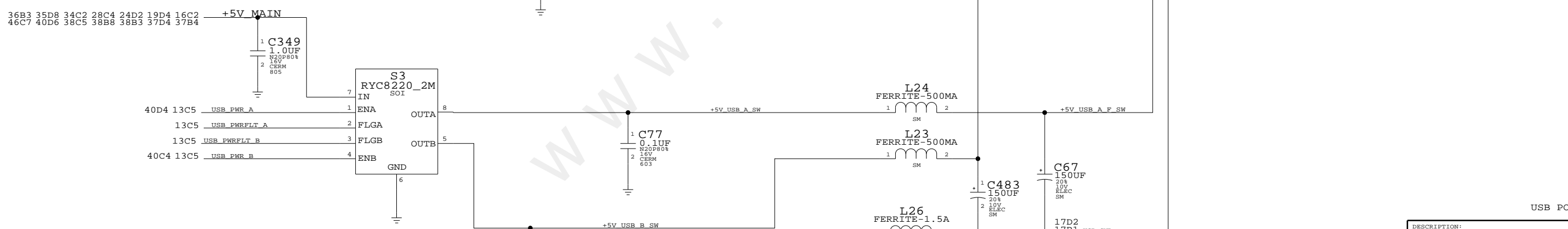


PLACE NEAR PANGEA

PLACE NEAR PANGEA



FRONT



USB PORT

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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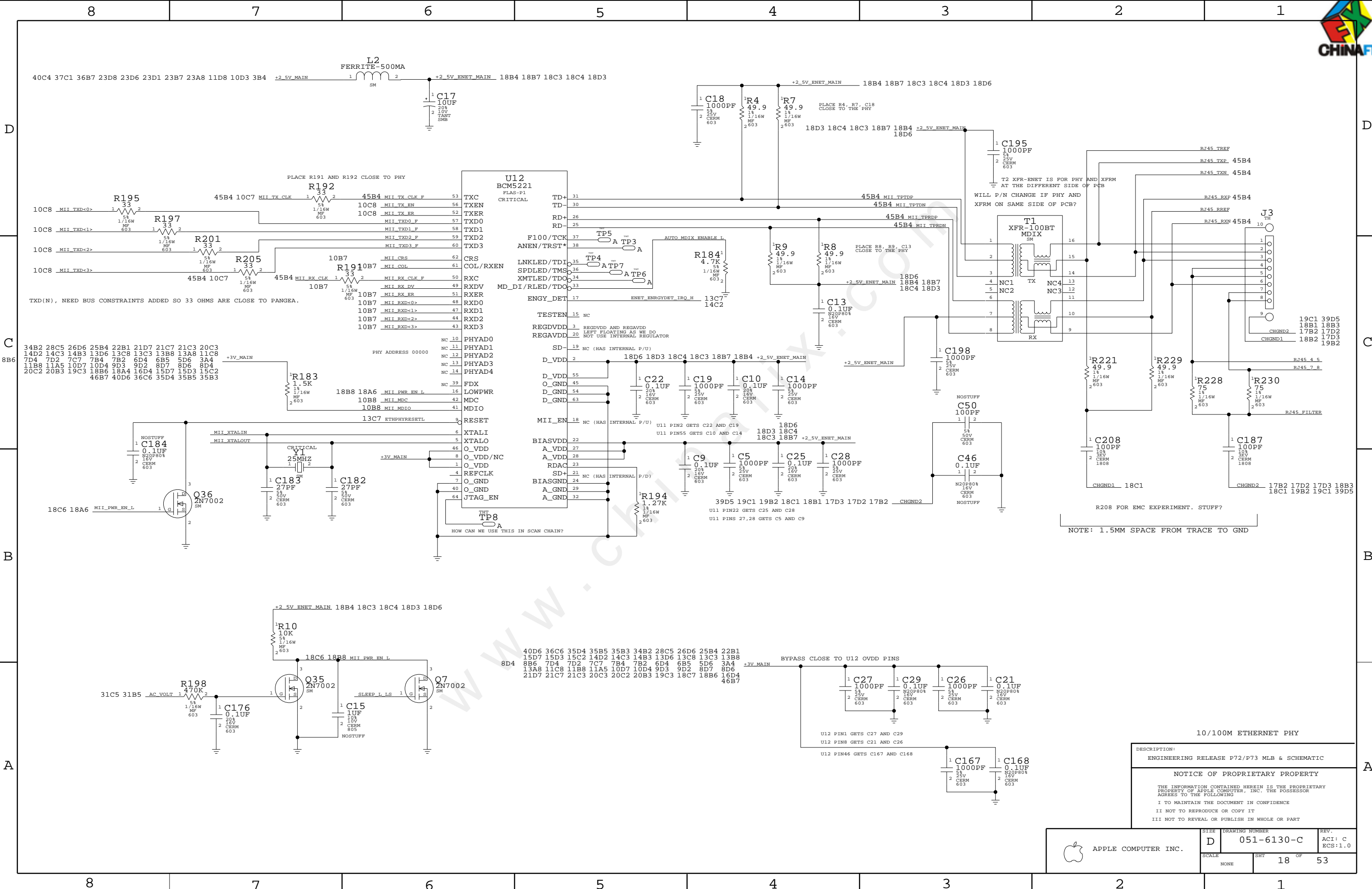
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	17 OF	53
NONE			

8 7 6 5 4 3 2 1





40C4 37C1 36B7 23D8 23D6 23D1 23B7 23A8 11D8 10D3 3B4 +2.5V\_MAIN

PLACE R191 AND R192 CLOSE TO PHY  
R192 33 1/16W MF 603  
R195 33 1/16W MF 603  
R197 33 1/16W MF 603  
R201 33 1/16W MF 603  
R205 33 1/16W MF 603  
10C8 MII\_TXD<0>  
10C8 MII\_TXD<1>  
10C8 MII\_TXD<2>  
10C8 MII\_TXD<3>  
45B4 10C7  
10B7 MII\_CS  
10B7 MII\_COL  
10B7 MII\_RX\_CLK\_F  
10B7 MII\_RX\_DV  
10B7 MII\_RX\_ER  
10B7 MII\_RXD<0>  
10B7 MII\_RXD<1>  
10B7 MII\_RXD<2>  
10B7 MII\_RXD<3>

34B2 28C5 26D6 25B4 22B1 21D7 21C7 21C3 20C3  
14D2 14C3 14B3 13D6 13C8 13C3 13B8 13A8 11C8  
7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4  
11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6 8D4  
20C2 20B3 19C3 18B6 18A4 16D4 15D7 15D3 15C2  
46B7 40D6 36C6 35D4 35B5 35B3

+3V\_MAIN  
R183 1.5K 1/16W MF 603  
18B8 18A6 MII\_PWR\_EN\_L  
10B8 MII\_MDC  
10B8 MII\_MDIO  
13C7 ETHPHYRESETL

NOSTUFF  
C184 0.1UF 16V N20P80% CERAM 603  
Y1 25MHZ 10K 5% 5V CERAM 603  
C183 27PF 5V CERAM 603  
C182 27PF 5V CERAM 603  
Q36 2N7002  
18C6 18A6 MII\_PWR\_EN\_L  
MII\_XTALIN  
MII\_XTALOUT  
CRITICAL  
+3V\_MAIN  
Q35 2N7002  
SLEEP\_L\_LS  
Q7 2N7002  
R10 10K 1/16W MF 603  
18C6 18B8 MII\_PWR\_EN\_L  
R198 470K 1/16W MF 603  
C176 0.1UF 20% 16V CERAM 603  
C15 1UF 10V CERAM 603  
NOSTUFF

+2.5V\_ENET\_MAIN 18B4 18C3 18C4 18D3 18D6  
R10 10K 1/16W MF 603  
18C6 18B8 MII\_PWR\_EN\_L  
31C5 31B5 AC\_VOLT  
R198 470K 1/16W MF 603  
C176 0.1UF 20% 16V CERAM 603  
C15 1UF 10V CERAM 603  
NOSTUFF  
Q35 2N7002  
SLEEP\_L\_LS  
Q7 2N7002  
R10 10K 1/16W MF 603  
18C6 18B8 MII\_PWR\_EN\_L  
31C5 31B5 AC\_VOLT  
R198 470K 1/16W MF 603  
C176 0.1UF 20% 16V CERAM 603  
C15 1UF 10V CERAM 603  
NOSTUFF  
Q35 2N7002  
SLEEP\_L\_LS  
Q7 2N7002

40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4 22B1  
15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8  
8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4  
13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6  
21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 16D4 46B7

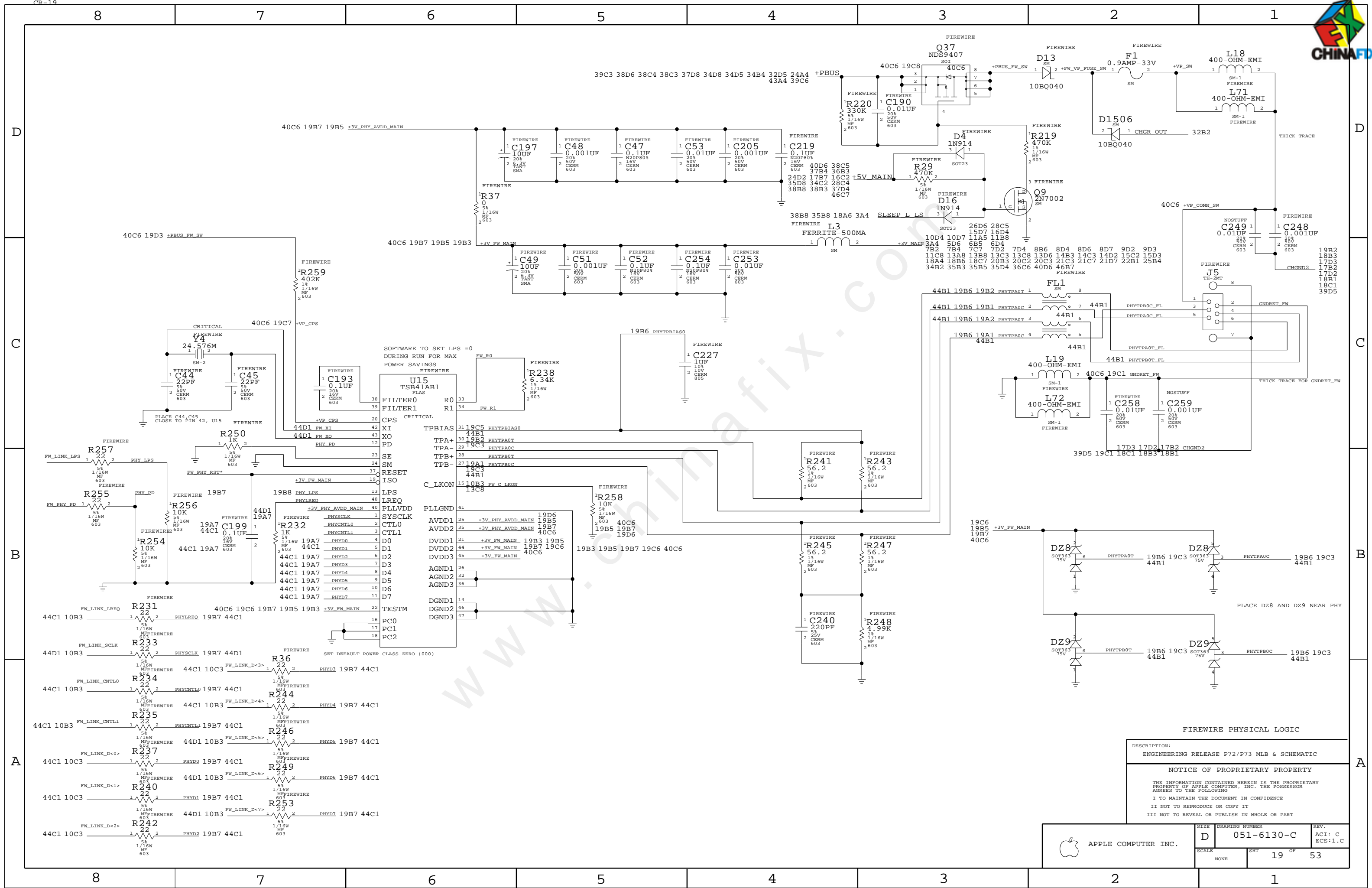
BYPASS CLOSE TO U12 OVDD PINS  
C27 1000PF 5% 25V CERAM 603  
C29 0.1UF 16V N20P80% CERAM 603  
C26 1000PF 5% 25V CERAM 603  
C21 0.1UF 16V N20P80% CERAM 603  
U12 PIN1 GETS C27 AND C29  
U12 PIN8 GETS C21 AND C26  
U12 PIN46 GETS C167 AND C168  
C167 1000PF 5% 25V CERAM 603  
C168 0.1UF 16V N20P80% CERAM 603

U12 BCM5221  
FLAS-P1 CRITICAL  
TD+ 31  
TD- 30  
RD+ 26  
RD- 25  
F100/TCK ANEN/TRST\* 38  
LNKLED/TDI 35  
SPDLED/TMS 36  
XMTLED/TDO 34  
MD\_DI/RLED/TDO 33  
ENET\_ENRGYDET\_IRQ\_H 13C7 14C2  
TESTEN 15 NC  
REGDVDD 3 REGDVDD AND REGAVDD LEFT FLOATING AS WE DO NOT USE INTERNAL REGULATOR  
REGAVDD 20  
SD- 19 NC (HAS INTERNAL P/U)  
D\_VDD 2  
D\_VDD 55  
O\_GND 45  
D\_GND 54  
D\_GND 63  
MII\_EN 18 NC (HAS INTERNAL P/U)  
BIASVDD 22  
A\_VDD 27  
A\_VDD 28  
RDAC 23  
SD+ 21  
BIASGND 24 NC (HAS INTERNAL P/D)  
A\_GND 29  
A\_GND 32  
TP8  
HOW CAN WE USE THIS IN SCAN CHAIN?

18D6 18D3 18C4 18C3 18B7 18B4 +2.5V\_ENET\_MAIN  
C22 0.1UF 20% 16V CERAM 603  
C19 1000PF 5% 25V CERAM 603  
C10 0.1UF 16V N20P80% CERAM 603  
C14 1000PF 5% 25V CERAM 603  
U11 PIN2 GETS C22 AND C19  
U11 PIN5 GETS C10 AND C14  
18D6 18C4 18C3 18B7 +2.5V\_ENET\_MAIN  
C9 0.1UF 20% 16V CERAM 603  
C5 1000PF 5% 25V CERAM 603  
C25 0.1UF 20% 16V CERAM 603  
C28 1000PF 5% 25V CERAM 603  
U11 PIN2 GETS C25 AND C28  
U11 PINS 27,28 GETS C5 AND C9  
18D6 18D3 18C4 18C3 18B7 18B4 +2.5V\_ENET\_MAIN  
C27 1000PF 5% 25V CERAM 603  
C29 0.1UF 16V N20P80% CERAM 603  
C26 1000PF 5% 25V CERAM 603  
C21 0.1UF 16V N20P80% CERAM 603  
U12 PIN1 GETS C27 AND C29  
U12 PIN8 GETS C21 AND C26  
U12 PIN46 GETS C167 AND C168  
C167 1000PF 5% 25V CERAM 603  
C168 0.1UF 16V N20P80% CERAM 603

+2.5V\_ENET\_MAIN 18B4 18B7 18C3 18C4 18D3 18D6  
C18 1000PF 5% 25V CERAM 603  
R4 49.9 1/16W MF 603  
R7 49.9 1/16W MF 603  
PLACE R4, R7, C18 CLOSE TO THE PHY  
18D3 18C4 18C3 18B7 18B4 +2.5V\_ENET\_MAIN 18D6  
C195 1000PF 5% 25V CERAM 603  
T2 XFR-ENET IS FOR PHY AND XFRM AT THE DIFFERENT SIDE OF PCB WILL P/N CHANGE IF PHY AND XFRM ON SAME SIDE OF PCB?  
R45\_TREF RJ45 TREF  
R45\_TXP 45B4  
R45\_TXN 45B4  
R45\_RXP 45B4  
R45\_RREF RJ45 RREF  
R45\_RXN 45B4  
T1 XFR-100BT MDIX SM  
NC1 TX  
NC2 NC3  
NC4 NC3  
R9 49.9 1/16W MF 603  
R8 49.9 1/16W MF 603  
PLACE R8, R9, C13 CLOSE TO THE PHY  
18D6 18B4 18B7 18C4 18D3  
C13 0.1UF 16V N20P80% CERAM 603  
C198 1000PF 5% 25V CERAM 603  
C208 1000PF 5% 25V CERAM 603  
C187 1000PF 5% 25V CERAM 603  
R221 49.9 1/16W MF 603  
R229 49.9 1/16W MF 603  
R228 75 1/16W MF 603  
R230 75 1/16W MF 603  
R45\_FILTER RJ45 FILTER  
C50 100PF 5% 25V CERAM 603  
NOSTUFF  
C46 0.1UF 16V N20P80% CERAM 603  
NOSTUFF  
CHGND1 18C1  
CHGND2 17B2 17D2 17D3 18B3 18C1 19B2 19C1 39D5

10/100M ETHERNET PHY  
DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC  
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SCALE NONE SHEET 18 OF 53  
REV. ACI: C ECS:1.0  
APPLE COMPUTER INC.  
D 051-6130-C



FIREWIRE PHYSICAL LOGIC

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

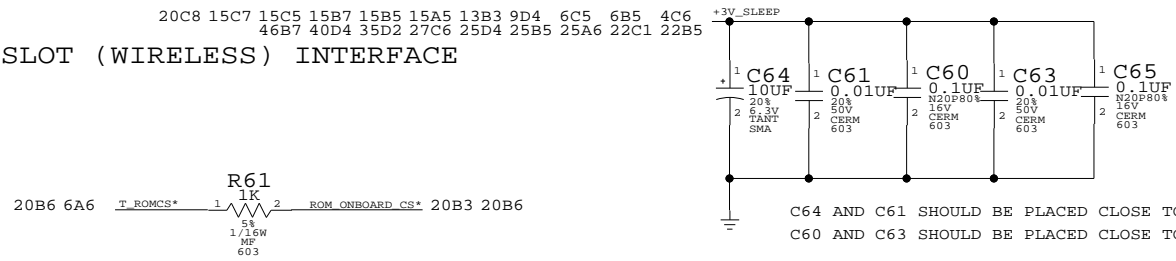
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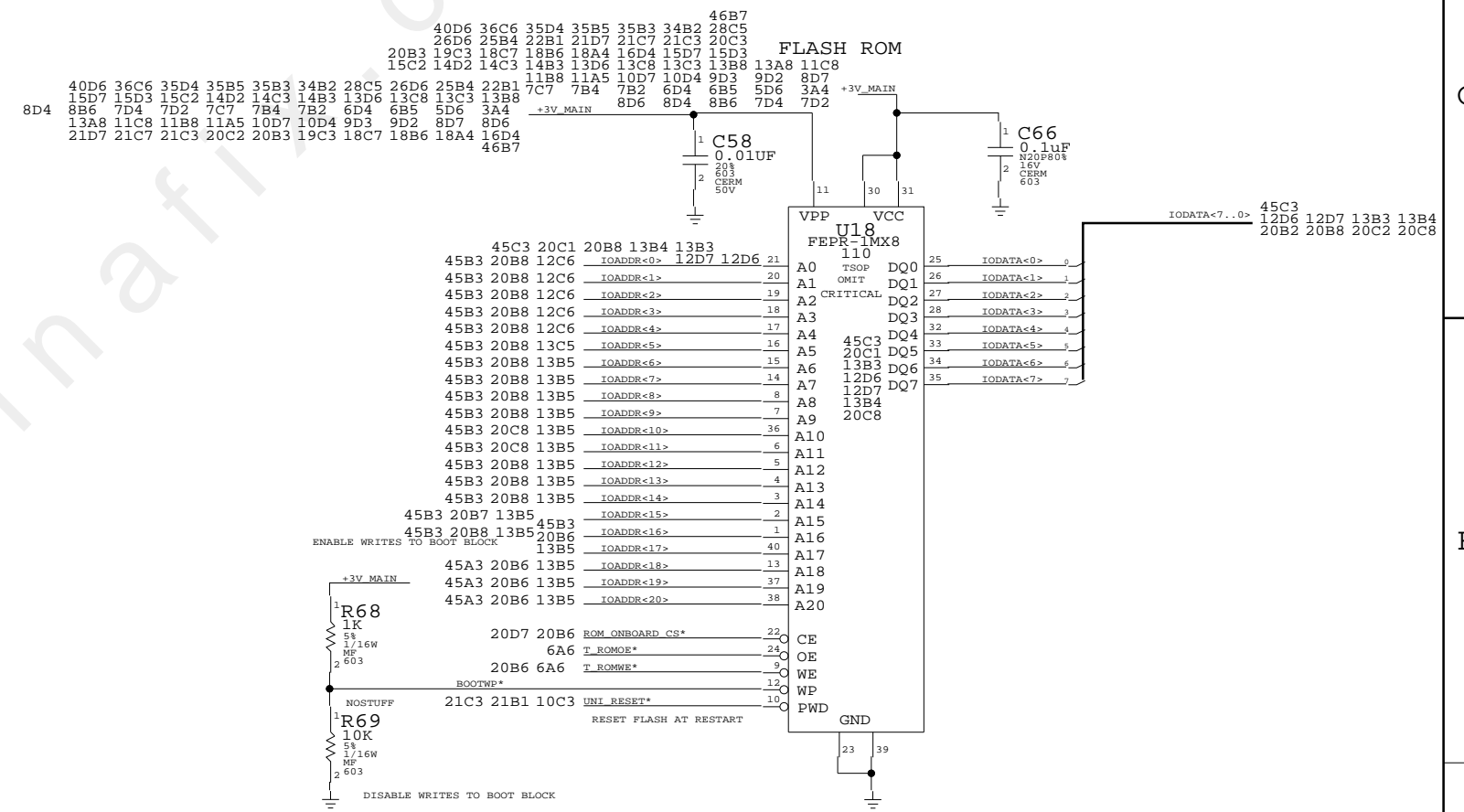
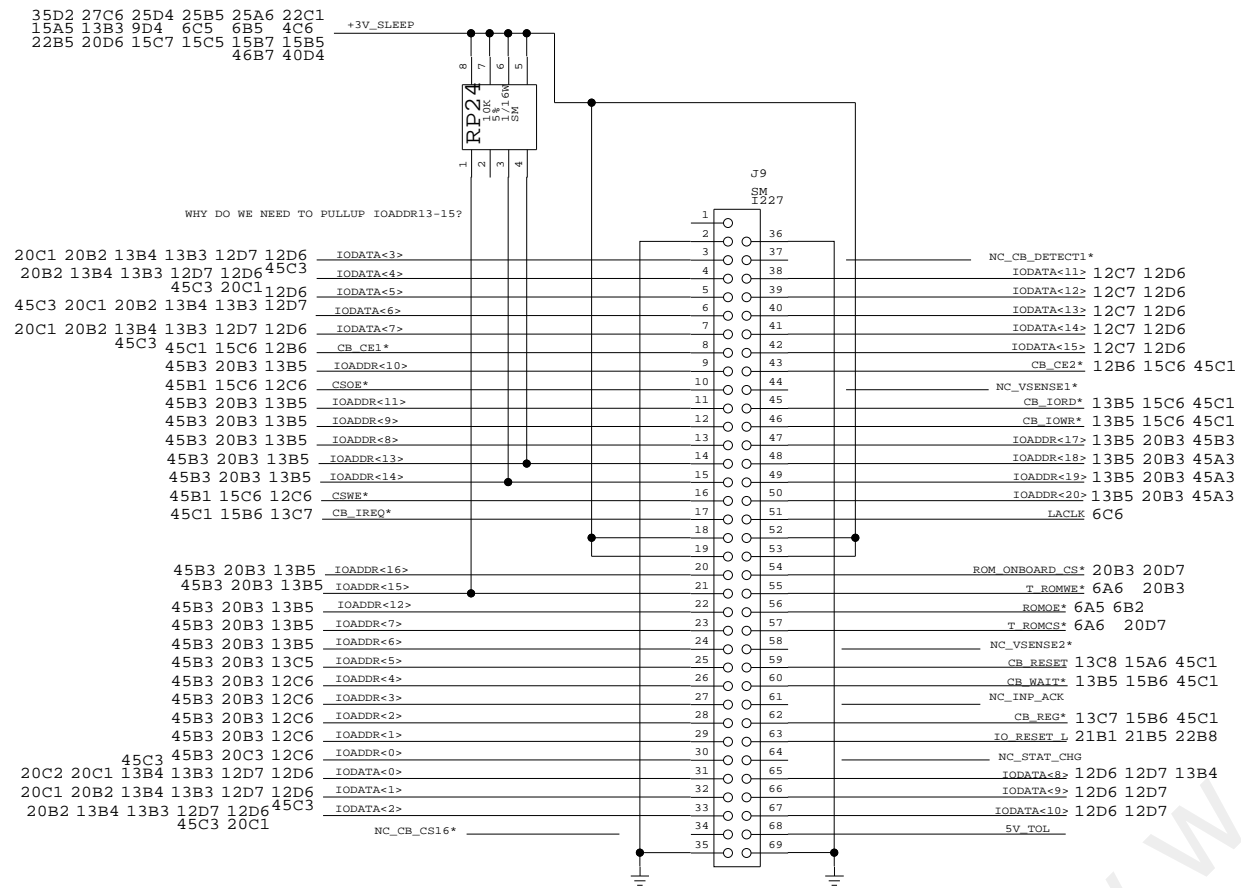
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6130-C	ACI: C ECS:1.C
SCALE		SHT	OF
		19	53

8 7 6 5 4 3 2 1

### CARDSLOT (WIRELESS) INTERFACE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1036	1	IC,ROM,CORE2001,IBOOK	U18	PROJECT	---
335S0350	1	BOOT ROM, BLANK	U18	PROJECT	OMIT



NOTE: 5V TOLERANCE LEAVE NC

#### CARDSLOT(WIRELESS) INTERFACE & BOOTROM

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	20 OF	53
NONE			

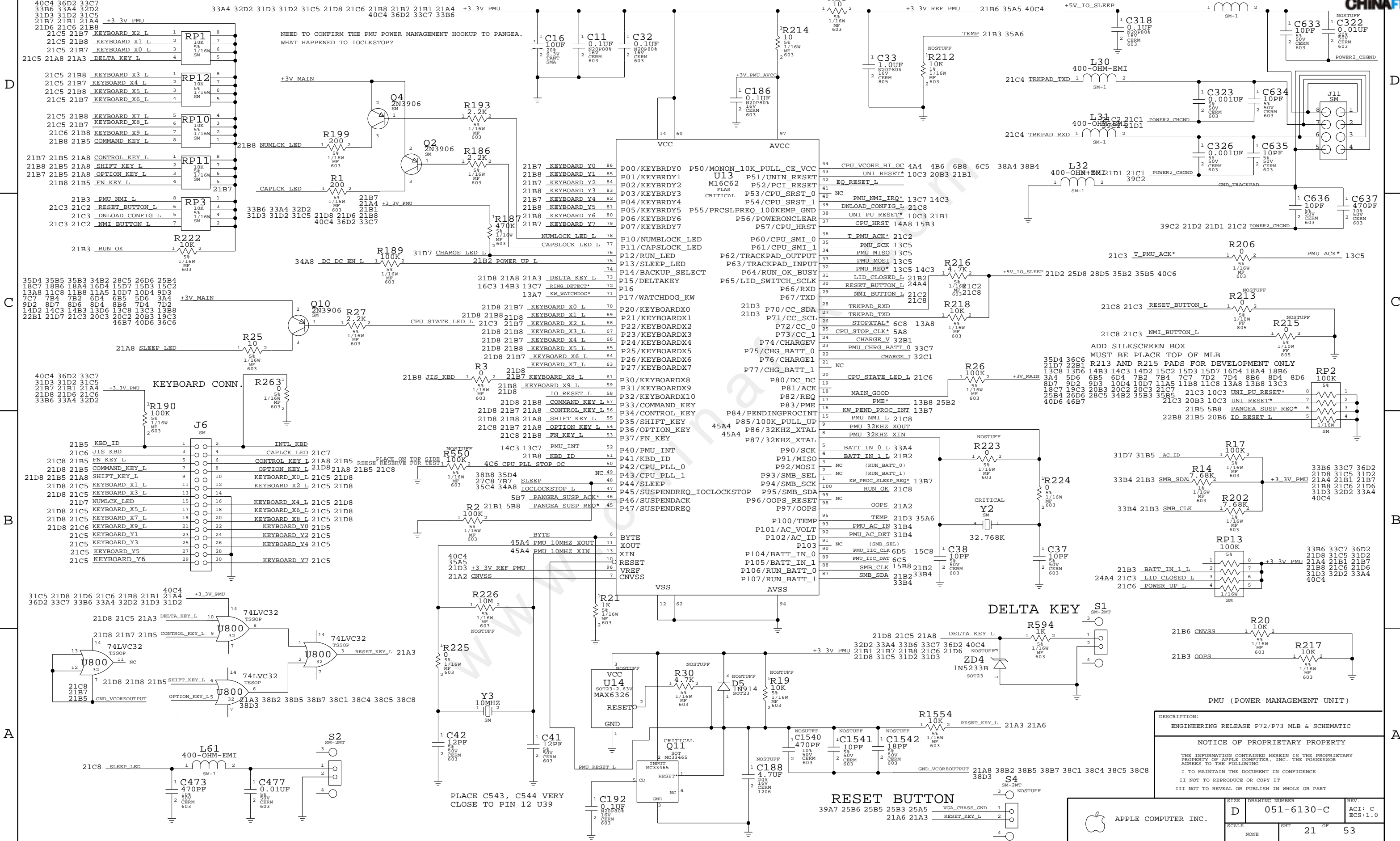
8 7 6 5 4 3 2 1





### PULL-UPS

### TRACKPAD CONN.



DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

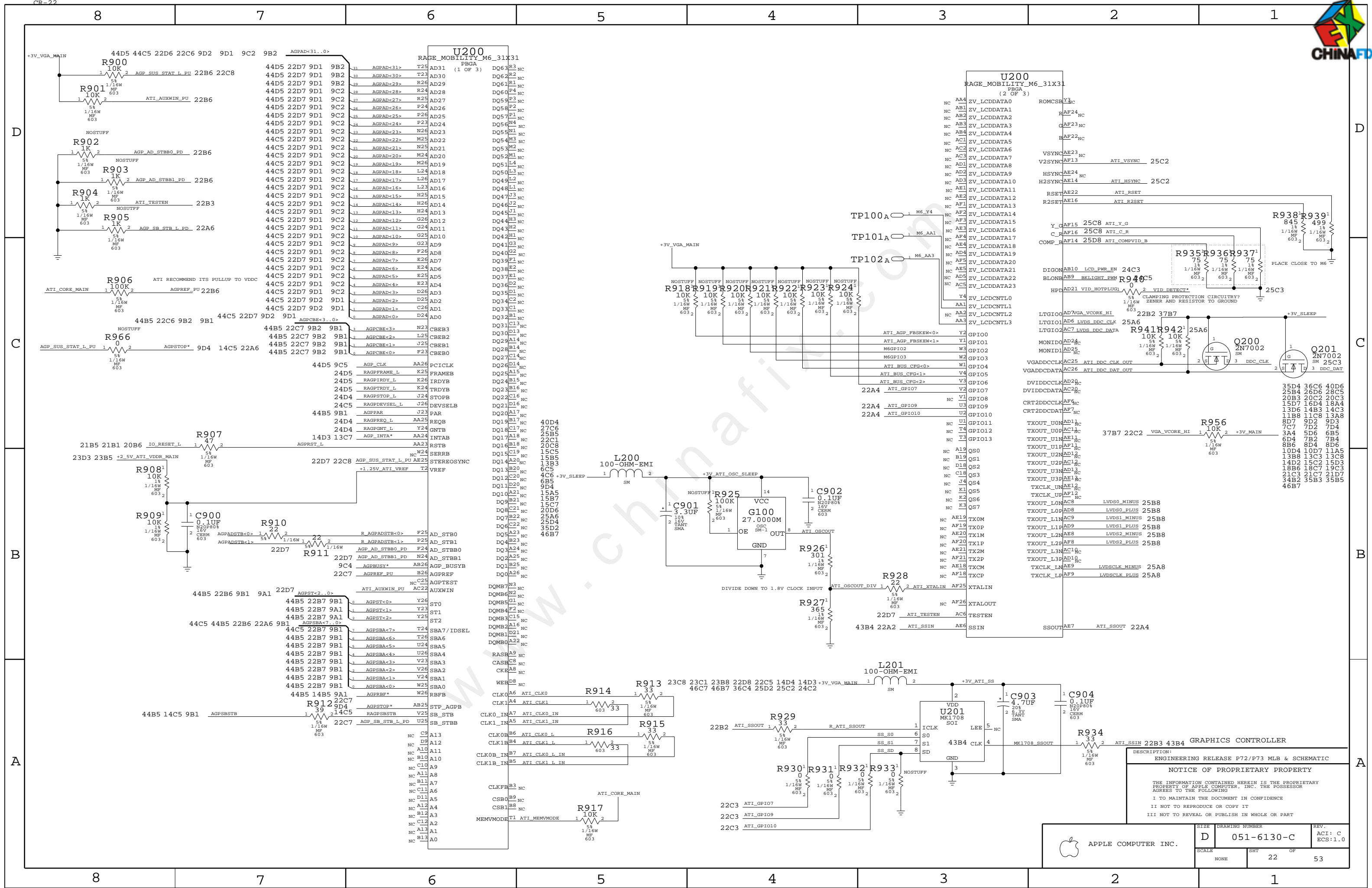
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APPLE COMPUTER INC.	SIZE	D	REV.	ACI: C
	DRAWING NUMBER	051-6130-C	REV.	ECS:1.0
SCALE	NONE	SHT	21	OF
			53	

PLACE C543, C544 VERY CLOSE TO PIN 12 U39

RESET BUTTON  
39A7 25B6 25B5 25B3 25A5 21A6 21A3





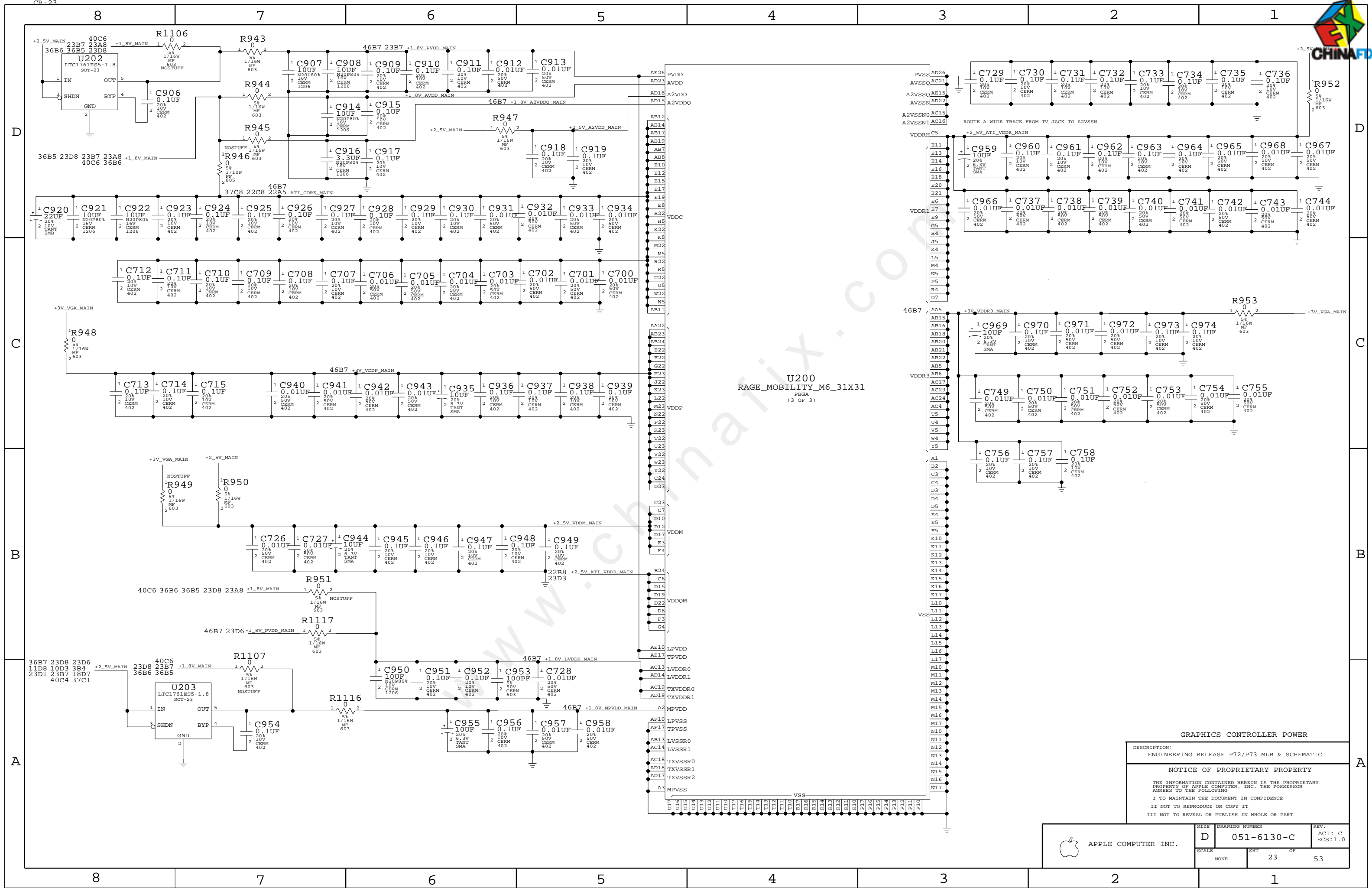
DESCRIPTION:  
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APPLE COMPUTER INC.	SIZE	D	REV.	ACI: C
	DRAWING NUMBER	051-6130-C	ECS:1.0	
SCALE	NONE	SHT	22	OF
				53



GRAPHICS CONTROLLER POWER

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

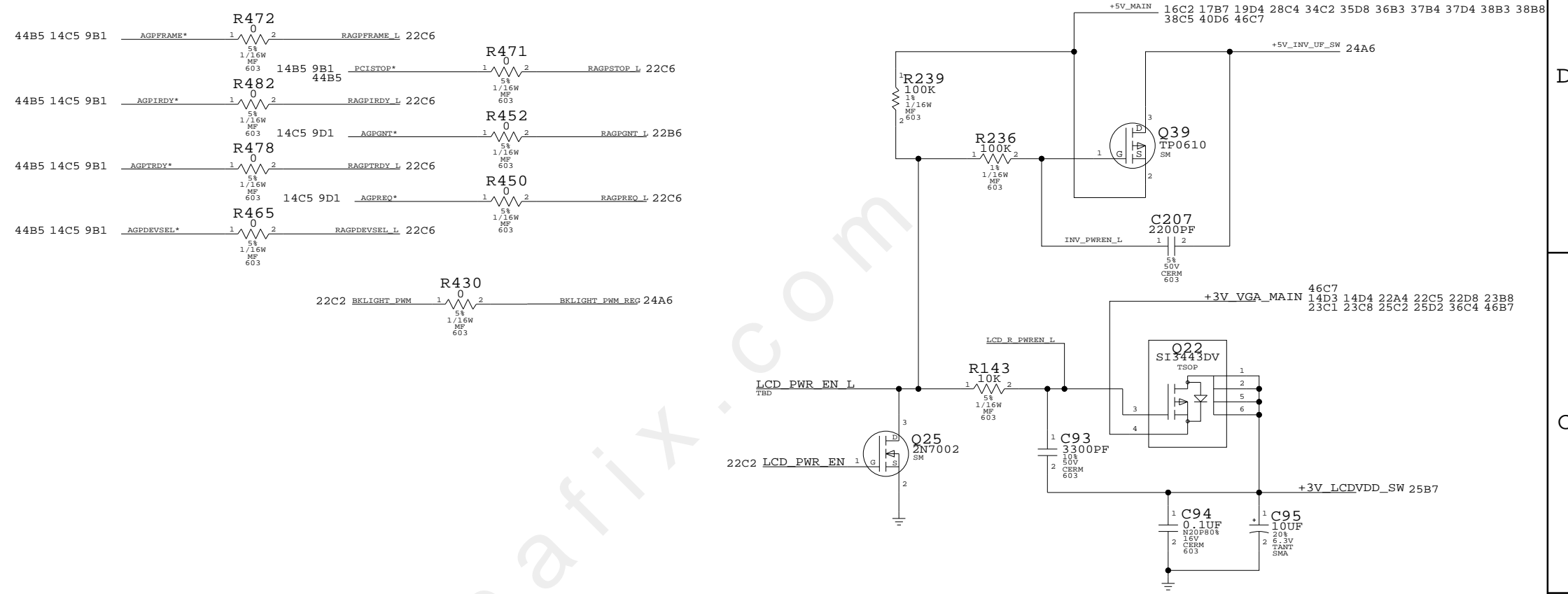
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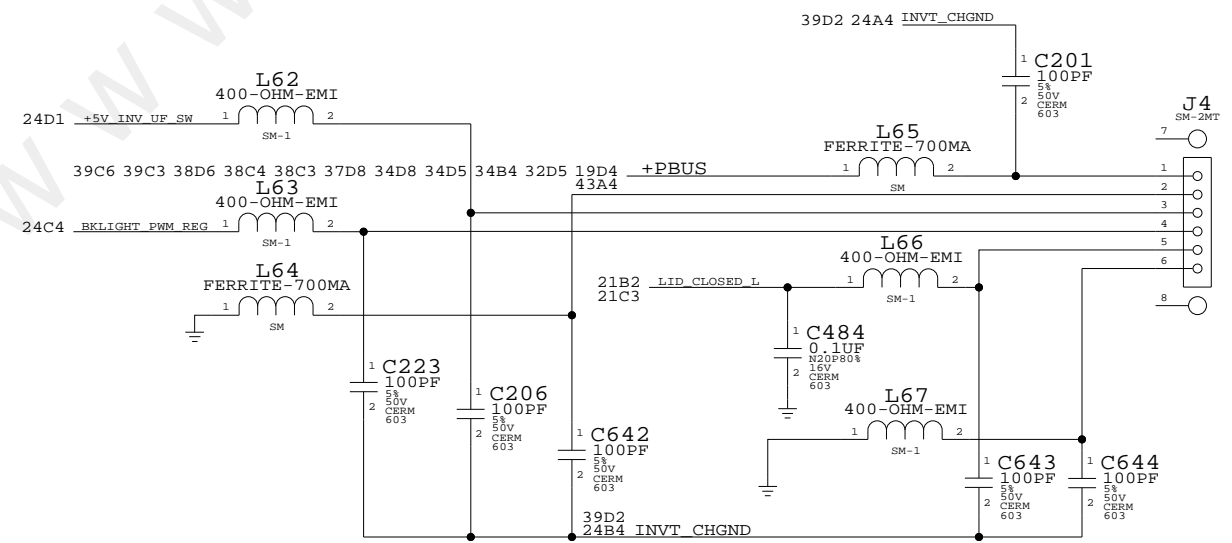
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	NONE	SHT	23 OF 53



# AGP BUS SERIES TERM



## INVERTER CONNECTOR



EMC\_GND DETERMINED BY ATC LAYOUT  
LCD I/F

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	24 OF	53
NONE			

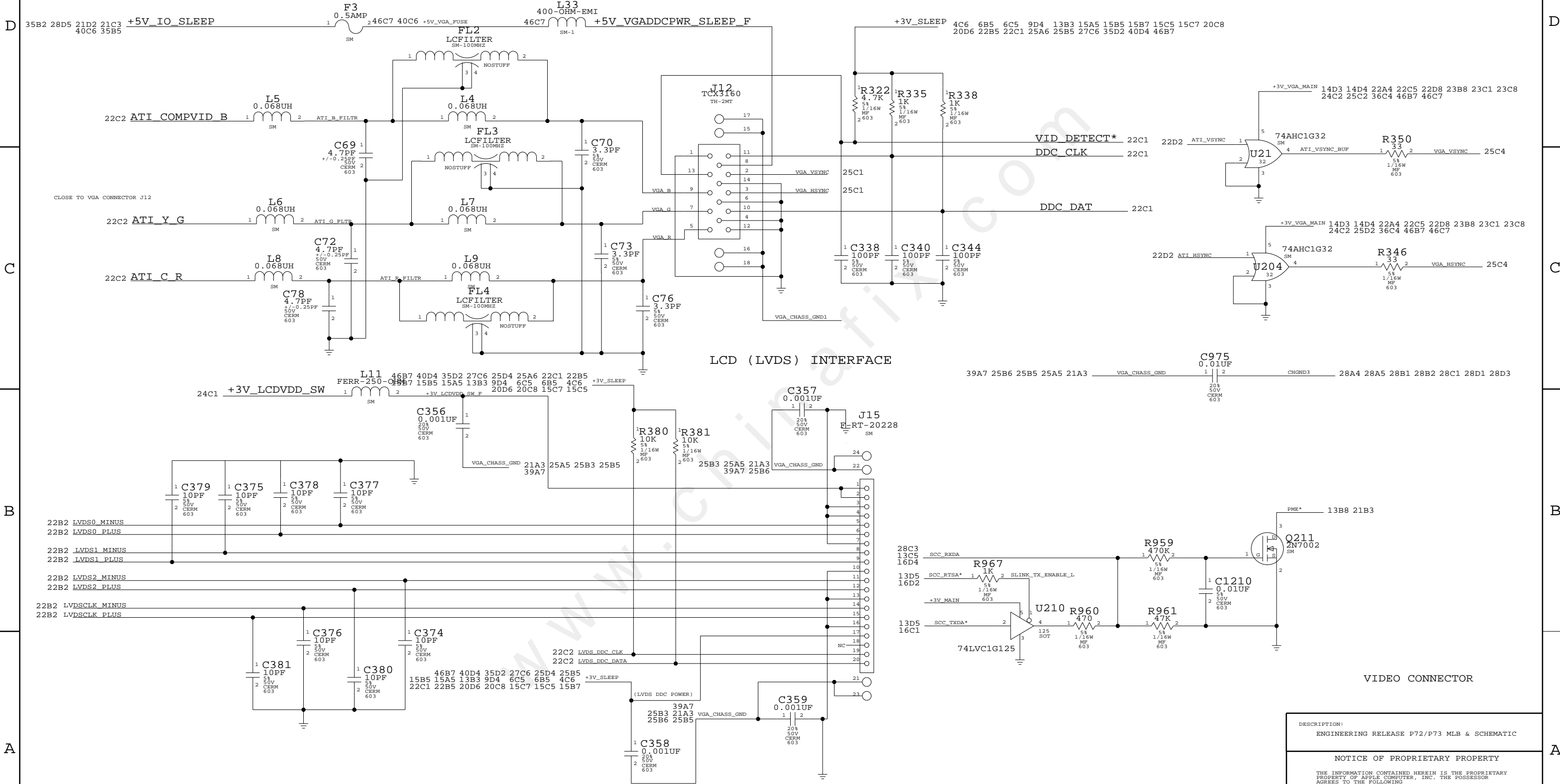


# Video Connectors

## EXTERNAL VIDEO (VGA) INTERFACE

### NOTES:

DUE TO EMI CONCERNS, THE FOLLOWING PINS (WHICH ARE LOCATED OVER THE CORRECT PORTION OF THE VGA\_CHASS\_GND1 PLANE) ARE CONNECTED TO THE VGA\_CHASS\_GND1 PLANE AS WELL AS DIGITAL GROUND.....  
 R90-2, C69-2, C70-2, C76-2, FL2-3/4, FL4-3/4, J12-1/4/6/14, C338-2, C339-2, C340-2, C344-2,

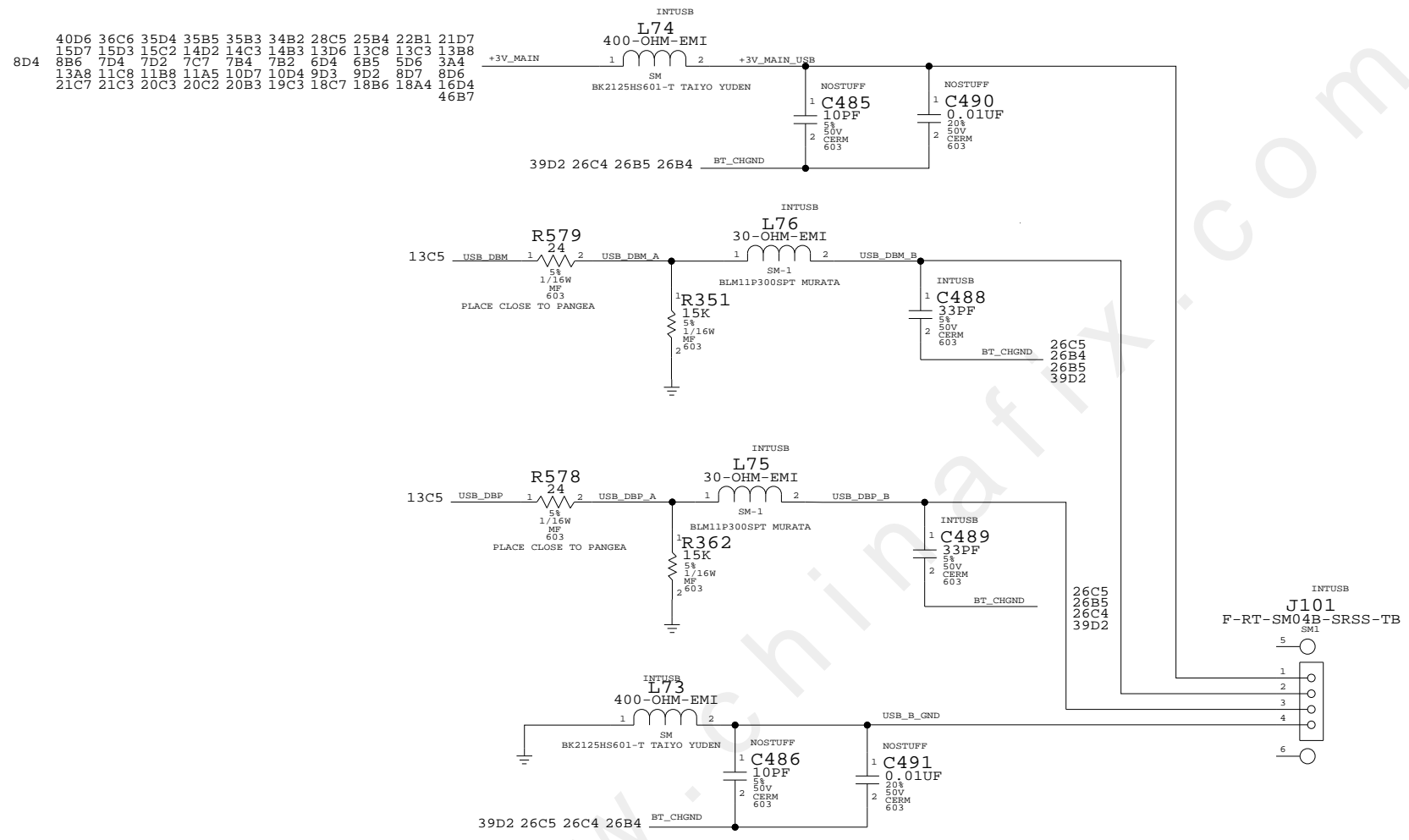


DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	25 OF	53
NONE			





### IRDA/BT USB CONNECTOR

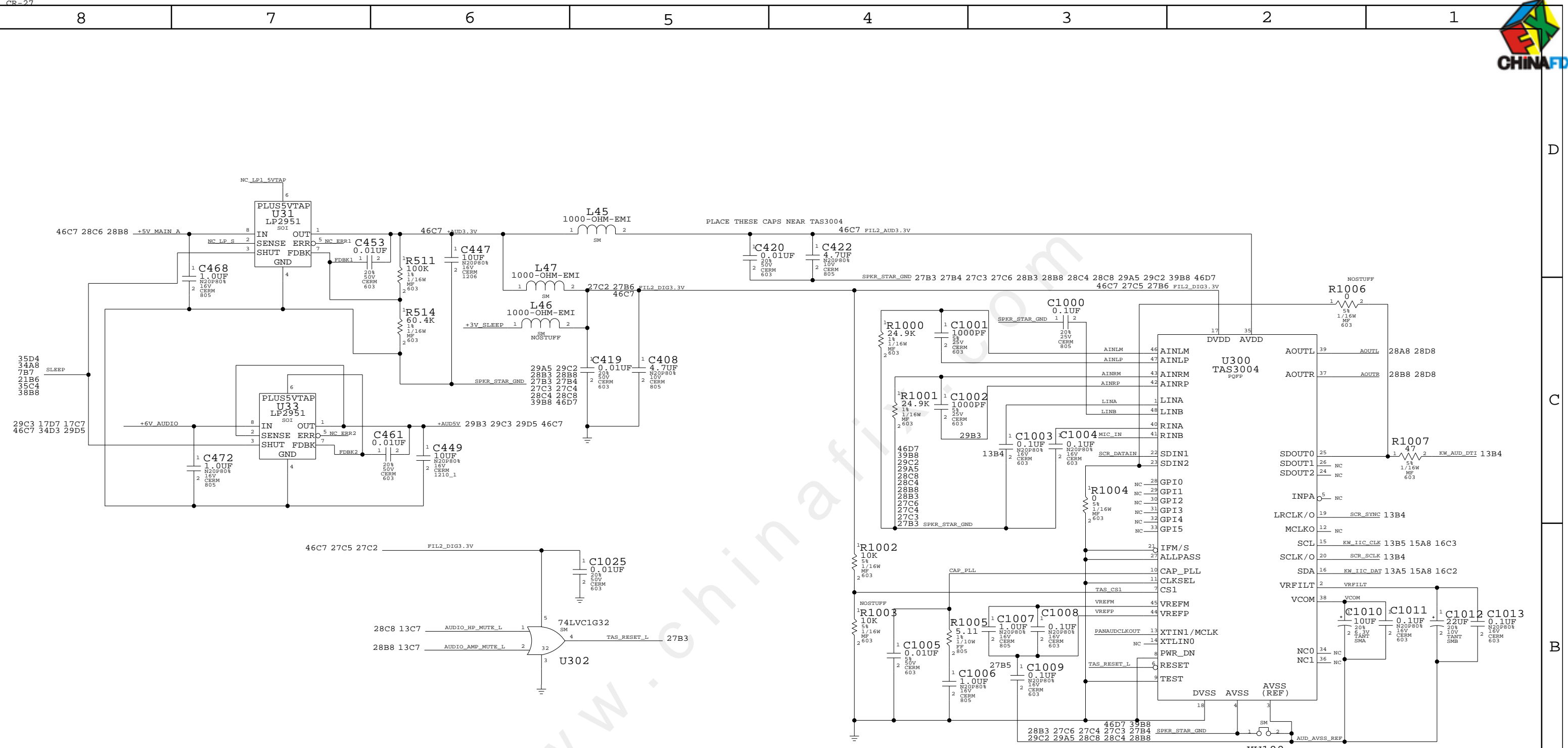
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	OF	53
NONE	26		



SNAPPER, CONTROL & D/A

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

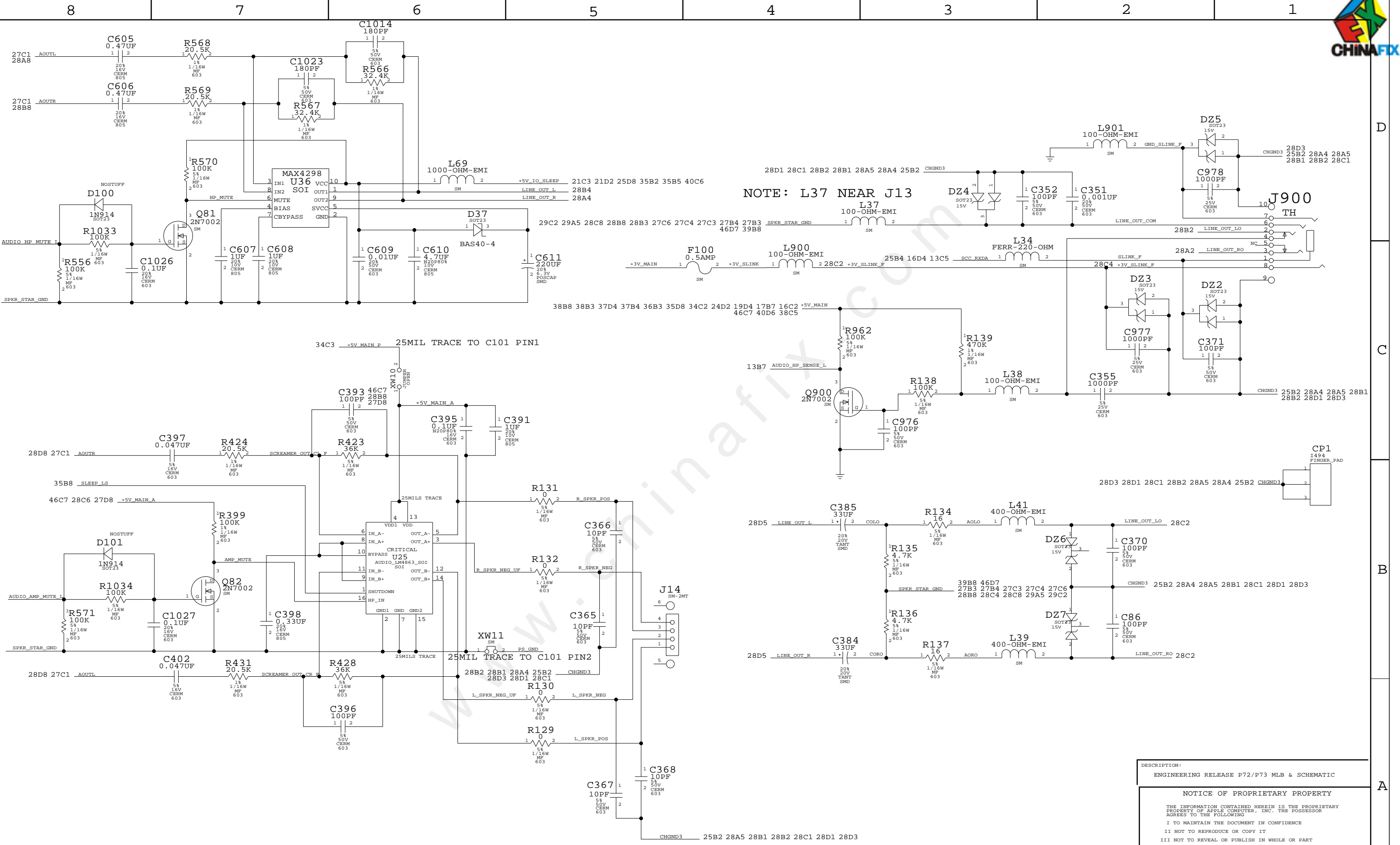
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	27 OF	53
NONE			



NOTE: L37 NEAR J13

### SNAPPER AUDIO, SPEAKER & HEADPHONE DRIVER

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: C ECS:1. B
	SCALE NONE	SHEET 28 OF 53	

8 7 6 5 4 3 2 1

D

D

C

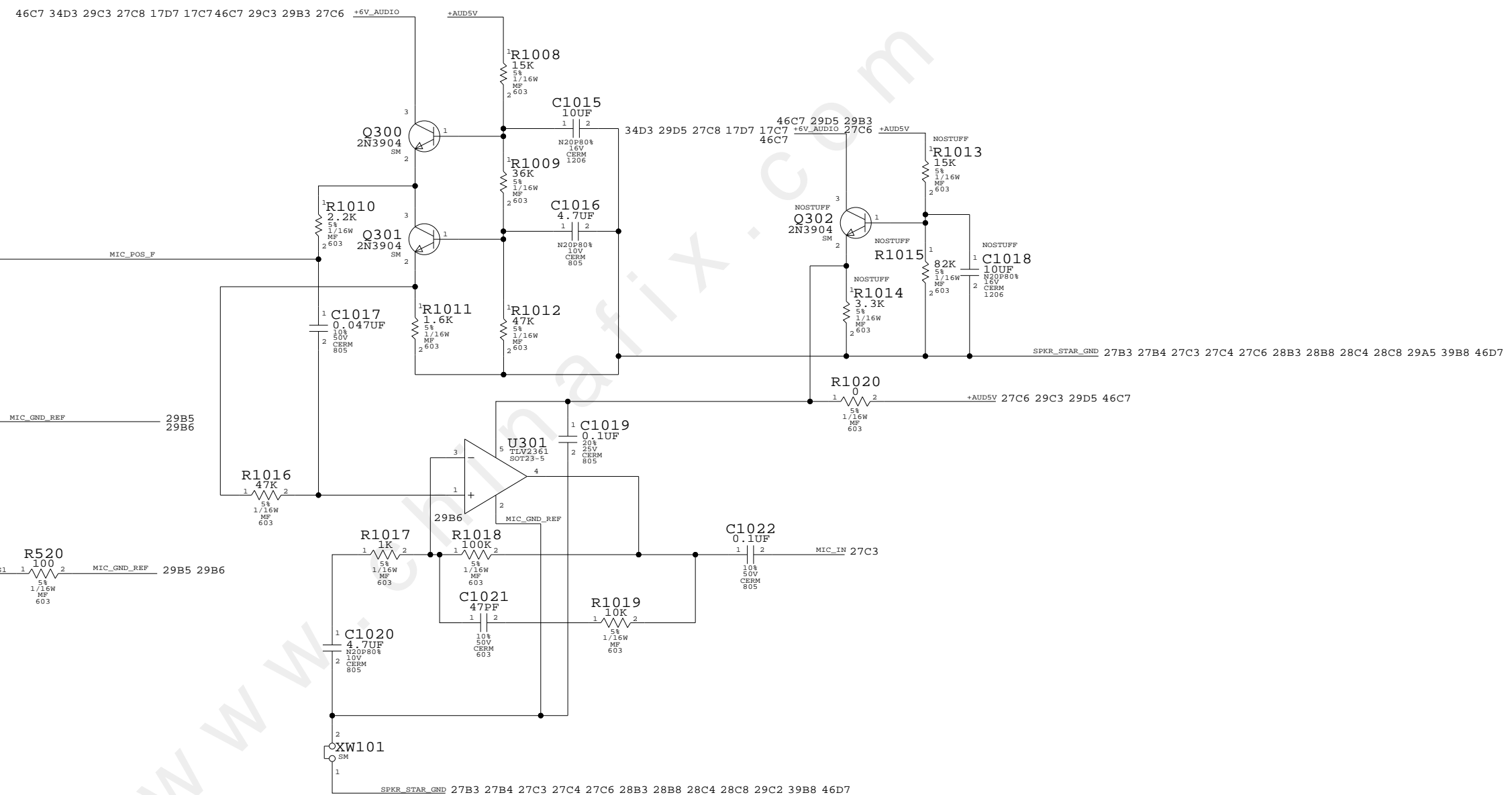
C

B

B

A

A



### SNAPPER AUDIO, MICROPHONE PREAMP

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

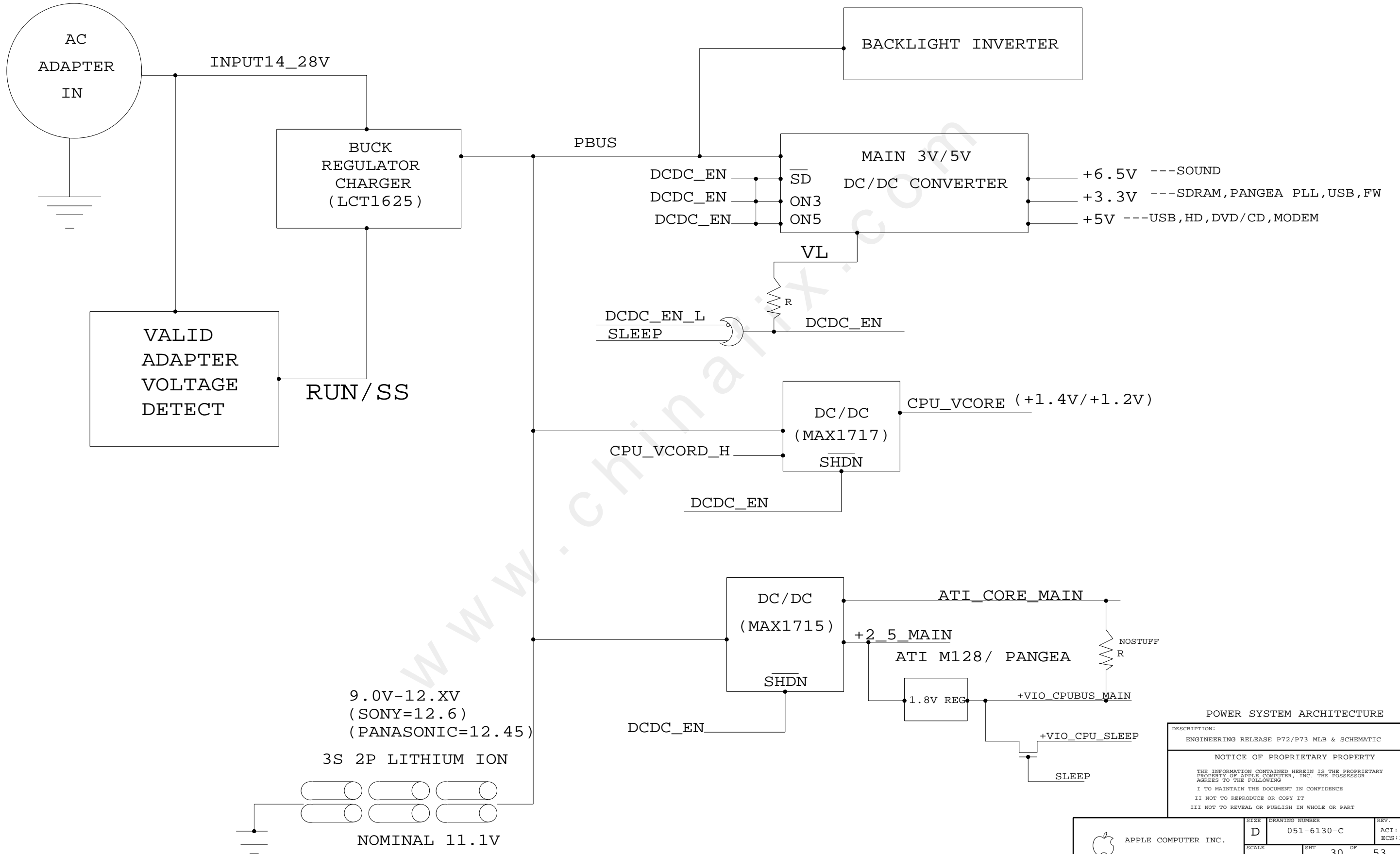
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT 29 OF 53		
NONE			

8 7 6 5 4 3 2 1



POWER SYSTEM ARCHITECTURE



POWER SYSTEM ARCHITECTURE

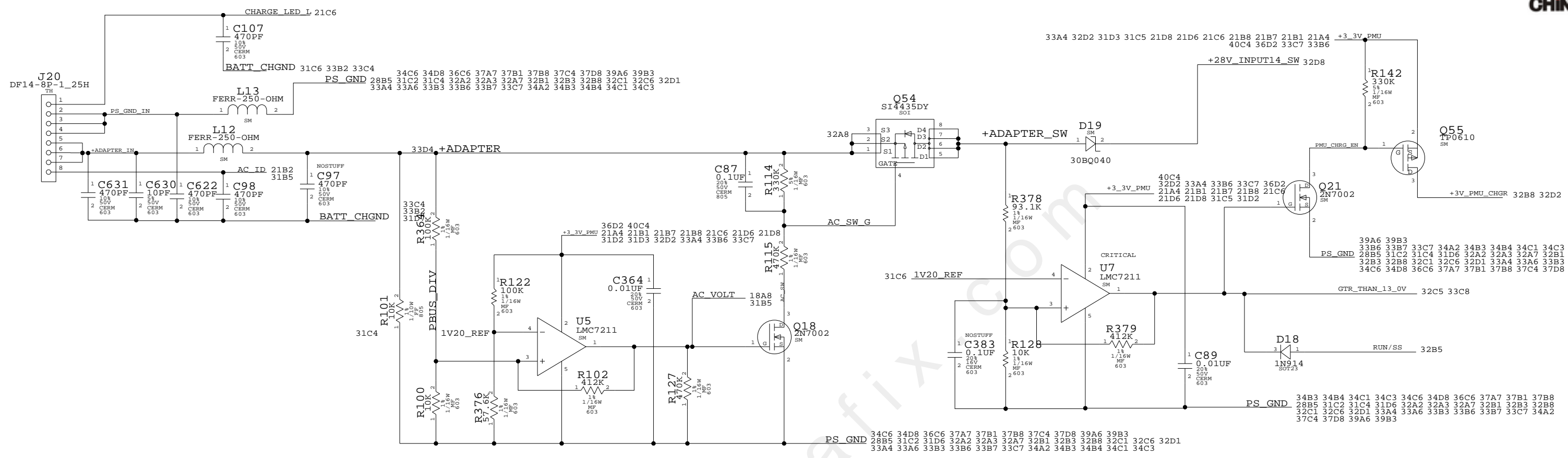
DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

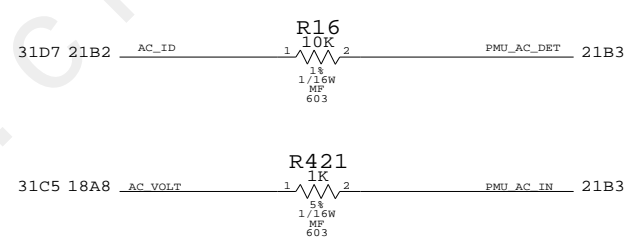
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	OF	
NONE	30	53	



GREATER THAN 13.5V DETECT



### DC-JACK INTERFACE

DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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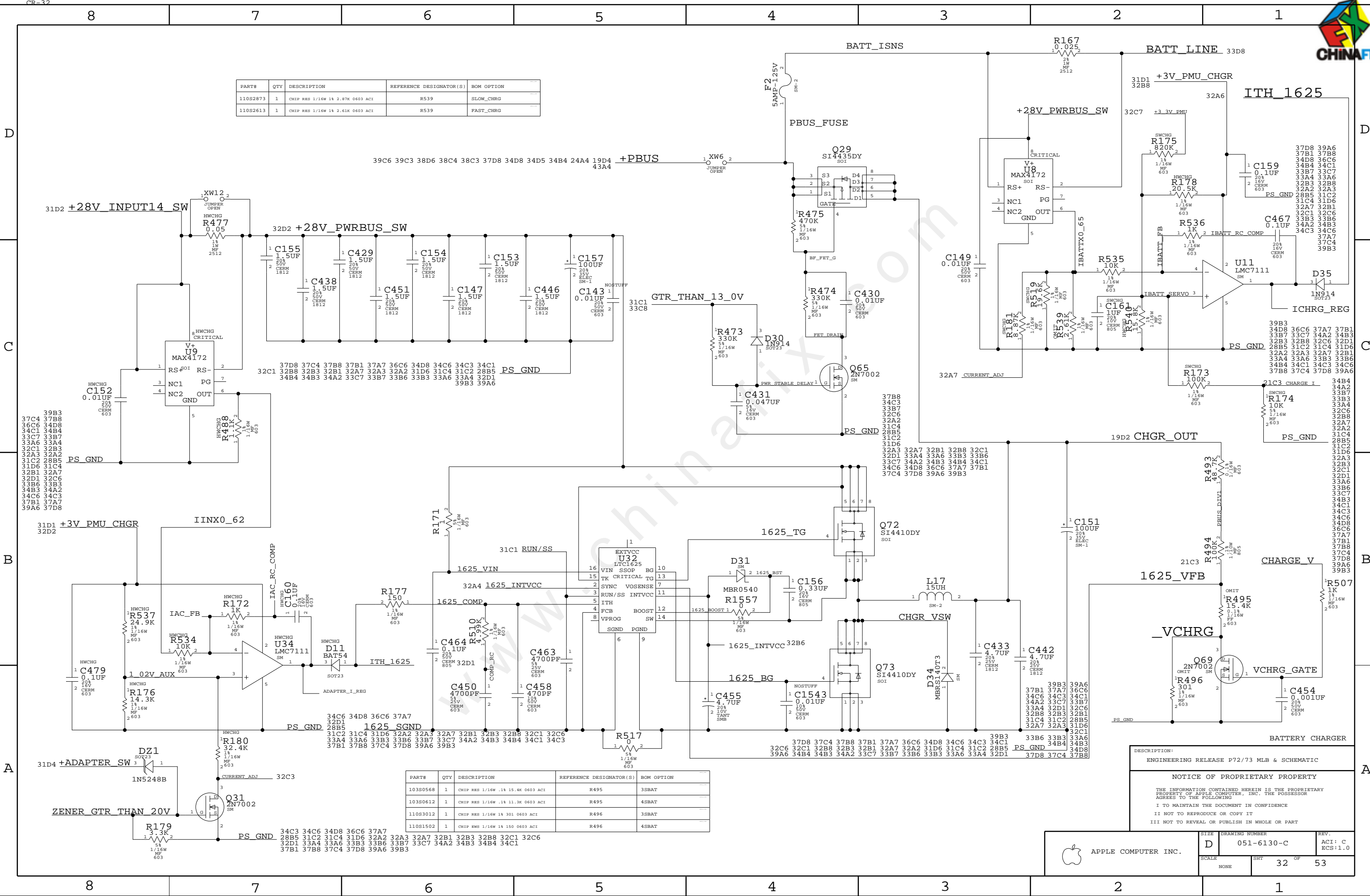
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.0
SCALE		SHT	OF
NONE		31	53

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S2873	1	CHIP RES 1/16W 1% 2.87K 0603 ACI	R539	SLOW_CHRG
110S2613	1	CHIP RES 1/16W 1% 2.61K 0603 ACI	R539	FAST_CHRG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
103S0568	1	CHIP RES 1/16W 1% 15.4K 0603 ACI	R495	3SBAT
103S0612	1	CHIP RES 1/16W 1% 11.3K 0603 ACI	R495	4SBAT
110S3012	1	CHIP RES 1/16W 1% 301 0603 ACI	R496	3SBAT
110S1502	1	CHIP RES 1/16W 1% 150 0603 ACI	R496	4SBAT

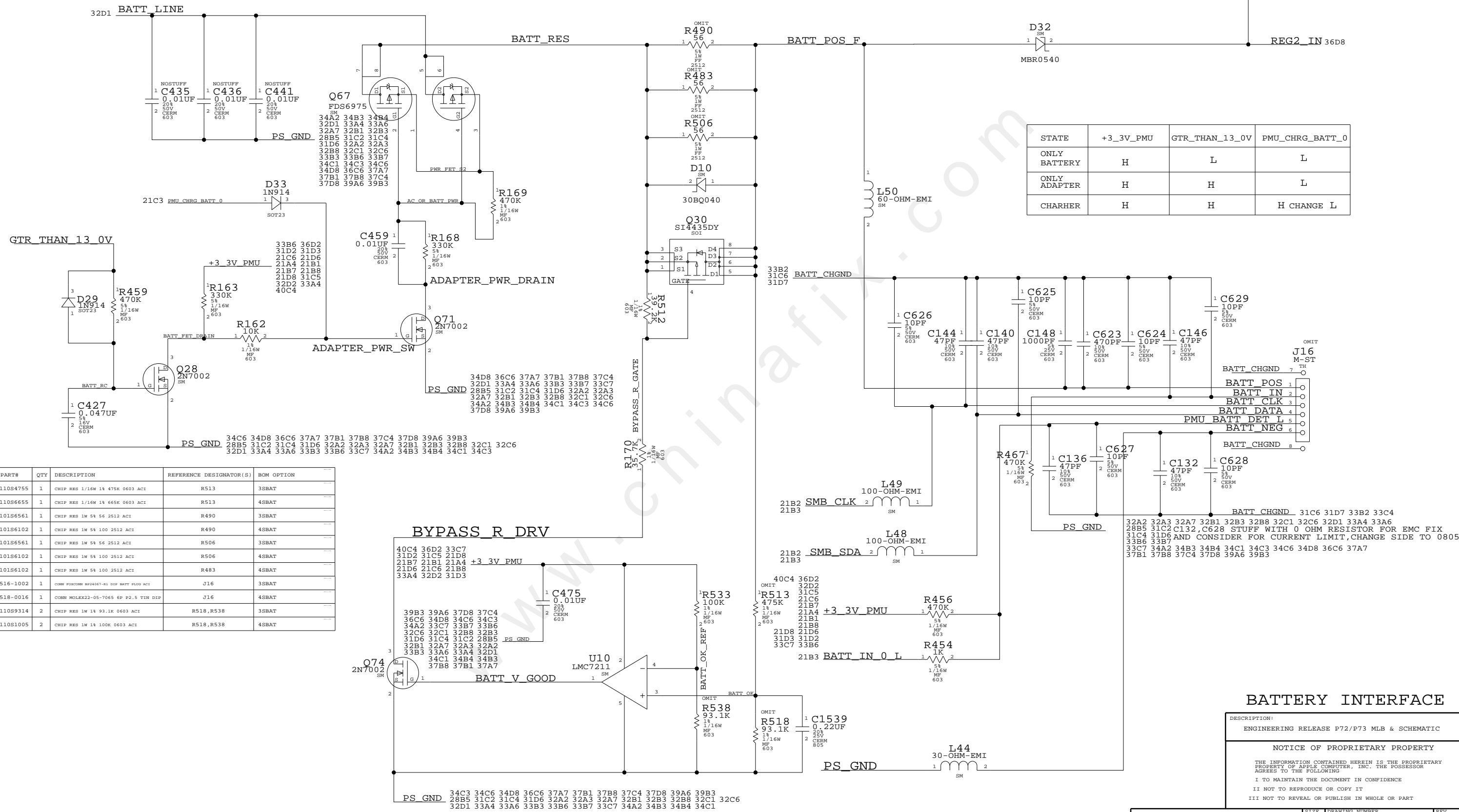
DESCRIPTION:  
ENGINEERING RELEASE P72/73 MLB & SCHEMATIC

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APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-6130-C	REV.	ACI: C
	SCALE	NONE	SHT	32	OF	53



# BATTERY INTERFACE



STATE	+3_3V_PMU	GTR_THAN_13_0V	PMU_CHRG_BATT_0
ONLY BATTERY	H	L	L
ONLY ADAPTER	H	H	L
CHARHER	H	H	H CHANGE L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S4755	1	CHIP RES 1/16W 1% 475K 0603 ACT	R513	3SBAT
110S6655	1	CHIP RES 1/16W 1% 665K 0603 ACT	R513	4SBAT
101S6561	1	CHIP RES 1W 5% 56 2512 ACT	R490	3SBAT
101S6102	1	CHIP RES 1W 5% 100 2512 ACT	R490	4SBAT
101S6561	1	CHIP RES 1W 5% 56 2512 ACT	R506	3SBAT
101S6102	1	CHIP RES 1W 5% 100 2512 ACT	R506	4SBAT
101S6102	1	CHIP RES 1W 5% 100 2512 ACT	R483	4SBAT
516-1002	1	CONN FORMDRM 8P24547-81 DSP BATT PLUG ACT	J16	3SBAT
518-0016	1	CONN MOLEX22-05-7065 6P P2.5 TIN DIP	J16	4SBAT
110S9314	2	CHIP RES 1W 1% 93.1K 0603 ACT	R518,R538	3SBAT
110S1005	2	CHIP RES 1W 1% 100K 0603 ACT	R518,R538	4SBAT

## BATTERY INTERFACE

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

### NOTICE OF PROPRIETARY PROPERTY

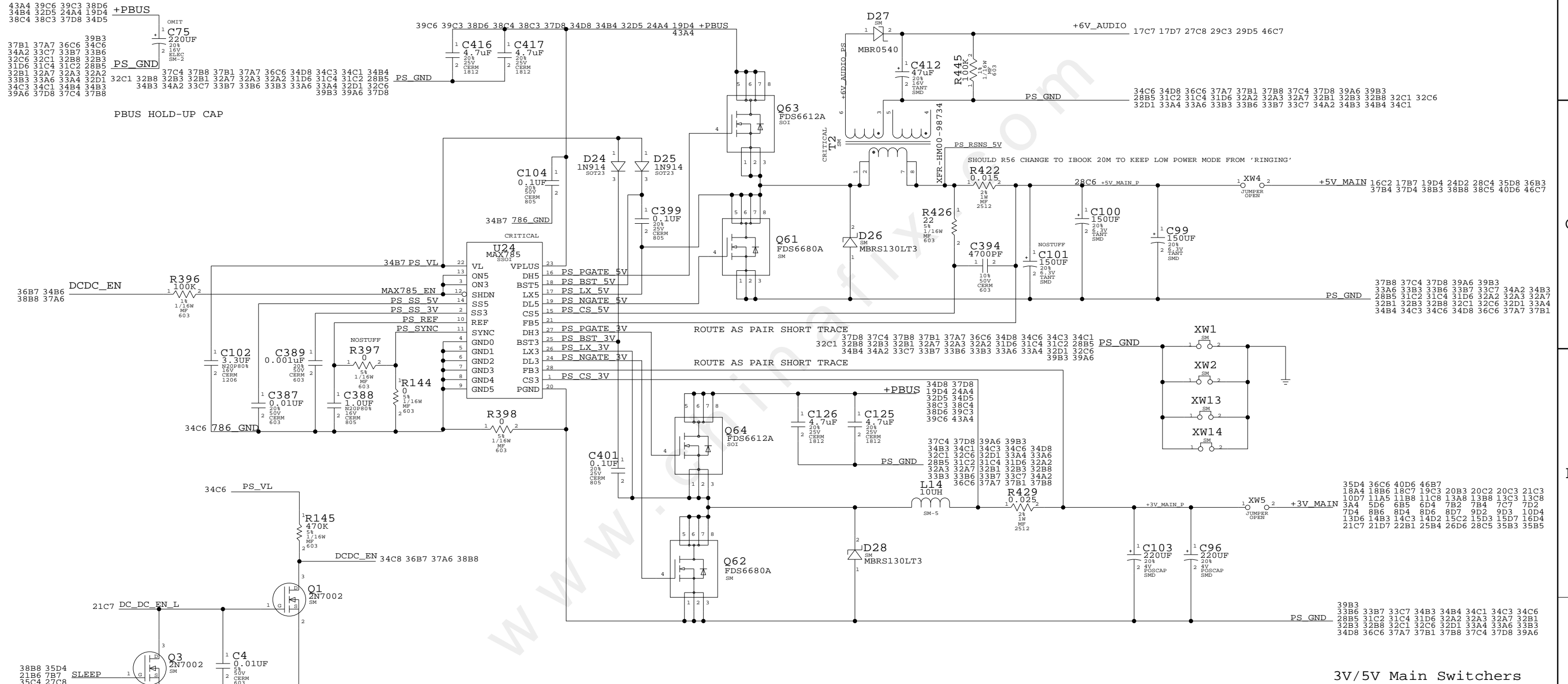
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6130-C	ACI: C ECS:1.A
SCALE		SHT	OF
		33	53



# 3V/5V Main Switchers

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
126S2228	1	ELEC 220UF/16V 20%	C75	3SBAT
126S1024	1	ELEC 100UF/35V 20%	C75	4SBAT



DC_DC_EN_L	DCDC_EN	SLEEP	SLEEP_L_LS	STATE
0	1	0	1	RUN
X	1	1	0	SLEEP
1	0	0	0	SHUTDOWN

3V/5V Main Switchers

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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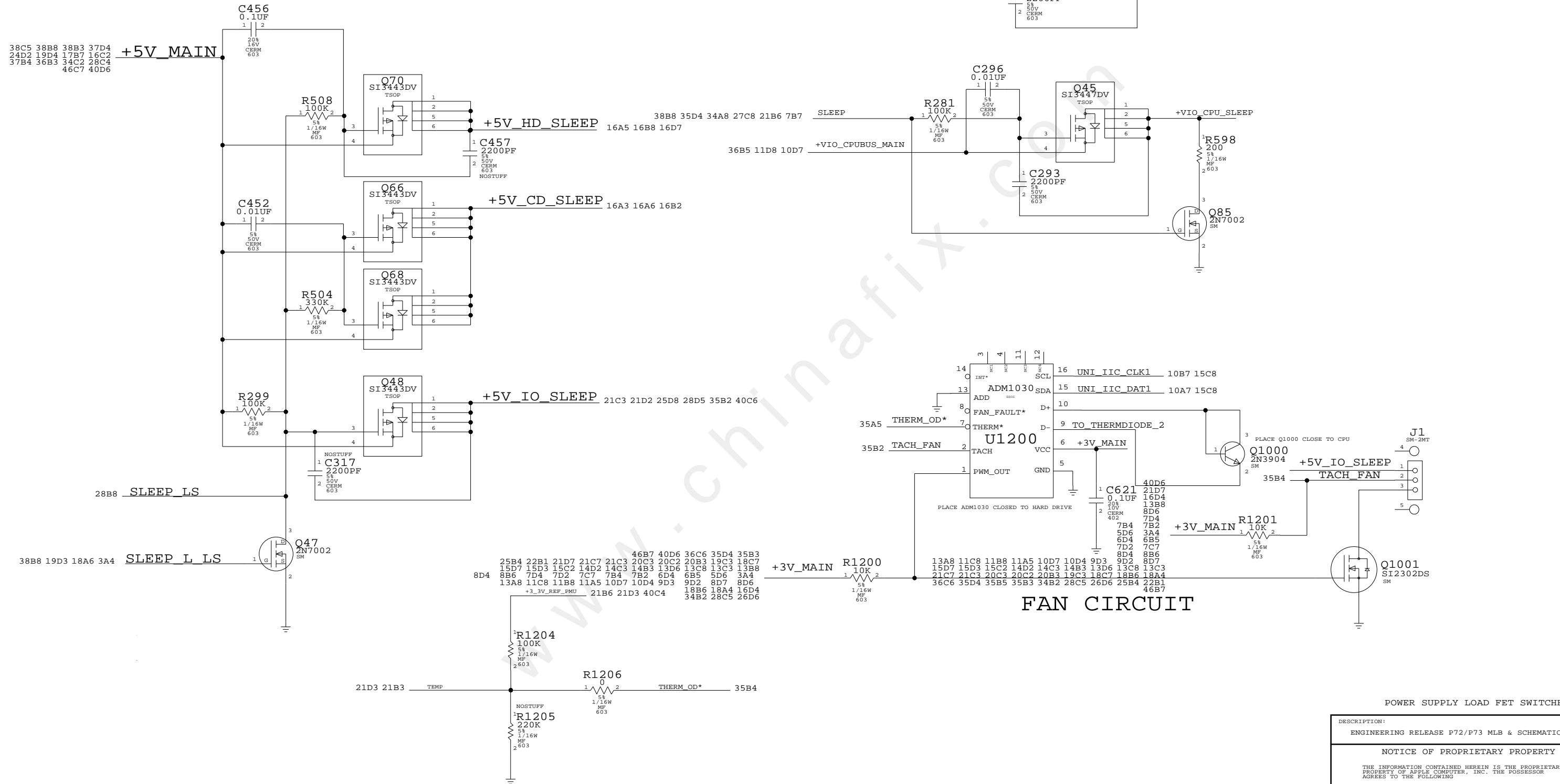
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	APPLE COMPUTER INC.		SIZE	D	DRAWING NUMBER	051-6130-C	REV.	ACT: C
	SCALE	NONE	SHT	34	OF	53	ECS:1.0	

LOW CURRENT. CAN WE CHANGE TO CHEAPER FET?

POWER FOR:

TRACKPAD  
VGA DDC POWER



### FAN CIRCUIT

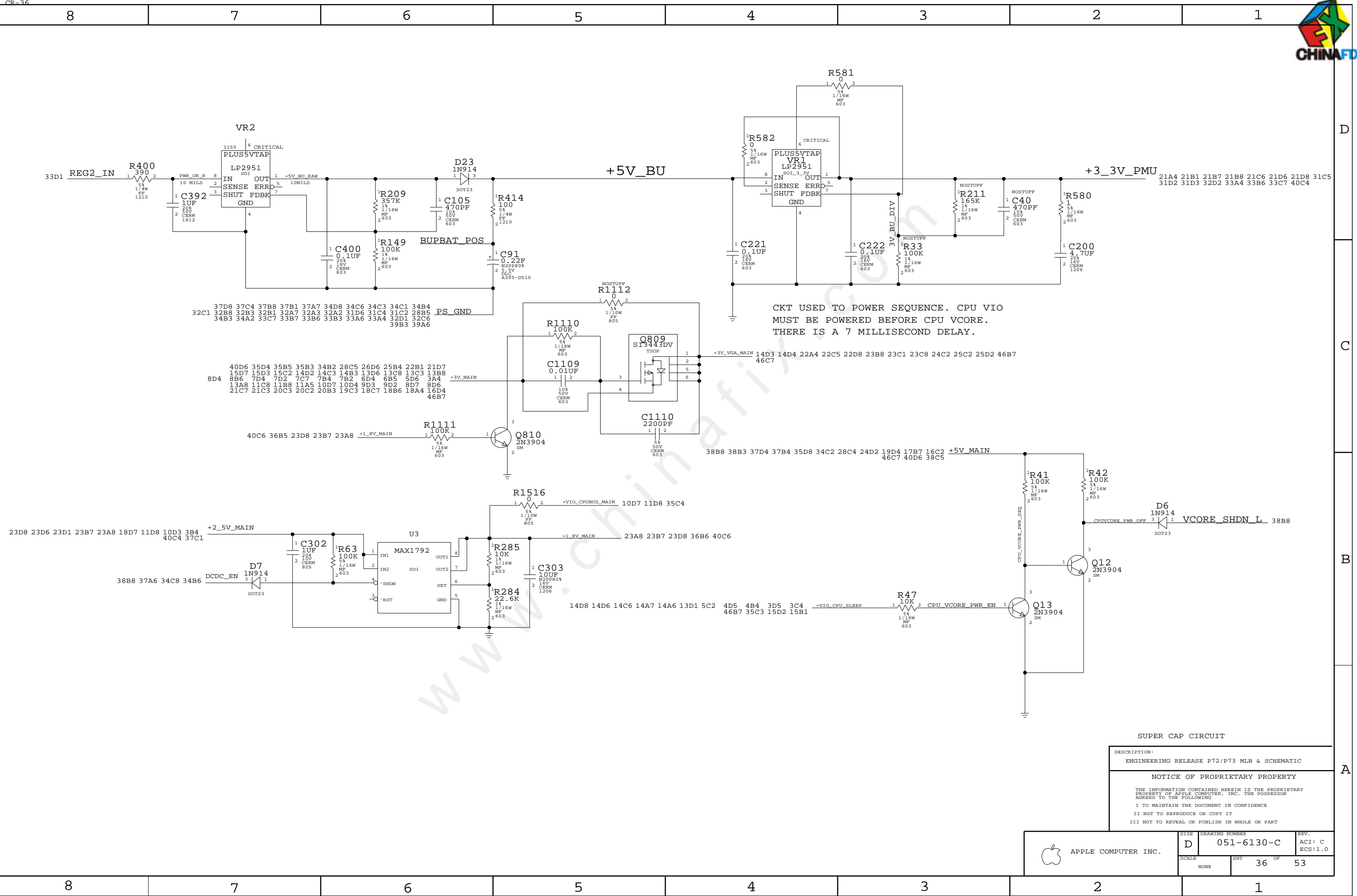
### POWER SUPPLY LOAD FET SWITCHES

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC5

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.B
SCALE	SHT	35 OF	53
NONE			



SUPER CAP CIRCUIT

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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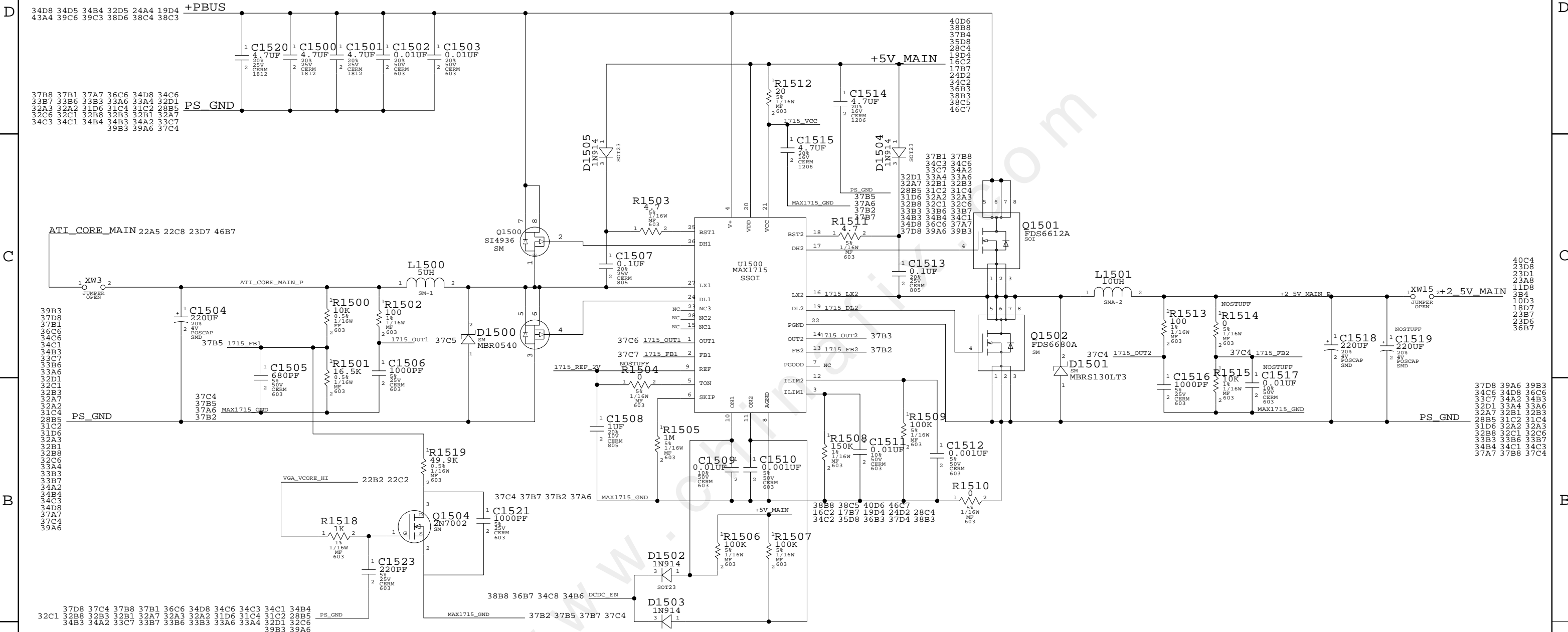
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: C
	SCALE NONE	SHEET 36 OF 53	ECS:1.0

8 7 6 5 4 3 2 1



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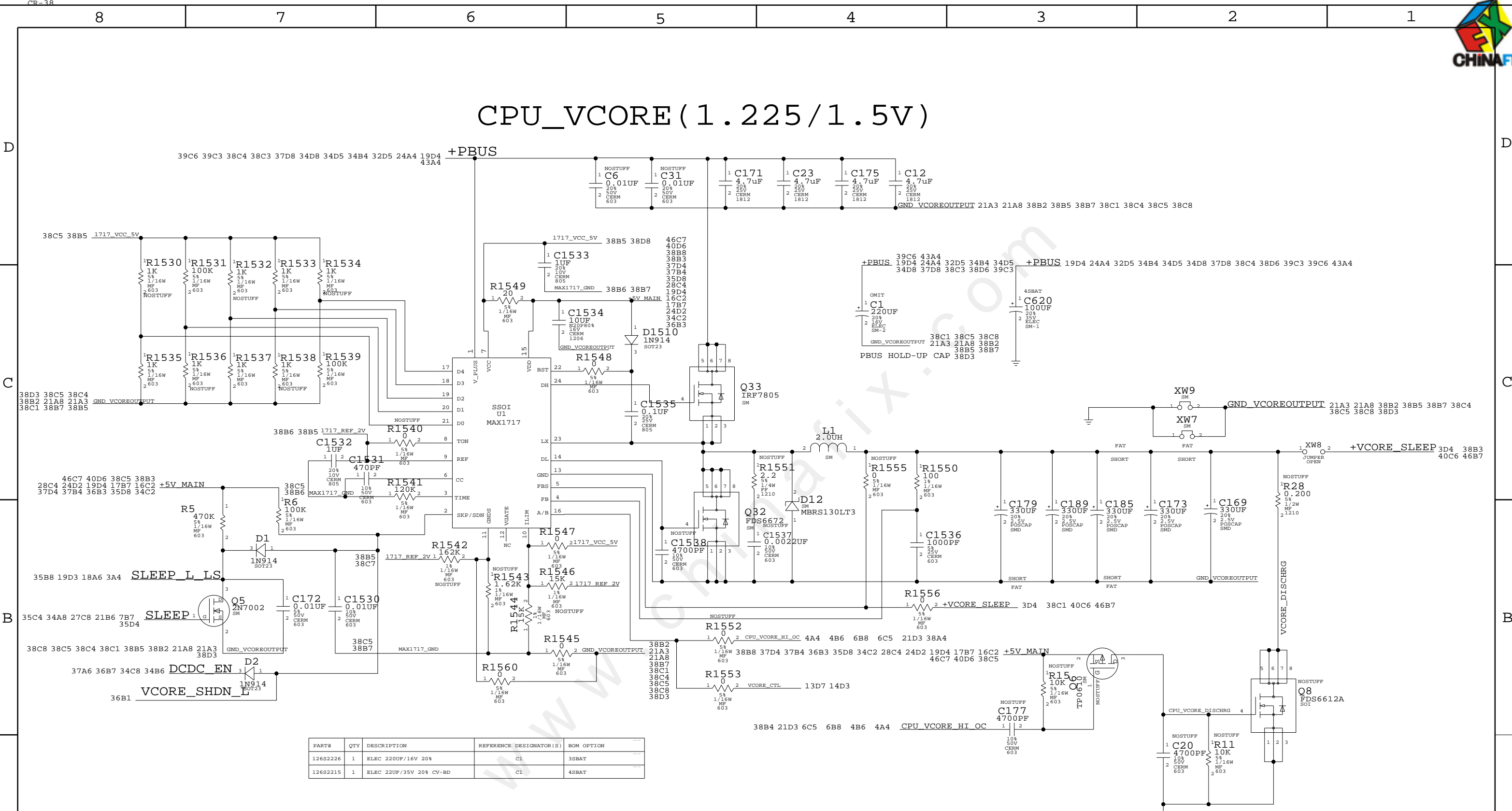
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	SCALE	SHT 37 OF 53	ACI: C ECS:1.0

8 7 6 5 4 3 2 1



# CPU\_VCORE (1.225/1.5V)



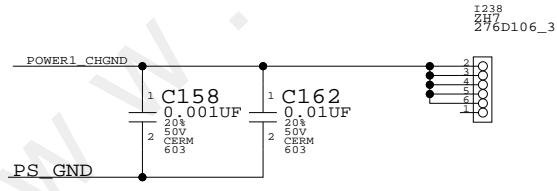
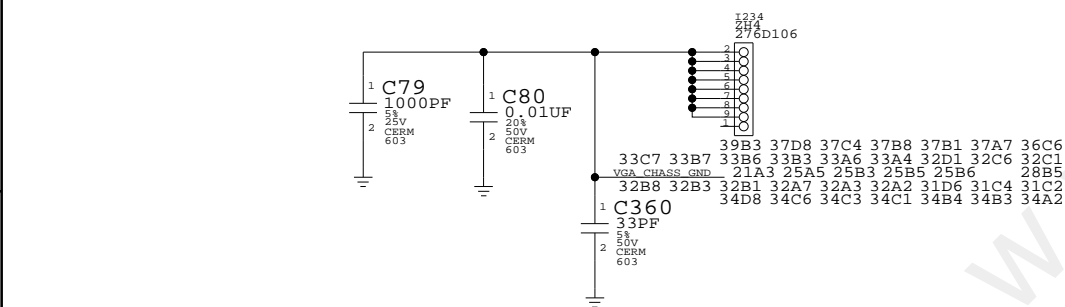
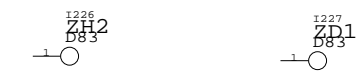
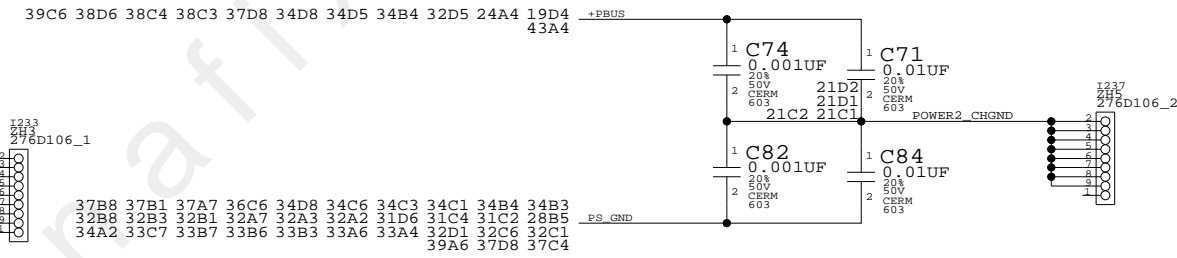
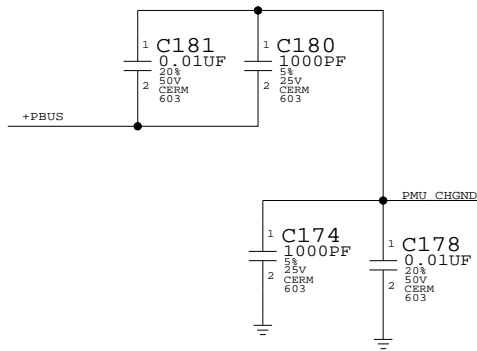
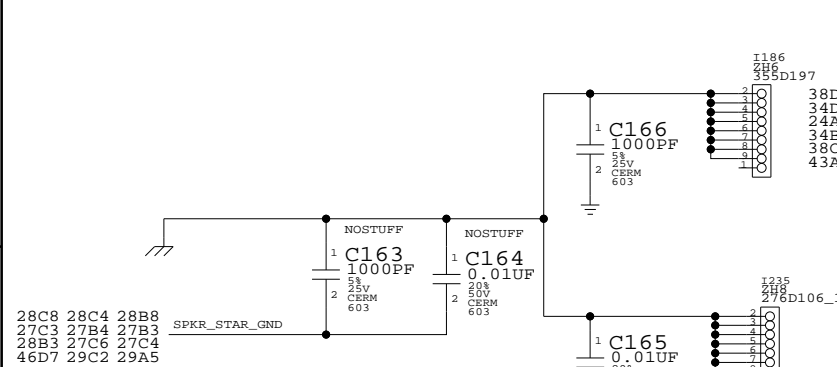
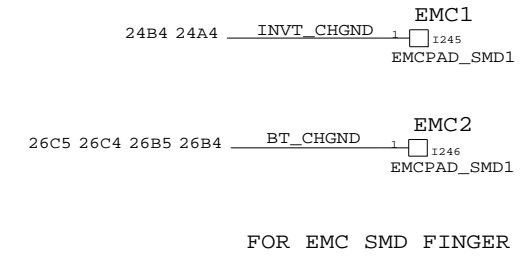
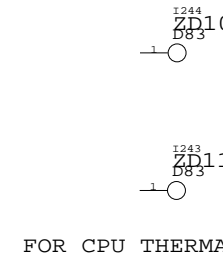
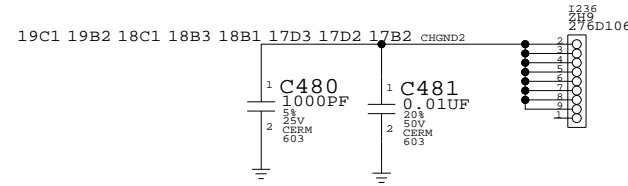
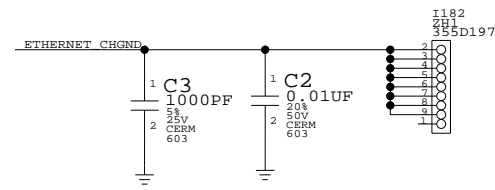
NOTE: SINCE ALL POWER SUPPLIES RESIDE ON THE SYSTEM BOARD JUMPERS HAVE BEEN INCORPORATED TO ALLOW ISOLATION OF THESE CIRCUITS FOR LOAD TESTING W/O THE RISK OF DAMAGE TO THE REST OF THE SYSTEM

CPU\_VCORE(1.2/1.4V) & 2.5V SWITCHERS  
 DESCRIPTION:  
 ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC  
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	SCALE	NONE	SHT	38	OF	53



8 7 6 5 4 3 2 1



BATTERY LOCK HOLE 4MM

TOOLING HOLES

DESCRIPTION:  
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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SCALE		SHT	OF
NONE		39	53

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	
+5V_MAIN		5	38B3 38B8 38C5 46C7
+3V_MAIN		3.3	16C2 17B7 19D4 24D2 28C4
		0	34C2 35D8 36B3 37B4 37D4
+2_5V_SLEEP	10	2.5	
+VCORE_SLEEP	10	1.8	
+3V_AVDD5_PANGEA_MAIN	10	3.3	3D4 38B3 38C1 46B7
+3V_AVDD4_PANGEA_MAIN	10	3.3	5D6
+3V_AVDD6_PANGEA_MAIN	10	3.3	6D3
AGPVREF	10	3.3	9D2
+3V_AMVDD_PANGEA_MAIN	10	3.3	9D4
PANGEA_TEI		0	10C7 11A8
ETH_RXD_PD		0	10B7
GBE_REFCLK		0	10B7 10D2
+3V_PHY_AVDD_MAIN		3.3	10B7 10D2
+VP_CPS			19B5 19B7 19D6 40C6
+3V_FW_MAIN		3.3	19C7
+3V_PHY_AVDD_MAIN		3.3	19B3 19B5 19B7 19C6
+PBUS_FW_SW			19B5 19B7 19D6 40C6
+FW_VP_FUSE_SW			19C8 19D3
+VP_SW			19D2
+VP_CONN_SW			19D2
GNDRET_FW			19D2
+5V_IO_SLEEP	20		19C1 19C2
+5V_VGA_FUSE	20		21C3 21D2 25D8 28D5 35B2
+1_8V_MAIN	10	1.8	35B5 46C7
+1_8V_1644_LX	10		23A8 23B7 23D8 36B5 36B6
+1_8V_1644_FB	10		

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	
+3V_SLEEP	25	3.3	4C6 6B5 6C5 9D4 13B3 15A5 15B5 15B7 15C5 15C7 20C8
+3V_VDDA3_PANGEA_MAIN	10	3.3	20D6 22B5 22C1 25A6 25B5 25D4 27C6 35D2 46B7
+3V_VDDA3_PANGEA_MAIN	10	3.3	13D6 40D4
+3V_VDDA3_PANGEA_MAIN	10	3.3	13D6 40D4
+3V_VDDA3_PANGEA_MAIN	10	3.3	13D6 40D4
VDD_USB	10	3.3	13C5
USB_PWR_A		3.3	13C5 17A7
USB_PWR_B		3.3	13C5 17A7
USB_PWR_FLT_AB		5	
USB_PWR_FLT_CD		5	
+3_3V_PMU	10	3.3	21A4 21B1 21B7 21B8 21C6 21D6 21D8 31C5 31D2 31D3 32D2
+3_3V_REF_PMU	10	3.3	21B6 21D3 35A5 33A4 33B6 33C7 36D2
+2_5V_ATILPVDD_MAIN	10	2.5	
+2_5V_F_A2VDDATI_MAIN	10	2.5	
+2_5V_MAIN	10	2.5	
+3V_AGPVDD_MAIN	10	3.3	3B4 10D3 11D8 18D7 23A8 23B7 23D1 23D6 23D8 36B7 37C1
+3V_VDDA1_PANGEA_MAIN	10	3.3	9D3
+3V_VDDA2_PANGEA_MAIN	10	3.3	13D6
MOBM3G1	10	0	13D6
MOBM3G2	10	0	
MOBM3G3	10	0	
MOBM3V1	10	2.5	
MOBM3V2	10	2.5	
MOBM3V3	10	2.5	
TXVSSR1	10	0	
PANGEA_ACS_REF	10	0	5A7
PANGEA_SD_REF	10	0	6B2
VREF_VDDQ	10	3.3	

XWS	SHORT	OPEN
XW1	X	
XW2	X	
XW3	X	
XW4	X	
XW5	X	
XW6	X	
XW7	X	
XW8	X	
XW9	X	
XW10	X	
XW11	X	
XW12	X	
XW13	X	
XW14	X	

I/O CONNECTORS		
USB	SHEET 17	J7, J10
ETHERNET	SHEET 18	J3
FIREWIRE	SHEET 19	J5
RGB	SHEET 24	J12
HEADPHONE	SHEET 27	J13
DC IN	SHEET 32	J20

### Holes and Slots AND EMC INFO

#### CONSTRAINTS -- POWER

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	APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
		D	051-6130-C	ACI: C ECS:1.0
SCALE		SHT	40 OF 53	
NONE				

8 7 6 5 4 3 2 1



Table with 7 columns: SIG\_NAME, PULSE\_PARAM, MAX\_VIA\_COUNT, NET\_SCHD, DELAY\_RULE, STUB\_LENGTH/ ECL, NET\_SPACING\_TYPE. Rows include CPU\_DATA<0> through CPU\_DATA<63>

Table with 7 columns: SIG\_NAME, PULSE\_PARAM, MAX\_VIA\_COUNT, NET\_SCHD, DELAY\_RULE, STUB\_LENGTH/ ECL, NET\_SPACING\_TYPE. Rows include KEY PANGEA TIMING, CPU\_BR\*, KEY PANGEA TIMING, TBST\*, AACK\*, KEY PANGEA TIMING, ARTRY\*, DBNO\*, KEY PANGEA TIMING, QACK\*, PAN QACK\*, TA\*, TEA\*, TT<0>, TT<1>, TT<2>, TT<3>, TT<4>, TSIZ<0>, TSIZ<1>, TSIZ<2>, CPU\_ADDR<0>, CPU\_ADDR<1>, CPU\_ADDR<2>, CPU\_ADDR<3>, CPU\_ADDR<4>, CPU\_ADDR<5>, CPU\_ADDR<6>, CPU\_ADDR<7>, CPU\_ADDR<8>, CPU\_ADDR<9>, CPU\_ADDR<10>, CPU\_ADDR<11>, CPU\_ADDR<12>, CPU\_ADDR<13>, CPU\_ADDR<14>, CPU\_ADDR<15>, CPU\_ADDR<16>, CPU\_ADDR<17>, CPU\_ADDR<18>, CPU\_ADDR<19>, CPU\_ADDR<20>, CPU\_ADDR<21>, CPU\_ADDR<22>, CPU\_ADDR<23>, CPU\_ADDR<24>, CPU\_ADDR<25>, CPU\_ADDR<26>, CPU\_ADDR<27>, CPU\_ADDR<28>, CPU\_ADDR<29>, CPU\_ADDR<30>, CPU\_ADDR<31>, CPU\_ADDR<32>, CPU\_ADDR<33>, CPU\_ADDR<34>, CPU\_ADDR<35>, CPU\_ADDR<36>, CPU\_ADDR<37>, CPU\_ADDR<38>, CPU\_ADDR<39>, CPU\_ADDR<40>, CPU\_ADDR<41>, CPU\_ADDR<42>, CPU\_ADDR<43>, CPU\_ADDR<44>, CPU\_ADDR<45>, CPU\_ADDR<46>, CPU\_ADDR<47>, CPU\_ADDR<48>, CPU\_ADDR<49>, CPU\_ADDR<50>, CPU\_ADDR<51>, CPU\_ADDR<52>, CPU\_ADDR<53>, CPU\_ADDR<54>, CPU\_ADDR<55>, CPU\_ADDR<56>, CPU\_ADDR<57>, CPU\_ADDR<58>, CPU\_ADDR<59>, CPU\_ADDR<60>, CPU\_ADDR<61>, CPU\_ADDR<62>, CPU\_ADDR<63>, GBL\*, CPU\_DBG\*, CPU\_BG\*, WT\*, CI\*

CONSTRAINTS -- CPU BUS

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CONSTRAINTS -- CPU BUS

Table with 3 columns: Apple logo/APPLE COMPUTER INC., Drawing Number (D 051-6130-C), Rev. (ACI: C, ECS:1.0). Includes scale information (SCALE NONE, SHEET 41 OF 53).







8 7 6 5 4 3 2 1

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH/ ECL	NET_SPACING_TYPE	NET_SCHED
T_M_BA0	100	5	::1100:2400	200 TRUE	5 MIL SPACING	RP2.1 J1.106
T_M_BA1	100	5	::1100:2400	200 TRUE	5 MIL SPACING	RP2.4 J1.110
T_SBRAS*	100	5		TRUE	5 MIL SPACING	RP15.4 J1.65
T_SDCAS*	100	5	::1100:2400	200 TRUE	5 MIL SPACING	RP15.3 J1.66
T_MEMWE*	100	5	::1100:2400	200 TRUE	5 MIL SPACING	R202.1 J1.67

6A6 7A4 7B2 7C2 7C4 8B4  
 6A6 7A2 7A4 7C2 7C4 8B4  
 6A6 7A2 7A4 7C2 7C4 8C5  
 6A6 7A2 7A4 7C2 7C4 8C4  
 6A6 7A2 7A4 7C2 7C4 8C5

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	ASSIGN_TOPOLOGY	NET_SCHED	DELAY_RULE	STUB_LENGTH/ ECL	NET_SPACING_TYPE
DOM0*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM1*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM2*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM3*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM4*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM5*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM6*	100	4			::3000:4000	200 TRUE	5 MIL SPACING
DOM7*	100	4			::3000:4000	200 TRUE	5 MIL SPACING

6C2 7C4  
 8C5  
 6C2 7C4  
 8C5  
 6C2 7C2  
 8B5  
 6C2 7A4  
 8C4  
 6C2 7A4  
 8B4  
 6C2 7A2  
 8B4  
 6C2 7A2  
 8B4

SIG_NAME	PULSE_PARAM	MIN_LINE_WIDTH MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH/ ECL	NET_SPACING_TYPE
PANGEA_CPU_CLK	100	2 5		::300:500	250	100 TRUE	
CPU_CLK	100	6 5		::12700:5500	250	200 TRUE	
CPUFROUT	100	2 5		::100:600		100 TRUE	10 MIL SPACING
TCPUFROUT	100	2 5		::475:700		100 TRUE	10 MIL SPACING
CPUF7	100	2 5		::900:1000		100 TRUE	10 MIL SPACING
CPUF6	100	2 5		::1800:2000		100 TRUE	10 MIL SPACING
CPUF5	100	2 5		::1800:2000		100 TRUE	10 MIL SPACING
CPUF4	100	2 5		::950:1100		100 TRUE	10 MIL SPACING
CPUF3	100	2 5		::1800:2000		100 TRUE	10 MIL SPACING
CPUF2	100	2 5		::1800:2000		100 TRUE	10 MIL SPACING
CPUF1	100	2 5		::900:1000		100 TRUE	10 MIL SPACING
CPUFBIN	100	6 5		::475:1200		100 TRUE	10 MIL SPACING
AGPFB0	66	2 5		::950:1000		100 TRUE	10 MIL SPACING
AGPFB1	66	2 5		::475:700		100 TRUE	10 MIL SPACING
AGPFB2	66	2 5		::950:1100		100 TRUE	10 MIL SPACING
AGPFB3	66	2 5		::475:700		100 TRUE	10 MIL SPACING
FROUT_CLK	100	2 10					10 MIL SPACING
28507_CLK1	100	2 10					10 MIL SPACING
28507_CLK2	100	2 10					10 MIL SPACING
28507_CLK3	100	2 10					10 MIL SPACING
28507_CLK4	100	2 10					10 MIL SPACING
28507_CLK5	100	2 10					10 MIL SPACING
MK1708_SSOUT		2 5					10 MIL SPACING
ATI_SSIN		2 5					10 MIL SPACING
TBENDIVCLK	100	2 5					10 MIL SPACING
TBEN	33	2 4					10 MIL SPACING
574_CLK	100	2 10					10 MIL SPACING

5A7  
 6C6  
 3A4  
 3A8  
 5B1  
 6C5  
 5B2  
 5B2  
 5B3  
 5B3  
 5B3  
 5B2  
 5B2  
 5B2  
 5B8  
 9B3  
 9B4  
 9B4  
 9C4  
 5A8  
 6D8  
 6C7  
 6C7  
 6D7  
 6D7  
 6D7  
 22A3  
 22A2 22B3  
 6B8 6C6  
 3A6 6B6 14B8  
 6C6 7B8

CS0*	100	5		U1.M3 RP8.7	::600:1100	200 TRUE	5 MIL SPACING
CS1*	100	5		U1.M5 RP8.8	::600:1100	200 TRUE	5 MIL SPACING
CS2*	100	5		U1.R3 RP8.5	::600:1100	200 TRUE	5 MIL SPACING
CS3*	100	5		U1.P7 RP8.6	::600:1100	200 TRUE	5 MIL SPACING
TICS0*	100	4			::300:1400	200 TRUE	5 MIL SPACING
TICS1*	100	4			::300:1400	200 TRUE	5 MIL SPACING
RAM_CKE0	100	4			::300:1400	200 TRUE	5 MIL SPACING
RAM_CKE1	100	4			::300:1400	200 TRUE	5 MIL SPACING
M_BA0	100	4			::400:1400	200 TRUE	5 MIL SPACING
M_BA1	100	4			::400:1400	200 TRUE	5 MIL SPACING
SBRAS*	100	4			::400:1000	200 TRUE	5 MIL SPACING
SDCAS*	100	4			::400:1000	200 TRUE	5 MIL SPACING
MEMWE*	100	4			::400:1000	200 TRUE	5 MIL SPACING

6A4 6C2  
 6A4 6C2  
 6A4 6C2  
 6A4 6C2  
 6A5 7A2  
 7A4 7C2  
 6A5  
 6C2 7B8  
 6C2 7B8  
 6A5 6C2  
 6A5 6C2  
 6A5 6C2  
 6A5 6C2  
 6A5 6C2

VCORE_CSH		U19.1:R354.1::590	VCORE_CS
VCORE_CSL		U19.2:R354.2::590	VCORE_CS
2_5V_CSH		U20.1:R355.1::590	2_5V_CS
2_5V_CSL		U20.2:R355.2::590	2_5V_CS
VCORE_DH		U19.18:Q53.4::780	
VCORE_DL		U19.15:Q42.4::780	
VCORE_LX		U19.19:L59.1::590	
2_5V_DH		U20.18:Q41.4::780	
2_5V_DL		U20.15:Q10.4::780	
2_5V_LX		U20.19:L38.1::590	
+PBUS		C442.1:Q53.5::390	19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS		C444.1:Q53.6::390	19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS		C446.1:Q53.7::390	19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS		C447.1:Q53.8::390	19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS		C443.1:Q41.5::390	19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS		C313.1:Q41.6::390	19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
VCORE_BST		U19.17:D31.3::780	
2_5V_BST		U20.17:D30.3::780	

CONSTRAINTS -- MEMORY PAGE (2)

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SCALE	SHT	OF	
NONE	43	53	

CONSTRAINTS -- MEMORY PAGE 2

8 7 6 5 4 3 2 1



AGP RELATED DOO-DAHS

CONSTRAINTS -- AGP, FIREWIRE

MIN\_LINE\_WIDTH

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	NET_SCHED	NET_SPACING_TYPE	DELAY_RULE	DELAY_RULE (THE SEQUEL!)
AGP_CLK	66 / 12	250 / 200	R213.1 U5.AG16	10 MIL SPACING	::3800:3900	5
PANGEA_AGP_CLK	66 / 3	250 / 200		10 MIL SPACING	::0225:0275	5
AGP_FB_IN	66 / 3	/ / 200		10 MIL SPACING	::1325:1350	5
AGP_FB_OUT	66 / 3	/ / 200		10 MIL SPACING	::0320:0335	5
AGPAD<31>	66 / 8	/ / 200	U1.B11 U5.AK14	5 MIL SPACING	::3750:3980	9C5
AGPAD<30>	66 / 8	/ / 200	U1.F11 U5.AG14	5 MIL SPACING	::3750:3980	9B2
AGPAD<29>	66 / 8	/ / 200	U1.F12 U5.AG15	5 MIL SPACING	::3750:3980	9B2
AGPAD<28>	66 / 8	/ / 200	U1.C9 U5.AH14	5 MIL SPACING	::3750:3980	9C2
AGPAD<27>	66 / 8	/ / 200	U1.A9 U5.AJ15	5 MIL SPACING	::3750:3980	9C2
AGPAD<26>	66 / 8	/ / 200	U1.F11 U5.AH15	5 MIL SPACING	::3750:3980	9C2
AGPAD<25>	66 / 8	/ / 200	U1.A8 U5.AK16	5 MIL SPACING	::3750:3980	9C2
AGPAD<24>	66 / 8	/ / 200	U1.G11 U5.AK17	5 MIL SPACING	::3750:3980	9C2
AGPAD<23>	66 / 8	/ / 200	U1.B10 U5.AJ16	5 MIL SPACING	::3750:3980	9C2
AGPAD<22>	66 / 8	/ / 200	U1.A10 U5.AH18	5 MIL SPACING	::3750:3980	9C2
AGPAD<21>	66 / 8	/ / 200	U1.B9 U5.AK19	5 MIL SPACING	::3750:3980	9C2
AGPAD<20>	66 / 8	/ / 200	U1.B8 U5.AJ18	5 MIL SPACING	::3750:3980	9C2
AGPAD<19>	66 / 8	/ / 200	U1.F12 U5.AG18	5 MIL SPACING	::3750:3980	9C2
AGPAD<18>	66 / 8	/ / 200	U1.C8 U5.AJ19	5 MIL SPACING	::3750:3980	9C2
AGPAD<17>	66 / 8	/ / 200	U1.C11 U5.AH19	5 MIL SPACING	::3750:3980	9C2
AGPAD<16>	66 / 8	/ / 200	U1.A7 U5.AG19	5 MIL SPACING	::3750:3980	9C2
AGPAD<15>	66 / 8	/ / 200	U1.E14 U5.AJ22	5 MIL SPACING	::3020:3270	9C2
AGPAD<14>	66 / 8	/ / 200	U1.F14 U5.AH22	5 MIL SPACING	::3020:3270	9C2
AGPAD<13>	66 / 8	/ / 200	U1.C12 U5.AK22	5 MIL SPACING	::3020:3270	9C2
AGPAD<12>	66 / 8	/ / 200	U1.F15 U5.AG23	5 MIL SPACING	::3020:3270	9C2
AGPAD<11>	66 / 8	/ / 200	U1.C14 U5.AH23	5 MIL SPACING	::3020:3270	9C2
AGPAD<10>	66 / 8	/ / 200	U1.F13 U5.AK25	5 MIL SPACING	::3020:3270	9C2
AGPAD<9>	66 / 8	/ / 200	U1.A12 U5.AK23	5 MIL SPACING	::3020:3270	9C2
AGPAD<8>	66 / 8	/ / 200	U1.B12 U5.AH24	5 MIL SPACING	::3020:3270	9C2
AGPAD<7>	66 / 8	/ / 200	U1.B13 U5.AK24	5 MIL SPACING	::3020:3270	9C2
AGPAD<6>	66 / 8	/ / 200	U1.C15 U5.AK24	5 MIL SPACING	::3020:3270	9C2
AGPAD<5>	66 / 8	/ / 200	U1.B14 U5.AH26	5 MIL SPACING	::3020:3270	9C2
AGPAD<4>	66 / 8	/ / 200	U1.F16 U5.AG24	5 MIL SPACING	::3020:3270	9C2
AGPAD<3>	66 / 8	/ / 200	U1.A11 U5.AJ27	5 MIL SPACING	::3020:3270	9C2
AGPAD<2>	66 / 8	/ / 200	U1.A13 U5.AK26	5 MIL SPACING	::3020:3270	9D1
AGPAD<1>	66 / 8	/ / 200	U1.A14 U5.AH27	5 MIL SPACING	::3020:3270	9D1
AGPAD<0>	66 / 8	/ / 200	U1.B15 U5.AJ28	5 MIL SPACING	::3020:3270	9D1
AGPADSTB<1>	66 / 8	/ / 200	R779.2 U5.AG17	10 MIL SPACING	::0500:0550	9A1
AGPADSTB<0>	66 / 8	/ / 200	R778.2 U5.AH25	10 MIL SPACING	::0600:0650	9A1
AGPSBA<7>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<6>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<5>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<4>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<3>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<2>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<1>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBA<0>	66 / 8	/ / 200		5 MIL SPACING		9B1
AGPSBSTB	66 / 5	/ / 200		10 MIL SPACING	::4385:4490	9B1
AGPCBE<3>	66 / 8	/ / 200	U1.E9 U5.AK18	5 MIL SPACING	::3750:3980	9B1
AGPCBE<2>	66 / 8	/ / 200	U1.F9 U5.AK21	5 MIL SPACING	::3750:3980	9B1
AGPCBE<1>	66 / 8	/ / 200	U1.A6 U5.AG22	5 MIL SPACING	::3020:3270	9B1
AGPCBE<0>	66 / 8	/ / 200	U1.F10 U5.AJ24	5 MIL SPACING	::3020:3270	9B1
AGPST<2>	66 / 8	/ / 200	U1.A15 U5.AK12	5 MIL SPACING	::3500:4500	9A1
AGPST<1>	66 / 8	/ / 200	U1.G16 U5.AJ12	5 MIL SPACING	::3500:4500	9A1
AGPST<0>	66 / 8	/ / 200	U1.B15 U5.AG12	5 MIL SPACING	::3500:4500	9B1
AGPPAR	66 / 8	/ / 200	U1.A16 U5.AJ21	5 MIL SPACING	::3500:4500	9B1
AGPFRAME*	66 / 8	/ / 200	U1.B17 U5.AH20	5 MIL SPACING	::3500:4500	9B1
AGPTRDY*	66 / 8	/ / 200	U1.B16 U5.AK20	5 MIL SPACING	::3500:4500	9B1
AGPIRDY*	66 / 8	/ / 200	U1.C17 U5.AG20	5 MIL SPACING	::3500:4500	9B1
PCISTOP*	66 / 8	/ / 200	U1.E17 U5.AH21	5 MIL SPACING	::3500:4500	9B1
AGPDEVSEL*	66 / 8	/ / 200	U1.B7 U5.AG21	5 MIL SPACING	::3500:4500	9B1
AGPPIFE*	66 / 8	/ / 200	U1.B5 U5.AG13	5 MIL SPACING	::3500:4500	9A1
AGPPEB*	66 / 8	/ / 200	U1.B6 U5.AH12	5 MIL SPACING	::3500:4500	9A1

FIREWIRE RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	
FW_XI	24.576 / 2	250	200	10 MIL SPACING	19B7
FW_XO	24.576 / 2	250	200	10 MIL SPACING	19B7
FW_LINK_SCLK	49.152 / 4	250	200	10 MIL SPACING	10B3 19A8
PHYSCLK	49.152 / 4	250	200	10 MIL SPACING	19A7 19B7
FW_LINK_D<7>	49.152 / 4	200			10B3 19A7
FW_LINK_D<6>	49.152 / 4	200			10B3 19A7
FW_LINK_D<5>	49.152 / 4	200			10B3 19A7
FW_LINK_D<4>	49.152 / 4	200			10B3 19A7
FW_LINK_D<3>	49.152 / 4	200			10C3 19A7
FW_LINK_D<2>	49.152 / 4	200			10C3 19A8
FW_LINK_D<1>	49.152 / 4	200			10C3 19A8
FW_LINK_D<0>	49.152 / 4	200			10C3 19A8
FW_LINK_CNTL1	49.152 / 4	200			10B3 19A8
FW_LINK_CNTL0	49.152 / 4	220			10B3 19A8
FW_LINK_LREQ	49.152 / 4	200			10B3 19B8
PHYD7	49.152 / 4	200			19A7 19B7
PHYD6	49.152 / 4	200			19A7 19B7
PHYD5	49.152 / 4	200			19A7 19B7
PHYD4	49.152 / 4	200			19A7 19B7
PHYD3	49.152 / 4	200			19A7 19B7
PHYD2	49.152 / 4	200			19A7 19B7
PHYD1	49.152 / 4	200			19A7 19B7
PHYD0	49.152 / 4	200			19A7 19B7
PHYCNLL1	49.152 / 4	200		5 MIL SPACING	20 19A7 19B7
PHYCNLL0	49.152 / 4	200		5 MIL SPACING	20 19A7 19B7
PHYLREQ	49.152 / 4	200	200	5 MIL SPACING	19B7

FIREWIRE DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PHYTPA0T	400 / 2	250		TRUE		PHYTPA0
PHYTPA0C	400 / 2	250		TRUE		PHYTPA0
PHYTPB0T	400 / 2	250		TRUE		PHYTPB0
PHYTPB0C	400 / 2	250		TRUE		PHYTPB0
PHYTPA0T_FL	400 / 2	250		TRUE		PHYTPA0_FL
PHYTPA0C_FL	400 / 2	250		TRUE		PHYTPA0_FL
PHYTPB0T_FL	400 / 2	250		TRUE		PHYTPB0_FL
PHYTPB0C_FL	400 / 2	250		TRUE		PHYTPB0_FL

CONSTRAINTS -- AGP, FIREWIRE

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	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	44	OF 53
NONE			



SIG_NAME	PULSE_PARAM	MAX_EXPOSED_LENGTH	ECL	DIFFERENTIAL_PAIR	MAX_VIA_COUNT	STUB_LENGTH	DELAY_RULE	NET_SPACING_TYPE	NET_SCHED
UIDE_DA<0>	66				6		:::5170:5920	5 MIL SPACING	12B6 12C5
UIDE_DA<1>	66				6		:::5170:5920	5 MIL SPACING	12B6 12C5
UIDE_DA<2>	66				6		:::5170:6100	5 MIL SPACING	12A6 12C5
UIDE_IORDY	66				6		:::5170:5920	5 MIL SPACING	12A6 16B8
UIDE_CS0 L	66				6		:::5170:5920	5 MIL SPACING	12A6 12C5
UIDE_CS1 L	66				6		:::5170:5920	5 MIL SPACING	12A6 12C5
UIDE_RESET L	66				6		:::1600:2000	5 MIL SPACING	12A6 12C5
UIDE_DIOW L	66				6		:::5920	10 MIL SPACING	12A6 12C5
UIDE_DIOR L	66				6		:::5920	10 MIL SPACING	12A6 12C5
UIDE_DMAACK L	66				6		:::5170:5920	5 MIL SPACING	12A6 12B5
UIDE_DMAREQ	66				6		:::5170:5920	5 MIL SPACING	12A6 12D5
UIDE_IRO	66				6		:::5170:5920	5 MIL SPACING	12A6 12D5
UIDE_D<0>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<1>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<2>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<3>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<4>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<5>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<6>	66				6		:::5170:5920	5 MIL SPACING	12B5 12B6
UIDE_D<7>	66				6		U1.J30:RP19.4:5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<8>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<9>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<10>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<11>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<12>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<13>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
UIDE_D<14>	66				6		:::5130:5920	5 MIL SPACING	12A5 12B6
UIDE_D<15>	66				6		:::5170:5920	5 MIL SPACING	12A5 12B6
T UIDE_RESET L	66				6	100	R300.2:710.1:3508:3858	5 MIL SPACING	12C4 16B6 16C7
MII_TX_CLK F	2.5,25		TRUE		4	100	:::300:500	10 MIL SPACING	18D6
MII_RX_CLK F	2.5,25		TRUE		4	100	:::300:500	10 MIL SPACING	18C6
MII_TX_CLK	2.5,25	250	TRUE		4	100	:::6000	10 MIL SPACING	10C7 18D7
MII_RX_CLK	2.5,25	250	TRUE		4	100	:::6000	10 MIL SPACING	10C7 18C7
MII_TPTDP	10,100				2	100		10 MIL SPACING	18D3
MII_TPTDN	10,100				2	100		10 MIL SPACING	18D3
MII_TPRDP	10,100				2	100		10 MIL SPACING	18C3
MII_TPRDN	10,100				2	100		10 MIL SPACING	18C3
RJ45_TXP	10,100			RJ45_TX	2	100		2KV_ISO===100 MIL SPACING	18D1
RJ45_TXN	10,100			RJ45_TX	2	100			18D1
RJ45_RXP	10,100			RJ45_RX	2	100			18D1
RJ45_RXN	10,100			RJ45_RX	2	100			18C1
PAN_XIB	18.432		TRUE		3		:::1000	10 MIL SPACING	13B7
PAN_XO	18.432		TRUE		2	100	:::1000	10 MIL SPACING	13B7
PAN_XT	18.432		TRUE		2		:::500	10 MIL SPACING	13B7
PMU_10MHZ_XOUT	10		TRUE		2	100	:::1000	10 MIL SPACING	21B5
PMU_10MHZ_XIN	10		TRUE		2	100	:::1000	10 MIL SPACING	21B5
PMU_32KHZ_XOUT	0.032768		TRUE		2	100	:::1000	10 MIL SPACING	21B4
PMU_32KHZ_XIN	0.032768		TRUE		2	100	:::1000	10 MIL SPACING	21B4
T UIDE_DIOW L	66				6		:::5170:5920	10 MIL SPACING	12C4 16B6
T UIDE_DIOR L	66				6		:::5170:5920	10 MIL SPACING	12C4 16B6

2KV\_ISO === 100MIL SPACING  
 MANUALLY TAKE CARE OF 2KV FOR ETHERNET

SIG_NAME	ECL	DIFFERENTIAL_PAIR	NET_SPACING_TYPE
USB_DCM	TRUE	USB_DC	13C5 17D8
USB_DCP	TRUE	USB_DC	13C5 17D8
USB_DAM	TRUE	USB_DA	13C5 17B8
USB_DAP	TRUE	USB_DA	13C5 17B8
USB_DCM_R	TRUE	USB_DC_R	17D5
USB_DCP_R	TRUE	USB_DC_R	17D5
USB_DAM_R	TRUE	USB_DA_R	17B5
USB_DAP_R	TRUE	USB_DA_R	17B5
USB_DCM_OUT	TRUE	USB_DC_OUT	17D2
USB_DCP_OUT	TRUE	USB_DC_OUT	17D2
USB_DAM_OUT	TRUE	USB_DA_OUT	17B1
USB_DAP_OUT	TRUE	USB_DA_OUT	17B1

SIG_NAME	NET_SCHED
IODATA<0>	U1.P34 R323.2 R324.1 U3.25 J11.30
IODATA<1>	U1.R32 R325.2 R326.1 U3.26 J11.31
IODATA<2>	U1.T29 R327.2 R328.1 U3.27 J11.32
IODATA<3>	U1.T28 R329.2 R330.1 U3.28 J11.2
IODATA<4>	U1.R33 R334.2 R335.1 U3.32 J11.3
IODATA<5>	U1.R34 R336.2 R337.1 U3.33 J11.4
IODATA<6>	U1.U29 R338.2 R339.1 U3.34 J11.5
IODATA<7>	U1.T33 U3.35 J11.6
IOADDR<0>	U1.N28 U3.21 J11.29
IOADDR<1>	U1.J34 U3.20 J11.28
IOADDR<2>	U1.M30 U3.19 J11.27
IOADDR<3>	U1.L32 U3.18 J11.26
IOADDR<4>	U1.K34 U3.17 J11.25
IOADDR<5>	U1.L33 U3.16 J11.24
IOADDR<6>	U1.N29 U3.15 J11.23
IOADDR<7>	U1.M32 U3.14 J11.22
IOADDR<8>	U1.L34 U3.8 J11.12
IOADDR<9>	U1.P28 U3.7 J11.11
IOADDR<10>	U1.M33 U3.36 J11.8
IOADDR<11>	U1.P29 U3.6 J11.10
IOADDR<12>	U1.M34 U3.5 J11.21
IOADDR<13>	U1.P30 U3.4 J11.13
IOADDR<14>	U1.N33 U3.3 J11.14
IOADDR<15>	U1.R28 U3.2 J11.20
IOADDR<16>	U1.P32 U3.1 J11.19
IOADDR<17>	U1.N34 U3.40 J11.46
IOADDR<18>	U1.R29 U3.13 J11.47
IOADDR<19>	U1.P33 U3.37 J11.48
IOADDR<20>	U1.R30 U3.38 J11.49

SIG_NAME	NET_SCHED
_CB_CE2*	U1.W28 RP43.4 J11.42
_CB_CE1*	U1.W29 RP43.3 J11.7
_CB_IORD*	U1.W33 RP43.1 J11.44
_CB_IOWR*	U1.W34 RP43.2 J11.45
_CB_IRQ*	U1.A32 R370.1 J11.16
_CB_REG*	U1.B31 R368.1 J11.61
_CB_RESET	U1.AE33 R306.2 J11.58
_CB_WAIT*	U1.Y34 R369.1 J11.59
_CSWE*	U1.V29 RP44.2 J11.15
_CSOE*	U1.Y33 RP44.1 J11.9

CONSTRAINTS -- MISCELLANEOUS

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	SCALE NONE	SHT 45 OF 53	





### NET ATTRIBUTES

NET	VOLTAGE	MIN. LINE WIDTH	MIN. LINE WIDTH
F ACOUT	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
ACOM IN RL	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
A COM IN RC	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
A COM IN	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
SPKR STAR GND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	27B3 27B4 27C3 27C4 27C6 28B3 28B8 28C4 28C8 29A5 29C2
MB IN STAR GND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	39B8 46D7
LINE STAR GND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
LINE OUT GND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
SPKR STAR GND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	46D7 27B3 27B4 27C3 27C4 27C6 28B3
DIG STAR GND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	28B8 28C4 28C8 29A5 29C2 39B8
SCREAMER AGND	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
LINE OUT COM STAR	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
ACOUT RL	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
ACOUT LCL	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
ACOUT	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
SCREAMER RET	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
SPEAKER RET	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
SCREAMER DVDD RET	VOLTAGE=0V	MIN. LINE WIDTH=10MIL	
+AVCC SCREAMER	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	
+AVCC F SCREAMER	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	
+DVDD F SCREAMER	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	
+6V AUDIO	VOLTAGE=6V	MIN. LINE WIDTH=10MIL	17C7 17D7 27C8 29C3 29D5 34D3
+5V MAIN	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	46C7 16C2 17B7 19D4 24D2 28C4
FILT MIC PWR	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	34C2 35D8 36B3 37B4 37D4 38B3
MIC PWR	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	38B8 38C5 40D6
+24V EXT	VOLTAGE=24V	MIN. LINE WIDTH=50MIL	
ADAPTER +24V	VOLTAGE=24V	MIN. LINE WIDTH=50MIL	
+24V EXT GND	VOLTAGE=0V	MIN. LINE WIDTH=50MIL	
+5V VGADDCPWR SLEEP F	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	25D5
+5V VGA_FUSE	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	25D6 40C6
+3V VGA_MAIN	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	14D3 14D4 22A4 22C5 22D8 23B8 23C1
+AUD3.3V	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	27D6 23C8 24C2 25C2 25D2 36C4 46B7
+5V MAIN_A	VOLTAGE=5V	MIN. LINE WIDTH=20MIL	27D8 28B8 28C6
+6V AUDIO	VOLTAGE=6V	MIN. LINE WIDTH=20MIL	17C7 17D7 27C8 29C3 29D5 34D3 46C7
+AUD5V	VOLTAGE=5V	MIN. LINE WIDTH=10MIL	27C6 29B3 29C3 29D5
FIL2_AUD3.3V	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	27D4
FIL2_DIG3.3V	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	27B6 27C2 27C5
+AVDD_CPU_SLEEP	VOLTAGE=1.4V	MIN. LINE WIDTH=10MIL	3B3
+AVDD_CPU_SLEEP	VOLTAGE=1.4V	MIN. LINE WIDTH=10MIL	3B2
+A2VDD_CPU_SLEEP	VOLTAGE=1.4V	MIN. LINE WIDTH=10MIL	3A2
+AVDD_CPU_F_SLEEP	VOLTAGE=1.4V	MIN. LINE WIDTH=10MIL	3B1 3D6
+A2VDD_CPU_F_SLEEP	VOLTAGE=1.4V	MIN. LINE WIDTH=10MIL	3A1 3D6
+VCORE_SLEEP	VOLTAGE=1.4V	MIN. LINE WIDTH=10MIL	3D4 38B3 38C1 40C6
+VIO_CPU_SLEEP	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	3C4 3D5 4B4 4D5 5C2 13D1 14A6 14A7 14C6 14D6 14D8 15B1
+3V_MAIN	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	15D2 35C3 36B4
+2.5V_MAIN	VOLTAGE=2.5V	MIN. LINE WIDTH=10MIL	
+3V_SLEEP	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	4C6 6B5 6C5 9D4 13B3 15A5 15B5 15B7 15C5 15C7 20C8 20D6
+3V_CLKGEN_AVDD_SLEEP	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	6B4 6D8 22B5 22C1 25A6 25B5 25D4 27C6 35D2 40D4
+3V_CLKGEN_SLEEP	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	6C4 6C8 6D4 6D8
+1.8V_EVDD_MAIN	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	23B7 23D6
+1.8V_AVDD_MAIN	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	23D6
+1.8V_A2VDDO_MAIN	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	23D6
ATI_CORE_MAIN	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	22A5 22C8 23D7 37C8
+1.8V_LVDDR_MAIN	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	23A5
+1.8V_MPVDD_MAIN	VOLTAGE=1.8V	MIN. LINE WIDTH=10MIL	23A5
+3V_VDDP_MAIN	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	23C6
+3V_VGA_MAIN	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	14D3 14D4 22A4 22C5 22D8 23B8 23C1 23C8 24C2 25C2 25D2 36C4
+3V_VDR3_MAIN	VOLTAGE=3V	MIN. LINE WIDTH=10MIL	23C3 46C7
+2.5V_ATI_VDDR_MAIN	VOLTAGE=2.5V	MIN. LINE WIDTH=10MIL	

### MLB STACKUP

LAYER	THICKNESS (MILS)	TRACE WIDTH (MILS)
L1 SIGNAL(TOP)	1.560	5.0
L1-L2	3.740	
L2 GROUND1(GND)	1.170	---
L2-L3	6.500	
L3 SIGNAL(IN1)	1.170	5.0
L3-L4	6.300	
L4 SIGNAL(IN2)	1.170	5.0
L4-L5	6.500	
L5 POWER(VCC)	1.170	---
L5-L6	6.500	
L6 SIGNAL(IN3)	1.170	5.0
L6-L7	6.500	
L7 GROUND2(GND)	1.170	---
L7-L8	3.540	
L8 SIGNAL(BOTTOM)	1.560	5.0
TOTAL		---

SIGNAL TRACE IMPEDANCE OF ? OHMS

CPU ROUTES ARE ? OHMS?  
AGP ROUTES ARE 5 MILLS OHMS?  
RAM ROUTES ARE ? OHMS?

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	D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	OF	
NONE	46	53	



# REVISION HISTORY (1)

## SAHARA QUAL PCB(REV:0.0)

- 1) CHANGE CPU FROM SIDEWINDER TO SAHARA
- 2) CHANGE VGA FROM ATI-M3 TO ATI-M6
- 3) CHANGE AUDIO FROM TUMBLER TO SNAPPER

## PROTO (REV:0.1)

- 1) ACCORDING RADAR#2773492 - UPDATES TO THE P72 SCHEMATICS
- 2) ACCORDING RADAR#2774277 - P72 M6 SCHEMATICS FIXES FOR PROTO2
  - A) UNSTUFF R902,R903,R905
  - B) CHANGE R906 TO 100K AND PULL UP TO VDDC
  - C) STUFF R914,R916 FOR M6 16MB VERSION
  - D) ADD R1116(0OHM) BETWEEN C954 AND C955
  - E) UNSTUFF R395 AND Q56
- 3) ACCORDING RADAR#2775061 - CHANGE P72 TO HARDWARE CHARGING
- 4) ACCORDING RADAR#2777820 - NEW AVC CABLE CONNECTIONS
  - A) ADD U210(74LVC1G125),F100,Q210,Q211,C1210,R957,R958,R959 FOR NEW AVC CONNCTOR.
- 5) ACCORDING RADAR#2780508 - CHANGE TO THE AUDIO POWER DOWN CIRCUIT
  - A) REMOVE R462,R599,R600,R601,R602,R603,C638,Q86,Q87
  - B) CONNECT U300/PIN8 TO DGND
  - C) CONNECT U300/PIN6 TO IO\_RESET\_L
  - D) CHANGE U4/PIN AA33 NAME FROM AUDIO\_HW\_RESET\_L TO PAN\_GPIO1
  - E) ADD 10K PULLUP FOR PAN\_GPIO1
- 6) ACCORDING RADAR#2779003 - ADD A BOM OPTION TO PREPARE FOR SAHARA DD2.0
- 7) ACCORDING RADAR#2780490 - NEW FAN SPEED CONTROL CIRCUIT
  - A) ADD U1200(ADM1030) AND Q1000 FOR NEW FAN CONTROL CIRCUIT
- 8) ACCORDING RADAR#2782007 - DASH MODEM PERFORMANCE IMPACTED BY VCORE SWITCHER
  - A) DISCONNECT ZH2 FROM GND
- 9) ACCORDING RADAR#2782669 - ADD OPTIONAL CONTROL FOR VCORE VLOTAGE
  - A) CHANGE U4/PIN AA33 NET NAME FROM PAN\_GPIO1 TO VCORE\_CTL
  - B) REMOVE THE NET NAME "CPU\_VCORE\_HI\_OC" FROM U1/PIN16
  - C) ADD R1552 BETWEEN U1/PIN16 AND THE NET "CPU\_VCORE\_HI\_OC"
  - D) ADD R1553(NOSTUFF) BETWEEN U1/PIN16 AND NET "VCORE\_CTL"
- 10) ACCORDING RADAR#2782721 - ADDITIONAL M6 CHANGES FOR OK TO FAB
  - A) ADD R954 FOR VGA\_CORE\_HI\_OC SIGNAL PULLUP
  - B) CHANGE Q1504/PIN2 CONNECTION FROM PS\_GND TO MAX1715\_GND
  - C) CHANGE THE NET NAME FROM VGA\_VCORE\_HI\_OC TO VGA\_VCORE\_HI
- 11) ACCORDING RADAR#2782641 - EXTERNAL VIDEO SCHEMATICS CHANGE
  - A) REMOVE R334,R393,R395,Q56,R392,C905
  - B) CHANGE R935,R936,R937 CONNECTION FROM U200/PIN AF22,AF23,AF24 TO U200/PIN AF14,AF15,AF16
  - C) REMOVE COMPVSS SIGNAL AND L36
- 12) ACCORDING RADAR#2784789 - PROTO BUILD BOM CHANGES
  - A) STUFF R803(113S1102),R805(113S1473,R820(113S1000),R1110,R1111,C1109,C1110,Q809,Q810
  - B) UNSTUFF R1115,R1112,Q211
  - C) CHANGE R539 TO 3.16K,1% (110S3163)

## EVT (REV:0.2)

- 1) ACCORDING RADAR#2798007 - ADD AUDIO/CONTROL CONNECTOR
  - A) USE J900(NEW FOXCONN AUDIO JACK) TO REPLACE J13
  - B) ADD CONTROL CIRCUITS FOR I-POD
- 2) ACCORDING RADAR#2794270 - SCHEMATICS CHANGE-NEW BLUETOOTH CONN.
  - A) USE 4PIN J100 CONN TO REPLACE J100(6PIN)
  - B) CHANGE THE USB-D CIRCUITS FOR BLUETOOTH MODULE.
- 3) ACCORDING RADAR#2805677 - CHANGES FROM EVT LAYOUT REVIEW
  - A) ADD R1300 BETWEEN J200-1 AND PAN\_XIB
  - B) ADD BYPASS CAP C1100 NEAR U802 ON +3V\_CLKGEN\_SLEEP
  - C) MOVE RESISTORS R963,R964 AND R965 NEAR PANGEA
  - D) CHANGE C803,C804 AND C805 FORM 1.0U TO 10.0U WITH 0805 PACKAGE
  - E) ADD 4 MORE VIAS WHERE +3VCORE\_SLEEP OF C800,C801,C836
  - F) ADD AN EXTRA VIA ON PIN9 OF U32 TO GROUND
  - G) MAKE THE TRACE FROM PIN2 OF D31 GO FIRST TO PIN1 OF C156, THEN TO PIN2 OF R1557
  - H) MOVE R1555 CLOSER TO U1 AND L1
- 4) ACCORDING RADAR#2805288 - CHANGE TO OVERTEMP CIRCUIT
  - A) CHANGE R1206 FORM 39K TO 27K
- 5) ACCORDING RADAR#2805242 - ADD RESISTOR TO SCC RTS SIGNAL FOR TESTING PURPOSES
  - A) ADD R967 BETWEEN PIN1 OF U210 AND SCC\_RTSA\*
  - B) NAMED SLINK\_TX\_ENABLE\_L ON U210 PIN1
- 6) ACCORDING RADAR#2794331 - REMOVE BLEED CIRCUIT FOR VCORE RAIL
  - A) NOSTUFF C177,R15,Q6,C20,R11,Q8

- 7) ACCORDING RADAR#2804787 - SCHEMATIC CHANGE-MOVE FAN TO SLEEP RAIL
  - A) USE J900(NEW FOXCONN AUDIO JACK) TO REPLACE J13
- 8) ACCORDING RADAR#2801304 - RETURN JOLLY ROGER OPTION
  - A) CONNECT SCC\_RTSA\* TO PIN6 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR
  - B) CONNECT SCC\_RXDA TO PIN9 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR
  - C) CONNECT SCC\_TXDA\* TO PIN12 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR
  - D) CONNECT SCC\_DTRA TO PIN8 OF J2
  - E) CONNECT SCC\_TRXCA TO PIN14 OF J2
- 9) ACCORDING RADAR#2804786 - REMOVE CPU\_VOCRE\_LO\_OC CIRCUIT
  - A) REMOVE R832 AND Q808
- 10) ACCORDING RADAR#2803484 - ADD SLOW\_CHRG AND FAST\_CHRG BOM OPTION
  - A) ADD TWO ROW OF BOM OPTION FOR - SLOW\_CHRG FOR P72, FAST\_CHRG FOR P73
  - B) REMOVE THE HWCHG BOM FROM R539 AND ADD THE OMIT LABEL
  - C) ADD A BOM OPTION FOR R539 - SLOW\_CHRG 3.16K AND FAST\_CHRG 2.61K
- 11) ACCORDING RADAR#2792009 - REMOVE UNUSED SCC LINES FOR MODEM
  - A) REMOVE NETS SCC\_DTRA\* AND SCC\_TRXCA
  - B) KEEP THE PULLDOWN RESISTORS ON SCC\_GPIOA\* AND SCC\_TRXCA
- 12) ACCORDING RADAR#2800865 - I CAN'T CHARGE IPOD WHILE IBOOK IS SLEEPING
  - A) ADD A 10BQ040 ,CATHODE CONNECT TO +FW\_VP\_FUSE\_SW AND ANODE TO +28V\_PWRBUS\_SW
- 13) ACCORDING RADAR#2802944 - ATI SUGGESTION FOR AGP SUSPEND
  - A) ADD A 0 OHM RESISTOR R966 BETWEEN AGP\_SUS\_STAT\_L\_PU AND AGPSTOP\*
- 14) ACCORDING RADAR#2803479 - CHANGE SOME TANTALUM AUDIO CAPS TO CERAMIC
  - A) CHANGE C607,C608 AND C391 FROM 1.0U TANT(127S1001) TO 1.0U CERMIC (132S1061)
- 15) ACCORDING RADAR#2803487 - MODIFICATION TO BATTERY CHARGING CIRCUIT
  - A) ADD A 0 OHM RESISTOR SERIES BETWEEN PIN12 OF U32 AND PIN2 OF D31
  - B) ADD A NOSTUFF 0.01U 003 CAP BETWEEN PIN4 OF Q73 AND PS\_GND
- 16) ACCORDING RADAR#2794253 - TBEN CIRCUIT-CHANGE D FLIP FLOPS TO JK
  - A) REPLACE THE DIVIDEBY THREE CIRCUIT WITH A DUAL J-K FLIP FLOP 74LVC109
- 17) ACCORDING RADAR#2800233 - CHANGE POWER SUPPLY FOR INTERNAL M6 DDR MEMORY
  - A) CHANGE THE VDDM OF M6 TO 2.5V. SO, UNSTUFF R949 AND STUFF R950
- 18) ACCORDING RADAR#2794264 - AC CONNECTOR WAKE FROM SLEEP CIRCUIT CAHNGE
  - A) MOVE F100 FROM PAGE 25 TO PAGE 28
  - B) REMOVE TP210 AND TP211
- 19) ACCORDING RADAR#2794755 - HSYNC AND VSYNC NEED TO BE MOVED TO DAC2
  - A) MOVE ATI\_VSYNC FROM PIN AE23 TO PIN AF13
  - B) MOVE ATI\_HSYNC FROM PIN AE24 TO PIN AE14
- 20) ACCORDING RADAR#2795893 - VGA\_VCORE\_HI NEEDS TO BE HIGH AT POWERON
  - A) CHANGE R956 TO 10K AND CONNECT TO +3V\_MAIN
- 21) ACCORDING RADAR#2795903 - UNSTUFFED COMPONENTS ON SCHEMATICS
  - A) UNSTUFF R1112 AND STUFF R1111,R1110,C1109,C1110,Q810 AND Q809
- 22) ACCORDING RADAR#2797834 - REMOVE PMU RESET BUTTON
  - A) NOSTUFF S4
- 23) ACCORDING RADAR#2754201- LENGTH CONSTRAINTS FOR CPU BUS SIGNALS
  - A) CHANGE THE CONSTRAINTS OF CPU BUS TO 2500:3500 AND THE MAX COUT OF VIA TO 5
- 24) ACCORDING RADAR#2794312 - FAN CIRCUITRY CHANGE
  - A) CHANGE THE NAME OF THERM\* TO THERM\_OD\*
  - B) CHANGE R1206 TO 39K
- 25) ACCORDING RADAR#2794262- INVESTIGATE M6 PLL POWER RAIL ARRANGEMENT
  - A) UNSTUFF R951 AND CONNECT +1\_8V\_PVDD\_MAIN TO +1\_8V\_LVDDR\_MAIN
- 26) ACCORDING RADAR#2794249 - NEW SPREAD SPECTRUM PART
  - A) CHANGE THE SPREAD SPECTRUM CHIP FROM IMI C9531 TO CYPRESS CY28507
  - B) ADD 2 RESISTORS - ONE BETWEEN PMU\_IIC\_CLK AND +3\_3V\_PMU ANOTHER IS PMU\_IIC\_DAT AND +3\_3V\_PMU
- 27) ACCORDING RADAR#2779003 - ADD A BOM OPTION TO PREPARE FOR SAHARA DD2.0
  - A) SET DD1X BOM OPTION FOR P72/P73 AND CHANGE THE BOM OPTION OF Q800,Q801,R804,R805 TO DD1X
- 28) ACCORDING RADAR#2780490 - NEW FAN SPEED CONTROL CIRCUIT
  - A) ADD A NEW FAN CONTROL CIRCUIT ADM1030 TO REPLACE THE TWO THERMOSTATS
- 29) ACCORDING RADAR#2791511 - ADD PMU RESET FROM KEYBOARD CIRCUIT
  - A) ADD RESET FUNCTION BY PRESSING THE SHIFT-CONTROL-FN-POWER KEY TO REPLACE RESET SWITCH
- 30) ACCORDING RADAR#2794257 - CHANGE NAME OF AGPREF\_PD
  - A) CHANGE THE NAME OF AGPREF\_PD TO AGPREF\_PU
- 31) ACCORDING RADAR#2794329 - REMOVE BLEED CIRCUIT FOR ATI\_CORE MAIN
  - A) REMOVE THE CURRENT BLEED CIRCUIT FOR ATI\_CORE\_MAIN IN THE BOTTOM LEFT CORNER ON PAGE 37

DESCRIPTION:  
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	D	051-6130-C	ACI: C ECS:1.0
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NONE			



# REVISION HISTORY (2)

- 32) ACCORDING RADAR#2791719 - SCHEMATIC CHANGE - REMOVE R1115
  - A) REMOVE R1115 BECAUSE SLEEP\_L\_LS IS ALREADY PULLED UP TO 5V RAIL
- 33) ACCORDING RADAR#2792071 - REMOVE UNUSED RGB SIGNALS ON PAGE 22
  - A) REMOVE THE UNUSED RGB SIGNALS ON PAGE 22 (PIN AF22,AF23,AF24 ON M6) AND ADD NC FOR THEM
- 34) ACCORDING RADAR#2792085 - REMOVE OLD HP\_DETECT SIGNALS ON PAGE 22
  - A) REMOVE THE COMPVID\_HP\_TEST AND COMPVID\_HP\_DETECT FROM PAGE 22 (AC20 AND AD20 ON M6)

## DVT (REV:0.3)

- 1) ACCORDING RADAR#2843372 - ADD BACK FIREWIRE DIODE
  - A) STUFF D1506
- 2) ACCORDING RADAR#2823008 - P72 EVT UNITS PLUG IN A BUS POWERED YANO FW HARD DRIVE - SCREEN GOES DARK. POWER PROBLEM
  - A) CHANGE THE NET OF D1506 PIN1 FROM +28V\_PWRBUS\_SW TO CHR9\_OUT AND NOSTUFF D1506
  - B) CHANGE C160 FROM 0.01UF TO 0.1UF
- 3) ACCORDING RADAR#2838736 - SCHEMATIC CHANGE - 700 MHZ AND 1.5V
  - A) CHANGE BOM TABLE OF CPU FROM 750MHZ TO 700MHZ
  - B) REMOVE THE BOM OPTION ON R825
  - C) CHANGE 600MHZ CPU VCORE TO 1.5V
- 4) ACCORDING RADAR#2840812 - CHANGE ALL MCLK LINES TO USE 0 OHM SERIES TERMINATION RESISTORS
  - A) CHANGE R841,R843,R847 TO 0 OHM
- 5) ACCORDING RADAR#2831933 - P72 PLL RANGE CONFIGURATIONS
  - A) ALL CONFIGS SHOULD NOW HAVE THE "MID" PLL RANGE OPTIONS (NO POWERSTEP)
  - B) ADD "MID OR HIGH RANGE NO PWRSTEP" AND "LOW OR MID PLL RANGE" ROW FOR P72 GOOD CONFIG
  - C) REMOVE "LOW PLL RANGE" ROW UNDER THE P72 CONFIGURATION
- 6) ACCORDING RADAR#2830139 - P72 IMPLEMENT POWERPLAY ON M6 ON P72
  - A) CHANGE C1505 TO 680P AND ADD C1521 1000P
- 7) ACCORDING RADAR#2831140 - P72 SCHEMATIC REVIEW ACTION ITEMS
- 8) ACCORDING RADAR#2824938 - REQUIRED WAKEUP PULSE ON P72 HEADPHONE JACK TAKES TOO LONG (H/W)
  - A) CHANGE C1210 WITH 0.047UF CAP AND PACKAGE FROM 0805 TO 0603
- 9) ACCORDING RADAR#2829465 - AUDIO FIX - Q900
  - A) PIN 2 AND 3 OF Q900 ARE REVERSED. PIN2 SHOULD CONNECT TO GROUND.
- 10) ACCORDING RADAR#2820867 - TBEN DIVIDE-BY-THREE SCHEMATIC REPAIR
  - A) CHANGE NET OF U802 PIN1 AND PIN15 FROM +3V\_CLKGEN\_SLEEP TO CPU\_VCORE\_HI\_OC
- 11) ACCORDING RADAR#2825538 - KEYBOARD CHORD RESET OF PMU BOOTS
  - A) CHANGE NET OF U800 PIN5 FROM FN\_KEY\_L TO OPTION\_KEY\_L
  - B) NOSTUFF R19
  - C) CHANGE R1554 FROM 1K(113S1103) TO 10K(113S1104)
- 12) ACCORDING RADAR#2828251 - PMU IIC PULLUPS WRONG AT EVT
  - A) ADD R1120 10K RESISTOR BETWEEN +3V\_SLEEP AND THE SIGNAL PMU\_IIC\_DAT
  - B) ADD R1121 10K RESISTOR BETWEEN +3V\_SLEEP AND THE SIGNAL PMU\_IIC\_CLK
  - C) CHANGE THE VOLTAGE ON R1118-2 FROM +3\_3V\_PMU TO +3V\_CLKGEN\_SLEEP
  - D) CHANGE THE VOLTAGE ON R1119-2 FROM +3\_3V\_PMU TO +3V\_CLKGEN\_SLEEP
- 13) ACCORDING RADAR#2829528 - UPDATE NO PWRSTEP BOM OPTION FOR NEW PLL RANGE BITS
  - A) ADD R1122 10K (BETWEEN Q806 PIN2 AND PIN3) WITH "MID OR HIGH RANGE NO PWRSTEP"
  - B) ADD R1123 4.7K (BETWEEN Q807 PIN2 AND PIN3) WITH "HIGH PLL RANGE NO PWRSTEP"
  - C) CHANGE Q806 BOM OPTION TO "MID OR HIGH RANGE PWRSTEP"
  - D) CHANGE Q807 BOM OPTION TO "HIGH PLL RANGE PWRSTEP"
  - E) DELETE TWO ROWS ON PAGE 1 "MID RANGE PLL" AND "MID OR HIGH RANGE PLL"
  - F) ADD 4 ROWS ON PAGE 1 - "MID OR HIGH RANGE NO PWRSTEP", "HIGH PLL NO PWRSTEP", "MID OR HIGH RANGE PWRSTEP", "HIGH PLL RANGE PWRSTEP"
- 14) ACCORDING RADAR#2830159 - FAST CHARGE FOR ALL SYSTEM CONFIGS
  - A) CHANGE ALL SYSTEM CONFIGS TO USE THE FAST\_CHRG OPTION ON PAGE 1
- 15) ACCORDING RADAR#2841691 - SERIAL LINE REMAINS AT INTERMEDIATE LEVEL
  - A) CHANGE R959 FROM 100K(113S1105) TO 470K (113S1475)
  - B) CHANGE C1210 FROM 0.047UF (132S4743) TO 0.01UF (132S1045)

## DVT2 (REV:0.4)

- 1) ACCORDING RADAR#2855154 - SNAPPER AUDIO CHIP NEEDS SEPARATE RESET
  - A) ADD Q901,Q902 (2N7002), AND R1031 (100K,5%)
  - B) CHANGE NET NAME OF U300 PIN6 FROM IO\_RESET\_L TO TAS\_RESET\_L
- 2) ACCORDING RADAR#2856224 - SCHEMATIC CHANGE - ARTRY PULL UP
  - A) DISCONNECT ARTRY\* FROM RP101
  - B) PULL UP ARTRY\* WITH 1K RESISTOR (R1032) TO +VIO\_CPU\_SLEEP
- 3) ACCORDING RADAR#2856231 - MORE BYPASS CAPACITORS ON SAHARA
  - A) ADD C980,C981(10U 0805) FOR +VCORE\_SLEEP
- 4) ACCORDING RADAR#2862722 - INCREASE BANDWIDTH OF MICROPHONE AMPLIFIER
  - A) CHANGE C1017 FROM 0.022UF TO 0.047UF
  - B) CHANGE C1021 FROM 150P TO 47P
  - C) CHANGE C1022 FROM 0.047UF TO 0.1UF
  - D) CHANGE R1019 FROM 36K TO 10K

- 5) ACCORDING RADAR#2831587 - P72 EVT : POP HEARD WHEN PLUG HEADPHONES INTO ANALOG LINE OUT
  - A) CHANGE R139 FROM 100K TO 470K
- 6) ACCORDING RADAR#2862391 - CHANGE NAME OF BOM OPTION
  - A) CHANGE R1123 BOM OPTION TO "HIGH PLL RANGE NO PWRSTEP"
  - B) CHANGE PAGE 1 BOM TABEL FROM "HIGH PLL RANGE NO PWRSTEP" TO "HIGH\_PLL\_RANGE\_NO\_PWRSTEP"
- 7) ACCORDING RADAR#2865479 - CHANGE CPU VCORE SETTING (LOW SETTING AND VOLTAGE POSITIONING)
  - A) CHANGE R1531 FROM 1K TO 100K FOR P72 GOOD CONFIGURATION
  - B) CHANGE R1535 FROM 100K TO 1K
  - C) DELETE R1542 AND R1543
  - D) ADD A 0 OHM RESISTOR R1560

## PVT (REV: A)

- 1) ACCORDING RADAR#2868519 - SOUND LEVEL RESETS TO LOW - UPDATE FOR PVT
  - B) ADD A NAND GATE 74LVC1G32 FOR AUDIO RESET CIRCUIT
- 2) ACCORDING RADAR#2874422 - FIREWIRE DEAD ON P25 AND P92 DVT
  - A) ADD TWO QUAD DIODE FOR PHYTPA0T,PHYTPA0C,PHYTPB0T,PHYTPB0C
- 3) ACCORDING RADAR#2878614 - P72/P73 POPS FROM INTERNAL SPEAKERS POST AUDIO REWORK
  - A) NOSTUFF D100 AND D101
  - B) CHANGE C1026 AND C1027 FROM 0.047UF TO 0.1UF
- 4) ACCORDING RADAR#2882917 - FIREWIRE AND BATTERY CHARGING PROTECTION
  - A) STUFF DZ8 AND DZ9
  - B) CHANGE VALUE OF C467 TO 0.1UF

## PVT (REV: A)

- 1) ACCORDING RADAR#2890158 - P72 DEPLETED BATTERY MAY NOT CHARGE IN SYSTEM
  - A) CHANGE R518 AND R538 FROM 100K TO 93.1K

## PVT2 (REV: A)

- 1) ACCORDING RADAR#2910360 - MATCH P72 SPEAKER AMP TO P92
  - A) CHANGE C397 AND C402 FROM 0.01UF(132S1045) TO 0.047UF(132S4743)
  - B) CHANGE R424 AND R431 FROM 27K(113S1274) TO 20.5K(110S2054)
  - C) CHANGE R428 AND R423 FROM 47K(113S1474) TO 36K(113S1364)
- 2) ACCORDING RADAR#2917330 - ADD BOOTBANGER BOARD TO P72/73
  - A) ADD OASIS AND MIRAGE OPTIONS TO THE BOM OPTION TABLE AT PAGE 1
  - B) CHANGE THE BOM OPTION OF J19 FROM NONPRODUCTION TO OMIT AT PAGE 15
  - C) ADD OMIT BOM OPTION TO R1531 AND R1535 AT PAGE 38.

## RAMP (REV: B)

- 1) ACCORDING RADAR#2917330 - ADD BOOTBANGER BOARD TO P72/P73
  - A) PAGE 38: CHANGE CPU VCORE SETTING TO 1.2V/1.5V
  - B) PAGE 14: ADD MIRAGE BOMOPTION TO R268
  - C) PAGE 15: ADD MIRAGE BOMOPTION TO R274
- 2) ACCORDING RADAR#2933296 - DIFFERENT CPU ACI P/N AND UPDATE SCH VERSION
  - A) PAGE 1 : ADD OASIS AND MIRAGE BOMOPTIONS FOR P72/P73
  - B) PAGE 3 : ADD MIRAGE CPU ACI P/N
  - C) CHANGE SCHEMATICS VERSION TO B
- 3) ACCORDING RADAR#2933252 - CHNAGE THE FAN FET TO A STRONGER PART
  - A) PAGE 35: CHANGE Q1001 FROM 2N7002 TO SI2302DS(372S0027)

## RAMP (REV: C)

- 1) ACCORDING RADAR#2942313 - MORE POST-RAMP SCHEMATIC MODIFICATIONS
  - A) PAGE 19: STUFF FIREWIRE PROTECTION DIODES DZ8 AND DZ9
  - B) PAGE 16: CHANGE J2 ACI P/N TO 516S0002
  - C) UPDATE SCHEMATICS VERSION TO REV.C
- 2) ACCORDING RADAR#2945017 - F3 BOOTROM
  - A) PAGE 20: CHANGE BOOTROM ACI P/N TO 341S1036

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NONE			





Main table with 8 columns (8-1) and 3 rows (A-C) containing component lists and reference designator location indexes.

\*\*\* Signal Cross-Reference \*\*\*  
--- for the entire design ---

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REFERENCE DESIGNATOR LOCATION INDEX (1)

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TCPUFBOUT 5 41  
 TEA\* 3 5 14 39  
 TEMP 21  
 TERM\_M\_ADDR<12..0> 6 7 8 40  
 TI\_CAP\_PLL 26  
 TI\_CS1 26  
 TI\_CS2 26  
 TI\_MOD0 26  
 TI\_MOD1 26  
 TI\_MOD2 26  
 TI\_TI\_SD 26  
 TI\_VCOM 26  
 TRKPAD\_RXD 21  
 TRKPAD\_TXD 21  
 TS\* 3 5 14 39  
 TSI2<2..0> 3 5 39  
 TT<4..0> 3 5 39  
 TXVSSR1 38  
 T\_MEMWE\* 6 7 8 41  
 T\_M\_BA0 6 7 8 41  
 T\_M\_BA1 6 7 8 41  
 T\_PANGEMCLK<6..6> 7  
 T\_PMU\_ACK\* 21  
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 T\_RAM\_CKE0\_L 7  
 T\_RAM\_CKE0\_MLB 7  
 T\_RAM\_CKE0\_MLB\_R 7  
 T\_RAM\_CKE0\_R 7  
 T\_RAM\_CKE1 7 8  
 T\_RAM\_CKE1\_L 7  
 T\_RAM\_CKE1\_R 7  
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 T\_ROMOE\* 6 20  
 T\_ROMWE\* 6 20  
 T\_SDCAS\* 6 7 8 41  
 T\_SDO 26  
 T\_SDRAS\* 6 7 8 41  
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 T\_UIDE\_CS1\_L 12 16  
 T\_UIDE\_D<15..0> 12 16  
 T\_UIDE\_DA<2..0> 12 16  
 T\_UIDE\_DIOR\_L 12 16 43  
 T\_UIDE\_DIOW\_L 12 16 43  
 T\_UIDE\_DMAACK\_L 12 16  
 T\_UIDE\_DMAREQ 12 16  
 T\_UIDE\_IORDY\_L 16  
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 UIDE\_DA<2..0> 12 43  
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 UIDE\_DMAREQ 12 43  
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 UNI\_IIC\_DAT1 10 15 34  
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 URESET\* 10  
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 USB\_DBF\_T 25  
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 USB\_DDP\_T 16  
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 USB\_PWRFLT\_B 13 17  
 USB\_PWR\_A 13 17 38  
 USB\_PWR\_B 13 17 38  
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 USB\_PWR\_FLT\_CD 38  
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 VCORE\_LX 35 41  
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 VCORE\_SYNC 35  
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 VGA\_DETECT\* 22 24  
 VGA\_G 24  
 VGA\_HSYNC 24  
 VGA\_R 24  
 VGA\_VSYNC 24  
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 VREFP 26  
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 XTALOUT 22  
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 \_VCHRG 31  
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 SLEEP\_LED 21  
 SLEEP\_LS 27 34  
 SLEEP\_L\_LS 18 19 25 34 35  
 SMB\_CLK 21 32  
 SMB\_SDA 21 32  
 SPEAKER\_RET 44  
 SPKR\_STAR\_GND 26 27 28 37 44  
 SRESET\* 3 14 15  
 SSIN 22  
 SSOUT 22  
 SS\_S0 22  
 SS\_S1 22  
 SS\_SD 22  
 STANDBY\_PU 22 23  
 STOPXTAL\* 13 21  
 SUSPEND\_PU 22  
 TICS0\* 6 7 41  
 TICS1\* 6 41  
 TICS2\* 6 8  
 TICS3\* 6 8  
 TA\* 3 5 14 39  
 TBST\* 3 5 14 39

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			NONE	50	53

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\*\*\* Unit Cross-Reference \*\*\*  
--- for the entire design ---

A1	CAP	13
A2	CAP	13
A3	CAP	11
A4	CAP	11
A5	CAP	11
A6	CAP	11
A7	CAP	11
A8	CAP	13
A9	CAP	11
A10	CAP	11
A11	CAP	11
A12	CAP	11
A13	CAP	11
A14	CAP	11
A15	CAP	5
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