1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-04-08

K78 MLB SCHEMATIC

04/08/11

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8871	1	SCHEM,MLB,K78	SCH	CRITICAL	
820-3024	1	PCBF,MLB,K78	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Apr 8 10:25:51 2011

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: SCHEM,MLB,K78

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
REVISION: 2.5.0
BRANCH:
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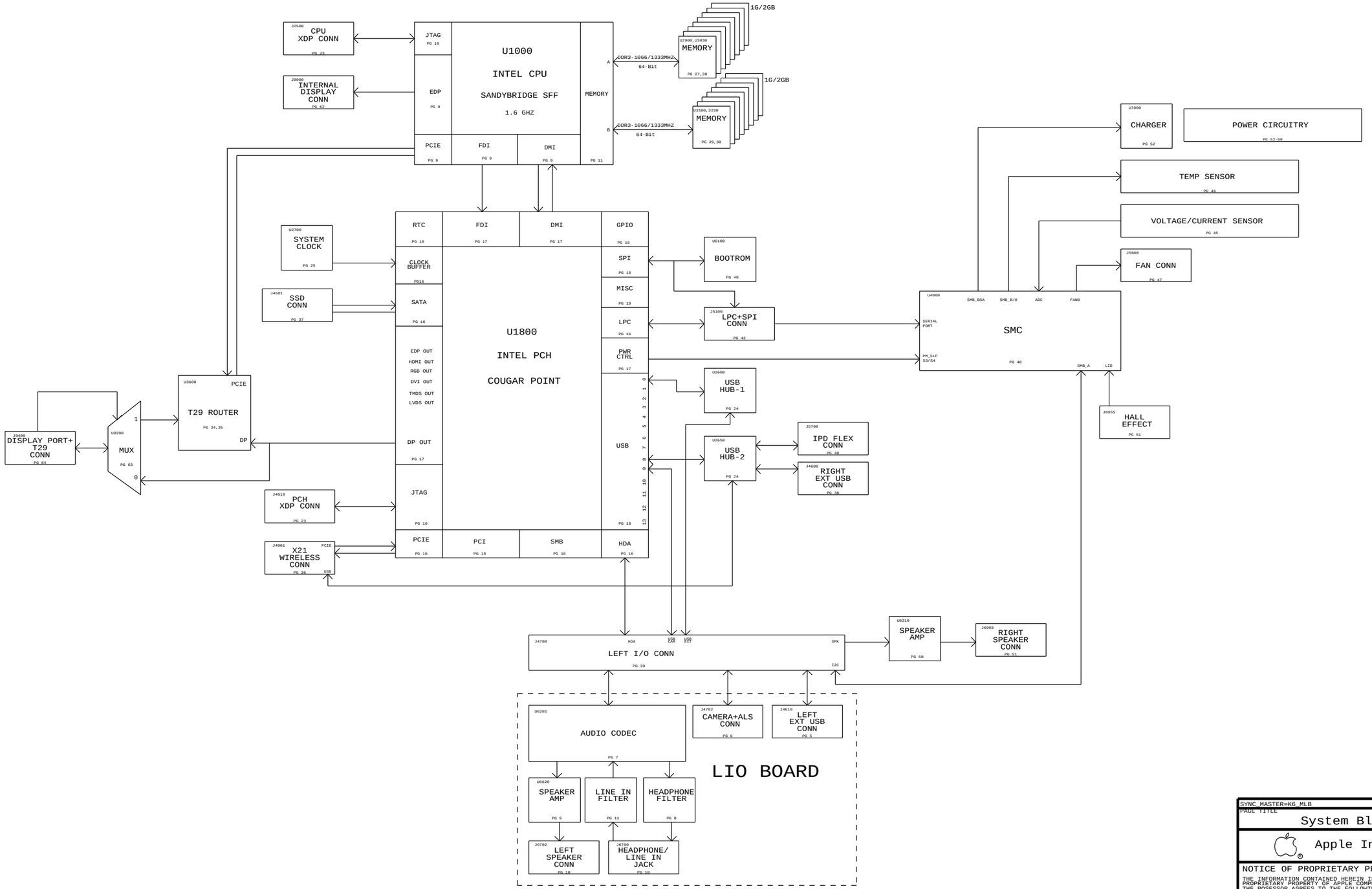

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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K78/K21 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(14.5V)
F6905 6A FUSE
SMC_DCIN_ISENSE
R7020
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 53)
VIN
VOUT
PPVBAT_G3H
SMC_RESET_L
R7050
SMC_BATT_ISENSE
J6950
PPVBATT_G3H_CONN
2S3P (6 TO 8.4V)
Q7055
PPVBAT_G3H_CHGR_R
CHGR_BGATE
PPDCIN_G3H_OR_PBUS
R6905
PPVIN_G3H_P3V42G3H
D6905
R6920
F7040
PPBUS_G3H
R5400
PP5V_S0_CPUVCCIOS0
CPUVCCIOS0_EN
U7600 ISL95870 1.05V
(PAGE 59)
PGOOD
CPUVCCIOS0_PGOOD
R7640
PPCPUVCCIO_S0_REG
SMC_CPU_FSB_ISENSE
TPS22924 U3816/U3815
(PAGE 36)
EN
PP1V05_T29_FET
T29_PWR_EN
R5320 SMC_CPU_VSENSE
PPVCORE_S0_CPU_REG
CPU VCORE MAX15092GTL U7400
CPUIMVP_VR_ON
VR_ON
(PAGE 57)
R5330 SMC_GFX_VSENSE
PPVCORE_S0_AXG_REG
CPUIMVP_PGOOD
CPUIMVP_AXG_PGOOD
DDRREG_EN
DDRVTT_EN
TPS51916 U7300 1.5V S5 0.75V S3
(PAGE 56)
VLDOIN
VOUT1
VOUT2
R7350
PPDDR_S3_REG
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
U7801
P1V5CPU_EN
PP1V5_S3RS0_FET
PP5V_S0_VCCSA
PVCCSA_EN
CPU_VCCSA_VID<1>
ISL95870A U7100
(PAGE 54)
VID1
PPVCCSA_S0_REG
R7140
PVCCSA_PGOOD
SMC POWER SN0903048 U5010 (PAGE 42)
SMC_RESET_L
ENABLE 3.425V G3HOT LT3470A U6990 (PAGE 52)
PP3V42_G3H_REG
COUGAR-POINT (PCH)
PWRBTN#
SYS_RESET#
RSMRST#
DPWROK
PLTRST#
PROCPWRGD
DRAMPWROK
PM_PCH_PWRGD
U2850
(PAGE 17~21)
PM_PWRBTN_L
PM_SYSRST_L
PM_RSMRST_L
PM_DSW_PWRGD
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
CPU U1000
SM_DRAMPWROK
UNCOREPWRGOOD
RESET*
(PAGE 9~15)
SMC U4900
(PAGE 41)
PWRGD(P12)
RSMRST_IN(P13)
PWR_BUTTON(P90)
RSMRST_OUT(P15)
99ms DLY
IMVP_VR_ON(P16)
SYSRST(PA2)
P17(BTN_OUT)
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
RES*
PM_DSW_PWRGD
PM_RSMRST_L
CPUIMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
R7962
S5_PWRGD
SMC_ONOFF_L
VDD U7960 ISL88042IRTEZ
(PAGE 62)
PP3V3_S0_VMON
PP5V_S0_VMON
PP1V5_S3RS0_VMON
PP1V05_S0_VMON
SMC U4900
(PAGE 41)
P60
SMC_PM_G2_EN
RC DELAY
P3V3S5_EN
COUGAR-POINT (PCH)
U1800
(PAGE 17~21)
SLP_S5#(E4)
PM_SLP_S5_L
SLP_SUS#
PM_SLP_SUS_L
U7940
P5V_3V3_SUS_EN
P3V3S3_EN
DDRREG_EN
P5VS3_EN
SLP_S4#(H4)
PM_SLP_S4_L
SLP_S3#(F4)
PM_SLP_S3_L
R7978
PM_SLP_S3_R_L
1V05_S0_LDO_EN
CPUVCCIOS0_EN
PVCCSA_EN
P1V5S0_EN
P1V8S0_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
PPVIN_S5_P5VP3V3
VIN 5V (L/H) 3.3V (R/H)
TPS51980 U7201
(PAGE 55)
EN1
EN2
VOUT1
VOUT2
PGOOD
P5VS3_EN
P3V3S5_EN
PP5V_S3_REG
PP3V3_S5_REG
PP3V3_S5
P5VS3_PGOOD
P3V3S5_PGOOD
Q7860
P5VS0_EN
PP5V_S0_FET
TPS720105 U7740
(PAGE 60)
PP3V3_SUS_FET
PP1V05_SUS_LDO
Q7820
P5V_3V3_SUS_EN
Q7810
P3V3S3_EN
PP5V_SUS_FET
Q7840
F9700
LCD_BKLT_EN
&& BKLT_PLT_RST_L
Q9706
VIN LP8550 U9701
(PAGE 66)
PPBUS_SW_LCDBKLT_PWR
EN
VOUT
PPVOUT_SW_LCDBKLT
Q5300
SMC_PBUS_VSENSE
PBUSVSENS_EN
Q3880
T29_A_HV_EN
T29BST_EN_UVLO
VIN LT3957 U3890
EN/UVLO
(PAGE 36)
PP15V_T29_REG
PP3V3_S0
P1V8S0_EN
ISL8014A U7720
(PAGE 60)
PP1V8_S0_REG
P1V8S0_PGOOD
1V05_S0_LDO_EN
TPS720105 U7780
PP1V05_S0_LDO.
U7770 TPS72015
(PAGE 60)
PP1V5_S0_REG
T29_PWR_EN
TPS22924 U3810
(PAGE 36)
PP3V3_T29_FET
PP1V5S0_EN
Q7830
P3V3S0_EN
CPUIMVP_AXG_PGOOD
P1V8S0_PGOOD
P5VS3_PGOOD
P3V3S5_PGOOD
CPUVCCIOS0_PGOOD
PVCCSA_PGOOD
ALL_SYS_PWRGD

SYNC_DATE=19/01/2011

PAGE TITLE: Power Block Diagram

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1808	PCBA,MLB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DK9L,DDR3:HYNIX_2GB
639-1989	PCBA,MLB,1.6GHZ,HY 4GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLCR,DDR3:HYNIX_4GB
639-1990	PCBA,MLB,1.6GHZ,SA 2GB,K78	K78_CMNPTS,CPU:1.66HZ,EEEE:DLCT,DDR3:SAMSUNG_2GB
639-1999	PCBA,MLB,1.6GHZ,SA 4GB,K78	K78_CMNPTS,CPU:1.66HZ,EEEE:DLD6,DDR3:SAMSUNG_4GB
639-1987	PCBA,MLB,1.6GHZ,MI 2GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLCP,DDR3:MICRON_2GB
639-1995	PCBA,MLB,1.6GHZ,EL 4GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLD1,DDR3:ELPIDA_4GB
639-1998	PCBA,MLB,1.5GHZ,HY 2GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLD4,DDR3:HYNIX_2GB
639-1991	PCBA,MLB,1.5GHZ,HY 4GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCV,DDR3:HYNIX_4GB
639-1986	PCBA,MLB,1.5GHZ,SA 2GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCN,DDR3:SAMSUNG_2GB
639-1985	PCBA,MLB,1.5GHZ,SA 4GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCM,DDR3:SAMSUNG_4GB
639-1992	PCBA,MLB,1.5GHZ,MI 2GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCW,DDR3:MICRON_2GB
639-1993	PCBA,MLB,1.5GHZ,EL 4GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCY,DDR3:ELPIDA_4GB
639-1994	PCBA,MLB,1.4GHZ,HY 2GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD0,DDR3:HYNIX_2GB
639-1988	PCBA,MLB,1.4GHZ,HY 4GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLCQ,DDR3:HYNIX_4GB
639-1997	PCBA,MLB,1.4GHZ,SA 2GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD3,DDR3:SAMSUNG_2GB
639-1984	PCBA,MLB,1.4GHZ,SA 4GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLCL,DDR3:SAMSUNG_4GB
639-2000	PCBA,MLB,1.4GHZ,MI 2GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD5,DDR3:MICRON_2GB
639-1996	PCBA,MLB,1.4GHZ,EL 4GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD2,DDR3:ELPIDA_4GB
085-2714	K78 MLB DEVELOPMENT BOM	K78_DEVEL:ENG
607-8084	CMN PTS,PCBA,MLB,K78	K78_COMMON

Bar Code Labels / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,LIO,K99	[EEEE_DK9L]	CRITICAL	EEEE:DK9L
825-7563	1	LABEL,LIO,K99	[EEEE_DLCL]	CRITICAL	EEEE:DLCL
825-7563	1	LABEL,LIO,K99	[EEEE_DLCM]	CRITICAL	EEEE:DLCM
825-7563	1	LABEL,LIO,K99	[EEEE_DLCN]	CRITICAL	EEEE:DLCN
825-7563	1	LABEL,LIO,K99	[EEEE_DLCP]	CRITICAL	EEEE:DLCP
825-7563	1	LABEL,LIO,K99	[EEEE_DLCQ]	CRITICAL	EEEE:DLCQ
825-7563	1	LABEL,LIO,K99	[EEEE_DLCR]	CRITICAL	EEEE:DLCR
825-7563	1	LABEL,LIO,K99	[EEEE_DLCT]	CRITICAL	EEEE:DLCT
825-7563	1	LABEL,LIO,K99	[EEEE_DLCV]	CRITICAL	EEEE:DLCV
825-7563	1	LABEL,LIO,K99	[EEEE_DLCW]	CRITICAL	EEEE:DLCW
825-7563	1	LABEL,LIO,K99	[EEEE_DLCY]	CRITICAL	EEEE:DLCY
825-7563	1	LABEL,LIO,K99	[EEEE_DLD0]	CRITICAL	EEEE:DLD0
825-7563	1	LABEL,LIO,K99	[EEEE_DLD1]	CRITICAL	EEEE:DLD1
825-7563	1	LABEL,LIO,K99	[EEEE_DLD2]	CRITICAL	EEEE:DLD2
825-7563	1	LABEL,LIO,K99	[EEEE_DLD3]	CRITICAL	EEEE:DLD3
825-7563	1	LABEL,LIO,K99	[EEEE_DLD4]	CRITICAL	EEEE:DLD4
825-7563	1	LABEL,LIO,K99	[EEEE_DLD5]	CRITICAL	EEEE:DLD5
825-7563	1	LABEL,LIO,K99	[EEEE_DLD6]	CRITICAL	EEEE:DLD6

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-2714	1	K78 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-8084	1	CMN PTS,PCBA,MLB,K78	CMNPTS	CRITICAL	K78_CMNPTS

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE

K78 BOM Variants

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K78 BOM GROUPS

BOM GROUP	BOM OPTIONS
K78_COMMON	ALTERNATE,COMMON,K78_MISC,K78_DEBUG:ENG,K78_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP
K78_MISC	PCH:B3,CPUMEM_S0,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRVI2C:MCU,SDRV_PD,KB_BL
K78_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K78_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
K78_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K78_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K78_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K78_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0550	1	EEPROM,32KBIT,2X3QFN	U3690	CRITICAL	T29ROM:BLANK
341T0354	1	IC,T29-ROM,K78	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0355	1	IC,T29-MCU,K78	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,RENESAS,H8S/2117RP,9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341T0350	1	IC,SMC,K78	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
341T0349	1	IC,EFI ROM,K21 K78	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
377S0107	377S0066		ALL	ONsemi alt to Semtech
138S0676	138S0691		ALL	Murata alt to Samsung
371S0679	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
138S0679	138S0678		ALL	Murata/Samsung alt to Taiyo
353S3312	353S3055		ALL	NXP ALT TO PERICOM
104S0035	104S0011		ALL	Panasonic alt to Cyntec
152S1085	152S1307		ALL	Toko alt to Cyntec
152S1462	152S1295		ALL	Toko alt to NEC inductor
128S0333	128S0294		ALL	Sanyo alt to Sanyo/Frederick
33754092	33754100		ALL	EARLY 1.5GHZ CPU SAMPLES
33754093	33754101		ALL	EARLY 1.4GHZ CPU SAMPLES
376S0874	376S0895		ALL	FDMC0202S alt to RJK03E0DNS
376S1018	376S0617		ALL	FDMS0349 alt to RJK0305DPB
376S0826	376S0917		ALL	RJK0332DPB alt to FDMS0355
514-0744	998-3941		ALL	mDP connector alt

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4101	1	SNB,QAM1,QS,J1,1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S4100	1	SNB,QAM2,QS,J1,1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
337S4099	1	SNB,QAM3,QS,J1,1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S4098	1	SNB,QALV,QS,J1,1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
337S4080	1	COUGAR POINT,SLHAG,PRQ,BD82QS67	U1800	CRITICAL	PCH:B2
337S4091	1	COUGAR POINT,B3,SLJ4K,PRQ,BD82QS67	U1800	CRITICAL	PCH:B3
338S0976	1	IC,T29, FCBGA,PRQ 8x9MM	U3600	CRITICAL	T29:YES
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

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BOM Configuration

Apple Inc.

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F (Need 6 TPs)	36
TRUE	WIFI_EVENT_L	36 40
TRUE	PCIE_AP_R2D_N	36 69
TRUE	PCIE_AP_R2D_P	36 69
TRUE	PCIE_CLK100M_AP_N	16 36 69
TRUE	PCIE_CLK100M_AP_P	16 36 69
TRUE	USB_BT_P	24 36 68
TRUE	USB_BT_N	24 36 68
TRUE	PCIE_AP_D2R_P	16 36 69
TRUE	PCIE_AP_D2R_N	16 36 69
TRUE	PCIE_WAKE_L	17 36
TRUE	AP_RESET_CONN_L	36
TRUE	AP_CLKREQ_O_L	36
TRUE	=PP3V3_S3_BT	7 36

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_HDD_R (Need 5 TPs)	37
TRUE	SATA_HDD_D2R_C_P	37 68
TRUE	SATA_HDD_D2R_C_N	37 68
TRUE	SATA_HDD_R2D_N	37 68
TRUE	SATA_HDD_R2D_P	37 68
TRUE	SMC_HDD_OOB_TEMP_CONN	37
TRUE	SMC_HDD_TEMP_CTL_CONN	37

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 39
TRUE	=PP3V3_S0_AUDIO	7 39
TRUE	=PP3V3R1V5_S0_AUDIO	7 39
TRUE	SYS_ONEWIRE	39 40
TRUE	SMC_BC_ACOK	39 40 41
TRUE	=USB_PWR_EN	38 39 61
TRUE	=I2C_LIO_SDA	39 43
TRUE	=I2C_LIO_SCL	39 43
TRUE	=I2C_MIKEY_SCL	39 43
TRUE	=I2C_MIKEY_SDA	39 43
TRUE	AUD_IPHS_SWITCH_EN	19 39
TRUE	AUD_IP_PERIPHERAL_DET	18 39
TRUE	AUD_I2C_INT_L	18 39
TRUE	AUD_GPIO_3	39 50
TRUE	SPKRAMP_INR_N	39 50 73
TRUE	SPKRAMP_INR_P	39 50 73
TRUE	USB_EXTD_N	24 39 68
TRUE	USB_EXTD_P	24 39 68
TRUE	USB_CAMERA_N	18 39 68
TRUE	USB_CAMERA_P	18 39 68
TRUE	HDA_SDOUT	16 39 69
TRUE	HDA_BIT_CLK	16 39 69
TRUE	HDA_SDIN0	16 39 69
TRUE	USB_EXTD_OC_L	24 39
TRUE	HDA_RST_L	16 39 69
TRUE	HDA_SYNC	16 39 69

(Need to add 5 GND TPs)

J5715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_FB	48
TRUE	KBDLED_ANODE	48

(Need to add 2 GND TPs)

J6955: HALL EFFECT Connector

TRUE	SMC_LID_R	51
TRUE	=PP3V42_G3H_HALL	7 51

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 42
TRUE	=PP5V_S0_LPCPLUS	7 42
TRUE	LPC_AD<3..0>	16 40 42 69
TRUE	SPI_ALT_MOSI	42
TRUE	SPI_ALT_MISO	42
TRUE	LPC_FRAME_L	16 40 42 69
TRUE	PM_CLKRUN_L	17 40 42
TRUE	SMC_TMS	40 41 42
TRUE	LPCPLUS_RESET_L	25 42
TRUE	SMC_TDO	40 41 42
TRUE	SMC_TRST_L	40 42
TRUE	SMC_MD1	40 42
TRUE	SMC_TX_L	38 40 41 42
TRUE	LPC_CLK33M_LPCPLUS	25 42 69
TRUE	SPIROM_USE_MLB	19 42 49
TRUE	SPI_ALT_CLK	42
TRUE	SPI_ALT_CS_L	42
TRUE	LPC_SERIRQ	16 40 42
TRUE	LPC_PWRDWN_L	17 40 42
TRUE	SMC_TDI	40 41 42
TRUE	SMC_TCK	40 41 42
TRUE	SMC_RESET_L	40 41 42 52
TRUE	SMC_NMI	40 42
TRUE	SMC_RX_L	38 40 41 42
TRUE	LPCPLUS_GPIO	19 42

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 47
TRUE	FAN_RT_TACH	47
TRUE	FAN_RT_PWM	47

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	SMC_PME_S4_WAKE_L	40 41 48
TRUE	PP5V_TPAD_FILT	48
TRUE	=PP3V42_G3H_TPAD	7 48
TRUE	PP3V3_TPAD_CONN	48
TRUE	USB_TPAD_CONN_P	48 73
TRUE	USB_TPAD_CONN_N	48 73
TRUE	=I2C_TPAD_SDA	43 48
TRUE	=I2C_TPAD_SCL	43 48
TRUE	SMC_ONOFF_L	40 41 48
TRUE	SMC_LID	40 41 48 51
TRUE	SMC_TPAD_RST_L	41 48

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 51 (Need 4 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 51 (Need 3 TPs)

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_R_P_OUT	50 51 73
TRUE	SPKRAMP_R_N_OUT	50 51 73

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	51 52 (Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	43 51
TRUE	=SMBUS_BATT_SDA	43 51
TRUE	SYS_DETECT_L	51

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	62 65 (Need 2 TPs)
TRUE	PP3V3_SW_LCD	62 (Need 2 TPs)
TRUE	I2C_TCON_SDA_R	62
TRUE	LED_RETURN_6	62 65
TRUE	LED_RETURN_5	62 65
TRUE	LED_RETURN_4	62 65
TRUE	LED_RETURN_3	62 65
TRUE	LED_RETURN_2	62 65
TRUE	LED_RETURN_1	62 65
TRUE	DP_INT_HPD_CONN	62
TRUE	DP_INT_AUX_CH_C_N	62 69
TRUE	DP_INT_AUX_CH_C_P	62 69
TRUE	DP_INT_ML_F_P<0>	62 69
TRUE	DP_INT_ML_F_N<0>	62 69
TRUE	DP_INT_ML_F_P<1>	62 69
TRUE	DP_INT_ML_F_N<1>	62 69
TRUE	I2C_TCON_SCL_R	62

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 51
TRUE	PPVIN_SW_T29BST	7 35
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7
TRUE	PPDCIN_G3H	7
TRUE	PP3V42_G3H	7
TRUE	PPVRTC_G3H	7
TRUE	PP5V_S5	7
TRUE	PP5V_SUS	7
TRUE	PP3V3_S5	7 73
TRUE	PP3V3_SUS	7
TRUE	PP3V3_S3	7
TRUE	PP1V8_S0	7
TRUE	PP3V3_S0	7 73
TRUE	PP1V5_S3	7 67
TRUE	PP1V5_S3RS0	7 67
TRUE	PP1V5_S0	7
TRUE	PP1V05_S0	7
TRUE	PPVTTDDR_S3	7
TRUE	PP0V75_S0_DDRVTT	7
TRUE	PPVCCSA_S0_CPU	7
TRUE	PP1V05_SUS	7
TRUE	PP15V_T29	7
TRUE	PP3V3_T29	7 (Need to add 27 GND TPs)
TRUE	PP1V05_T29	7 35
TRUE	PP1V05_S0_PCH_VCCADPLL	7
TRUE	PPVCORE_S0_CPU	7
TRUE	PPVCORE_S0_AXG	7
TRUE	PP1V5_S3_CPU_VCCDQ	7
TRUE	PP1V05_S0_CPU_VCCPQE	7
TRUE	PP1V8_S0_CPU_VCCPLL_R	7

NO_TEST Nets

NO_TEST

17	TP_CRT_IG_BLUE	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	TRUE, MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
	TP_LVDS_IG_CTRL_CLK	TRUE, MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
	TP_LVDS_IG_CTRL_DATA	TRUE, MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
	TP_PCH_LVDS_VBG	TRUE, MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	TRUE, MAKE_BASE=TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	TRUE, MAKE_BASE=TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	TRUE, MAKE_BASE=TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	TRUE, MAKE_BASE=TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	TRUE, MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
16	TP_CLINK_CLK	TRUE, MAKE_BASE=TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	TRUE, MAKE_BASE=TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	TRUE, MAKE_BASE=TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP
17	TP_SDVO_TVCLKINN	TRUE, MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	TRUE, MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	TRUE, MAKE_BASE=TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	TRUE, MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	TRUE, MAKE_BASE=TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	TRUE, MAKE_BASE=TRUE	NC_SDVO_INTP
23	TP_XDP_PCH_OBSFN_A<0..1>	TRUE, MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	TRUE, MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	TRUE, MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	TRUE, MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	TRUE, MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	TRUE, MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	TRUE, MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE, MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE, MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE, MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE, MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

	NC_EDP_TXP<0..3>	TRUE, MAKE_BASE=TRUE	TP_EDP_TX_P<0..3> 9
	NC_EDP_TXN<0..3>	TRUE, MAKE_BASE=TRUE	TP_EDP_TX_N<0..3> 9
	NC_EDP_AUXP	TRUE, MAKE_BASE=TRUE	TP_EDP_AUX_P
	NC_EDP_AUXN	TRUE, MAKE_BASE=TRUE	TP_EDP_AUX_N
	NC_CPU_THERMDA	TRUE, MAKE_BASE=TRUE	TP_CPU_THERMDA
	NC_CPU_THERMDC	TRUE, MAKE_BASE=TRUE	TP_CPU_THERMDC
	NC_CPU_RSVD<30..45>	TRUE, MAKE_BASE=TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27>	TRUE, MAKE_BASE=TRUE	TP_CPU_RSVD<8..27>
	NC_PEG_R2D_CP<15..4>	TRUE, MAKE_BASE=TRUE	=PEG_R2D_C_P<15..4> 9
	NC_PEG_R2D_CN<15..4>	TRUE, MAKE_BASE=TRUE	=PEG_R2D_C_N<15..4> 9
	NC_PEG_D2RP<15..4>	TRUE, MAKE_BASE=TRUE	=PEG_D2R_P<15..4> 9
	NC_PEG_D2RN<15..4>	TRUE, MAKE_BASE=TRUE	=PEG_D2R_N<15..4> 9

	TP_PCIE_CLK100M_PE4N	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
	TP_PCIE_CLK100M_PE4P	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
16	TP_PCIE_CLK100M_PE5N	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
16	TP_PCIE_CLK100M_PE5P	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
16	TP_PCIE_CLK100M_PE6N	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
16	TP_PCIE_CLK100M_PE6P	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
16	TP_PCIE_CLK100M_PE7N	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
16	TP_PCIE_CLK100M_PE7P	TRUE, MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
	TP_PSOC_P1_3	TRUE, MAKE_BASE=TRUE	NC_PSOC_P1_3
16	TP_SATA_B_D2RN	TRUE, MAKE_BASE=TRUE	NC_SATA_B_D2RN
16	TP_SATA_B_D2RP	TRUE, MAKE_BASE=TRUE	NC_SATA_B_D2RP
16	TP_SATA_B_R2D_CN	TRUE, MAKE_BASE=TRUE	NC_SATA_B_R2D_CN
16	TP_SATA_B_R2D_CP	TRUE, MAKE_BASE=TRUE	NC_SATA_B_R2D_CP
16	TP_SATA_D_D2RN	TRUE, MAKE_BASE=TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	TRUE, MAKE_BASE=TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	TRUE, MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	TRUE, MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	TRUE, MAKE_BASE=TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	TRUE, MAKE_BASE=TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	TRUE, MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	TRUE, MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	TRUE, MAKE_BASE=TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	TRUE, MAKE_BASE=TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	TRUE, MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	TRUE, MAKE_BASE=TRUE	NC_SATA_F_R2D_CP

	TP_PCH_TP18	TRUE, MAKE_BASE=TRUE	NC_PCH_TP18
	TP_PCH_TP17	TRUE, MAKE_BASE=TRUE	NC_PCH_TP17
	TP_PCH_TP16	TRUE, MAKE_BASE=TRUE	NC_PCH_TP16
	TP_PCH_TP15	TRUE, MAKE_BASE=TRUE	NC_PCH_TP15
	TP_PCH_TP14	TRUE, MAKE_BASE=TRUE	NC_PCH_TP14
	TP_PCH_TP13	TRUE, MAKE_BASE=TRUE	NC_PCH_TP13
	TP_PCH_TP12	TRUE, MAKE_BASE=TRUE	NC_PCH_TP12
	TP_PCH_TP10	TRUE, MAKE_BASE=TRUE	NC_PCH_TP10
	TP_PCH_TP9	TRUE, MAKE_BASE=TRUE	NC_PCH_TP9
	TP_PCH_TP8	TRUE, MAKE_BASE=TRUE	NC_PCH_TP8
	TP_PCH_TP7	TRUE, MAKE_BASE=TRUE	NC_PCH_TP7
	TP_PCH_TP6	TRUE, MAKE_BASE=TRUE	NC_PCH_TP6
	TP_PCH_TP5	TRUE, MAKE_BASE=TRUE	NC_PCH_TP5
	TP_PCH_TP4	TRUE, MAKE_BASE=TRUE	NC_PCH_TP4
	TP_PCH_TP3	TRUE, MAKE_BASE=TRUE	NC_PCH_TP3
	TP_PCH_TP2	TRUE, MAKE_BASE=TRUE	NC_PCH_TP2
	TP_PCH_TP1	TRUE, MAKE_BASE=TRUE	NC_PCH_TP1

E58	PCH_VSS_NCTF<1>	TRUE	69
E59	PCH_VSS_NCTF<2>	TRUE	69
E60	PCH_VSS_NCTF<5>	TRUE	69
E57	PCH_VSS_NCTF<9>	TRUE	69
E73	PCH_VSS_NCTF<11>	TRUE	69
E56	PCH_VSS_NCTF<12>	TRUE	69
E55	PCH_VSS_NCTF<15>	TRUE	69
E49	PCH_VSS_NCTF<17>	TRUE	69
E54	PCH_VSS_NCTF<19>	TRUE	6 69
E50	PCH_VSS_NCTF<19>	TRUE	6 69
E48	PCH_VSS_NCTF<21>	TRUE	69
E44	PCH_VSS_NCTF<25>	TRUE	69
E46	PCH_VSS_NCTF<27>	TRUE	69
E45	PCH_VSS_NCTF<29>	TRUE	69

8	TP_LVDS_IG_B_CLKN	TRUE, MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	TRUE, MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	TRUE, MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	TRUE, MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

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"G3Hot" (Always-Present) Rails

52 =PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_G0_LCDBKLT 65
=PPBUS_G0_VSENSE 44
=PPVIN_SW_T29BST 8 35
=PPVIN_S5_HS_COMPUTING_ISNS_R 45
=PPVIN_S5_P5VP3V3 54

35 6 PPVIN_SW_T29BST
VOLTAGE=12.6V

45 =PPVIN_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS 6
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP 56 57
=PPVIN_S3_DDRREG 55
=PPVIN_S0_CPUVCCIOS0 58
=PPVIN_S0_VCCSAS0 53
=PPVIN_S0_CPUAXG 57

51 6 =PP18V5_DCIN_CONN
PPDCIN_G3H 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 52
=PPDCIN_S5_VSENSE 44

51 =PP3V42_G3H_REG
PP3V42_G3H 6
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS 6 42
=PP3V3_S5_SMC 40 41
=PP3V42_G3H_HALL 6 51
=PP3V42_G3H_CHGR 52
=PP3V42_G3H_PWRCTL 61
=PP3V42_G3H_SMBUS_SMC_BSA 43
=PP3V42_G3H_SMCUSBMUX 38
=PP3V42_G3H_TPAD 6 48
=PPVIN_S5_SMCVREF 41
=PPVBAT_G3_SYSCLK 25
=PP3V42_G3H_ONEWIRE 6 39

25 =PPVRTC_G3_OUT
PPVRTC_G3H 6
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
=PPVRTC_G3_PCH 16 17 20

5V Rails

54 =PP5V_S5_LDO
PP5V_S5 6
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S5_P1V5DDRFET 60
=PP5V_S5_P5VSUSFET 60
=PP5V_S5_TPAD 48

60 =PP5V_SUS_FET
PP5V_SUS 6
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP5V_SUS_PCH 22

54 =PP5V_S3_REG
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_AUDIO_AMP 50
=PP5V_S3_DDRREG 55
=PP5V_S3_MEMRESET 26
=PP5V_S3_P5VS0FET 60
=PP5V_S3_RTUSB 38
=PP5V_S3_LIO_CONN 6 51

60 =PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_BKL 65
=PP5V_S0_CPUIMVP 56
=PP5V_S0_CPUVCCIOS0 58
=PP5V_S0_FAN 6 47
=PP5V_S0_LPCPLUS 6 42
=PP5V_S0_VCCSA 53
=PP5V_S0_PCH 22
=PP5V_S0_VMON 61
=PP5V_S0_KBDLED 48

3.3V Rails

54 =PP3V3_S5_REG
PP3V3_S5 6 73
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S5_XDP 23
=PP3V3_S0_P3V3S0FET 60
=PP3V3_S3_P3V3S3FET 60
=PP3V3_S5_CPU_VCCDDR 26
=PP3V3_S4_SMC 41
=PP3V3_S5_LCD 62
=PP3V3_S5_PCH 17 19
=PP3V3_S5_PCHPWRGD 25
=PP3V3_S5_SMCBATLOW 41
=PP3V3_S5_ROM 49
=PP3V3_S5_USB_RESET 24
=PP3V3_S5_PCH_VCCDSW 20 22
=PP3V3_S5_SYSCLK 25
=PP3V3_S5_VMON 61
=PP3V3_S5_PWRCTL 61
=PP3V3_S5_PCH_VCC_SPI 20 22
=PP3V3_S5_P3V3SUSFET 60
=PP3V3_S5_TPAD 48
=PP3V3_S4_DPAPWRSW 64

60 =PP3V3_SUS_FET
PP3V3_SUS 6
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_SUS_PCH_VCCSUS_USB 20 22
=PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
=PP3V3_SUS_PCH_VCCSUS 20
=PP3V3_SUS_GPIO 16 17 18 19
=PP3V3_SUS_PCH 22
=PP3V3_SUS_PWRCTL 61
=PP3V3_SUS_P1V05SUSLDO 59
=PP3V3_SUS_SMC 41

60 =PP3V3_S3_FET
PP3V3_S3 6
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_S3_BT 6 36
=PP3V3_S3_MEMRESET 26
=PP3V3_S3_SMBUS_SMC_A_S3 43
=PP3V3_S3_SMBUS_SMC_MGMT 43
=PP3V3_S3_USB_HUB 8 24
=PP3V3_S3_USB_RESET 24
=PP3V3_S3_VREFMRGN 31
=PP3V3_S3_WLAN 36
=PP3V3_S3_WLANISNS 45
=PP3V3_S3_BMON_ISNS 45
=PP3V3_S3_PCH_GPIO 18 19
=PP3V3_S3_1V5S3ISNS 45
=PP3V3_S3_DBGLEDS 51

60 =PP3V3_S0_FET
PP3V3_S0 6 73
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_S0_CPUVCCIOISNS 44
=PP3V3_S0_AUDIO 6 39
=PP3V3_S0_BKL_VDDIO 65
=PP3V3_S0_HS_COMPUTING_ISNS 45
=PP3V3_S0_CPUTHMSNS 46
=PP3V3_S0_CPU_VCCIO_SEL 12
=PP3V3_S0_DP_DDC 8
=PP3V3_S0_FAN 47
=PP3V3_S0_P3V3T29FET 35
=PP3V3_S0_P1V8S0 59
=PP3V3_S0_PCH 16 19 22
=PP3V3_S0_PCH_GPIO 18
=PP3V3_S0_PCH_VCC3_3_CLK 22
=PP3V3_S0_PCH_VCC3_3_GPIO 20 22
=PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
=PP3V3_S0_PCH_VCC3_3_PCI 20 22
=PP3V3_S0_PCH_VCC3_3_SATA 20 22
=PP3V3_S0_PCH_VCCADAC 22
=PP3V3_S0_PCH_STRAPS 16 17 19
=PP3V3_S0_PWRCTL 61
=PP3V3_S0_RSTBUF 25
=PP3V3_S0_SB_PM 25
=PP3V3_S0_SMBUS_PCH 43
=PP3V3_S0_SMBUS_SMC_0_S0 43
=PP3V3_S0_SMBUS_SMC_B_S0 43
=PP3V3_S0_SMC 41
=PP3V3_S0_HDD 37
=PP3V3_S0_HDDISNS 45
=PP3V3_S0_VMON 61
=PP3V3_S0_P1V5S0 59
=PP3V3_S0_T29PWRCTL 35
=PP3V3_S0_DPSDRVA 63
=PP3V3_S0_P1V05S0LDO 59
=PP3V3_S0_IMVPISNS 44
=PP3V3_S0_XDP 23
=PP3V3_S0_T29I2C 43
=PP3V3_S0_BKLTISNS 45
=PP3V3_S0_SYSCLKGEN 25

1.8V/1.5V/1.2V/1.05V Rails

59 =PP1V8_S0_REG
2A max supply
PP1V8_S0 6
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S0_CPU_VCCPLL 14
=PP1V8_S0_PCH_VCC_DFTERM 18 20 22
=PP1V8_S0_P1V05S0LDO 59
=PP1V8R1V5_S0_PCH_VCCVRM 20
=PPVDDIO_S0_SBCLK 25
=PP1V8_S0_P1V5S0 59

55 =PPDDR_S3_REG
PP1V5_S3 6 67
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET 26
=PP1V5_S3_MEM_A 27 28 32
=PP1V5_S3_MEM_B 29 30 32
=PP1V5_S3_P1V5S3RS0_FET 60
=PPVIN_S0_DDRREG_LDO 55

60 =PP1V5_S3RS0_FET
PP1V5_S3RS0 6 67
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_CPU_VCCDDR 10 12 15 26
=PP1V5_S3RS0_VMON 61

59 =PP1V5_S0_REG
PP1V5_S0 6
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP3V3R1V5_S0_AUDIO 6 39
=PP3V3R1V5_S0_PCH_VCCSUSHDA 16 20 22

55 31 =PPVTT_S3_DDR_BUF
PPVTTDDR_S3 6
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

55 =PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT 6
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A 32
=PP0V75_S0_MEM_VTT_B 32
=PPVTT_S0_VTTCLAMP 26

53 =PPVCCSA_S0_REG
PPVCCSA_S0_CPU 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCCSA_S0_CPU 12 15

59 =PP1V05_SUS_LDO
PP1V05_SUS 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG 23

58 =PPCPUVCCIO_S0_REG
? mA
PP1V05_S0 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCIO_PLLPCIE 20
=PP1V05_S0_CPU_VCCIO 9 10 12 14
=PP1V05_S0_PCH 16 22
=PP1V05_S0_PCH_VCCIO 20 22
=PP1V05_S0_PCH_VCCIO_PCIE 17
=PP1V05_S0_PCH_VCCIO_SATA 16 20 22
=PP1V05_S0_PCH_VCCASW 20 22
=PP1V05_S0_PCH_VCCIO_USB 20 22
=PP1V05_S0_PCH_VCC_CORE 20 22
=PP1V05_S0_VMON 61
=PP1V05_S0_PCH_VCCIO_CLK 20 22
=PPVCCIO_S0_CPUIMVP 56
=PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
=PP1V05_S0_PCH_VCCSSC 20 22
=PP1V05_S0_PCH_V_PROC_IO 20 22
=PP1V05_S0_PCH_VCCIO_PLLUSB 20
=PP1V05_S0_PCH_VCC_DMI 20 22
=PP1V05_S0_PCH_VCCIO_PLLFDI 20
=PP1V05_S0_PCH_VCCDMI_FDI 20
=PPVCCIO_S0_XDP 23
=PPVCCIO_S0_SMC 40
=PP1V05_S0_P1V05T29FET 35

T29 Rails (off when no cable)

35 8 =PP15V_T29_REG
PP15V_T29 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.0V
MAKE_BASE=TRUE
=PPHV_SW_DPAPWRSW 64

35 =PP3V3_T29_FET
PP3V3_T29 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PPVDDIO_T29_CLK 25
=PP3V3_T29_RTR 33 34 35
=PP3V3_T29_PCH_GPIO 16 19

35 =PP1V05_T29_FET
PP1V05_T29 6 35
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_T29_RTR 34

1V05 S0 LDO

59 =PP1V05_S0_LDO
PP1V05_S0_PCH_VCCADPLL 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCADPLL 20

Chipset "VCore" Rails

57 =PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 9 12 14
=PPCPUVCORE_S0_VSENSE 44

57 =PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU_VCCAXG 9 12 15
=PPGFXVCORE_S0_VSENSE 44

15 12 =PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

14 12 =PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE
Power Aliases
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DRAWING NUMBER 051-8871
SIZE D
REVISION 2.5.0
BRANCH
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CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905 STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914 STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915 STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.00D-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.00D-3.6H-K86-K87
SM
870-1938

CRITICAL
ZS0904
POGO-2.00D-2.95H-K86-K87
SM
870-1940

CRITICAL
ZS0907
1.4DIA-SHORT-SILVER-K99
SM
870-2015

T29 Can Slots

SL0901 TH-NSP SL-1.1X0.4-1.4x0.7 998-2691
SL0902 TH-NSP SL-1.1X0.4-1.4x0.7 998-2691

DisplayPort PCB Stiffener

(Provides PCB support for small finger above J9400)

NO STUFF
MT0900
STIFFENER-K16-K99
SM-SP
806-1176

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

CPU signals

MEMVTT_EN — MAKE_BASE=TRUE — =DDRVTT_EN

DP_EXTA_ML_C_P<3..0>	DP_IG_ML_P<3..0>	TP_DP_IG_B_MLP<3..0>
DP_EXTA_ML_C_N<3..0>	DP_IG_ML_N<3..0>	TP_DP_IG_B_MLN<3..0>
DP_EXTA_AUXCH_C_P	DP_IG_AUX_CH_P	DP_IG_B_AUX_P
DP_EXTA_AUXCH_C_N	DP_IG_AUX_CH_N	DP_IG_B_AUX_N

PCIE_EXCARD_D2R_N	TRUE	NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P	TRUE	NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N	TRUE	NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P	TRUE	NC_PCIE_EXCARD_R2D_CP
PCIE_CLK100M_EXCARD_N	TRUE	NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P	TRUE	NC_PCIE_CLK100M_EXCARDP

PEG_CLK100M_P		NC_PEG_CLK100MP
PEG_CLK100M_N		NC_PEG_CLK100MN
TP_PCH_CLKOUT_DPN	DPLL_REF_CLK_N	DPLL_REF_CLKN
TP_PCH_CLKOUT_DPP	DPLL_REF_CLK_P	DPLL_REF_CLKP

MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1>
MEM_A_CLK_N<1>	TP_MEM_A_CLKN<1>
MEM_A_CKE<1>	NC_MEM_A_CKE<1>
MEM_A_CS_L<1>	NC_MEM_A_CS_L<1>
MEM_A_ODT<1>	NC_MEM_A_ODT<1>
MEM_B_CLK_P<1>	TP_MEM_B_CLKP<1>
MEM_B_CLK_N<1>	TP_MEM_B_CLKN<1>
MEM_B_CKE<1>	NC_MEM_B_CKE<1>
MEM_B_CS_L<1>	NC_MEM_B_CS_L<1>
MEM_B_ODT<1>	NC_MEM_B_ODT<1>
MEM_A_A<15>	TP_MEM_A_A<15>
MEM_B_A<15>	TP_MEM_B_A<15>

T29BST:N
R0960 0 5% 1/8W MF-LF 805
=PPVIN_SW_T29BST — =PP15V_T29_REG

T29_A_BIAS — C0960 0.01UF 10% 10V X5R 201

T29_A_BIAS caps

T29_A_BIAS_R	R0931 51 5% 1/20W MF 201	T29_A_BIAS_R2DP0 — C0901 0.01UF 10% 10V X5R 201
T29_A_BIAS_R	R0932 51 5% 1/20W MF 201	T29_A_BIAS_R2DN0 — C0902 0.01UF 10% 10V X5R 201
T29_A_BIAS_R	R0933 51 5% 1/20W MF 201	T29_A_BIAS_R2DP1 — C0903 0.01UF 10% 10V X5R 201
T29_A_BIAS_R	R0934 51 5% 1/20W MF 201	T29_A_BIAS_R2DN1 — C0904 0.01UF 10% 10V X5R 201

SIGNAL_MODEL=EMPTY

T29 DP Ports

=PEG_R2D_C_P<3..0>	PEG_R2D_C_P<3..0>	PCIE_T29_R2D_C_P<3..0>
=PEG_R2D_C_N<3..0>	PEG_R2D_C_N<3..0>	PCIE_T29_R2D_C_N<3..0>
=PEG_D2R_P<3..0>	PEG_D2R_P<3..0>	PCIE_T29_D2R_P<3..0>
=PEG_D2R_N<3..0>	PEG_D2R_N<3..0>	PCIE_T29_D2R_N<3..0>

=PP3V3_S0_DP_DDC
R0920 2.2K 5% 1/20W MF 201
R0921 2.2K 5% 1/20W MF 201
R0922 2.2K 5% 1/20W MF 201
R0923 2.2K 5% 1/20W MF 201

TP_DP_IG_C_CTRL_CLK		DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA		DP_IG_C_CTRL_DATA
TP_DP_IG_D_CTRL_CLK		DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA		DP_IG_D_CTRL_DATA

TP_DP_IG_C_HPD		DP_T29SNK0_HPD
TP_DP_IG_C_MLP<3..0>		DP_T29SNK0_ML_C_P<3..0>
TP_DP_IG_C_MLN<3..0>		DP_T29SNK0_ML_C_N<3..0>
TP_DP_IG_C_AUXP		DP_T29SNK0_AUXCH_C_P
TP_DP_IG_C_AUXN		DP_T29SNK0_AUXCH_C_N
TP_DP_IG_D_HPD		DP_IG_D_HPD

R0909 100K 5% 1/20W MF 201

=PP3V3_S0_DP_DDC
R0924 2.2K 5% 1/20W MF 201
R0925 2.2K 5% 1/20W MF 201

DP_EXTA_DDC_CLK		DP_IG_B_DDC_CLK
DP_EXTA_DDC_DATA		DP_IG_B_DDC_DATA
DP_EXTA_HPD		DP_IG_B_HPD

R0908 100K 5% 1/20W MF 201
CRITICAL
R0910 0.01 0.5% 1W MF 0612-1

PPBUS_SW_LCDBKLT_PWR — R0911 0 — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
ISNS_LCDBKLT_P (OUT)
ISNS_LCDBKLT_N (OUT) — =PPBUS_SW_BKL

NC_USB_HUB1_OCS4	=USB_HUB1_OCS4
NC_USB_HUB2_OCS4	=USB_HUB2_OCS4

T29_A_BIAS caps

T29_A_BIAS_R — R0926 51 — T29_A_BIAS_D2RP1 — C0906 0.01UF 10% 10V X5R 201
T29_A_BIAS_R — R0927 51 — T29_A_BIAS_D2RN1 — C0907 0.01UF 10% 10V X5R 201

DP_A_BIAS caps

C0962 0.01UF 10% 10V X5R 201 — DP_A_BIAS_P_2
C0964 0.01UF 10% 10V X5R 201 — DP_A_BIAS_P_0
C0905 0.01UF 10% 10V X5R 201 — DP_A_BIAS_N_2
C0908 0.01UF 10% 10V X5R 201 — DP_A_BIAS_N_0

T29 Aliases

Unused USB ports

=PP3V3_S3_USB_HUB
R0915 10K 5% 1/20W MF 201
R0916 10K 5% 1/20W MF 201
NO STUFF
R0917 0 1/20W MF 201 — T29_A_RSVD_N — USB_T29A_N
R0918 0 1/20W MF 201 — T29_A_RSVD_P — USB_T29A_P
NO STUFF

LVDS Aliases

TP_LVDS_IG_B_CLKP		LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN		LVDS_IG_B_CLK_N
NC_LVDS_IG_B_DATAP<0..3>		LVDS_IG_B_DATA_P<0..3>
NC_LVDS_IG_B_DATAN<0..3>		LVDS_IG_B_DATA_N<0..3>
NC_LVDS_IG_A_DATAP<3>		LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3>		LVDS_IG_A_DATA_N<3>
LCD_BKLT_PWM		LVDS_IG_BKL_PWM
LCD_IG_PWR_EN		LVDS_IG_PANEL_PWR
LCD_BKLT_EN		LVDS_IG_BKL_ON

SATA Aliases

Unused SATA ODD Signals

SATA_ODD_R2D_C_P (IN)		NC_SATA_ODD_R2DCP
SATA_ODD_R2D_C_N (IN)		NC_SATA_ODD_R2DCN
SATA_ODD_D2R_P (OUT)		NC_SATA_ODD_D2RP
SATA_ODD_D2R_N (OUT)		NC_SATA_ODD_D2RN

UNUSED SDCARD USB Aliases

=PP3V3_S3_USB_HUB
R0901 10K 5% 1/20W MF 201
R0902 10K 5% 1/20W MF 201
USB_SDCARD_N (OUT)
USB_SDCARD_P (OUT)

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE		P1V5S3RS0_RAMP_DONE (IN)
TP_DDRREG_PGOOD		DDRREG_PGOOD (IN)

T29 JTAG

R0990 0 5% 1/20W MF 201

JTAG_ISP_TCK (IN)	JTAG_T29_TCK_R	JTAG_T29_TCK (OUT)
JTAG_ISP_TDI (IN)	JTAG_T29_TDI	JTAG_T29_TDI (OUT)
JTAG_ISP_TDO (OUT)	JTAG_T29_TDO	JTAG_T29_TDO (IN)

SYNC_MASTER=K91_MLB — SYNC_DATE=05/15/2010
PAGE TITLE: Signal Aliases

Apple Inc.

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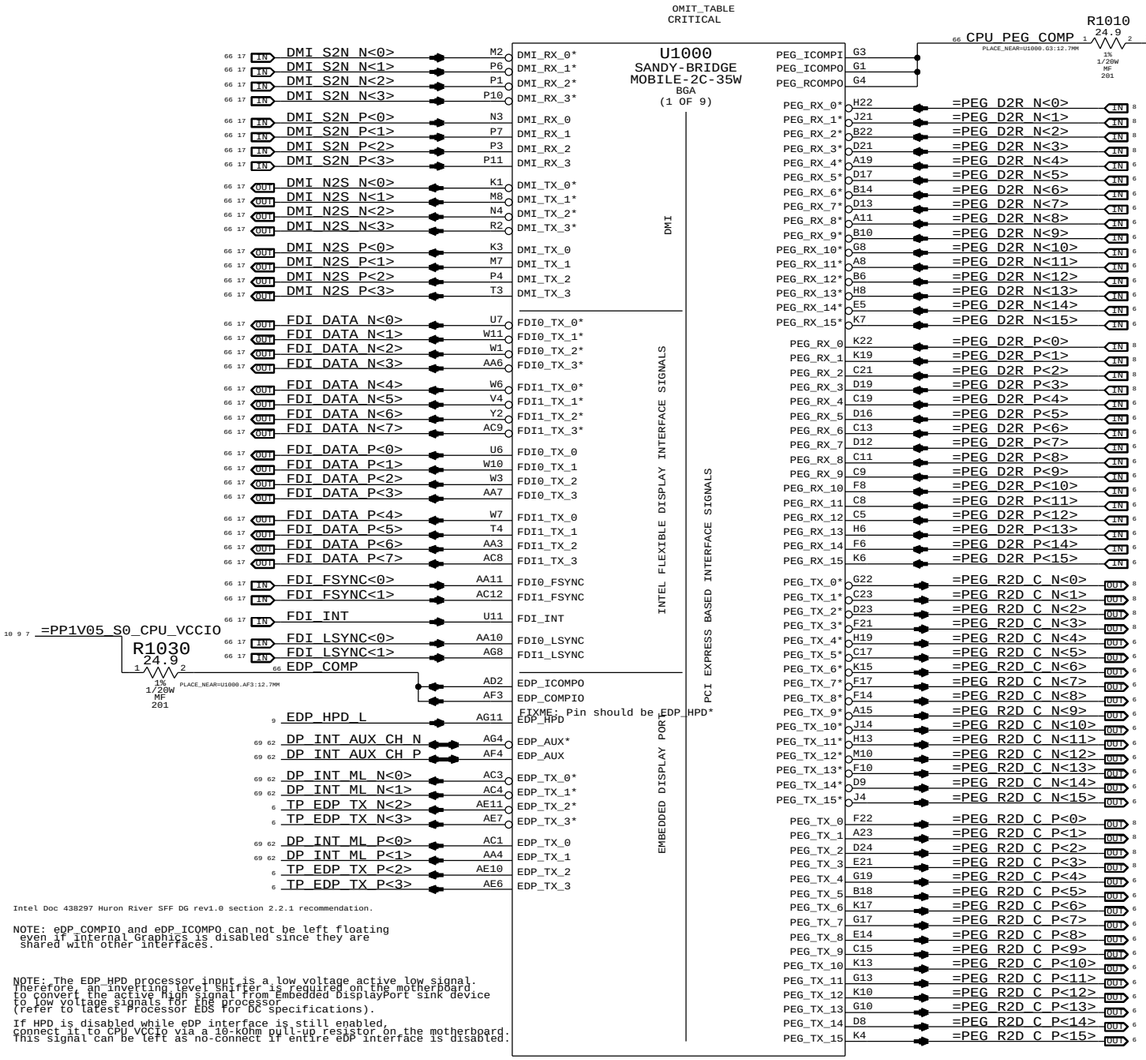
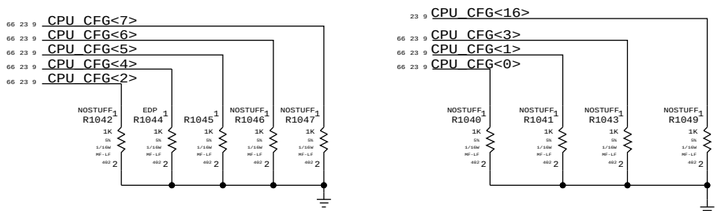
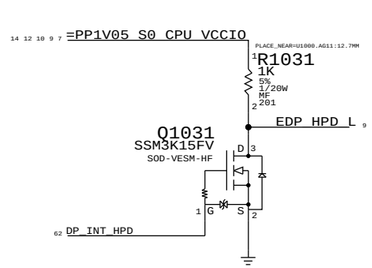


NOTE: Intel is investigating future processor VREF_DQ generation to replace M1 and M2.
This would require routing processor signal balls BE7 and BG7 for Sandy Bridge 2-core
to SO-DIMM connectors directly. FETs are needed in order to avoid potential leakage while system is in S3 state.



These can be Placed close to J2500 and Only for debug access



FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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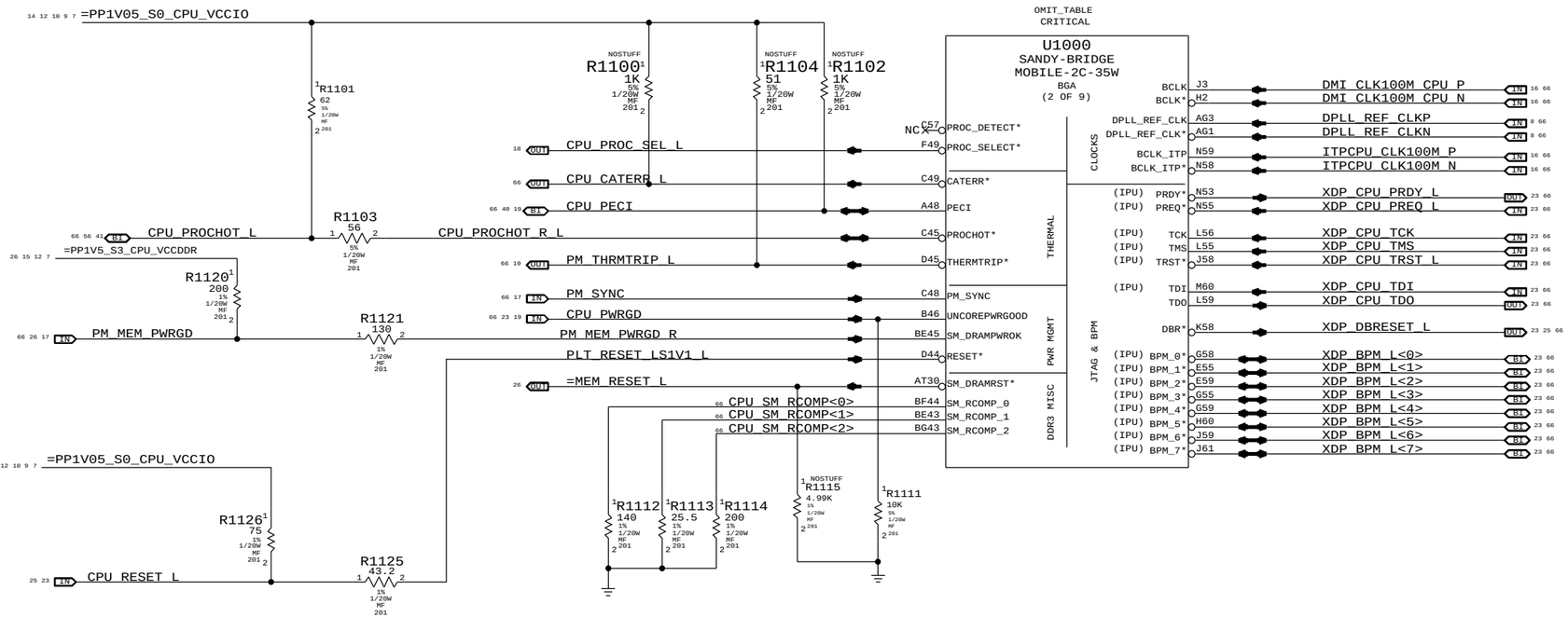

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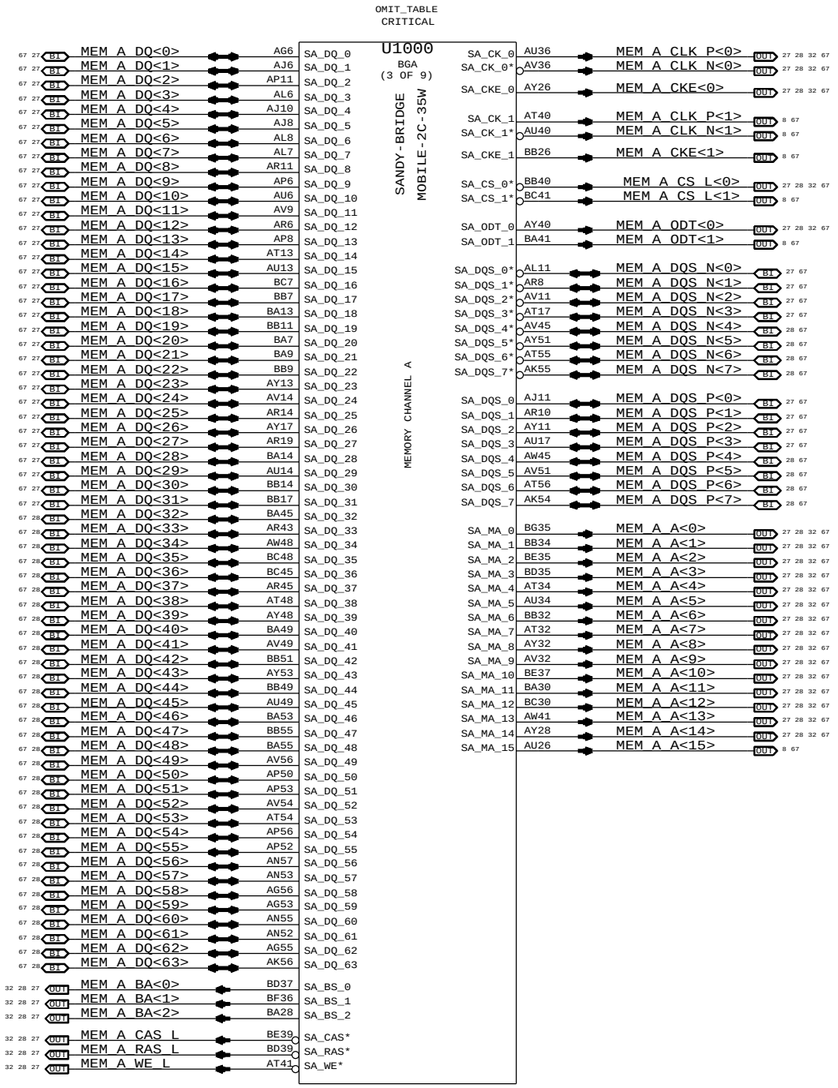

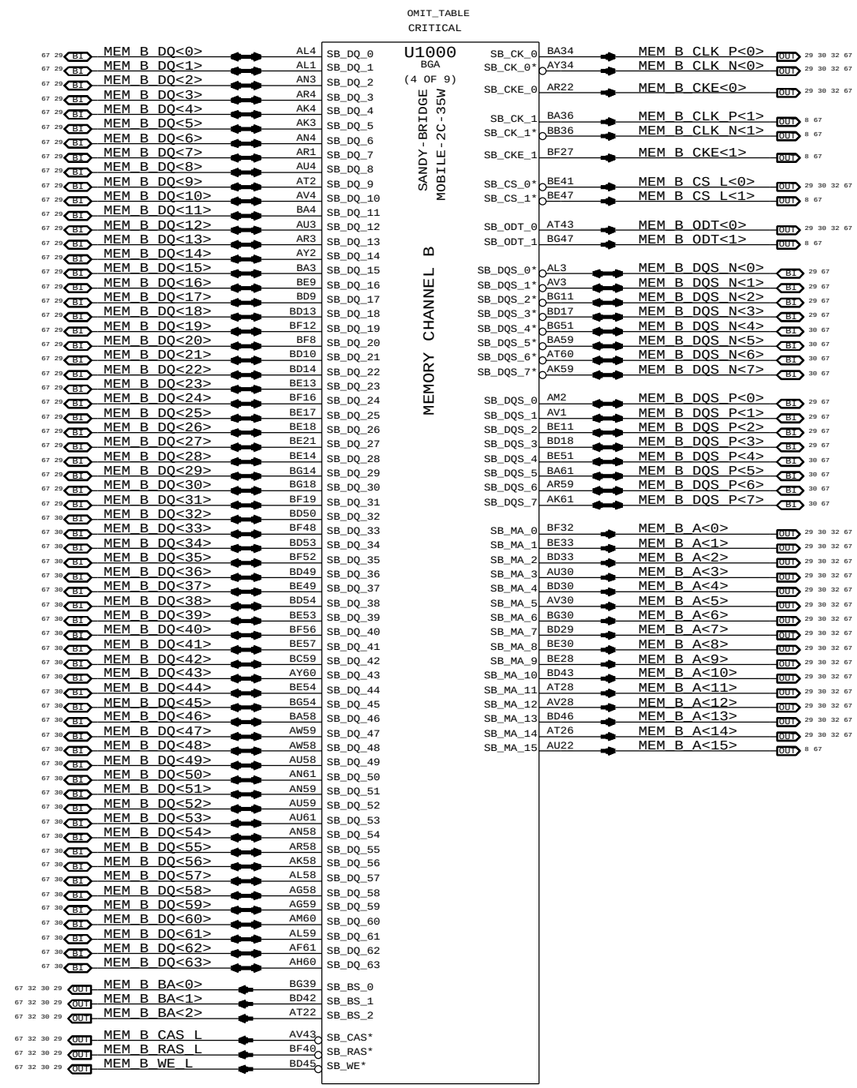

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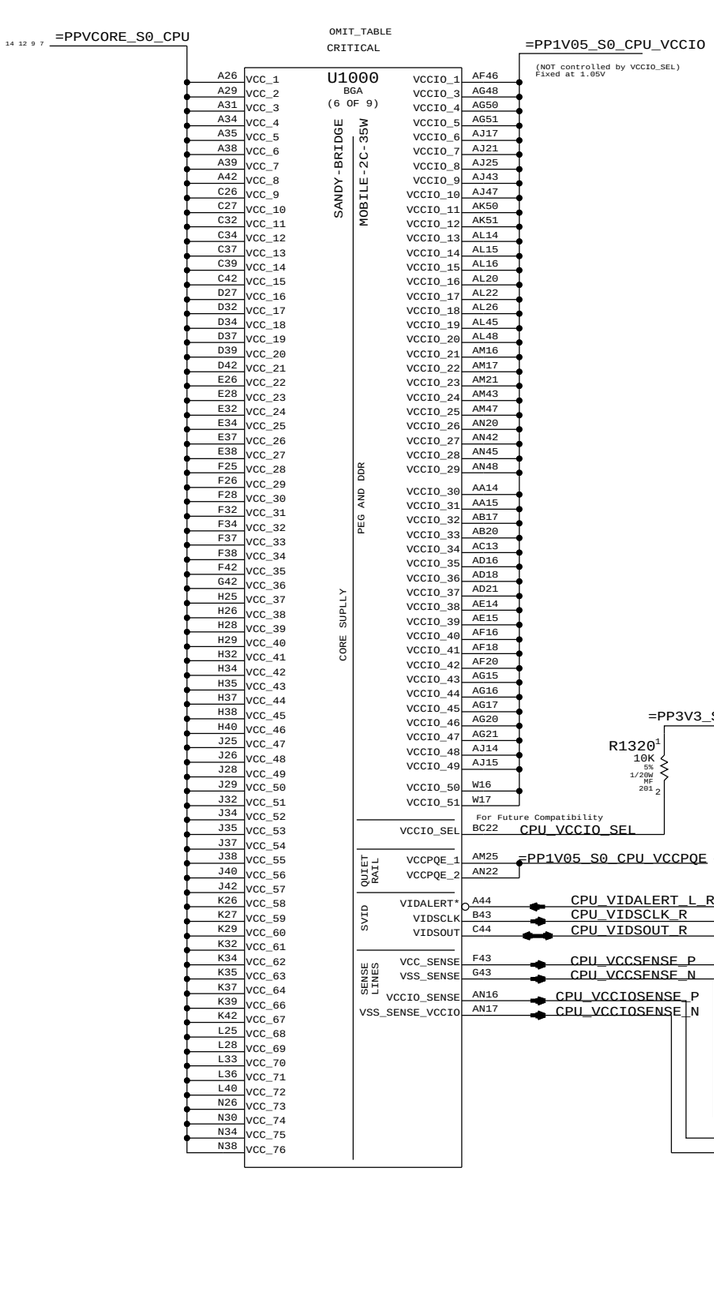

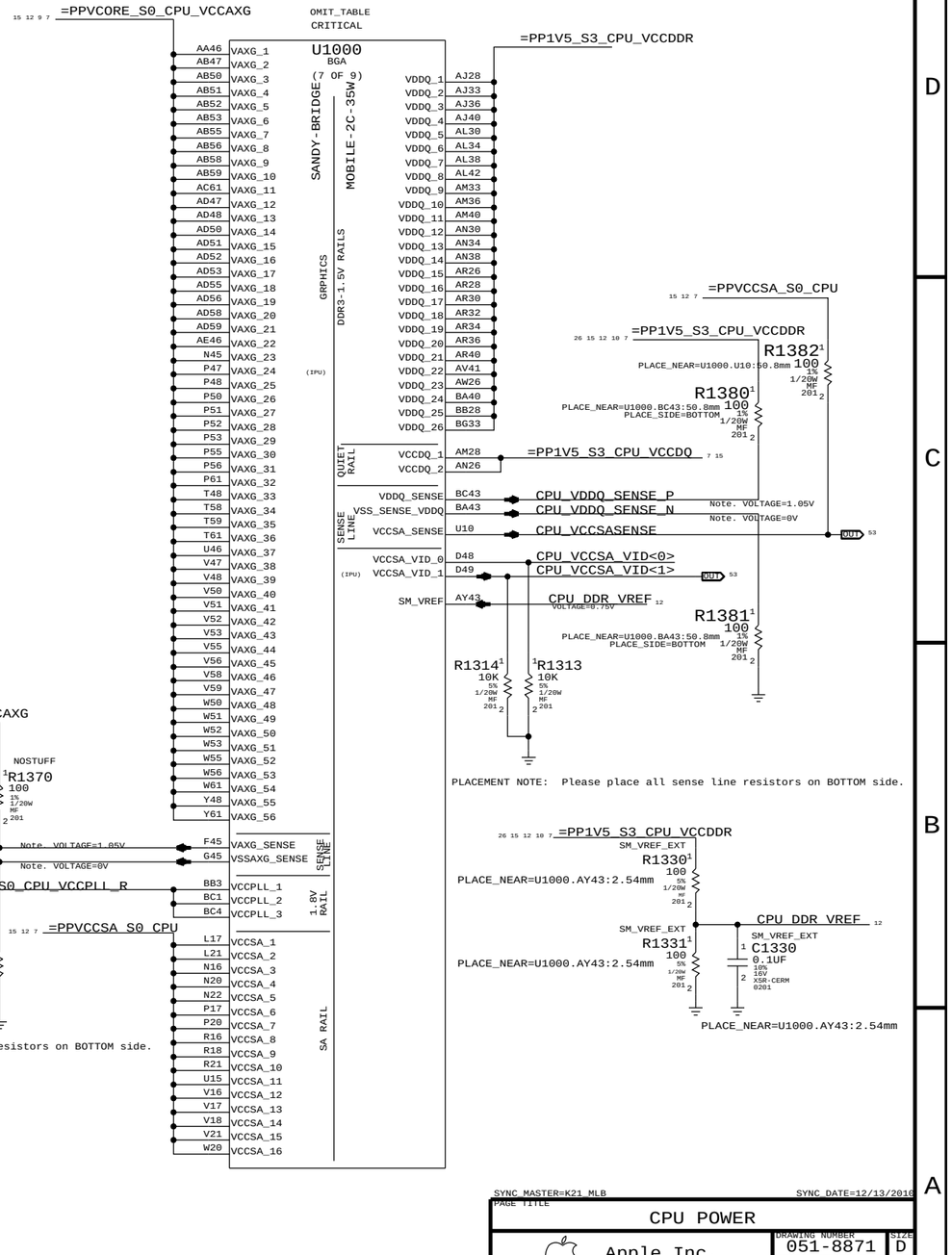

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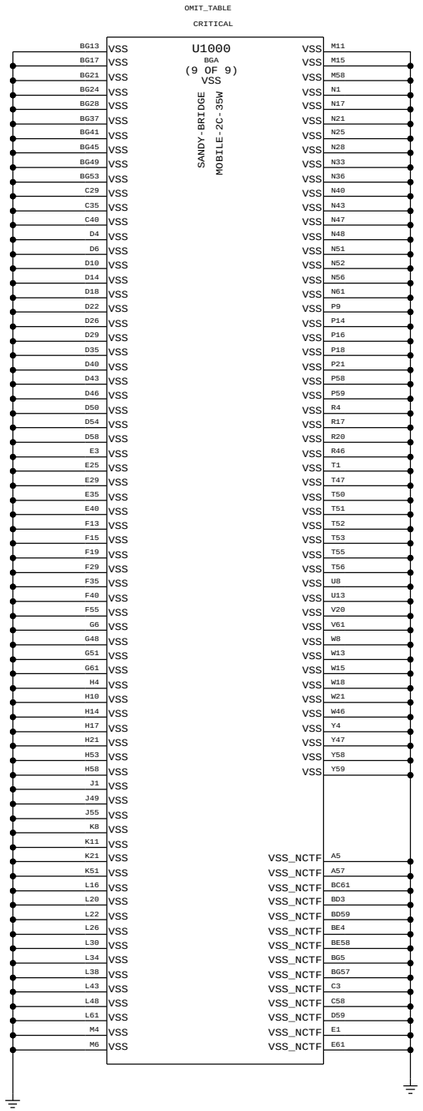

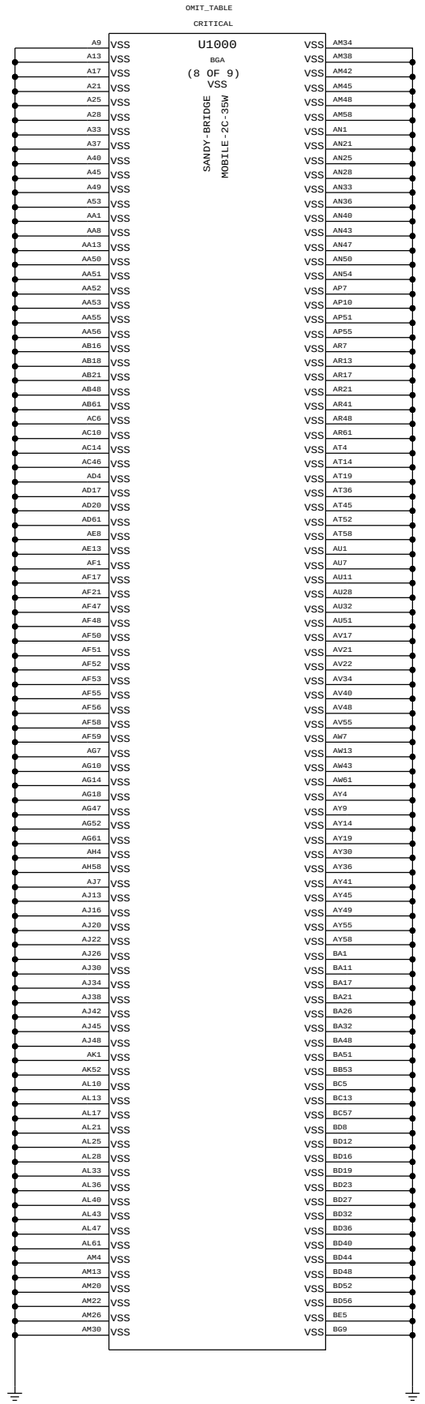

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Processor Load Line : -2.9 mOhms

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 4V X5R 402
CRITICAL C1601 2.2UF 20% 4V X5R 402
CRITICAL C1602 2.2UF 20% 4V X5R 402
CRITICAL C1603 2.2UF 20% 4V X5R 402
CRITICAL C1604 2.2UF 20% 4V X5R 402
CRITICAL C1605 2.2UF 20% 4V X5R 402
CRITICAL C1606 2.2UF 20% 4V X5R 402
CRITICAL C1607 2.2UF 20% 4V X5R 402
CRITICAL C1608 2.2UF 20% 4V X5R 402
CRITICAL C1609 2.2UF 20% 4V X5R 402
CRITICAL C1610 2.2UF 20% 4V X5R 402
CRITICAL C1611 2.2UF 20% 4V X5R 402
CRITICAL C1612 2.2UF 20% 4V X5R 402
CRITICAL C1613 2.2UF 20% 4V X5R 402
CRITICAL C1614 2.2UF 20% 4V X5R 402
CRITICAL C1615 2.2UF 20% 4V X5R 402

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1655 22UF 20% 4V X5R 402
CRITICAL C1656 22UF 20% 4V X5R 402
CRITICAL C1657 22UF 20% 4V X5R 402
CRITICAL C1658 22UF 20% 4V X5R 402
CRITICAL C1659 22UF 20% 4V X5R 402
CRITICAL C1660 22UF 20% 4V X5R 402
CRITICAL C1661 22UF 20% 4V X5R 402
CRITICAL C1662 22UF 20% 4V X5R 402
CRITICAL C1663 22UF 20% 4V X5R 402
CRITICAL C1664 22UF 20% 4V X5R 402
CRITICAL C1665 22UF 20% 4V X5R 402
CRITICAL C1666 22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 270UF 20% 2V TANT CASE-B2-SM
C1681 270UF 20% 2V TANT CASE-B2-SM
C1682 270UF 20% 2V TANT CASE-B2-SM
C1683 270UF 20% 2V TANT CASE-B2-SM
C1679 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

12 10 9 7 =PP1V05_S0_CPU_VCCIO

Place on bottom side of U1000

C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402
C1687 1UF 10% 10V X5R 402
C1688 1UF 10% 10V X5R 402
C1689 1UF 10% 10V X5R 402
C1690 1UF 10% 10V X5R 402
C1691 1UF 10% 10V X5R 402
C1692 1UF 10% 10V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1695 1UF 10% 10V X5R 402
C1696 1UF 10% 10V X5R 402

C1697 1UF 10% 10V X5R 402
C1698 1UF 10% 10V X5R 402
C1699 1UF 10% 10V X5R 402
C169A 1UF 10% 10V X5R 402
C169B 1UF 10% 10V X5R 402
C169C 1UF 10% 10V X5R 402
C169D 1UF 10% 10V X5R 402
C169E 1UF 10% 10V X5R 402
C169F 1UF 10% 10V X5R 402
C161A 1UF 10% 10V X5R 402
C161B 1UF 10% 10V X5R 402
C161C 1UF 10% 10V X5R 402
C161D 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C167G 270UF 20% 2V TANT CASE-B2-SM
C167H 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 7 12
C167F 1UF 10% 10V X5R 402 Note:The smallest 10mOhm available in the library are the 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF-LF 402
=PP1V8_S0_CPU_VCCPLL_R 7 12
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

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VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1718 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1719 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1720 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1721 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1722 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1723-C1724):

C1723 270UF 20% 2V TANT CASE-B2-SM
C1724 270UF 20% 2V TANT CASE-B2-SM
C1725 270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 270UF 20% 2V TANT CASE-B2-SM

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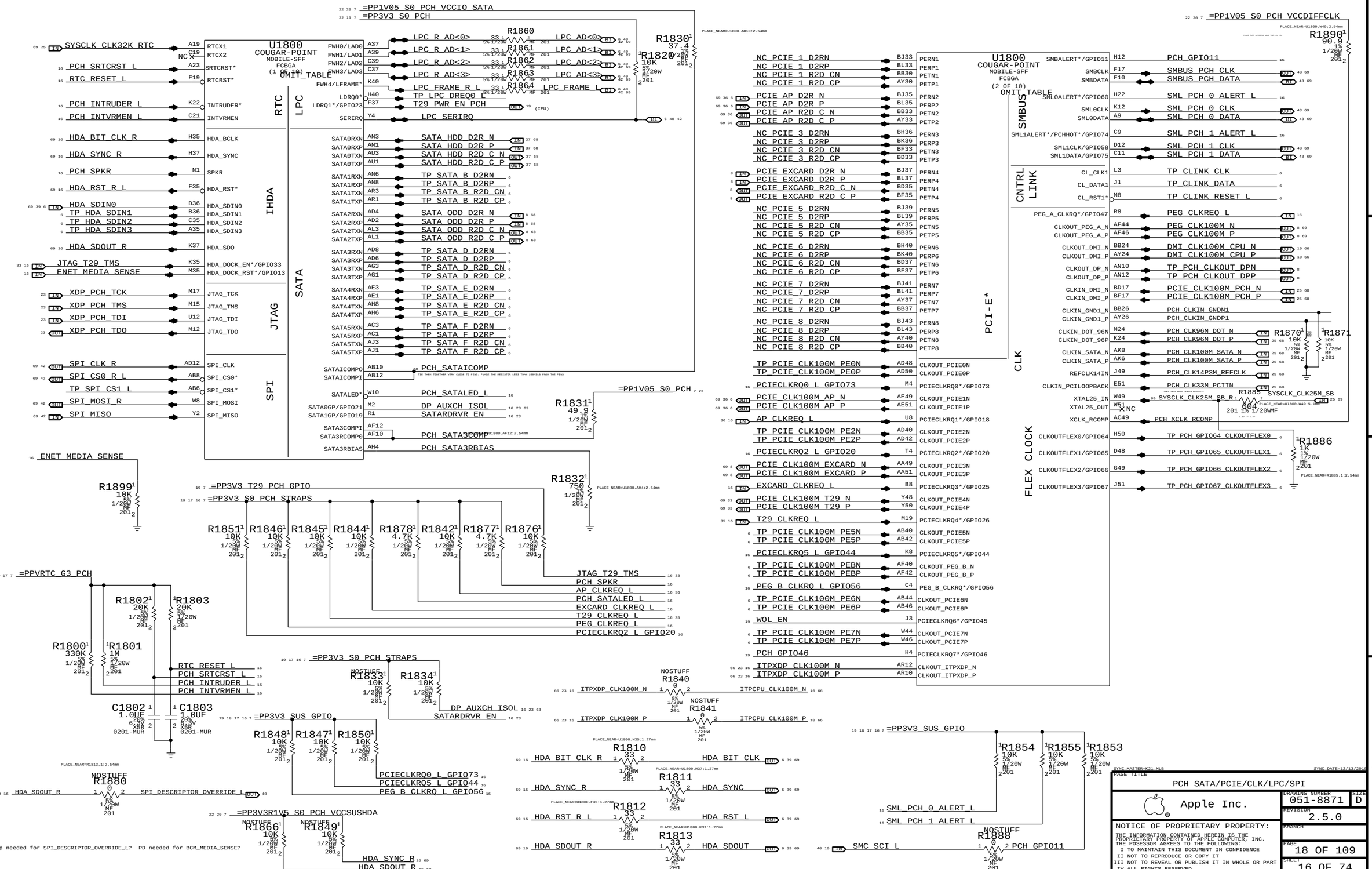

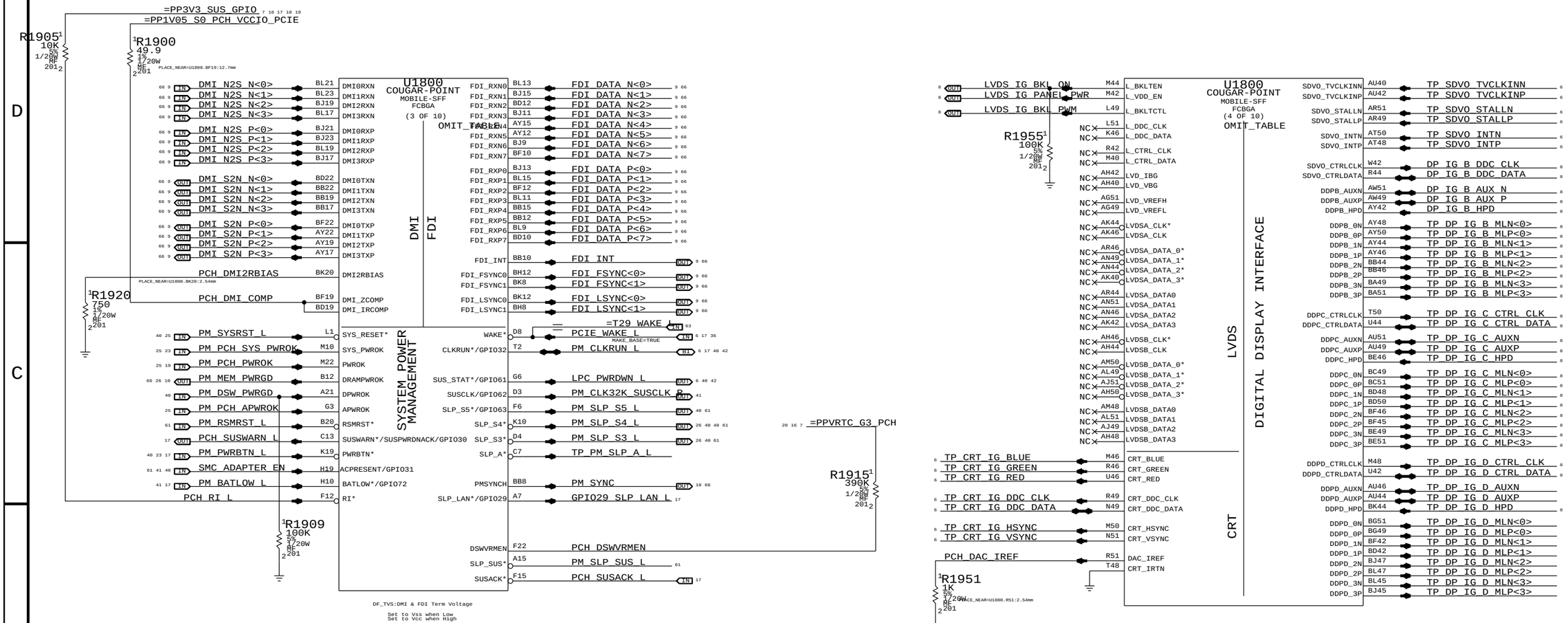

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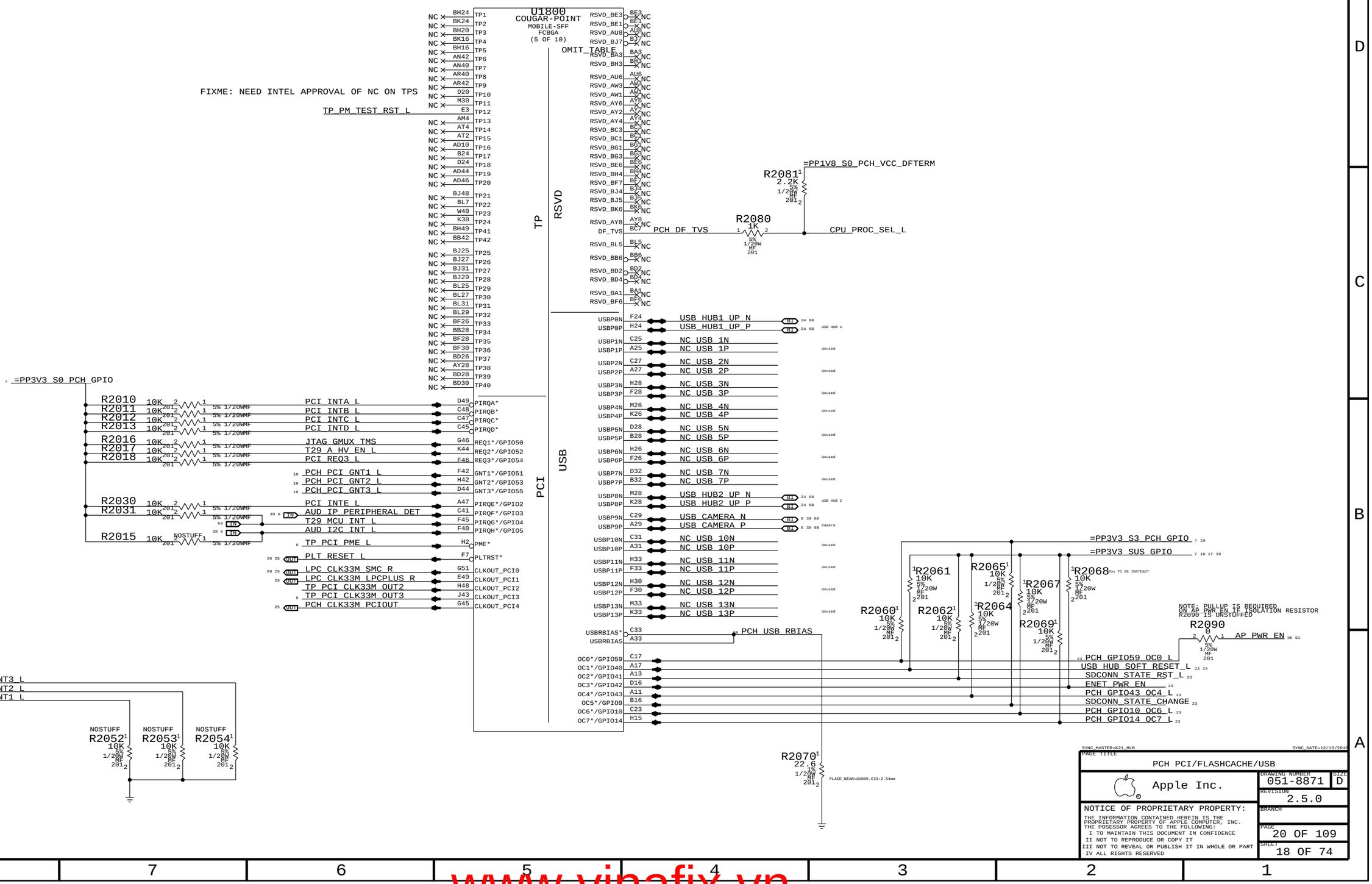

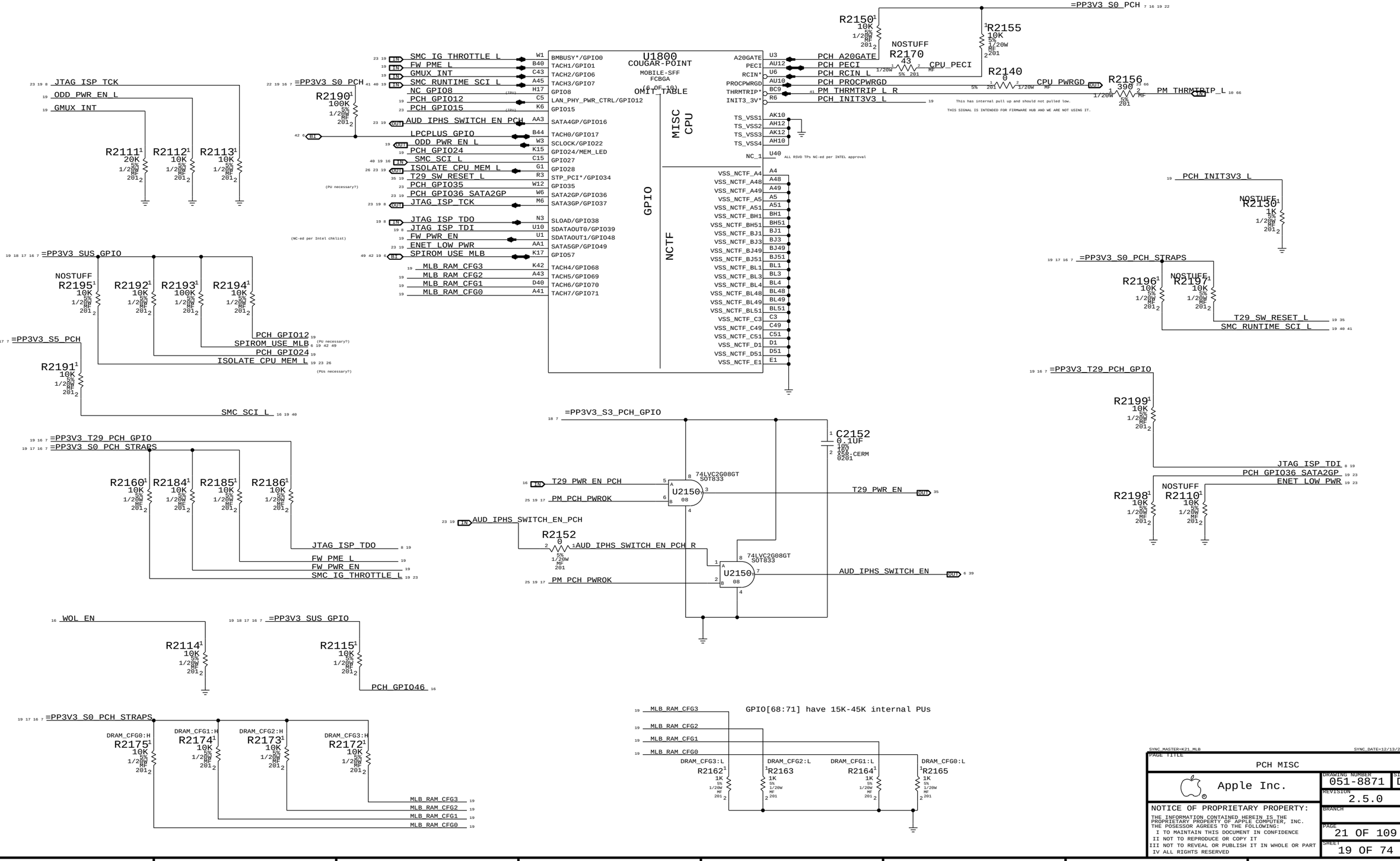

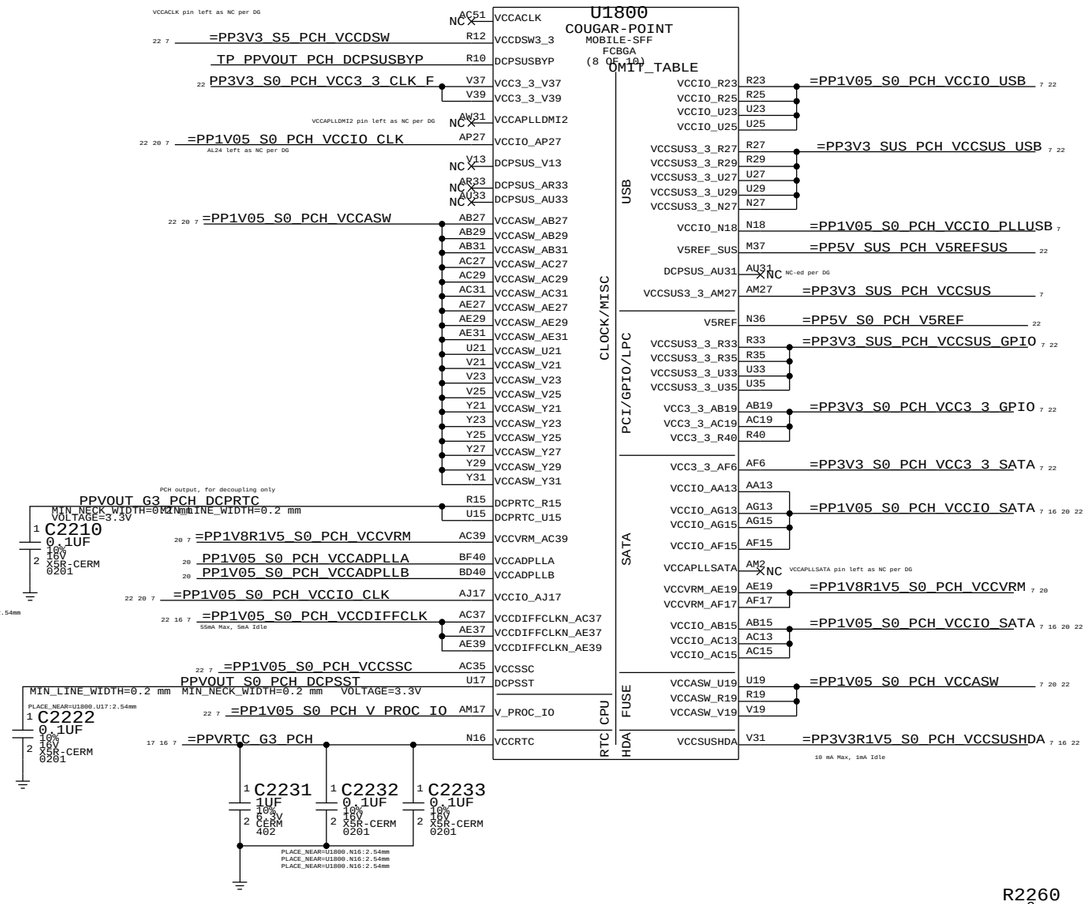

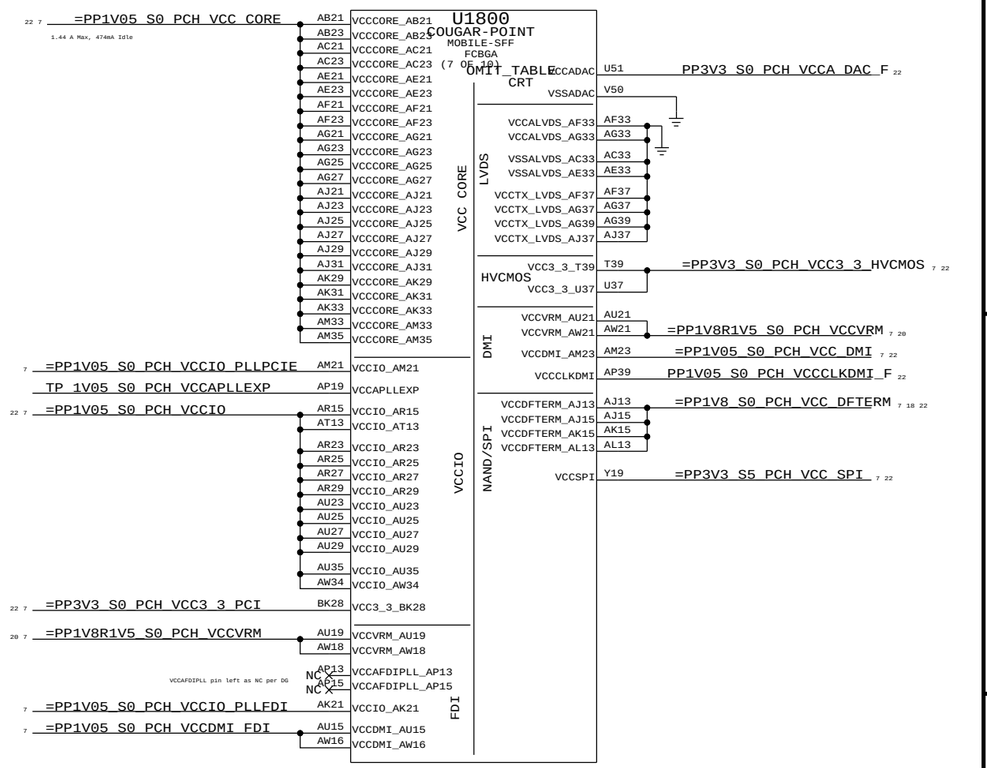

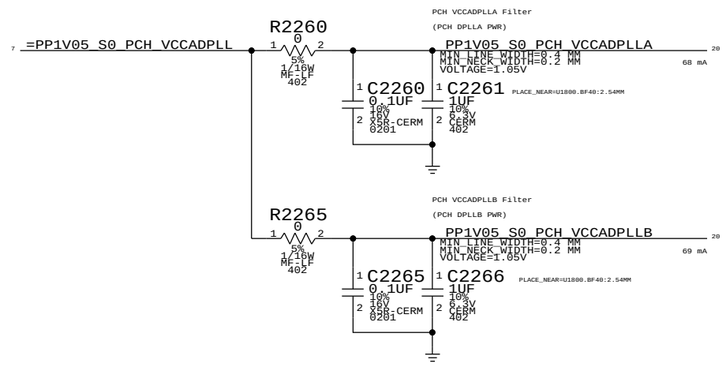

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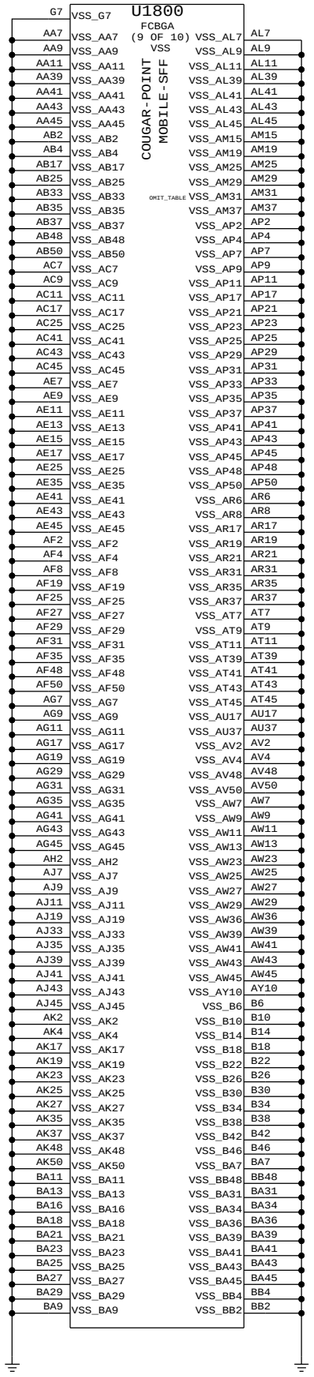

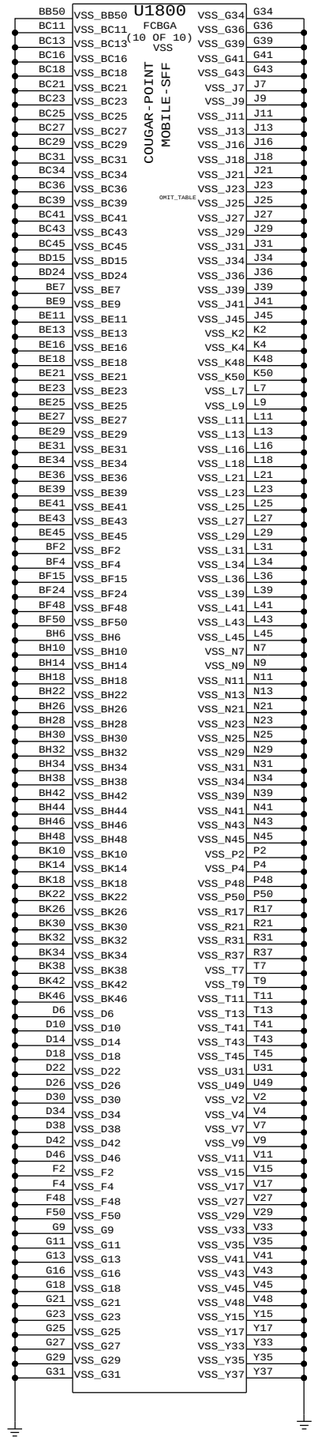

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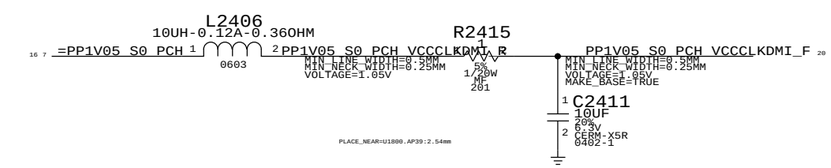

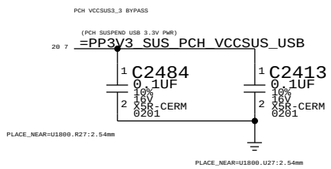

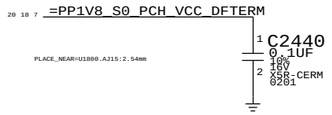

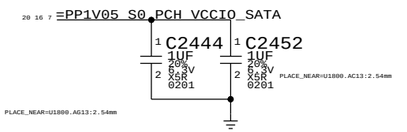

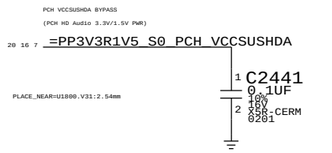

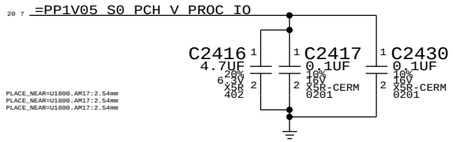

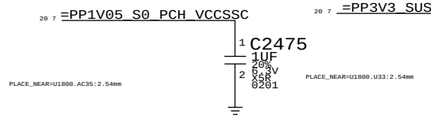

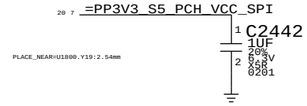

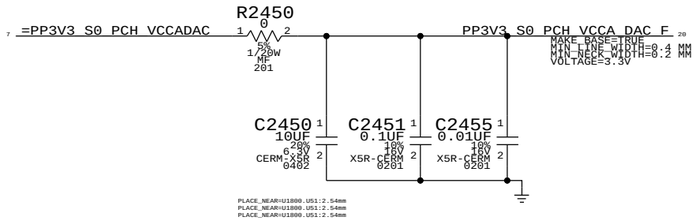

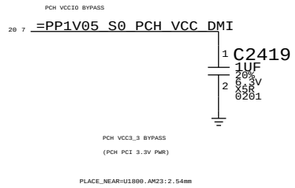

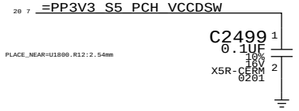

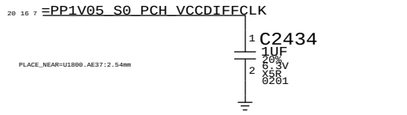

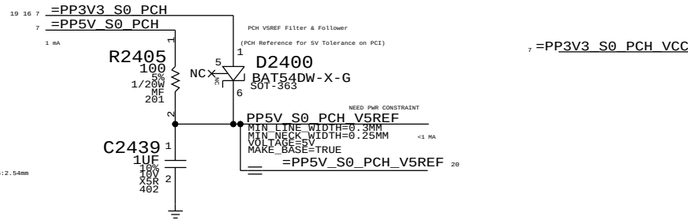

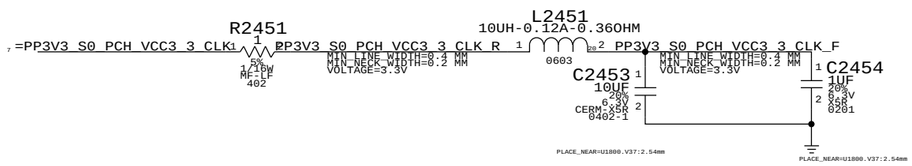

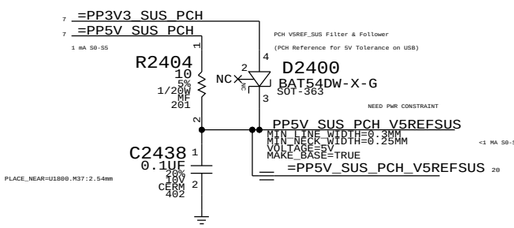

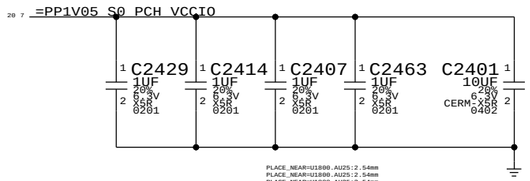

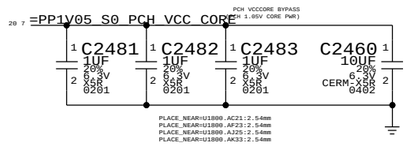

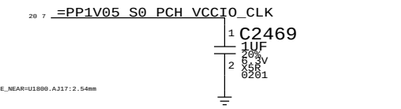

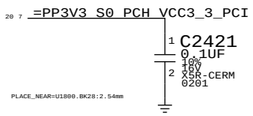

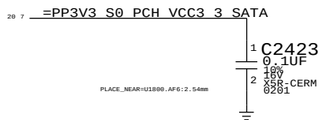

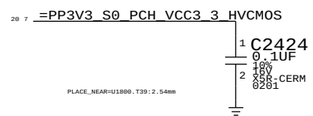

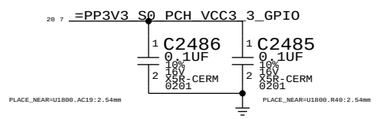

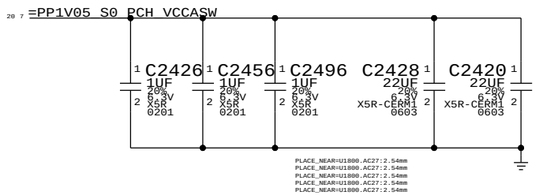

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: PCH DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
REVISION: 2.5.0
BRANCH:
PAGE: 24 OF 109
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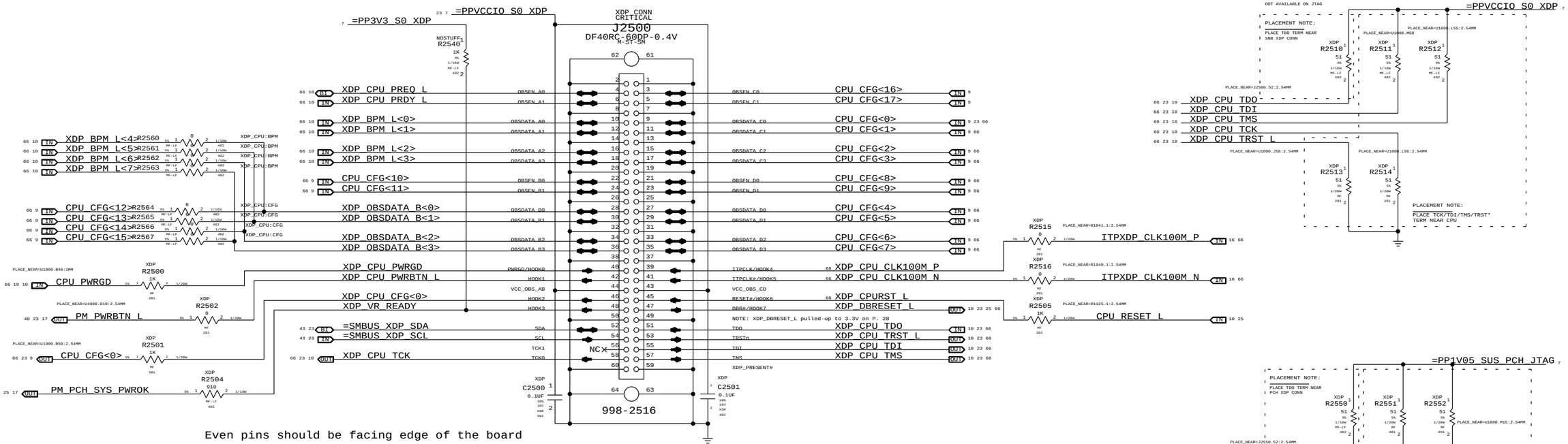
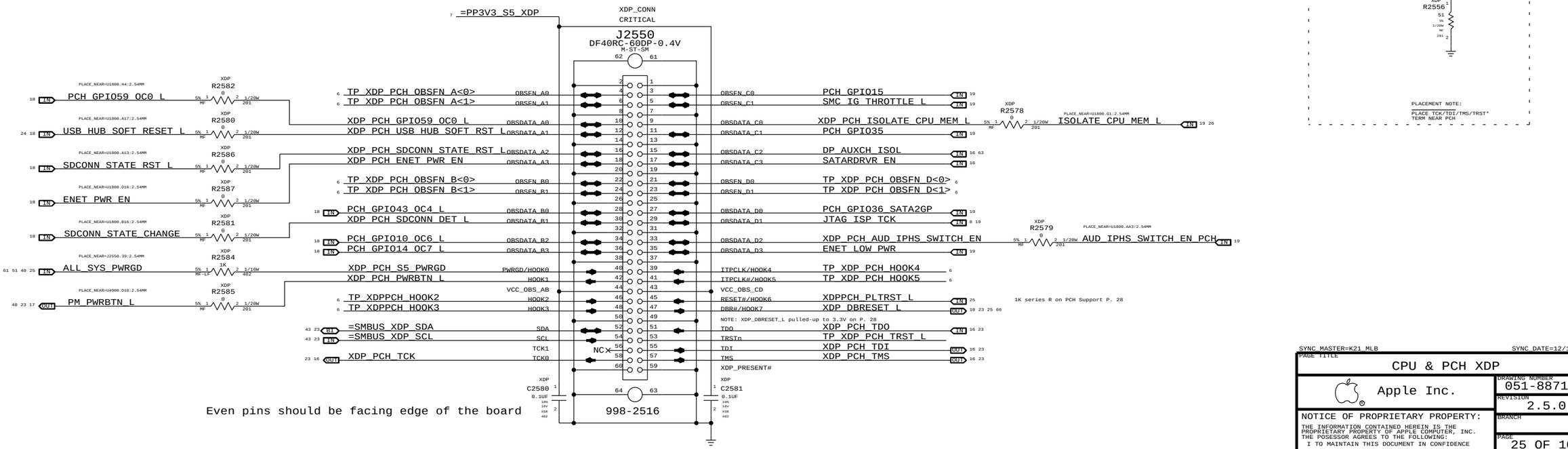
PROCESSOR MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



PCH MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2016

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
REVISION: 2.5.0
BRANCH:
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: USB HUBS

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
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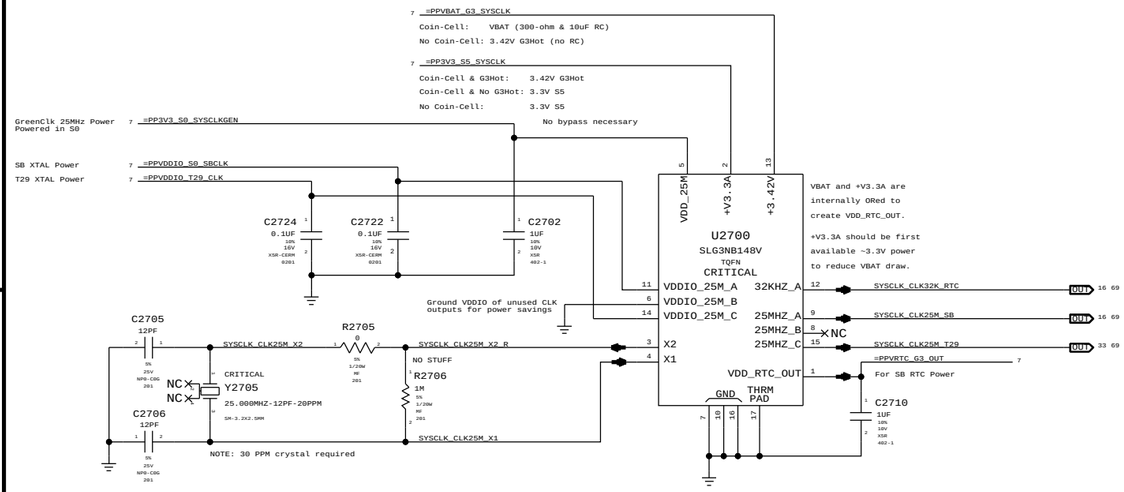
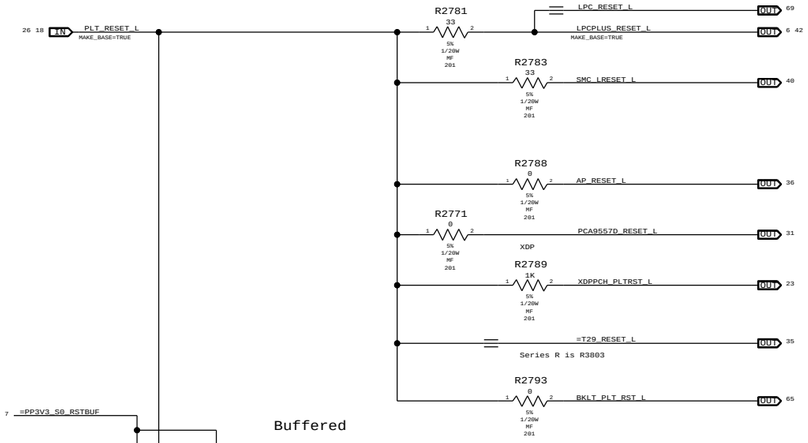
System RTC Power Source & 32kHz / 25MHz Clock Generator

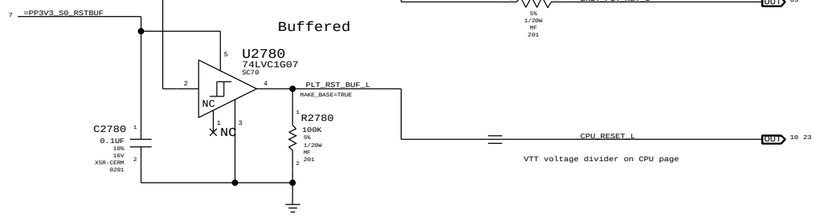


Platform Reset Connections

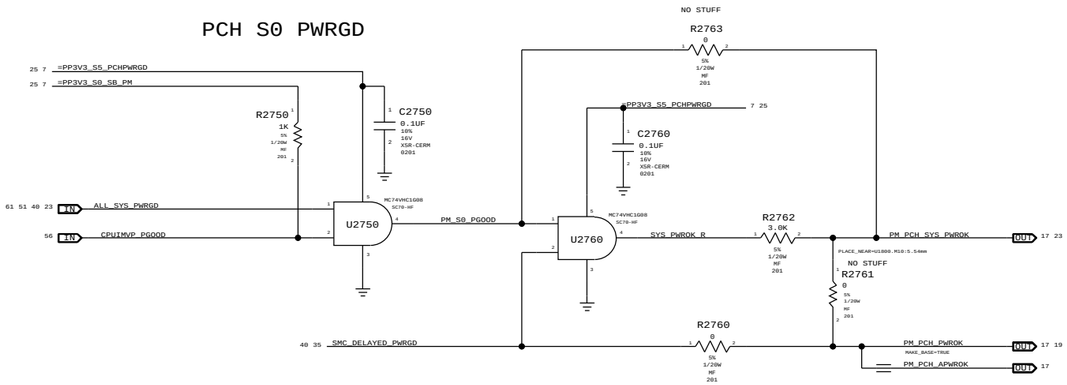
Unbuffered



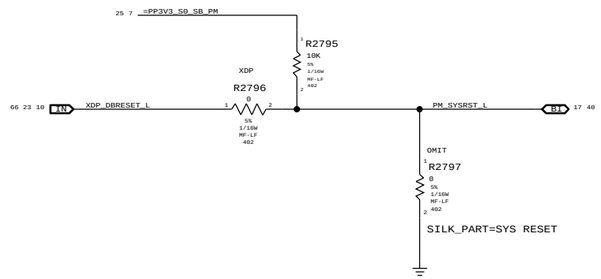
Buffered



PCH S0 PWRGD

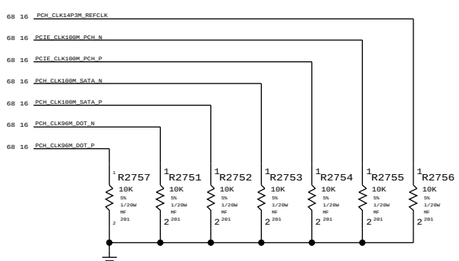


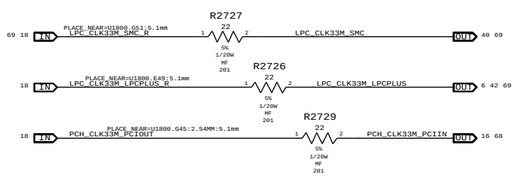
PCH Reset Button



CLOCK (CK505)

UNUSED clock terminations for FCIM MODE





PAGE TITLE	Clock (CK505) and Chipset Support
	Apple Inc.
DRAWING NUMBER	051-8871
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

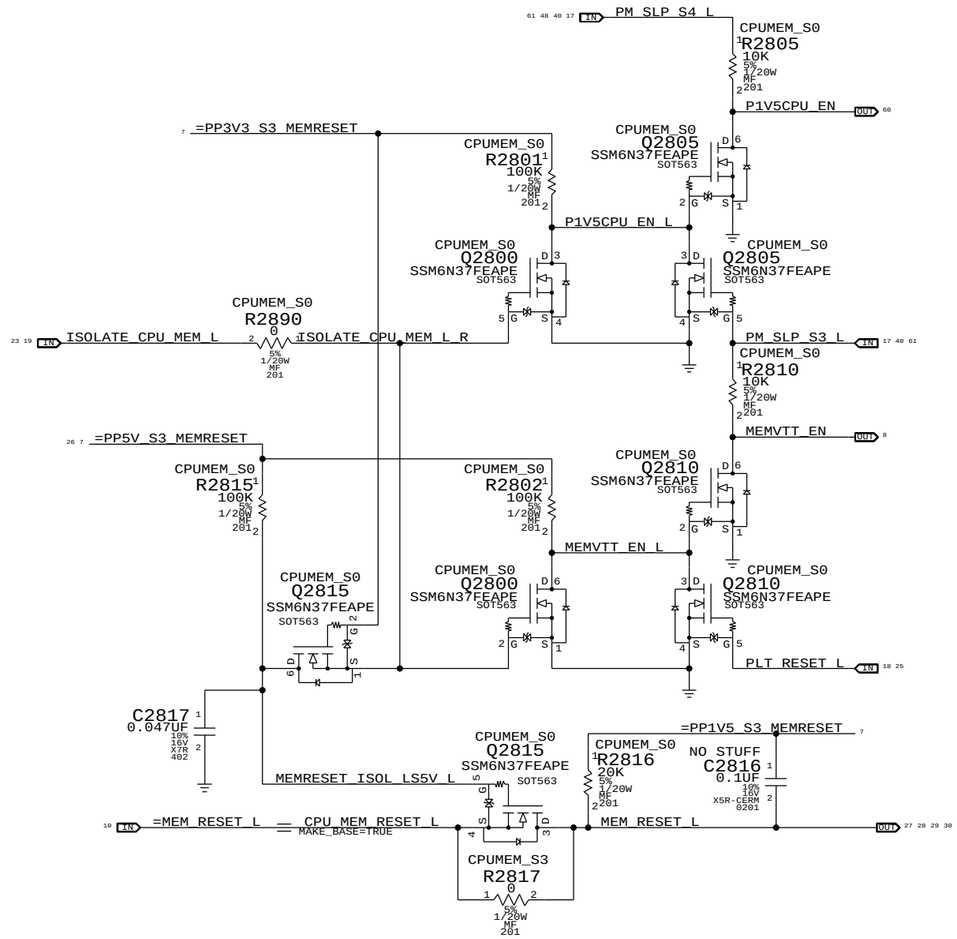
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

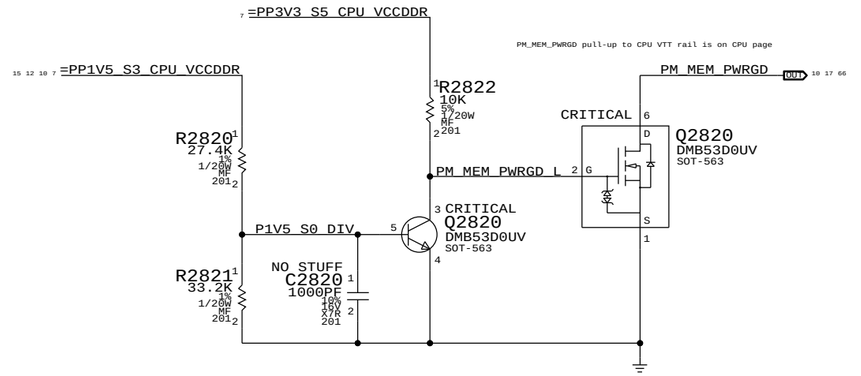


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

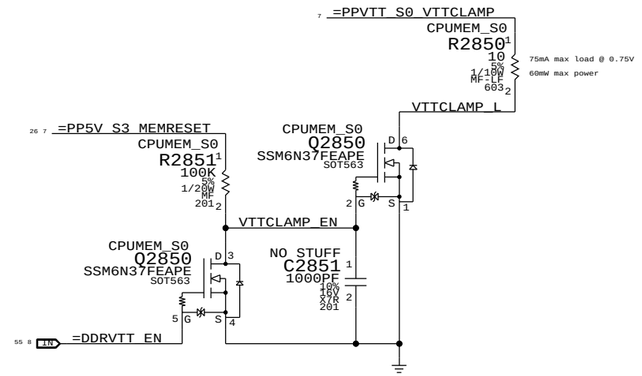
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

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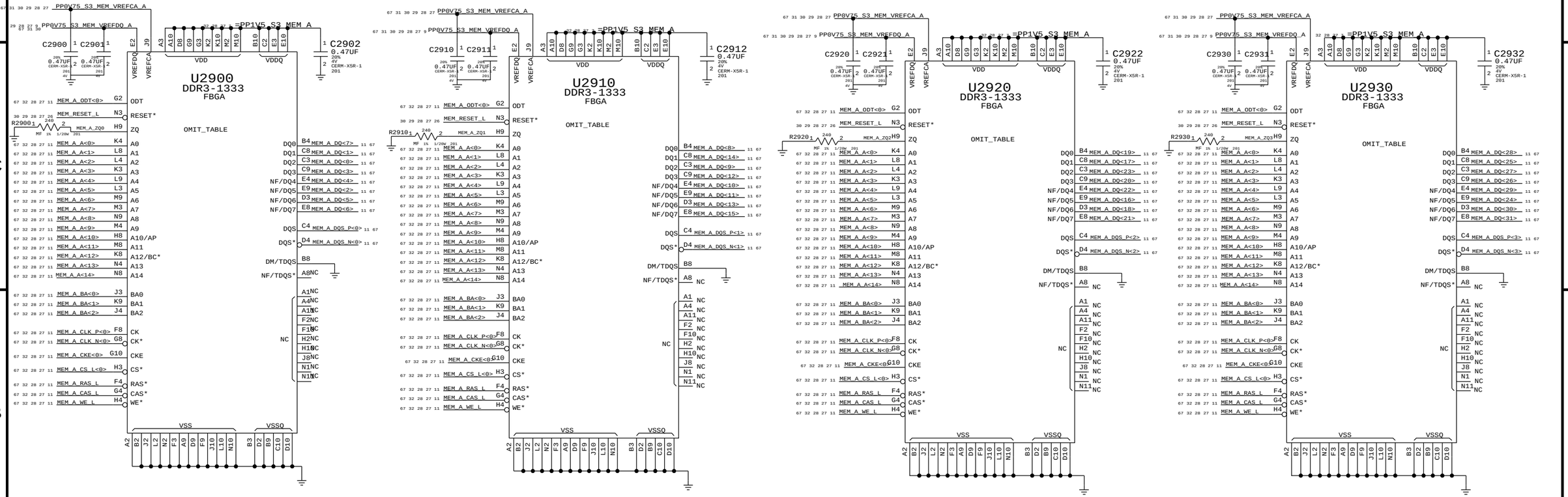

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D
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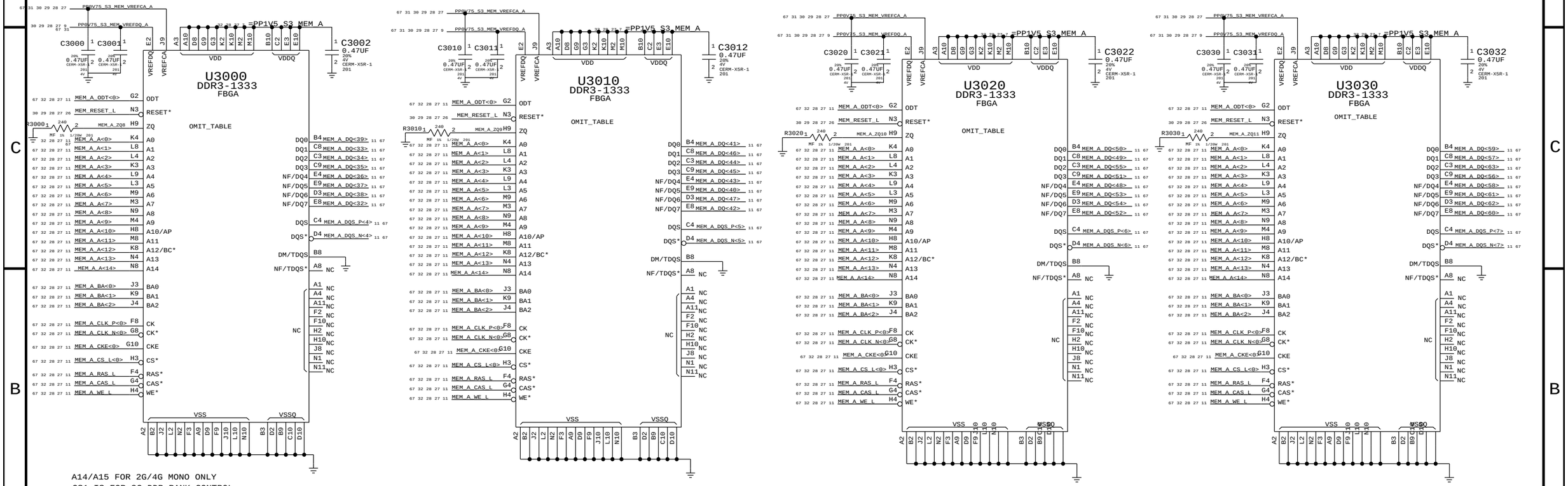

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
DDR3 DRAM CHANNEL A (32-63)

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
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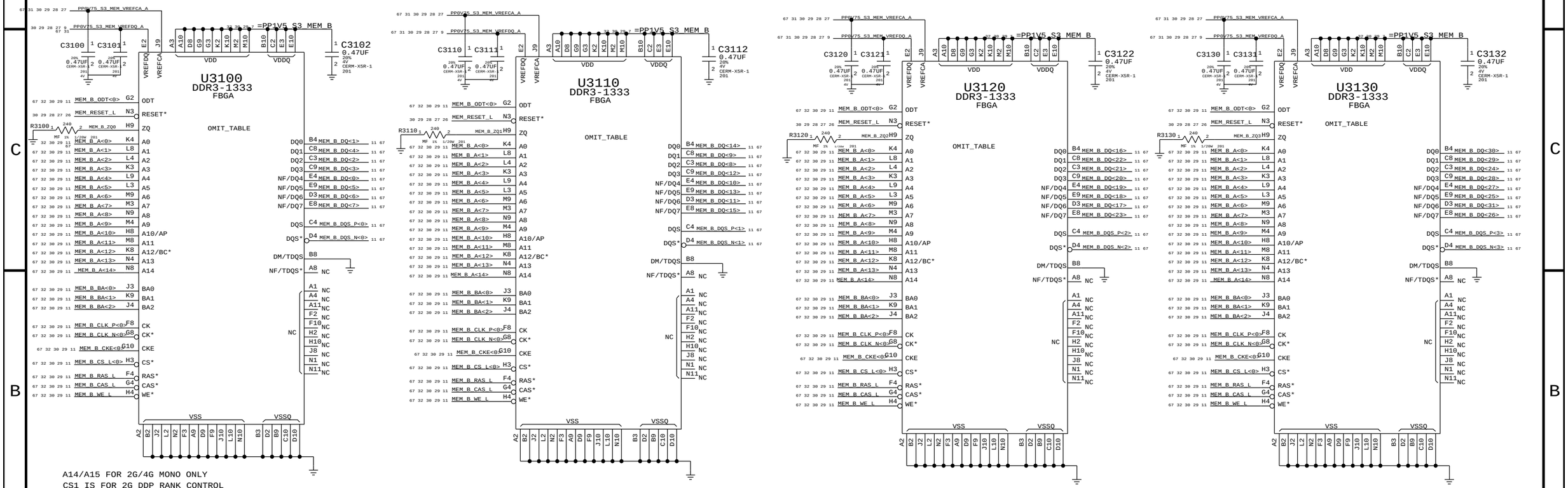

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

DDR3 DRAM CHANNEL B (0-31)

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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BRANCH

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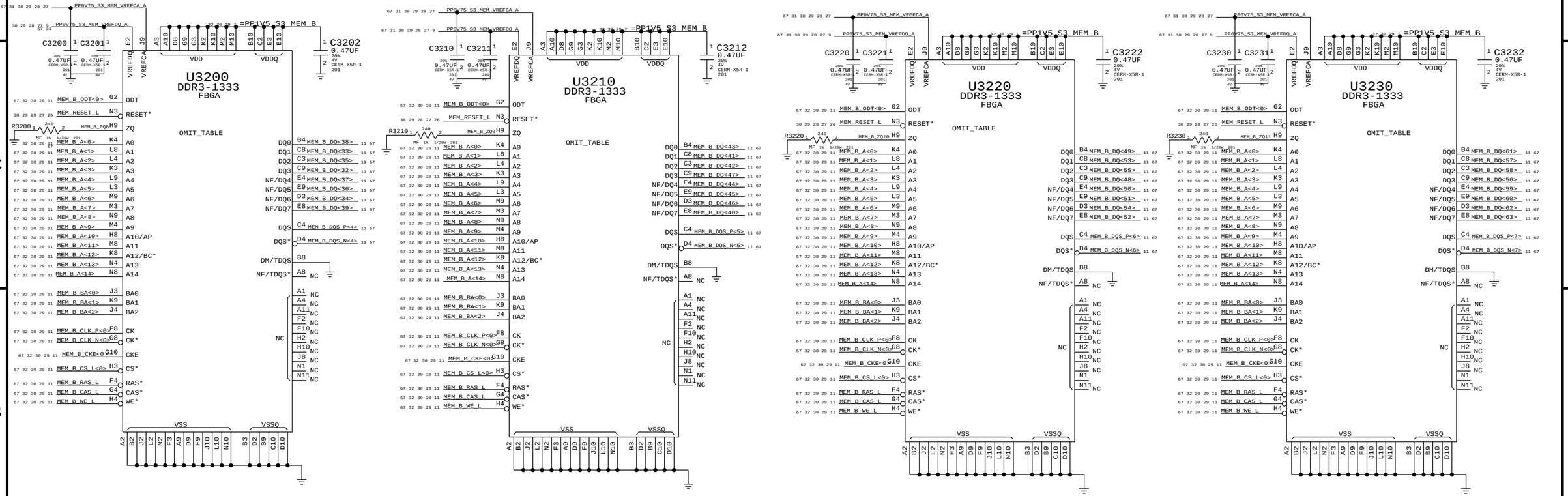

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: DDR3 DRAM CHANNEL B (32-63)

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

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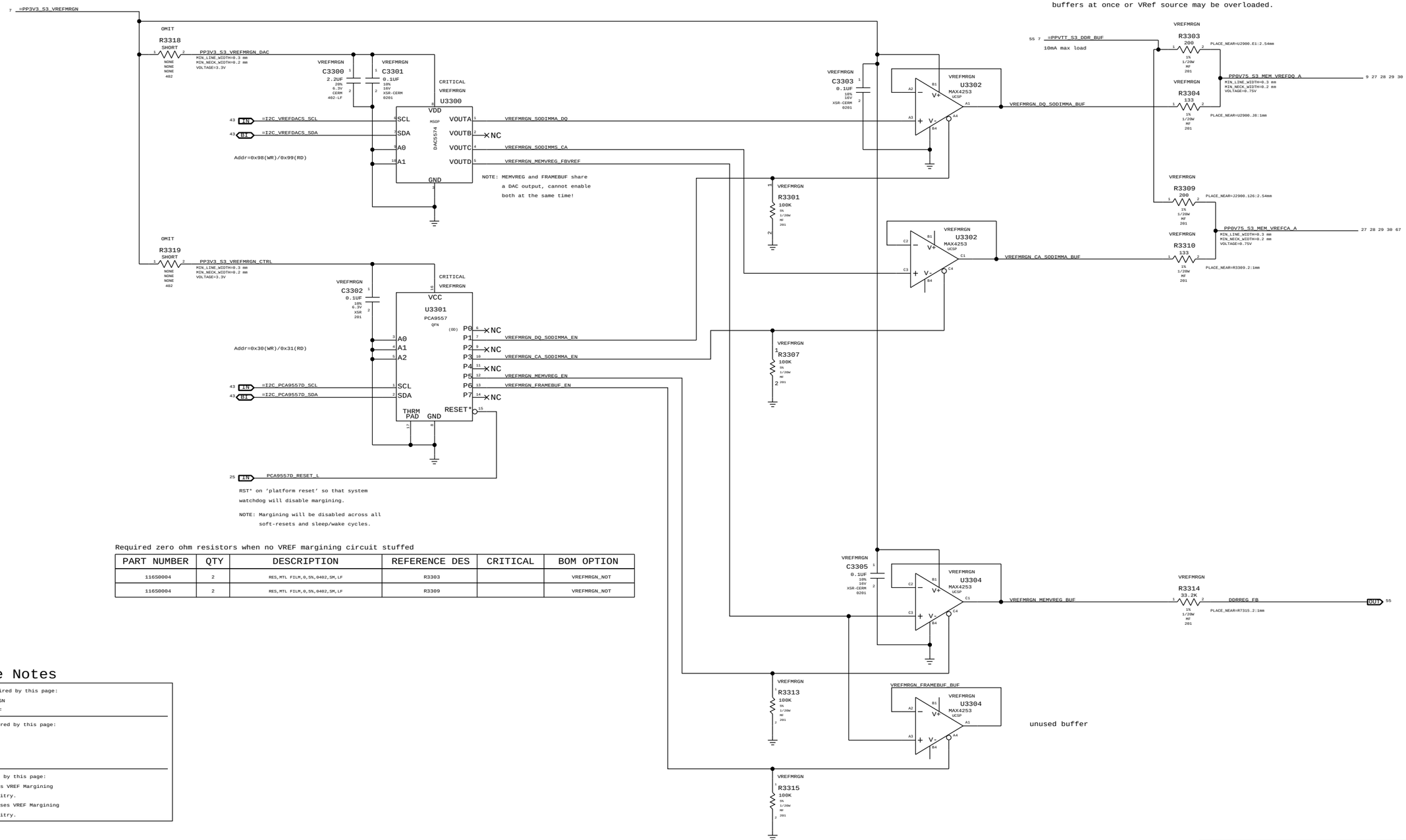

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
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RP3409

=PP1V5_S3_MEM_A

C3408 2.2UF 20% 6.3V CERM 402-LF
C3400 2.2UF 20% 6.3V CERM 402-LF
C3410 2.2UF 20% 6.3V CERM 402-LF
C3420 2.2UF 20% 6.3V CERM 402-LF
C3409 2.2UF 20% 6.3V CERM 402-LF
C3401 2.2UF 20% 6.3V CERM 402-LF
C3411 2.2UF 20% 6.3V CERM 402-LF
C3421 2.2UF 20% 6.3V CERM 402-LF
C3412 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3404 2.2UF 20% 6.3V CERM 402-LF
C3414 2.2UF 20% 6.3V CERM 402-LF
C3424 2.2UF 20% 6.3V CERM 402-LF
C3405 2.2UF 20% 6.3V CERM 402-LF
C3415 2.2UF 20% 6.3V CERM 402-LF
C3425 2.2UF 20% 6.3V CERM 402-LF
C3416 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

=PP1V5_S3_MEM_A

C3418 2.2UF 20% 6.3V CERM 402-LF
C3430 2.2UF 20% 6.3V CERM 402-LF
C3440 2.2UF 20% 6.3V CERM 402-LF
C3450 2.2UF 20% 6.3V CERM 402-LF
C3419 2.2UF 20% 6.3V CERM 402-LF
C3431 2.2UF 20% 6.3V CERM 402-LF
C3441 2.2UF 20% 6.3V CERM 402-LF
C3451 2.2UF 20% 6.3V CERM 402-LF
C3442 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3434 2.2UF 20% 6.3V CERM 402-LF
C3444 2.2UF 20% 6.3V CERM 402-LF
C3454 2.2UF 20% 6.3V CERM 402-LF
C3435 2.2UF 20% 6.3V CERM 402-LF
C3445 2.2UF 20% 6.3V CERM 402-LF
C3455 2.2UF 20% 6.3V CERM 402-LF
C3446 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

=PP0V75_S0_MEM_VTT_A

MEM_A_CKE<0>	RP3401	36	4	5
MEM_A_WE_L	RP3402	36	2	7
MEM_A_A<5>	RP3406	36	2	7
MEM_A_BA<0>	RP3403	36	1	8
MEM_A_CS_L<0>	RP3402	36	1	8
MEM_A_ODT<0>	RP3401	36	2	7
MEM_A_A<12>	RP3403	36	2	7
MEM_A_A<14>	RP3407	36	3	6
MEM_A_A<2>	RP3406	36	1	8
MEM_A_A<11>	RP3406	36	4	5
MEM_A_A<10>	RP3402	36	3	6
MEM_A_A<1>	RP3404	36	3	6
MEM_A_A<0>	RP3403	36	4	5
MEM_A_A<4>	RP3404	36	1	8
MEM_A_A<8>	RP3407	36	2	7
MEM_A_BA<2>	RP3402	36	4	5
MEM_A_BA<1>	RP3403	36	3	6
MEM_A_A<6>	RP3407	36	1	8
MEM_A_A<13>	RP3407	36	4	5
MEM_A_A<3>	RP3404	36	2	7
MEM_A_A<7>	RP3404	36	4	5
MEM_A_CAS_L	RP3401	36	3	6
MEM_A_RAS_L	RP3401	36	1	8
MEM_A_A<9>	RP3406	36	3	6

All: 5%1/32W 4X0201

C3480 0.47UF 20% 4V CERM-X5R-1 201
C3482 0.47UF 20% 4V CERM-X5R-1 201
C3483 0.47UF 20% 4V CERM-X5R-1 201
C3484 0.47UF 20% 4V CERM-X5R-1 201
C3485 0.47UF 20% 4V CERM-X5R-1 201
C3486 0.47UF 20% 4V CERM-X5R-1 201
C3487 0.47UF 20% 4V CERM-X5R-1 201
C3488 0.47UF 20% 4V CERM-X5R-1 201
C3489 0.47UF 20% 4V CERM-X5R-1 201

=PP1V5_S3_MEM_B

C3428 2.2UF 20% 6.3V CERM 402-LF
C3402 2.2UF 20% 6.3V CERM 402-LF
C3470 2.2UF 20% 6.3V CERM 402-LF
C3422 2.2UF 20% 6.3V CERM 402-LF
C3429 2.2UF 20% 6.3V CERM 402-LF
C3403 2.2UF 20% 6.3V CERM 402-LF
C3471 2.2UF 20% 6.3V CERM 402-LF
C3423 2.2UF 20% 6.3V CERM 402-LF
C3472 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3406 2.2UF 20% 6.3V CERM 402-LF
C3474 2.2UF 20% 6.3V CERM 402-LF
C3426 2.2UF 20% 6.3V CERM 402-LF
C3407 2.2UF 20% 6.3V CERM 402-LF
C3475 2.2UF 20% 6.3V CERM 402-LF
C3427 2.2UF 20% 6.3V CERM 402-LF
C3476 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

=PP1V5_S3_MEM_B

C3438 2.2UF 20% 6.3V CERM 402-LF
C3432 2.2UF 20% 6.3V CERM 402-LF
C3490 2.2UF 20% 6.3V CERM 402-LF
C3452 2.2UF 20% 6.3V CERM 402-LF
C3439 2.2UF 20% 6.3V CERM 402-LF
C3433 2.2UF 20% 6.3V CERM 402-LF
C3491 2.2UF 20% 6.3V CERM 402-LF
C3453 2.2UF 20% 6.3V CERM 402-LF
C3492 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3436 2.2UF 20% 6.3V CERM 402-LF
C3494 2.2UF 20% 6.3V CERM 402-LF
C3456 2.2UF 20% 6.3V CERM 402-LF
C3437 2.2UF 20% 6.3V CERM 402-LF
C3495 2.2UF 20% 6.3V CERM 402-LF
C3457 2.2UF 20% 6.3V CERM 402-LF
C3496 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

=PP0V75_S0_MEM_VTT_B

MEM_B_RAS_L	RP3413	36	1	8
MEM_B_A<8>	RP3410	36	1	8
MEM_B_CKE<0>	RP3409	36	1	8
MEM_B_A<7>	RP3411	36	4	5
MEM_B_WE_L	RP3409	36	3	6
MEM_B_A<9>	RP3410	36	3	6
MEM_B_A<0>	RP3408	36	4	5
MEM_B_A<10>	RP3413	36	3	6
MEM_B_A<5>	RP3411	36	2	7
MEM_B_CAS_L	RP3413	36	4	5
MEM_B_A<6>	RP3411	36	3	6
MEM_B_BA<2>		36	4	5
MEM_B_BA<0>	RP3408	36	2	7
MEM_B_BA<1>	RP3408	36	3	6
MEM_B_CS_L<0>	RP3409	36	2	7
MEM_B_A<14>	RP3410	36	4	5
MEM_B_A<4>	RP3414	36	4	5
MEM_B_A<12>	RP3408	36	1	8
MEM_B_A<13>	RP3410	36	2	7
MEM_B_A<2>	RP3414	36	2	7
MEM_B_A<1>	RP3414	36	1	8
MEM_B_ODT<0>	RP3413	36	2	7
MEM_B_A<3>	RP3414	36	3	6
MEM_B_A<11>	RP3411	36	1	8

All: 5%1/32W 4X0201

C3481 0.47UF 20% 4V CERM-X5R-1 201
C3460 0.47UF 20% 4V CERM-X5R-1 201
C3461 0.47UF 20% 4V CERM-X5R-1 201
C3462 0.47UF 20% 4V CERM-X5R-1 201
C3463 0.47UF 20% 4V CERM-X5R-1 201
C3464 0.47UF 20% 4V CERM-X5R-1 201
C3465 0.47UF 20% 4V CERM-X5R-1 201
C3466 0.47UF 20% 4V CERM-X5R-1 201
C3467 0.47UF 20% 4V CERM-X5R-1 201

MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0>
R3468 30 5% 1/20W MF 201
MEM_A_CLK_TERM_R VOLTAGE=0V
C3469 0.1UF 10% X5R 201 6.3V
C3468 3.3PF 5% 25V CERM 201
MEM_A_CLK_P<0>
R3469 30 5% 1/20W MF 201

MEM_B_CLK_N<0>
R3478 30 5% 1/20W MF 201
MEM_B_CLK_TERM_R VOLTAGE=0V
C3479 0.1UF 10% X5R 201 6.3V
C3478 3.3PF 5% 25V CERM 201
MEM_B_CLK_P<0>
R3479 30 5% 1/20W MF 201

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: DDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
REVISION: 2.5.0
BRANCH:
PAGE: 34 OF 109
SHEET: 32 OF 74

CRITICAL
OMIT_TABLE

U3600
EAGLE_RIDGE-192
FCBGA
(1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_R2D_C_P<0>	C3600 0.1UF	PCIE_T29_R2D_P<0>	P14	PERP_0
PCIE_T29_R2D_C_N<0>	C3601 0.1UF	PCIE_T29_R2D_N<0>	P15	PERN_0
PCIE_T29_R2D_C_P<1>	C3602 0.1UF	PCIE_T29_R2D_P<1>	K14	PERP_1
PCIE_T29_R2D_C_N<1>	C3603 0.1UF	PCIE_T29_R2D_N<1>	K15	PERN_1
PCIE_T29_R2D_C_P<2>	C3604 0.1UF	PCIE_T29_R2D_P<2>	F14	PERP_2
PCIE_T29_R2D_C_N<2>	C3605 0.1UF	PCIE_T29_R2D_N<2>	F15	PERN_2
PCIE_T29_R2D_C_P<3>	C3606 0.1UF	PCIE_T29_R2D_P<3>	B15	PERP_3
PCIE_T29_R2D_C_N<3>	C3607 0.1UF	PCIE_T29_R2D_N<3>	B14	PERN_3

TRANSMIT

PETP_0	T14	PCIE_T29_D2R_C_P<0>	C3640 0.1UF	PCIE_T29_D2R_P<0>
PETN_0	T15	PCIE_T29_D2R_C_N<0>	C3641 0.1UF	PCIE_T29_D2R_N<0>
PETP_1	M14	PCIE_T29_D2R_C_P<1>	C3642 0.1UF	PCIE_T29_D2R_P<1>
PETN_1	M15	PCIE_T29_D2R_C_N<1>	C3643 0.1UF	PCIE_T29_D2R_N<1>
PETP_2	H14	PCIE_T29_D2R_C_P<2>	C3644 0.1UF	PCIE_T29_D2R_P<2>
PETN_2	H15	PCIE_T29_D2R_C_N<2>	C3645 0.1UF	PCIE_T29_D2R_N<2>
PETP_3	D14	PCIE_T29_D2R_C_P<3>	C3646 0.1UF	PCIE_T29_D2R_P<3>
PETN_3	D15	PCIE_T29_D2R_C_N<3>	C3647 0.1UF	PCIE_T29_D2R_N<3>

TP_T29_MONDC0	R3610 0 NO STUFF	T29_MONDC0	A14 MONDC0
TP_T29_MONDC1	R3611 0 NO STUFF	T29_MONDC1	A15 MONDC1
TP_T29_MONOBSP	C3615 0.1UF	T29_MONOBSP	A13 MONOBSP
TP_T29_MONOBSN	C3616 0.1UF	T29_MONOBSN	B13 MONOBSN

DEBUG: For monitoring current/voltage

DEBUG: For monitoring clock

WAKE*	M2	T29_PCIE_WAKE_L	R3651 10K =PP3V3_T29_RTR
PERST*	C2	T29_RESET_L	
RSENSE	C8	T29_RSENSE	R3655 1.0K 0.1% 1/10W TF 402
RBIAS	C7	T29_RBIAS	

CLK REQUEST

=T29_CLKREQ_L	P1	PCIE_CLKREQ_0*	

MISC

POWER ON RESET

Not used in host mode.

PCIE_RST_0*	R1	TP_T29_PCIE_RESET0_L
PCIE_RST_1*	L1	TP_T29_PCIE_RESET1_L
PCIE_RST_2*	L2	TP_T29_PCIE_RESET2_L
PCIE_RST_3*	G2	TP_T29_PCIE_RESET3_L

JTAG

TDI	T3	JTAG_T29_TDI
TMS	T5	JTAG_T29_TMS
TCK	R2	JTAG_T29_TCK
TDO	U4	JTAG_T29_TDO

CLOCKS

REFCLK_100_IN_P	A12	PCIE_CLK100M_T29_P
REFCLK_100_IN_N	B12	PCIE_CLK100M_T29_N
XTAL_25_IN	D11	SYSCLK_CLK25M_T29_R
XTAL_25_OUT	C11	TP_T29_XTAL25OUT
TMU_CLK_OUT	U5	T29_TMU_CLK_OUT
TMU_CLK_IN	M1	T29_TMU_CLK_IN

=PP3V3_T29_RTR → R3698 10K

R3695 806 → SYSCLK_CLK25M_T29

R3696 1K

NO STUFF R3699 10K

T29_SPI_MOSI	U6	EE_DI	EEPROM
T29_SPI_MISO	P2	EE_DO	
T29_SPI_CS_L	U3	EE_CS*	
T29_SPI_CLK	N1	EE_CLK	
TP_T29_THERM_DP	B2	THERM_DP	
T29_TEST_EN	E2	TEST_EN	TEST PORT
T29_TEST_POINT_3	D1	TEST_PWR_GOOD	

Use B1 GND ball for THERM_DN

R3625 0

R3629 0

DP_T29SNK0_ML_P<3>	T8	DPSNK0_ML_LANE_3P_IN0_HDMI_TMDS_CLK_P	SINK PORT 0
DP_T29SNK0_ML_N<3>	U8	DPSNK0_ML_LANE_3N_IN0_HDMI_TMDS_CLK_N	
DP_T29SNK0_ML_P<2>	T9	DPSNK0_ML_LANE_2P_IN0_HDMI_TMDS_O_P	
DP_T29SNK0_ML_N<2>	U9	DPSNK0_ML_LANE_2N_IN0_HDMI_TMDS_0_N	
DP_T29SNK0_ML_P<1>	T10	DPSNK0_ML_LANE_1P_IN0_HDMI_TMDS_1_P	
DP_T29SNK0_ML_N<1>	U10	DPSNK0_ML_LANE_1N_IN0_HDMI_TMDS_1_N	
DP_T29SNK0_ML_P<0>	T11	DPSNK0_ML_LANE_0P_IN0_HDMI_TMDS_2_P	
DP_T29SNK0_ML_N<0>	U11	DPSNK0_ML_LANE_0N_IN0_HDMI_TMDS_2_N	
DP_T29SNK0_AUXCH_P	T7	DPSNK0_AUX_CHP	
DP_T29SNK0_AUXCH_N	U7	DPSNK0_AUX_CHN	
DP_T29SNK0_HPD	T4	DPSNK0_HDMI_IN_HOT_PLUG_DET	

R3630 100K

DPSRC0_ML_LANE_3P_OUT0_HDMI_TMDS_2_P	T12	DP_T29SRC_ML_CP<3>	R3661 0
DPSRC0_ML_LANE_3N_OUT0_HDMI_TMDS_2_N	U12	DP_T29SRC_ML_CN<3>	R3662 0
DPSRC0_ML_LANE_0P_OUT0_HDMI_TMDS_CLK_P	N12	DP_T29SRC_ML_CP<0>	R3663 0
DPSRC0_ML_LANE_0N_OUT0_HDMI_TMDS_CLK_N	R12	DP_T29SRC_ML_CN<0>	R3664 0

SOURCE PORT 0

=PP3V3_T29_RTR

100pF SRF > 40MHz

DPSRC0_HOT_PLUG_DET	T6	DP_T29SRC_HPD
DP_ATEST	U15	T29_DP_ATEST
DP_RES	U14	T29_DP_RES

C3685 100PF C3686 0.01UF

HDMI/
DISPLAYPORT

TP_T29_HDMI_5V_OUT	U1	HDMI_5V_OUT	HDMI
HDMI_SCL_IN	B1	T29_HDMI_SCL_IN	R3685 14K R3632 100K
HDMI_SDA_IN	A2	T29_HDMI_SDA_IN	
HDMI_OUT_HOT_PLUG_DET	F3	T29_HDMI_OUT_HPD	

PORTS

PRT0_CIOT_P	A6	T29_R2D_C_P<0>
PRT0_CIOT_N	B6	T29_R2D_C_N<0>
PRT0_CIOR_P	A4	T29_D2R_P<0>
PRT0_CIOR_N	B4	T29_D2R_N<0>
CIO_0_LSEO	H2	T29_LSEO<0>
CIO_0_LSOE	K1	T29_LSOE<0>
PRT1_CIOT_P	B10	T29_R2D_C_P<1>
PRT1_CIOT_N	A10	T29_R2D_C_N<1>
PRT1_CIOR_P	A8	T29_D2R_P<1>
PRT1_CIOR_N	B8	T29_D2R_N<1>
CIO_1_LSEO	J1	T29_LSEO<1>
CIO_1_LSOE	K2	T29_LSOE<1>
CIO_PLUG_EVENT	H1	T29_CIO_PLUG_EVENT

PORT0 / PORT1

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

I2C_T29_SCL	C1	CIO_MDC
I2C_T29_SDA	F1	CIO_MDIO

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0>	C3620 0.1UF	DP_T29SNK0_ML_P<0>	
DP_T29SNK0_ML_C_N<0>	C3621 0.1UF	DP_T29SNK0_ML_N<0>	
DP_T29SNK0_ML_C_P<1>	C3622 0.1UF	DP_T29SNK0_ML_P<1>	
DP_T29SNK0_ML_C_N<1>	C3623 0.1UF	DP_T29SNK0_ML_N<1>	
DP_T29SNK0_ML_C_P<2>	C3624 0.1UF	DP_T29SNK0_ML_P<2>	
DP_T29SNK0_ML_C_N<2>	C3625 0.1UF	DP_T29SNK0_ML_N<2>	
DP_T29SNK0_ML_C_P<3>	C3626 0.1UF	DP_T29SNK0_ML_P<3>	
DP_T29SNK0_ML_C_N<3>	C3627 0.1UF	DP_T29SNK0_ML_N<3>	
DP_T29SNK0_AUXCH_C_P	C3628 0.1UF	DP_T29SNK0_AUXCH_P	
DP_T29SNK0_AUXCH_C_N	C3629 0.1UF	DP_T29SNK0_AUXCH_N	

=PP3V3_T29_RTR → R3690 3.3K, R3691 3.3K, C3690 1.0UF 20% 6.3V X5R 0201-MUR, R3692 3.3K, R3693 3.3K

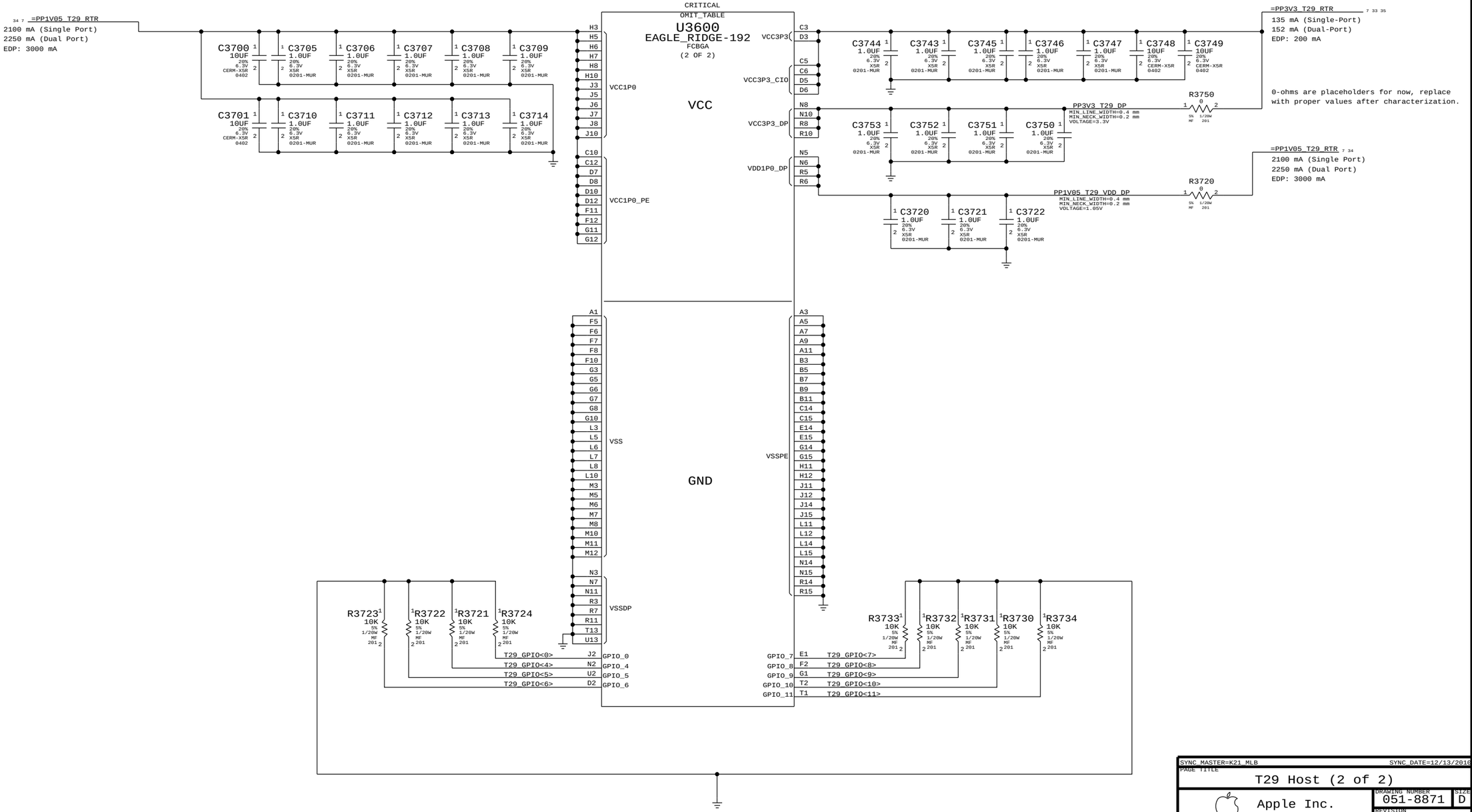
U3690 M95160 2KX8-1.8V MLP

CRITICAL
OMIT_TABLE

T29_SPI_MOSI	D	Q T29_SPI_MISO
T29_SPI_CLK	C	
T29_SPI_CS_L	S_L	
T29ROM_WP_L	W_L	
T29ROM_HOLD_L	HOLD_L	
	VSS	THM PAD

=PP3V3_T29_RTR → R3670 10K, R3671 10K

T29_HDMI_SCL_IN	R3673 10K
T29_HDMI_SDA_IN	R3674 10K
T29_CIO_PLUG_EVENT	
T29_HDMI_OUT_HPD	



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH:

PAGE: 37 OF 109

SHEET: 34 OF 74

Page Notes

Power aliases required by this page:

- =PPVIN_SW_T29BST	(8-13V Boost Input)
- =PP18V_T29_REG	(18V Boost Output)
- =PP3V3_T29_P3V3T29FET	(3.3V FET Input)
- =PP3V3_T29_FET	(3.3V FET Output)
- =PP3V3_S0_T29PWRCTL	
- =PP1V05_T29_P1V05T29FET	(1.05V FET Input)
- =PP1V05_T29_FET	(1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 18V Boost Regulator

=PPVIN_SW_T29BST
8-13V Input
Changes required
for 2S.

R3820 0.010 1% 1/4W MF 805 — =PPVIN_SW_T29BST_R

CRITICAL
T29BST:Y
Q3880
SI8409DB
8GA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

Voltage not specified here,
add property on another page.

T29BST:Y R3880 470K 5% 1/20W MF 201 — C3880 0.1UF 10% 25V X5R 402 — T29BST_PWREN_DIV_L

T29BST:Y R3881 150K 5% 1/20W MF 201 — T29BST_PWREN_L

T29BST:Y Q3805 SSM3K15FV SOD-VESM-HF — T29_A_HV_EN

T29BST:Y R3891 200K 1% 1/20W MF 201 <R1> — T29BST_EN_UVLO

T29BST:Y C3890 10UF 10% 25V X5R 805
T29BST:Y C3891 10UF 10% 25V X5R 805

CRITICAL
T29BST:Y
L3895
6.8UH-4.0A
PIMB062D-SM

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
T29BST:Y
U3890
LT3957
QFN

VIN	27
SW	8, 9, 20, 21, 38
SNS1	6
SNS2	3
EN/UVLO	25
INTVCC	28
VC	30
RT	33
SS	32
SYNC	34
NC	1, 2, 10, 35, 36
FBX	31
SGND	4, 23, 24, 37
GND	12, 13, 14, 15, 16, 17

T29BST_SNS1
T29BST:Y R3889 0 5% 1/20W MF 201

CRITICAL
T29BST:Y
D3895
POWERDI-123
DFLS230L

T29BST_SNS2
XW3895 SM — PLACE_NEAR=C3895.1:2 mm

T29BST_VSNS
T29BST:Y R3895 133K 1% 1/10W MF-LF 402 <Ra>
T29BST:Y C3888 10PF 5% 50V CERM 402

T29BST_FBX
T29BST:Y R3896 15.8K 1% 1/10W MF-LF 402 <Rb>
NO STUFF C3889 100PF 5% 50V CERM 402

T29BST:Y C3892 4.7UF 10% 10V X5R 805
T29BST:Y C3887 47PF 5% 25V NP0-C0G 201
T29BST:Y R3893 10K 1% 1/20W MF 201 — T29BST_VC_RC
T29BST:Y R3892 73.2K 1% 1/20W MF 201 <R2>
T29BST:Y C3893 3300PF 10% 10V X7R 201
T29BST:Y R3894 41.2K 1% 1/20W MF 201
T29BST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS

GND_T29BST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to
GND inside package,
no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

=PP15V_T29_REG
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

T29BST:Y C3895 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3896 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3897 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3898 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3899 0.001UF 10% 50V X7R 402

T29BST:Y Q3888 SSM6N37FEAPE SOT563 — Max Vgs: 10V
T29BST:Y R3888 330K 5% 1/20W MF 201 — T29BST_SHDN_DIV
T29BST:Y R3887 330K 5% 1/20W MF 201
T29BST:Y Q3888 SSM6N37FEAPE SOT563 — SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL
C3800 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
U3800
SLG4AP016V
TDFN

Platform (PCIe) Reset
=T29_RESET_L
R3803 10K 5% 1/20W MF 201

Open-Drain GPIO
T29_SW_RESET_L
T29_CLKREQ_L
Pull-up provided by SB page.

=PP3V3_T29_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_T29
SENSE 0.7V
DLY
RESET*
T29_RESET_L
DLY = 60 ms +/- 20%
=T29_CLKREQ_L
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE
MR*
EN
OUT (OD)
IN
GND
THRM PAD

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET
U3810 TPS22924 CSP
VIN VOUT ON GND CRITICAL
C3810 1UF 10% 6.3V CERM 402
=PP3V3_T29_FET
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

=PP1V05_S0_P1V05T29FET
U3815 TPS22924 CSP
VIN VOUT ON GND CRITICAL
C3815 1UF 10% 6.3V CERM 402
=PP1V05_T29_FET
Max Current = 3.4A (85C)

U3816 TPS22924 CSP
VIN VOUT ON GND CRITICAL
T29_PWR_EN
Pull-up provided by SB page.
U3816.A2: PLACE_NEAR=U3815.B2:3 mm

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L OUT 6 40

69 6 PCIE_AP_R2D_N — C4030 0.1UF 10% 6.3V 201 X5R — PCIE_AP_R2D_C_N IN 16 69
PLACEMENT_NOTE=Place close to J4001.

69 6 PCIE_AP_R2D_P — C4031 0.1UF 10% 6.3V X5R 201 — PCIE_AP_R2D_C_P IN 16 69
PLACEMENT_NOTE=Place close to J4001.

PCIE_CLK100M_AP_N IN 6 16 69
PCIE_CLK100M_AP_P IN 6 16 69

PCIE_AP_D2R_P OUT 6 16 69
PCIE_AP_D2R_N OUT 6 16 69

PCIE_WAKE_L OUT 6 17

BLUETOOTH

USB_BT_N BI 6 24 68
USB_BT_P BI 6 24 68

=PP3V3_S3_BT 6 7

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.18:1.5mm

MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

PP3V3_WLAN_F 5 — C4021 0.1UF 10% 6.3V X5R 201 — C4020 10UF 20% 16V X5R 603
PLACEMENT_NOTE=Place close to Q4050.

CRITICAL
R4052 0.020 1% 0.25W MF 805
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
3 — 4 PP3V3_WLAN_R

CRITICAL
Q4050
TPCP8102
23V1K-SM

C4050 0.1UF 10% 16V X5R-CERM 0201

C4051 0.033UF 10% 16V X5R 402

R4050 100K 5% 1/20W MF 201

R4051 10K 5% 1/20W MF 201

P3V3WLAN_SS

=PP3V3_S3_WLAN 7 36

PM_WLAN_EN_L IN 61

ISNS_AIRPORT_P OUT 45 73
ISNS_AIRPORT_N OUT 45 73

DLY = 60 MS +/- 20%

=PP3V3_S3_WLAN 7 36

C4053 0.1UF 10% 6.3V X5R 201

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE 0.7V
DLY
RESET* 4
MR* 3
EN 6
OUT 8 (OD)
IN 7
THRM PAD 9
GND 5

R4053 100K 1% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 1% 1/20W MF 201

P3V3WLAN_VMON
6 AP_RESET_CONN_L
6 AP_CLKREQ_O_L

AP_RESET_L IN 25
AP_PWR_EN IN 18 61
AP_CLKREQ_L_R — R4090 0 5% 1/20W MF 201 — AP_CLKREQ_L OUT 16

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8871
SIZE D
REVISION 2.5.0
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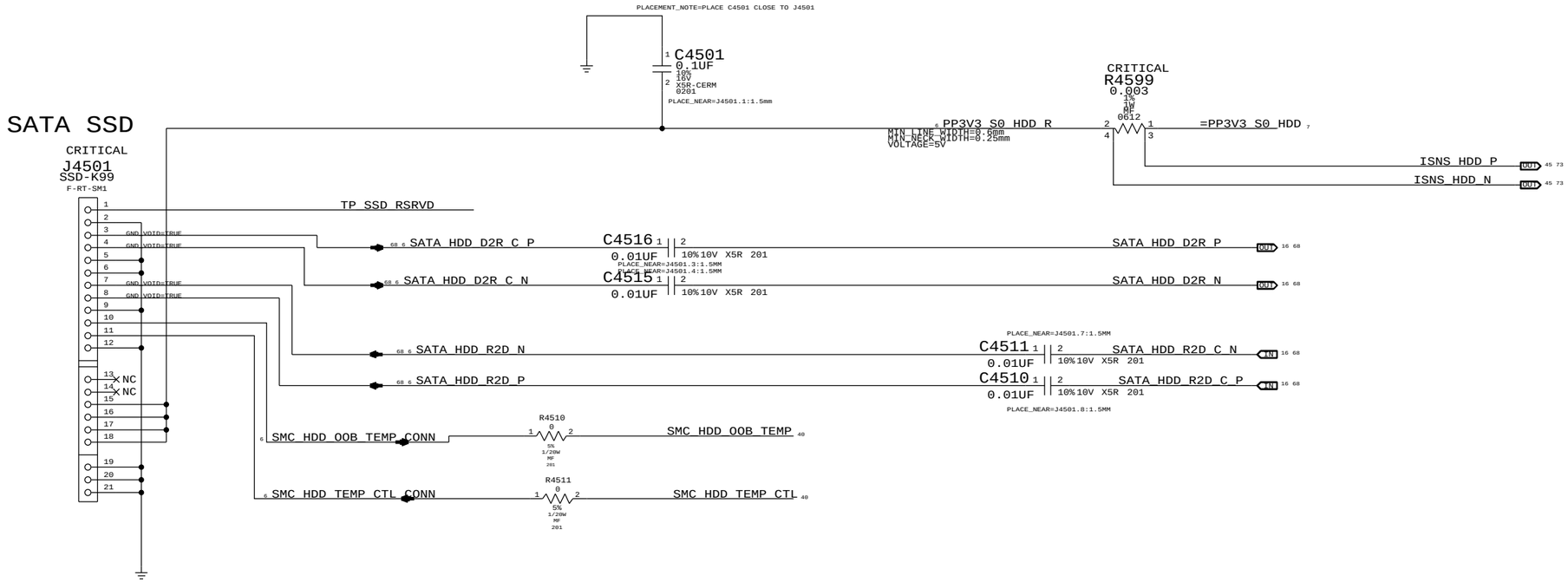

SYNC MASTER=K21_MLB SYNC DATE=12/13/2010

PAGE TITLE

SATA CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

BRANCH

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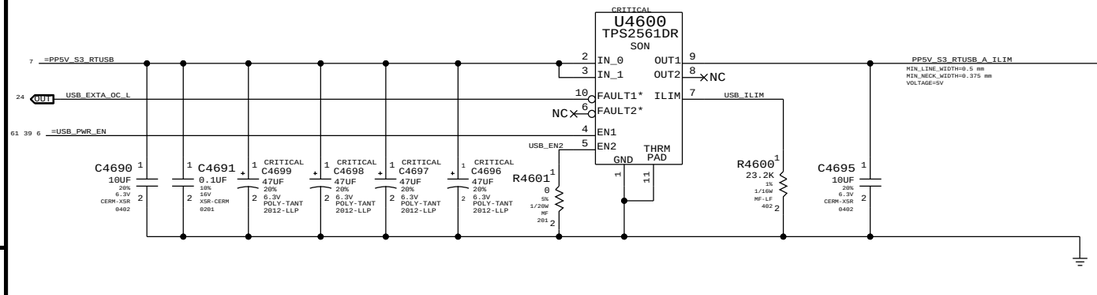
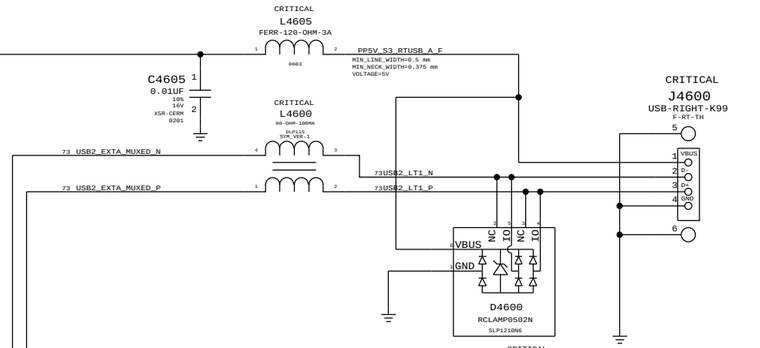
USB Port Power Switch



Current limit (R4600): 2.17-2.59A

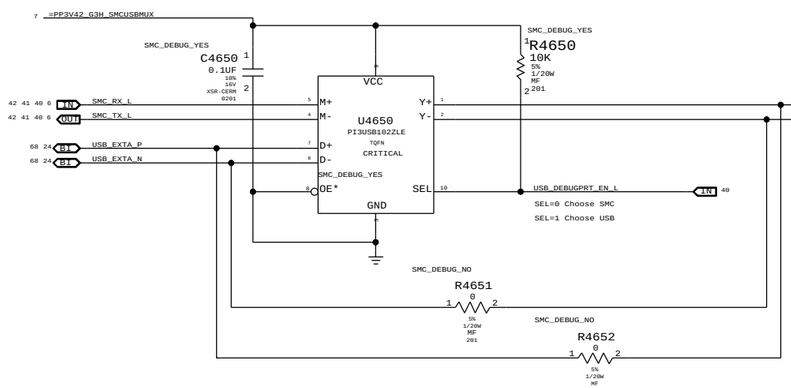
Right USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 at connector pin

USB/SMC Debug Mux



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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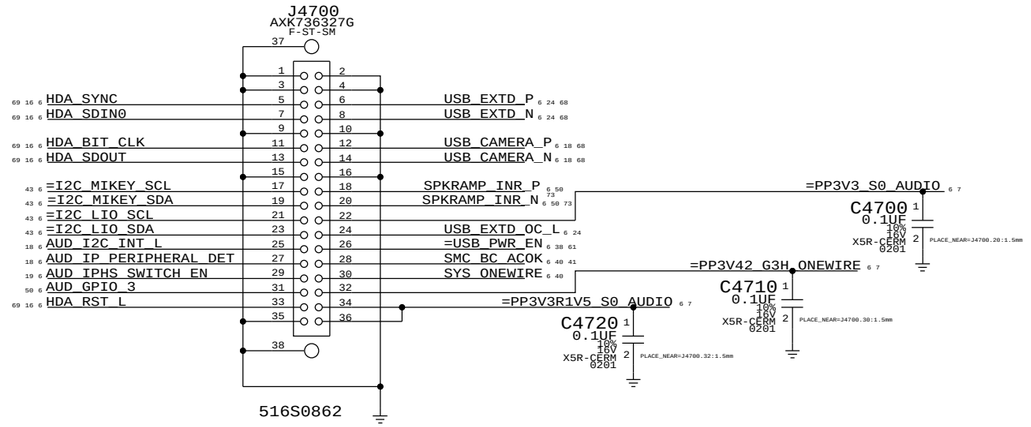
LIO CONNECTOR



SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	LIO CONNECTORS
Apple Inc.	DRAWING NUMBER 051-8871 · SIZE D
	REVISION 2.5.0
	BRANCH
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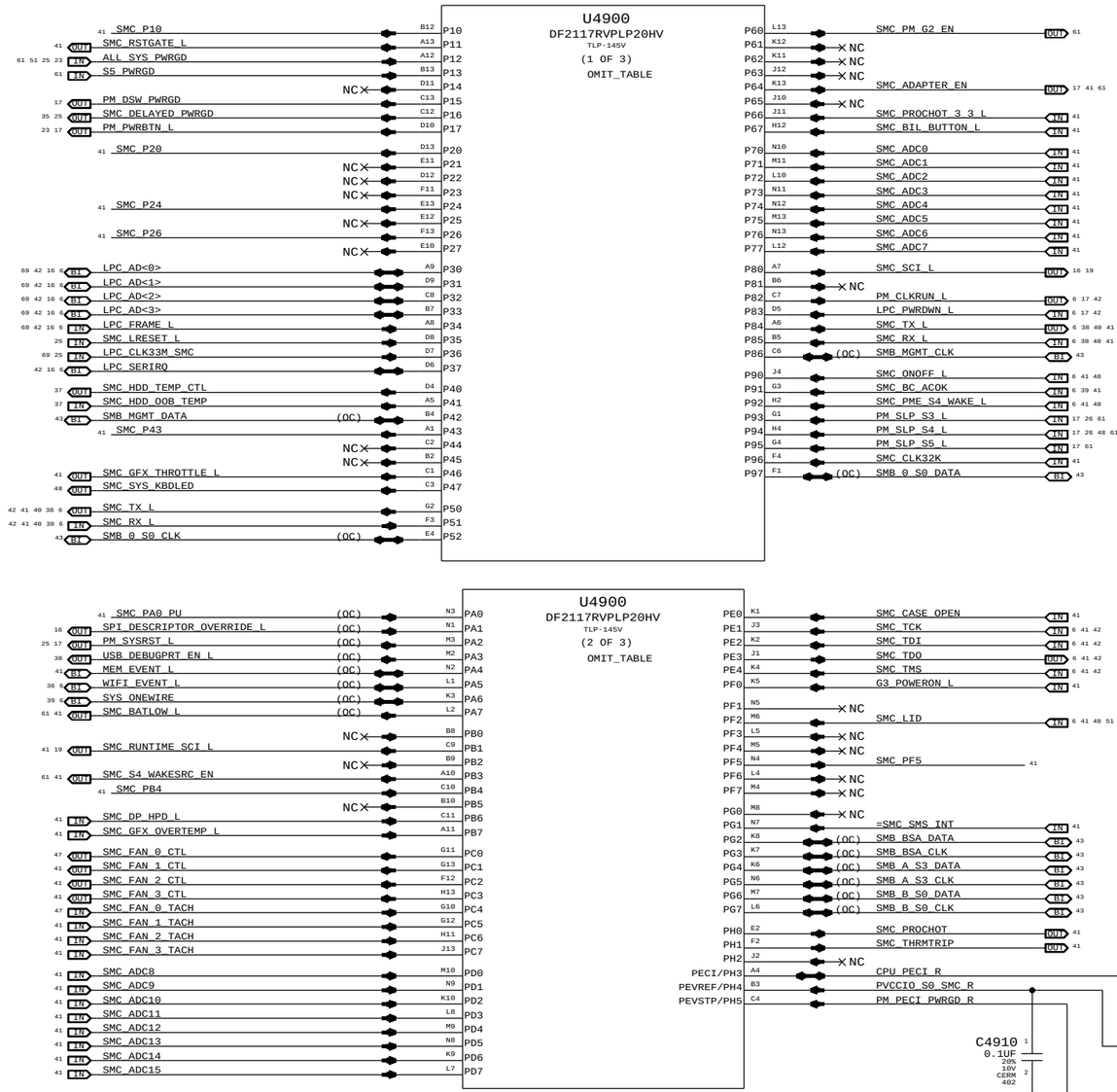
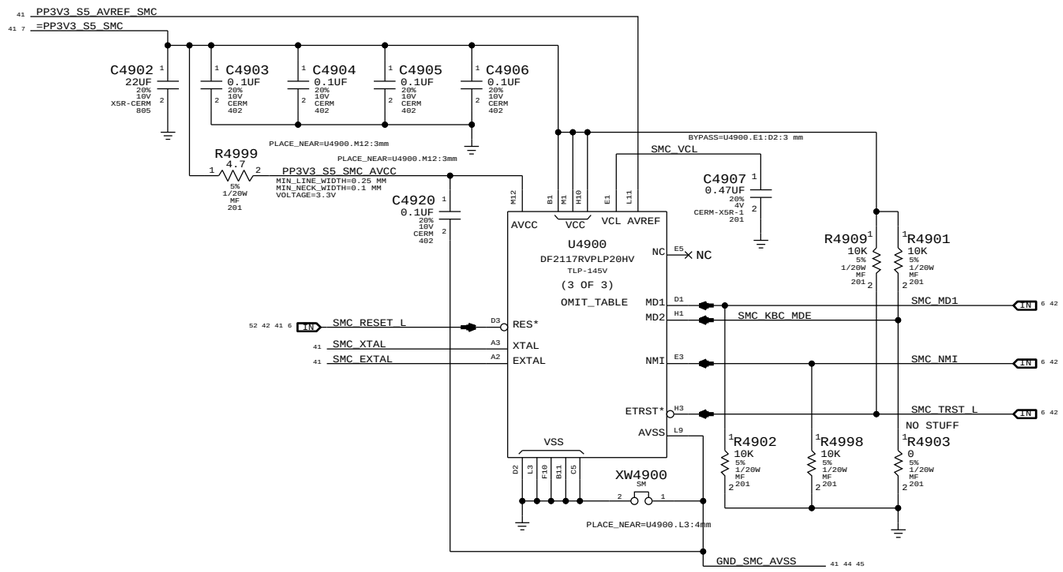
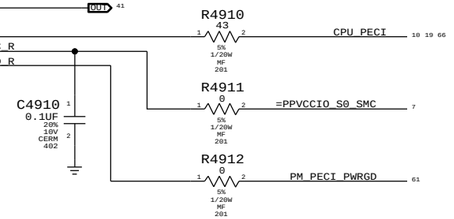
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

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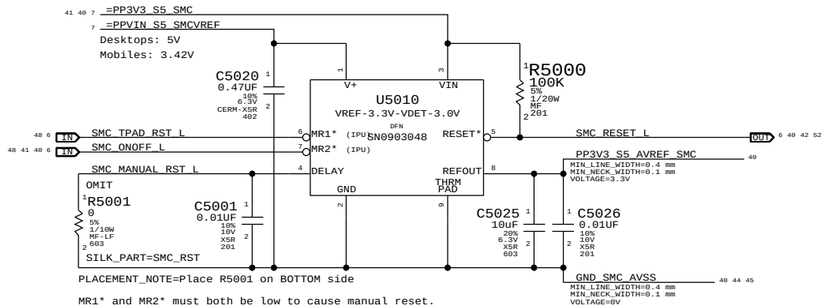
SMC Reset "Button", Supervisor & AVREF Supply



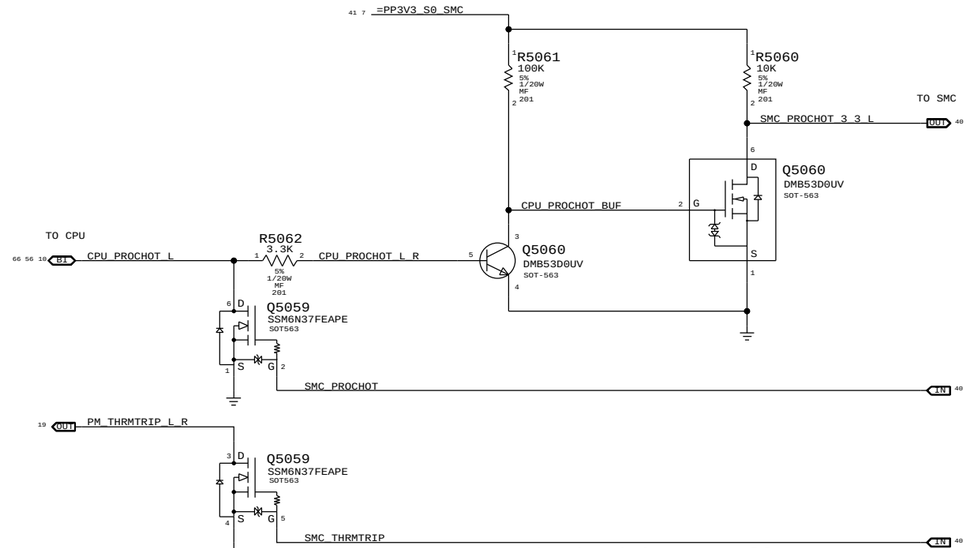
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

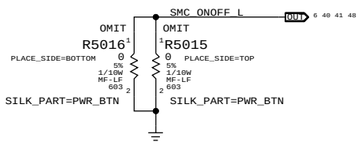
SMC_FAN_2_CTL — NC_SMC_FAN_2_CTL
SMC_FAN_2_TACH — NC_SMC_FAN_2_TACH
SMC_FAN_3_CTL — NC_SMC_FAN_3_CTL
SMC_FAN_3_TACH — NC_SMC_FAN_3_TACH
=CHGR_ACOK — SMC_BC_ACOK
=SMC_SMS_INT — SMS_INT_L
SMC_ADC0 — SMC_CPU_VSENSE
SMC_ADC1 — SMC_CPU_ISENSE
SMC_ADC2 — SMC_DCIN_VSENSE
SMC_ADC3 — SMC_DCIN_ISENSE
SMC_ADC4 — SMC_GFX_VSENSE
SMC_ADC5 — SMC_GFX_ISENSE
SMC_ADC6 — SMC_1V553_ISENSE
SMC_ADC7 — SMC_CPUVCCIO_ISENSE
SMC_ADC8 — SMC_LCDBKLT_ISENSE
SMC_ADC9 — SMC_WLAN_ISENSE
SMC_ADC10 — SMC_HDD_ISENSE
SMC_ADC11 — SMC_PBUS_VSENSE
SMC_ADC12 — SMC_BMON_ISENSE
(all MAKE_BASE=TRUE)

SMC_ADC13 — TP_SMC_ADC13
SMC_ADC15 — TP_SMC_ADC15
SMC_P10 — TP_SMC_P10
SMC_P20 — TP_SMC_P20
SMC_P24 — TP_SMC_P24
SMC_P26 — SMC_BMON_MUX_SEL
SMC_P43 — TP_SMC_P43
SMC_PF5 — TP_SMC_PF5
SMC_RSTGATE_L — TP_SMC_RSTGATE_L
(all MAKE_BASE=TRUE)

PROCHOT Level Shifting to 3V3



Debug Power "Buttons"



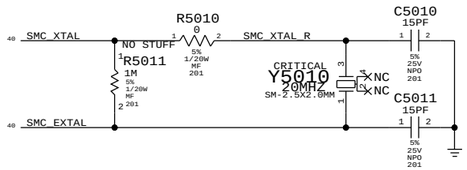
Check with SMC pullup S0

MEM_EVENT_L — R5075 10K 5% 1/20W MF 201 — =PP3V3_S0_SMC

Check with SMC pullup S5

SMC_ONOFF_L — R5070 10K
G3_POWERON_L — R5072 10K
SMC_LID — R5071 100K
SMC_TX_L — R5073 10K
SMC_RX_L — R5074 100K
SMC_TMS — R5077 10K
SMC_TDO — R5078 10K
SMC_TDI — R5079 10K
SMC_TCK — R5080 10K
SMC_BIL_BUTTON_L — R5081 10K
SMC_BC_ACOK — R5087 470K
SMS_INT_L — R5093 10K
(NOSTUFF)
SMC_PA0_PU — R5091 100K
SMC_RUNTIME_SCI_L — R5094 100K
(NOSTUFF)
SMC_ADAPTER_EN — R5085 10K
SMC_CASE_OPEN — R5086 10K
SMC_PB4 — R5088 10K
SMC_S4_WAKESRC_EN — R5090 100K
(all 5% 1/20W MF 201; =PP3V3_S5_SMC)

SMC Crystal Circuit



Q5020 (DP_A_EXT_HPD)

=PP3V3_S4_SMC
R5020 100K 5% 1/20W MF 201
SMC_DP_HPD_L
Q5020 SSM3K15FV SOD-VESM-HF
DP_A_EXT_HPD

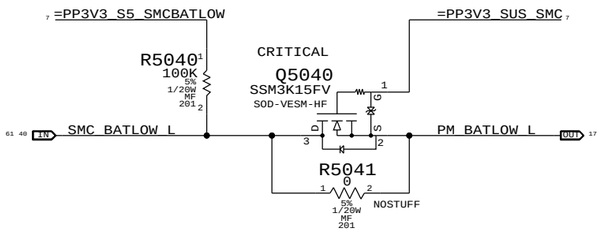
R5076 (SMC_PME_S4_WAKE_L)

=PP3V3_S4_SMC
R5076 100K 5% 1/20W MF 201
SMC_PME_S4_WAKE_L
MAKE_BASE=TRUE

R5012 (PM_CLK32K_SUSCLK_R → SMC_CLK32K)

R5012 22 5% 1/20W MF 201
PLACE_NEAR=U1800.N14:5.1mm

BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

Below connections are different from K91

SMC_PA0_PU — HISIDE_ISENSE_OC
SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
SMC_ADC14 — SMC_HS_COMPUTING_ISENSE
SMC_GFX_THROTTLE_L — TP_SMC_GFX_THROTTLE_L
(all MAKE_BASE=TRUE)

SMC_GFX_OVERTEMP_L — R5095 10K 5% 1/20W MF 201 — =PP3V3_S5_SMC

SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2010
PAGE TITLE: SMC Support
Apple Inc.
DRAWING NUMBER: 051-8871
SIZE: D
REVISION: 2.5.0
BRANCH:
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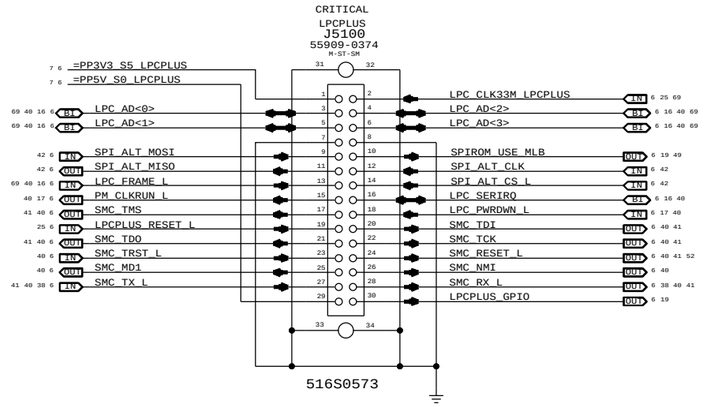
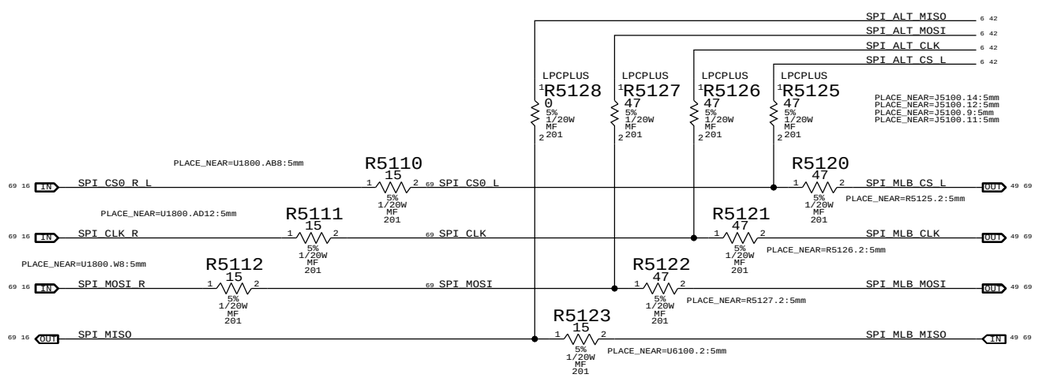
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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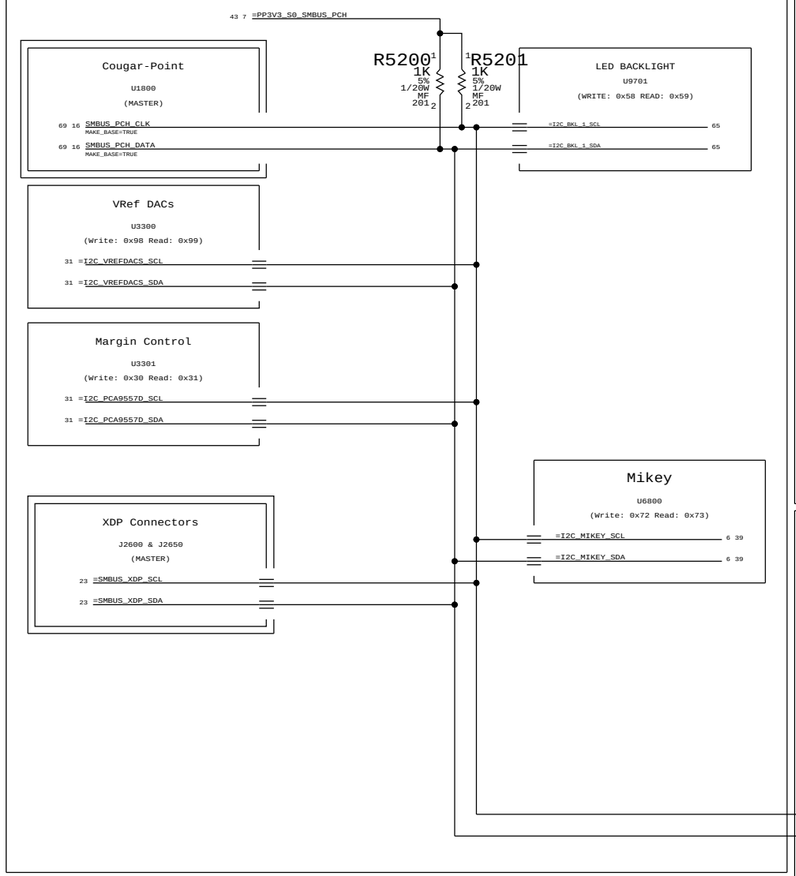
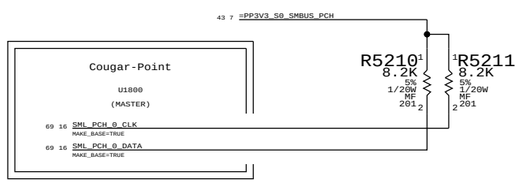
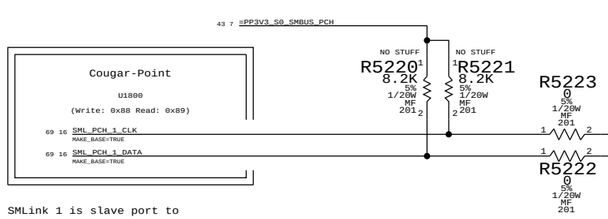
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

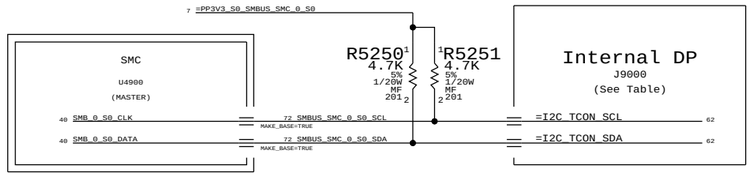


PCH "SMLink 1" Connections



SMLink 1 is slave port to
access PCH & CPU via PECI.

SMC "0" SMBus Connections



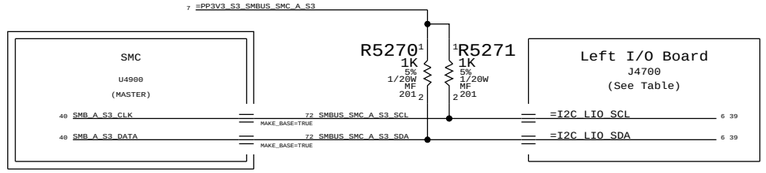
(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "A" SMBus Connections

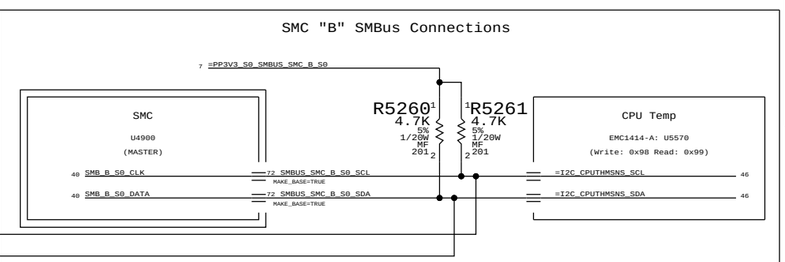
NOTE: SMC RMT bus remains powered and may be active in S3 state



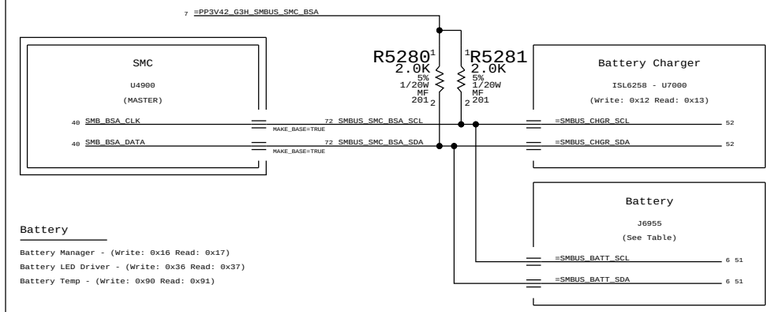
Left I/O Board

ALS - (write: 0x72 Read: 0x73)
Finstack Temp - (Write: 0x92 Read: 0x93)

SMC "B" SMBus Connections



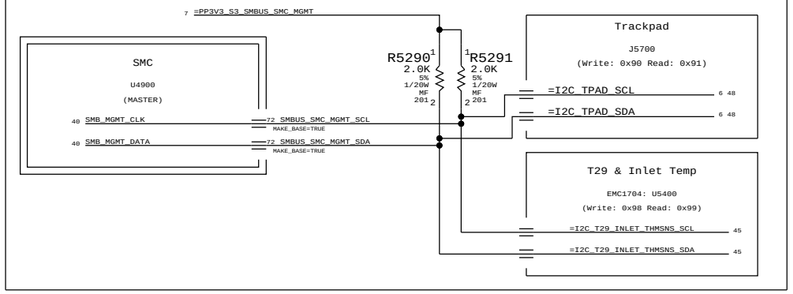
SMC "Battery A" SMBus Connections



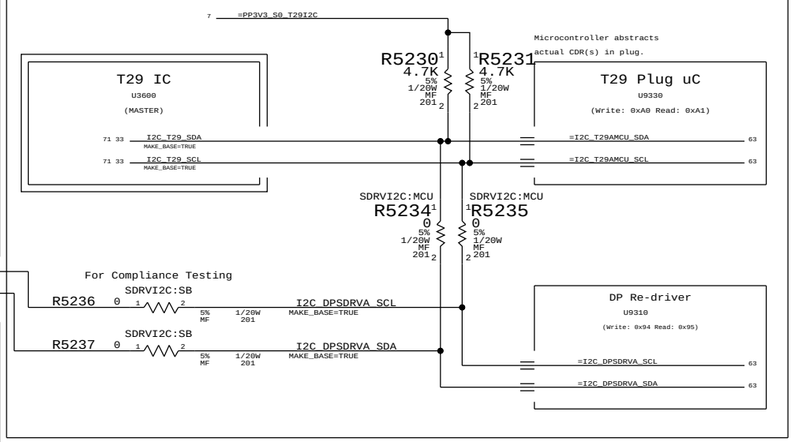
Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections



T29 I2C Connections



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
SMBus Connections

Apple Inc.

DRAWING NUMBER 051-8871
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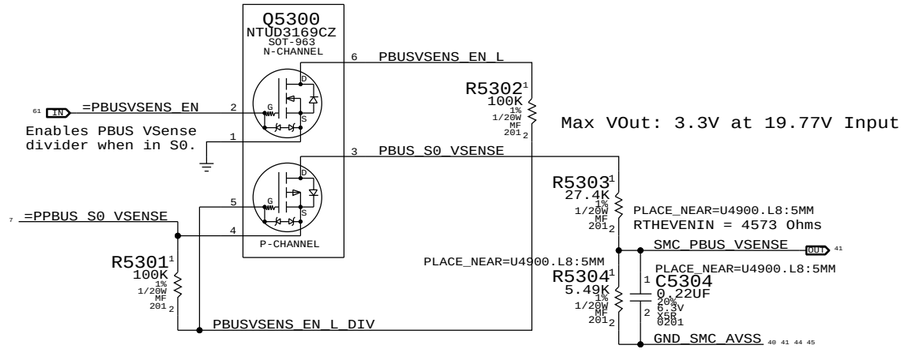
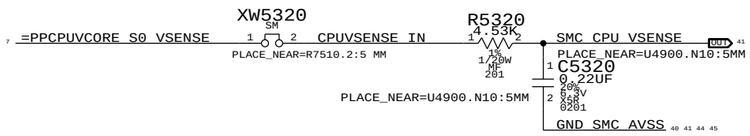
PBUS Voltage Sense Enable & Filter

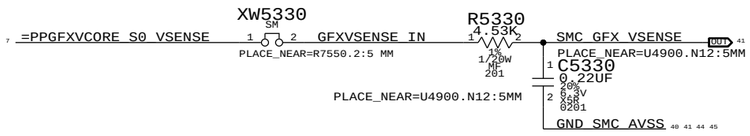


DC-In Voltage Sense Enable & Filter

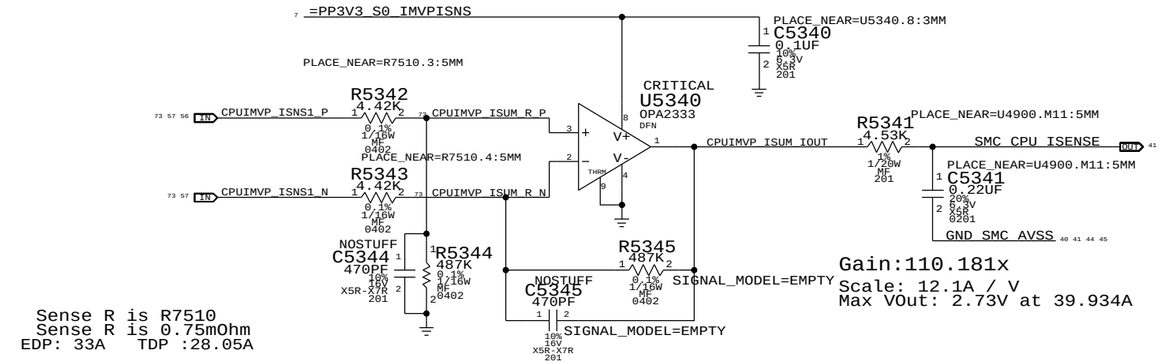
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter

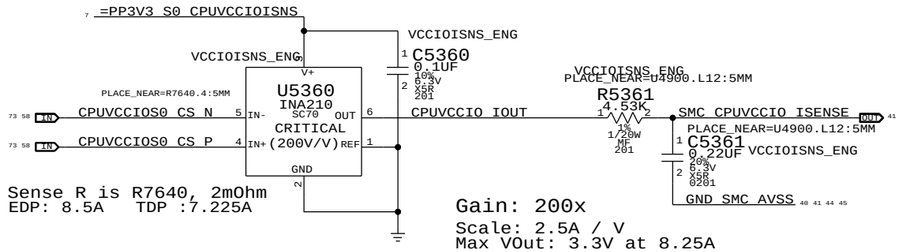


CPU VCore Load Side Current Sense / Filter



GFX/IG VCore Load Side Current Sense / Filter

CPU 1.05V VCCIO Current Sense / Filter



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH:

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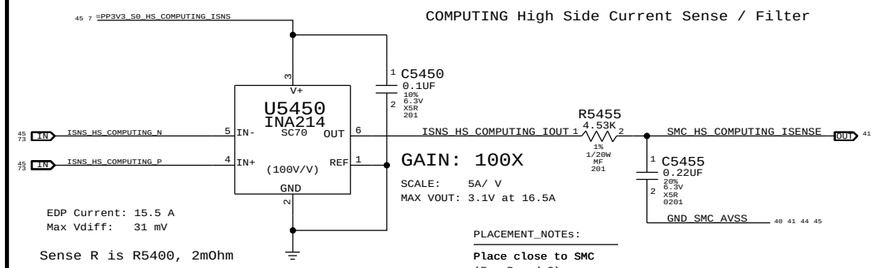
COMPUTING High Side Current Sense / Filter

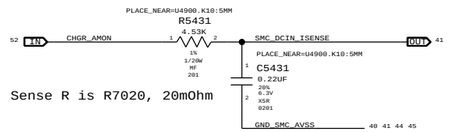


EDP Current: 15.5 A
Max Vdiff: 31 mV

Sense R is R5400, 2mOhm

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

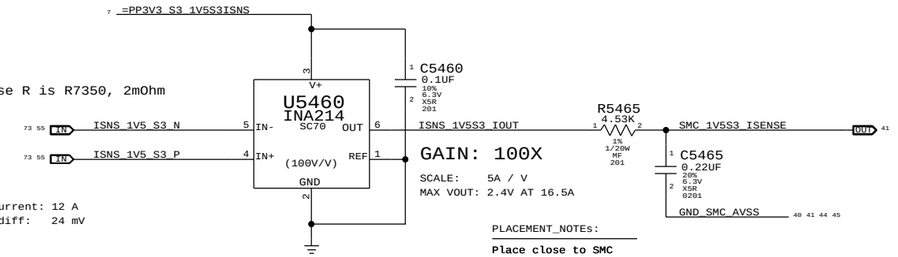
DC-IN (AMON) Current Sense Filter



Sense R is R7020, 20mOhm

DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max VOut: 1.4V at 8.25A
EDP Current: 3.5A

DDR3 1V5R1V35 Current Sense / Filter

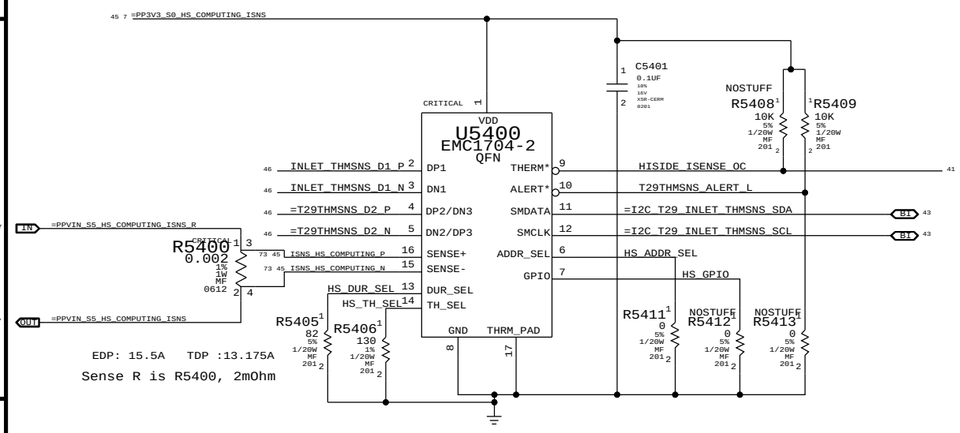


Sense R is R7350, 2mOhm

EDP Current: 12 A
Max Vdiff: 24 mV

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

COMPUTING High Side Current Sense / Filter & T29/Inlet Temp Sensor

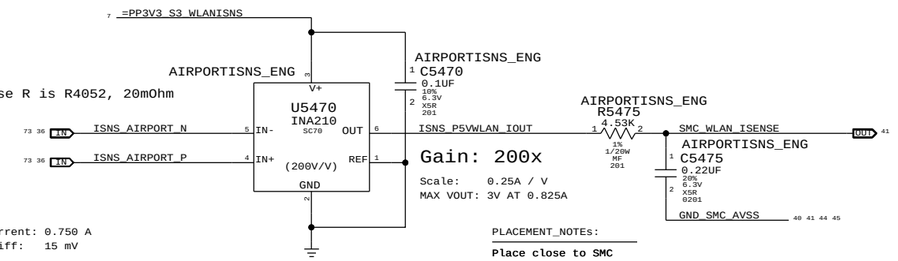


EDP: 15.5A TDP :13.175A

Sense R is R5400, 2mOhm

Write Address: 0x98
Read Address: 0x99

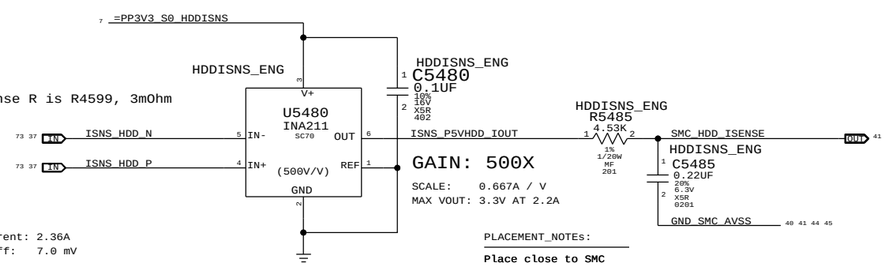
AirPort Current Sense / Filter



EDP Current: 0.750 A
Max Vdiff: 15 mV

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

HDD Current Sense / Filter

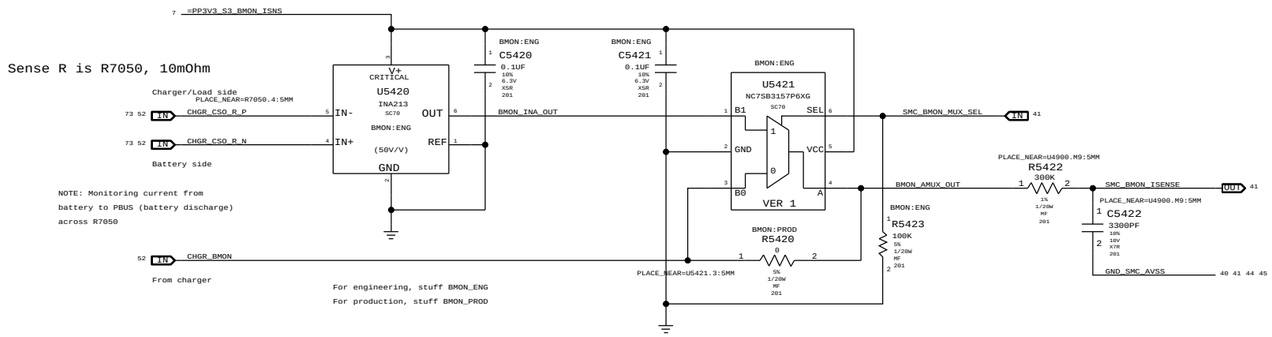


Sense R is R4599, 3mOhm

EDP Current: 2.36A
Max Vdiff: 7.0 mV

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



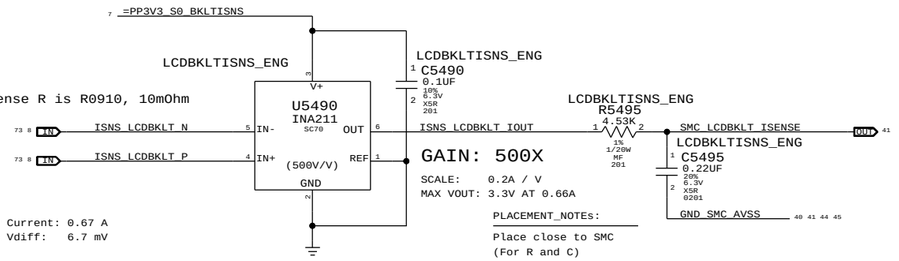
Sense R is R7050, 10mOhm

NOTE: Monitoring current from battery to PBUS (battery discharge) across R7050

INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A
EDP Current: 10A

Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A
EDP Current: 310A

LCD Backlight Driver Input Current Sense / Filter



EDP Current: 0.67 A
Max Vdiff: 6.7 mV

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
High Side Current Sensing

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D
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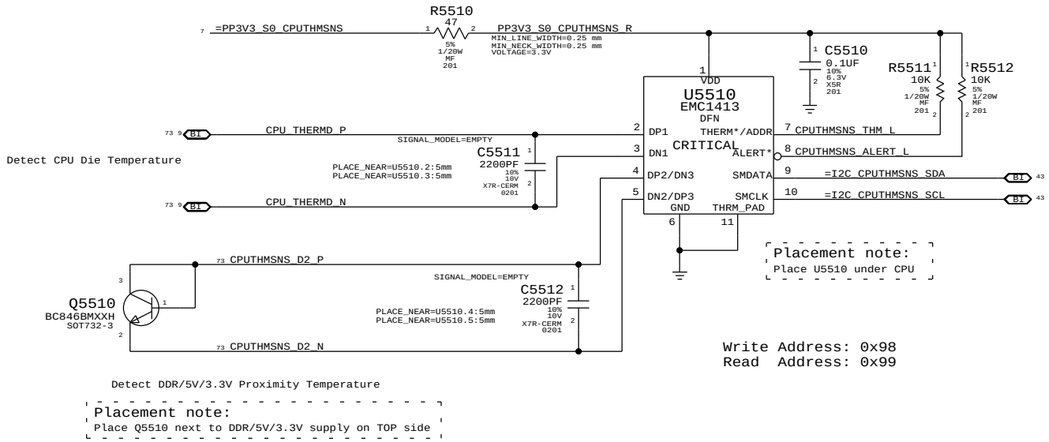
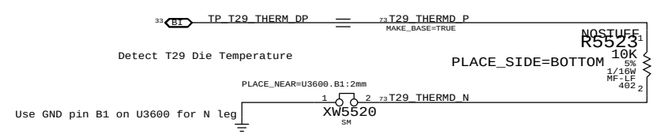
CPU Proximity Sensor



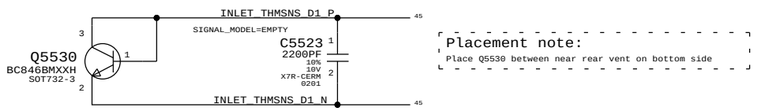
T29 Die

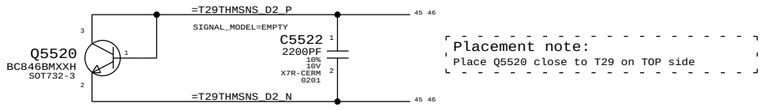


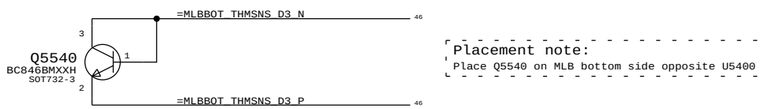
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

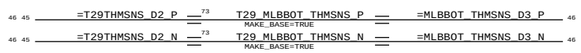
Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors









SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

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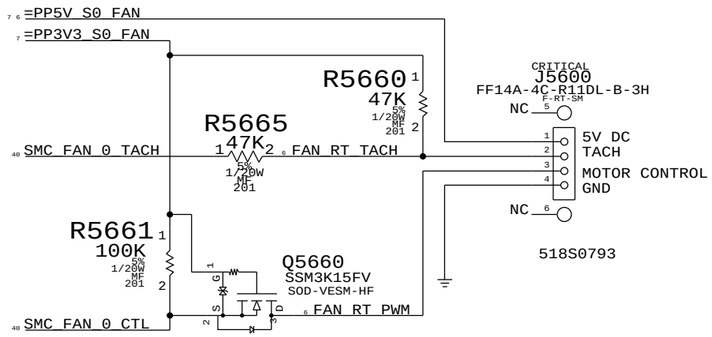
FAN CONNECTOR



SYNC MASTER=K21_MLB	SYNC DATE=12/13/2010
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: 051-8871 SIZE: D
	REVISION: 2.5.0
	BRANCH:
	PAGE: 56 OF 109
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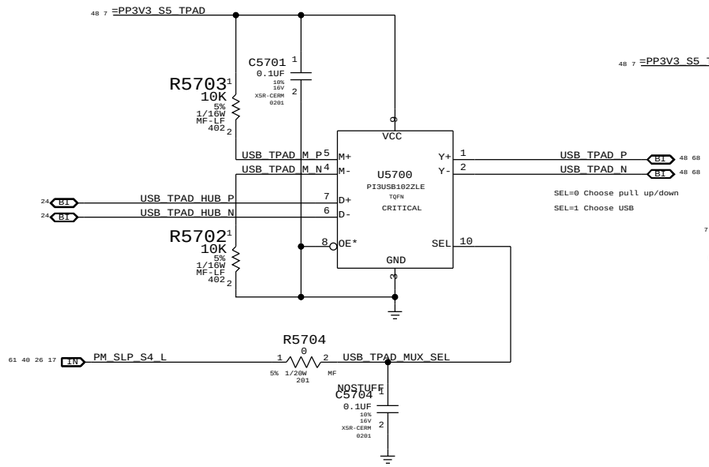
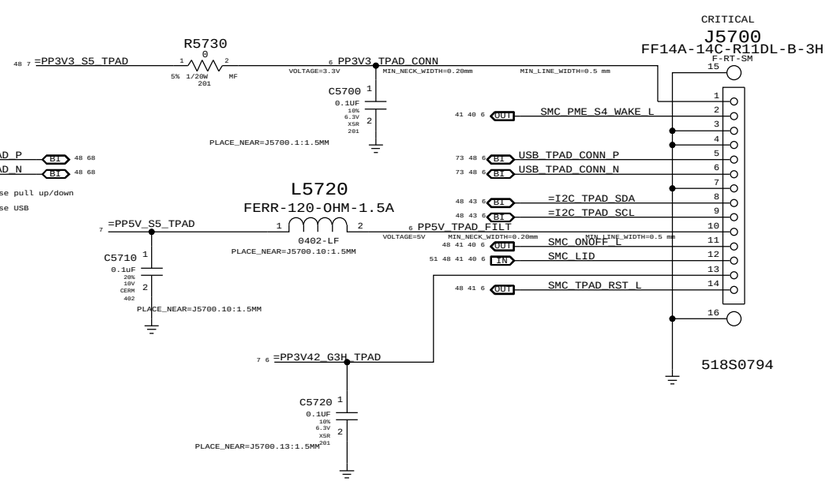
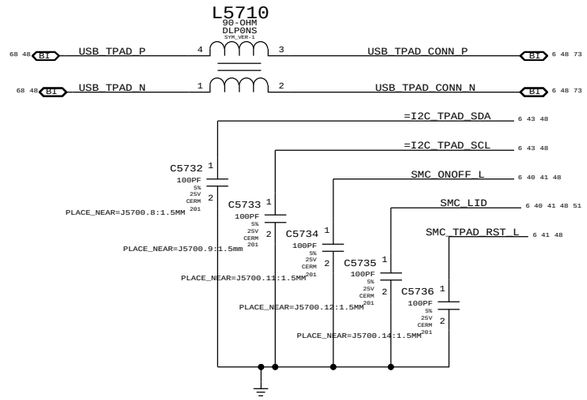
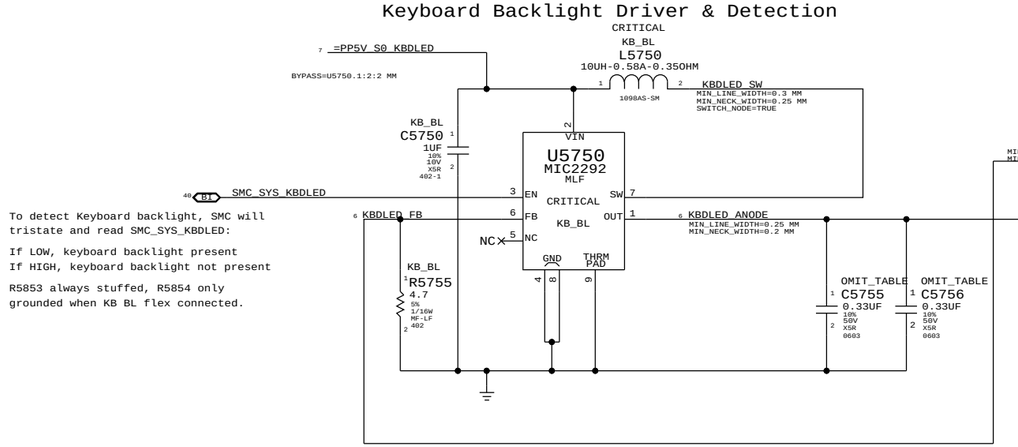
IPD Flex Connector







Keyboard Backlight Driver & Detection

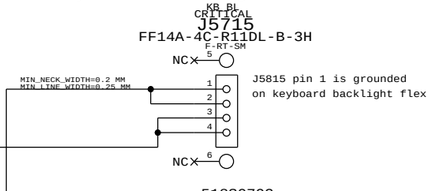


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP,CER,0.22UF,10%,50V,XSR,0603	C5756,C5755		KB_BL

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: IPD / KBD Backlight

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

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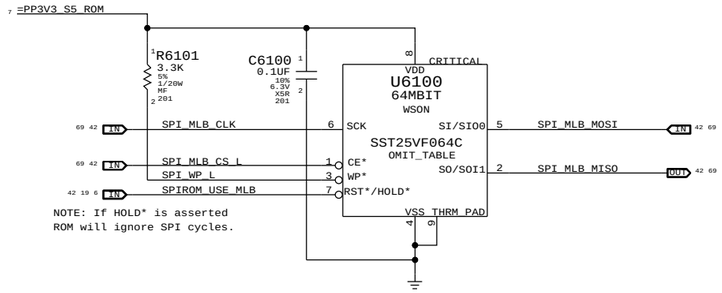

SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE: SPI ROM	
Apple Inc.	DRAWING NUMBER: 051-8871 SIZE: D
	REVISION: 2.5.0
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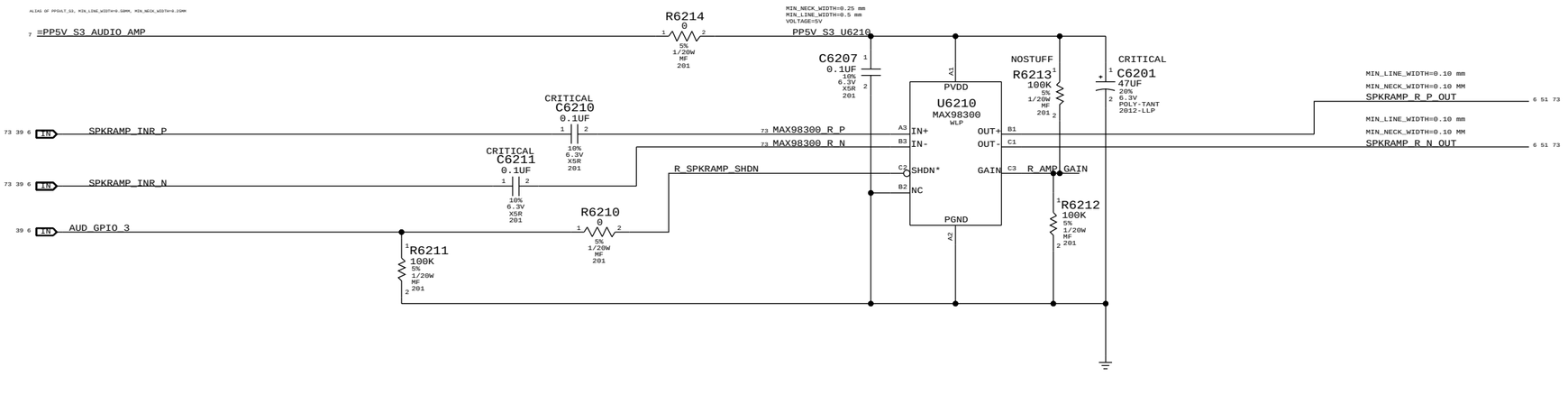
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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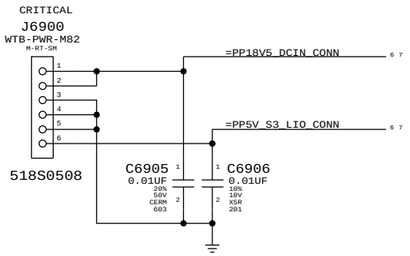
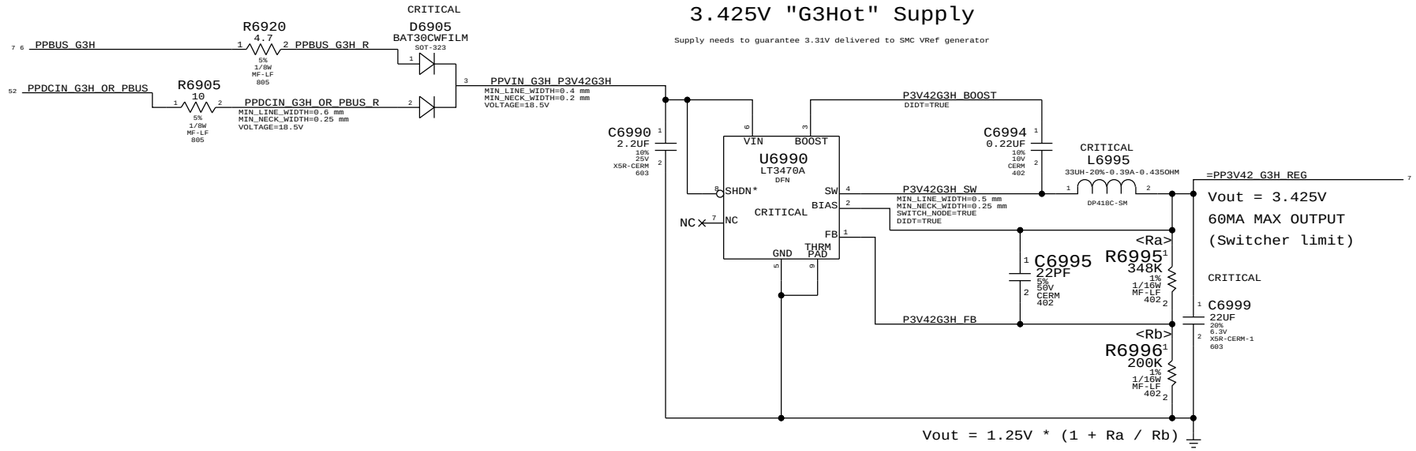
MLB to LIO Power Cable Connector



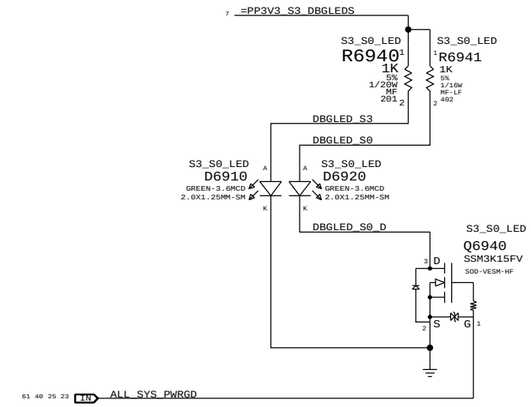
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

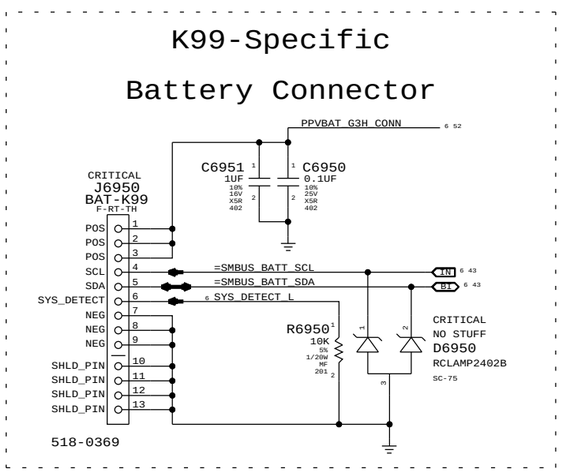


Debug LEDs

(For development only)



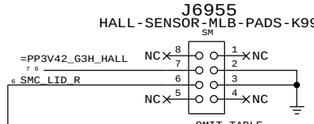
K99-Specific Battery Connector



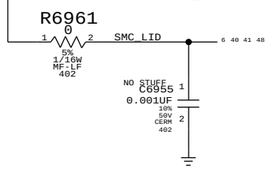
J6955

HALL-SENSOR-MLB-PADS-K99

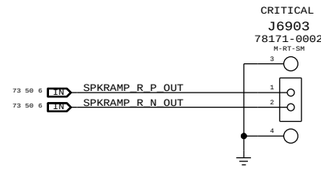
SM



518-0369



Right Speaker Connector



518S0519

SYNC_MASTER=K21_MLB SYNC_DATE=11/11/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH:

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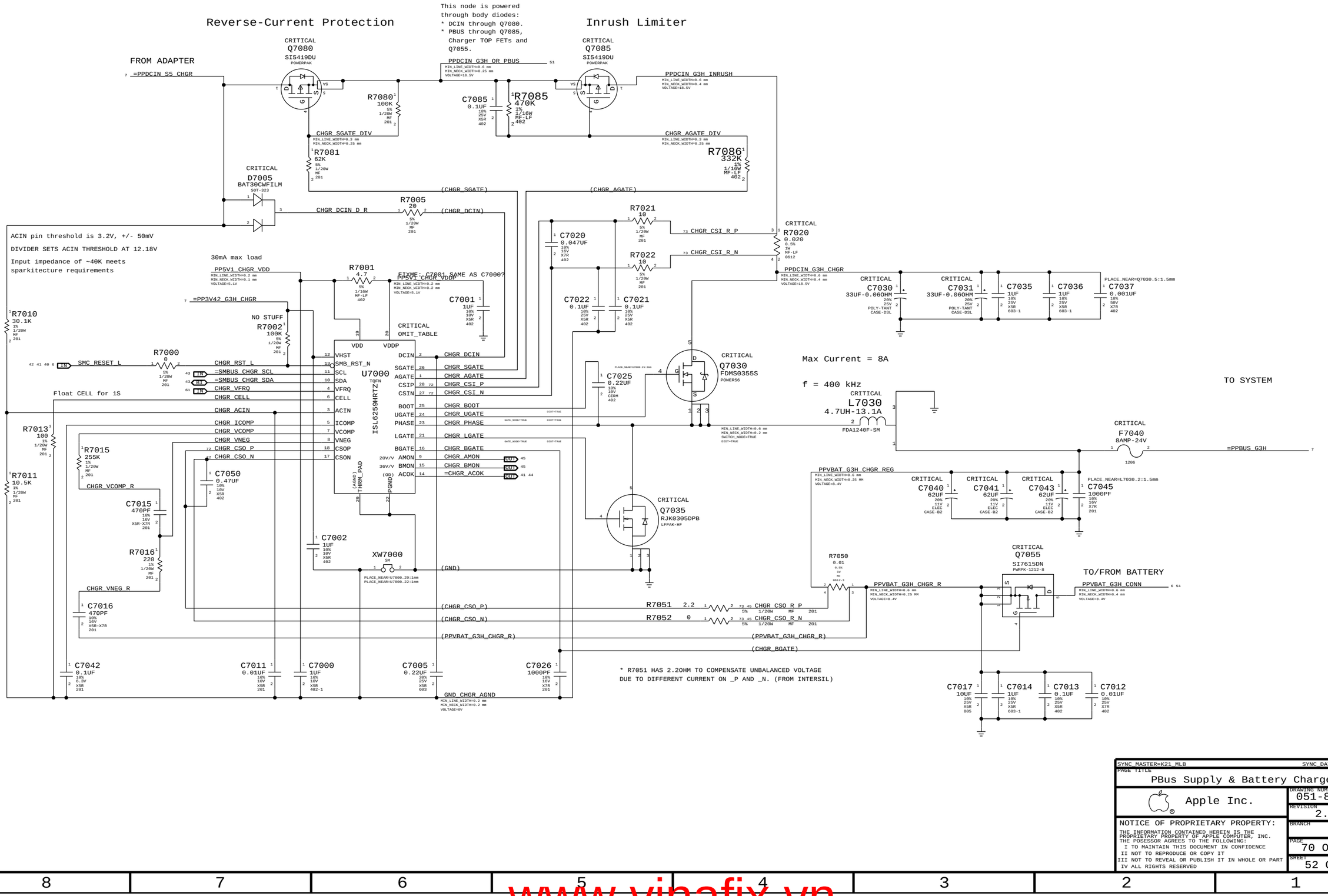

SYNC_MASTER=K21_MLB SYNC_DATE=11/30/2010

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

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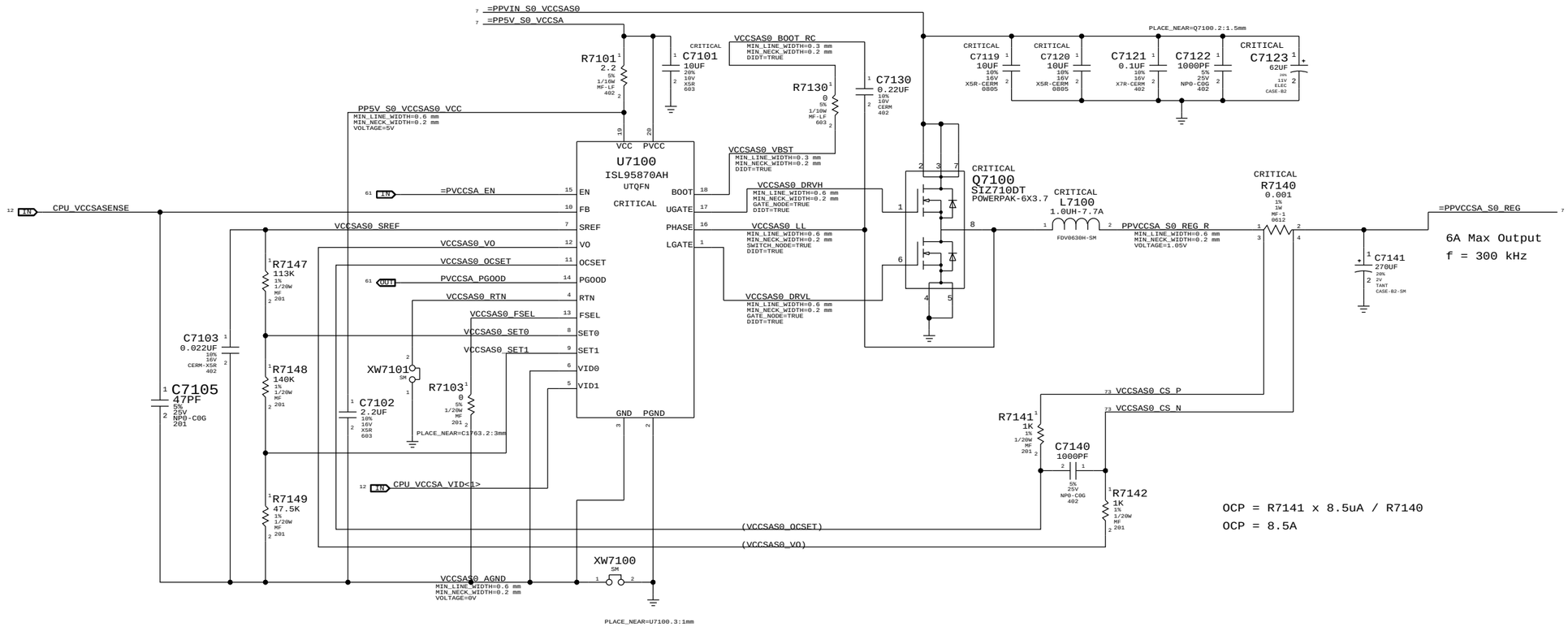

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH:

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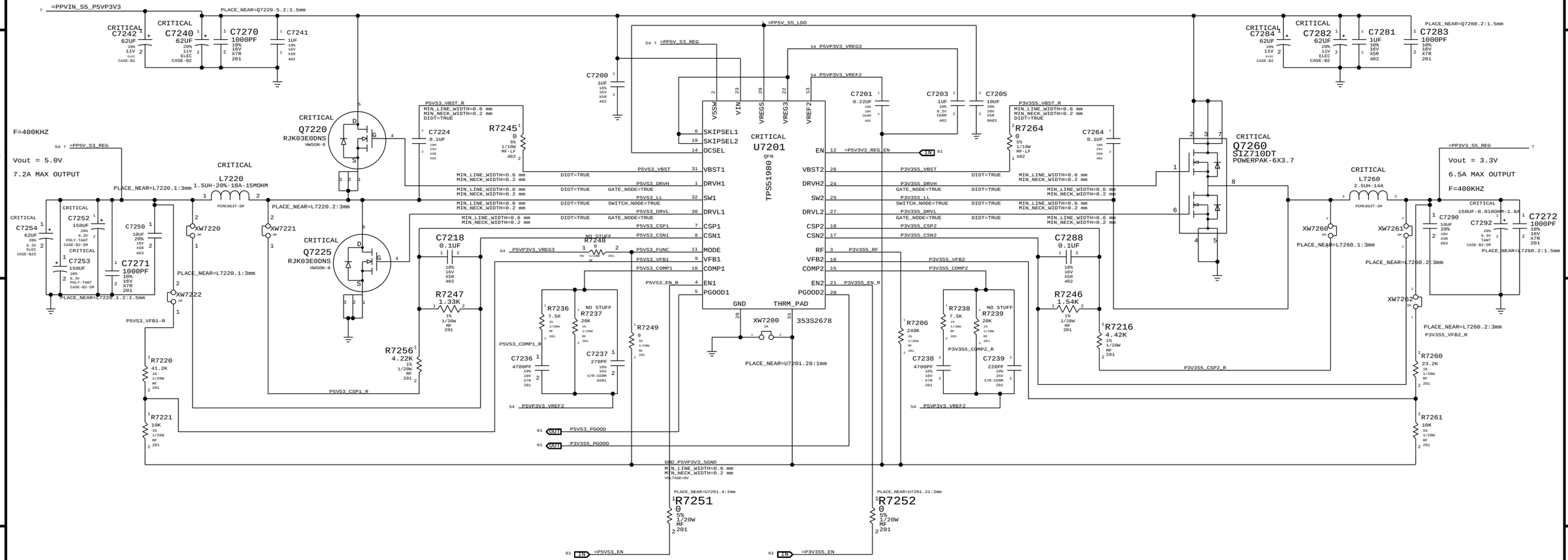
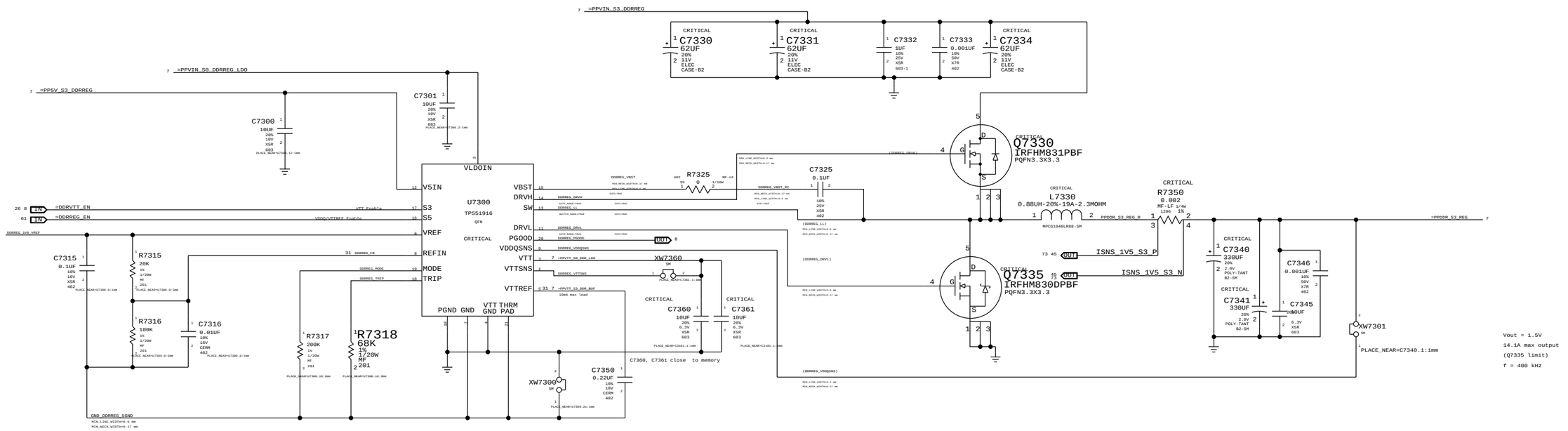


SYNC_MASTER=K21_MLB	SYNC_DATE=11/30/2010
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-8871 · SIZE D
	REVISION 2.5.0
	BRANCH
	PAGE 72 OF 109
	SHEET 54 OF 74



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

BRANCH

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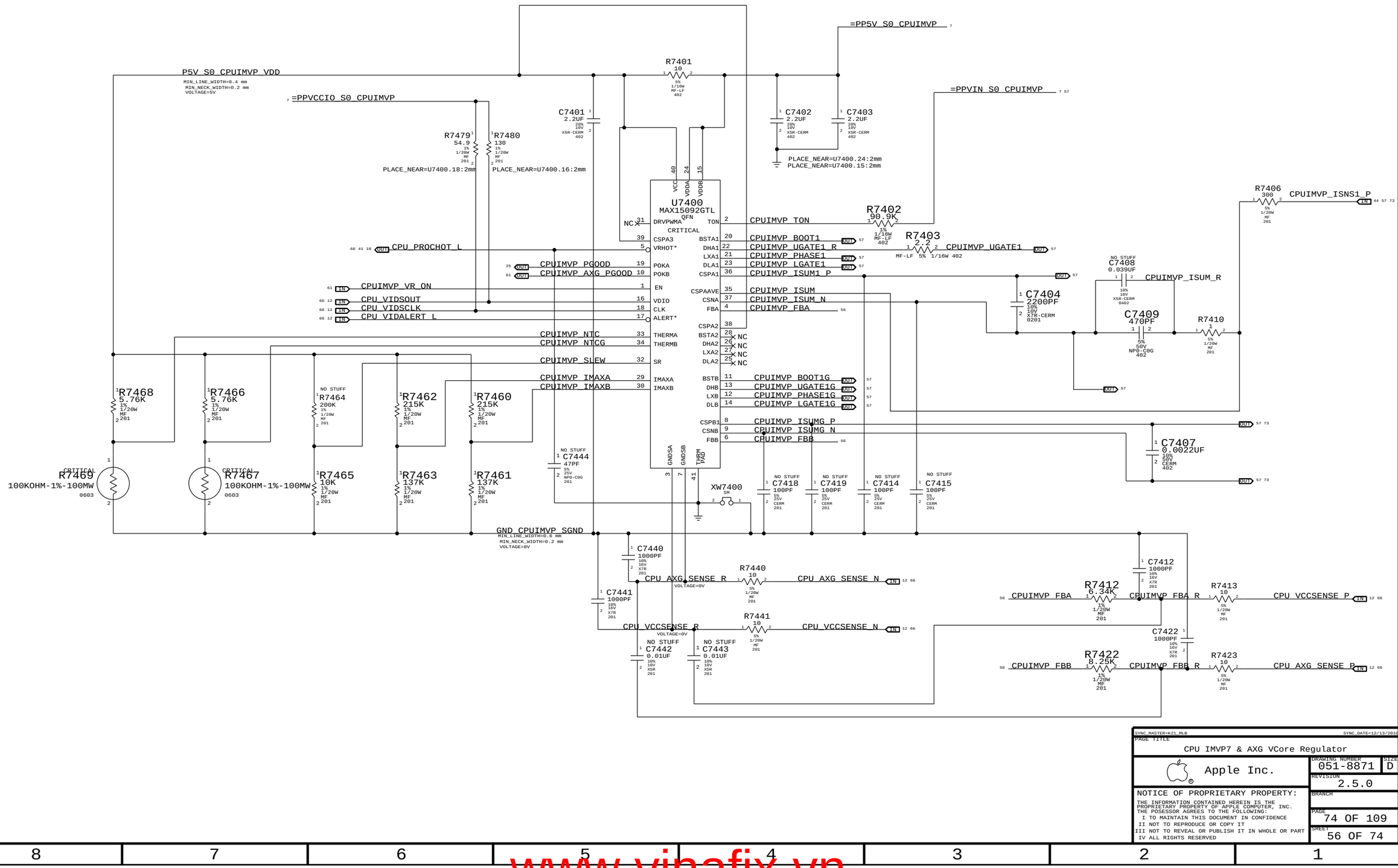

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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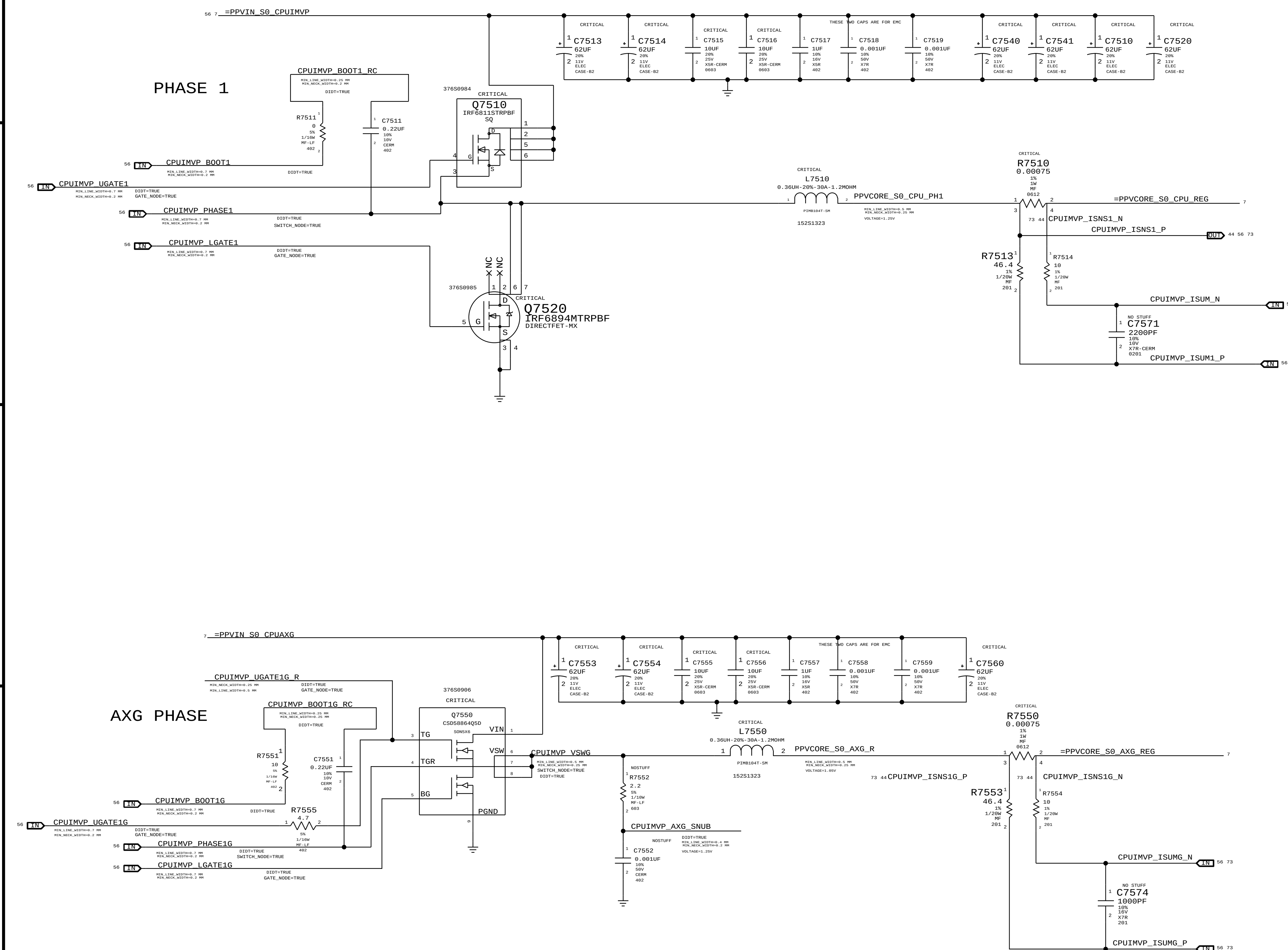
CPU=Sandy Bridge ULV, AXG=GT2



CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER	051-8871
SIZE	D
REVISION	2.5.0
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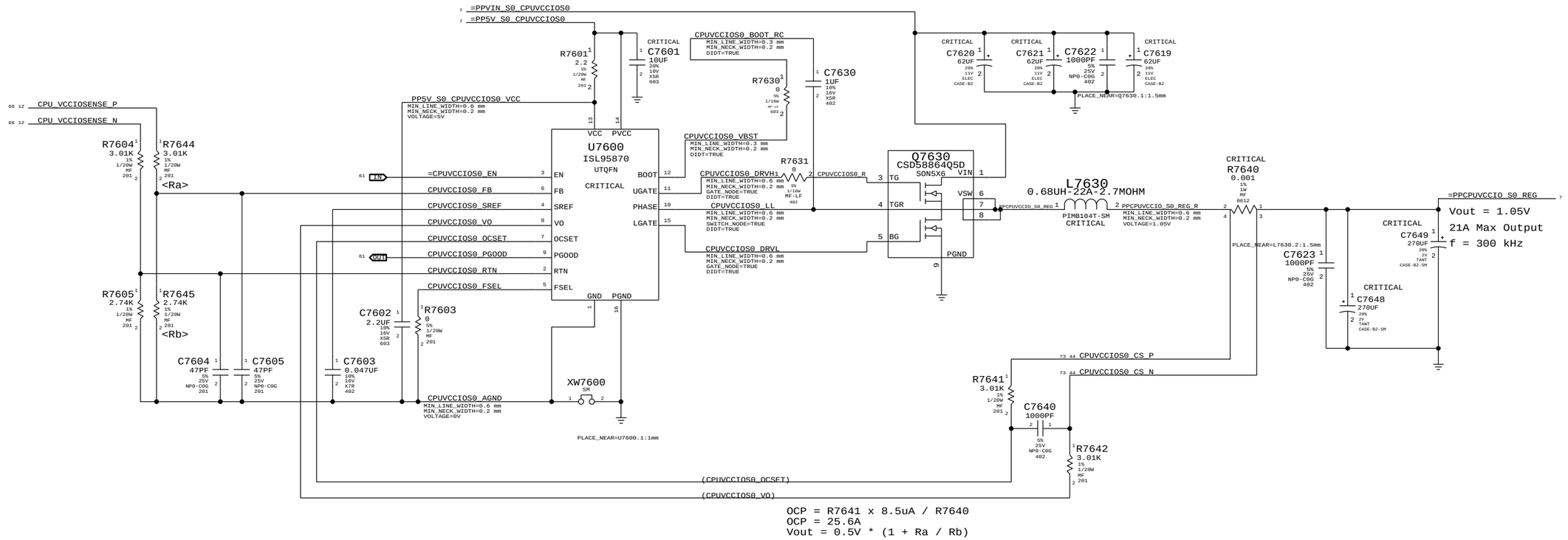
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

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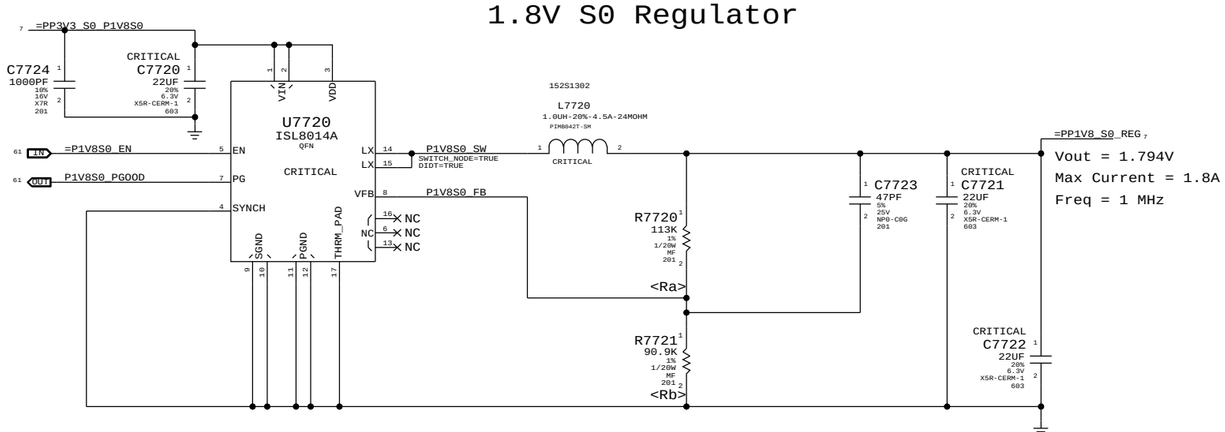
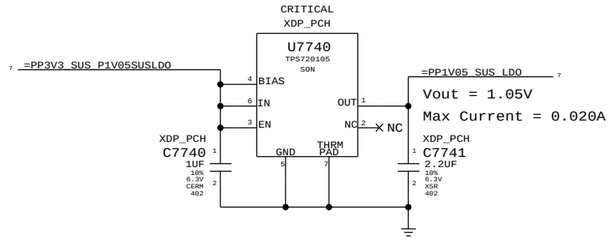
1.8V S0 Regulator



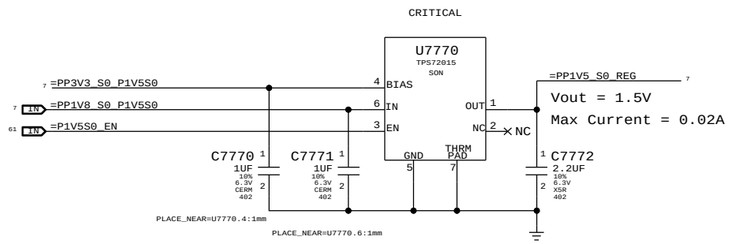
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

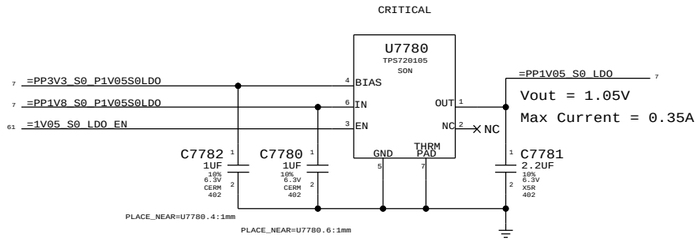
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D
REVISION: 2.5.0
BRANCH:
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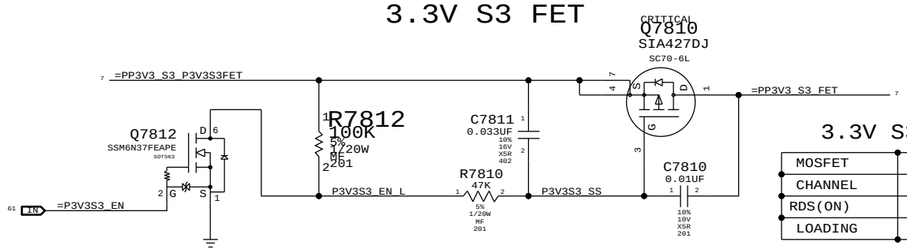
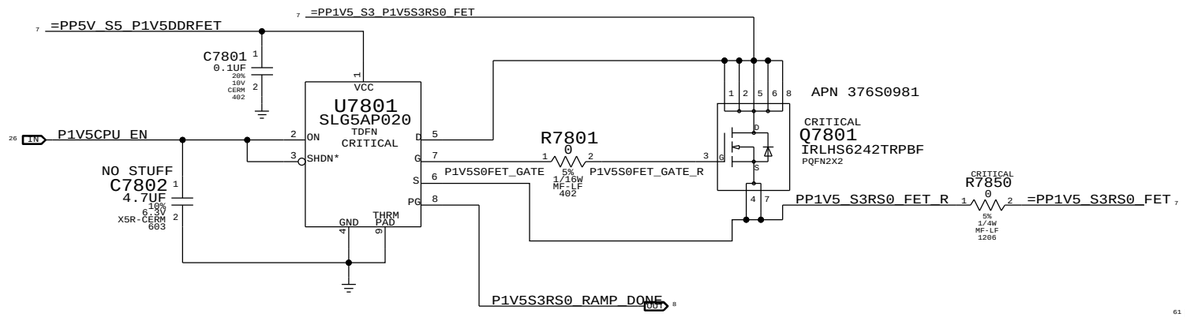
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

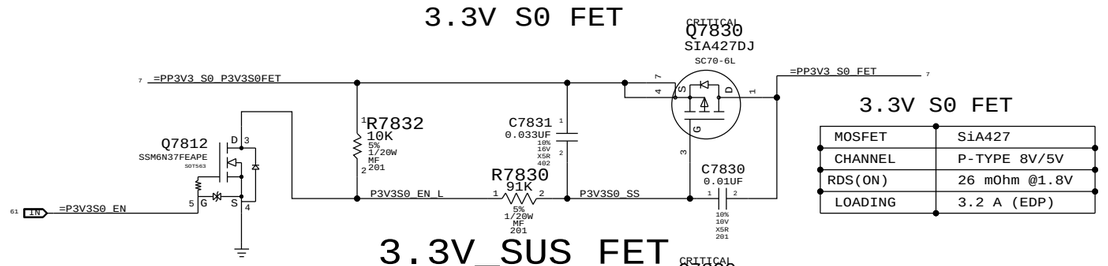
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

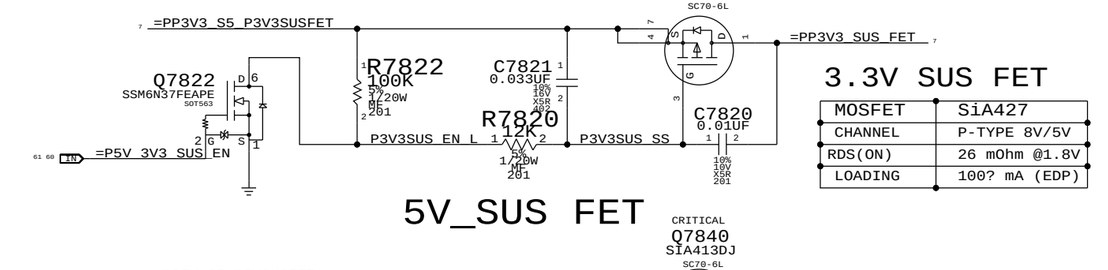
3.3V S0 FET



3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

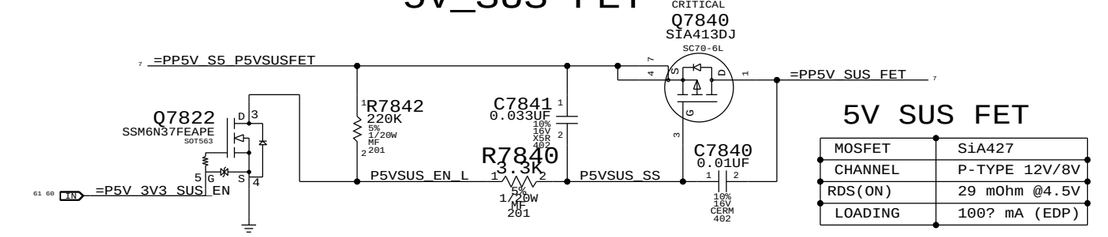
3.3V_SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

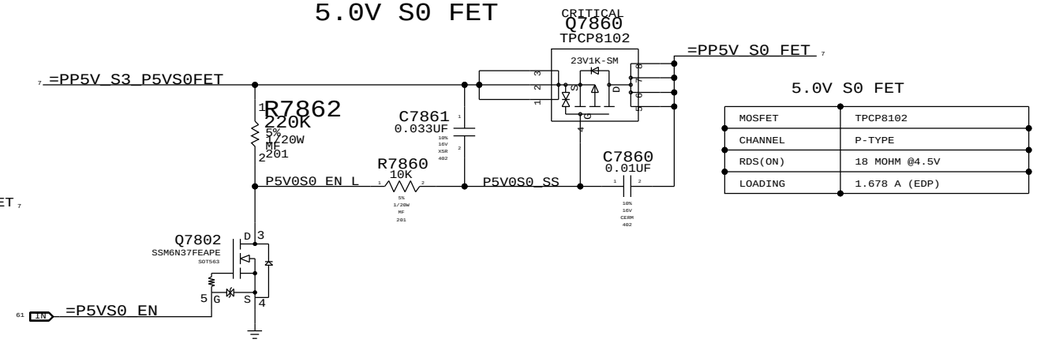
5V_SUS FET



5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K21 MLB SYNC DATE=12/13/2010

PAGE TITLE: Power FETs

Apple Inc.

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S5 Rail Enables & PGOOD

=PP3V42_G3H_PWRCTL

Internal pull-ups 100K +/- 20%

C7940 0.1UF 10% 6.3V X5R 201

U7941 SLG4AP012 TDFN

CRITICAL 343S0497

SMC_PM_G2_EN MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 10% 25V X7R-CERM 201

R7941 100 5% 1/20W MF 201

C7942 0.033UF 10% 16V X5R 402 NO STUFF

P3V3S5_EN MAKE_BASE=TRUE =P3V3S5_EN OUT 54

P5V3V3_REG_EN MAKE_BASE=TRUE =P5V3V3_REG_EN OUT 54

S5_PWRGD MAKE_BASE=TRUE OUT 40

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V S4 ENABLE

PM_SLP_S5_L

R7915 100K 5% 1/20W MF 201

Delete R when pull-down added to PCH page

3.3V,5V S3 ENABLE

Delete R when pull-down added to PCH page

PM_SLP_S4_L MAKE_BASE=TRUE

R7910 100K 5% 1/20W MF 201

R7913 0 5% 1/20W MF 201

P5VS3_EN MAKE_BASE=TRUE =P5VS3_EN OUT 54

PLACE_NEAR=U7300.16:6mm

R7911 5.1K 1% 1/20W MF 201

R7912 9.1K 1% 1/20W MF 201

NO STUFF C7913 0.068UF 10% 16V CERM 402

PLACE_NEAR=Q7812.2:6mm

P3V3S3_EN MAKE_BASE=TRUE =P3V3S3_EN OUT 60

DDRREG_EN MAKE_BASE=TRUE =DDRREG_EN OUT 55

=USB_PWR_EN OUT 6 38 39

PLACE_NEAR=U7300.16:6mm C7910 0.47UF 10% 6.3V CERM-X5R 402

PLACE_NEAR=Q7812.2:6mm C7912 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD

R7974 0 5% 1/20W MF 201

PLACE_NEAR=U7400.1:5mm

CPUIMVP_VR_ON OUT 56

PLACE_NEAR=U7400.1:5mm

R7976 0 5% 1/20W MF 201

NO STUFF

PLACE_NEAR=U7400.1:5mm

CPUVCCIOS0_PGOOD R7975 0 5% 1/20W MF 201 PM_PECI_PWRGD OUT 40

S0 ENABLE

PM_SLP_S3_L

R7978 100 5% 1/20W MF 201

R7979 100K 5% 1/20W MF 201

PLACE_NEAR=U1800.04:5mm

Delete R when pull-down added to PCH page

(PM_SLP_S3_R_L)

PM_SLP_S3_R_L MAKE_BASE=TRUE

R7987 33K 5% 1/20W MF 201 PLACE_NEAR=U7100.15:6mm

R7981 20K 5% 1/20W MF 201 PLACE_NEAR=U7600.3:6mm

R7988 39K 1% 1/20W MF 201 PLACE_NEAR=U7770.3:6mm

R7986 5.1K 5% 1/20W MF 201 PLACE_NEAR=U7720.5:6mm

=P5VS0_EN OUT 60

=P3V3S0_EN OUT 60

=PBUSVSENS_EN OUT 44

P1V8S0_EN MAKE_BASE=TRUE =P1V8S0_EN OUT 59

P1V5S0_EN MAKE_BASE=TRUE =P1V5S0_EN OUT 59

=1V05_S0_LDO_EN OUT 59

CPUVCCIOS0_EN MAKE_BASE=TRUE =CPUVCCIOS0_EN OUT 58

PVCCSA_EN MAKE_BASE=TRUE =PVCCSA_EN OUT 53

C7987 0.47UF 10% 6.3V CERM-X5R 402

C7981 0.47UF 10% 6.3V CERM-X5R 402

C7988 0.47UF 10% 6.3V CERM-X5R 402

C7986 0.47UF 10% 6.3V CERM-X5R 402

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON

=PP3V3_S5_VMON

R7956 150K 1% 1/20W MF 201

R7951 15K 1% 1/20W MF 201

R7953 1K 5% 1/20W MF 201

VMON_3V3_DIV

VMON_Q2_BASE

S0PGD_C

R7952 7.15K 1% 1/20W MF 201

R7954 1K 5% 1/20W MF 201

=PP1V5_S3RS0_VMON

PP1V5_S3RS0

VMON_Q3_BASE

NC

Q7950 ASMCC0179 DFN2015H4-8

CRITICAL

NC

R7955 1K 5% 1/20W MF 201

=PP1V05_S0_VMON

VMON_Q4_BASE

353S2809 S0PGD_BJT_GND_R

R7957 100 5% 1/20W MF 201

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL

PLACE_NEAR=U7940.5:2.3mm

C7943 0.1UF 10% 6.3V X5R 201

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L

U7940 74AUP1G3208 SOT891

ALL_SYS_PWRGD

PM_SLP_SUS_L

PM_SUS_EN MAKE_BASE=TRUE =P5V_3V3_SUS_EN OUT 60

PLACE_NEAR=U1800.A15:5mm

R7918 100K 5% 1/20W MF 201

Delete R when pull-down added to PCH page

NO STUFF R7917 0 5% 1/20W MF 201

CHGR VFRQ Generation

=PP3V42_G3H_PWRCTL

R7931 10K 5% 1/20W MF 201

CHGR_VFRQ OUT 52

Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

3.3V SUS Detect

=PP3V3_S5_PWRCTL

PLACE_NEAR=U7930.6:2.3mm

No stuff C7931, 12ms Min delay time, U7930 Sense input threhold is 3.07v

C7930 0.1UF 10% 6.3V X5R 201

=PP3V3_SUS_PWRCTL

R7933 100K 5% 1/20W MF 201

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 (90K IN)

=PP3V3_SUS_PWRCTL

PM_RSMRST

PM_RSMRST_L goes to U1800.C21

C7931 1000PF 10% 16V X7R 201 NO STUFF

S0 Rail PGOOD Circuitry

(ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

P1V5S0_PGOOD from U7710

=PP5V_S0_VMON

=PP3V3_S0_VMON

=PP1V5_S3RS0_VMON

=PP1V05_S0_VMON

S0PGOOD_ISL

R7960 6.04K 1% 1/20W MF 201

R7970 10K 1% 1/20W MF 201

R7972 6.04K 1% 1/20W MF 201

C7960 0.1UF 10% 6.3V X5R 201

U7960 ISL88042IRTEZ TDFN (TPU) CRITICAL

P5V_DIV_VMON

P1V5_DIV_VMON

P1V05_DIV_VMON

R7961 15K 1% 1/20W MF 201

R7971 10K 1% 1/20W MF 201

R7973 15K 1% 1/20W MF 201

NC

ALL_SYS_PWRGD_R

353S2310

R7967 10K 5% 1/20W MF 201

NO STUFF R7968 100 5% 1/20W MF 201

CPUIMVP_AXG_PGOOD

R7966 100 5% 1/20W MF 201

P1V8S0_PGOOD

R7965 100 5% 1/20W MF 201

P3V3S5_PGOOD

R7901 100 5% 1/20W MF 201

P5VS3_PGOOD

R7964 100 5% 1/20W MF 201

CPUVCCIOS0_PGOOD

R7963 100 5% 1/20W MF 201

PVCCSA_PGOOD

R7962 330 5% 1/20W MF 201

ALL_SYS_PWRGD OUT 23 25 40 51 61

DP S4 Power Enable

SMC_S4_WAKESRC_EN MAKE_BASE=TRUE =DPAPWRSW_EN OUT 64

PSOC USB Power Enable

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L OUT 36

Q7925 2N7002DW-X-G SOT-363

AP_PWR_EN

(AC_EN_L)

AC_EN_L

Q7920 2N7002DW-X-G SOT-363

NO STUFF R7929 0 5% 1/20W MF 201

SMC_ADAPTER_EN

(PM_SLP_S3_L)

PM_SLP_S3_L

Q7925 2N7002DW-X-G SOT-363 NC

Unused fet

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CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

CRITICAL
U9000
FPF1009
MFET-2X2-8IN

7 =PP3V3_S5_LCD
8 IN LCD_IG_PWR_EN
ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9014 1K 5% 1/20W MF 201
C9009 0.1UF 10% 6.3V X5R 201
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603

R9061 0 5% 1/20W MF 201
43 BI =I2C_TCON_SDA
6 I2C_TCON_SDA_R

R9062 0 5% 1/20W MF 201
43 IN =I2C_TCON_SCL
6 I2C_TCON_SCL_R

Pull-ups on panel side,
4.7 kOhm to 3.3V

9 OUT DP_INT_HPD
R9060 0 5% 1/20W MF 201
6 DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

C9015 1000PF 10% 16V X7R 201
R9070 100K 5% 1/20W MF 201

6 PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

C9024 0.1UF 10% 16V X5R-CERM 0201
C9025 0.1UF 10% 16V X5R-CERM 0201
C9020 0.1UF 10% 16V X5R-CERM 0201
C9021 0.1UF 10% 16V X5R-CERM 0201
C9022 0.1UF 10% 16V X5R-CERM 0201
C9023 0.1UF 10% 16V X5R-CERM 0201

69 9 BI DP_INT_AUX_CH_N
(DP_INT_AUX_CH_C_N)
69 9 BI DP_INT_AUX_CH_P
(DP_INT_AUX_CH_C_P)
69 9 IN DP_INT_ML_P<0>
DP_INT_ML_C_P<0>
69 9 IN DP_INT_ML_N<0>
DP_INT_ML_C_N<0>
69 9 IN DP_INT_ML_P<1>
DP_INT_ML_C_P<1>
69 9 IN DP_INT_ML_N<1>
DP_INT_ML_C_N<1>

CRITICAL
FL9000
12-OHM-100MA-8.5GHZ
TCM0806-4SM
SYM_VER-2

CRITICAL
FL9001
12-OHM-100MA-8.5GHZ
TCM0806-4SM
SYM_VER-2

R9050 100K 5% 1/20W MF 201
R9080 100K 5% 1/20W MF 201

65 6 PPVOUT_SW_LCDBKLT

65 6 OUT LED_RETURN_6
65 6 OUT LED_RETURN_5
65 6 OUT LED_RETURN_4
65 6 OUT LED_RETURN_3
65 6 OUT LED_RETURN_2
65 6 OUT LED_RETURN_1

69 6 DP_INT_AUX_CH_C_N
69 6 DP_INT_AUX_CH_C_P
69 6 DP_INT_ML_F_P<0>
69 6 DP_INT_ML_F_N<0>
69 6 DP_INT_ML_F_P<1>
69 6 DP_INT_ML_F_N<1>

PLACE_NEAR=J9000.24:1mm
PLACE_NEAR=J9000.25:1mm
R9018 1M 5% 1/20W MF 201
R9017 1M 5% 1/20W MF 201

PLACE_NEAR=J9000.3:2mm
C9017 1000PF 5% 50V C0G-CERM 603

LCD Connector
Internal DP Connector: 518S0787

CRITICAL
J9000
CABLINE-CA
F-RT-SM

NC
NC
NC

LED Backlight I/F
DisplayPort I/F

SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2010

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Internal DisplayPort Connector

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DP A Super-Driver

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

U9310 PS8301TQFN40GTR-A2 QFN

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

T29 A High-Speed Signals

T29 signals are P/N-swapped after AC caps to improve layout.

T29 Path Biasing

IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

U9390 PI3VEDP212 TQFN

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

U9330 LPC1112A HVQFN25

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

AUXCH Snoop Port, used by PS8301 during training.

I2C Addr: 0x26/0x27 (Wr/Rd)

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

P2R = Plug to Receptacle
R2P = Receptacle to Plug

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3.3V/HV Power MUX

Port A HV Power Switch

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	1A (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200k / RFLT = 2A
ILIM = 201k / RLIM = 957mA
TFLT = CCT * 38900
TSD = CCT * 1000000

Bleeder Resistor
2.5V / 249 ohm = 10mA
P = ~27mW

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

3.3V/HV MUXed

Blocking FET, off when Source >3.4V or HV_EN high.

3.3V Always

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

Port A 3.3V Power Switch

DP_PWR must be S4/S5 to support wake from T29 devices.

DisplayPort/T29 A Connector

Circuit threshold range: 2.877-2.941V (2.903V nominal)

T29: Unused

T29: TX_0

T29: LSX_R2P/P2R (P/N)

T29: TX_1

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

470k R's for ESD protection on AC-coupled signals.

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

F9700 3AMP-32V-467 603-HF BOTTOM

=PPBUS_S0_LCDBKLT → PPBUS_S0_LCDBKLT_FUSED (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V)

CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF

PPBUS_SW_LCDBKLT_PWR (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V) → 8 65

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

R9788 301K 1% 1/20W MF 201

C9782 0.1UF 10% 16V X5R 402

LCDBKLT_EN_DIV

R9789 147K 1% 1/20W MF 201

LCDBKLT_EN_L

Q9707 SSM6N15FEAPE SOT563

8 IN LCD_BKLT_EN

LCDBKLT_DISABLE

Q9707 SSM6N15FEAPE SOT563

25 IN BKLT_PLT_RST_L

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

7 =PP5V_S0_BKL

8 =PPBUS_SW_BKL

CRITICAL L9701 15UH-2.8A PIMB053T-SM

PPBUS_SW_LCDBKLT_PWR_SW (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=50V, SWITCH_NODE=TRUE, DIDT=TRUE)

PLACE_NEAR=L9701.2:3mm
CRITICAL D9701 SOD-123 RB160M-60G

PLACE_NEAR=U9701.A5:3mm

C9796 220PF 10% 50V X7R-CERM 402

CRITICAL C9797 10UF 10% 50V X5R 1210-1

CRITICAL C9799 10UF 10% 50V X5R 1210-1

PLACE_NEAR=D9701.2:5mm

PPVOUT_SW_LCDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=50V) → 6 62

PLACE_NEAR=D9701.2:3mm

CRITICAL C9712 10UF 10% 25V X5R 805

C9713 0.1UF 10% 25V X5R 402

PLACE_NEAR=L9701.1:3mm

PLACE_NEAR=L9701.1:3mm

PLACE_NEAR=U9701.D1:5mm

C9710 1UF 10% 25V X5R 603-1

PLACE_NEAR=U9701.D1:3mm

C9714 0.01UF 10% 10V X5R 201

XW9720 SM

PPVOUT_SW_LCDBKLT_FB (VOLTAGE=50V, MIN_LINE_WIDTH=0.1 MM, MIN_NECK_WIDTH=0.1 MM)

PLACE_NEAR=L9797.1:5mm

7 =PP3V3_S0_BKL_VDDIO

PLACE_NEAR=U9701.C4:4mm

C9711 0.1UF 10% 6.3V X5R 201

U9701 25-BUMP-MICRO LP8550

		VDDIO VLDO VIN	C4 D1 C1
BKL_VSYNC_R	D2	VSYNC	SW_0 B1
BKL_FLTR	C2	FILTER	SW_1 B2
BKL_ISET	B3	ISET	FB A5
BKL_FSET	B4	FSET	
BKL_SCL	D3	SCLK	OUT1 E5 BKL_ISEN1
BKL_SDA	D4	SDA	OUT2 D5 BKL_ISEN2
BKL_PWM	A4	PWM	OUT3 C5 BKL_ISEN3
BKL_EN	A3	EN	OUT4 E3 BKL_ISEN4
TP_BKL_FAULT	C3	FAULT	OUT5 E2 BKL_ISEN5
			OUT6 E1 BKL_ISEN6
		GND_S B5	GND_L E4 GND_SW A1 GND_SW A2

R9741 10K 5% 1/20W MF 201

R9753 0 5% 1/20W MF 201

43 IN =I2C_BKL_1_SCL

R9757 0 5% 1/20W MF 201

43 BI =I2C_BKL_1_SDA

Addr: 0x58(Wr)/0x59(Rd)

65 8 PPBUS_SW_LCDBKLT_PWR

R9731 200K 1% 1/20W MF 201

R9715 100K 1% 1/20W MF 201

PLACE_SIDE=BOTTOM

8 IN LCD_BKLT_PWM

R9704 33 5% 1/20W MF 201

C9704 33PF 5% 25V NP0-C0G 201

Fpwm=9.62kHz
see spec for others

R9755 10K 1% 1/20W MF 201

R9716 90.9K 1% 1/20W MF 201

I_LED=20.3mA

R9714 18.2K 1% 1/20W MF 201

GND_BKL_SGND (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)

XW9710 SM

PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E5:10mm
LED_RETURN_1 → OUT 6 62

BKLT:PROD
R9718 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.D5:10mm
LED_RETURN_2 → OUT 6 62

BKLT:PROD
R9719 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.C5:10mm
LED_RETURN_3 → OUT 6 62

BKLT:PROD
R9720 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E3:10mm
LED_RETURN_4 → OUT 6 62

BKLT:PROD
R9721 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E2:10mm
LED_RETURN_5 → OUT 6 62

BKLT:PROD
R9722 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E1:10mm
LED_RETURN_6 → OUT 6 62

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_XDP_BPM	TOP,BOTTOM	100 MIL	100 MIL	100 MIL	100 MIL	=STANDARD	=STANDARD
CPU_XDP_BPM	*	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S

NOTE: CPU_XDP_BPM physical constraint is to prevent routing on outer layers.
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_BMIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 41 56
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	8 10
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_XDP_BPM	CPU_ITP	XDP_BPM_L<7..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 56
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 56
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 58
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 56
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 56
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 56
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 56
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE
CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP_BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP_BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9,ISL10	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	0.6 MM	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_2PWR
MEM_CTRL	MEM_PWR	*	MEM_2PWR
MEM_CMD	MEM_PWR	*	MEM_2PWR
MEM_DATA	MEM_PWR	*	MEM_2PWR
MEM_DQS	MEM_PWR	*	MEM_2PWR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_2GND
MEM_CTRL	GND	*	MEM_2GND
MEM_CMD	GND	*	MEM_2GND
MEM_DATA	GND	*	MEM_2GND
MEM_DQS	GND	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_CKE<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_CS_L<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_ODT<3..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<15..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_CKE<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_CS_L<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_ODT<3..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<15..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 29 30 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	9 27 28 29 30 31

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2012

PAGE TITLE: Memory Constraints

Apple Inc.

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	
	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<3>	8
	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<3>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_P	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_N	8
	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 37
	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_N	6 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 37
	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 37
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 37
	SATA_90D	SATA	SATA_ODD_R2D_C_P	8 16
	SATA_90D	SATA	SATA_ODD_R2D_C_N	8 16
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	8 16
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	8 16
	SATA_90D	SATA	SATA_HDD_R2D_RC_P	
	SATA_90D	SATA	SATA_HDD_R2D_RC_N	
	SATA_90D	SATA	SATA_HDD_D2R_RC_P	
	SATA_90D	SATA	SATA_HDD_D2R_RC_N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 38
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 38
USB_EXTB	USB_85D	USB	USB_EXTB_P	
	USB_85D	USB	USB_EXTB_N	
USB_EXTC	USB_85D	USB	USB_EXTC_P	
	USB_85D	USB	USB_EXTC_N	
USB_EXTD	USB_85D	USB	USB_EXTD_P	6 24 39
	USB_85D	USB	USB_EXTD_N	6 24 39
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 63
	USB_85D	USB	T29_A_RSVD_N	8 63
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	6 18 39
	USB_85D	USB	USB_CAMERA_N	6 18 39
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	
	USB_85D	USB	USB_CAMERA_CONN_N	
USB_BT	USB_85D	USB	USB_BT_P	6 24 36
USB_BT	USB_85D	USB	USB_BT_N	6 24 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	48
	USB_85D	USB	USB_TPAD_N	48
USB_IR	USB_85D	USB	USB_IR_P	
	USB_85D	USB	USB_IR_N	
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	8 24
	USB_85D	USB	USB_SDCARD_N	8 24
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 40 42
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 40 42
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 40
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 42
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 43
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 43
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 43
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 43
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 43
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 43
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	6 16 39
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	6 16 39
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	6 16 39
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	6 16 39
	HDA_50S	HDA	AUD_SDI_R	
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	6 16 39
	HDA_50S	HDA	HDA_SDOUT_R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 42
	SPI_55S	SPI	SPI_CLK	42
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 42
	SPI_55S	SPI	SPI_MOSI	42
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 42
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 42
	SPI_55S	SPI	SPI_CS0_L	42
	SPI_55S	SPI	SPI_MLB_CLK	42 49
	SPI_55S	SPI	SPI_MLB_MOSI	42 49
	SPI_55S	SPI	SPI_MLB_MISO	42 49
	SPI_55S	SPI	SPI_MLB_CS_L	42 49
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 36
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 36
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 36
	PCIE_85D	PCIE	PCIE_FW_R2D_P	
	PCIE_85D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	
	PCIE_85D	PCIE	PCIE_FW_D2R_N	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 36
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 69
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 69
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 63
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 63
	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	63
	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	63
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 63
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 63
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	63
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	63
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	62
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	62
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	9 62
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	9 62
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	6 62
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	6 62
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_C_P	6 62
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_C_N	6 62
	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_P	9 62
	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_N	9 62
	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 33
	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 33
PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE	PCIE_T29_D2R_P<3>	8 33
PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE	PCIE_T29_D2R_P<2>	8 33
PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE	PCIE_T29_D2R_P<1>	8 33
PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE	PCIE_T29_D2R_P<0>	8 33
PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE	PCIE_T29_D2R_N<3>	8 33
PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE	PCIE_T29_D2R_N<2>	8 33
PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE	PCIE_T29_D2R_N<1>	8 33
PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE	PCIE_T29_D2R_N<0>	8 33
PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE	PCIE_T29_R2D_P<3>	33
PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE	PCIE_T29_R2D_P<2>	33
PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE	PCIE_T29_R2D_P<1>	33
PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE	PCIE_T29_R2D_P<0>	33
PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE	PCIE_T29_R2D_N<3>	33
PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE	PCIE_T29_R2D_N<2>	33
PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE	PCIE_T29_R2D_N<1>	33
PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE	PCIE_T29_R2D_N<0>	33
	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 25
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	25 33
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	33

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PCH Constraints 2

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N
Port 2 Not Used			

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 8 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 8 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 8 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 8 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N
	T29_I2C_55S	T29_I2C	I2C_T29_SCL 33 43
	T29_I2C_55S	T29_I2C	I2C_T29_SDA 33 43
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK 33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI 33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO 33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L 33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0> 33 63
	T29DP_80D	T29DP	T29_R2D_C_N<3..0> 33 63
	T29DP_80D	T29DP	T29_D2R_P<3..0> 33 63
	T29DP_80D	T29DP	T29_D2R_N<3..0> 33 63
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0> 63
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0> 63
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1> 63
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1> 63
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>
T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_P<0> 63 64
T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_N<0> 63 64
T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_P<1> 63 64
T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_N<1> 63 64
	T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_P 64
	T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_N 64
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0> 63
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0> 63
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0> 63
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<0> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<0> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<1> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<1> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2> 63
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3> 63
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3> 63
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P 63
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N 63
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P 63
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N 63
T29DPA_ML_ODD			T29DPA_ML_P<1> 63 64 71
T29DPA_ML_ODD			T29DPA_ML_N<1> 63 64 71
T29DPA_ML_ODD			T29DPA_ML_P<3> 63 64 71
T29DPA_ML_ODD			T29DPA_ML_N<3> 63 64 71
	T29DP_80D	T29DP	T29DPA_ML_P<3..0> 63 64 71
	T29DP_80D	T29DP	T29DPA_ML_N<3..0> 63 64 71
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0> 63 64
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0> 63 64
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P 63 64
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N 63 64

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	43
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	43
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	43
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	43
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	43
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	43
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	43
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	43
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	43
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	52
	1TO1_DIFFPAIR		CHGR_CSI_N	52
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	52
	1TO1_DIFFPAIR		CHGR_CSO_N	52

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
MEM_72D	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
MEM_37S	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
MEM_85D	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
PCIE_85D	*	OVERRIDE	OVERRIDE	0.076 MM	10 mm	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
USB_85D	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
CPU_27P4S	TOP	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
CLK_PCIE_90D	TOP	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN P<3..0>	
	ENET_100D	ENETCONN	ENETCONN N<3..0>	
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	
E295	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	
E296	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	
E297	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	
E298	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	46
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	46
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 46
E68	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 46
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	46
	THERM_1TO1_55S	THERM	T29_THERMD_N	46
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_P	46
	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	44 58
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	44 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	44 56 57
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	44 57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	44 57
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	44 57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	44
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	44
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	53
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	56 57
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	37 45
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	37 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	8 45
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	8 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	45 55
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	45 55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	36 45
E830	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	36 45
E293	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N	
E294	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
E832 SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50 73
E833	DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50 73
E834 MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	50
E835	DIFFPAIR	AUDIO	MAX98300_R_N	50

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	
	1TO1_DIFFPAIR		CHGR_CSI_R_P	52
	1TO1_DIFFPAIR		CHGR_CSI_R_N	52
	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 52
	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 52
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	38
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	38
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	38
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	38
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	
	USB_85D	USB	USB_LT2_N	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 50 51
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 50 51
E299 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	
E300 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	
E301 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	
E302 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	
E303 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	
E304 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	
E305 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	
E306 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	
E307 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	
E308 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	
E309 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	
E310 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	
E311 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	
E312 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	
E313 SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50 73
E314 AUD_DIFF	DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50 73
E315 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	
E316 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	
	USB_85D	USB	USB_TPAD_R_P	
	USB_85D	USB	USB_TPAD_R_N	
	SB_POWER		PP3V3_S5	6 7
	SB_POWER		PP3V3_S0	6 7
	GND		GND	

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E517 (USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_P
E518 (USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_N
E519 (USB_EXTA)	USB_85D	USB	USB_LT1_P
E520 (USB_EXTA)	USB_85D	USB	USB_LT1_N
E521 (USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_P 6 48
E522 (USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_N 6 48
E523 SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	I2C_SMC_SMS_SDA_R
E524 SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	I2C_SMC_SMS_SCL_R
E525	SMB_5SS	SMB	I2C_TCON_SCL
E527	SMB_5SS	SMB	I2C_TCON_SDA
E528	SMB_5SS	SMB	I2C_TCON_SCL_CONN
E526	SMB_5SS	SMB	I2C_TCON_SDA_CONN

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Project Specific Constraints

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4,ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

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