### Table of Contents

1. Table of Contents

#### Table 1: System Block Diagram
- Page 2
- Page 3

#### Table 2: Power Block Diagram
- Page 4

#### Table 3:isman Scan Chain
- Page 5

#### Table 4: Functional / ICT Test
- Page 6

#### Table 5: Power Aliases
- Page 7

#### Table 6: Signal Aliases
- Page 8

#### Table 7: Functional / ICT Test
- Page 9

#### Table 8: Power Block Diagram
- Page 10

#### Table 9: Power Block Diagram
- Page 11

#### Table 10: Power Block Diagram
- Page 12

#### Table 11: Functional / ICT Test
- Page 13

#### Table 12: Power Block Diagram
- Page 14

#### Table 13: Power Block Diagram
- Page 15

### DDR

<table>
<thead>
<tr>
<th>Page</th>
<th>Contents</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Table of Contents</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Power Block Diagram</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>isisman Scan Chain</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Functional / ICT Test</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Power Aliases</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Signal Aliases</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CPU FSB</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>CPU Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>CPU Decoupling &amp; VID</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>LLC/Supplies</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Memory Interface</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Memory MX</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>PCIe Interfaces</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Ethernet &amp; Graphics</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>SATA &amp; USB</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>HDA &amp; NSC</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>Standard Decoupling</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Standard Decoupling</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>MUXGFX Graphics Support</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>Misc Power Supplies</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Power Control</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Power FETs</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>NV GS6 PCI-E</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>NV GS6 Core/FB Power</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>NV GS6 Frame Buffer 1/2</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>GDDR3 Frame Buffer A (Top)</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>GDDR3 Frame Buffer B (Top)</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>G96 CHIP/2 Integrated Memory</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Ethernet &amp; AirPort Support</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Ethernet Connectors Support</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>ExpressCard Connector</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Ethernet PHY (RTL8211C)</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>Ethernet PHY (RTL8211C)</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>DisplayPort Controller</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>FireWire Ports</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>SATA Connectors</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>MUXGFX Graphics Support</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>USB Connectors</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>USB Connectors</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>SMC</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>SMG</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>LPC SPI Debug Connector</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>USB Bus Connections</td>
<td></td>
</tr>
</tbody>
</table>
1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)

From XDP connector
or via level translator

U1000 CPU
To XDP connector
and/or level translator

U1400 MCP

U8000 GPU

U9200 GMUX

GMUX CPLD Programming Port

CRITICAL
PLACEMENT_NOTE=Place near pin U1000.AB3

PLACEMENT_NOTE=Place near pin U1400.F19

PLACEMENT_NOTE=Place close to U0600

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place near pin U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000

PLACEMENT_NOTE=Place close to U1400.F19

PLACEMENT_NOTE=Place close to U8000
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

CPU VCORE HF AND BULK DECOUPLING

- 1x 330uF, 20x 22uF 0805

VCC (CPU I/O) DECOUPLING

- 1x 470uF, 6x 0.1uF 0402

VCCA (CPU AVdd) DECOUPLING

- 1x 470uF, 6x 0.1uF 0402
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).
3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.

- 3.3V LATRIGGER_L
- 3.3V SYSTEM_RST_DEBOUNCE_L
- 3.3V BATTERY_L
- 3.3V PWRT_N_L
- 3.3V WAKE_SCI_L
- 3.3V JTAG_MCP_TMS
- 3.3V JTAG_MCP_TDI
- 3.3V PCIE_WAKE_L

5% 1/16W MF-LF 402
10K

R2400
1 2
R2401
1 2
R2402
1 2
R2403
1 2
R2404
1 2
R2405
1 2
R2406
1 2
R2407
1 2
R2408
1 2
R2409
1 2

www.laptop-schematics.com
MCP Core Power

MCP PCIEX (16x4) Power

MCP SATA (DVDD) Power

MCP Memory Power

MCP 3.3V AUX/USB Power

MCP 3.3V/1.5V HDA Power

MCP Data (USB) Power

MCP 1.05V BBMI Power

MCP PEB (VTI) Power

MCP FEB (VTI) Power

MCP Memory Power

MCP 3.3V Power

MCP 3.3V and USB Power

MCP 3.3V/1.5V HDA Power

MCP 79 Ethernet VRef

Apple: 4x 2.2uF 0402 (8.8 uF)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 9x 0.1uF 0402 (14.9 uF)

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)

Apple: 5x 2.2uF 0402 (11 uF)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)

Apple: 1x 2.2uF 0402 (2.2 uF)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

Apple: 2x 2.2uF 0402 (4.4 uF)

Current numbers from email Paveach Kocher provided 11/30/2007 4:00pm (no official document number).
The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. To maintain the document in confidence
II. Not to reproduce or copy it
III. Not to reveal or publish in whole or part

Notice of Proprietary Property

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).
OUT
OUT

RTC Power Sources

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

Platform Reset Connections

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

Reset Button

SB Misc

MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections.

MCPSEQ_MLB is cross between MLB and internal power sequencing, which
results in earlier NMI/LK and FCB PER interface initialization.

MCPSEQ_MLB should guarantee CPU_VLD does not go high before
CPU_PWRGD, which is 50-100ms after FCB_PWRGD assertion.

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.
**Page Notes**

- I2C_PCA9557D_SDA
- I2C_PCA9557D_SCL
- PP3V3_S3_VREFMRGN

**SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.**

- Place close to U1000.AD26
- Place close to U8500, U8550
- Place close to U8400, U8450
- Place close to J3200.126
- Place close to J3100.126

**RES, MTL FILM, 0.5%, 0402, SM, LF**
DDR3 RESET Support

MCP’s cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

1. 1.8V input must be stable before
before 1.8V starts to rise to
avoid glitch on MEM_RESET_L.

3.3V input must be stable before
MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

DDR3 Support

SYNC_DATE=06/18/2008
SYNC_MASTER=T18_MLB
TXDLY = 0 (No TXCLK Delay)
RXDLY = 0 (RXCLK transitions with data)
AN[1:0] = 11 (Full auto-negotiation)
PHYAD = 01 (PHY Address 00001)

Configuration Settings:
- RXDLY = 0 (No TXCLK Delay)
- TXDLY = 0 (No TXCLK Delay)
- AN[1:0] = 11 (Full auto-negotiation)
- PHYAD = 01 (PHY Address 00001)

Hence, RC (R3725 and C3725) are made NOSTUFF.
ENET_RESET_L is not asserted when WOL is active.

If internal switcher is used, must place 1x22uF & 1x22uF within 5mm of U3700 and 1x22uF & 1x22uF within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.

NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

If internal switcher is used, must place inductor within 5mm of U3700, and 1x22uF & 1x22uF within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.

If internal switcher is used, must place 1x22uF & 1x22uF within 5mm of U3700, and 1x22uF & 1x22uF within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.

If internal switcher is used, must place 1x22uF & 1x22uF within 5mm of U3700, and 1x22uF & 1x22uF within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.
WLAN Enable Generation

"WLAN" = ((("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

1.05V ENET FET

Pull-up to 3.3V power FET.

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
Transformers should be mirrored on opposite sides of the board.

Place one of 0.1uf cap close to each center tap pin of transformer.

Power aliases required by this page:

BOM options provided by this page:

Signal aliases required by this page:

www.laptop-schematics.com
The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it
II. Not to reveal or publish in whole or part
III. To maintain the document in confidence

Notice of Proprietary Property
FireWire Design Guide (FWDG 0.6, 5/14/03)

1394b implementation based on Apple TPA/TPB XNets to apply to entire TPA/TPB XNets.

**Page Notes**

**FireWire PHY Config Straps**

Configured PHY for:
- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

**Termination**

Place close to FireWire PHY
- FWJ TPA<R>

**Latest-VG Protection Power**

PPVPHY_FWKERED needs to be biased to at least 2.0V for FF signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms and for a 3.3V rail

**Cable Power**

Note: Trace PPVP_FW_PORT1 must handle up to 5A

**FireWire Ports**

REV. 1.0A

APPLE INC.
We can add protection to 5V if we want, but leaving NC for now.

USB/SMC Debug Mux

Port Power Switch

Left USB Port A

Left USB Port B

External USB Connectors

The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. To maintain the document in confidence.
II. Not to reproduce or copy it.
III. Not to reveal or publish in whole or part.
those designated as inputs require pull-ups.

pins designed as outputs can be left floating,
Alternate SPI ROM Support

MCP79 Internal SPI MUX Support

MCP SPI Override Options

SPI Frequency Clamp

SPI MUX BYPASS

LPC+SPI Debug Connector

Notice of Proprietary Property

APPLE INC.

AGREES TO THE FOLLOWING

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

OF THIS DOCUMENT AGREES TO THE FOLLOWING

I. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

II. NOT TO REPRODUCE OR COPY IT

III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

OF THIS DOCUMENT AGREES TO THE FOLLOWING

I. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

II. NOT TO REPRODUCE OR COPY IT
Current from battery to PBUS

Monitors battery discharge

=PP3V42_G3H_CPUCOREISNS
=PPVIN_S5_CPU_IMVP_ISNS
=PPVIN_S5_CPU_IMVP_ISNS_R
=PPVCORE_S0_CPU
=PPVCORE_GPU_REG

Place short near U8000 center

Place short near U1000 center

REGULATOR SIDE:

=PP3V42_G3H_BMON_ISNS
=PP3V42_G3H_CPUCOREISNS
=PP3V42_G3H_BMON_ISNS

Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU Voltage Sense / Filter

GPU Voltage Sense / Filter

MCP Voltage Sense / Filter

BMON Current Sense - Entire circuit must be near SMC (U4900)

INA213 has gain of 50V/V

CPU VCore High Side Current Sensor

CPU VCore Load Side Current Sense / Filter

Current & Voltage Sensing
MCP VCore Current Sense

MCP MEM VDD Current Sense

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share
dual package opamp U5440

CPU FSB 1.05V Current Sense

1.05V CPU FSB Current Sense Filter

GPU VCore Current Sense

GPU VCore Current Sense and GPU 1.8V Current Sense share
dual package opamp U5410

GPU 1.8V Current Sense

Current Sensing

Gain: 274x

SIGNAL MODEL=EMPTY

Note: 24 pin sense current up to 11.5Amps.

Gain: 274x

SIGNAL MODEL=EMPTY

Not to reveal or publish in whole or part.

Not to reproduce or copy it.

Agrees to the following

The information contained herein is the proprietary

Copyright of all rights reserved.

Sync master = sensor

Sync date = 08/14/2008

Rev. A.0.0051-7546

Apple Inc.

http://www.laptop-schematics.com
Digital SMS

Pull-up required if SMS_INT_L is not used.

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

Analog SMS

R5921 Pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

www.laptop-schematics.com
SPI ROM

---

**Frequency** | **SPI_MODE** | **SPI_CLK**
--- | --- | ---
33 MHz | 0 | 0
42 MHz | 0 | 1
25 MHz | 1 | 0

25MHz is selected with R6190 and R6191
Any of the 9 frequencies can be selected with R6190, R6191, R6195 and R6196

---

www.laptop-schematics.com
Pseudo-Diff Line-In Filter

GAIN = -5.4DB  AV = 0.52
FC = 1.8 HZ
Headphone Amplifier (MAX9724A)
APN: 353S1637

1st Order DAC Filter
HP: 3.52 Hz  LP: 34 kHz
VOLTAGE GAIN: 1.53
1.5V DDR3 Supply

- **VDDQ**
  - PGOOD
  - S3
  - S5
  - VTTSNS
  - VTT
  - VTTREF
- **VDDQSET**
  - VBST
  - VDDQ/VTTREF Enable
- **VCORE**
  - DRVL
  - DRVH
  - VDDQ
  - GND
  - CS
  - CS_TAG
  - THRM_PAD
  - GND

**Circuit Components**

- **C7300**: 4.7UF 10%
- **C7305**: 6.3V 20%
- **C7310**: 100PF X5R
- **C7320**: 10UF 603-1
- **C7325**: 1UF X5R
- **C7330**: 0.1UF 10%
- **C7331**: 0.1UF X7R
- **C7332**: 0.033UF 10%
- **C7333**: 15A max output
- **C7334**: 10k
- **C7335**: 50V
- **C7340**: 4.7k 603-1
- **C7341**: 1% 1/16W
- **C7345**: 402 1%
- **C7350**: 1.0UH 13A-5.6MOHM
- **C7355**: 22UF 20%
- **C7360**: 6.3V 20%
- **C7361**: 1UF X5R 1000PF
- **R7305**: 10k
- **R7310**: 10k
- **R7320**: 10k
- **R7321**: 10k
- **XW7300**: 1%
- **XW7335**: 1%
- **XW7345**: 1%

**Notes**

- **SM PLACEMENT_NOTE**
  - Place next to Q7335
  - Place next to C7355

**Design Specifications**

- 1.5V DDR3 Supply
- Switch Node = TRUE
- Critical Components
- Min Neck Width = 0.2 mm
- Min Line Width = 0.6 mm

**Notice of Proprietary Property**

- The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:
  1. Not to reproduce or copy it
  2. Not to reveal or publish in whole or part
  3. To maintain the document in confidence
MCP79 Rev A01 requires higher core & analog voltage

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DEC</th>
<th>CRITICAL</th>
<th>NOTE OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>X5R10V10%</td>
<td>1</td>
<td>1UF 10V</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>CERM-X7R</td>
<td>1</td>
<td>1000PF 10V</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>CERM402</td>
<td>1</td>
<td>1UF 10V</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>C7503</td>
<td>1</td>
<td>1UF 10V</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>C7530</td>
<td>1</td>
<td>1UF 10V</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>C7504</td>
<td>1</td>
<td>0.1UF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7564</td>
<td>1</td>
<td>0.01UF 16V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7563</td>
<td>1</td>
<td>20%1/16W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C7561</td>
<td>1</td>
<td>20%1/16W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C7560</td>
<td>1</td>
<td>20%1/16W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7514</td>
<td>1</td>
<td>100K MF-LF 1/16W 1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7564</td>
<td>1</td>
<td>100K MF-LF 1/16W 1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7570</td>
<td>1</td>
<td>54.9K MF 1/16W 1/16W 1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7581</td>
<td>1</td>
<td>237K MF 1/16W 1/16W 1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7582</td>
<td>1</td>
<td>110K MF 1/16W 1/16W 1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7580</td>
<td>1</td>
<td>475K 0.1%1/16W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7571</td>
<td>1</td>
<td>48.7K 0.1%1/16W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R5425</td>
<td>1</td>
<td>0.001 1W</td>
<td></td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>U7500</td>
<td>1</td>
<td>MCF 10-MF 5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C7590</td>
<td>1</td>
<td>0.01UF 16V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7551</td>
<td>1</td>
<td>10UF X5R</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>C7550</td>
<td>1</td>
<td>10UF X5R</td>
<td></td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>C7520</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7519</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7518</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7517</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7516</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7515</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7514</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7513</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7512</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7511</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7510</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7509</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7508</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7507</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>C7506</td>
<td>1</td>
<td>1000PF 25V</td>
<td></td>
<td>10%</td>
<td></td>
</tr>
</tbody>
</table>

Vout = 0.7V * (1 + Ra / Rb)

Vout = 2.0V * Req / (Ra + Req)

Max load 50uA

MCP79 Rev A01 requires higher core & analog voltage

1.05V / MCP Core Regulator

APPLE INC.

SYNC MASTER = M99_MLB

NOTICE OF PROPRIETARY PROPERTY

A.0.0051-7546

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

TO MAINTAIN THE DOCUMENT IN CONFIDENCE

MIN_NECK_WIDTH = 0.2MM

MIN_LINE_WIDTH = 0.5MM

Internal 10-ohm path from PVCC to VCC

Max Current 5A

Q7510 Limit? f = 400 kHz
Vout = 0.75V \times (1 + Ra / Rb)

Vout = 1.052V

6A max output

Brain = PP_CPUVTTS0_REG

CPUVTTS0_VFB

GND_CPUVTTS0_SGND

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

CPUVTTS0_TRIP

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

CPUVTTS0_DRVH

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

CPUVTTS0_VBST

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

CPUVTTS0_LL

SWITCH_NODE=TRUE

GATE_NODE=TRUE

PP5V_S0_CPUVTTS0

_VOLTAGE=5V

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

PP5V_S0_CPUVTTS0_V5FILT

VOLTAGE=10V

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

PP5V_S0_CPUVTTS0_PGOOD

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

PP5V_S0_CPUVTTS0_TON

VOLTAGE=10V

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

PP5V_S0_CPUVTTS0_PGOOD

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

PP5V_S0_CPUVTTS0_VSNS

GATE_NODE=TRUE

CPUVTTS0_DRVL

GATE_NODE=TRUE

PPCPUFSB_ISNS

SYNC_MASTER=M99_MLB
SYNC_DATE=12/14/2007

CPU VTT Power Supply

B2-SM 2.0 VPOLY-TANT

330 UF 20%

CRITICAL

IHLP2525CZ-SM1 2.2UH-14A

CRITICAL

SM

PLACEMENT_NOTE=Place XW7665 next to C7665

200 1%

MF-LF402 1/16W 1%

6.34 K 1/16W 1%

8.06 K 402 1%

MF-LF402 1/16W 1%

68 68 QFN

TPS51117RGY_QFN14

CRITICAL

X5R603 10% 2.2 UF 16V X5R

1 UF 10% 10V

402 MF-LF 1%

402 MF-LF 1%

B2-SM 2.0 VPOLY-TANT

330 UF 20%

CRITICAL

POLY-TANT CASE-D2-SM

20%

MLP

FDMS9600S

CRITICAL

SM

PLACEMENT_NOTE=Place XW7665 next to C7665

200 1%

MF-LF402 1/16W 1%

6.34 K 1/16W 1%

8.06 K 402 1%

MF-LF402 1/16W 1%

68 68 QFN

TPS51117RGY_QFN14

CRITICAL

X5R603 10% 2.2 UF 16V X5R

1 UF 10% 10V

402 MF-LF 1%

402 MF-LF 1%

B2-SM 2.0 VPOLY-TANT

330 UF 20%

CRITICAL

POLY-TANT CASE-D2-SM

20%

MLP

FDMS9600S

CRITICAL

SM

PLACEMENT_NOTE=Place XW7665 next to C7665

200 1%

MF-LF402 1/16W 1%

6.34 K 1/16W 1%

8.06 K 402 1%

MF-LF402 1/16W 1%

68 68 QFN

TPS51117RGY_QFN14

CRITICAL

X5R603 10% 2.2 UF 16V X5R

1 UF 10% 10V

402 MF-LF 1%

402 MF-LF 1%

B2-SM 2.0 VPOLY-TANT

330 UF 20%

CRITICAL

POLY-TANT CASE-D2-SM

20%

MLP

FDMS9600S

CRITICAL

SM

PLACEMENT_NOTE=Place XW7665 next to C7665

200 1%

MF-LF402 1/16W 1%

6.34 K 1/16W 1%

8.06 K 402 1%

MF-LF402 1/16W 1%

68 68 QFN

TPS51117RGY_QFN14

CRITICAL

X5R603 10% 2.2 UF 16V X5R

1 UF 10% 10V

402 MF-LF 1%

402 MF-LF 1%
1.8V S0 Switcher / 1.0VFW SWITCHER

2.5 power required for output discharge feature.

Vout = 0.6V * (1 + Ra/Rb)

MCP 1.05V AUXC Supply

Vout = 1.001V
100mA max output
(Switcher limit)

f = 2.25 MHz

Vout = 1.816V
0.3A max output
(Switcher limit)

f = 1.6 MHz

1.8V S0 Switcher
MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends powering during sleep.

In order to support powering rails, hardware must guarantee MEM_CKE signals are low

on VTT rail, which pulls all CKE signals low through VTT termination resistors.

MEM_VTT_EN output from MCP79 used to enable clamp before rail is turned off, and remains low until after rail turns back on or DIMMs

In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep.
2.5V/1.2V S3 Switcher

Vout = 0.6V * (1 + Ra/Rb)

500mA max output (Switcher limit)

f = 2.25 MHz

Vout = 2.5V

0.3A max output (Switcher limit)

f = 2.25 MHz

Misc Power Supplies

SYNC_MASTER=MUXGFX
SYNC_DATE=02/01/2008

=PP3V3_S0_P1V2P2V5
=PP2V5_S0_REG
=P1V2S0_VFB
=P1V2S0_EN
=P2V5S0_VFB
=P2V5S0_EN
=PP1V2_S0_REG
### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP_MEM_COMP</td>
<td>Memory Bus Constraints</td>
</tr>
</tbody>
</table>

#### MCP MEM COMP Signal Constraints

- **SOURCE:** MCP Interface DG (DG-03328-001_v0D), Section 2.3.4

- **No DQS to clock matching requirement.**
- **DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.**
- **DQ signals should be matched within 5 ps of associated DQS pair.**
- **DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.**
- **All DQS pairs should be matched within 100 ps of clocks.**

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP_MEM_COMP</td>
<td>Memory Bus Spacing Group Assignments</td>
</tr>
</tbody>
</table>

### Memory Net Properties

<table>
<thead>
<tr>
<th>Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP_MEM_COMP</td>
<td>Memory Net Properties</td>
</tr>
</tbody>
</table>

#### Memory Net Properties

- **SOURCE:** MCP Interface DG (DG-03328-001_v0D), Section 2.3.4
### MCP RGMII (Ethernet) Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Pin</th>
<th>Constraint Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>MCP MII COMP</td>
<td>33</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
<tr>
<td>Source</td>
<td>MCP MII COMP</td>
<td>34</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
<tr>
<td>Source</td>
<td>MCP_MII_COMP</td>
<td>35</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
<tr>
<td>Source</td>
<td>MCP MII COMP GND</td>
<td>34</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

### 88E1116R (Ethernet PHY) Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Pin</th>
<th>Constraint Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>MCP MII COMP</td>
<td>33</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
<tr>
<td>Source</td>
<td>MCP MII COMP</td>
<td>34</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
<tr>
<td>Source</td>
<td>MCP_MII_COMP</td>
<td>35</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
<tr>
<td>Source</td>
<td>MCP_MII COMP GND</td>
<td>34</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

---

**Ethernet Constraints**

**Note:** This information is subject to the non-exclusive license, copyright, and trademark rights of Apple, Inc., and is provided "as is" without warranty of any kind. For more information, please visit [www.laptop-schematics.com](http://www.laptop-schematics.com).
From T18 MXM:
Digital Video Signal Constraints

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
Max length of DP/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DS (00-0328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

GDDR3 FB A/B Net Properties

GDDR3 FB C/D Net Properties

G96 Net Properties

GPU (G96) Constraints

Apple Inc. 2001-7644 A-5-4
<table>
<thead>
<tr>
<th>BOARD LAYERS BOARD AREAS</th>
<th>PHYSICAL_RULE_SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON LAYER?</td>
<td>LAYER MINIMUM NECK WIDTH</td>
</tr>
<tr>
<td></td>
<td>DIFFPAIR PRIMARY GAP</td>
</tr>
<tr>
<td>100_OHM_DIFF</td>
<td>0.200 MM</td>
</tr>
<tr>
<td>ISL2, ISL11</td>
<td>0.115 MM</td>
</tr>
<tr>
<td>90_OHM_DIFF</td>
<td>0.102 MM</td>
</tr>
<tr>
<td>ISL3, ISL4</td>
<td>0.076 MM</td>
</tr>
<tr>
<td>55_OHM_SE</td>
<td>0.089 MM</td>
</tr>
<tr>
<td>STTap, BOTTOM</td>
<td>0.220 MM</td>
</tr>
<tr>
<td>Y110_OHM_DIFF</td>
<td>0.330 MM</td>
</tr>
<tr>
<td>ISL9, ISL10</td>
<td>0.160 MM</td>
</tr>
<tr>
<td>70_OHM_DIFF</td>
<td>0.135 MM</td>
</tr>
<tr>
<td>ISL3, ISL4</td>
<td>0.077 MM</td>
</tr>
<tr>
<td>110_OHM_DIFF</td>
<td>0.330 MM</td>
</tr>
<tr>
<td>STTap, BOTTOM</td>
<td>0.200 MM</td>
</tr>
<tr>
<td>100_OHM_DIFF</td>
<td>0.115 MM</td>
</tr>
<tr>
<td>ISL2, ISL11</td>
<td>0.102 MM</td>
</tr>
<tr>
<td>55_OHM_SE</td>
<td>0.089 MM</td>
</tr>
<tr>
<td>STTap, BOTTOM</td>
<td>0.220 MM</td>
</tr>
</tbody>
</table>

**NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.