1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MBP 15"MLB

08/18/2008

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7546	1	SCHEM,FIBBO,M98	SCH	CRITICAL	
820-2330	1	PCBF,FIBBO,M98	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Aug 18 01:48:34 2008

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

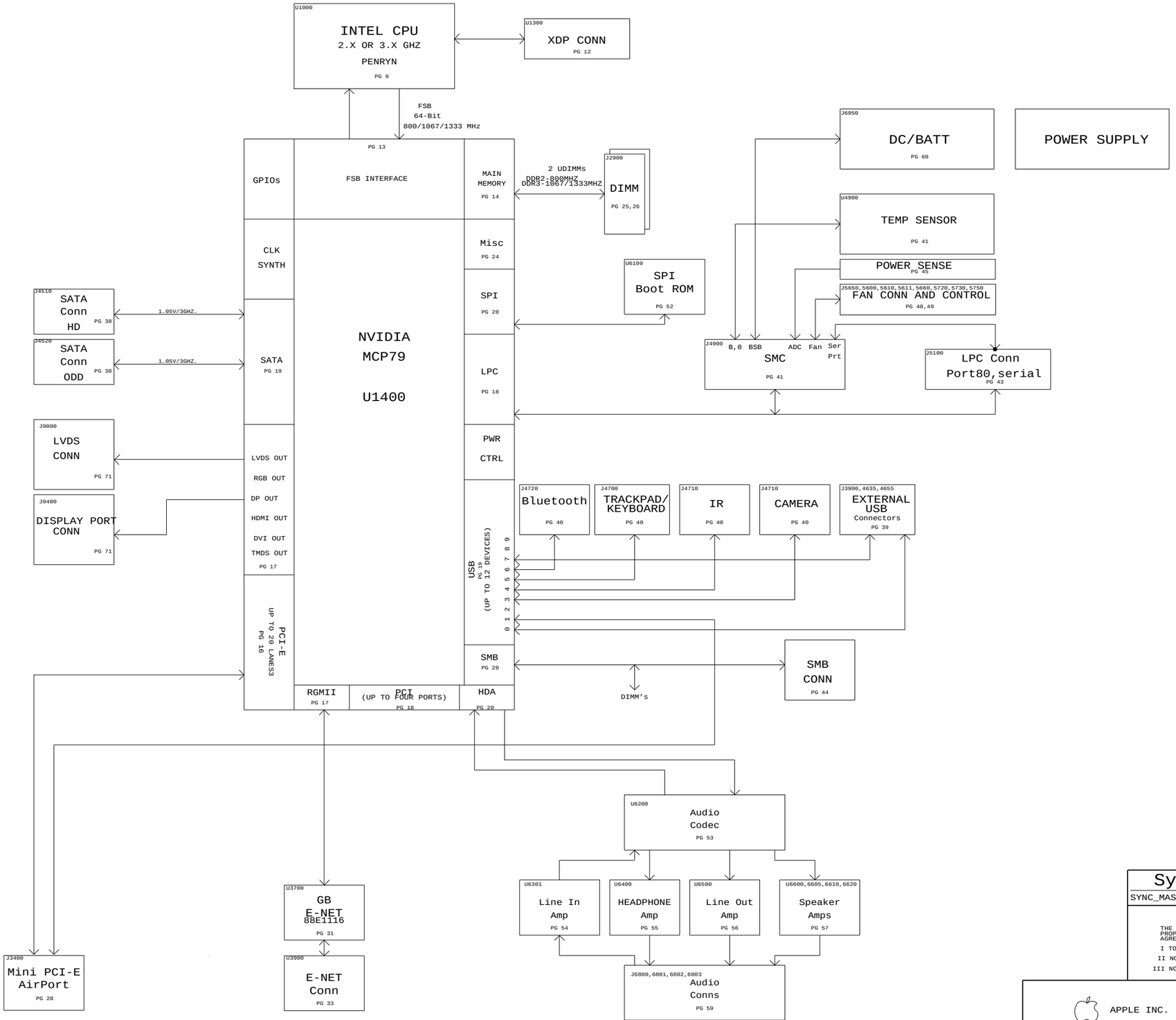
MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

APPLE INC.

TITLE
SCHEM,MBP 15MLB

DRAWING NUMBER 051-7546
REV. A.0.0
SHT 1 OF 96



System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 2 OF 96	

M98 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN(16.5V)
6A FUSE
LIO_DCIN_ISENSE
U5705
CHGR_EN (S5)
ENABLES
VIN
(PAGE 60) PBUS SUPPLY/ BATTERY CHARGER
ISL6258A U7000
VOUT
D6905
D6905
PPVIN_G3H_P3V42G3H
PBUSB_VSENSE
Q5315
8A FUSE
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
ENABLE 3.425V G3HOT LT3470 U6990 (PAGE 59)
PP3V42_G3H_REG
SMC PWRGD RN5VD30A-E U5000 (PAGE 43)
SMC_RESET_L
SMC_GPU_VSENSE
CPUVTTS0_EN
VIN
EN_PSV
VOUT
1.05V
TPS51117 U7600 (PAG 66)
PGOOD
PPCPUVTT_S0_REG (6A MAX CURRENT)
U5498
GPU VCORE
VIN
VOUT
ISL6263B U8900
EN_PSV
PGOOD
(PAGE 78)
PM_GPUVCORE_EN
GPUVCORE_IOUT
PPVCORE_GPU_REG (18A MAX CURRENT)
GPUVCORE_PGOOD
CPUVTTS0_PGOOD
U2830
VR_PWRGD_CLKEN
MCP79
CK_PWRGD
VRMPWRGD
PWRBTN#
PLTRST*
RSMRST*
PWROK
CPUPWRGD(GPIO49)
U1400 (PAGE 14~22)
PLT_RST_L
CPU_PWRGD
MCP_PS_PWRGD
U2850
J6950
3S2P (9 TO 12.6V)
BATT_POS_F
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
U5400
SMC_CPU_VSENSE
PPVCORE_CPU_S0
CPU VCORE
VIN
VOUT
ISL9504B U7100
IMVP_VR_ON_R
VR_ON
PGOOD
(PAGE 61)
CPUVCORE_IOUT
VR_PWRGD_CLKEN_L
VR_PWRGOOD_DELAY
CPU PWRGOOD
U1000 (PAGE 10,11)
RESET*
PPBUS_G3H
Q7920
PP5V_S0_FET
P5VS0_SS
Q7900
PP5V_S3_FET
P5VS3_SS
P1V1GPU_EN
EN1 VIN
VOUT1
1.103V(L/H)
PP1V1_S0GPU_REG
P1V8FB_EN
EN2
VOUT2
1.8V(R/H)
PP1V8_GPU_REG
TPS51124 U9500 (PAGE 82)
MCP79
SLP_S5#(H17)
SLP_S3#(G17)
U1400 (PAGE 14~22)
P3V3S3_EN
P5VS3_EN
LIO_S3_EN
SMC
U4900
(PAGE 42)
U7859
SMC_PM_G2_EN
P60 (S5)
VIN
5V (L/H)
VOUT1
PP5V_S5_REG (8A MAX CURRENT)
3.3V (R/H)
VOUT2
PP3V3_S5_REG (5.5A MAX CURRENT)
TPS51125 U7201 (PAGE 62)
EN0
PGOOD1,2
VREG3
P3V3S5_EN
P5V3V3_S5_PGOOD
PP5V_S3
PP3V3_S5
PP3V3_S3_FET
Q7910
P3V3S3_SS
ISL8009 U7750 (PAGE 66)
V4
PP1V05_S5_MCP
U7400
VIN
EN/PSV
VOUT
SC417 (PAGE 64)
ENL
PGOOD
PP5V_RT_REG
P5V_RT_EN
P5V_RT_PGOOD
Q7930
PP3V3_S0GPU_FET
P3V3S0_SS
Q7970
PP3V3_S0_FET
P3V3GPU_SS
Q3810
P3V3_ENET_FET
P3V3ENET_EN_L
Q3805
WOW_EN
PM_WLAN_EN_L
Q3801
PM_ENET_EN
PM_ENET_EN_L
Q3800
WOL_EN
SMC_ADAPTER_EN
PM_ENET_EN_L
RC DELAY
BKLT_EN
U9701 (PAGE 84)
GOSHAWK6P
ENA
VOUT
PPVOUT_S0_LCDBKLT
P1V2ENET_EN
ENETAVDD_EN
VINLTC3407
RUN2
RUN1
VOUT1
VOUT2
U3850 (PAGE 33)
PP1V9_ENET_REG
PP1V2_ENET_REG
SMC
RSMRST_OUT(P15)
PM_RSMRST_L
ALL_SYS_PWRGD
PWRGD(P12)→99ms DLY
IMVP_VR_ON(P16)
IMVP_VR_ON
RSMRST_PWRGD
RSMRST_IN(P13)
PLT_RST*
SMC_ONOFF_L
PWR_BUTTON(P90)
P17(BTN_OUT)
PM_PWRBTN_L
RST*
SMC_RESET_L
P1V05S0_PGOOD
P5VRIGHT_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P1V8S0_PGOOD
P1V5S0_PGOOD
S0PGOOD_PWROK
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900 (PAGE 42)
PPVIN_S0_DDRREG_LDO
DDRREG_EN
DDRVTT_EN
PM_SLP_S3_L
VIN
VLDOIN
S5 1.8V
S3 0.9V
VOUT1
VOUT2
TPS51116 U7300 (PAGE 63)
PPDDR_S3_REG (12A MAX CURRENT)
PPVTT_S0_DDR_LDO
RST*
PP5V_S0
PP3V3_S0
PP1V5_S0_REG
V1
V2
V3
V4
LTC2900 U7870 (PAGE 68)
RC DELAY
P5VRIGHT_EN
P1V8S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P5VS0_EN (S0)
P3V3S0_EN (S0)
PBUSVSENS_EN (S0)
PM_SLP_S3_DELAY_L (S0)
MCP_CORE
EN2
VOUT2
1.1V
EN1
VOUT1
ISL6236 U7500 (PAGE 65)
VIN
MCPCORES0_EN
P1V05S0_EN
MCPCPCORE_S0_REG
PP5V_RT_REG
(25A MAX CURRENT)
(5A MAX CURRENT)

Power Block Diagram

SYNC_MASTER=T18_MLB
SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 3 OF 96	

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	4	96

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9334	PCBA,2.4GHZ,256SAM_VRAM,M98	M98_COMMON,EEE_0ZA,CPU_2_4GHZ,FB_256_SAMSUNG
630-9335	PCBA,2.4GHZ,256HYN_VRAM,M98	M98_COMMON,EEE_0ZB,CPU_2_4GHZ,FB_256_HYNIX
630-9336	PCBA,2.5GHZ,512SAM_VRAM,M98	M98_COMMON,EEE_0ZC,CPU_2_5GHZ,FB_512_SAMSUNG
630-9337	PCBA,2.5GHZ,512QIM_VRAM,M98	M98_COMMON,EEE_0ZD,CPU_2_5GHZ,FB_512_QIMONDA
630-9585	PCBA,2.8GHZ,512SAM_VRAM,M98	M98_COMMON,EEE_2NH,CPU_2_8GHZ,FB_512_SAMSUNG
630-9586	PCBA,2.8GHZ,512QIM_VRAM,M98	M98_COMMON,EEE_2NJ,CPU_2_8GHZ,FB_512_QIMONDA

M98 BOM Groups

BOM GROUP	BOM OPTIONS
M98_COMMON	ALTERNATE,COMMON,M98_COMMON1,M98_COMMON2,M98_COMMON3,M98_DEBUG,M98_PROGPARTS
M98_COMMON1	ONEWIRE_PU,ISL6258A,MEMRESET_HW,MEMRESET_MCP,MCP_B02,MCP_PROD,MCPSEQ_SMC
M98_COMMON2	BKLT_PLL_NOT,BMON_ENG,MIKEY,BOOT_MODE_USER,GPUVID_1P00V,MUXGFX
M98_COMMON3	DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_HW,DP_CA_DET_EG_PLD,MCP_CS1_NO
M98_DEBUG	SMC_DEBUG_YES,XDP,LPCPLUS,VREFMRGN
M98_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_QIMONDA	VRAM4,VRAM_512_QIMONDA

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZA]	CRITICAL	EEE_0ZA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZB]	CRITICAL	EEE_0ZB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZC]	CRITICAL	EEE_0ZC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:0ZD]	CRITICAL	EEE_0ZD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2NH]	CRITICAL	EEE_2NH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2NJ]	CRITICAL	EEE_2NJ

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3639	1	IC,PDC,SLB4N,PRQ,2.4G,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3640	1	IC,PDC,SL3BX,PRQ,2.53G,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
338S0554	1	IC,GPU,55nm,NV G96-GS,BGA969,LF	U8000	CRITICAL	
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER,48P TQFP	U3700	CRITICAL	
338S0523	1	IC,FW643-06,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0600	1	IC,GMCP,MCP79-B01,35x35MM,BGA1437	U1400	CRITICAL	MCP_B01
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2289	1	IC,SMC,DEVELOPMENT,M98	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2366	1	IC,EFI ROM,DEVELOPMENT,M98	U6100	CRITICAL	BOOTROM_PROG
341S2272	1	IC,HDCP ROM,NVG96, 8 PIN SOIC,LF,HF	U8770	CRITICAL	HDCP_YES
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
338S0635	1	IC,GMCP,MCP79-B02,35x35MM,BGA1437	U1400	CRITICAL	MCP_B02
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3641	1	IC,PDC,SLB43,PRQ,2.8G,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_8GHZ
333S0482	4	IC,SGRAM,GDDR3,16Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0481	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
353S1681	353S1294		ALL	LMV2011,OPAMP. GBW
152S0276	152S0683		ALL	Maglayers alt to Dale/Vishay
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0867		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
353S2312	353S1466		ALL	INTERSIL ALT TO INTERSIL
514-0612	514-0607		ALL	FOXLINK XCVR ALT TO FOXCONN
514-0613	514-0608		ALL	FOXLINK RCVR ALT TO FOXCONN
152S0915	152S0796		ALL	Maglayers alt to Cyntec IND

BOM Configuration

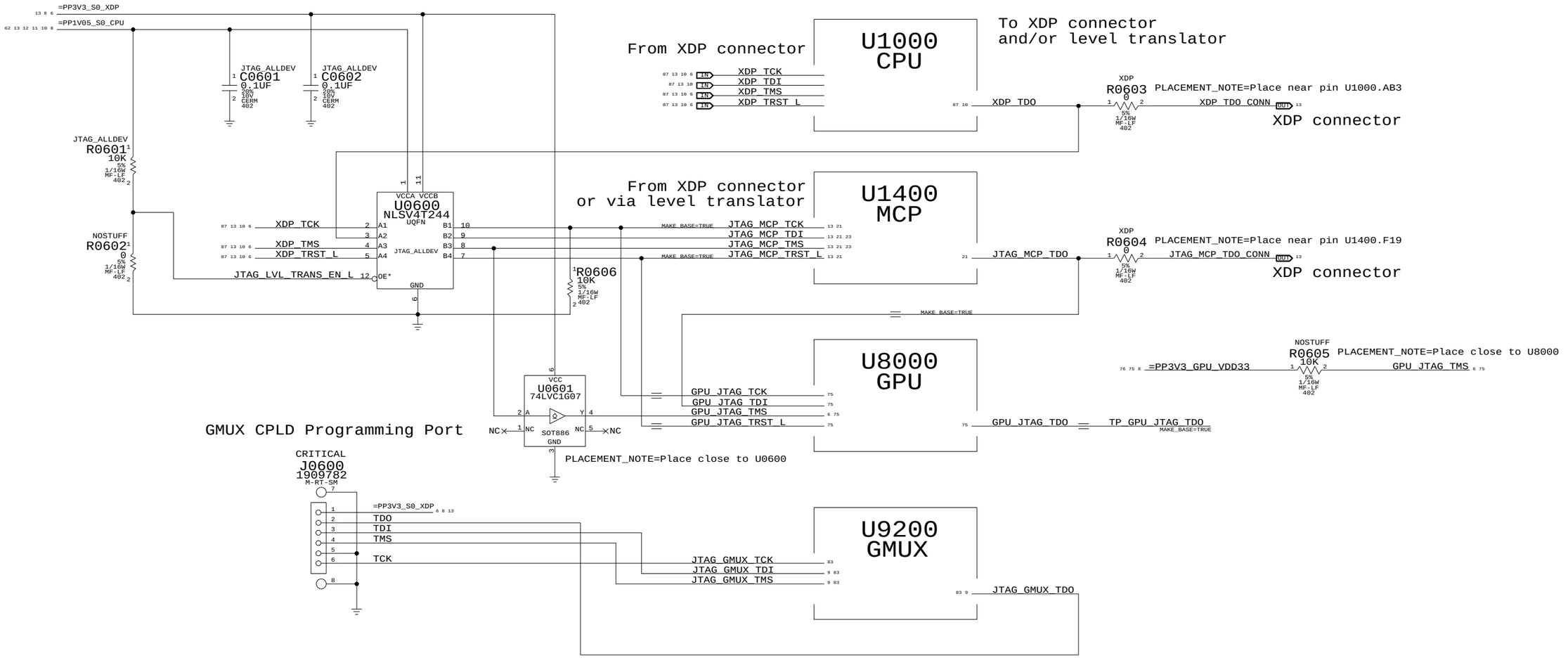
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE D | DRAWING NUMBER 051-7546 | REV. A.0.0

SCALE NONE | SHT 5 OF 96

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 6 OF 96	

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 49	3 TPs per Fan
TRUE	FAN_LT_PWM	49	
TRUE	FAN_LT_TACH	49	
TRUE	FAN_RT_PWM	49	
TRUE	FAN_RT_TACH	49	5 TPs per Fan
TRUE	GND		

LVDS Connectors

FUNC_TEST

L566	TRUE	=PP3V3_S0_DDC_LCD	8 76 79
L567	TRUE	PP3V3_SW_LCD	79
L570	TRUE	BKL_SYNC	79 84
L571	TRUE	LVDS_DDC_CLK	79 80
L572	TRUE	LVDS_DDC_DATA	79 80
L573	TRUE	LVDS_CONN_A_DATA_N<0>	79 80 94
L569	TRUE	LVDS_CONN_A_DATA_P<0>	79 80 94
L574	TRUE	LVDS_CONN_A_DATA_N<1>	79 80 94
L566	TRUE	LVDS_CONN_A_DATA_P<1>	79 80 94
L573	TRUE	LVDS_CONN_A_DATA_N<2>	79 80 94
L575	TRUE	LVDS_CONN_A_DATA_P<2>	79 80 94
L577	TRUE	LVDS_CONN_A_CLK_F_N	79 94
L578	TRUE	LVDS_CONN_A_CLK_F_P	79 94
L579	TRUE	LVDS_CONN_B_DATA_N<0>	79 80 94
L580	TRUE	LVDS_CONN_B_DATA_P<0>	79 80 94
L581	TRUE	LVDS_CONN_B_DATA_N<1>	79 80 94
L582	TRUE	LVDS_CONN_B_DATA_P<1>	79 80 94
L583	TRUE	LVDS_CONN_B_DATA_N<2>	79 80 94
L584	TRUE	LVDS_CONN_B_DATA_P<2>	79 80 94
L585	TRUE	LVDS_CONN_B_CLK_F_N	79 94
L586	TRUE	LVDS_CONN_B_CLK_F_P	79 94
L587	TRUE	LED_RETURN_1	79 84
L588	TRUE	LED_RETURN_2	79 84
L589	TRUE	LED_RETURN_3	79 84
L590	TRUE	LED_RETURN_4	79 84
L592	TRUE	LED_RETURN_5	79 84
L593	TRUE	LED_RETURN_6	79 84

EXCARD Connector

FUNC_TEST

L642	TRUE	USB2_EXCARD_CONN_N	32 95
L643	TRUE	USB2_EXCARD_CONN_P	32 95
L644	TRUE	PCIE_CLK100M_EXCARD_CONN_N	32 95
L645	TRUE	PCIE_CLK100M_EXCARD_CONN_P	32 95
L646	TRUE	PCIE_EXCARD_R2D_N	32 89 95
L648	TRUE	PCIE_EXCARD_R2D_P	32 89 95
L647	TRUE	PCIE_EXCARD_D2R_P	17 32 89
L650	TRUE	PCIE_EXCARD_D2R_N	17 32 89
L649	TRUE	PP3V3_S3_EXCARD_SWITCH	32
L651	TRUE	PP3V3_S0_EXCARD_SWITCH	32
L653	TRUE	PP1V5_S0_EXCARD_SWITCH	32
L652	TRUE	PLT_RESET_SWITCH_L	32
L654	TRUE	EXCARD_CPPE_L	32
L655	TRUE	EXCARD_CPUSB_L	32
L641	TRUE	EXCARD_CLKREQ_CONN_L	32
L657	TRUE	SMBUS_MCP_0_CLK	13 21 45 90
L656	TRUE	SMBUS_MCP_0_DATA	13 21 45 90

Speaker Connectors

FUNC_TEST

L557	TRUE	BI_MIC_LO	58 59
L558	TRUE	BI_MIC_SHIELD	58 59
L559	TRUE	BI_MIC_HI	58 59
L560	TRUE	SPKRCONN_L_P_OUT	57 58 95
L561	TRUE	SPKRCONN_L_N_OUT	57 58 95
L562	TRUE	SPKRCONN_R_P_OUT	57 58 95
L563	TRUE	SPKRCONN_R_N_OUT	57 58 95
L564	TRUE	SPKRCONN_S_P_OUT	57 58 95
L565	TRUE	SPKRCONN_S_N_OUT	57 58 95
	TRUE	GND	6 TPs

SATA ODD Connectors

FUNC_TEST

L599	TRUE	PP5V_SW_ODD	39 4 TPs
L594	TRUE	SMC_ODD_DETECT	39 42
L596	TRUE	SATA_ODD_R2D_P	39 89
L597	TRUE	SATA_ODD_R2D_N	39 89
L602	TRUE	SATA_ODD_D2R_C_N	39 89
L598	TRUE	SATA_ODD_D2R_C_P	39 89
	TRUE	GND	5 TPs

POWER RAILS

L605	TRUE	PM_SLP_S3_L	21 34 37 42 44 68 81 83
L609	TRUE	PPBUS_G3H	8 46
L606	TRUE	PPBUS_CPU_IMVP_ISNS	8
L608	TRUE	PP3V42_G3H	7 8 43
L604	TRUE	PP5V_S3	8
L603	TRUE	PP5V_S0	8
L607	TRUE	PPVCORE_S0_CPU	8
L610	TRUE	PPVCORE_S0_MCP_REG	8
L600	TRUE	PPVCORE_S0_MCP	
L616	TRUE	PP3V3_S5	8 95
L612	TRUE	PP3V3_S3	8
L614	TRUE	PP3V3_S0	8 95
L613	TRUE	PP2V5_S0	8
L615	TRUE	PP1V2_S0	8
L620	TRUE	PP1V8_S0	8
L624	TRUE	PP1V8R1V5_S3	8
L625	TRUE	PP1V8R1V5_S0_FET	8
L622	TRUE	PPMCPDDR_ISNS	8
L626	TRUE	PP1V05_S0_REG	8
L623	TRUE	PP1V2R1V05_S5	8
L618	TRUE	PPCPUVTT_S0	8
L619	TRUE	PPCPUFSB_ISNS_R	
L617	TRUE	PP0V9R0V75_S0_DDRVTT	8
L635	TRUE	PP1V2R1V05_ENET	8
L636	TRUE	PP3V3_ENET_PHY	8
L634	TRUE	PPVP_FW	8
L627	TRUE	PP1V0_FW	8
L630	TRUE	PP3V3_S0GPU	8
L633	TRUE	PP1V1_S0GPU_REG	8
L628	TRUE	PP1V8_S0GPU_ISNS	8
L637	TRUE	PPVCORE_GPU	8
L629	TRUE	PP1V8_S0GPU_ISNS_R	8
L601	TRUE	PP3V3_S5_AVREF_SMC	42 43
L632	TRUE	PPVOUT_S0_LCDBKLT	79 84
L631	TRUE	PPDCIN_G3H	8
L621	TRUE	PPVTTDDR_S3	8
L605	TRUE	PP1V8_GPUIFPX	8

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

	TRUE	FSB_A_L<31..3>	10 14 87
	TRUE	FSB_ADS_L	10 14 87
	TRUE	FSB_ADSTB_L<1..0>	10 14 87
	TRUE	FSB_D_L<63..0>	10 14 87
	TRUE	FSB_DINV_L<3..0>	10 14 87
	TRUE	FSB_DSTB_L_N<3..0>	10 14 87
	TRUE	FSB_DSTB_L_P<3..0>	10 14 87
	TRUE	FSB_HIT_L	10 14 87
	TRUE	FSB_HITM_L	10 14 87
	TRUE	FSB_LOCK_L	10 14 87
	TRUE	FSB_REQ_L<4..0>	10 14 87

IPD_FLEX_CONN

L757	TRUE	PP3V3_S3_LDO	51
L758	TRUE	PP18V5_S3	51
L760	TRUE	TPAD_GND_F	7 51
L756	TRUE	Z2_CS_L	50 51
L753	TRUE	Z2_DEBUG3	50 51
L752	TRUE	Z2_MOSI	50 51
L754	TRUE	Z2_MISO	50 51
L755	TRUE	Z2_SCLK	50 51
L761	TRUE	Z2_BOOST_EN	51
L749	TRUE	Z2_HOST_INTN	50 51
L750	TRUE	Z2_BOOT_CFG1	50 51
L748	TRUE	Z2_CLKIN	50 51
L746	TRUE	Z2_KEY_ACT_L	50 51
L747	TRUE	Z2_RESET	50 51
L745	TRUE	PSOC_MISO	50 51
L744	TRUE	PSOC_MOSI	50 51
L743	TRUE	PSOC_SCLK	50 51
L741	TRUE	SMBUS_SMC_A_S3_SDA	45 93
L742	TRUE	SMBUS_SMC_A_S3_SCL	45 93
L740	TRUE	PSOC_F_CS_L	50 51
L739	TRUE	PICKB_L	50 51

KEYBOARD CONN

L730	TRUE	PP3V42_G3H	7 8 43
L737	TRUE	WS_KBD1	50
L735	TRUE	WS_KBD2	50
L734	TRUE	WS_KBD3	50
L733	TRUE	WS_KBD4	50
L731	TRUE	WS_KBD5	50
L732	TRUE	WS_KBD6	50
L736	TRUE	WS_KBD7	50
L728	TRUE	WS_KBD8	50
L729	TRUE	WS_KBD9	50
L726	TRUE	WS_KBD10	50
L727	TRUE	WS_KBD11	50
L724	TRUE	WS_KBD12	50
L722	TRUE	WS_KBD13	50
L725	TRUE	WS_KBD14	50
L723	TRUE	WS_KBD15_CAP	50
L721	TRUE	WS_KBD16_NUM	50
L720	TRUE	WS_KBD17	50
L718	TRUE	WS_KBD18	50
L719	TRUE	WS_KBD19	50
L717	TRUE	WS_KBD20	50
L716	TRUE	WS_KBD21	50
L710	TRUE	WS_KBD22	50
L715	TRUE	WS_KBD23	50
L714	TRUE	WS_KBD_ONOFF_L	50
L712	TRUE	WS_LEFT_SHIFT_KBD	50
L711	TRUE	WS_LEFT_OPTION_KBD	50
L710	TRUE	WS_CONTROL_KBD	50
L709	TRUE	KBDLED_ANODE	51
L762	TRUE	TPAD_GND_F	7 51

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 7 OF 96

"G3Hot" (Always-Present) Rails

=PPBUS_G3H (61) — PPBUS_G3H (7 46)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVIN_S5_P5VP3V3 (63)
- =PPVIN_S0_CPUVTTS0 (66)
- =PPBUS_S0_LCDBKLT (85)
- =PPBUS_S5_FWPWRSW (37)
- =PPVIN_GPU_GPUVCORE (78)
- =PPVIN_S5_CPU_IMVP_ISNS_R (46)
- =PPVIN_S0_P5VRTS0_MCPCORE (65)
- =PPVIN_S3_DDRREG (64)
- =PPVIN_S0GPU_P1V8P1V1 (82)
- =PPVBAT_G3H_P3V42G3H (60)
- =PPVIN_S0_P1V05S5 (67)

=PPVIN_S5_CPU_IMVP_ISNS (46) — PPBUS_CPU_IMVP_ISNS (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVIN_S5_CPU_IMVP (62)

=PP18V5_DCIN_CONN (60) — PPDCIN_G3H (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR (61)

=PP3V42_G3H_REG (60) — PP3V42_G3H (7 43)
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V42_G3H_SMCUSBMUX (40)
- =PP3V42_G3H_SMBUS_SMC_BSA (45)
- =PP3V42_G3H_LIDSWITCH (41)
- =PP3V3_S5_SMC (42 43 52)
- =PP3V3_S5_LPCPLUS (44)
- =PPVIN_S5_SMCVREF (43)
- =PP3V42_G3H_PWRCTL (63 68)
- =PP3V42_G3H_CHGR (61)
- =PP3V3_S5_RTC_D (26)
- =PP3V42_G3H_BATT (60)
- =PP3V42_G3H_TPAD (50)
- =PP3V42_G3H_BMON_ISNS (46)
- =PP3V42_G3H_CPUCOREISNS (46)

5V Rails

=PP5V_S3_REG (63) — PP5V_S3 (7)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_SYSLED (43)
- =PP5V_S3_BTCAMERA (31)
- =PP5V_S3_WLAN (31)
- =PP5V_S3_IR (41)
- =PP5V_S3_DDRREG (64)
- =PP5V_S3_GPUVCORE (78)
- =PP5V_S3_RTUSB (40)
- =PP5V_S3_TPAD (51)
- =PP5V_S3_P1V05S0FET (69)
- =PP5V_S3_MCPDDRFET (69)
- =PP5V_S3_VTTCLAMP (69)
- =PP5V_S3_AUDIO_PWR (9)

=PP5V_RT_REG (65) — PP5V_S0 (7)
MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_FAN_LT (7 49)
- =PP5V_S0_FAN_RT (49)
- =PP5V_S0_CPU_IMVP (62)
- =PP5V_S0_CPUVTTS0 (66)
- =PP5V_S0_KBDLED (51)
- =PP5V_S0GPU_P1V1P1V8_GPU (82)
- =PP5V_S0_LPCPLUS (44)
- =PP5V_S0_ODD (39)
- =PP5V_S0_HDD (39)

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG (62) — PPVCORE_S0_CPU (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU (11 12 46)

=PPMCPCORE_S0_REG (65) — PPVCORE_S0_MCP_REG (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_MCP (22 24 46)

3.3V-2.5V Rails

=PP3V3_S5_REG (63) — PP3V3_S5 (7 95)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_MCP_A01 (23 44)
- =PP3V3_S5_ROM (44 53)
- =PP3V3_S5_MEMRESET (30)
- =PP3V3_S3_P3V3S3FET (69)
- =PP3V3_S5_LCD (79)
- =PP3V3_S0_P3V3S0FET (69)
- =PP3V3_GPU_P3V3GPUFET (69)
- =PP3V3_S5_PWRCTL (68)
- =PP3V3_S5_P1V05FET (69)
- =PP3V3_S5_MCP (22 24)
- =PP3V3_S5_MCP_GPIO (18 20)
- =PP3V3_FW_LATEVG_ACTIVE (37)
- =PP3V3_S5_MCPPWRGD (26)
- =PP3V3_FW_LATEVG (38)
- =PP3V3_S5_P1V05ENETFET (34)
- =PP3V3_S5_P3V3ENETFET (34)
- =PP3V3_S5_DP_PORT_PWR (81)

=PP3V3_S3_FET (69) — PP3V3_S3 (7)
MIN_LINE_WIDTH=0.58MM
MIN_NECK_WIDTH=0.28MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_FW_REG (8)
- =PP3V3_S3_SMBUS_SMC_A_S3 (45)
- =PP3V3_S3_SMS (52)
- =PP3V3_S3_REMTHMSNS (48)
- =PP3V3_S3_TPAD (50)
- =PP3V3_S3_WLAN (31)
- =PP3V3_S3_MCP_GPIO (21)
- =PP3V3_S3_VREFMRGN (27)
- =PP3V3_S3_SMBUS_SMC_MGMT (45)
- =PP3V3_S3_EXCARD (32)
- =PP3V3_S3_P1V8S0 (67)

=PP3V3_S0_FET (69) — PP3V3_S0 (7 95)
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_S0_LPCPLUS (44)
- =PP3V3_S0_SMC (43)
- =PP3V3_S0_SMBUS_SMC_B_S0 (45)
- =PP3V3_S0_MCPDDRISNS (47)
- =PP3V3_S0_GPU1V8ISNS (47)
- =PP3V3_S0_CPUTHMSNS (48)
- =PP3V3_S0_GPUTHMSNS (48)
- =PP3V3_S0_FAN_LT (49)
- =PP3V3_S0_FAN_RT (49)
- =PP3V3_S0_IMVP (62)
- =PP3V3_S0_PWRCTL (68)
- =PP3V3_S0_DDC_LCD (7 76 79)
- =PP3V3_S0_XDP (6 13)
- =PP3V3_S0_MCPCOREISNS (47)
- =PPSPD_S0_MEM_A (28)
- =PPSPD_S0_MEM_B (29)
- =PP3V3_S0_SMBUS_MCP_0 (45)
- =PP3V3_S0_GMUX (83)
- =PP3V3_S0_DPMUX (80)
- =PP3V3_S0_DPCONN (81)
- =PP3V3_S0_P1V2P2V5 (86)
- =PP3V3_S0_MCP_GPIO (18 19 21)
- =PP3V3_S0_HDCPROM (25)
- =PP3V3R1V5_S0_MCP_HDA (21 24)
- =PP3V3_S0_MCP_PLL_UF (24)
- =PP3V3_S0_MCP_VPLL_UF (25)
- =PP3V3_S0_MCP_DAC_UF (25)
- =PP3V3_S0_MCP (21 22 24)
- =PP3V3_S0_AUDIO (54 58 59)
- =PP3V3_S0_ODD (39)
- =PP3V3_S0_VMON (68)
- =PP3V3_S0_SMBUS_MCP_1 (45)
- =PP3V3_FC_CON (32)
- =PP3V3_S0_EXCARD (32)
- =PP3V3_S0_LVDSDDCMUX (80)
- =PP3V3_S0_BATTCHARGERTMPSNSR (48)
- =PP3V3_GPU_SMBUS_SMC_0_S0 (45)
- =PP3V3_S0_TPAD (51)

=PP2V5_S0_REG (86) — PP2V5_S0 (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE
- =PP2V5_S0_GMUX (83)

=PP1V2_S0_REG (86) — PP1V2_S0 (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
- =PP1V2_S0_GMUX (83)

1.8V/DDR 1.5V Rails

=PP1V8_S0_REG (67) — PP1V8_S0 (7)
500 mA max supply
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- 190 mA =PP3V3R1V8_S0_MCP_IFP_VDD (18 25)

=PPDDR_S3_REG (64) — PP1V8R1V5_S3 (7)
MIN_LINE_WIDTH=0.8 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V8R1V5_S0_MCP_FET (69)
- =PPVIN_S0_DDRREG_LDO (64)
- =PP1V5_S3_MEM_A (28)
- =PP1V5_S3_MEM_B (29)
- =PP1V5_S3_MEMRESET (30)

=PP1V8R1V5_S0_FET (69) — PP1V8R1V5_S0_FET (7)
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- 4771 mA =PPMCPDDR_ISNS_R (47)
- 130 mA =PP1V5_S0_CPU (11 12)
- 500 mA =PP1V5_S0_EXCARD (32)
- =PP1V5_S0_VMON (68)
- =PP1V5_FC_CON (32)

=PP1V8R1V5_S0_MCP_MEM (24 16) — PPMCPDDR_ISNS (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S0_MEM_A (28)
- =PP1V5_S0_MEM_B (29)
- =PPMCPDDR_ISNS (47)

=PP1V05_S0_FET (69) — PP1V05_S0_REG (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- 1034 mA =PP1V05_S0_MCP_AVDD_UF (24)
- =PP1V05_S0_MCP_PEX_DVDD (8 24)
- =PP1V05_S0_MCP_PLL_UF (24)
- =PP1V05_S0_MCP_SATA_DVDD (8 24)
- =PP1V05_S0_MCP_HDMI_VDD (18 25)
- =PP1V05_S0_VMON (68)

=PP1V05_S0_MCP_PEX_DVDD (24 8) — =PP1V05_S0_MCP_PEX_DVDD0 (17)
=PP1V05_S0_MCP_PEX_DVDD1 (17)

PP1V05_S0_MCP_PEX_AVDD (24) MAKE_BASE=TRUE — =PP1V05_S0_MCP_PEX_AVDD0 (17)
=PP1V05_S0_MCP_PEX_AVDD1 (17)

=PP1V05_S0_MCP_SATA_DVDD (24 8) — =PP1V05_S0_MCP_SATA_DVDD0 (20)

PP1V05_S0_MCP_SATA_AVDD (24) MAKE_BASE=TRUE — =PP1V05_S0_MCP_SATA_AVDD0 (20)

=PP1V05_S5_MCP (67) — PP1V2R1V05_S5 (1.1V for A01) (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- 241 mA max load
- 105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC (22 24)
- 139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET (34)
- =PP1V05_S5_P1V05S0FET (69)

=PPCPUVTT_S0_REG (66) — PPCPUVTT_S0 (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- 5300 mA
- 4500 mA =PP1V05_S0_CPU (6 10 11 12 13 62)
- =PP1V05_S0_SMC_LS (43)
- 1182 mA =PP1V05_S0_MCP_FSB (9 14 22 24)

=PPVTT_S3_DDR_BUF (64 27) — PPVTTDDR_S3 (7)
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO (64) — PP0V9R0V75_S0_DDRVTT (7)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A (28)
- =PP0V75_S0_MEM_VTT_B (29)
- =PPVTT_S0_VTTCLAMP (69)
- OR 0.75V

ENET Rails

=PP1V05_ENET_FET (34) — PP1V2R1V05_ENET (7)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_ENET_MCP_PLL_MAC (24)
- =PP1V05_ENET_MCP_RMGT (18 24)
- =PP1V05_ENET_PHY (33)

=PP3V3_ENET_FET (34) — PP3V3_ENET_PHY (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_ENET_MCP_RMGT (18 24)
- =PP3V3_ENET_PHY (33)

"FW" (FireWire) Rails

=PPBUS_S5_FW_FET (37) — PPVP_FW (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVP_FW_PORT1 (38)
- =PPVP_FW_PHY_CPS_FET (38)

=PP3V3_FW_REG (8) — =PP3V3_FW_FWPHY (36 38)
- =PP3V3_FW_P1V0FW (67)

=PP1V0_FW_REG (67) — PP1V0_FW (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V0_FW_FWPHY (36)

"GPU" Rails

=PP3V3_S0GPU_FET (69) — PP3V3_S0GPU (7)
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_GPU_VDD33 (6 75 76)
- =PP3V3_GPU_MIO (75 76)
- =PP3V3_GPU_LVDS_DDC (80)
- =PP3V3_GPU_PWRCTL (68)
- =PP3V3_GPU_VCORELOGIC (78)
- =PP3V3_GPU_P1V8S0 (67)

=PP1V1_S0GPU_REG (82) — PP1V1_S0GPU_REG (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE
- =PP1V1_GPU_PEX_IOVDDQ (70)
- =PP1V1_GPU_PEX_IOVDD (70)
- =PP1V1_GPU_PEX_PLLXVDD (70)
- =PP1V1_GPU_PLLVDD (75)
- =PP1V1_GPU_H_PLLVDD (75)
- =PP1V1_GPU_VID_PLLVDD (75)
- =PP1V1_GPU_FBPLLAVDD (72)
- =PP1V1_GPU_IFPCD_IOVDD (77)

=PP1V8_GPUIFPX_REG (67) — PP1V8_GPUIFPX (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_GPU_IFPX (77)

=PP1V8_S0GPU_ISNS (47) — PP1V8_S0GPU_ISNS (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_GPU_FB_VDD (73 74)
- =PP1V8_GPU_FB_VDDQ (9 73 74)
- =PP1V8_GPU_FBVDDQ (71)
- =PP1V8_GPU_FBIO (72)

=PPVCORE_GPU_REG (78 46) — PPVCORE_GPU (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.4V
MAKE_BASE=TRUE
- =PPVCORE_GPU (71)

=PP1V8_GPU_REG (82) — PP1V8_S0GPU_ISNS_R (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0GPU_ISNS_R (47)

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	8	96

Thermal Module Holes

ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
Bottom Left GPU TM Hole
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0950 TH — GND_CHASSIS_FAN (SL-3.1X2.7-6CIR-NSP)
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0990 3R2P5 — GND_CHASSIS_BATTCONN

=PP1V8_GPU_FB_VDDQ
R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV — =PP1V8_GPU_FB_VREF_A
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV — =PP1V8_GPU_FB_VREF_B

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

=PP1V05_S0_MCP_FSB
R0950 NO STUFF 220 5% 1/16W MF-LF 402
R0970 NO STUFF 200 5% 1/16W MF-LF 402
R0990 NO STUFF 150 1% 1/16W MF-LF 402
R0960 NO STUFF 62 5% 1/16W MF-LF 402
R0980 NO STUFF 150 1% 1/16W MF-LF 402

CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI

Bosses for VRAM HS

ZT0951 4.0OD1.65H-M1.6X0.35
ZT0952 4.0OD1.65H-M1.6X0.35
ZT0953 4.0OD1.65H-M1.6X0.35

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L
CPU_VID<0..6> — IMVP6_VID<0..6>
CPU_BSEL<0..2> — =MCP_BSEL<0..2>
MEM_VTT_EN — =DDRVTT_EN
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB

GPU signals

PEG_D2R_P<0..15> — =PEG_D2R_P<0..15>
PEG_D2R_N<0..15> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15>

PCIE_CLK100M_FC_P — TP_PCIE_CLK100M_PE4P
PCIE_CLK100M_FC_N — TP_PCIE_CLK100M_PE4N
PCIE_FC_R2D_C_P — TP_PCIE_PE4_R2D_CP
PCIE_FC_R2D_C_N — TP_PCIE_PE4_R2D_CN
FC_CLKREQ_L — TP_PE4_CLKREQ_L
FC_PRSNT_L — TP_PE4_PRSNT_L
PCIE_FC_D2R_P — TP_PCIE_PE4_D2RP
PCIE_FC_D2R_N — TP_PCIE_PE4_D2RN

GMUX ALIASES

LCD_BKLT_EN — LVDS_BKL_ON
DP_IG_ML_P<3> — =MCP_HDMI_TXC_P
DP_IG_ML_N<3> — =MCP_HDMI_TXC_N
DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2>
DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2>
DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK
DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA
DP_IG_HPD — =MCP_HDMI_HPD
PM_ALL_GPU_PGOOD — ALL_EG_PGOOD
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG
EG_RESET_L — GPU_RESET_L

JTAG_GMUX_TDI — GMUX_JTAG_TDI
JTAG_GMUX_TMS — GMUX_JTAG_TMS
JTAG_GMUX_TDO — GMUX_JTAG_TDO
LVDS_IG_BKL_ON — IG_BKLT_EN
LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN

TP_USB_EXTDP — USB_EXTD_P
TP_USB_EXTDN — USB_EXTD_N
TP_USB_MINIP — USB_MINI_P
TP_USB_MININ — USB_MINI_N
GMUX_INT — =DVI_HPD_GMUX_INT

R0903 0 5% 1/16W MF-LF 402
MCP_SPKR — SMC_MCP_SAFE_MODE

TP_MEM_A_A<15> — MEM_A_A<15>
TP_MEM_B_A<15> — MEM_B_A<15>
TP_USB_EXTCP — USB_EXTC_P
TP_USB_EXTCN — USB_EXTC_N
TP_CPU_PECI_MCP — CPU_PECI_MCP
TP_MCP_GPIO_17 — AUD_IP_PERIPHERAL_DET
PCIE_RESET_L — FC_RESET_L

AUDIO ALIASES

HDA_BITCLK — HDA_BIT_CLK

XW0000
=PP5V_S3_AUDIO_PWR — PP5V_S3_AUDIO (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
XW0901
PP5V_S3_AUDIO_AMP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)

R0902 10K 5% 1/16W MF-LF 402
AUD_IPHS_SWITCH_EN

ETHERNET ALIASES

=P3V3ENET_EN — PM_SLP_RMGT_L
=P1V05ENET_EN
=PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
=RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG

ZT0934 STDOFF-4.00D3.0H-TH
ZT0935 STDOFF-4.00D3.0H-TH
ZT0931 STDOFF-4.00D3.0H-TH
ZT0932 STDOFF-4.00D3.0H-TH
ZT0933 STDOFF-4.00D3.0H-TH
VENICE

NC_LVDS_B_DATAP<3> — LVDS_B_DATA_P<3>
NC_LVDS_B_DATAN<3> — LVDS_B_DATA_N<3>
NC_LVDS_A_DATAP<3> — LVDS_A_DATA_P<3>
NC_LVDS_A_DATAN<3> — LVDS_A_DATA_N<3>
(MAKE_BASE=TRUE, NO_TEST=TRUE)

TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N
TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM

ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3>
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3>
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3>
NC_LVDS_A_DATAP<3> — LVDS_A_DATA_P<3>
NC_LVDS_A_DATAN<3> — LVDS_A_DATA_N<3>
NC_LVDS_B_DATAP<3> — LVDS_B_DATA_P<3>
NC_LVDS_B_DATAN<3> — LVDS_B_DATA_N<3>

MCP79 PCIe PRSNT# Straps

These need work. Add other PRSNT# straps if needed. .

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L
R0927 NO STUFF 0 5% 1/16W MF-LF 402 — PEG_PRSNT_L
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L

MCP_MII_PD
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER
=MCP_MII_CRS
=MCP_MII_COL

=PP1V05_S0_MCP_SATA_DVDD1
=PP1V05_S0_MCP_SATA_AVDD1

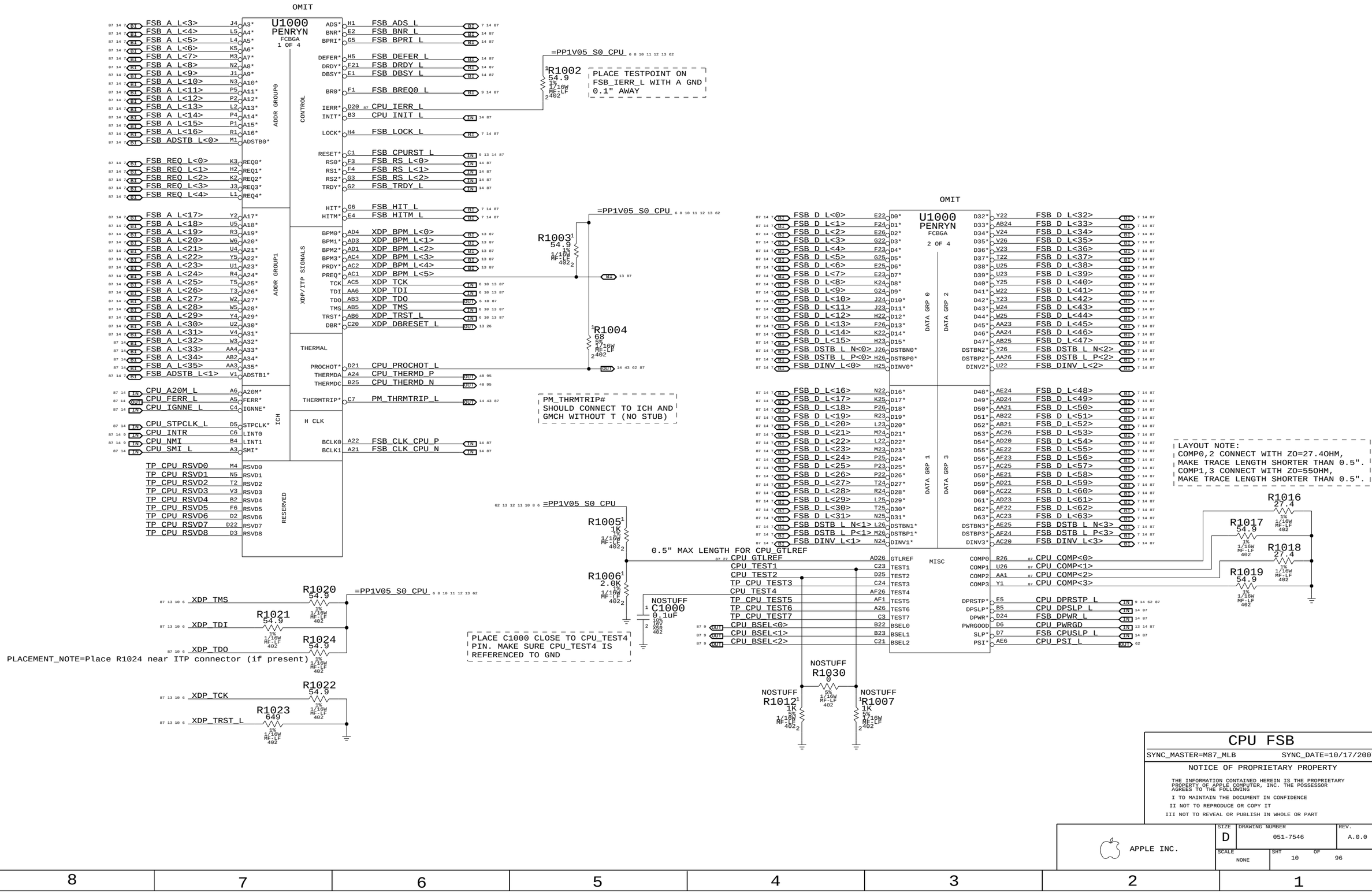
Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.09MM, VOLTAGE=0V)

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.
SIZE D | DRAWING NUMBER 051-7546 | REV. A.0.0
SCALE NONE | SHT 9 OF 96



CPU FSB

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 10 OF 96	

(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 46

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
3 OF 4

VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 6 8 10 12 13 62

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26 C26

VID0 AD6 CPU_VID<0> OUT 9 87
VID1 AF5 CPU_VID<1> OUT 9 87
VID2 AE5 CPU_VID<2> OUT 9 87
VID3 AF4 CPU_VID<3> OUT 9 87
VID4 AE3 CPU_VID<4> OUT 9 87
VID5 AF3 CPU_VID<5> OUT 9 87
VID6 AE2 CPU_VID<6> OUT 9 87

VCCSENSE AF7 CPU_VCCSENSE_P OUT 62 87
VSSSENSE AE7 CPU_VCCSENSE_N OUT 62 87

=PPVCORE_S0_CPU 8 11 12 46

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
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VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3 B1

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

CPU Power & Ground

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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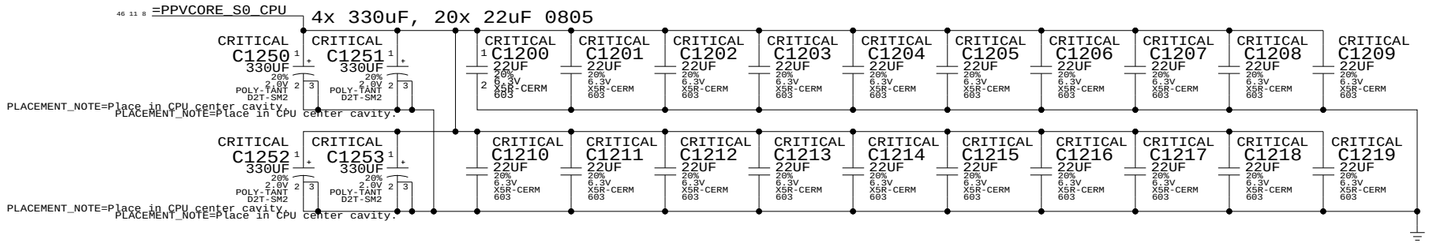
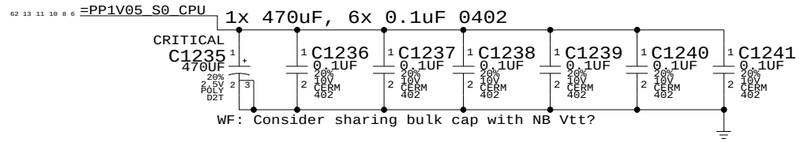
SCALE: NONE	SHT 11 OF 96	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

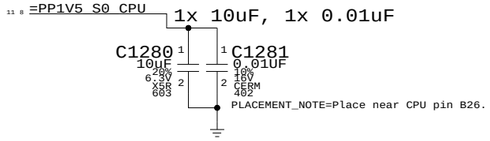
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

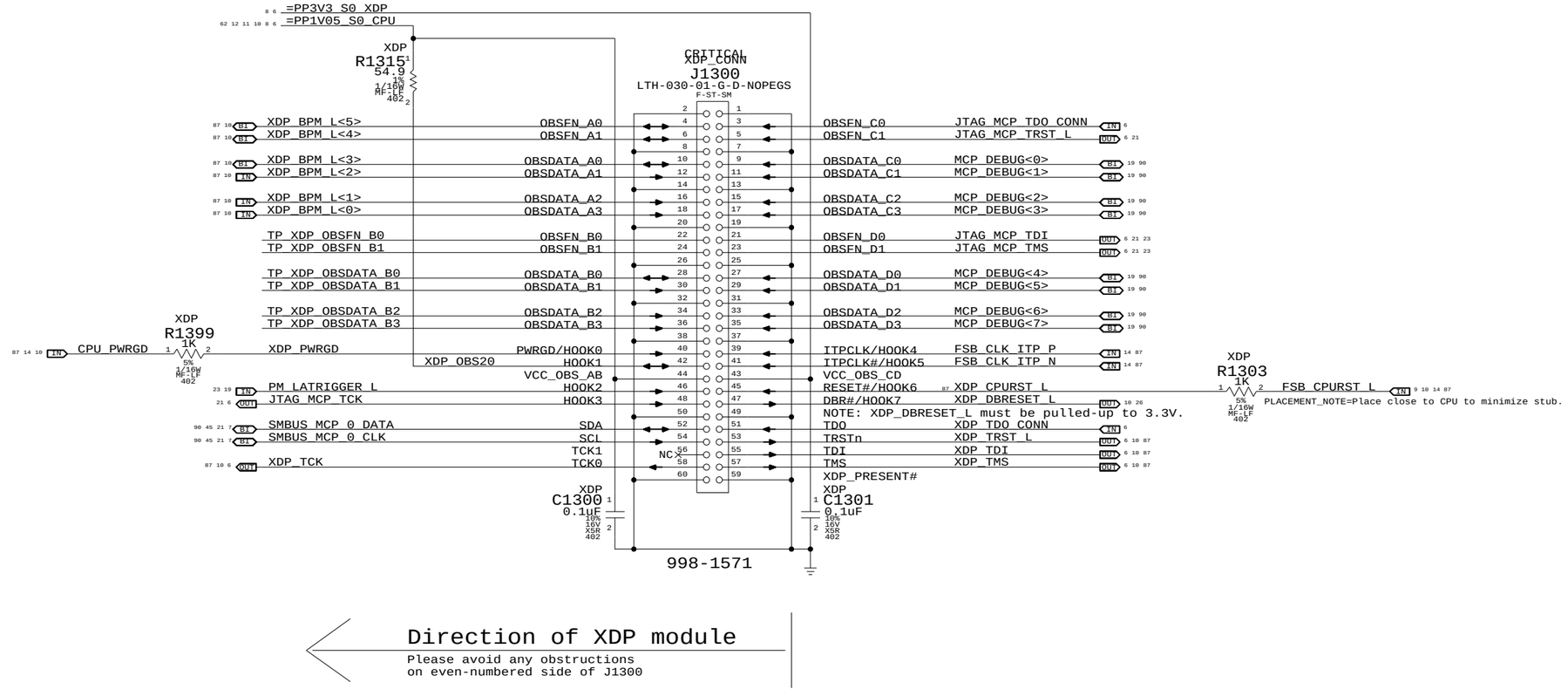
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 12 OF 96	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 13 OF 96	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
PP1V05_S0_MCP_PLL_FSB	AG27	+V_DLL_DLCELL_AVDD	206 mA
270 mA (A01)	AH27	+V_PLL_MCLK	20 mA
	AG28	+V_PLL_FSB	29 mA
	AH28	+V_PLL_CPU	15 mA
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0#	Y43	FSB_D_L<0>
CPU_D1#	W42	FSB_D_L<1>
CPU_D2#	Y40	FSB_D_L<2>
CPU_D3#	W41	FSB_D_L<3>
CPU_D4#	Y39	FSB_D_L<4>
CPU_D5#	V42	FSB_D_L<5>
CPU_D6#	Y41	FSB_D_L<6>
CPU_D7#	Y42	FSB_D_L<7>
CPU_D8#	P42	FSB_D_L<8>
CPU_D9#	U41	FSB_D_L<9>
CPU_D10#	R42	FSB_D_L<10>
CPU_D11#	T39	FSB_D_L<11>
CPU_D12#	T42	FSB_D_L<12>
CPU_D13#	T41	FSB_D_L<13>
CPU_D14#	R41	FSB_D_L<14>
CPU_D15#	T43	FSB_D_L<15>
CPU_D16#	W35	FSB_D_L<16>
CPU_D17#	AA37	FSB_D_L<17>
CPU_D18#	W33	FSB_D_L<18>
CPU_D19#	W34	FSB_D_L<19>
CPU_D20#	AA36	FSB_D_L<20>
CPU_D21#	AA34	FSB_D_L<21>
CPU_D22#	AA38	FSB_D_L<22>
CPU_D23#	AA35	FSB_D_L<23>
CPU_D24#	U38	FSB_D_L<24>
CPU_D25#	U36	FSB_D_L<25>
CPU_D26#	U35	FSB_D_L<26>
CPU_D27#	U33	FSB_D_L<27>
CPU_D28#	U34	FSB_D_L<28>
CPU_D29#	W38	FSB_D_L<29>
CPU_D30#	R33	FSB_D_L<30>
CPU_D31#	U37	FSB_D_L<31>
CPU_D32#	N34	FSB_D_L<32>
CPU_D33#	N33	FSB_D_L<33>
CPU_D34#	R34	FSB_D_L<34>
CPU_D35#	R35	FSB_D_L<35>
CPU_D36#	P35	FSB_D_L<36>
CPU_D37#	R39	FSB_D_L<37>
CPU_D38#	R37	FSB_D_L<38>
CPU_D39#	R38	FSB_D_L<39>
CPU_D40#	L37	FSB_D_L<40>
CPU_D41#	L39	FSB_D_L<41>
CPU_D42#	L38	FSB_D_L<42>
CPU_D43#	N36	FSB_D_L<43>
CPU_D44#	N38	FSB_D_L<44>
CPU_D45#	J39	FSB_D_L<45>
CPU_D46#	J38	FSB_D_L<46>
CPU_D47#	J37	FSB_D_L<47>
CPU_D48#	L42	FSB_D_L<48>
CPU_D49#	M42	FSB_D_L<49>
CPU_D50#	P41	FSB_D_L<50>
CPU_D51#	N41	FSB_D_L<51>
CPU_D52#	N40	FSB_D_L<52>
CPU_D53#	M40	FSB_D_L<53>
CPU_D54#	H40	FSB_D_L<54>
CPU_D55#	K42	FSB_D_L<55>
CPU_D56#	H41	FSB_D_L<56>
CPU_D57#	L41	FSB_D_L<57>
CPU_D58#	H43	FSB_D_L<58>
CPU_D59#	H42	FSB_D_L<59>
CPU_D60#	K41	FSB_D_L<60>
CPU_D61#	J40	FSB_D_L<61>
CPU_D62#	H39	FSB_D_L<62>
CPU_D63#	M43	FSB_D_L<63>
CPU_BPRI#	AA41	FSB_BPRI_L
CPU_DEFER#	AA40	FSB_DEFER_L
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N
BCLK_IN_N	AK41	
BCLK_IN_P	AJ40	
CPU_A20M#	AF41	CPU_A20M_L
CPU_IGNNE#	AH39	CPU_IGNNE_L
CPU_INIT#	AH42	CPU_INIT_L
CPU_INTR	AF42	CPU_INTR
CPU_NMI	AG41	CPU_NMI
CPU_SMI#	AH41	CPU_SMI_L
CPU_PWRGD	AH43	CPU_PWRGD
CPU_RESET#	H38	FSB_CPURST_L
CPU_SLP#	AM33	FSB_CPUSLP_L
CPU_DPSLP#	AN33	CPU_DPSLP_L
CPU_DPWR#	AM32	FSB_DPWR_L
CPU_STPCLK#	AG42	CPU_STPCLK_L
CPU_DPRSTP#	AN32	CPU_DPRSTP_L

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/10W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/10W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/10W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402

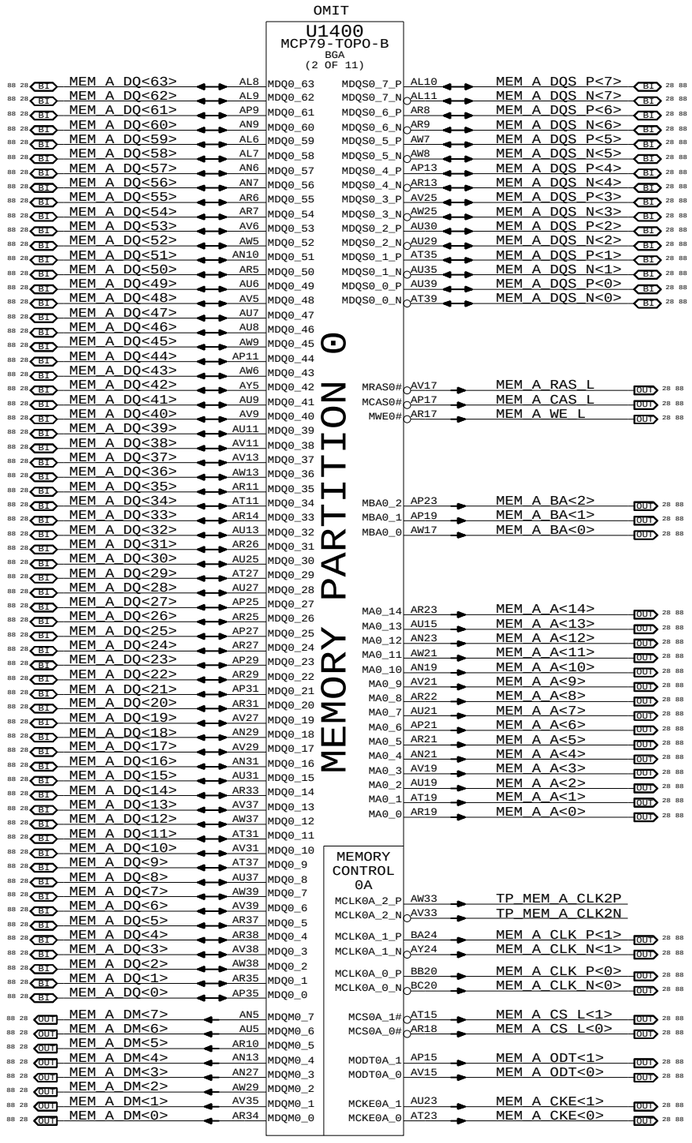
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

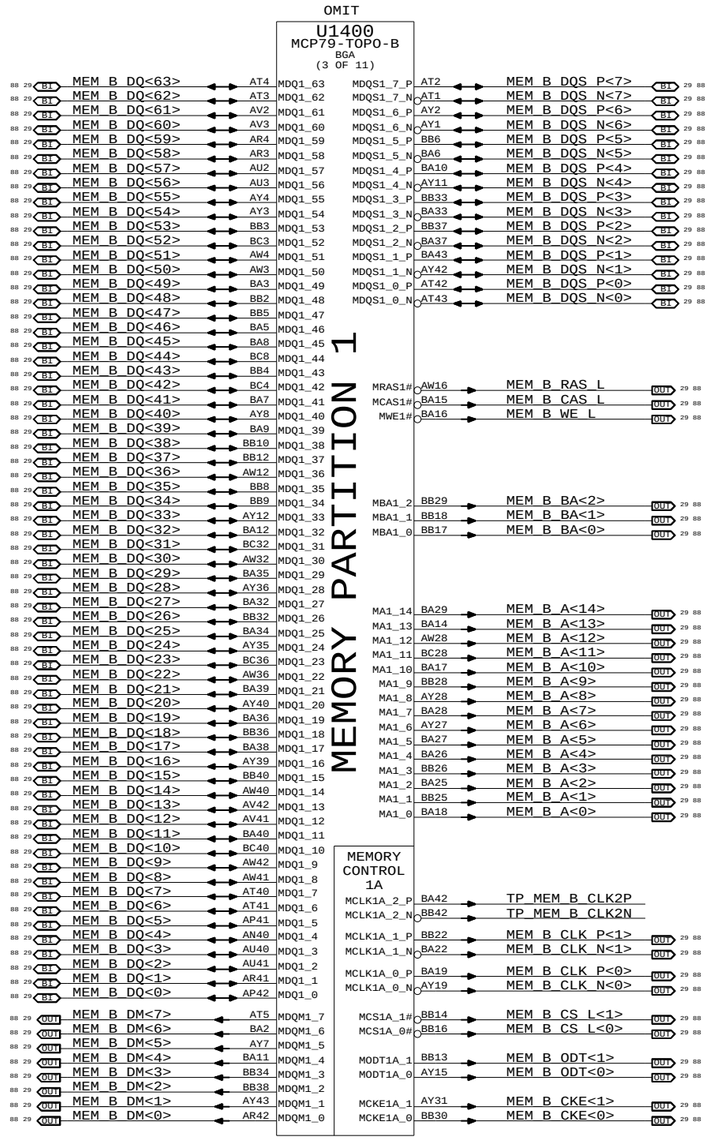
MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 14 OF 96	





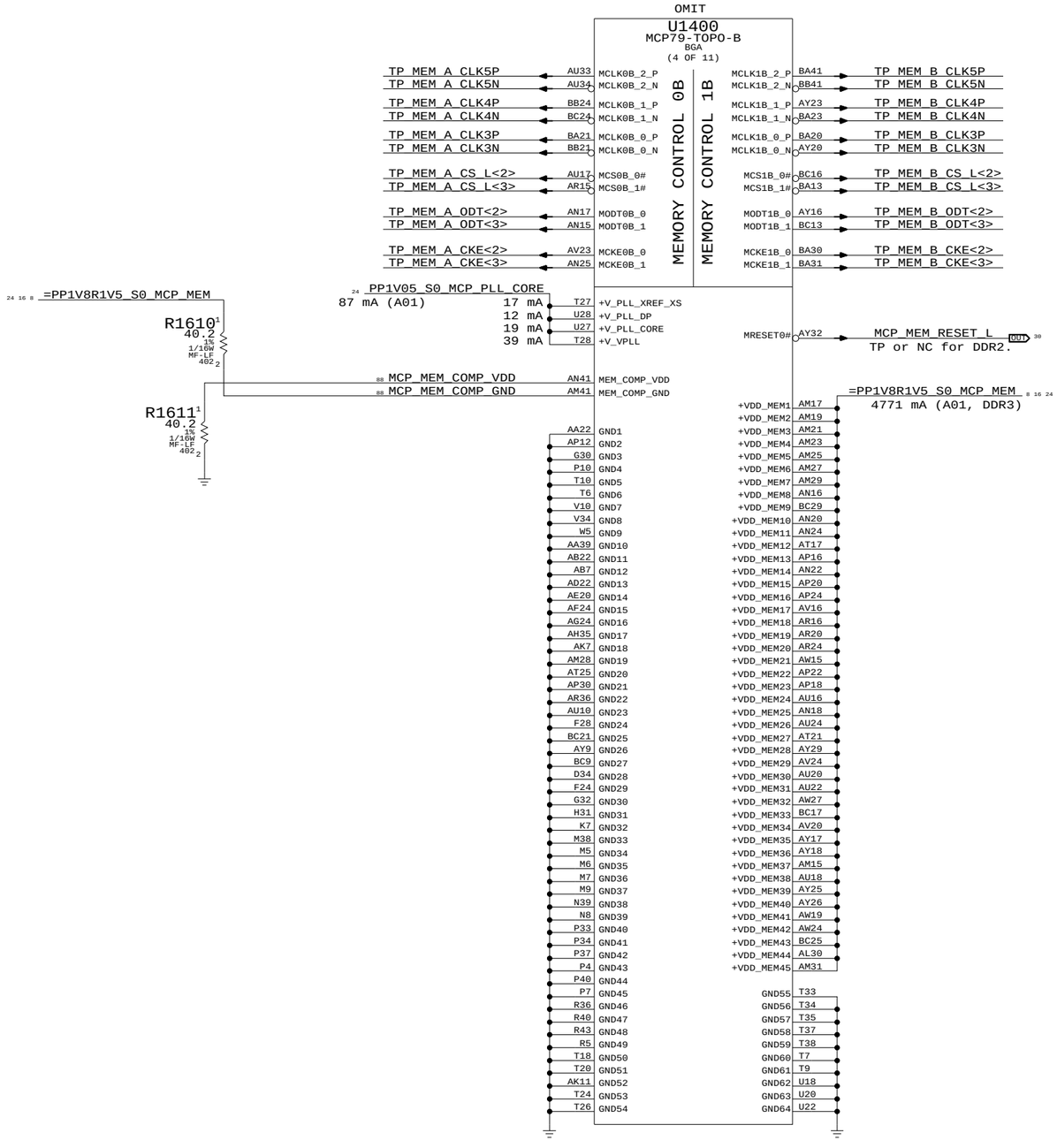
MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	15	96



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 16 OF 96	

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

9 IN	=PEG_D2R_P<0>	F7	PE0_RX0_P	PE0_TX0_P	C5	=PEG_R2D_C_P<0>	OUT 9
9 IN	=PEG_D2R_N<0>	E7	PE0_RX0_N	PE0_TX0_N	D4	=PEG_R2D_C_N<0>	OUT 9
9 IN	=PEG_D2R_P<1>	D7	PE0_RX1_P	PE0_TX1_P	C4	=PEG_R2D_C_P<1>	OUT 9
9 IN	=PEG_D2R_N<1>	C7	PE0_RX1_N	PE0_TX1_N	B4	=PEG_R2D_C_N<1>	OUT 9
9 IN	=PEG_D2R_P<2>	E6	PE0_RX2_P	PE0_TX2_P	A4	=PEG_R2D_C_P<2>	OUT 9
9 IN	=PEG_D2R_N<2>	F6	PE0_RX2_N	PE0_TX2_N	A3	=PEG_R2D_C_N<2>	OUT 9
9 IN	=PEG_D2R_P<3>	E5	PE0_RX3_P	PE0_TX3_P	B3	=PEG_R2D_C_P<3>	OUT 9
9 IN	=PEG_D2R_N<3>	F5	PE0_RX3_N	PE0_TX3_N	B2	=PEG_R2D_C_N<3>	OUT 9
9 IN	=PEG_D2R_P<4>	E4	PE0_RX4_P	PE0_TX4_P	C1	=PEG_R2D_C_P<4>	OUT 9
9 IN	=PEG_D2R_N<4>	E3	PE0_RX4_N	PE0_TX4_N	D1	=PEG_R2D_C_N<4>	OUT 9
9 IN	=PEG_D2R_P<5>	C3	PE0_RX5_P	PE0_TX5_P	D2	=PEG_R2D_C_P<5>	OUT 9
9 IN	=PEG_D2R_N<5>	D3	PE0_RX5_N	PE0_TX5_N	E1	=PEG_R2D_C_N<5>	OUT 9
9 IN	=PEG_D2R_P<6>	G5	PE0_RX6_P	PE0_TX6_P	E2	=PEG_R2D_C_P<6>	OUT 9
9 IN	=PEG_D2R_N<6>	H5	PE0_RX6_N	PE0_TX6_N	F2	=PEG_R2D_C_N<6>	OUT 9
9 IN	=PEG_D2R_P<7>	J7	PE0_RX7_P	PE0_TX7_P	F3	=PEG_R2D_C_P<7>	OUT 9
9 IN	=PEG_D2R_N<7>	J6	PE0_RX7_N	PE0_TX7_N	F4	=PEG_R2D_C_N<7>	OUT 9
9 IN	=PEG_D2R_P<8>	J5	PE0_RX8_P	PE0_TX8_P	G3	=PEG_R2D_C_P<8>	OUT 9
9 IN	=PEG_D2R_N<8>	J4	PE0_RX8_N	PE0_TX8_N	H4	=PEG_R2D_C_N<8>	OUT 9
9 IN	=PEG_D2R_P<9>	L11	PE0_RX9_P	PE0_TX9_P	H3	=PEG_R2D_C_P<9>	OUT 9
9 IN	=PEG_D2R_N<9>	L10	PE0_RX9_N	PE0_TX9_N	H2	=PEG_R2D_C_N<9>	OUT 9
9 IN	=PEG_D2R_P<10>	L9	PE0_RX10_P	PE0_TX10_P	H1	=PEG_R2D_C_P<10>	OUT 9
9 IN	=PEG_D2R_N<10>	L8	PE0_RX10_N	PE0_TX10_N	J1	=PEG_R2D_C_N<10>	OUT 9
9 IN	=PEG_D2R_P<11>	L7	PE0_RX11_P	PE0_TX11_P	J2	=PEG_R2D_C_P<11>	OUT 9
9 IN	=PEG_D2R_N<11>	L6	PE0_RX11_N	PE0_TX11_N	J3	=PEG_R2D_C_N<11>	OUT 9
9 IN	=PEG_D2R_P<12>	N11	PE0_RX12_P	PE0_TX12_P	K2	=PEG_R2D_C_P<12>	OUT 9
9 IN	=PEG_D2R_N<12>	N10	PE0_RX12_N	PE0_TX12_N	K3	=PEG_R2D_C_N<12>	OUT 9
9 IN	=PEG_D2R_P<13>	N9	PE0_RX13_P	PE0_TX13_P	L4	=PEG_R2D_C_P<13>	OUT 9
9 IN	=PEG_D2R_N<13>	P9	PE0_RX13_N	PE0_TX13_N	L3	=PEG_R2D_C_N<13>	OUT 9
9 IN	=PEG_D2R_P<14>	N7	PE0_RX14_P	PE0_TX14_P	M4	=PEG_R2D_C_P<14>	OUT 9
9 IN	=PEG_D2R_N<14>	N6	PE0_RX14_N	PE0_TX14_N	M3	=PEG_R2D_C_N<14>	OUT 9
9 IN	=PEG_D2R_P<15>	N5	PE0_RX15_P	PE0_TX15_P	M2	=PEG_R2D_C_P<15>	OUT 9
9 IN	=PEG_D2R_N<15>	N4	PE0_RX15_N	PE0_TX15_N	M1	=PEG_R2D_C_N<15>	OUT 9

				PE0_REFCLK_P	E11	PEG_CLK100M_P	OUT 70 89
				PE0_REFCLK_N	D11	PEG_CLK100M_N	OUT 70 89
9 IN	PEG_PRSNT_L	C9	PE0_PRSNT_16# Int PU				
31 IN	MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU	PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P	OUT 31 89
31 IN	PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N	OUT 31 89
36 IN	FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU	PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P	OUT 36 89
9 IN	PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N	OUT 36 89
32 IN	EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU	PE3_REFCLK_P	G13	PCIE_CLK100M_EXCARD_P	OUT 32 89
32 IN	PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	PE3_REFCLK_N	F13	PCIE_CLK100M_EXCARD_N	OUT 32 89
9	TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU	PE4_REFCLK_P	J13	TP_PCIE_CLK100M_PE4P	9
9	TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	PE4_REFCLK_N	H13	TP_PCIE_CLK100M_PE4N	9
9 IN	AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17 Int PU	PE5_REFCLK_P	L14	TP_PCIE_CLK100M_PE5P	
83 OUT	GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	PE5_REFCLK_N	K14	TP_PCIE_CLK100M_PE5N	
	TP_MCP_GPIO_18	M17	PEG_CLKREQ#/GPIO_18 Int PU	PE6_REFCLK_P	N14	TP_PCIE_CLK100M_PE6P	
9 IN	GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N	
32 31 23 IN	PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	PEX_RST0#	K11	PCIE_RESET_L	OUT 9 26
89 31 IN	PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8	PCIE_MINI_R2D_C_P	OUT 31 89
89 31 IN	PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8	PCIE_MINI_R2D_C_N	OUT 31 89
89 36 IN	PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8	PCIE_FW_R2D_C_P	OUT 36 89
89 36 IN	PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8	PCIE_FW_R2D_C_N	OUT 36 89
89 32 7 IN	PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	PE1_TX2_P	A7	PCIE_EXCARD_R2D_C_P	OUT 32 89
89 32 7 IN	PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	PE1_TX2_N	B7	PCIE_EXCARD_R2D_C_N	OUT 32 89
9	TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP	9
9	TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6	TP_PCIE_PE4_R2D_CN	9

8 =PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

T17	+DVDD0_PEX1	
W19	+DVDD0_PEX2	
U17	+DVDD0_PEX3	
V19	+DVDD0_PEX4	
W16	+DVDD0_PEX5	
W17	+DVDD0_PEX6	
W18	+DVDD0_PEX7	
U16	+DVDD0_PEX8	

8 =PP1V05_S0_MCP_PEX_DVDD1

T19	+DVDD1_PEX1	
U19	+DVDD1_PEX2	

24 PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

T16	+V_PLL_PEX	

89 MCP_PEX_CLK_COMP

A11	PEX_CLK_COMP	

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

+AVDD0_PEX1	Y12	
+AVDD0_PEX2	AA12	
+AVDD0_PEX3	AB12	
+AVDD0_PEX4	M12	
+AVDD0_PEX5	P12	
+AVDD0_PEX6	R12	
+AVDD0_PEX7	N12	
+AVDD0_PEX8	T12	
+AVDD0_PEX9	U12	
+AVDD0_PEX10	AC12	
+AVDD0_PEX11	AD12	
+AVDD0_PEX12	V12	
+AVDD0_PEX13	W12	

8 =PP1V05_S0_MCP_PEX_AVDD0
206 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

8 =PP1V05_S0_MCP_PEX_AVDD1

+AVDD1_PEX1	M13	
+AVDD1_PEX2	N13	
+AVDD1_PEX3	P13	

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

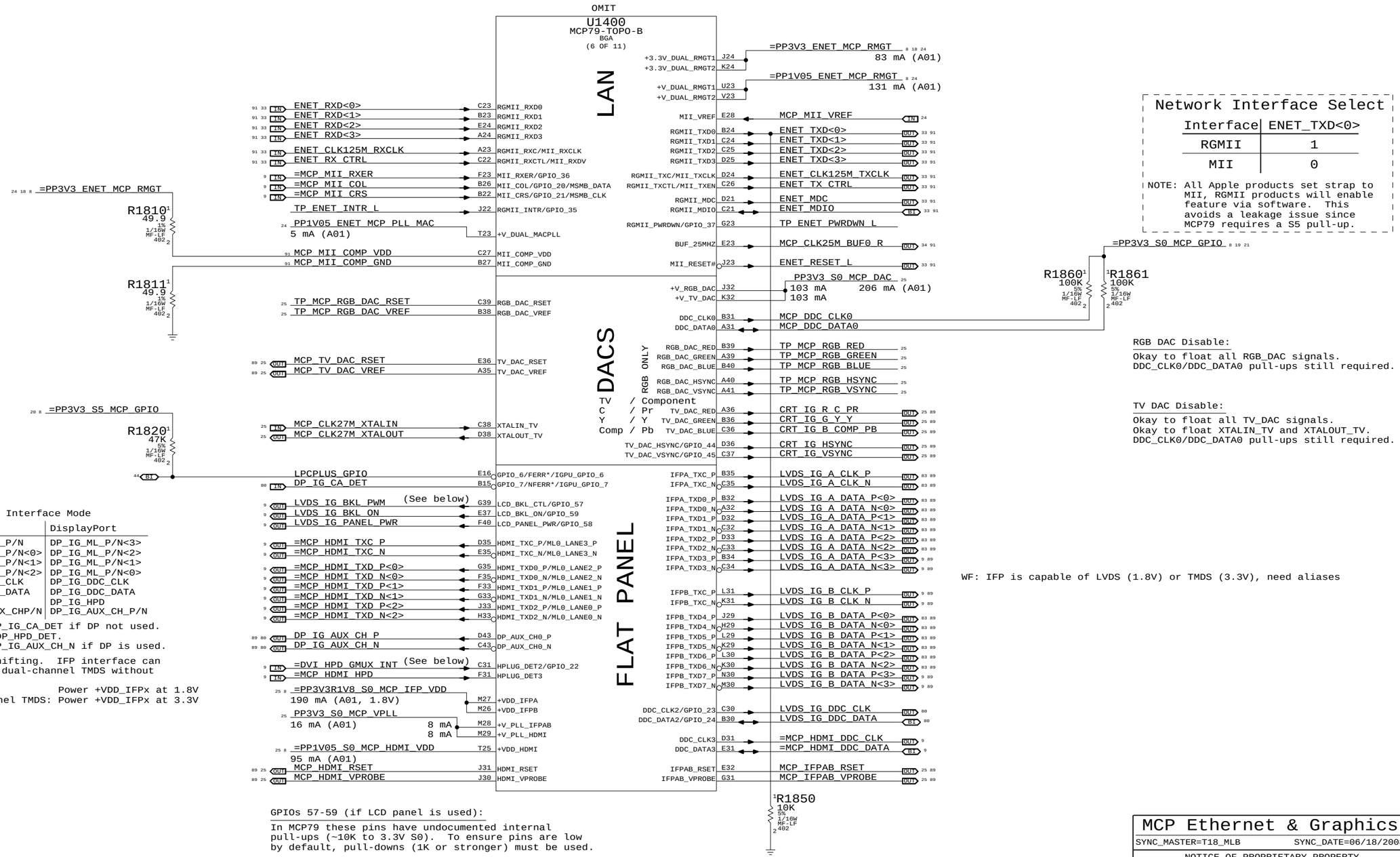
SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE: NONE SHT 17 OF 96

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 18 OF 96	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

90 19	PCI_REQ0_L	T2	PCI_REQ0#		
90 19	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2		
19 OUT	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT2#/GPIO_41/RS232_DTR#	R4 GMUX_JTAG_TMS OUT 9
59 9 OUT	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT3#/GPIO_39/RS232_RTS#	U11 GMUX_JTAG_TDI OUT 9
19 IN	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT4#/GPIO_53/RS232_SOUT#	P3 MCP_RS232_SOUT_L OUT 19
90 13 BI	MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0#	AA3 TP_PCI_C_BE_L<0>
90 13 BI	MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1#	AA6 TP_PCI_C_BE_L<1>
90 13 BI	MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2#	AA11 TP_PCI_C_BE_L<2>
90 13 BI	MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3#	W10 TP_PCI_C_BE_L<3>
90 13 BI	MCP_DEBUG<4>	AB3	PCI_AD4		
90 13 BI	MCP_DEBUG<5>	AC6	PCI_AD5	PCI_DEVSEL#	AA9 TP_PCI_DEVSEL_L
90 13 BI	MCP_DEBUG<6>	AB2	PCI_AD6	PCI_FRAME#	Y4 TP_PCI_FRAME_L
90 13 BI	MCP_DEBUG<7>	AC7	PCI_AD7	PCI_IRDY#	AA10 TP_PCI_IRDY_L
	TP_PCI_AD<8>	AC8	PCI_AD8	PCI_PAR	Y1 TP_PCI_PAR
	TP_PCI_AD<9>	AA2	PCI_AD9	PCI_PERR#/GPIO_43/RS232_DCD#	AB9 TP_PCI_PERR_L
	TP_PCI_AD<10>	AC9	PCI_AD10	PCI_SERR#	AA7 TP_PCI_SERR_L
	TP_PCI_AD<11>	AC10	PCI_AD11	PCI_STOP#	Y2 TP_PCI_STOP_L
	TP_PCI_AD<12>	AC11	PCI_AD12	PCI_PME#/GPIO_30 Int PU (S5)	T1 PM_LATRIGGER_L OUT 13 23
	TP_PCI_AD<13>	AA1	PCI_AD13		
	TP_PCI_AD<14>	AA5	PCI_AD14	PCI_RESET0#	R10 MEM_VTT_EN_R OUT 26
	TP_PCI_AD<15>	Y5	PCI_AD15	PCI_RESET1#	R11 TP_PCI_RESET1_L
	TP_PCI_AD<16>	W3	PCI_AD16		
	TP_PCI_AD<17>	W6	PCI_AD17	PCI_CLK0	R6 TP_PCI_CLK0
	TP_PCI_AD<18>	W4	PCI_AD18	PCI_CLK1	R7 TP_PCI_CLK1
	TP_PCI_AD<19>	W7	PCI_AD19	PCI_CLK2	R8 90 PCI_CLK33M_MCP_R
	TP_PCI_AD<20>	V3	PCI_AD20		
	TP_PCI_AD<21>	W8	PCI_AD21		
	TP_PCI_AD<22>	V2	PCI_AD22		
	TP_PCI_AD<23>	W9	PCI_AD23		
	TP_PCI_AD<24>	U3	PCI_AD24		
	TP_PCI_AD<25>	W11	PCI_AD25		
	TP_PCI_AD<26>	U2	PCI_AD26		
	TP_PCI_AD<27>	U5	PCI_AD27		
	TP_PCI_AD<28>	U1	PCI_AD28		
	TP_PCI_AD<29>	U6	PCI_AD29		
	TP_PCI_AD<30>	T5	PCI_AD30		
	TP_PCI_AD<31>	U7	PCI_AD31		
	TP_PCI_INTW_L	P2	PCI_INTW#		
	TP_PCI_INTX_L	N3	PCI_INTX#		
	TP_PCI_INTY_L	N2	PCI_INTY#		
	TP_PCI_INTZ_L	N1	PCI_INTZ#		
	TP_PCI_TRDY_L	Y3	PCI_TRDY#		
44 42 IN	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42		
36 IN	FW_PME_L	AE2	PCI_DRQ1#/GPIO_19 Int PU		
	TP_LPC_DRQ0_L	AE1	PCI_DRQ0# Int PU		
44 42 BI	LPC_SERIRQ	AE6	PCI_SERIRQ Int PU		

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

PCI_CLKIN R9 90 PCI_CLK33M_MCP

LPC

LPC_FRAME#	AD4	4	LPC_FRAME_R_L	R1960 22	LPC_FRAME_L OUT 42 44 83 90
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12		LPC_PWRDWN_L		OUT 42 44
LPC_RESET0#	AE5		LPC_RESET_L		OUT 26 83 90
LPC_AD0	AD3		LPC_AD_R<0>	R1950 22	LPC_AD<0> BI 42 44 83 90
LPC_AD1	AD2		LPC_AD_R<1>	R1951 22	LPC_AD<1> BI 42 44 83 90
LPC_AD2	AD1		LPC_AD_R<2>	R1952 22	LPC_AD<2> BI 42 44 83 90
LPC_AD3	AD5		LPC_AD_R<3>	R1953 22	LPC_AD<3> BI 42 44 83 90
LPC_CLK0	AE9		LPC_CLK33M_SMC_R		OUT 26 90

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

	U24 GND65	GND98	Y26
	U26 GND66	GND99	Y27
	U39 GND67	GND100	AB18
	U4 GND68	GND101	H34
	U8 GND69	GND102	AB20
	V16 GND70	GND103	AB21
	V17 GND71	GND104	AB23
	V18 GND72	GND105	AB24
	V20 GND73	GND106	AB25
	V22 GND74	GND107	AB26
	V24 GND75	GND108	AB27
	V26 GND76	GND109	AB28
	V27 GND77	GND110	AB34
	V28 GND78	GND111	AB37
	V33 GND79	GND112	AB4
	V37 GND80	GND113	AB40
	V4 GND81	GND114	AC22
	V40 GND82	GND115	AC36
	V7 GND83	GND116	AC40
	W20 GND84	GND117	AB33
	W22 GND85	GND118	AC5
	W24 GND86	GND119	AD16
	W36 GND87	GND120	AD17
	W40 GND88	GND121	AD18
	W43 GND89	GND122	AD19
	Y16 GND90	GND123	AD20
	Y17 GND91	GND124	AD24
	Y18 GND92	GND125	AD25
	Y19 GND93	GND126	AD26
	Y20 GND94	GND127	AD27
	Y22 GND95	GND128	AD28
	Y24 GND96	GND129	AD33
	Y25 GND97	GND130	AD34

21 18 8 =PP3V3_S0_MCP_GPIO

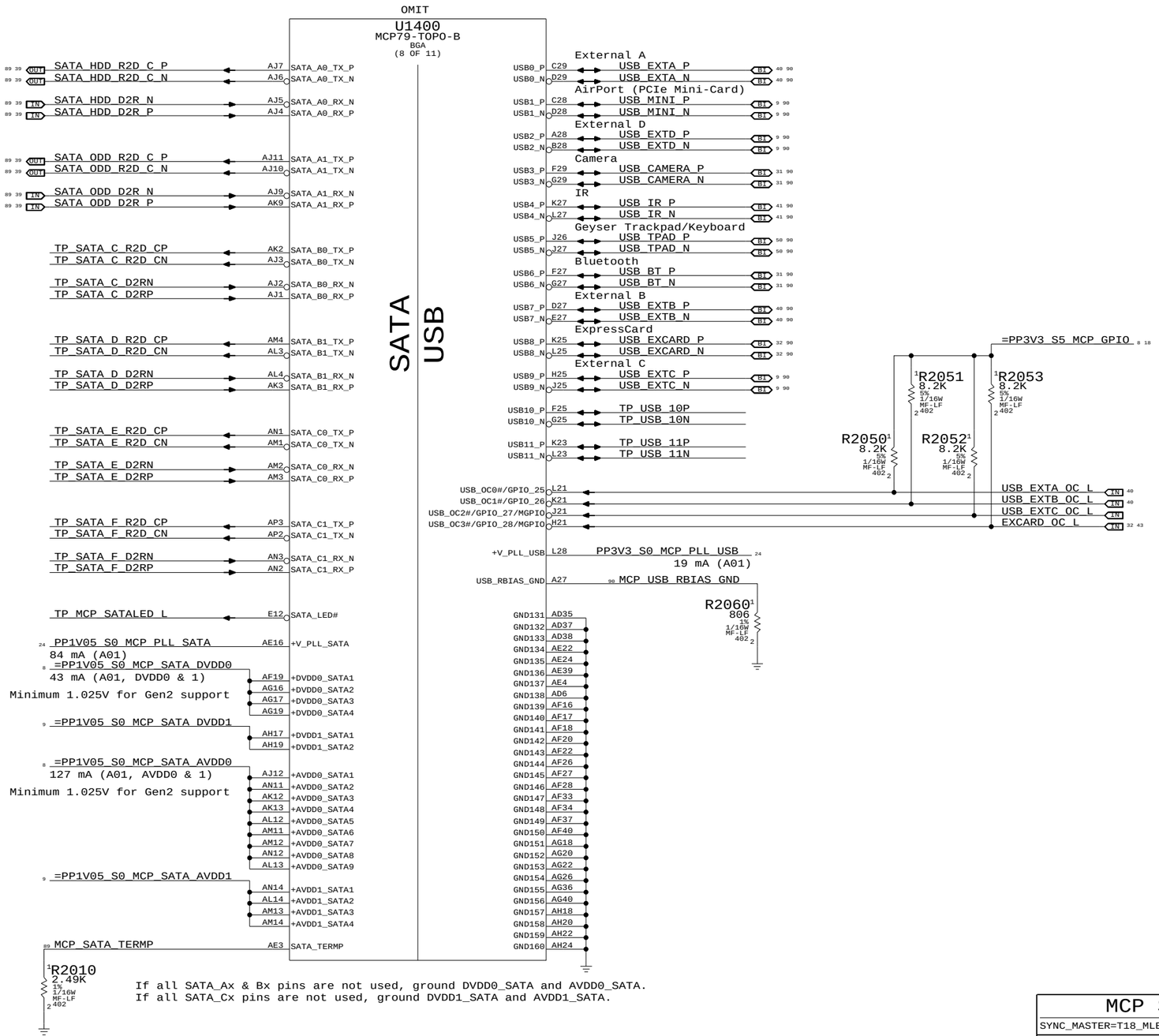
19	MCP_RS232_SOUT_L	R1989 8.2K	5% 1/16W MF-LF 402
90 19	PCI_REQ0_L	R1990 8.2K	5% 1/16W MF-LF 402
90 19	PCI_REQ1_L	R1991 8.2K	5% 1/16W MF-LF 402
19	CRTMUX_SEL_TV_L	R1992 8.2K	5% 1/16W MF-LF 402
19	MCP_RS232_SIN_L	R1994 8.2K	5% 1/16W MF-LF 402

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE NONE	SHT 19 OF 96	



MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 20 OF 96	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

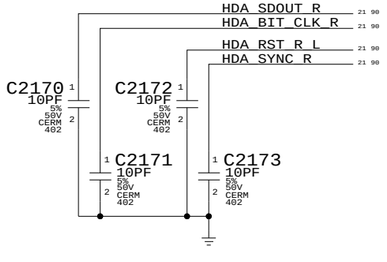
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE: NONE SHT 21 OF 96

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

=PPVCORE_S0_MCP
46 24 8
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32	=PP1V05_S0_MCP_FSB	
AC23	+VDD_CORE2	+VTT_CPU2	AC32	1139 mA	1182 mA (A01)
U25	+VDD_CORE3	+VTT_CPU3	E40	8 9 14 24	
AH12	+VDD_CORE4	+VTT_CPU4	J36		
AG10	+VDD_CORE5	+VTT_CPU5	N32		
AG5	+VDD_CORE6	+VTT_CPU6	T32		
Y21	+VDD_CORE7	+VTT_CPU7	U32		
Y23	+VDD_CORE8	+VTT_CPU8	V32		
AA16	+VDD_CORE9	+VTT_CPU9	W32		
AA26	+VDD_CORE10	+VTT_CPU10	P31		
AA27	+VDD_CORE11	+VTT_CPU11	AF32		
AA28	+VDD_CORE12	+VTT_CPU12	AE32		
AC16	+VDD_CORE13	+VTT_CPU13	AH32		
AC17	+VDD_CORE14	+VTT_CPU14	AJ32		
AC18	+VDD_CORE15	+VTT_CPU15	AK31		
AC19	+VDD_CORE16	+VTT_CPU16	AK32		
AC20	+VDD_CORE17	+VTT_CPU17	AD32		
AC21	+VDD_CORE18	+VTT_CPU18	AL31		
AA17	+VDD_CORE19	+VTT_CPU19	AB32		
AC24	+VDD_CORE20	+VTT_CPU20	B41		
AC25	+VDD_CORE21	+VTT_CPU21	B42		
AC26	+VDD_CORE22	+VTT_CPU22	C40		
AC27	+VDD_CORE23	+VTT_CPU23	C41		
AC28	+VDD_CORE24	+VTT_CPU24	C42		
AD21	+VDD_CORE25	+VTT_CPU25	D39		
AD23	+VDD_CORE26	+VTT_CPU26	D40		
W27	+VDD_CORE27	+VTT_CPU27	D41		
V25	+VDD_CORE28	+VTT_CPU28	E38		
AA18	+VDD_CORE29	+VTT_CPU29	E39		
AE19	+VDD_CORE30	+VTT_CPU30	F37		
AE21	+VDD_CORE31	+VTT_CPU31	F38		
AE23	+VDD_CORE32	+VTT_CPU32	F39		
AE25	+VDD_CORE33	+VTT_CPU33	G36		
AE26	+VDD_CORE34	+VTT_CPU34	G37		
AE27	+VDD_CORE35	+VTT_CPU35	G38		
AE28	+VDD_CORE36	+VTT_CPU36	H35		
AF10	+VDD_CORE37	+VTT_CPU37	H37		
AF11	+VDD_CORE38	+VTT_CPU38	J34		
AA19	+VDD_CORE39	+VTT_CPU39	J35		
AF2	+VDD_CORE40	+VTT_CPU40	K33		
AF21	+VDD_CORE41	+VTT_CPU41	K34		
AF23	+VDD_CORE42	+VTT_CPU42	K35		
AF25	+VDD_CORE43	+VTT_CPU43	L32		
AF3	+VDD_CORE44	+VTT_CPU44	L33		
AF4	+VDD_CORE45	+VTT_CPU45	L34		
AF7	+VDD_CORE46	+VTT_CPU46	M31		
AH23	+VDD_CORE47	+VTT_CPU47	M32		
AF9	+VDD_CORE48	+VTT_CPU48	M33		
AA20	+VDD_CORE49	+VTT_CPU49	N31		
AG11	+VDD_CORE50	+VTT_CPU50	P32		
AG12	+VDD_CORE51	+VTT_CPU51	Y32		
AG21	+VDD_CORE52	+VTT_CPU52	AA32		
AG23	+VDD_CORE53				
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA	
AG3	+VDD_CORE55				
AG4	+VDD_CORE56				
AA21	+VDD_CORE57				
AG6	+VDD_CORE58				
AG7	+VDD_CORE59	+3.3V_1	AD10	=PP3V3_S0_MCP	
AG8	+VDD_CORE60	+3.3V_2	AE8	8 21 24	
AG9	+VDD_CORE61	+3.3V_3	AB10	450 mA (A01)	
AH1	+VDD_CORE62	+3.3V_4	AD9		
AH10	+VDD_CORE63	+3.3V_5	Y10		
AH11	+VDD_CORE64	+3.3V_6	AB11		
W26	+VDD_CORE65	+3.3V_7	AA8		
AH2	+VDD_CORE66	+3.3V_8	Y9		
AA23	+VDD_CORE67				
W28	+VDD_CORE68				
AH25	+VDD_CORE69				
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	=PP3V3_S5_MCP	
AH3	+VDD_CORE71	+3.3V_DUAL2	H19	8 24	
AH4	+VDD_CORE72	+3.3V_DUAL3	J20	16 mA	266 mA (A01)
AH5	+VDD_CORE73	+3.3V_DUAL4	K20		
AH6	+VDD_CORE74				
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA	
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27		
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28		
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28		
W23	+VDD_CORE79				
W25	+VDD_CORE80				
AF12	+VDD_CORE81				
		+VDD_AUXC1	T21	=PP1V05_S5_MCP_VDD_AUXC	
		+VDD_AUXC2	U21	8 24	
A20	+VBAT	+VDD_AUXC3	V21	105 mA (A01)	

26 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

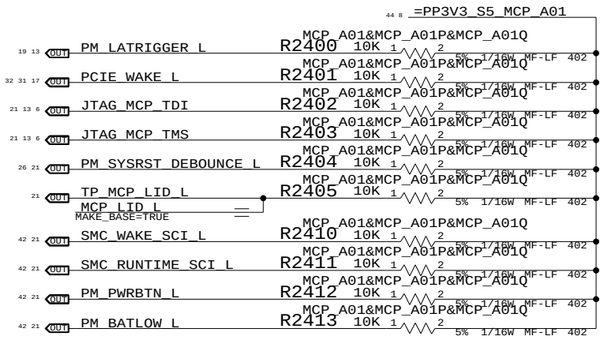
SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 22 OF 96	

3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 23 OF 96	

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

=PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

=PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_ENET_MCP_PLL_MAC

5 mA (A01)

L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/10W MF-LF 402
R2590 1.47K 1% 1/10W MF-LF 402
MCP_MII_VREF (OUT)
C2591 0.1UF 20% 10V CERM 402

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

=PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF

19 mA (A01)

L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_AVDD_UF

333 mA (A01)

L2570 30-OHM-5A 0603
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_UF

562 mA (A01)

R2580 0.2 1% 1/6W MF 402-HF
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 20% 6.3V CERM 402-LF

L2582 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

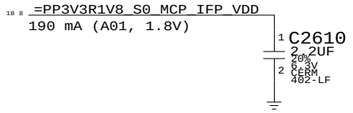
APPLE INC.

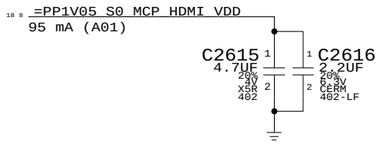
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

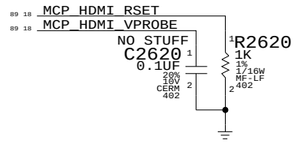
SCALE: NONE SHT 24 OF 96

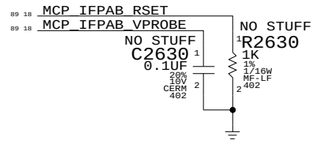
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



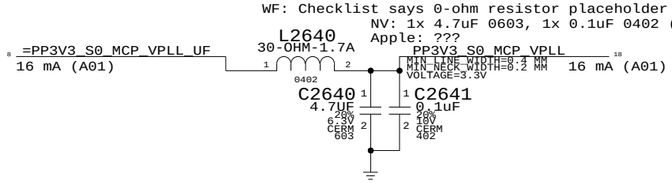


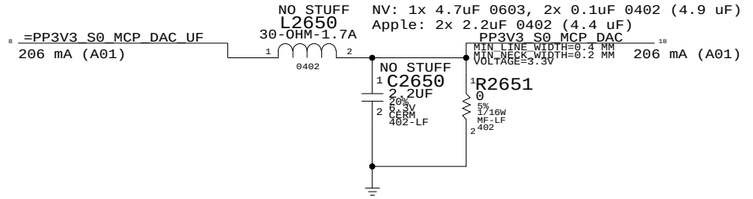




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

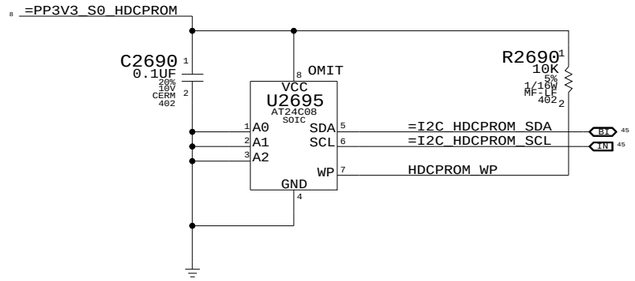




18	TP_MCP_RGB_RED		NC_MCP_RGB_RED (MAKE_BASE=TRUE)
18	TP_MCP_RGB_GREEN		NC_MCP_RGB_GREEN (MAKE_BASE=TRUE)
18	TP_MCP_RGB_BLUE		NC_MCP_RGB_BLUE (MAKE_BASE=TRUE)
18	TP_MCP_RGB_HSYNC		NC_MCP_RGB_HSYNC (MAKE_BASE=TRUE)
18	TP_MCP_RGB_VSYNC		NC_MCP_RGB_VSYNC (MAKE_BASE=TRUE)
89 18	CRT_IG_R_C_PR		NC_CRT_IG_R_C_PR (MAKE_BASE=TRUE)
89 18	CRT_IG_G_Y_Y		NC_CRT_IG_G_Y_Y (MAKE_BASE=TRUE)
89 18	CRT_IG_B_COMP_PB		NC_CRT_IG_B_COMP_PB (MAKE_BASE=TRUE)
89 18	CRT_IG_HSYNC		NC_CRT_IG_HSYNC (MAKE_BASE=TRUE)
89 18	CRT_IG_VSYNC		NC_CRT_IG_VSYNC (MAKE_BASE=TRUE)
18	TP_MCP_RGB_DAC_RSET		NC_MCP_RGB_DAC_RSET (MAKE_BASE=TRUE)
18	TP_MCP_RGB_DAC_VREF		NC_MCP_RGB_DAC_VREF (MAKE_BASE=TRUE)
89 18	MCP_TV_DAC_RSET		NC_MCP_TV_DAC_RSET (MAKE_BASE=TRUE)
89 18	MCP_TV_DAC_VREF		NC_MCP_TV_DAC_VREF (MAKE_BASE=TRUE)
18	MCP_CLK27M_XTALIN		NC_MCP_CLK27M_XTALIN (MAKE_BASE=TRUE)
18	MCP_CLK27M_XTALOUT		NC_MCP_CLK27M_XTALOUT (MAKE_BASE=TRUE)

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.



Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

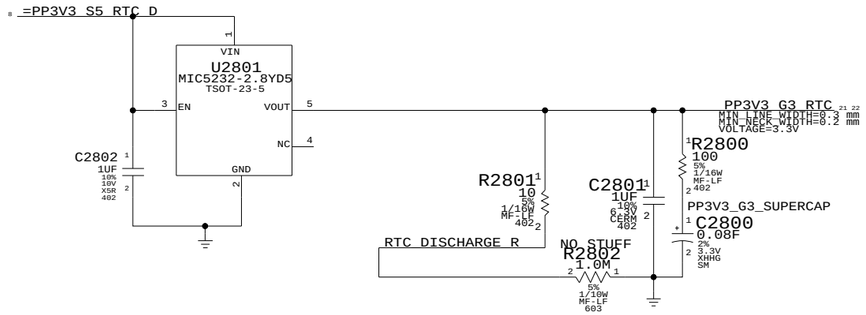
MCP Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

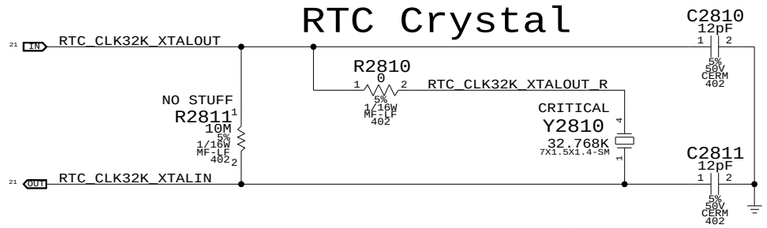
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 25 OF 96	

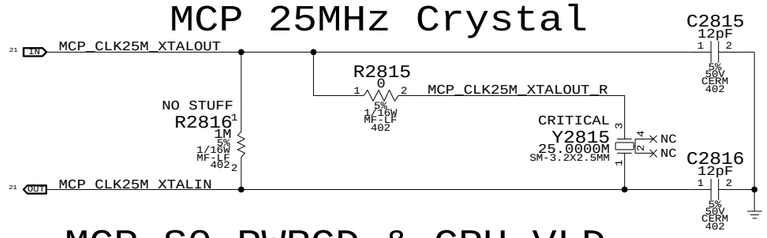
RTC Power Sources



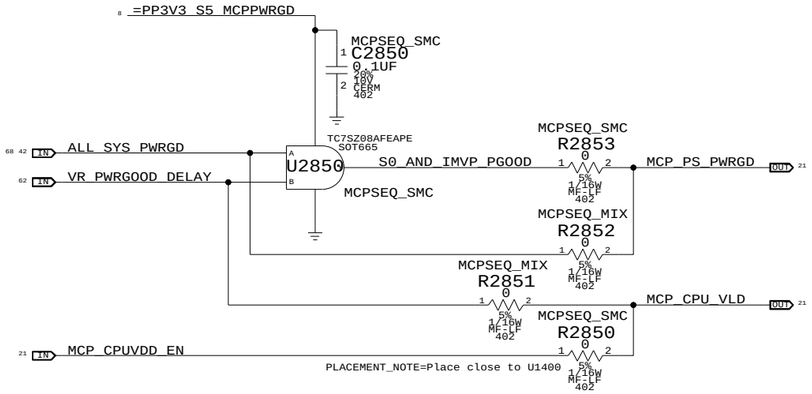
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 ‘MLB’ power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

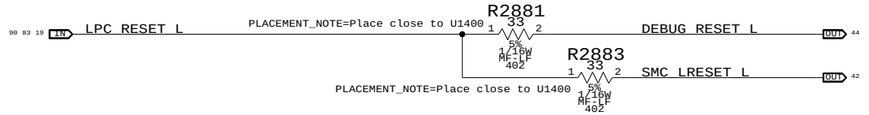
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

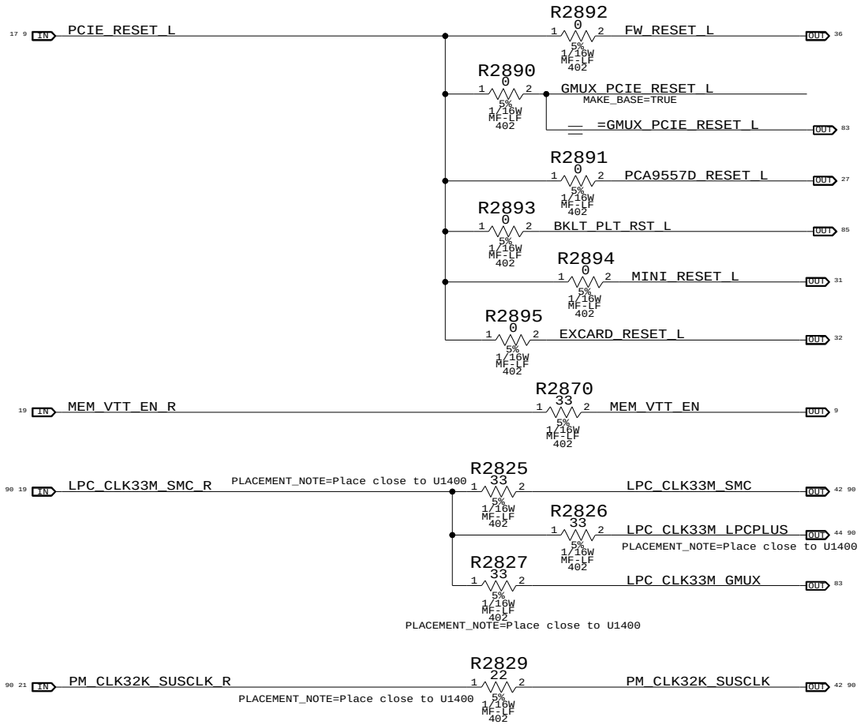
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

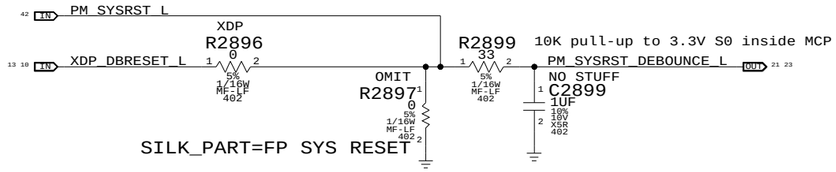
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc

SYNC_MASTER=T18_MLB SYNC_DATE=12/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 26 OF 96	

Page Notes

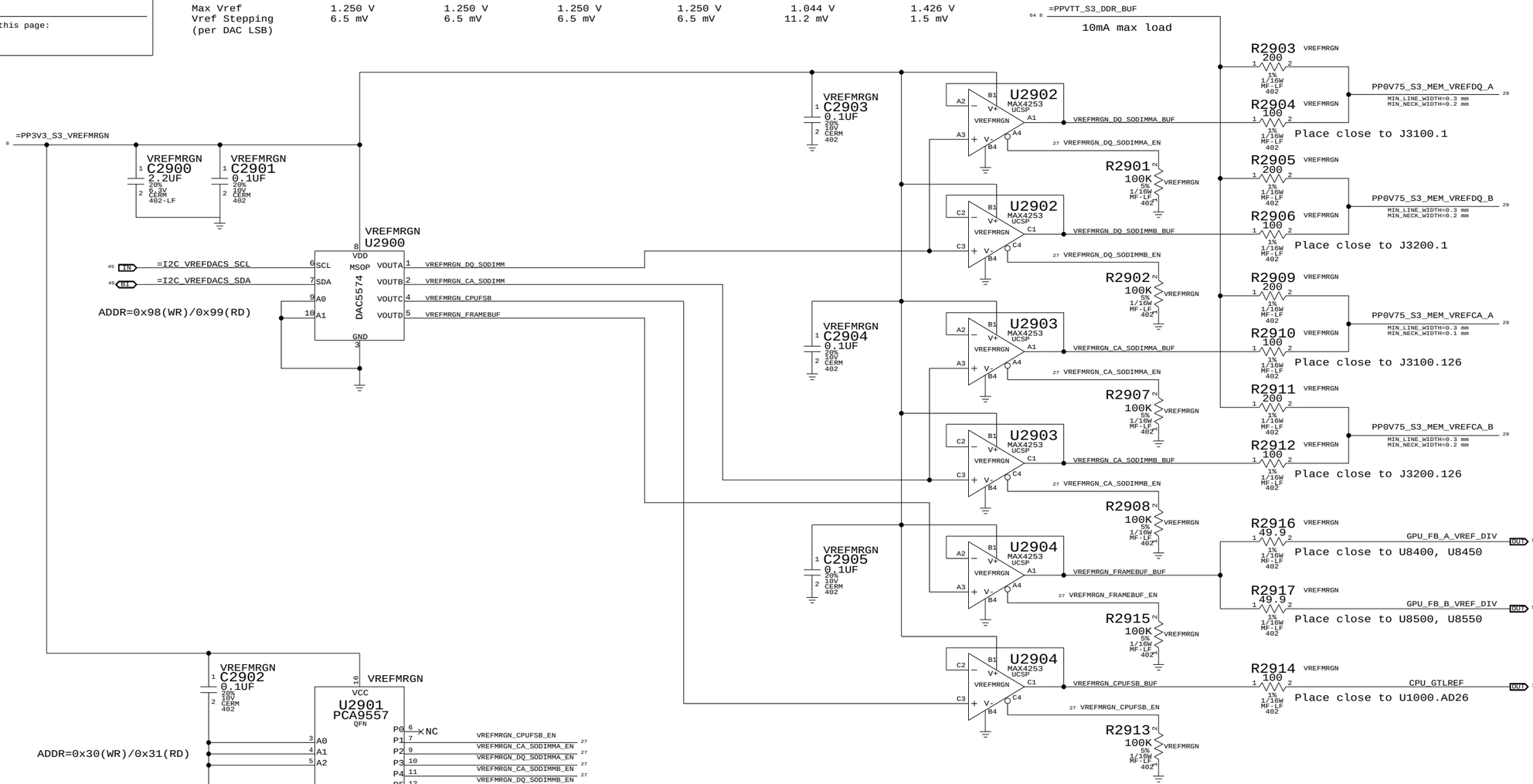
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	27	96

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

8 =PP1V5_S0_MEM_A

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X6S CERM 603
C3101 10UF 20% 6.3V X6S CERM 603

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

27 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 — DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2) F-RT-THB

KEY

73	CKE0		CKE1	74	MEM_A_CKE<1> IN 15 88
75	VDD		VDD	76	
77	NC		A15	78	MEM_A_A<15> IN 9
79	BA2		A14	80	MEM_A_A<14> IN 15 88
81	VDD		VDD	82	
83	A12/BC*		A11	84	MEM_A_A<11> IN 15 88
85	A9		A7	86	MEM_A_A<7> IN 15 88
87	VDD		VDD	88	
89	A8		A6	90	MEM_A_A<6> IN 15 88
91	A5		A4	92	MEM_A_A<4> IN 15 88
93	VDD		VDD	94	
95	A3		A2	96	MEM_A_A<2> IN 15 88
97	A1		A0	98	MEM_A_A<0> IN 15 88
99	VDD		VDD	100	
101	CK0		CK1	102	MEM_A_CLK_P<1> IN 15 88
103	CK0*		CK1*	104	MEM_A_CLK_N<1> IN 15 88
105	VDD		VDD	106	
107	A10/AP		BA1	108	MEM_A_BA<1> IN 15 88
109	BA0		RAS*	110	MEM_A_RAS_L IN 15 88
111	VDD		VDD	112	
113	WE*		S0*	114	MEM_A_CS_L<0> IN 15 88
115	CAS*		ODT0	116	MEM_A_ODT<0> IN 15 88
117	VDD		VDD	118	
119	A13		ODT1	120	MEM_A_ODT<1> IN 15 88
121	S1*		NC	122	
123	VDD		VDD	124	
125	TEST		VREFCA	126	
127	VSS		VSS	128	
129	DQ32		DQ36	130	MEM_A_DQ<36> BI 15 88
131	DQ33		DQ37	132	MEM_A_DQ<37> BI 15 88
133	VSS		VSS	134	
135	DQS4*		DM4	136	MEM_A_DM<4> IN 15 88
137	DQS4		VSS	138	
139	VSS		DQ38	140	MEM_A_DQ<38> BI 15 88
141	DQ34		DQ39	142	MEM_A_DQ<39> BI 15 88
143	DQ35		VSS	144	
145	VSS		DQ44	146	MEM_A_DQ<47> BI 15 88
147	DQ40		DQ45	148	MEM_A_DQ<40> BI 15 88
149	DQ41		VSS	150	
151	VSS		DQS5*	152	MEM_A_DQS_N<5> BI 15 88
153	DM5		DQS5	154	MEM_A_DQS_P<5> BI 15 88
155	VSS		VSS	156	
157	DQ42		DQ46	158	MEM_A_DQ<46> BI 15 88
159	DQ43		DQ47	160	MEM_A_DQ<43> BI 15 88
161	VSS		VSS	162	
163	DQ48		DQ52	164	MEM_A_DQ<48> BI 15 88
165	DQ49		DQ53	166	MEM_A_DQ<53> BI 15 88
167	VSS		VSS	168	
169	DQS6*		DM6	170	MEM_A_DM<6> IN 15 88
171	DQS6		VSS	172	
173	VSS		DQ54	174	MEM_A_DQ<50> BI 15 88
175	DQ50		DQ55	176	MEM_A_DQ<49> BI 15 88
177	DQ51		VSS	178	
179	VSS		DQ60	180	MEM_A_DQ<57> BI 15 88
181	DQ56		DQ61	182	MEM_A_DQ<56> BI 15 88
183	DQ57		VSS	184	
185	VSS		DQS7*	186	MEM_A_DQS_N<7> BI 15 88
187	DM7		DQS7	188	MEM_A_DQS_P<7> BI 15 88
189	VSS		VSS	190	
191	DQ58		DQ62	192	MEM_A_DQ<62> BI 15 88
193	DQ59		DQ63	194	MEM_A_DQ<63> BI 15 88
195	VSS		VSS	196	
197	SA0		EVENT*	198	MEM_EVENT_L OUT 21 29 42
199	VDDSPD		SDA	200	=I2C_SODIMMA_SDA BI 45
201	SA1		SCL	202	=I2C_SODIMMA_SCL IN 45
203	VTT		VTT	204	=PP0V75_S0_MEM_VTT_A 8

MEM_A_CKE<0> IN 15 88
MEM_A_BA<2> IN 15 88
MEM_A_A<12> IN 15 88
MEM_A_A<9> IN 15 88
MEM_A_A<8> IN 15 88
MEM_A_A<5> IN 15 88
MEM_A_A<3> IN 15 88
MEM_A_A<1> IN 15 88
MEM_A_CLK_P<0> IN 15 88
MEM_A_CLK_N<0> IN 15 88
MEM_A_A<10> IN 15 88
MEM_A_BA<0> IN 15 88
MEM_A_WE_L IN 15 88
MEM_A_CAS_L IN 15 88
MEM_A_A<13> IN 15 88
MEM_A_CS_L<1> IN 15 88
MEM_A_DQ<33> BI 15 88
MEM_A_DQ<32> BI 15 88
MEM_A_DQS_N<4> BI 15 88
MEM_A_DQS_P<4> BI 15 88
MEM_A_DQ<34> BI 15 88
MEM_A_DQ<35> BI 15 88
MEM_A_DQ<44> BI 15 88
MEM_A_DQ<41> BI 15 88
MEM_A_DM<5> IN 15 88
MEM_A_DQ<45> BI 15 88
MEM_A_DQ<42> BI 15 88
MEM_A_DQ<52> BI 15 88
MEM_A_DQ<51> BI 15 88
MEM_A_DQS_N<6> BI 15 88
MEM_A_DQS_P<6> BI 15 88
MEM_A_DQ<55> BI 15 88
MEM_A_DQ<54> BI 15 88
MEM_A_DQ<61> BI 15 88
MEM_A_DQ<60> BI 15 88
MEM_A_DM<7> IN 15 88
MEM_A_DQ<58> BI 15 88
MEM_A_DQ<59> BI 15 88

J3100 — DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2) CRITICAL F-RT-THB

KEY

1	VREFDQ		VSS	2	
3	VSS		DQ4	4	MEM_A_DQ<4> BI 15 88
5	DQ0		DQ5	6	MEM_A_DQ<5> BI 15 88
7	DQ1		VSS	8	
9	VSS		DQS0*	10	MEM_A_DQS_N<0> BI 15 88
11	DM0		DQS0	12	MEM_A_DQS_P<0> BI 15 88
13	VSS		VSS	14	
15	DQ2		DQ6	16	MEM_A_DQ<6> BI 15 88
17	DQ3		DQ7	18	MEM_A_DQ<7> BI 15 88
19	VSS		VSS	20	
21	DQ8		DQ12	22	MEM_A_DQ<8> BI 15 88
23	DQ9		DQ13	24	MEM_A_DQ<12> BI 15 88
25	VSS		VSS	26	
27	DQS1*		DM1	28	MEM_A_DM<1> IN 15 88
29	DQS1		RESET*	30	MEM_RESET_L IN 29 30
31	VSS		VSS	32	
33	DQ10		DQ14	34	MEM_A_DQ<15> BI 15 88
35	DQ11		DQ15	36	MEM_A_DQ<10> BI 15 88
37	VSS		VSS	38	
39	DQ16		DQ20	40	MEM_A_DQ<21> BI 15 88
41	DQ17		DQ21	42	MEM_A_DQ<20> BI 15 88
43	VSS		VSS	44	
45	DQS2*		DM2	46	MEM_A_DM<2> IN 15 88
47	DQS2		VSS	48	
49	VSS		DQ22	50	MEM_A_DQ<17> BI 15 88
51	DQ18		DQ23	52	MEM_A_DQ<22> BI 15 88
53	DQ19		VSS	54	
55	VSS		DQ28	56	MEM_A_DQ<29> BI 15 88
57	DQ24		DQ29	58	MEM_A_DQ<28> BI 15 88
59	DQ25		VSS	60	
61	VSS		DQS3*	62	MEM_A_DQS_N<3> BI 15 88
63	DM3		DQS3	64	MEM_A_DQS_P<3> BI 15 88
65	VSS		VSS	66	
67	DQ26		DQ30	68	MEM_A_DQ<26> BI 15 88
69	DQ27		DQ31	70	MEM_A_DQ<31> BI 15 88
71	VSS		VSS	72	

MEM_A_DQ<0> BI 15 88
MEM_A_DQ<1> BI 15 88
MEM_A_DM<0> IN 15 88
MEM_A_DQ<3> BI 15 88
MEM_A_DQ<2> BI 15 88
MEM_A_DQ<9> BI 15 88
MEM_A_DQ<13> BI 15 88
MEM_A_DQS_N<1> BI 15 88
MEM_A_DQS_P<1> BI 15 88
MEM_A_DQ<11> BI 15 88
MEM_A_DQ<14> BI 15 88
MEM_A_DQ<16> BI 15 88
MEM_A_DQ<18> BI 15 88
MEM_A_DQS_N<2> BI 15 88
MEM_A_DQS_P<2> BI 15 88
MEM_A_DQ<23> BI 15 88
MEM_A_DQ<19> BI 15 88
MEM_A_DQ<24> BI 15 88
MEM_A_DQ<30> BI 15 88
MEM_A_DM<3> IN 15 88
MEM_A_DQ<27> BI 15 88
MEM_A_DQ<25> BI 15 88

516-0196

PP0V75_S3_MEM_VREFCA_A 27

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

8 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

MEM_A_SA<0>
MEM_A_SA<1>

516-0196
SPD ADDR=0xA0(WR)/0xA1(RD)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 28 OF 96	

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

8 =PP1V5_S0_MEM_B

8 =PP1V5_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603

27 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

88 15 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15 88
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 9
88 15 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15 88
		81	VDD	VDD	82		
88 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15 88
88 15 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15 88
		87	VDD	VDD	88		
88 15 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15 88
88 15 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15 88
		93	VDD	VDD	94		
88 15 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15 88
88 15 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15 88
		99	VDD	VDD	100		
88 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15 88
88 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15 88
		105	VDD	VDD	106		
88 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15 88
88 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15 88
		111	VDD	VDD	112		
88 15 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15 88
88 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15 88
		117	VDD	VDD	118		
88 15 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15 88
88 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
88 15 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33>	BI 15 88
88 15 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36>	BI 15 88
		133	VSS	VSS	134		
88 15 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15 88
88 15 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 15 88
88 15 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	BI 15 88
88 15 BI	MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<44>	BI 15 88
88 15 BI	MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45>	BI 15 88
88 15 BI	MEM_B_DQ<40>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 15 88
88 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 15 88
		155	VSS	VSS	156		
88 15 BI	MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47>	BI 15 88
88 15 BI	MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46>	BI 15 88
		161	VSS	VSS	162		
88 15 BI	MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48>	BI 15 88
88 15 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54>	BI 15 88
		167	VSS	VSS	168		
88 15 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15 88
88 15 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<53>	BI 15 88
88 15 BI	MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 15 88
88 15 BI	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<60>	BI 15 88
88 15 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>	BI 15 88
88 15 BI	MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 15 88
88 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15 88
		189	VSS	VSS	190		
88 15 BI	MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58>	BI 15 88
88 15 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62>	BI 15 88
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21 28 42
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 45
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 45
		203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B	8
		MTG PINS					
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

KEY

516s0704

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402

8 =PPSPD_S0_MEM_B

C3240 2.2UF 20% 6.3V CERM 402-LF

R3241 10K 5% 1/16W MF-LF 402

J3200 F-RT-BGA3 DDR3-SODIMM (1 OF 2) CRITICAL

		1	VREFDQ	VSS	2		
88 15 BI	MEM_B_DQ<0>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15 88
88 15 BI	MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15 88
		7	DQ1	VSS	8		
88 15 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15 88
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15 88
		13	VSS	VSS	14		
88 15 BI	MEM_B_DQ<2>	15	DQ2	DQ6	16	MEM_B_DQ<6>	BI 15 88
88 15 BI	MEM_B_DQ<3>	17	DQ3	DQ7	18	MEM_B_DQ<7>	BI 15 88
		19	VSS	VSS	20		
88 15 BI	MEM_B_DQ<28>	21	DQ8	DQ12	22	MEM_B_DQ<29>	BI 15 88
88 15 BI	MEM_B_DQ<24>	23	DQ9	DQ13	24	MEM_B_DQ<25>	BI 15 88
		25	VSS	VSS	26		
88 15 BI	MEM_B_DQS_N<3>	27	DQS1*	DM1	28	MEM_B_DM<3>	IN 15 88
88 15 BI	MEM_B_DQS_P<3>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28 30
		31	VSS	VSS	32		
88 15 BI	MEM_B_DQ<31>	33	DQ10	DQ14	34	MEM_B_DQ<26>	BI 15 88
88 15 BI	MEM_B_DQ<30>	35	DQ11	DQ15	36	MEM_B_DQ<27>	BI 15 88
		37	VSS	VSS	38		
88 15 BI	MEM_B_DQ<9>	39	DQ16	DQ20	40	MEM_B_DQ<13>	BI 15 88
88 15 BI	MEM_B_DQ<8>	41	DQ17	DQ21	42	MEM_B_DQ<12>	BI 15 88
		43	VSS	VSS	44		
88 15 BI	MEM_B_DQS_N<1>	45	DQS2*	DM2	46	MEM_B_DM<1>	IN 15 88
88 15 BI	MEM_B_DQS_P<1>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<14>	BI 15 88
88 15 BI	MEM_B_DQ<15>	51	DQ18	DQ23	52	MEM_B_DQ<11>	BI 15 88
88 15 BI	MEM_B_DQ<10>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<20>	BI 15 88
88 15 BI	MEM_B_DQ<21>	57	DQ24	DQ29	58	MEM_B_DQ<16>	BI 15 88
88 15 BI	MEM_B_DQ<17>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<2>	BI 15 88
88 15 IN	MEM_B_DM<2>	63	DM3	DQS3	64	MEM_B_DQS_P<2>	BI 15 88
		65	VSS	VSS	66		
88 15 BI	MEM_B_DQ<18>	67	DQ26	DQ30	68	MEM_B_DQ<19>	BI 15 88
88 15 BI	MEM_B_DQ<22>	69	DQ27	DQ31	70	MEM_B_DQ<23>	BI 15 88
		71	VSS	VSS	72		

KEY

516s0704

PP0V75_S3_MEM_VREFCA_B 27

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

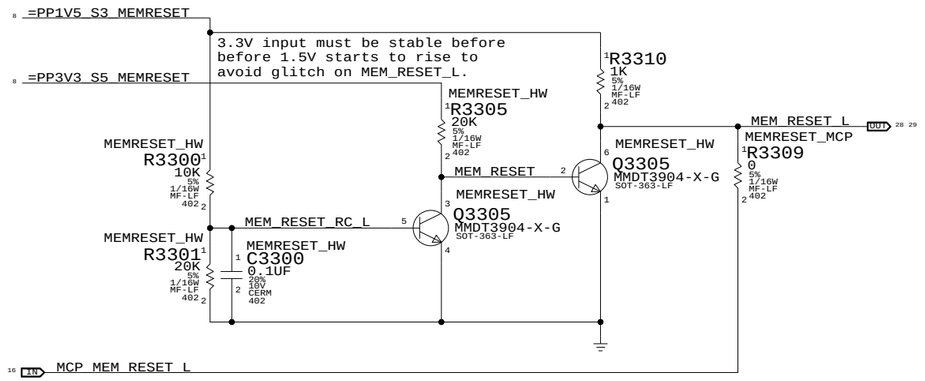
SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 29 OF 96	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 30 OF 96	

PCIE_MINI_PRSNT_L

Q3401
SSM6N15FEAPE
SOT563

AP_PWR_EN

MINI_CLKREQ_L

Q3401
SSM6N15FEAPE
SOT563

5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PLACEMENT_NOTE=Place close to J3401.

C3431 0.1uF 10% 16V X5R 402 PCIE_MINI_R2D_C_P

C3430 0.1uF 10% 16V X5R 402 PCIE_MINI_R2D_C_N

PLACEMENT_NOTE=Place close to J3401.

1000 mA peak
750 mA nominal max

L3404
FERR-120-OHM-1.5A
0402-LF

PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

C3422 1uF 20% 10V CERM 402

C3421 0.1uF 20% 10V CERM 402

C3420 10UF 20% 10V X5R 805

PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

Q3450
FDC606P_G
SOT-6

C3450 0.1UF 10% 16V X5R 402

P5VWLAN_SS

C3451 0.033UF 10% 16V X5R 402

R3450 100K 5% 1/16W MF-LF 402

R3451 10K 5% 1/16W MF-LF 402

=PP5V_S3_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

PM_WLAN_EN_L

PLACEMENT_NOTE=Place close to J3401.

PLACEMENT_NOTE=Place close to Q3450.

PLACEMENT_NOTE=Place close to Q3450.

AIRPORT

L3401
90-OHM-100MA
DLP11S

PCIE_CLK100M_MINI_P

PCIE_CLK100M_MINI_N

PLACEMENT_NOTE=Place close to J3401.

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_O_L
PCIE_WAKE_L

NC
NC

L3405
275 mA peak
206 mA nominal max
FERR-120-OHM-1.5A
0402-LF

PP5V_S3_BTCAMERA_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C3452 0.1UF 10% 16V CERM 402

=PP5V_S3_BTCAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

I2C_ALS_SDA
I2C_ALS_SCL

ALS CAMERA

USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

L3402
90-OHM
DLP0NS

USB_CAMERA_P

USB_CAMERA_N

PLACEMENT_NOTE=Place close to J3401.

CONN_USB2_BT_P
CONN_USB2_BT_N

BLUETOOTH

L3403
90-OHM
DLP0NS

USB_BT_P

USB_BT_N

PLACEMENT_NOTE=Place close to J3401.

PP5V_WLAN_F

=PP3V3_S3_WLAN

R3453 33K 5% 1/16W MF-LF 402

U3402
74LVC1G17DRL
SOT-553

TC7SZ08AFEAPE
SOT665

U3401

MINI_RESET_CONN_L

WLAN_SMIT_BUF

WLAN_SMIT_RC

NC
NC

C3453 1UF 10% 6.3V CERM 402

R3454 62K 5% 1/16W MF-LF 402

MINI_RESET_L

Right Clutch Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 31 OF 96	

EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

32 8 =PP3V3_S3_EXCARD
C3530 0.1uF 20% 10V CERM 402
C3531 10uF 20% 6.3V X5R 603

32 8 =PP1V5_S0_EXCARD
C3534 0.1uF 20% 10V CERM 402
C3535 10uF 20% 6.3V X5R 603

L3502

90-OHM DLP0NS SYM_VER_1

90 20 BI USB_EXCARD_N — 4 — 3 — USB2_EXCARD_CONN_N 7 32 95
90 20 BI USB_EXCARD_P — 1 — 2 — USB2_EXCARD_CONN_P 7 32 95

PLACEMENT_NOTE=Place close to J3500

L3503

90-OHM-100MA DLP11S SYM_VER_1

89 17 IN PCIE_CLK100M_EXCARD_N — 4 — 3 — PCIE_CLK100M_EXCARD_CONN_N 7 32 95
89 17 IN PCIE_CLK100M_EXCARD_P — 1 — 2 — PCIE_CLK100M_EXCARD_CONN_P 7 32 95

PLACEMENT_NOTE=Place close to J3500

PLACEMENT_NOTE=Place close to J3500

C3571 / C3570

89 17 IN PCIE_EXCARD_R2D_C_N — 1 — 2 — 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_N 7 32 89 95
89 17 IN PCIE_EXCARD_R2D_C_P — 1 — 2 — 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_P 7 32 89 95

C3570 PLACEMENT_NOTE=Place close to J3500

CRITICAL

J3500

502250-8727 F-RT-SM

95 89 32 7 PCIE_EXCARD_R2D_N — 4 — PCIE_EXCARD_R2D_P 7 32 89 95
89 17 7 OUT PCIE_EXCARD_D2R_P — 6 — PCIE_EXCARD_D2R_N 7 17 89 OUT
95 32 7 PCIE_CLK100M_EXCARD_CONN_N — 10 — PCIE_CLK100M_EXCARD_CONN_P 7 32 95
32 7 EXCARD_CLKREQ_CONN_L — 12 — EXCARD_CPPE_L 7 32
32 7 PP3V3_S0_EXCARD_SWITCH — 14 — PP3V3_S0_EXCARD_SWITCH 7 32
32 7 PP3V3_S3_EXCARD_SWITCH — 16 — PLT_RESET_SWITCH_L 7 32
32 7 PP1V5_S0_EXCARD_SWITCH — 18 — PCIE_WAKE_L 17 23 31 OUT
40 BI =SMBUS_EXCARD_SDA — 20 — PP1V5_S0_EXCARD_SWITCH 7 32
NC — 22 — =SMBUS_EXCARD_SCL 45 BI
32 7 EXCARD_CPUSB_L — 24 — NC
95 32 7 USB2_EXCARD_CONN_N — 26 — USB2_EXCARD_CONN_P 7 32 95

28 29 27 25 23 NC

32 7 EXCARD_CPPE_L — R3501 0.1 MF-LF 402 2 5% 1/16W — PCIE_EXCARD_PRSNT_L 17

OUTPUT DECOUPLING

CRITICAL

U3500

TPS2231

32 8 =PP3V3_S3_EXCARD	17 AUXIN	AUXOUT	15
32 8 =PP3V3_S0_EXCARD	2 VIN3P3	VOUT3P3	3
32 8 =PP1V5_S0_EXCARD	12 VIN1P5	VOUT1P5	11
42 IN SMC_EXCARD_PWR_EN	20 SHDN*	PERST*	8
TP_EXCARD_STBY_L	1 STBY*	CPPE*	10
26 IN EXCARD_RESET_L	6 SYSRST*	CPUSB*	9
43 28 IN EXCARD_OC_L	19 OC*		
NC	4 NC0	RCLKEN	18 EXCARD_RCLKEN 32
NC	5 NC1		
NC	13 NC2		
NC	14 NC3		
NC	16 NC4	THRML_PAD	21
		GND	7

R3500 0 MF-LF 402 2 5% 1/16W — EXCARD_SHDN_L_R

PP3V3_S3_EXCARD_SWITCH 7 32
VOLTAGE=3.3V MIN_LINE_WIDTH=.3mm MIN_NECK_WIDTH=0.2mm
C3500 0.1uF 20% 10V CERM 402
C3503 10uF 20% 6.3V X5R 603

PP3V3_S0_EXCARD_SWITCH 7 32
VOLTAGE=3.3V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3501 0.1uF 20% 10V CERM 402
C3504 10uF 20% 6.3V X5R 603

PP1V5_S0_EXCARD_SWITCH 7 32
VOLTAGE=1.5V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3502 0.1uF 20% 10V CERM 402
C3505 10uF 20% 6.3V X5R 603

PLT_RESET_SWITCH_L 7 32
EXCARD_CPPE_L 7 32
EXCARD_CPUSB_L 7 32

C3573 / C3572 VENICE

95 9 IN PCIE_FC_R2D_C_P — 1 — 2 — 0.1uF 10% 16V X5R 402 — PCIE_FC_R2D_P 95 9
95 9 IN PCIE_FC_R2D_C_N — 1 — 2 — 0.1uF 10% 16V X5R 402 — PCIE_FC_R2D_N 95 9

C3572 VENICE
PLACEMENT_NOTE=Place close to J3501.

CRITICAL

J3501

503219-0221 M-ST-SM

9 OUT FC_CLKREQ_L — 1 — 2
95 9 IN PCIE_CLK100M_FC_P — 3 — 4
95 9 IN PCIE_CLK100M_FC_N — 5 — 6
NC — 7 — 8
=PP3V3_FC_CON 8 — 9 — 10
NC — 11 — 12
NC — 13 — 14
=PP1V5_FC_CON 8 — 15 — 16
NC — 17 — 18
95 9 OUT PCIE_FC_D2R_P — 19 — 20 — FC_PRSNT_L 9 OUT
95 9 OUT PCIE_FC_D2R_N — 21 — 22 — FC_RESET_L 9 OUT

23 24 25 26 NC

VENICE

Venice Connector

U3551

32 8 =PP3V3_S3_EXCARD
32 7 EXCARD_CPUSB_L — 1
32 7 EXCARD_CPPE_L — 2
3
5 74HC1G00GWDG SC70-5
SMC_EXCARD_CP OUT 42 43

C3550 0.1uF 20% 10V CERM 402

U3561

32 8 =PP3V3_S0_EXCARD
R3561 100K 1% 1/16W MF-LF 402
32 7 EXCARD_CLKREQ_CONN_L — B1
A2 U3561 SN74LVC1G04YZPR C2 C1 BGA

U3560

32 EXCARD_RCLKEN — 1
EXCARD_CLKREQ_CONN — 2
3
5 74HC1G00GWDG SC70-5
4 EXCARD_CLKREQ_L OUT 17

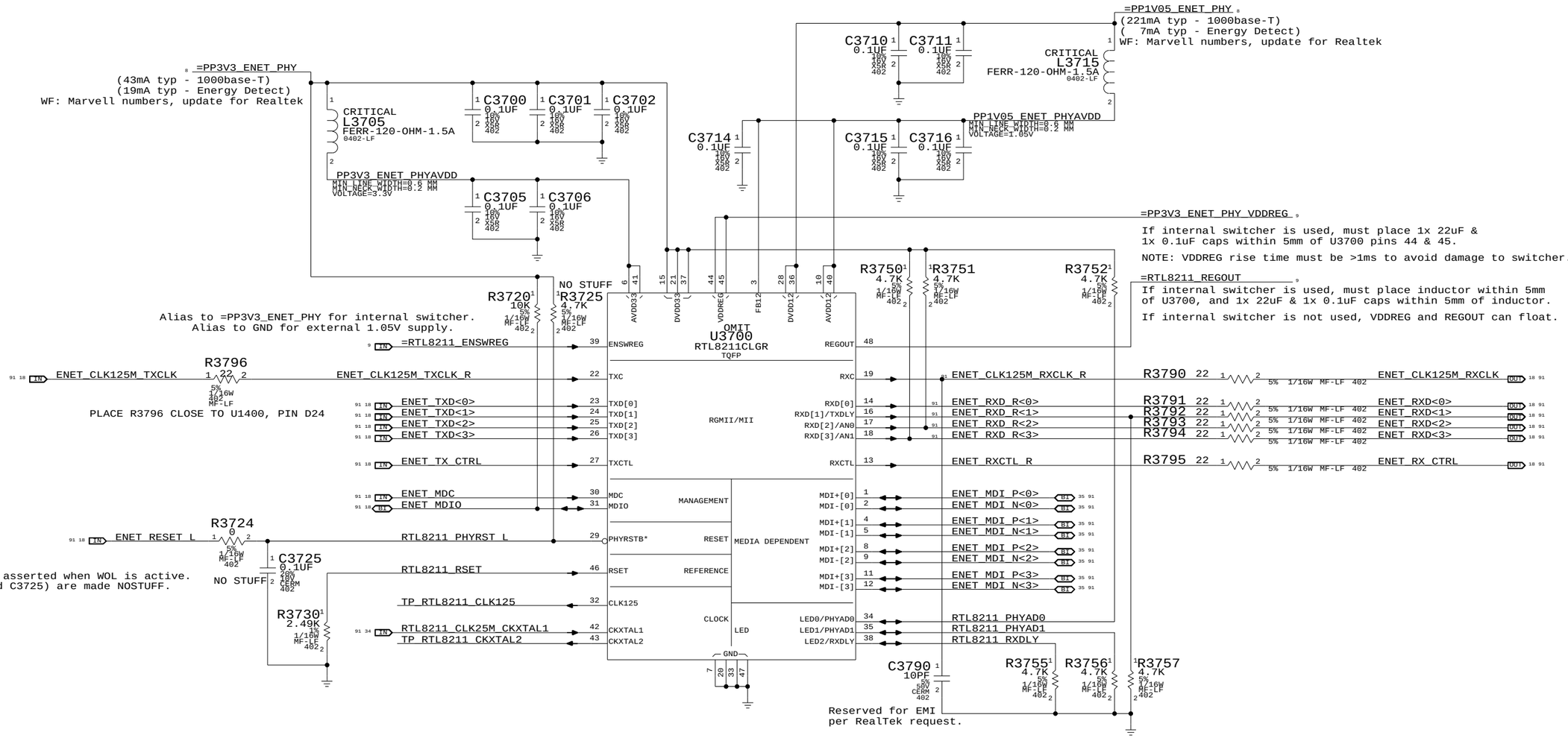
C3560 0.1uF 20% 10V CERM 402

ExpressCard Connector

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 32 OF 96	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

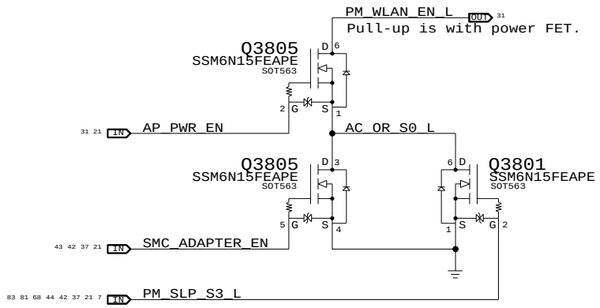
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 33 OF 96	

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

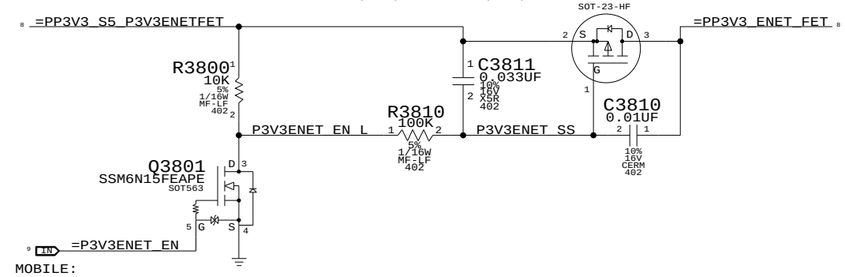
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

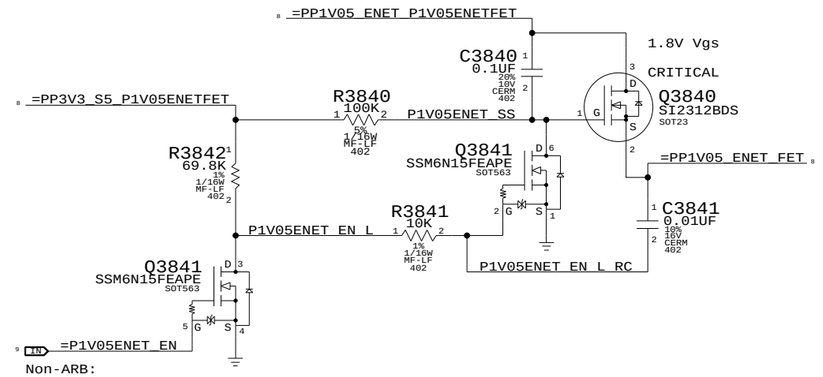
CRITICAL
Q3810
NTR4101P
SOT-23-HF



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

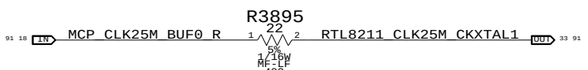


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

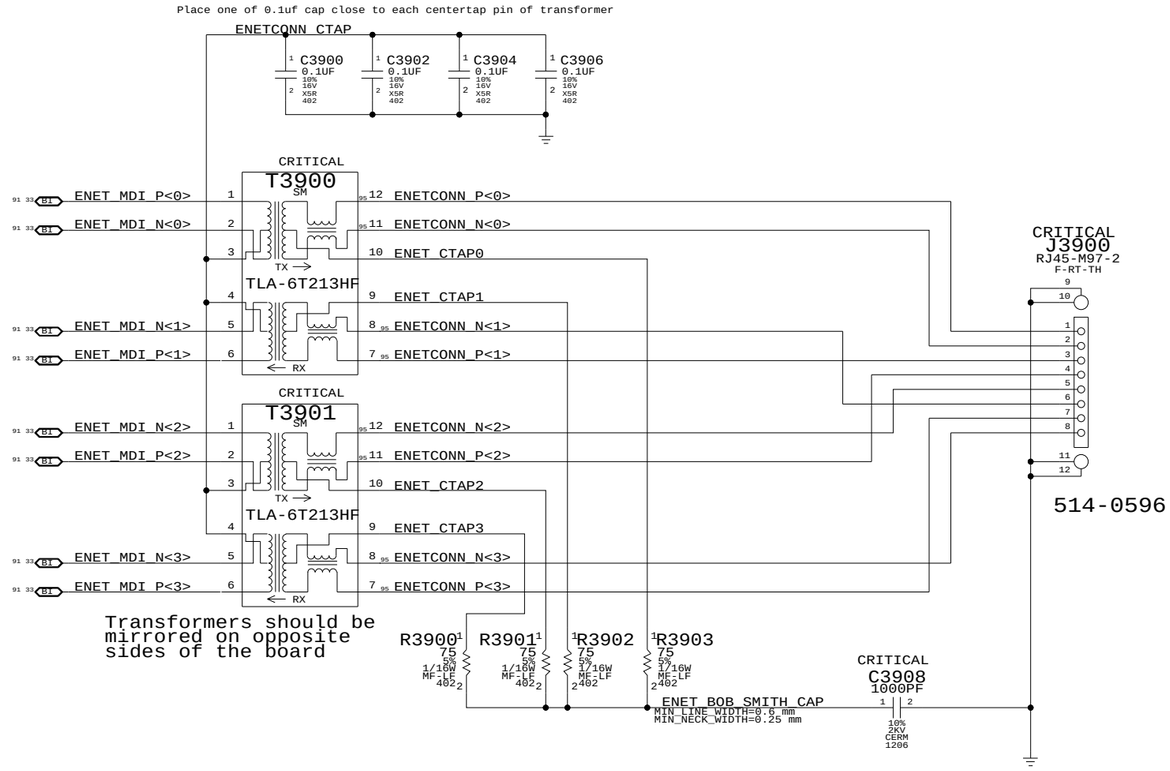
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 34 OF 96	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

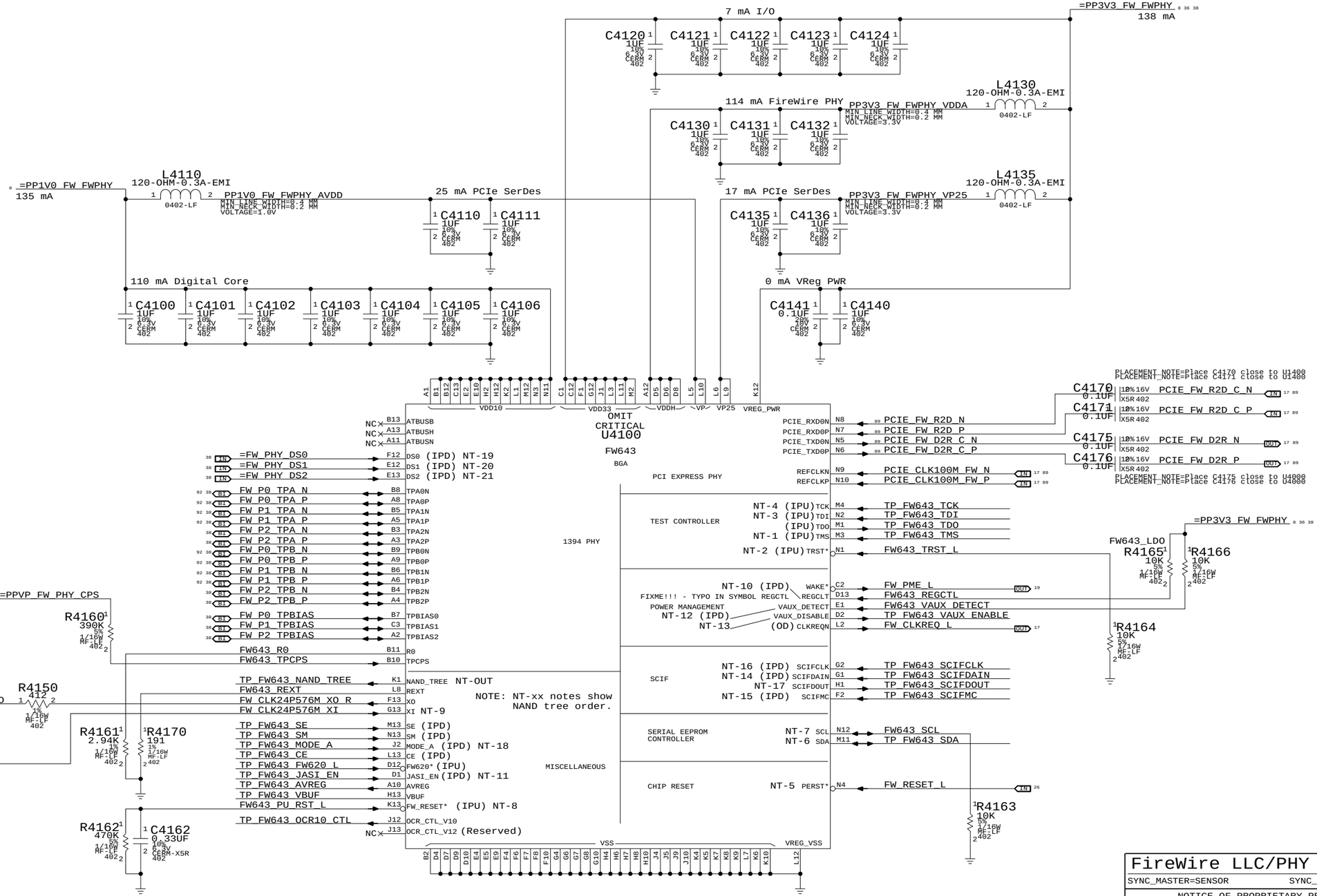


Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 35 OF 96	


7 mA I/O
=PP3V3_FW_FWPHY
138 mA
C4120 C4121 C4122 C4123 C4124
1UF 10% 6.3V CERM 402
L4130
120-OHM-0.3A-EMI
114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
0402-LF
C4130 C4131 C4132
1UF 10% 10V CERM 402
L4135
120-OHM-0.3A-EMI
17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
C4135 C4136
0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402
=PP1V0_FW_FWPHY
135 mA
L4110
120-OHM-0.3A-EMI
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
25 mA PCIe SerDes
C4110 C4111
110 mA Digital Core
C4100 C4101 C4102 C4103 C4104 C4105 C4106
PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000
VDD10 VDD33 VDDH VP VP25 VREG_PWR
OMIT
CRITICAL
U4100
FW643
BGA
PCI EXPRESS PHY
PCIE_RXD0N PCIE_FW_R2D_N
PCIE_RXD0P PCIE_FW_R2D_P
PCIE_TXD0N PCIE_FW_D2R_C_N
PCIE_TXD0P PCIE_FW_D2R_C_P
REFCLKN PCIE_CLK100M_FW_N
REFCLKP PCIE_CLK100M_FW_P
ATBUSB
ATBUSH
ATBUSN
=FW_PHY_DS0
=FW_PHY_DS1
=FW_PHY_DS2
DS0 (IPD) NT-19
DS1 (IPD) NT-20
DS2 (IPD) NT-21
FW_P0_TPA_N
FW_P0_TPA_P
FW_P1_TPA_N
FW_P1_TPA_P
FW_P2_TPA_N
FW_P2_TPA_P
FW_P0_TPB_N
FW_P0_TPB_P
FW_P1_TPB_N
FW_P1_TPB_P
FW_P2_TPB_N
FW_P2_TPB_P
TPA0N TPA0P TPA1N TPA1P TPA2N TPA2P TPB0N TPB0P TPB1N TPB1P TPB2N TPB2P
1394 PHY
TEST CONTROLLER
NT-4 (IPU) TCK TP_FW643_TCK
NT-3 (IPU) TDI TP_FW643_TDI
(IPU) TDO TP_FW643_TDO
NT-1 (IPU) TMS TP_FW643_TMS
NT-2 (IPU) TRST* FW643_TRST_L
=PP3V3_FW_FWPHY
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
=PPVP_FW_PHY_CPS
R4160 390K 5% 1/16W MF-LF 402
FW643_R0
FW643_TPCPS
TPBIAS0 TPBIAS1 TPBIAS2
FW_P0_TPBIAS
FW_P1_TPBIAS
FW_P2_TPBIAS
R0 TPCPS
NT-10 (IPD) WAKE* FW_PME_L
FIXME!!! - TYPO IN SYMBOL REGCTL REGCLT FW643_REGCTL
POWER MANAGEMENT
NT-12 (IPD) VAUX_DETECT FW643_VAUX_DETECT
NT-13 (OD) VAUX_DISABLE TP_FW643_VAUX_ENABLE
CLKREQN FW_CLKREQ_L
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150
24.576MHZ
SM-3.2X2.5MM
R4150 412 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402
TP_FW643_NAND_TREE
FW643_REXT
FW_CLK24P576M_XO_R
FW_CLK24P576M_XI
NAND_TREE NT-OUT
REXT
XO
XI NT-9
NOTE: NT-xx notes show NAND tree order.
TP_FW643_SE
TP_FW643_SM
TP_FW643_MODE_A
TP_FW643_CE
TP_FW643_FW620_L
TP_FW643_JASI_EN
TP_FW643_AVREG
TP_FW643_VBUF
FW643_PU_RST_L
SE (IPD)
SM (IPD)
MODE_A (IPD) NT-18
CE (IPD)
FW620* (IPU)
JASI_EN (IPD) NT-11
AVREG
VBUF
FW_RESET* (IPU) NT-8
MISCELLANEOUS
SCIF
NT-16 (IPD) SCIFCLK TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN TP_FW643_SCIFDAIN
NT-17 SCIFDOUT TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC TP_FW643_SCIFMC
SERIAL EEPROM CONTROLLER
NT-7 SCL FW643_SCL
NT-6 SDA TP_FW643_SDA
CHIP RESET
NT-5 PERST* FW_RESET_L
R4163 10K 5% 1/16W MF-LF 402
TP_FW643_OCR10_CTL
OCR_CTL_V10
OCR_CTL_V12 (Reserved)
VSS VREG_VSS
FireWire LLC/PHY (FW643)
SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008
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APPLE INC.
SIZE D
DRAWING NUMBER 051-7546
REV. A.0.0
SCALE NONE
SHT 36 OF 96

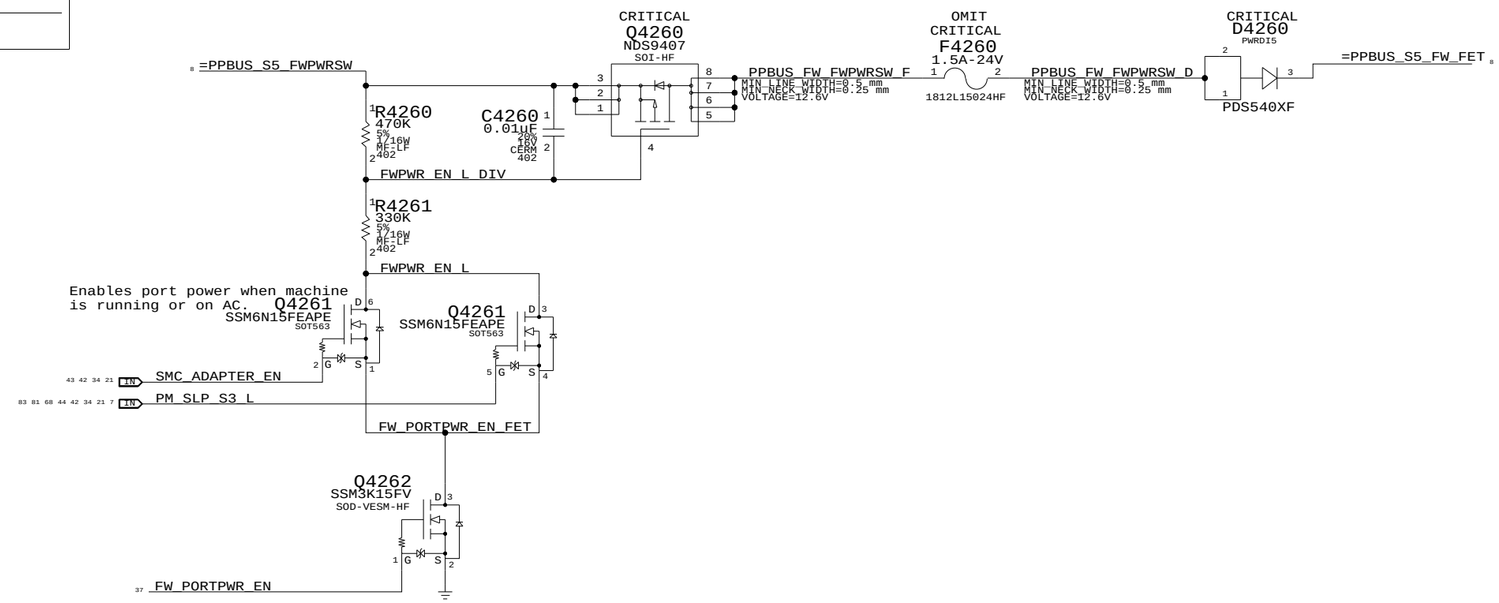
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

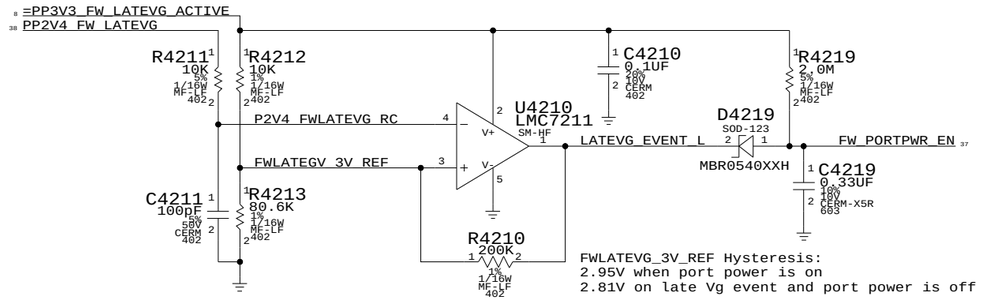
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
740S0080	1	LITTLEFUSE, 1.5A RESETTABLE 24V	F4260	CRITICAL	

FireWire Port Power

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 37 OF 96	

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

38 36 8 =PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE = =FW_PHY_DS0 36

FWPHY_DS2 MAKE_BASE=TRUE = =FW_PHY_DS2 36

FWPHY_DS1 MAKE_BASE=TRUE = =FW_PHY_DS1 36

R4381 10K 1% 1/10W MF-LF 402

36 FW_P0_TPBIAS = NC_FW0_TPBIAS MAKE_BASE=TRUE

36 FW_P2_TPBIAS = NC_FW2_TPBIAS MAKE_BASE=TRUE

92 36 FW_P0_TPA_N = NC_FW0_TPAN MAKE_BASE=TRUE

92 36 FW_P0_TPA_P = NC_FW0_TPAP MAKE_BASE=TRUE

36 FW_P2_TPA_N = NC_FW2_TPAN MAKE_BASE=TRUE

36 FW_P2_TPA_P = NC_FW2_TPAP MAKE_BASE=TRUE

92 36 FW_P0_TPB_N = NC_FW0_TPBN MAKE_BASE=TRUE

92 36 FW_P0_TPB_P = NC_FW0_TPBP MAKE_BASE=TRUE

36 FW_P2_TPB_N = NC_FW2_TPBN MAKE_BASE=TRUE

36 FW_P2_TPB_P = NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

36 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

92 36 FW_P1_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE 38

92 36 FW_P1_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE 38

92 36 FW_P1_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE 38

92 36 FW_P1_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE 38

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 50V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

8 =PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW SOT-363 (SYM-VER2)

R4311 470K 5% 1/10W MF-LF 402

PPVP_FW_PHY_CPS MAKE_BASE=TRUE = =PPVP_FW_PHY_CPS 36

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CPS_EN_L_DIV

R4312 330K 5% 1/10W MF-LF 402

CPS_EN_L

38 36 8 =PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

Cable Power

8 =PPVP_FW_PORT1

CRITICAL
L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

"Snapback" & "Late VG" Protection

38 37 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363

C4311 0.01uF 10% 50V X7R 402

DP4310 BAV99DW-X-G SOT-363

C4310 0.01uF 10% 50V X7R 402

38 FW_PORT1_TPB_N

38 FW_PORT1_TPB_P

38 FW_PORT1_TPA_N

38 FW_PORT1_TPA_P

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

DP4311 BAV99DW-X-G SOT-363

C4313 0.01uF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

PORT 1

BILINGUAL

CRITICAL
J4310 1394B-M97 F-RT-TH1

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

TPB- TPB(R)
TPB+ TPB<R> OUTPUT
VP
NC VG
TPA- TPA(R)
TPA+ TPA<R> INPUT
CABLE OUTER SHLD
CHASSIS GND

514S0605

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power

8 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V

CRITICAL
D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

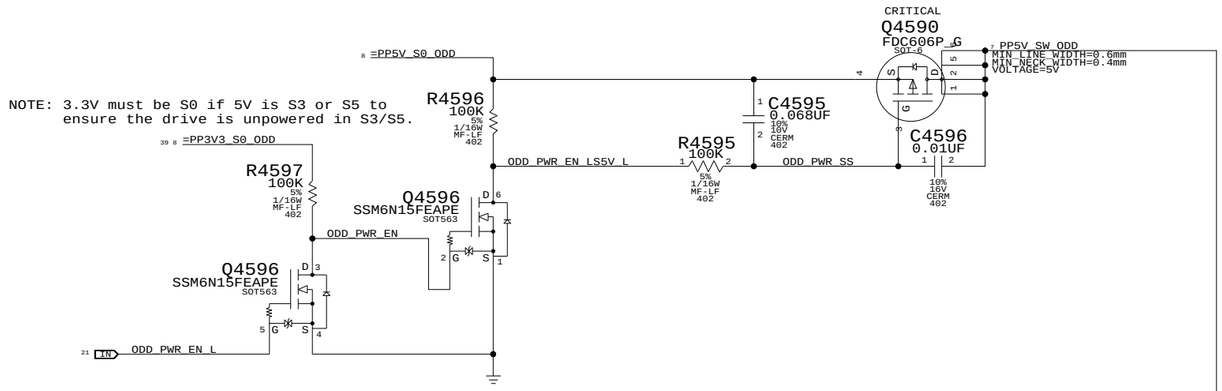
FireWire Ports

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

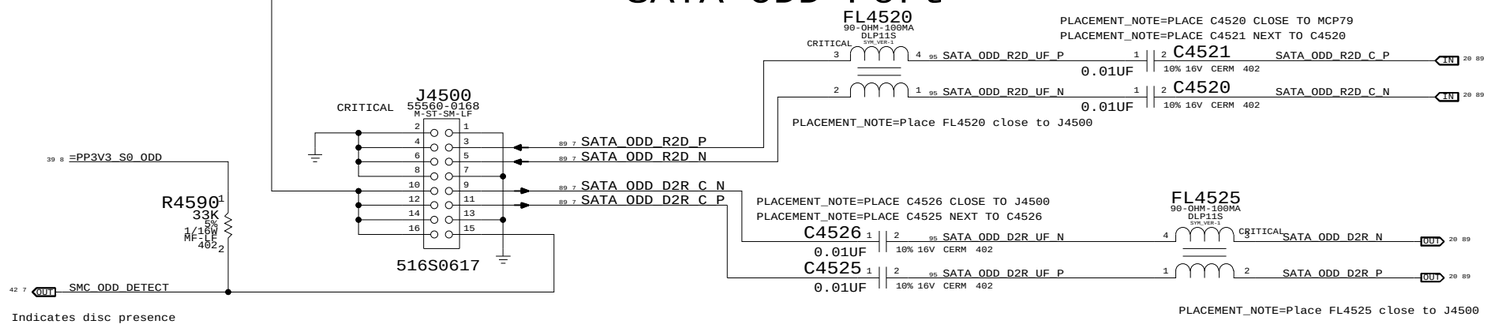
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 38 OF 96	

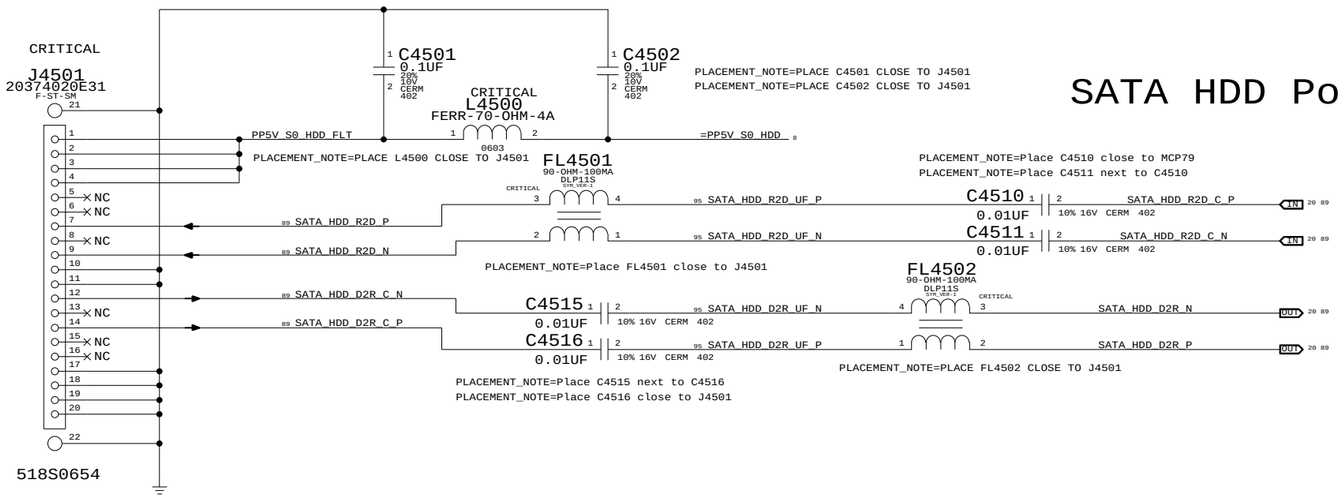
ODD Power Control



SATA ODD Port



SATA HDD Port



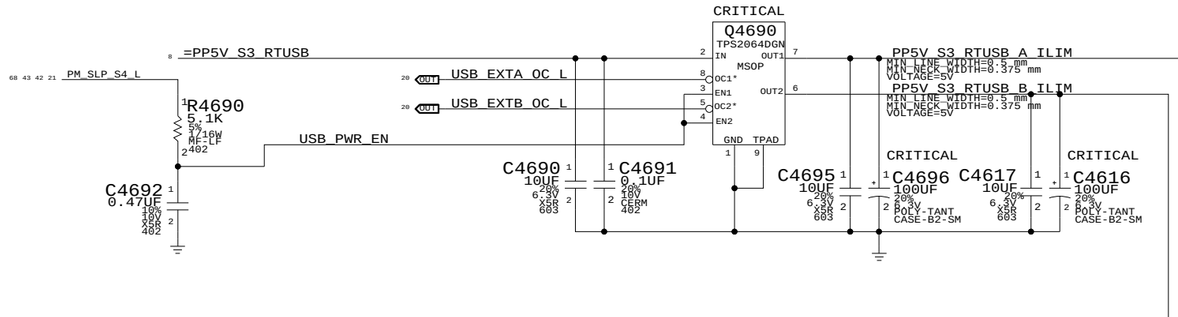
SATA Connectors

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

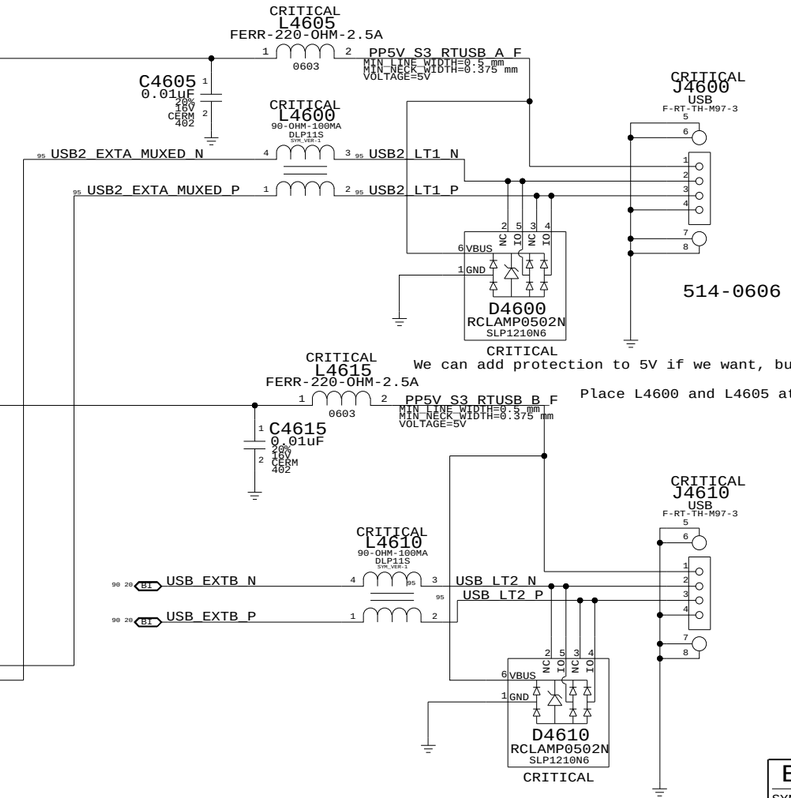
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 39 OF 96	

Port Power Switch



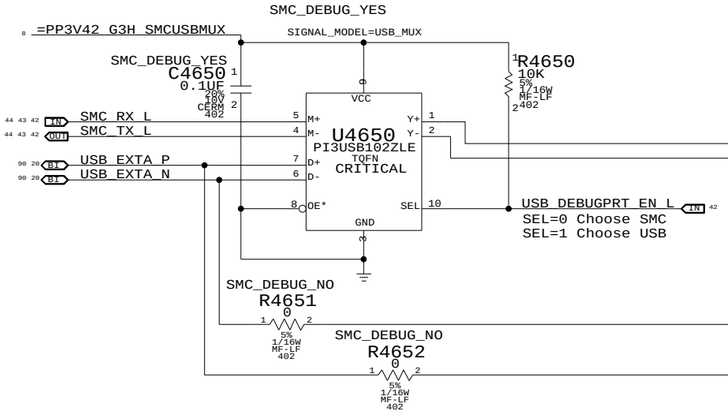
Left USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



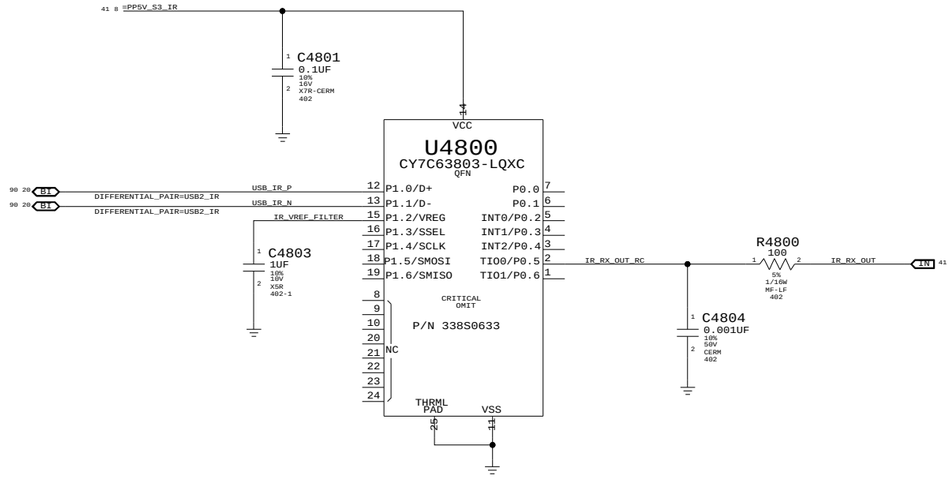
Left USB Port B

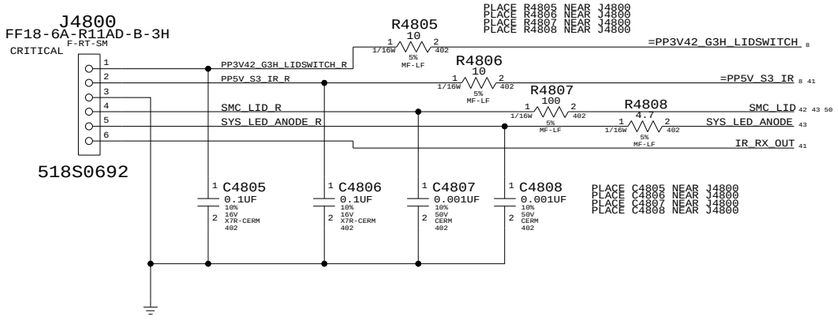
External USB Connectors

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 40 OF 96	





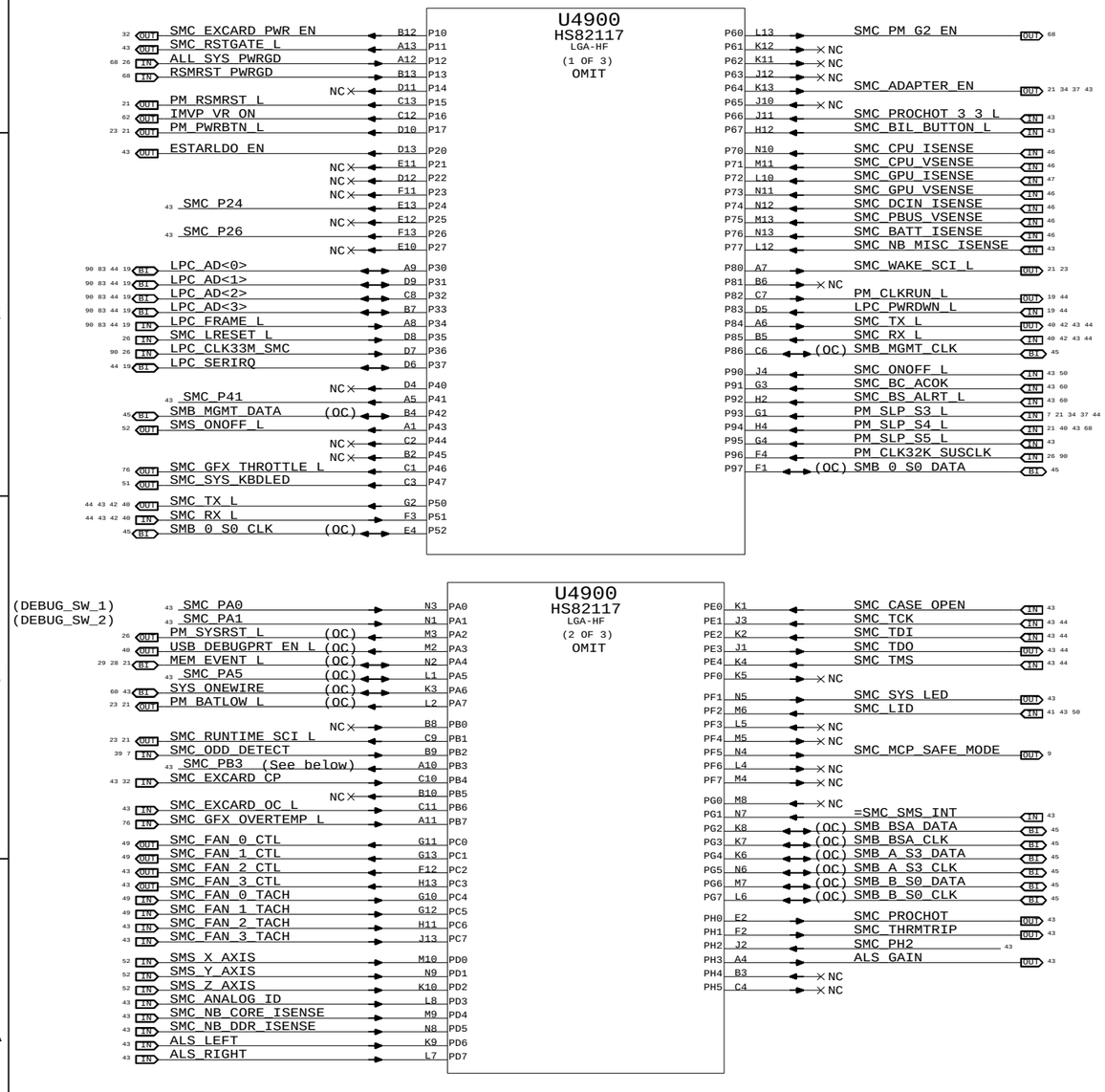
Front Flex Support

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

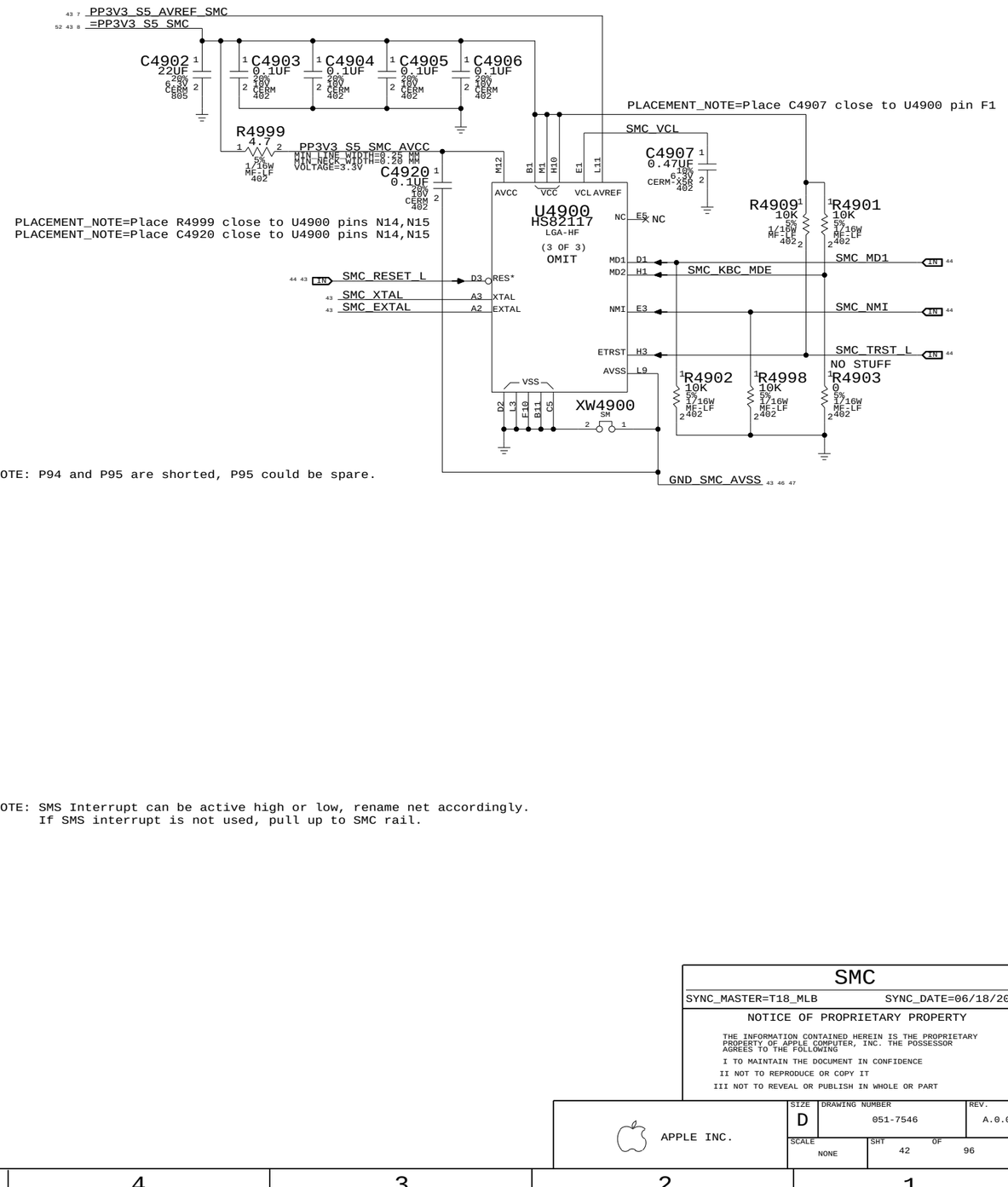
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 41 OF 96	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

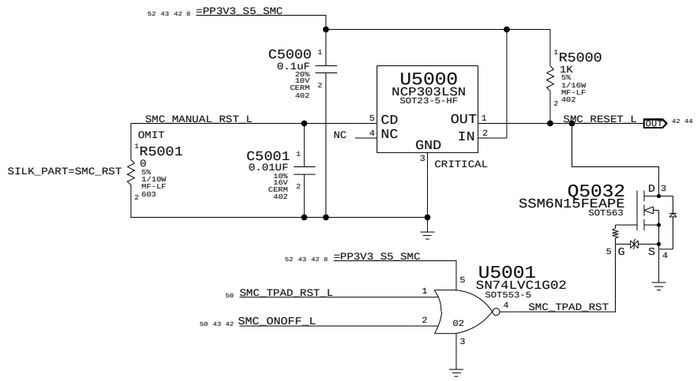
SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

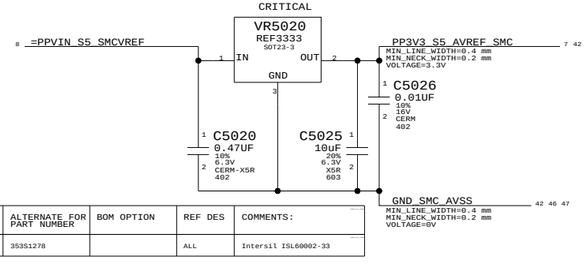
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 42 OF 96	

SMC Reset "Button" / Brownout Detect

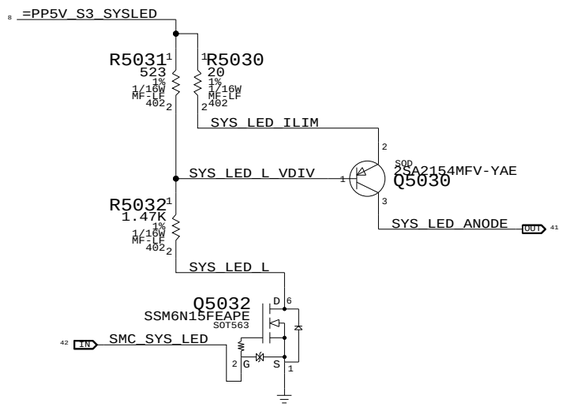


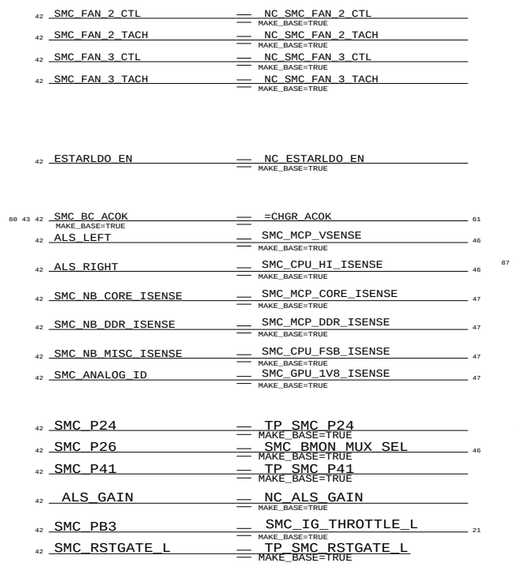
SMC AVREF Supply



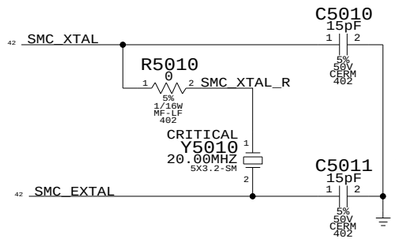
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit

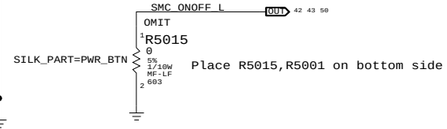


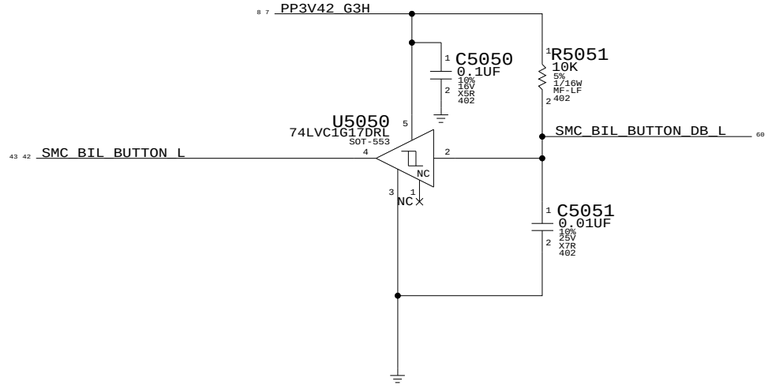


SMC Crystal Circuit

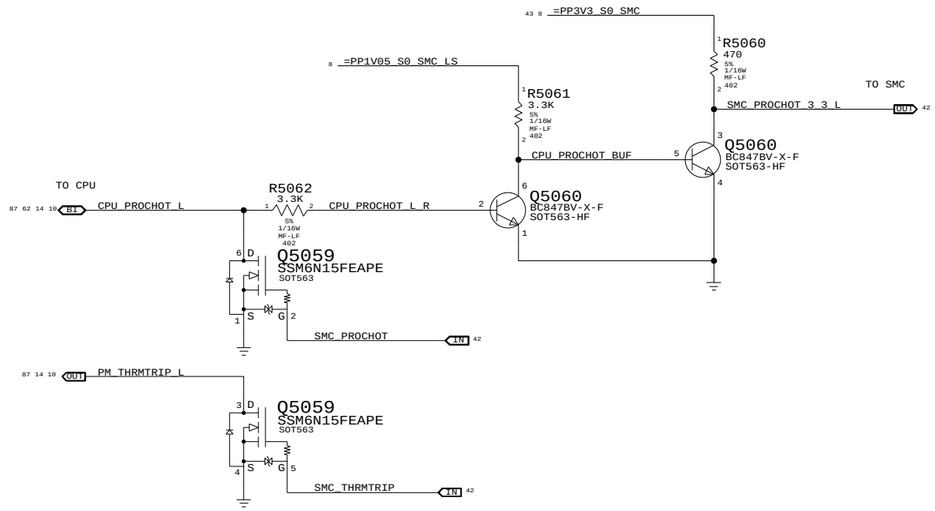


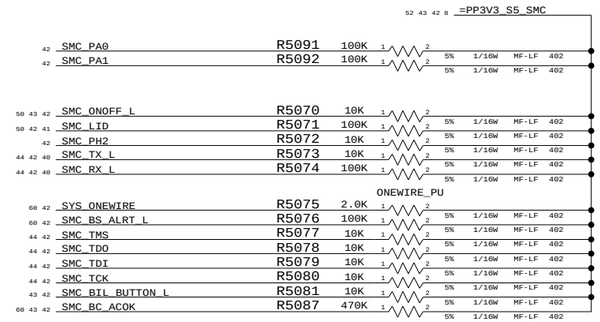
Debug Power "Button"

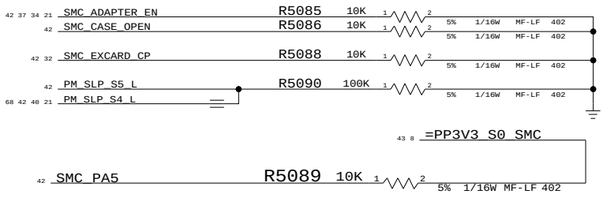




SMC FSB to 3.3V Level Shifting







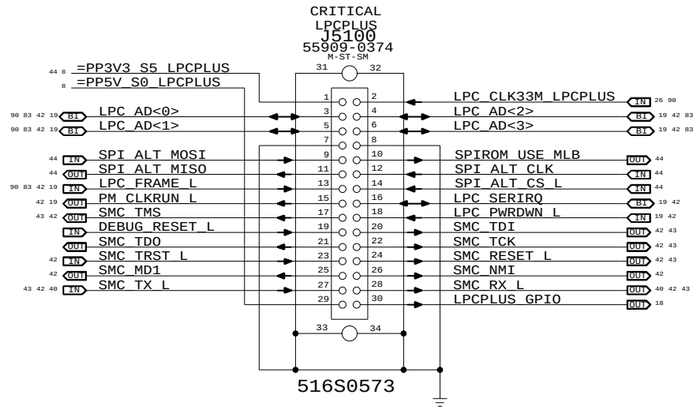
SMC Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

APPLE INC.

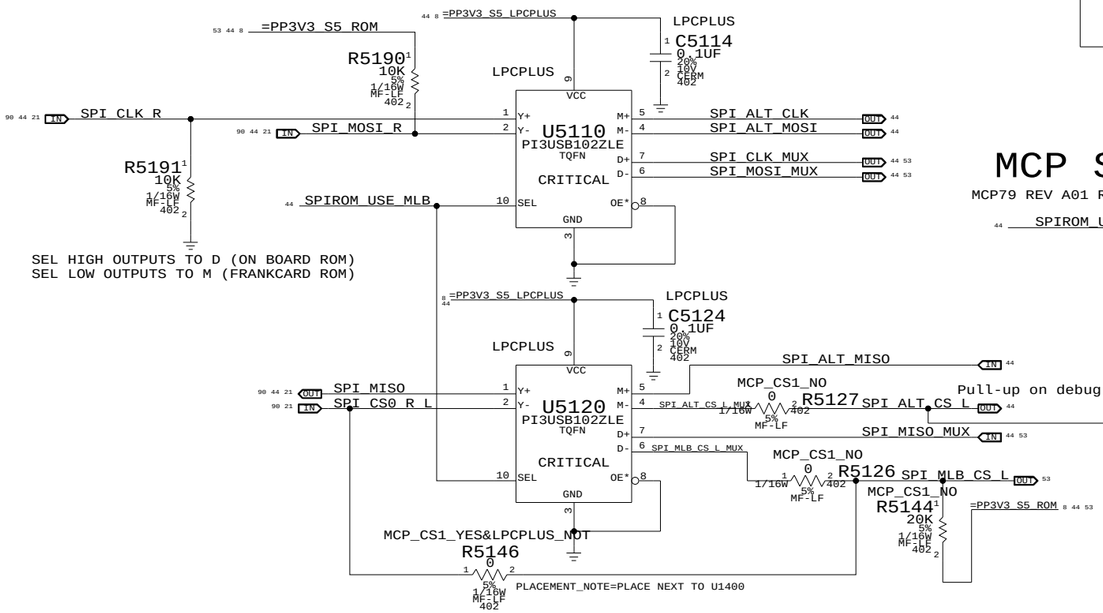
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 43 OF 96	

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

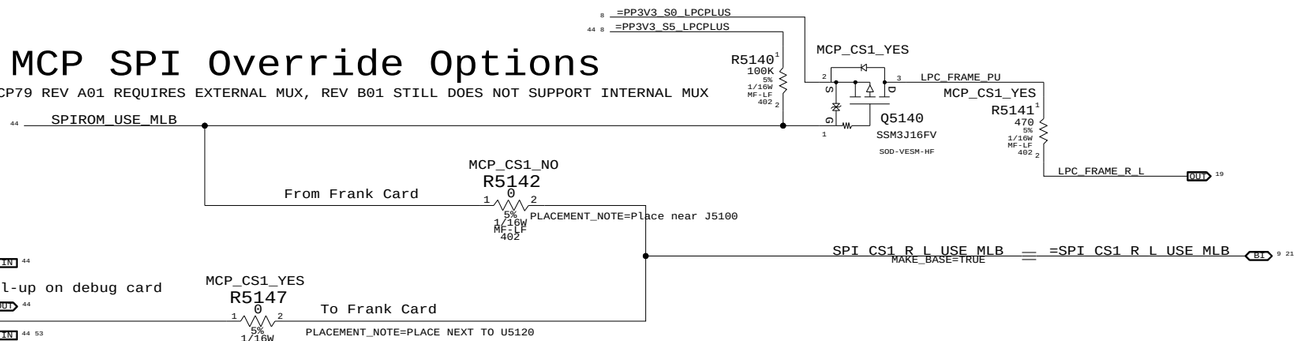


MCP79 Internal SPI MUX Support

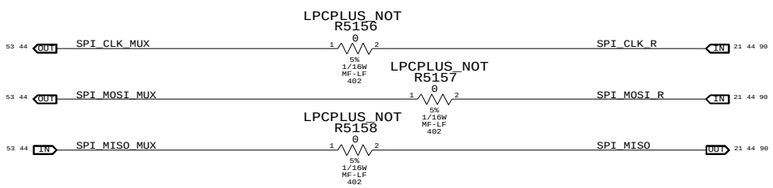
NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

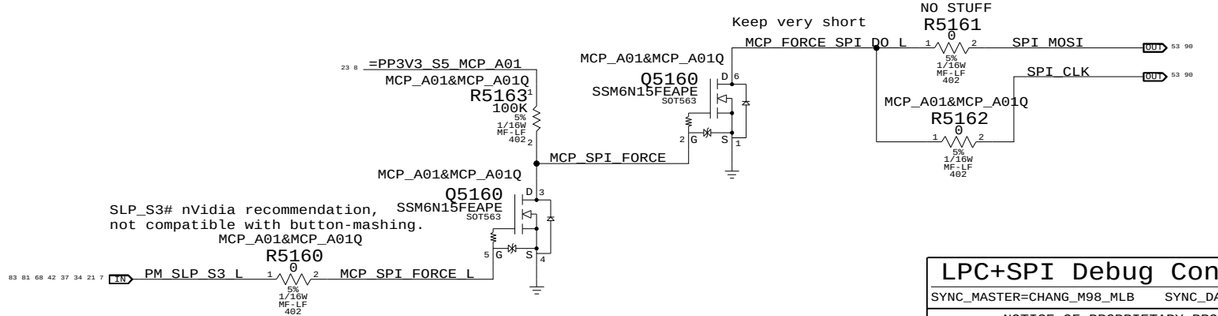


SPI MUX BYPASS



SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED.NOT NEEDED FOR B01 OR LATER.



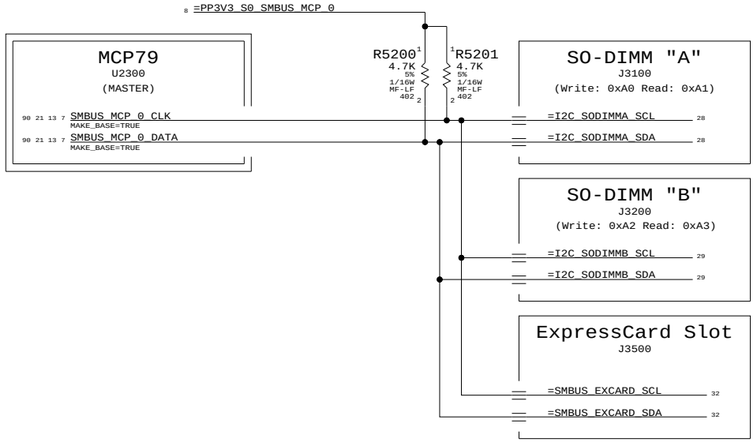
LPC+SPI Debug Connector

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

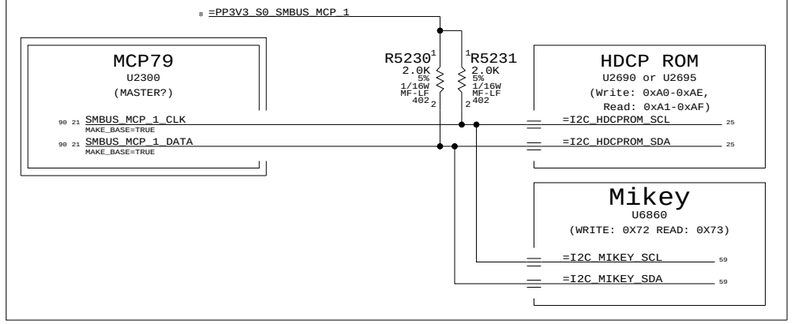
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 44 OF 96	

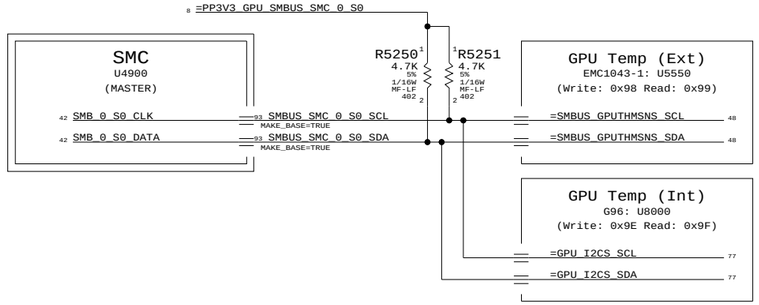
MCP79 SMBus "0" Connections



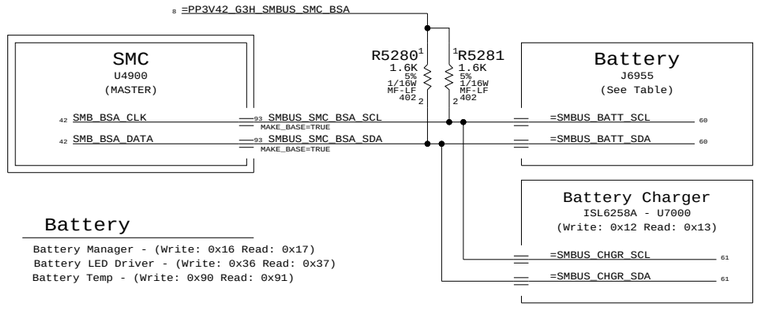
MCP79 SMBus "1" Connections



SMC "0" SMBus Connections



SMC "Battery A" SMBus Connections

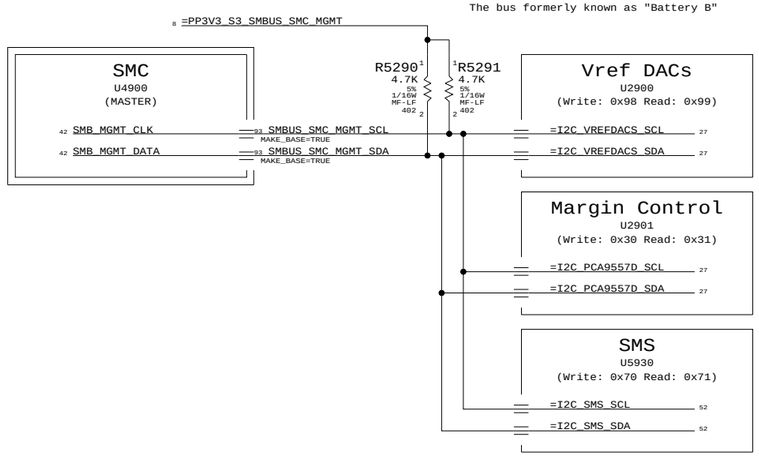


Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

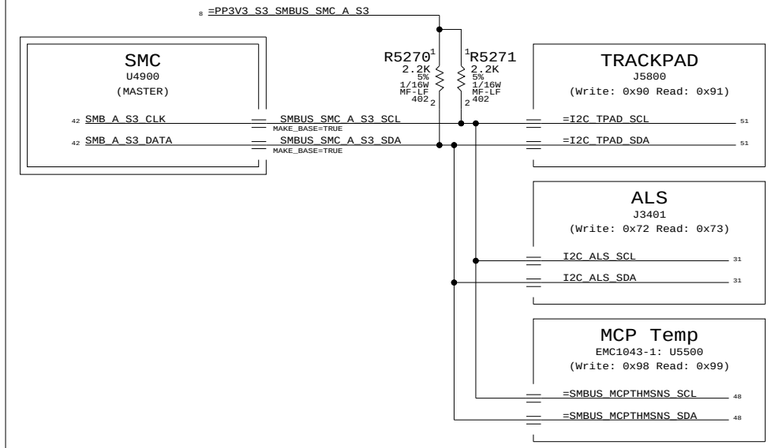
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

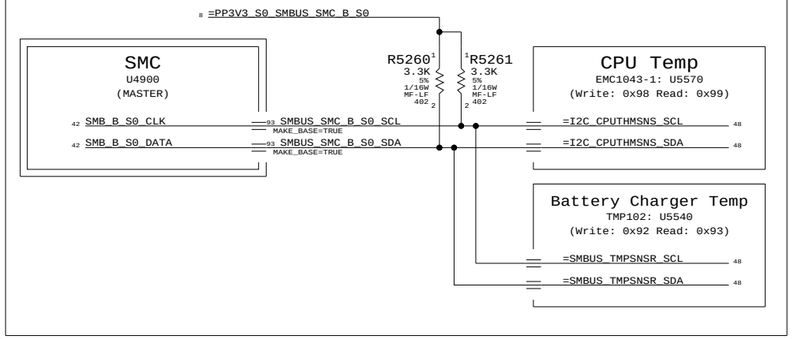


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



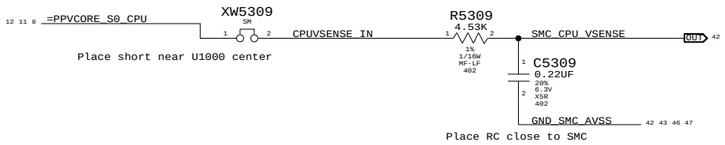
M98 SMBus Connections

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 45 OF 96	

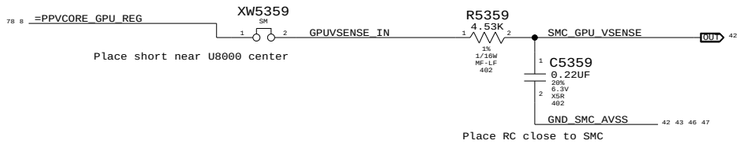
CPU Voltage Sense / Filter



Place short near U1000 center

Place RC close to SMC

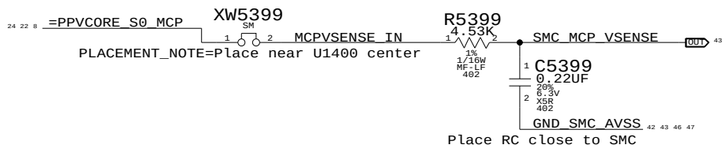
GPU Voltage Sense / Filter



Place short near U8000 center

Place RC close to SMC

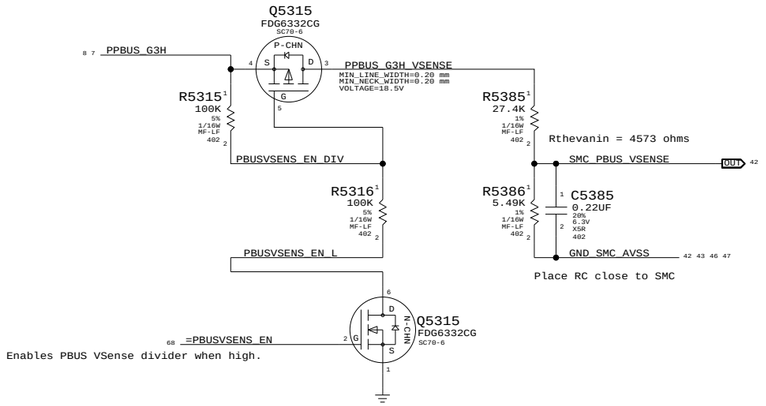
MCP Voltage Sense / Filter



PLACEMENT_NOTE=Place near U1400 center

Place RC close to SMC

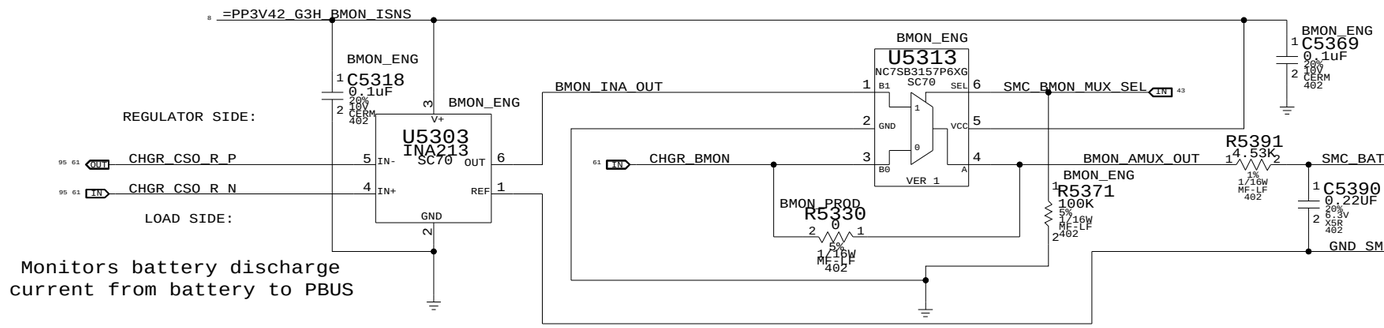
PBUS Voltage Sense & Filter



Place RC close to SMC

Enables PBUS VSense divider when high.

BMON Current Sense - Entire circuit must be near SMC (U4900)

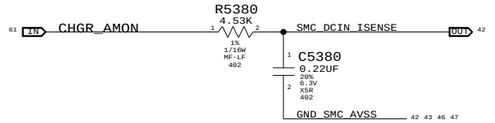


Monitors battery discharge current from battery to PBUS

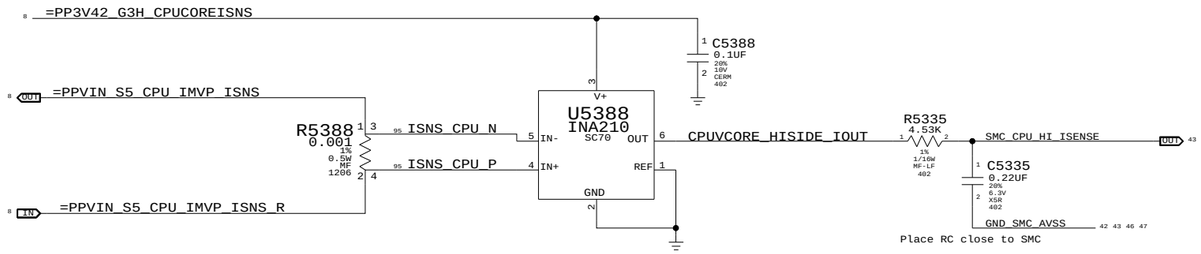
INA213 has gain of 50V/V

DCIN Current Sense Filter

Place RC close to SMC



CPU VCore High Side Current Sensor

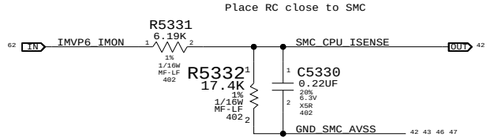


Place RC close to SMC

Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

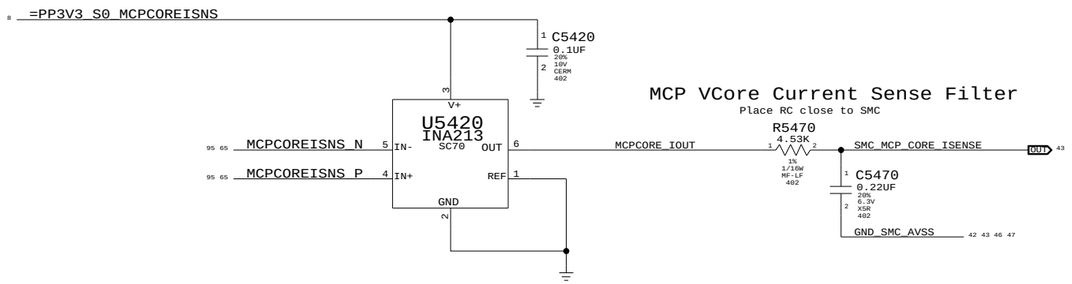
CPU VCore Load Side Current Sense / Filter

Place RC close to SMC

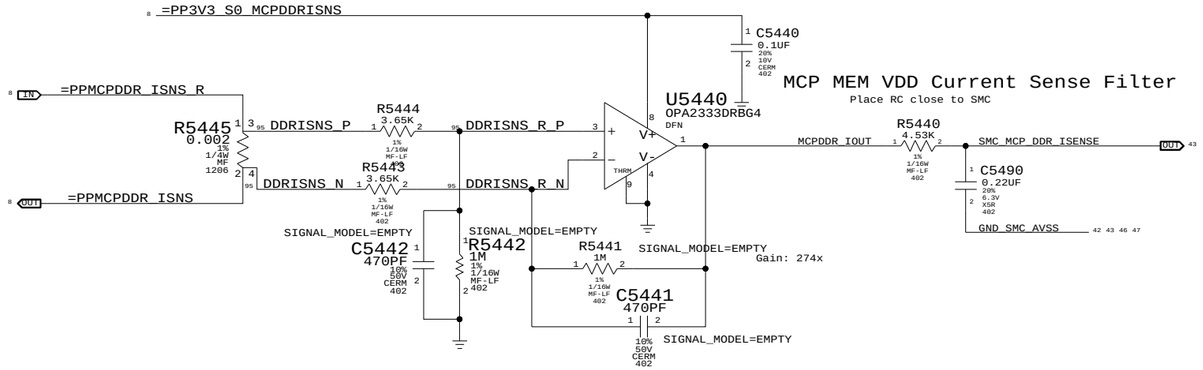


Current & Voltage Sensing			
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7546	REV: A.0.0
	SCALE: NONE	SHT: 46	OF: 96

MCP VCore Current Sense



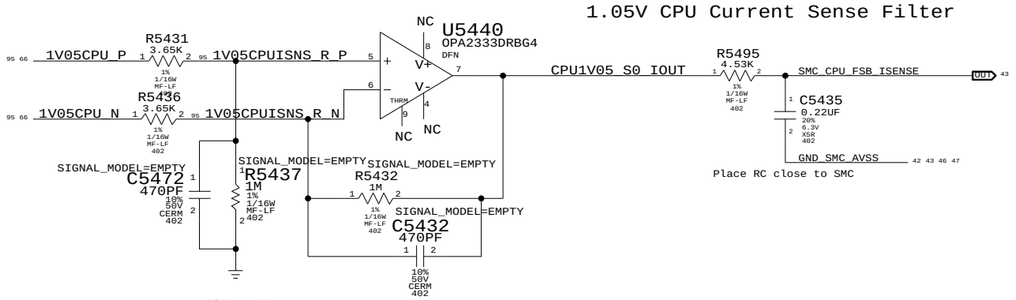
MCP MEM VDD Current Sense



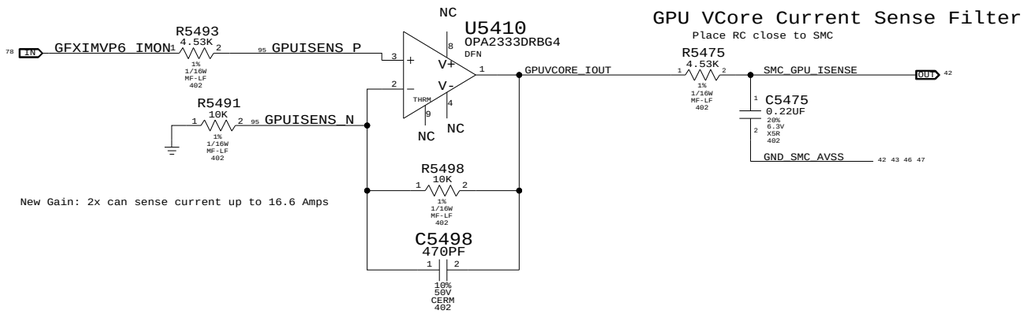
OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense

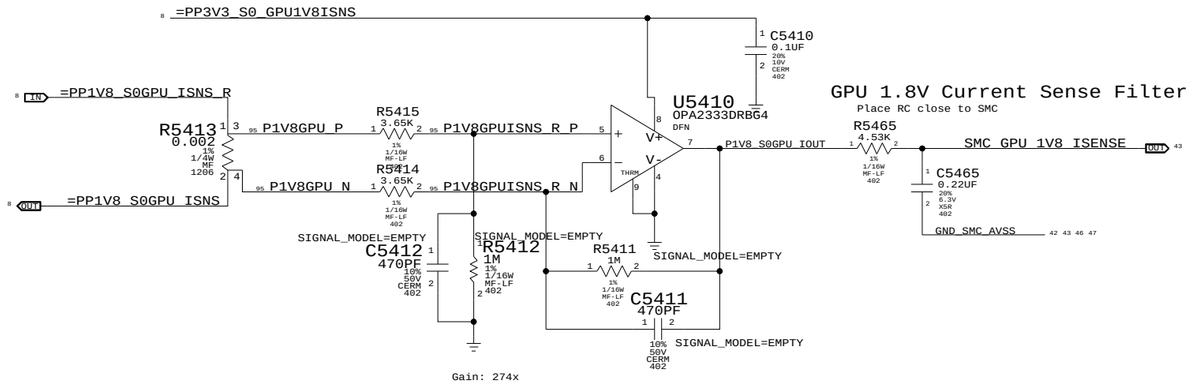


GPU VCore Current Sense



GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

GPU 1.8V Current Sense



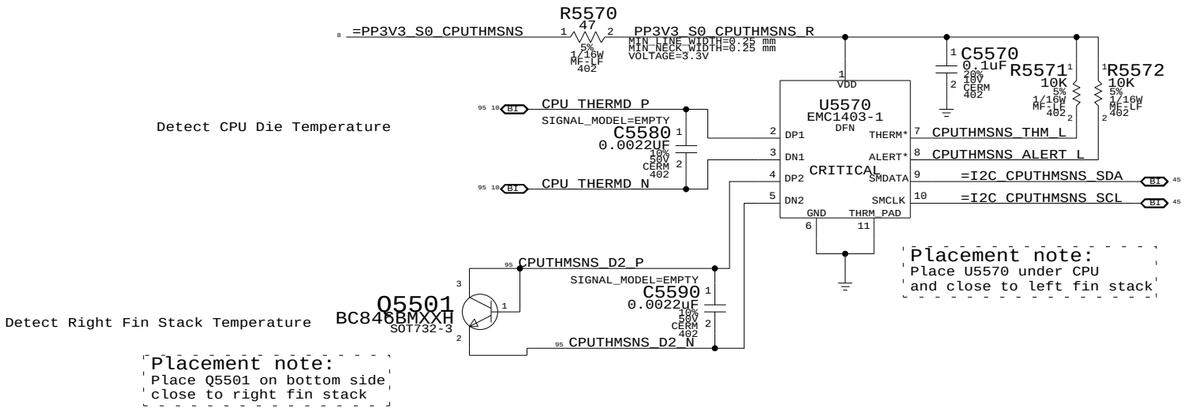
Current Sensing

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

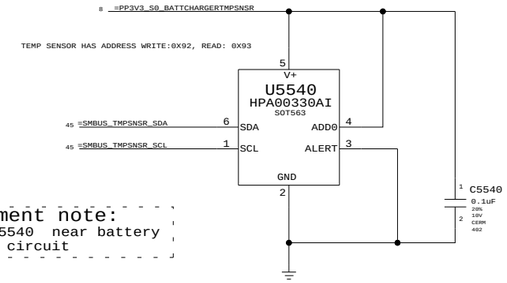
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 47 OF 96	

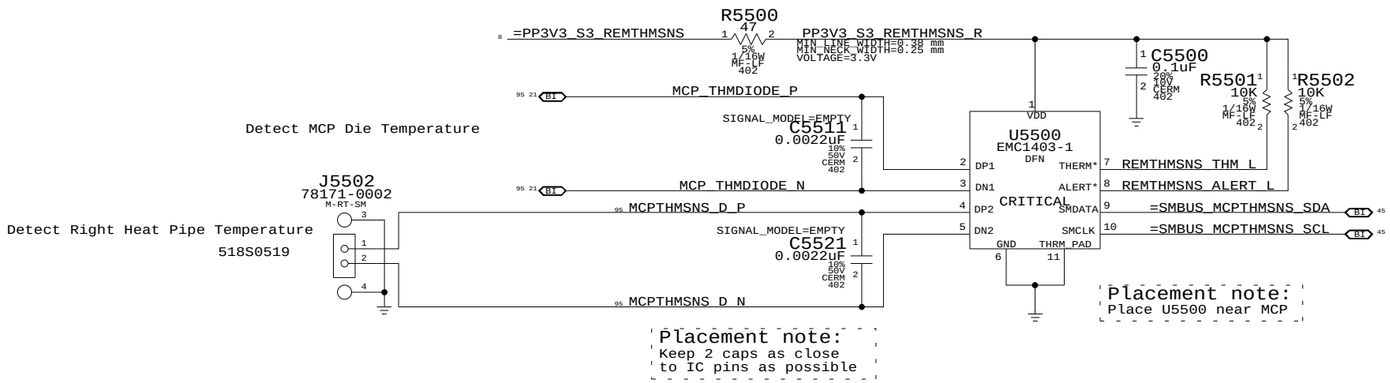
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity

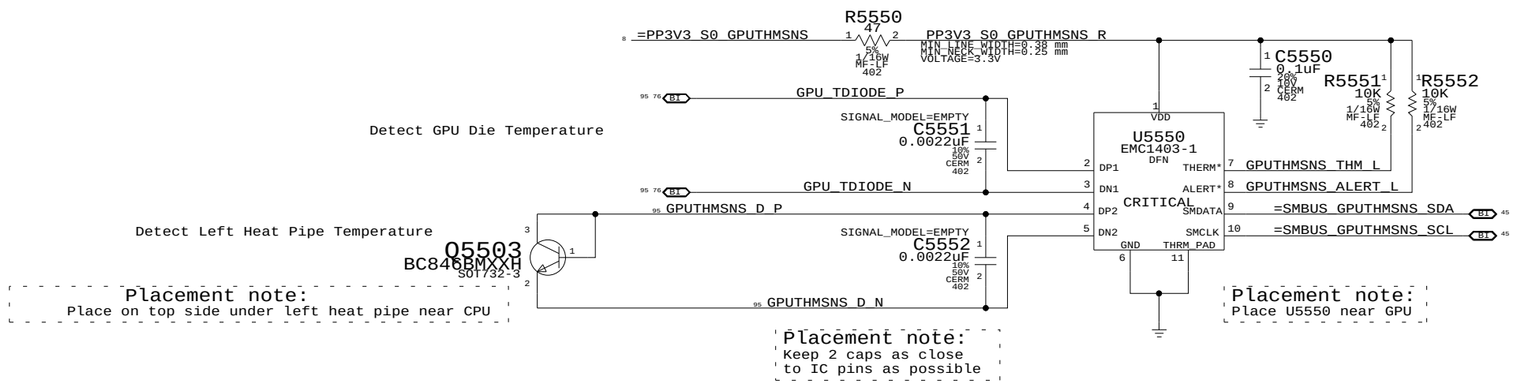


MCP Proximity/MCP Die/Right Heat Pipe



Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



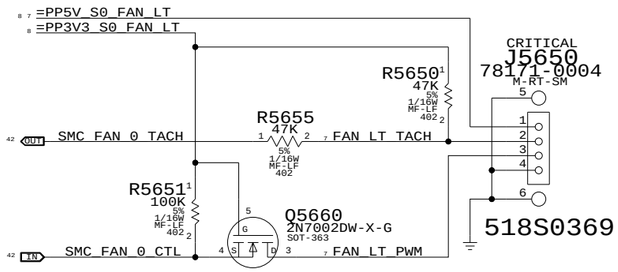
Thermal Sensors

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

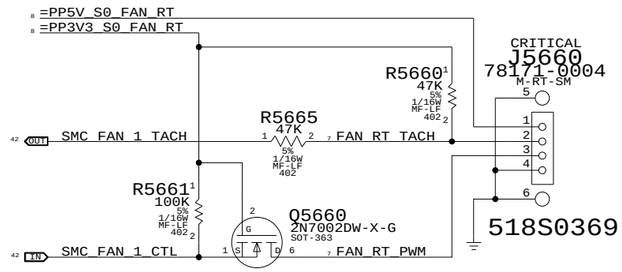
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 48 OF 96	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

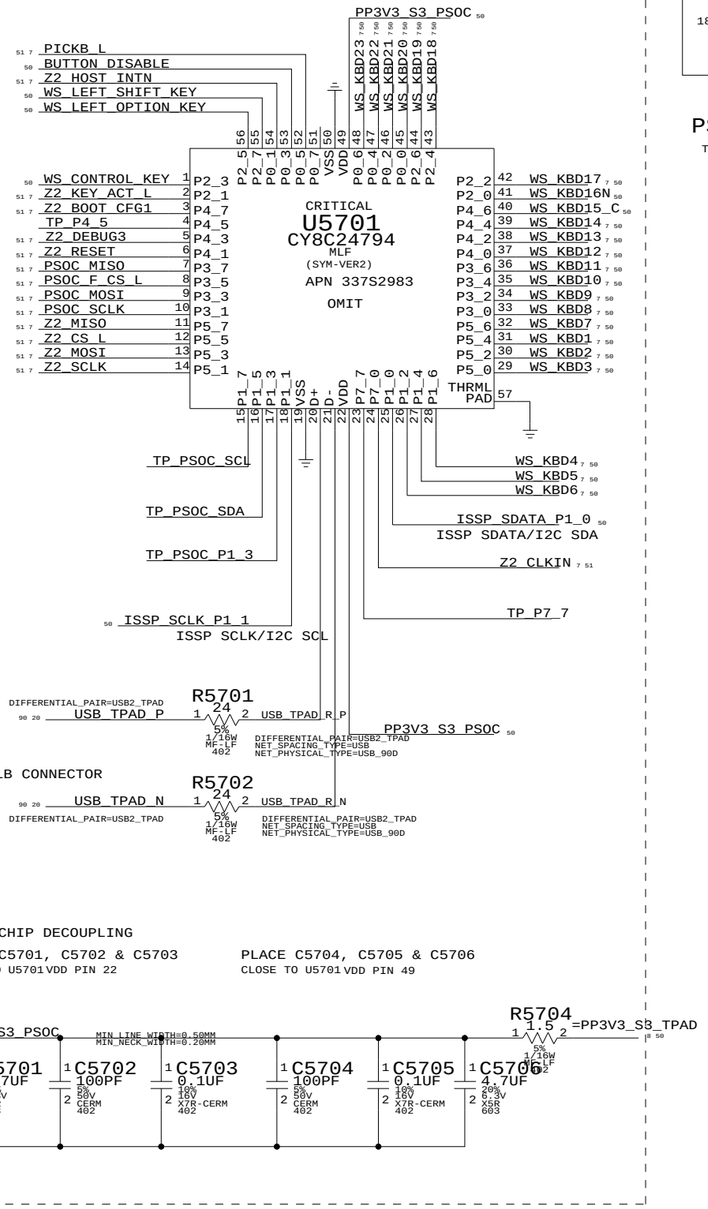
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	49	96

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

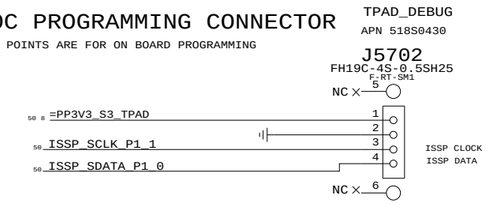
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

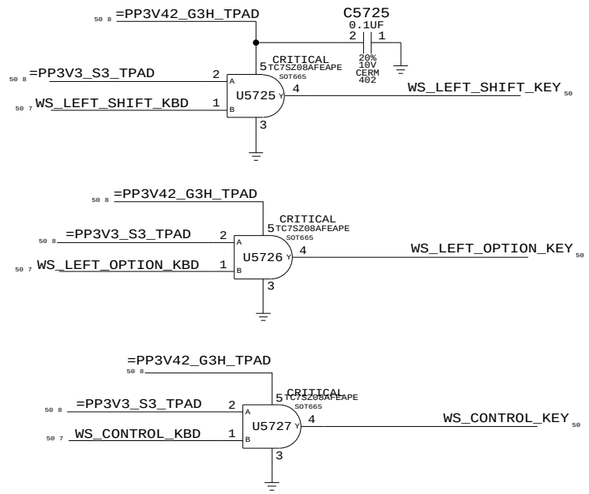
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

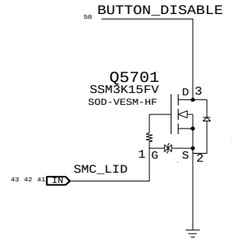
TEST POINTS ARE FOR ON BOARD PROGRAMMING



ISOLATION CIRCUIT



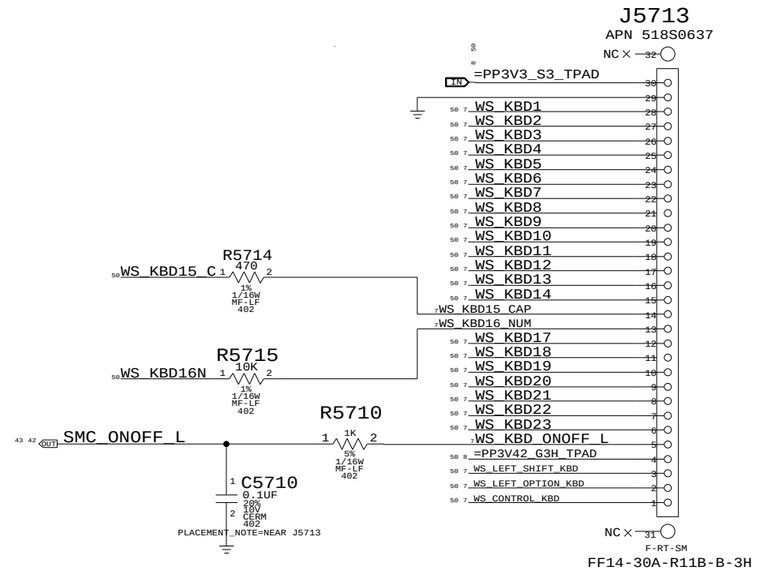
TPAD BUTTONS DISABLE



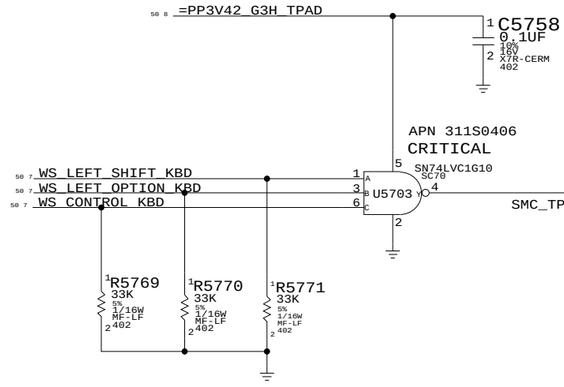
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



WELLSPRING 1

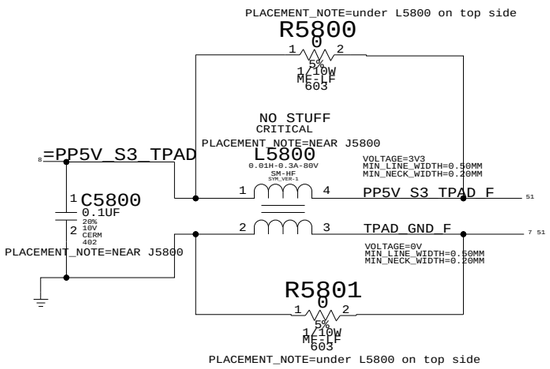
SYNC_MASTER=AMASON_M98 SYNC_DATE=06/18/2008

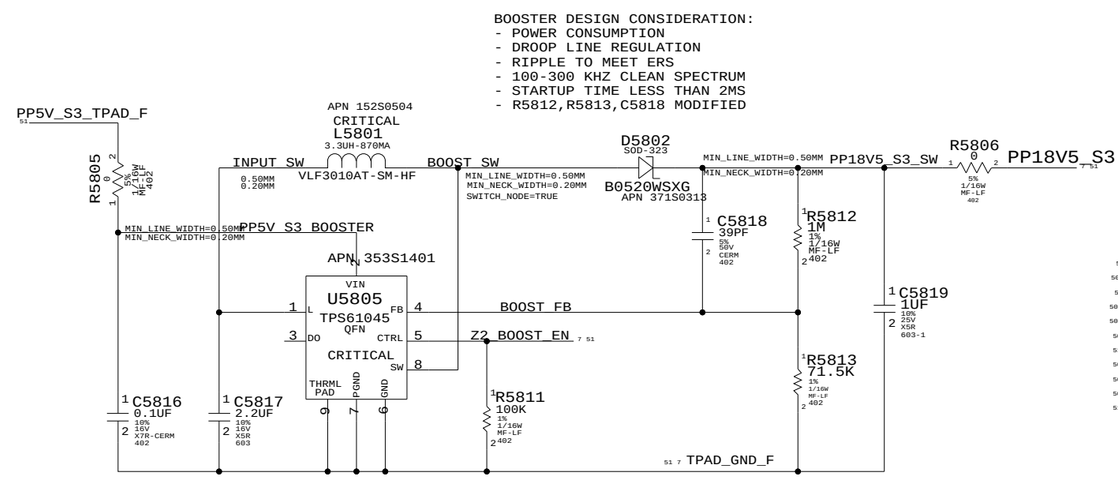
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 50 OF 96	

BOOSTER +18.5VDC FOR SENSORS

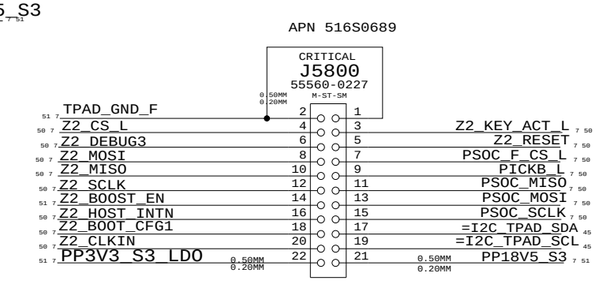
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

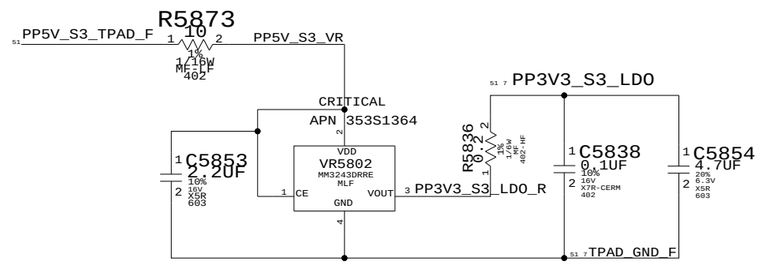




3V3 LDO FOR IPD

IPD FLEX CONNECTOR

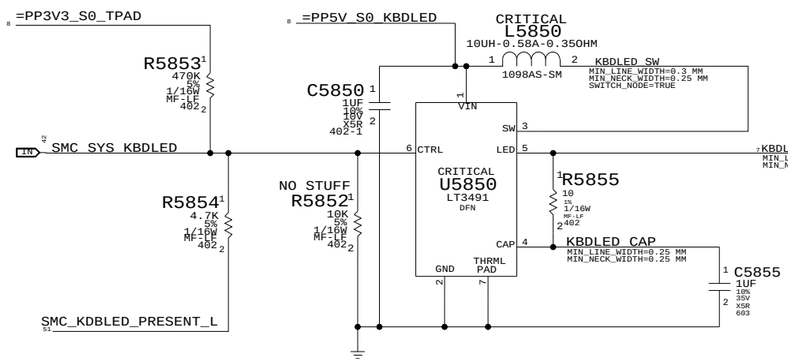


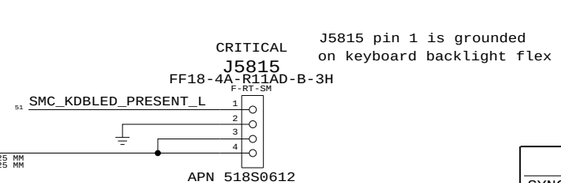


Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





KBD BACKLIGHT CONNECTOR

WELLSPRING 2

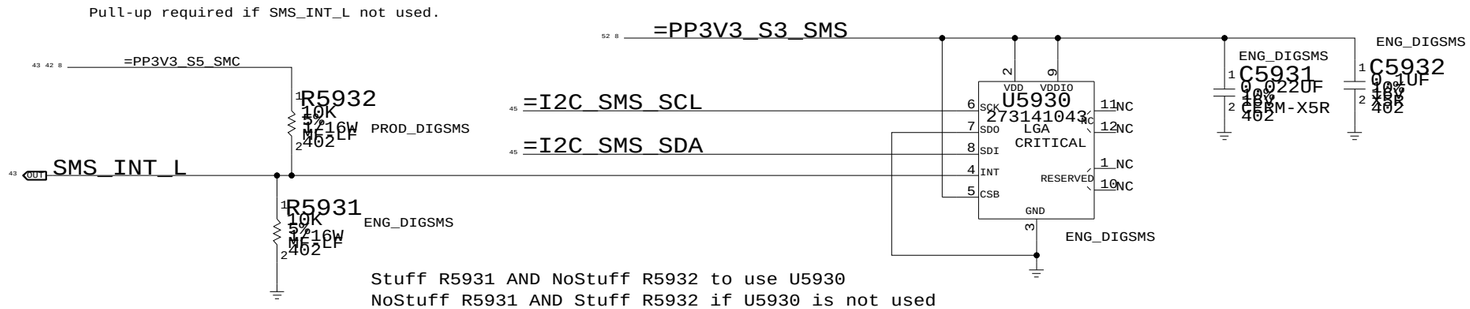
SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008

APPLE INC.

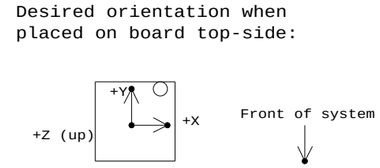
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE: NONE SHT: 51 OF 96

Digital SMS



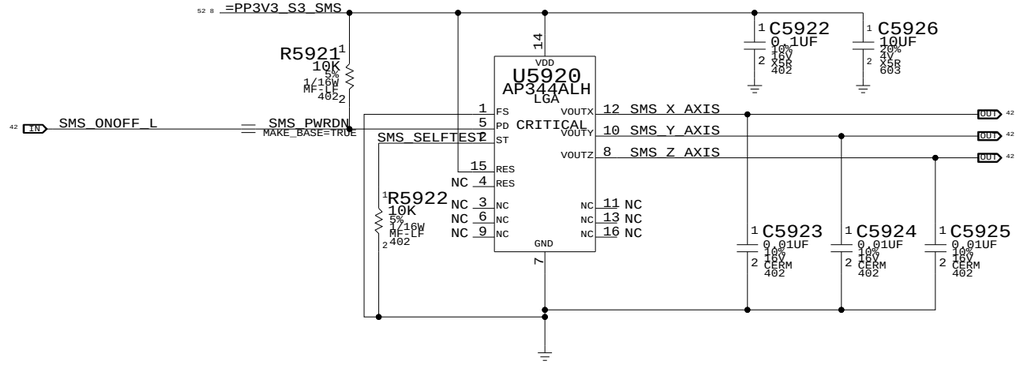
Stuff R5931 AND NoStuff R5932 to use U5930
NoStuff R5931 AND Stuff R5932 if U5930 is not used

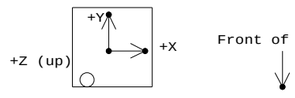


Circle indicates pin 1 location when placed
in correct orientation

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC





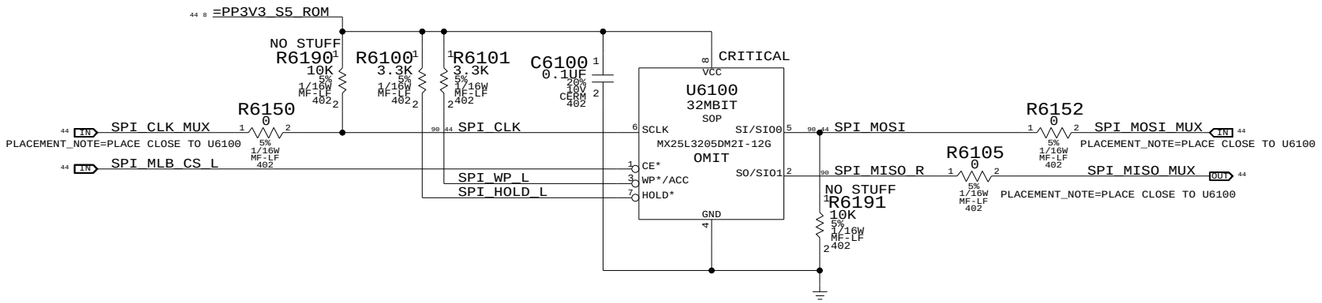
Circle indicates pin 1 location when placed
in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 52 OF 96	



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

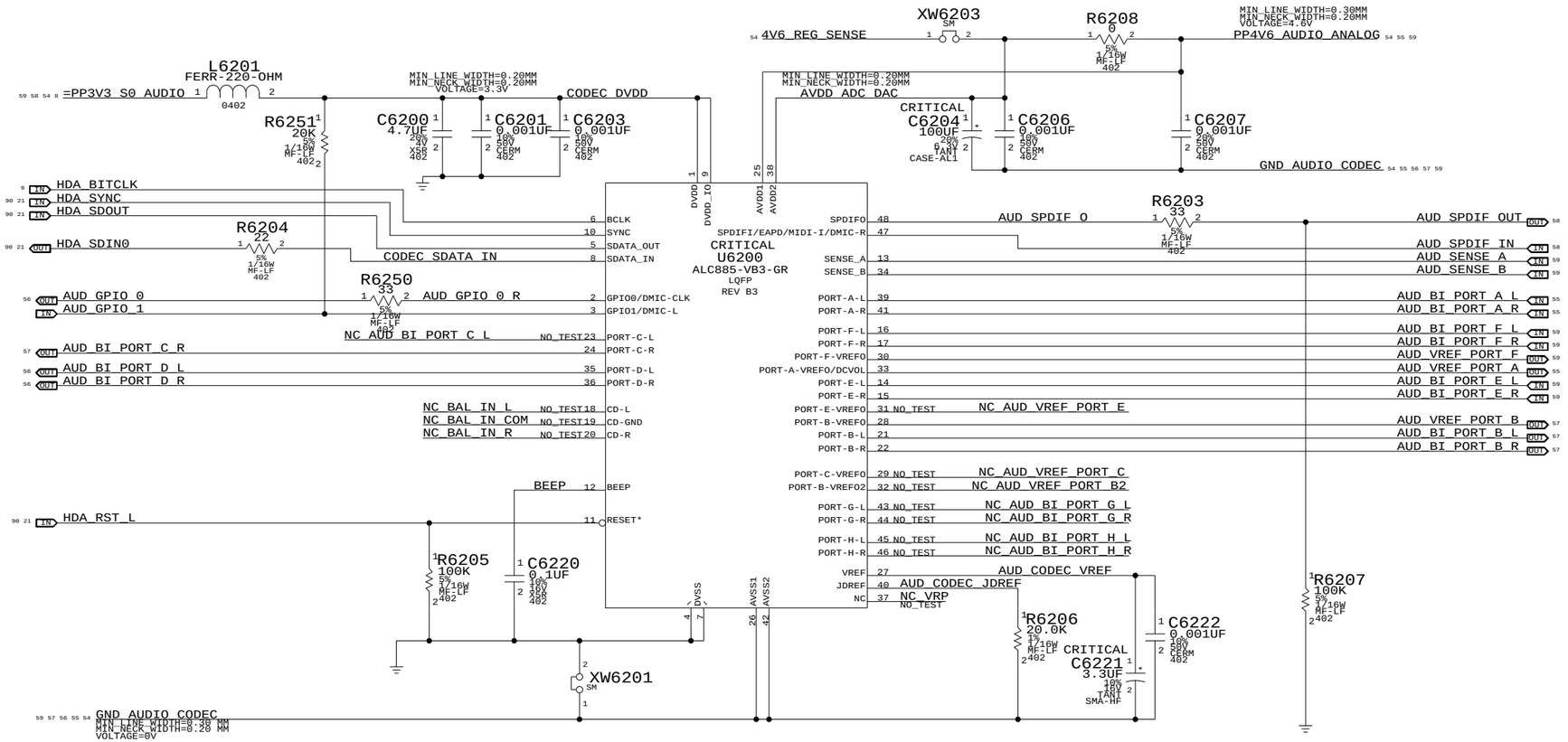
SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 53 OF 96	

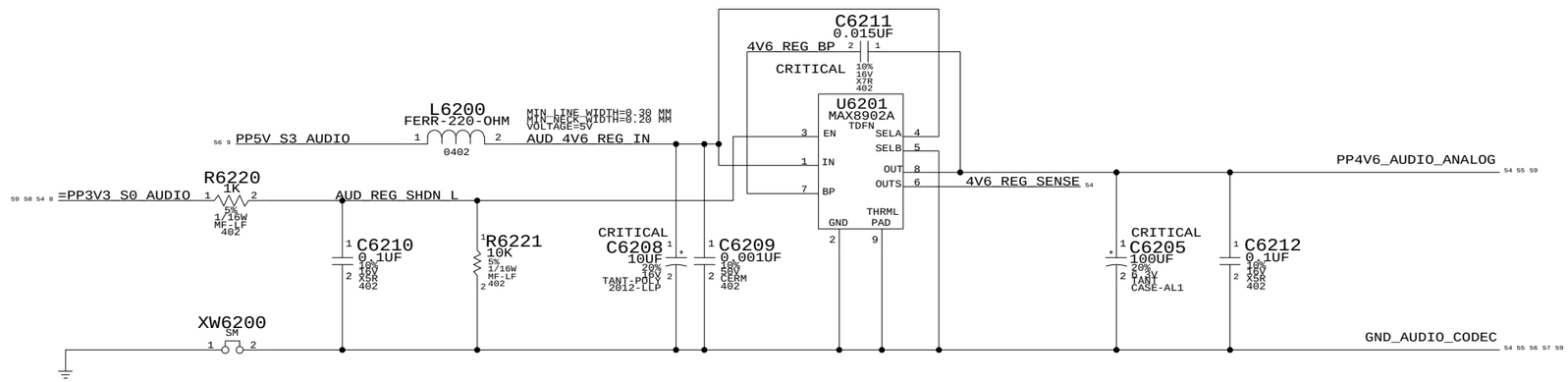
AUDIO CODEC

APPLE P/N 353S1527



AUDIO 4.6V REGULATOR

APPLE P/N 353S1897



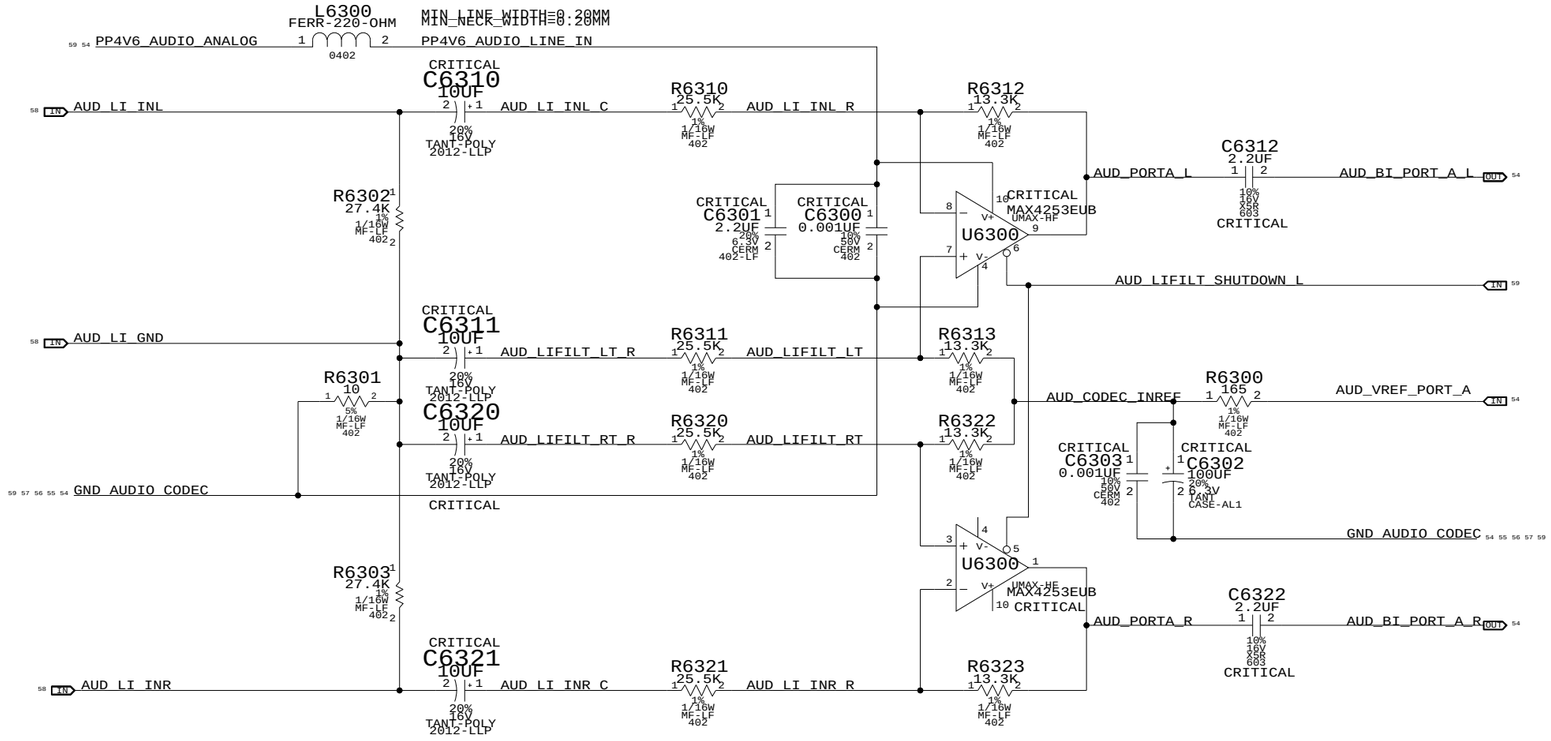
AUDIO:CODEC

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 54 OF 96	

Pseudo-Diff Line-In Filter
GAIN = -5.4DB AV = 0.52
FC = 1.8 HZ



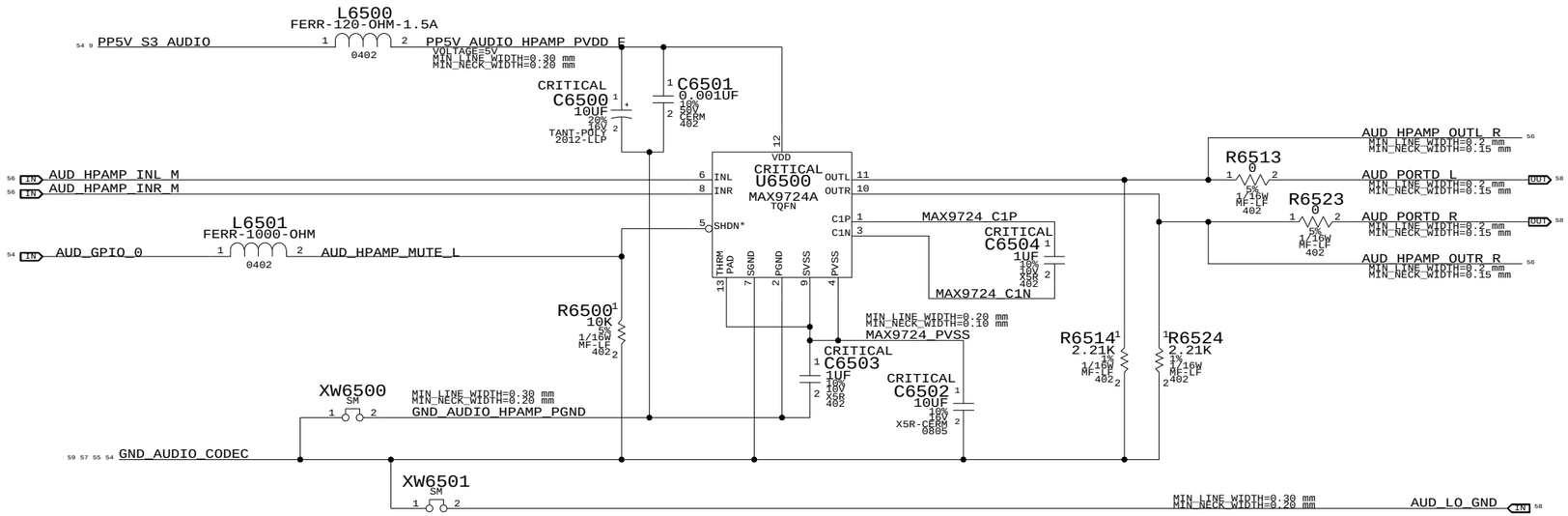
AUDIO: LINE IN

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

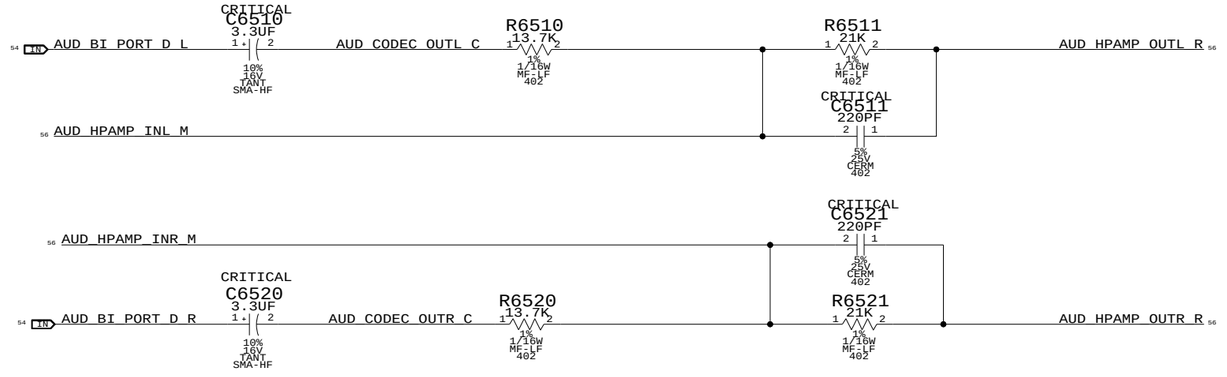
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 55 OF 96	

Headphone Amplifier (MAX9724A)
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ
VOLTAGE GAIN:1.53



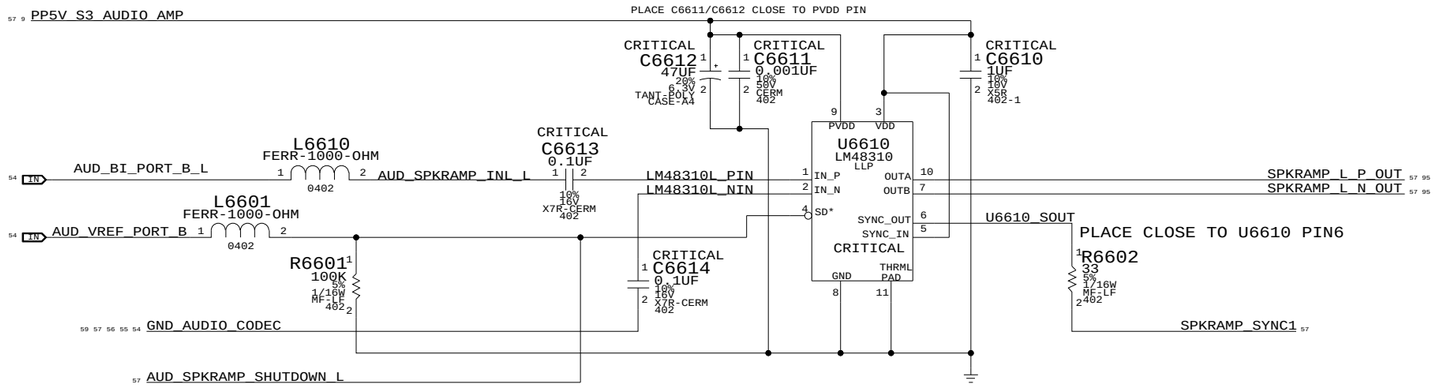
AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

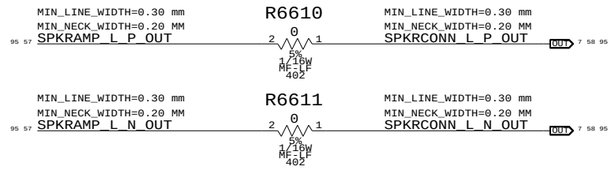
APPLE INC.

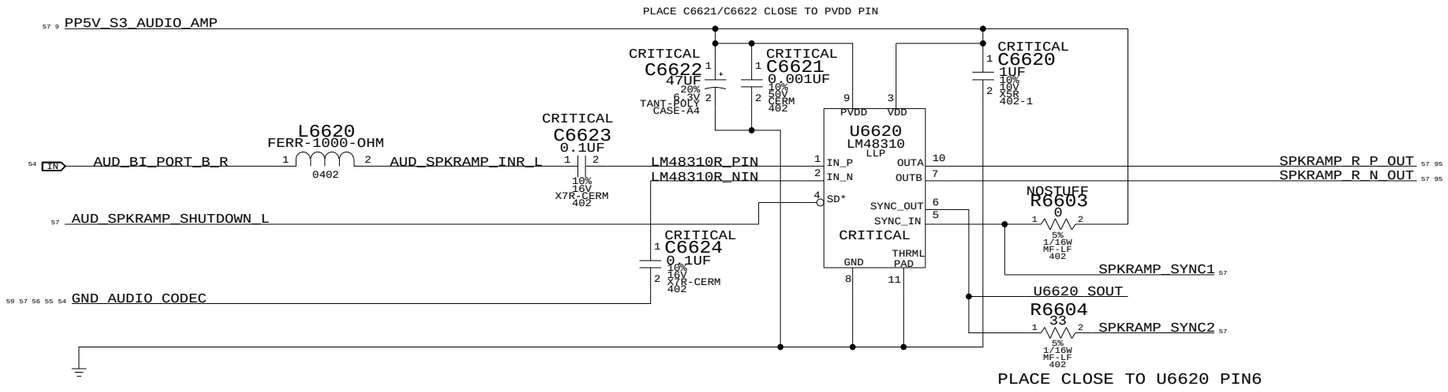
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 56 OF 96	

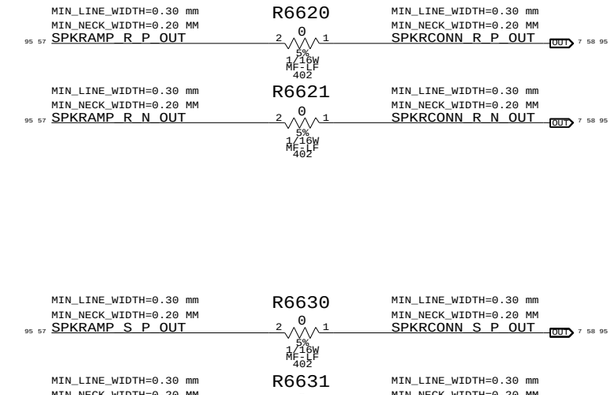
2X MONO SPEAKER AMPLIFIERS (LM48310)
APN: 353S1901
GAIN = 12DB
79Hz < FC (L&R) < 93Hz
53Hz < FC (SUB) < 62Hz

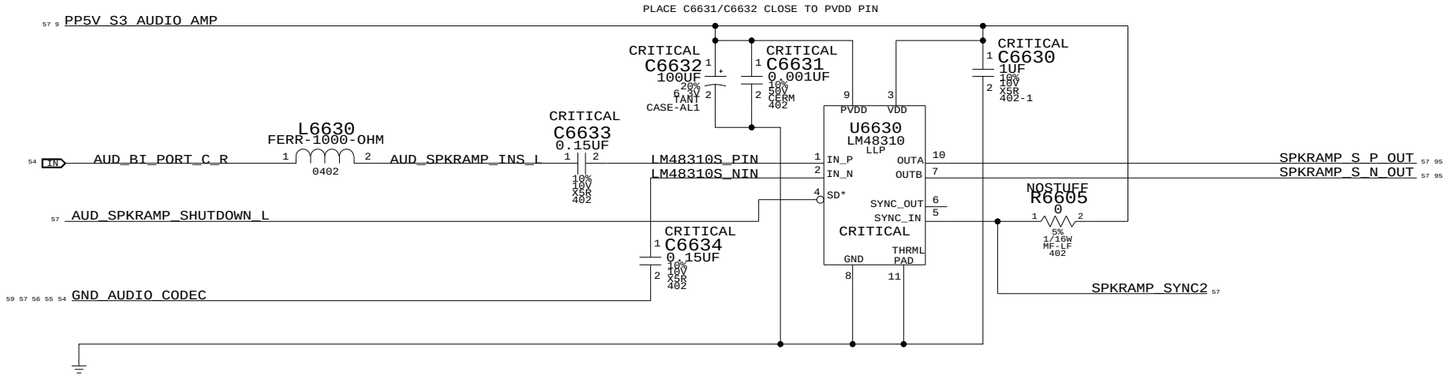


SPEAKER CHECKPOINTS









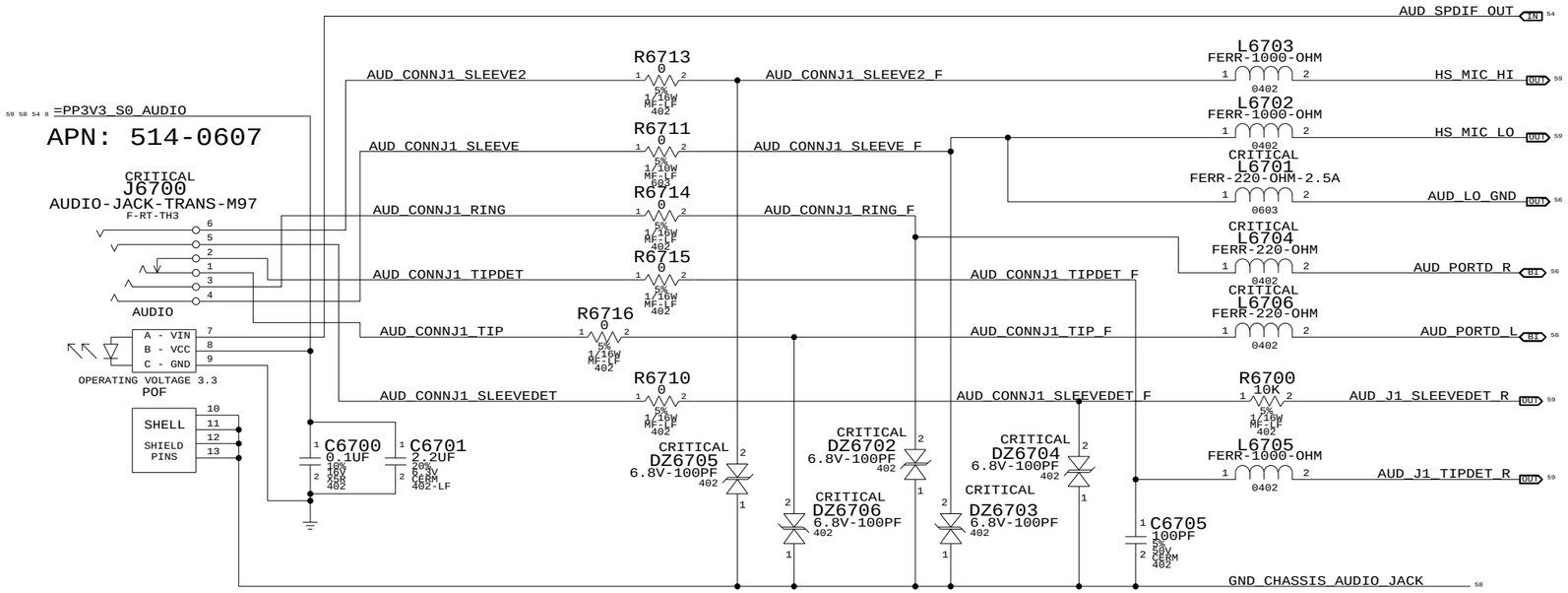
AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 57 OF 96	

AUDIO JACK 1 LO/HP JACK, SPDIF TX



MIC CONNECTOR

APN: 518S0520

CRITICAL
J6780
78171-0003
M-RT-SM

BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI

SPEAKER CONNECTOR

APN: 518S0519

CRITICAL
J6781
78171-0002
M-RT-SM

SPKRCONN_L_P_OUT
SPKRCONN_L_N_OUT

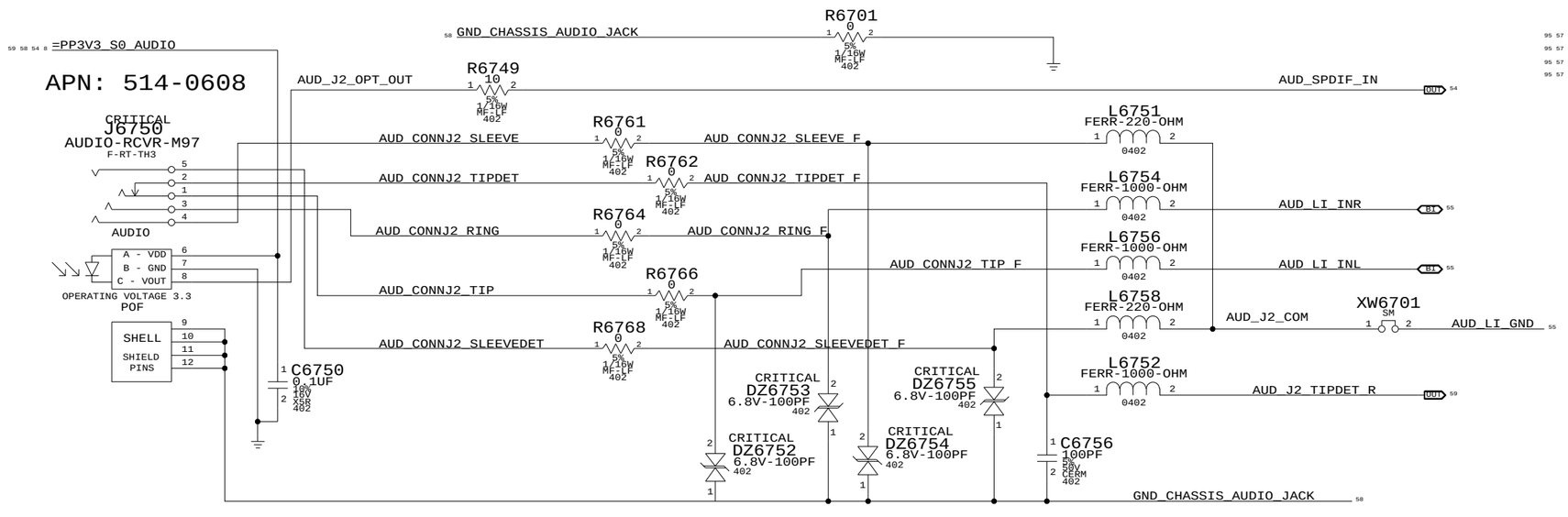
CRITICAL
J6782
78171-0004
M-RT-SM

APN: 518S0521

SPKRCONN_S_P_OUT
SPKRCONN_S_N_OUT
SPKRCONN_R_P_OUT
SPKRCONN_R_N_OUT

NOSTUFF CRITICAL C6781 100PF 5% 50V CERM 402
NOSTUFF CRITICAL C6783 100PF 5% 50V CERM 402
NOSTUFF CRITICAL C6782 100PF 5% 50V CERM 402
NOSTUFF CRITICAL C6784 100PF 5% 50V CERM 402

RETURN FOR HF NOISE



AUDIO JACK 2 LINE IN JACK, SPDIF RX

AUDIO: JACKS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	58	96

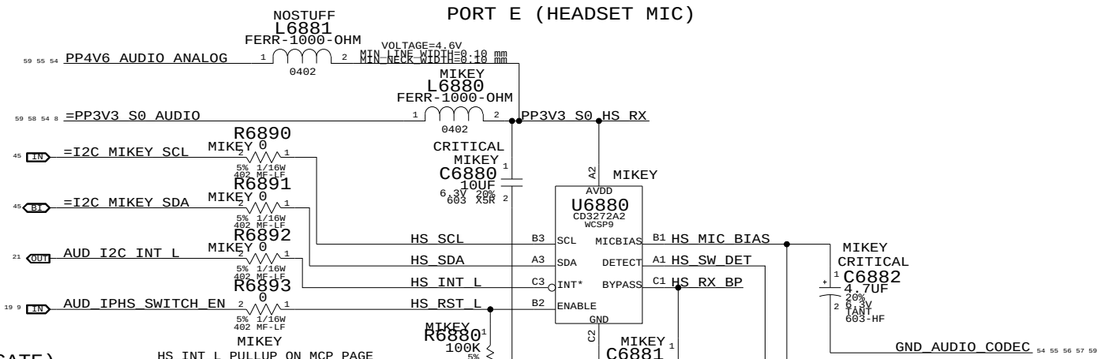
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SATELLITES	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SUB	0X0F (15)	0X05 (05)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)		0X1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

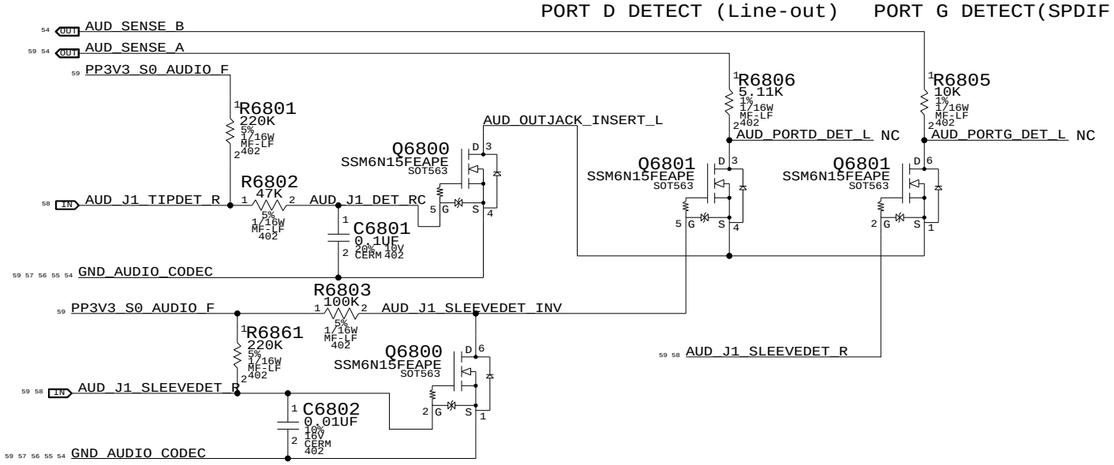
FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0X1F (SPDIF IN)	N/A	N/A
BUILT-IN MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT E (HEADSET MIC)



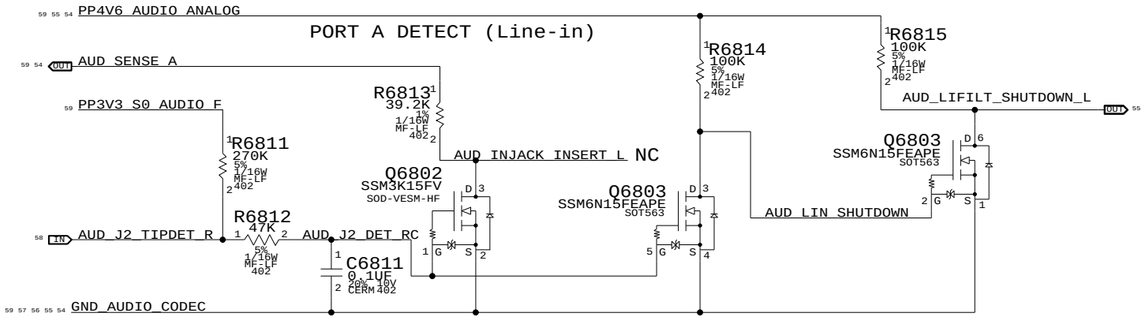
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6883	MIKEY
131S1513	1	15PF 5% 0402 CAPACITOR	C6884	MIKEY
132S0045	1	100PF 10% 0402 CAPACITOR	C6885	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6883	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6884	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6885	NOMIKEY

PORT D DETECT (Line-out) PORT G DETECT(SPDIF DELEGATE)

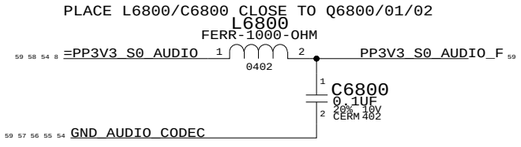


LINE_IN AMP SHUTDOWN CONTROL

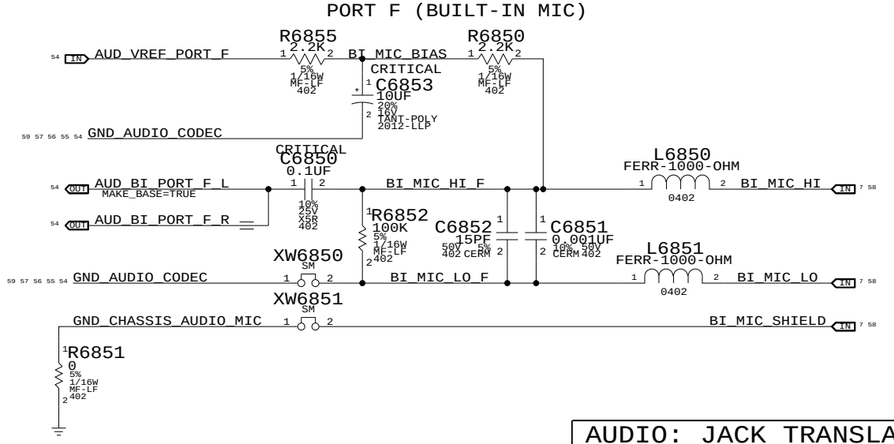
PORT A DETECT (Line-in)



PLACE L6800/C6800 CLOSE TO Q6800/01/02



PORT F (BUILT-IN MIC)



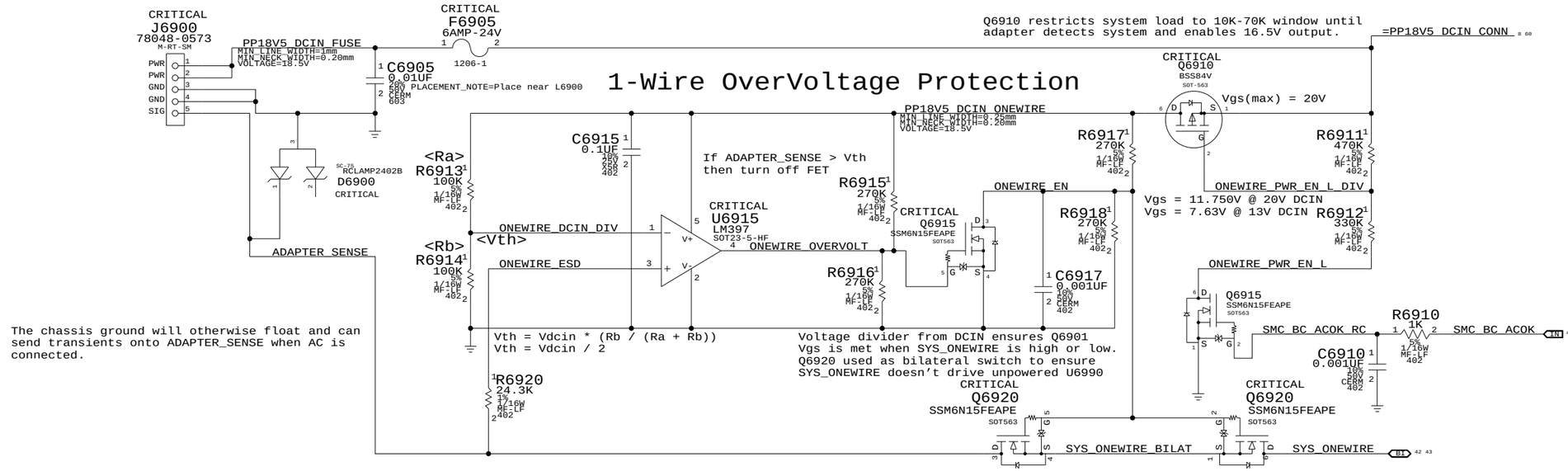
AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

APPLE INC.

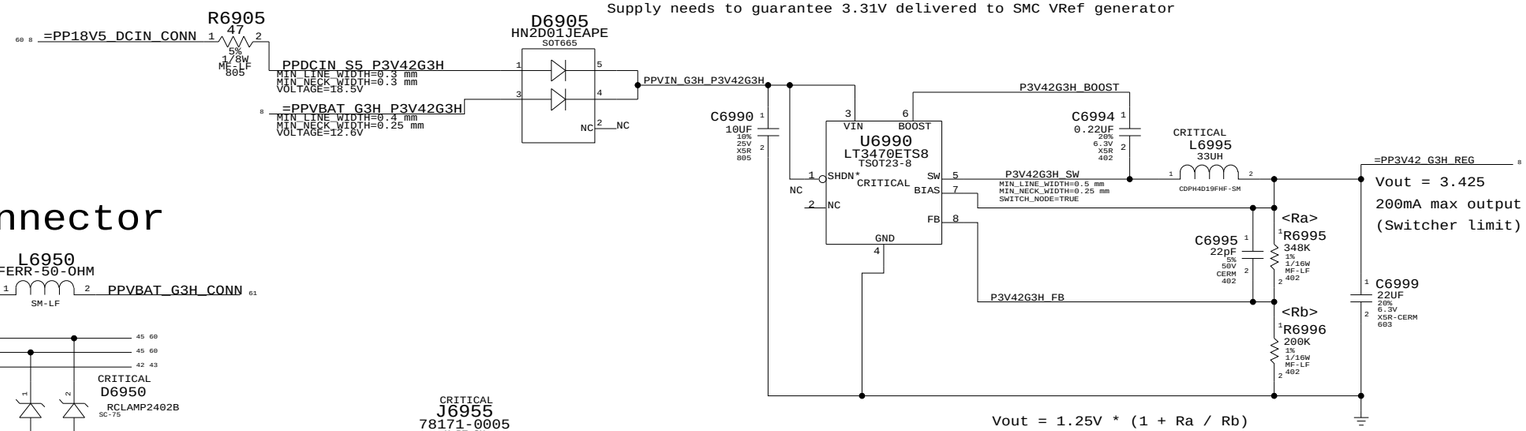
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 59 OF 96	

MagSafe DC Power Jack

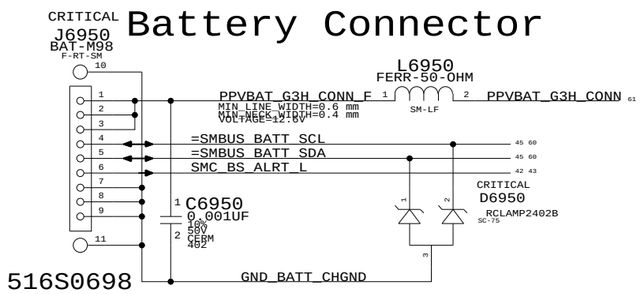


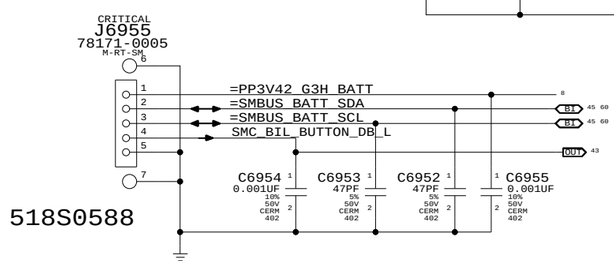
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Battery Connector



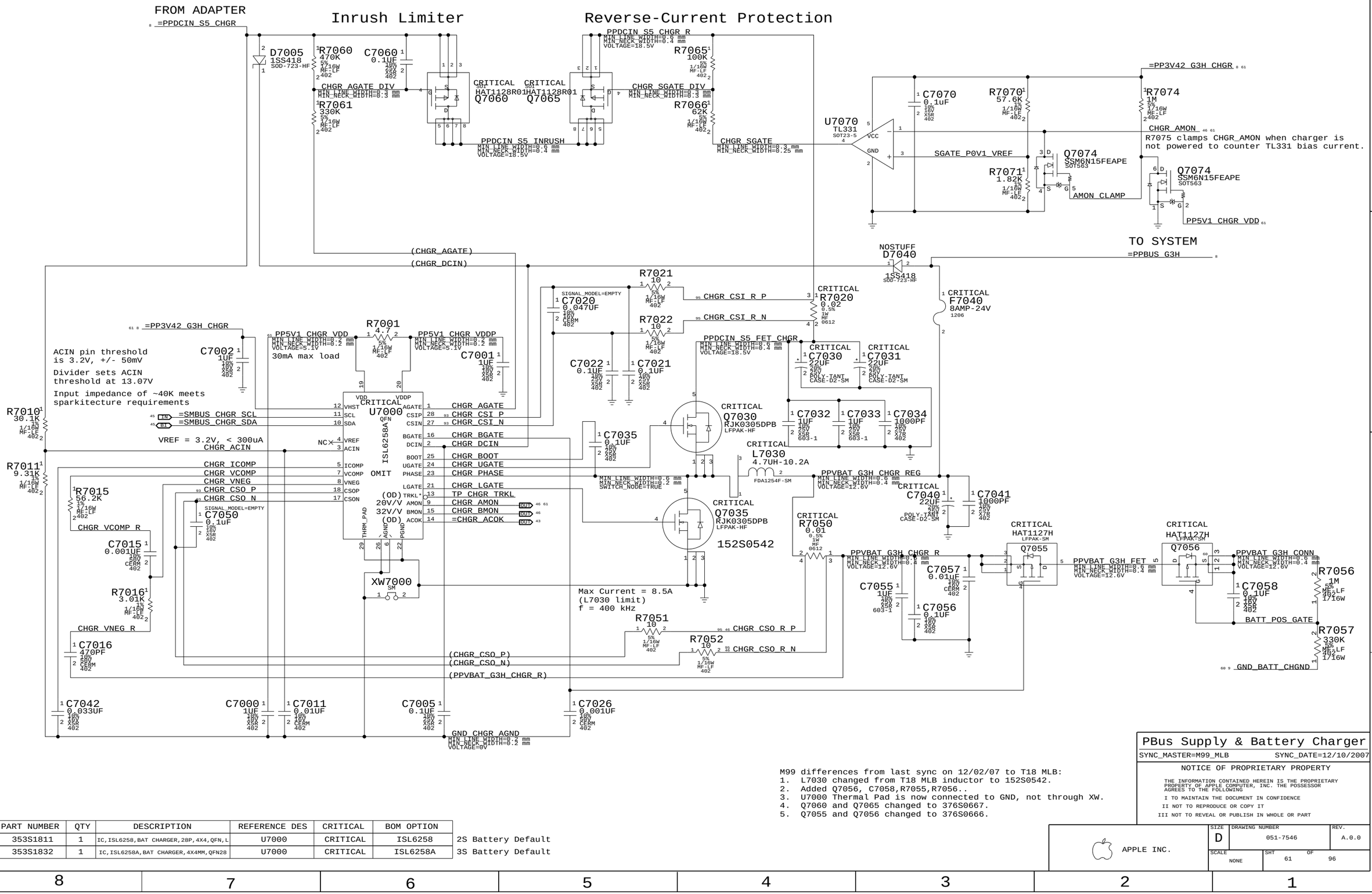


DC-In & Battery Connectors

SYNC_MASTER=T18_MLB SYNC_DATE=12/06/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 60 OF 96	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1811	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger

SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT: 61	OF: 96

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

Place R7131 Between L7100,L7101 and CPU

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

IMVP_VR_ON	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM	IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM						
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM						
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM						
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM						

IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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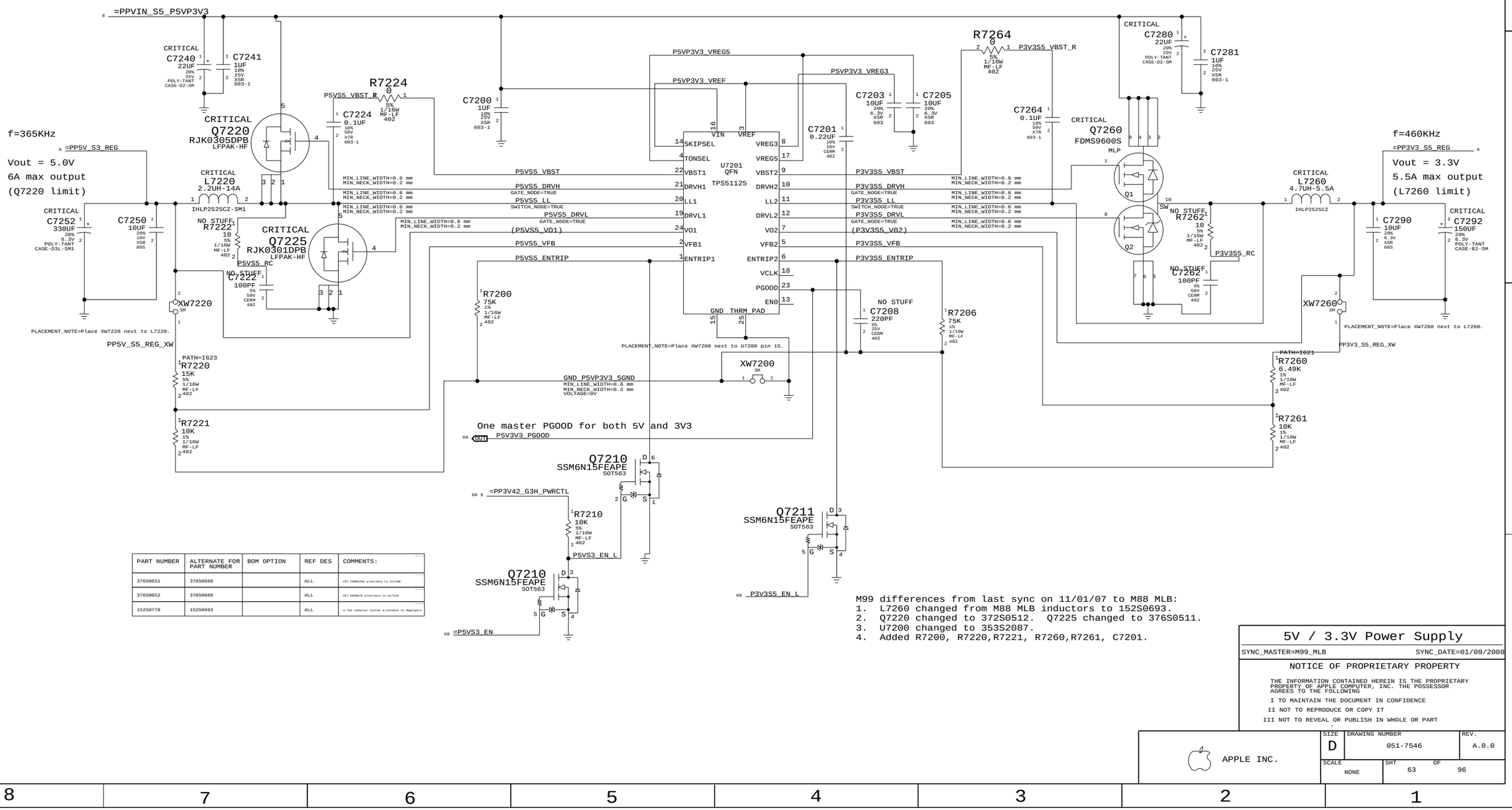
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 62 OF 96	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0651	376S0668		ALL	FET FDMS8676S alternate to Si7540
376S0652	376S0669		ALL	FET FDMS8670 alternate to Si7510
152S0778	152S0693		ALL	4.7uH inductor Cyntec alternate to MagLayers

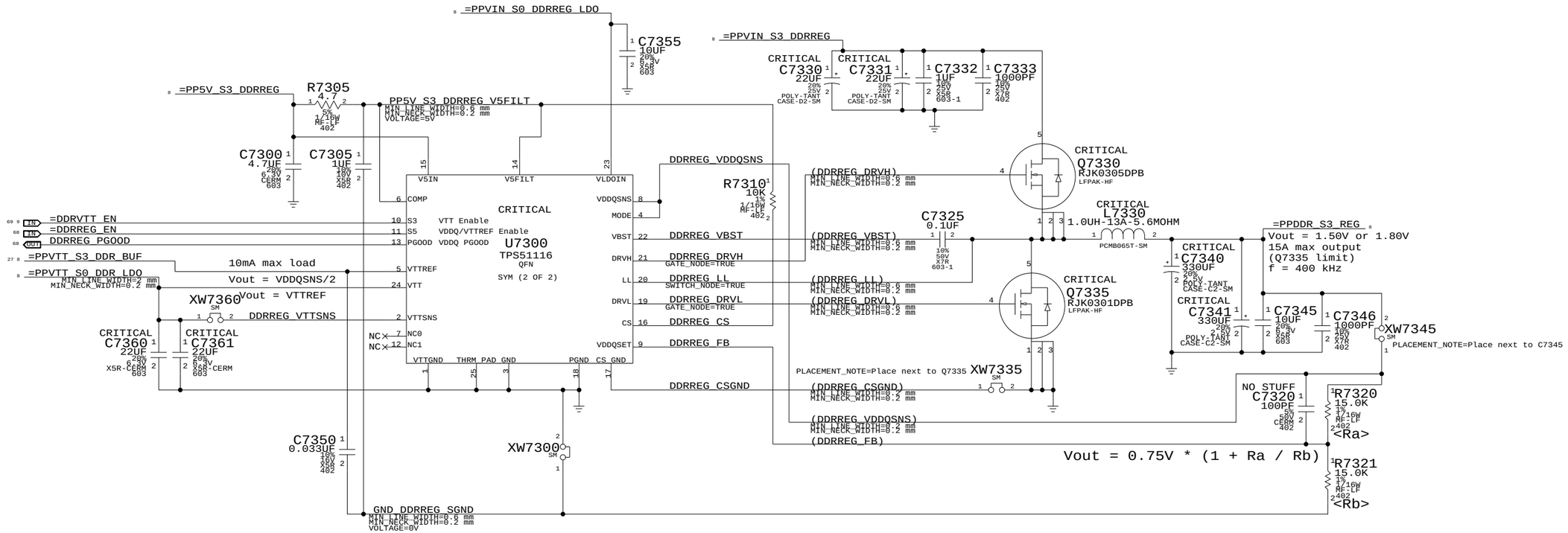
M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220,R7221, R7260,R7261, C7201.

5V / 3.3V Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=01/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 63 OF 96	



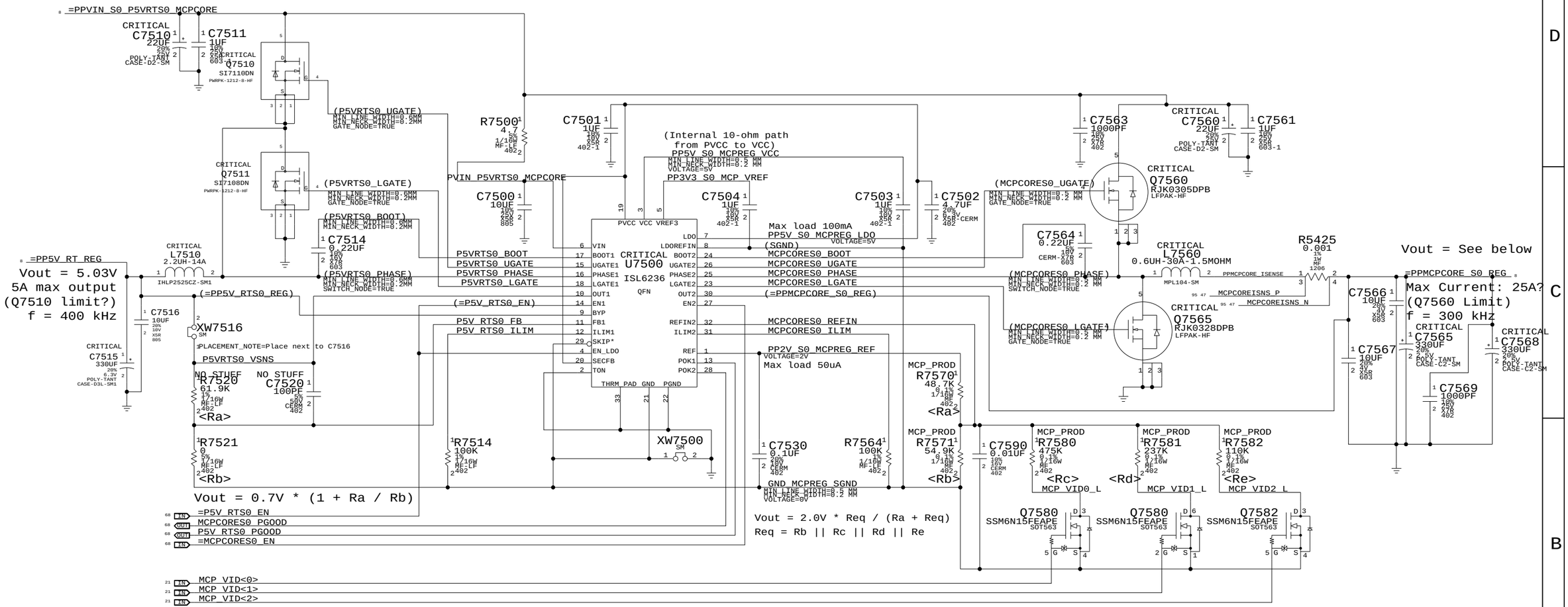
1.5V DDR3 Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/13/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	64	96



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

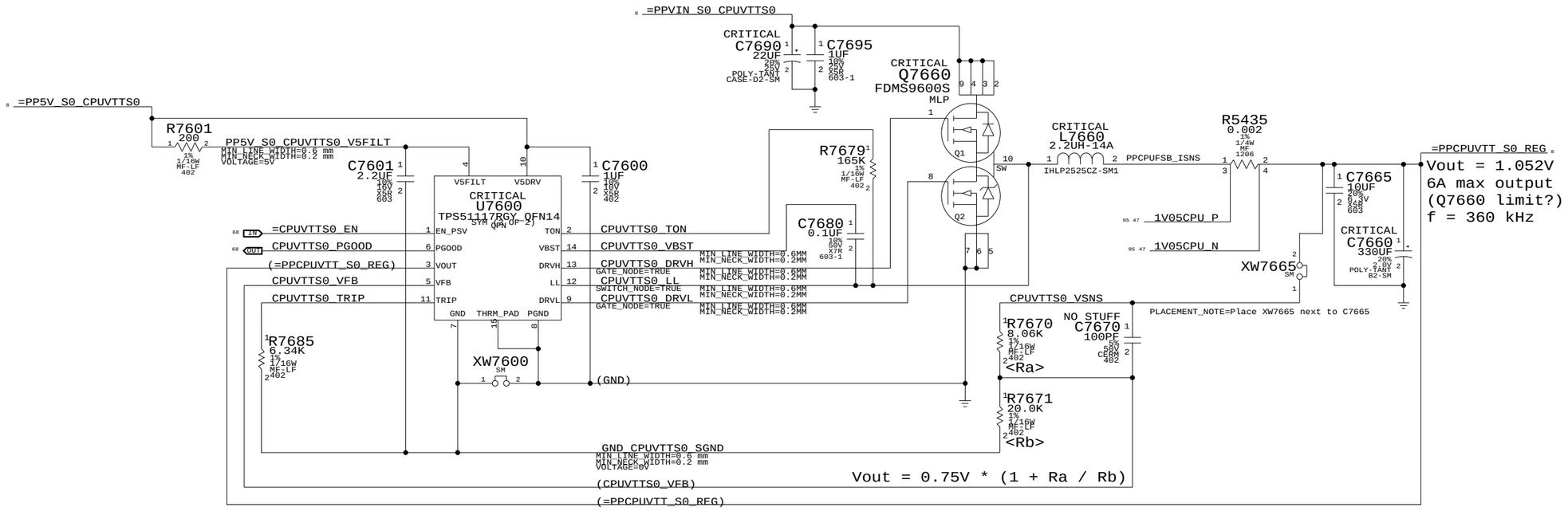
VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

1.05V / MCP Core Regulator

SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 65 OF 96	



M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

CPU VTT Power Supply

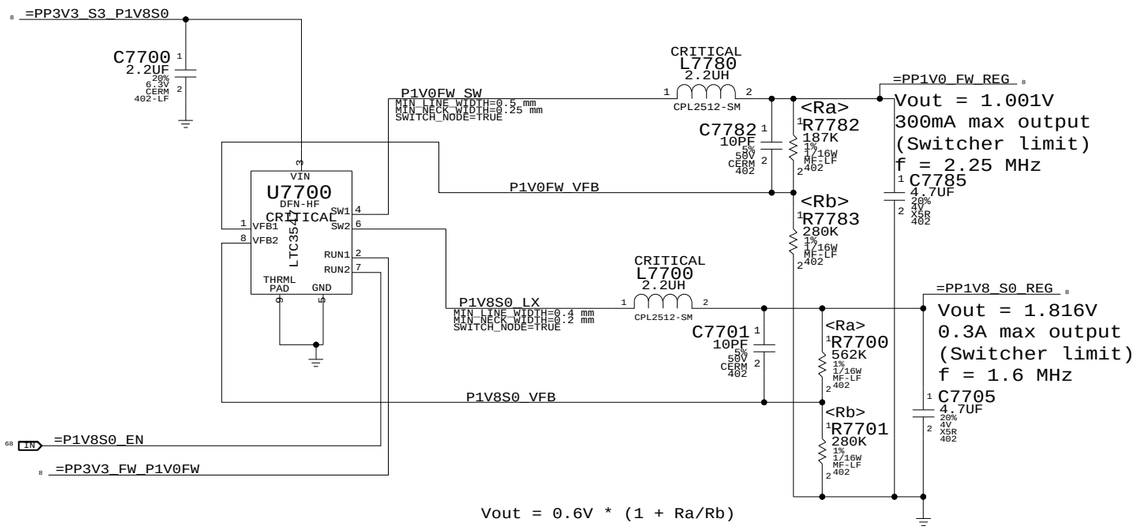
SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 66 OF 96	

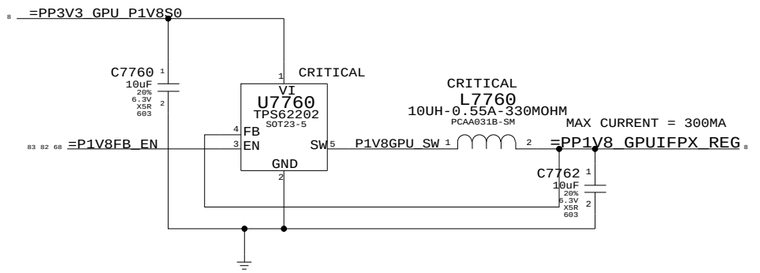
1.8V S0 Switcher / 1.0VFW SWITCHER

S5 power required for output discharge feature

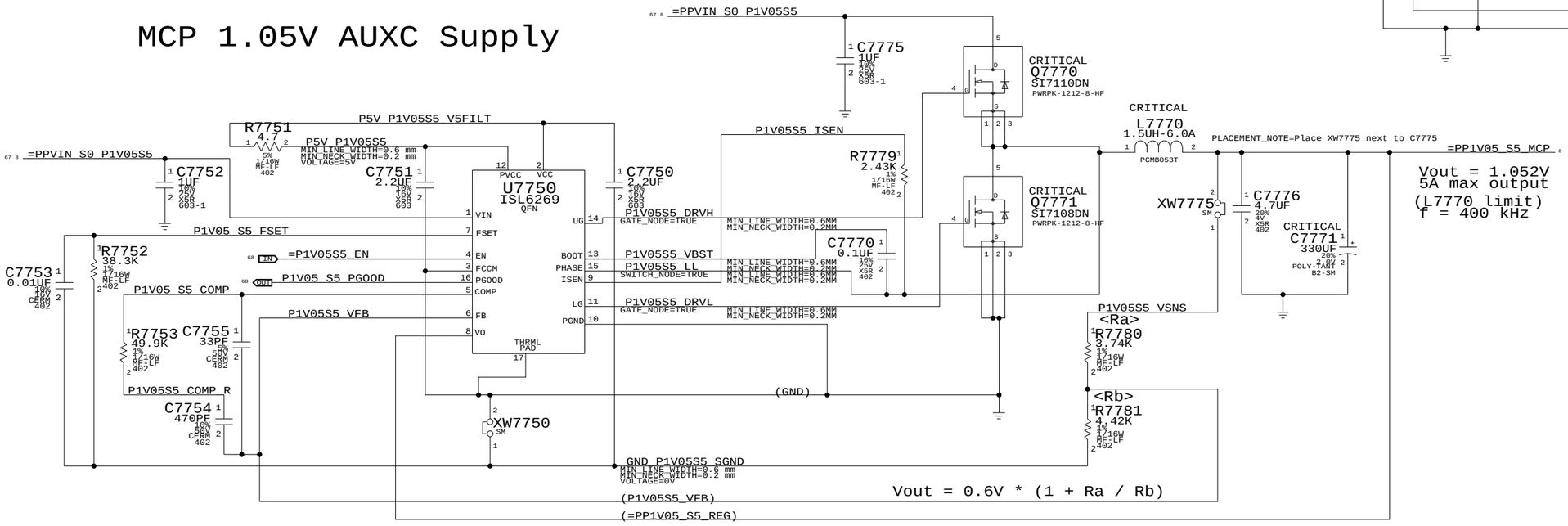


1.8V S0 Switcher

INPUT RAIL IS 3.3V S0



MCP 1.05V AUXC Supply



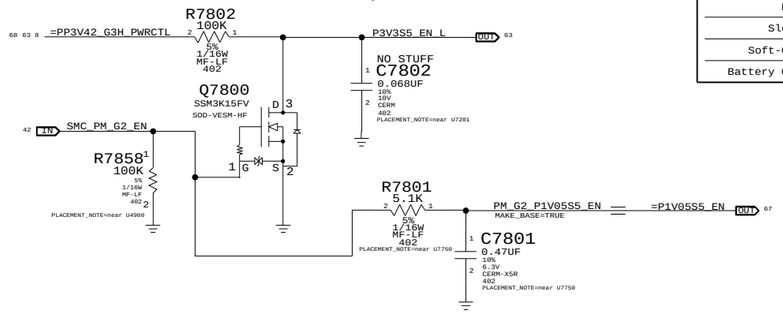
Misc Power Supplies

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

APPLE INC.

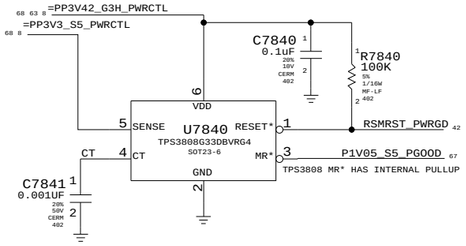
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 67 OF 96	

3.3V 1,05V S5 ENABLE

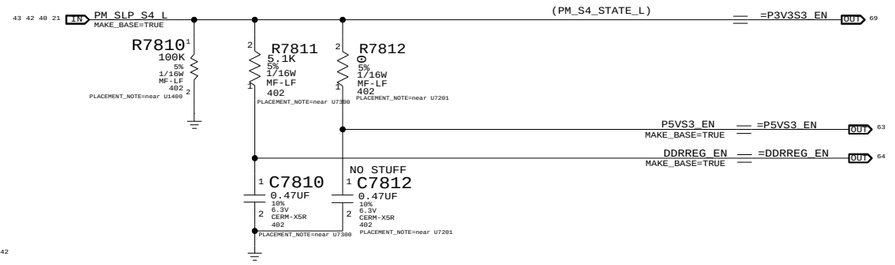


State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

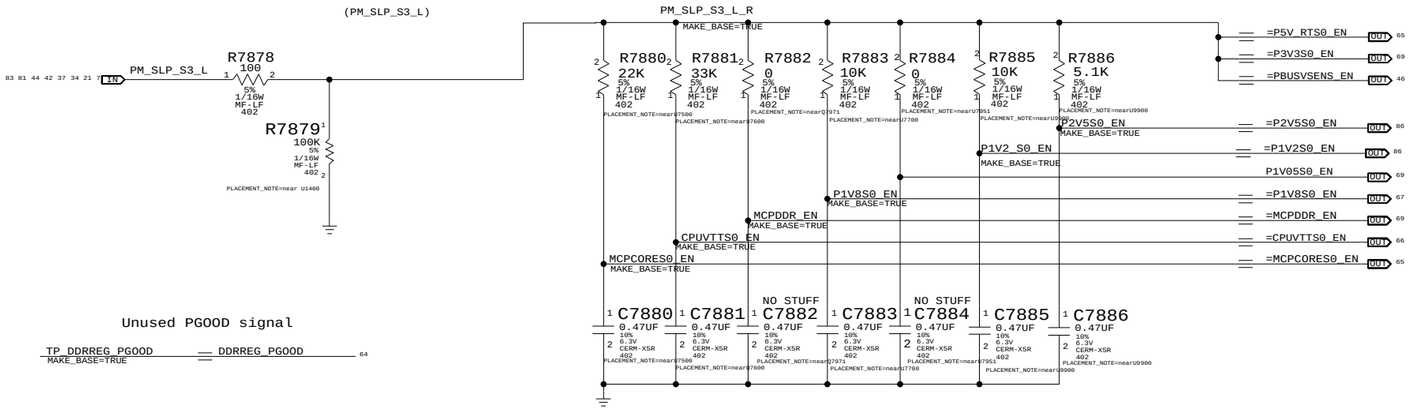
S5 rail PWRGD



3.3V,5V S3 ENABLE

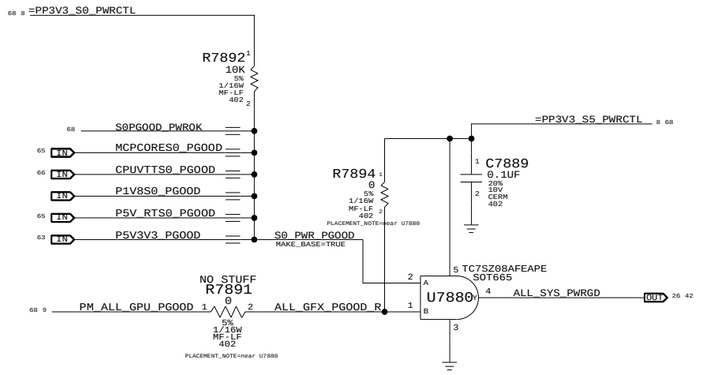


S0 ENABLE



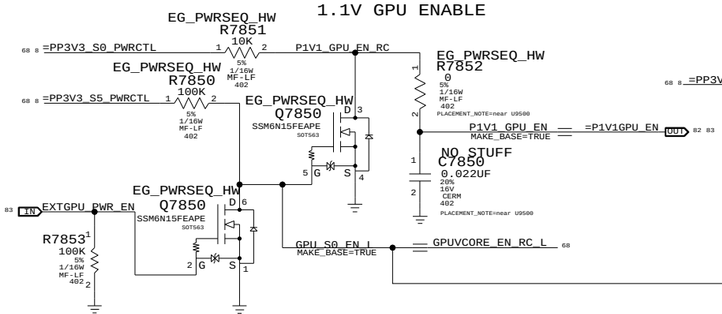
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

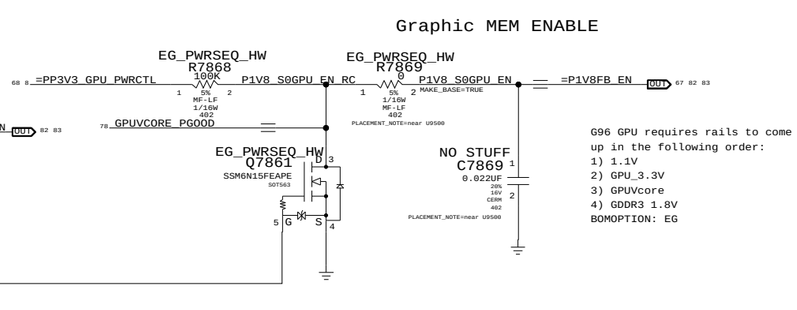


Unused PGOOD signal

1.1V GPU ENABLE

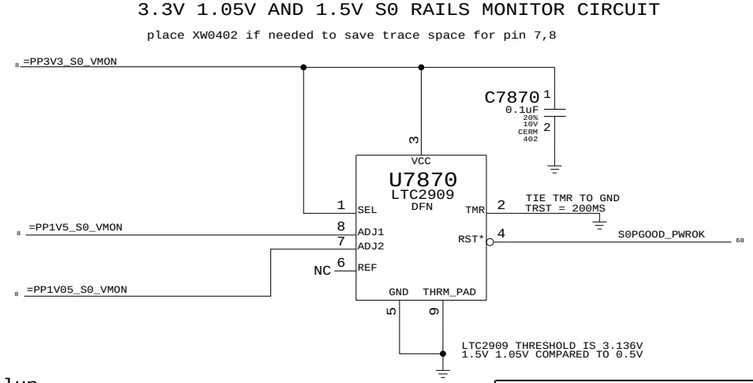


Graphic MEM ENABLE

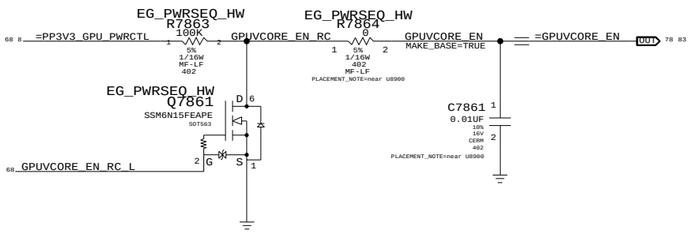


3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

place XW0402 if needed to save trace space for pin 7,8



GPUVCORE ENABLE



EXT GPU PWRGD Pullup

Power Control

SYNC_MASTER=PWRSQNC SYNC_DATE=05/12/2008

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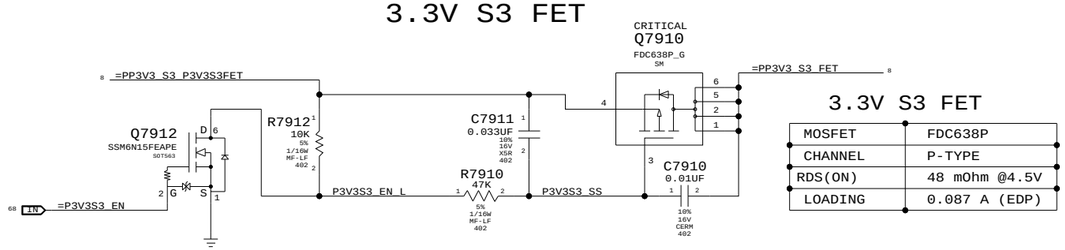
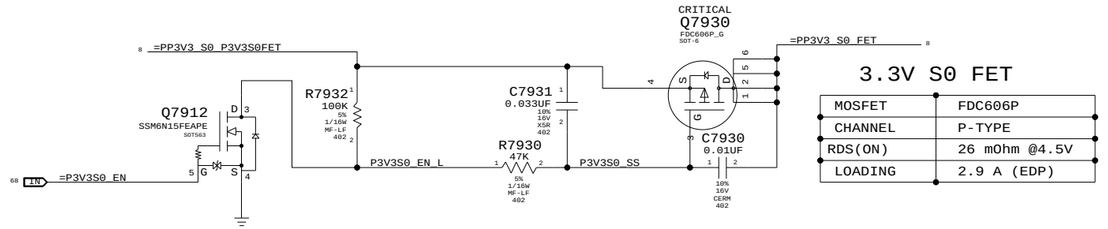
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 68 OF 96	

3.3V S3 FET



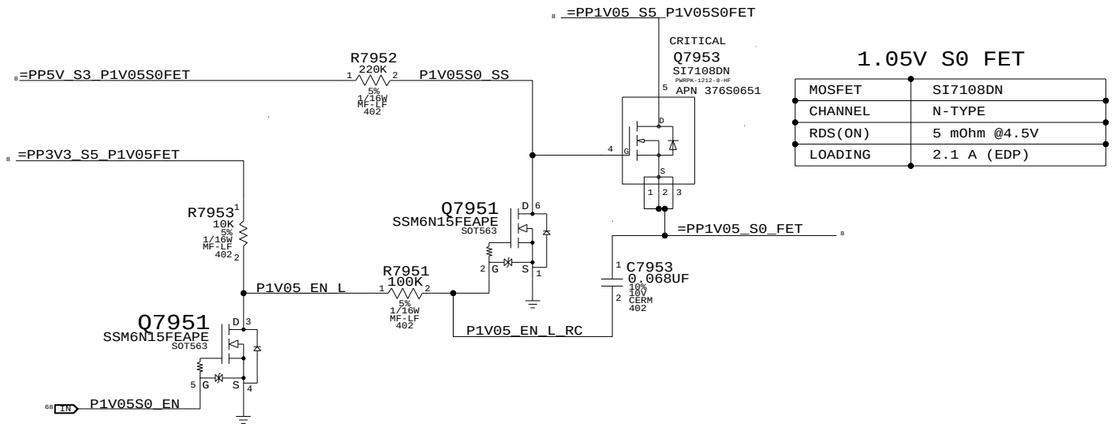
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



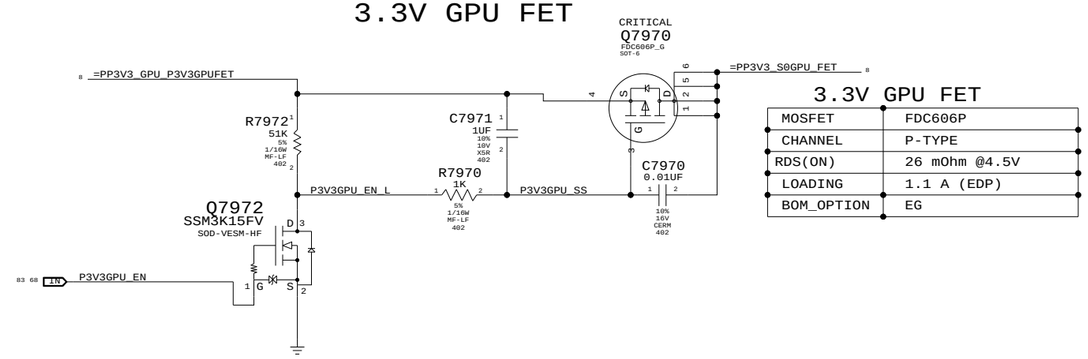
3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET



1.05V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	2.1 A (EDP)

3.3V GPU FET

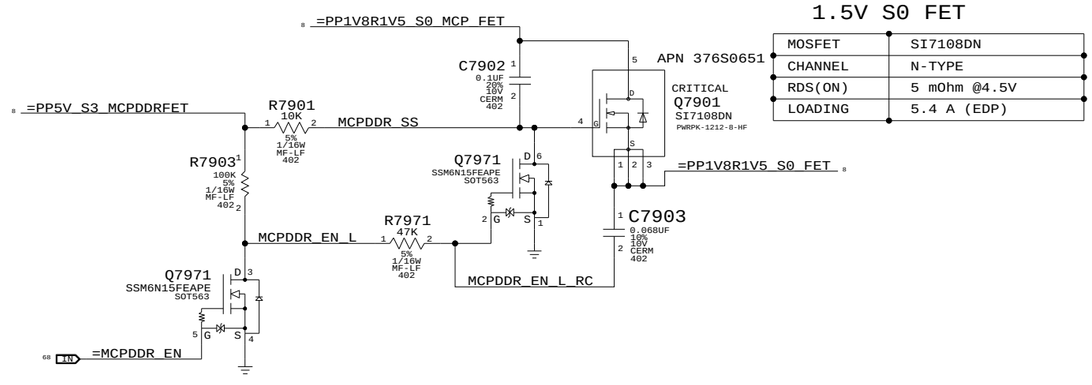


3.3V GPU FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

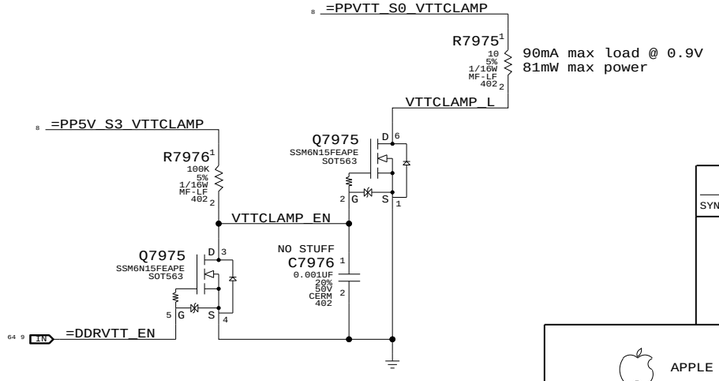
MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

1.5V S0 FET



1.5V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)



Power FETs	
SYNC_MASTER=PWRSQNC	SYNC_DATE=05/12/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
	SCALE: NONE	SHT 69 OF 96	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V1_GPU_PEX_PLLXVDD
=PP1V1_GPU_PEX_IOVDDQ
=PP1V1_GPU_PEX_IOVDD

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA

L8015 10NH-600MA 0603

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

OMIT

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H32	PEX_IOVDD1	AK16
M7	PEX_IOVDD2	AK17
P6	PEX_IOVDD3	AK21
P7	PEX_IOVDD4	AK24
R7	PEX_IOVDD5	AK27
U7		
V6		
AB7		
AD6	PEX_IOVDDQ1	AG11
AF6	PEX_IOVDDQ2	AG12
AG6	PEX_IOVDDQ3	AG13
AJ5	PEX_IOVDDQ4	AG15
D35	PEX_IOVDDQ5	AG16
AK15	PEX_IOVDDQ6	AG17
AL7	PEX_IOVDDQ7	AG18
E7	PEX_IOVDDQ8	AG22
E35	PEX_IOVDDQ9	AG23
F7	PEX_IOVDDQ10	AG24
A2	PEX_IOVDDQ11	AG25
	PEX_IOVDDQ12	AG26
	PEX_IOVDDQ13	AJ14
	PEX_IOVDDQ14	AJ15
	PEX_IOVDDQ15	AJ19
	PEX_IOVDDQ16	AJ21
	PEX_IOVDDQ17	AJ22
	PEX_IOVDDQ18	AJ24
	PEX_IOVDDQ19	AJ25
	PEX_IOVDDQ20	AJ27
	PEX_IOVDDQ21	AK18
	PEX_IOVDDQ22	AK20
	PEX_IOVDDQ23	AK23
	PEX_IOVDDQ24	AK26
	PEX_IOVDDQ25	AL16
	PEX_PLLVDD	AG14
	VDD_SENSE	AD20
	GND_SENSE	AD19

NC

GPU_VDD_SENSE 78
GPU_GND_SENSE 78

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0	
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PEG_CLK100M_N			AR17	PEX_REFCLK*	
GPU_RESET_L	R8020 0 5% 1/10W MF-LF 402	GPU_RESET_R_L	AM16	PEX_RST*	
		TP_PEX_CLKREQ_L	AR13	PEX_CLKREQ*	

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PEX_TX0	AL17	PEG_D2R_C_P<0>	C8055 0.1uF
PEX_TX0*	AM17	PEG_D2R_C_N<0>	C8056 0.1uF
PEX_TX1	AM18	PEG_D2R_C_P<1>	C8057 0.1uF
PEX_TX1*	AM19	PEG_D2R_C_N<1>	C8058 0.1uF
PEX_TX2	AL19	PEG_D2R_C_P<2>	C8059 0.1uF
PEX_TX2*	AK19	PEG_D2R_C_N<2>	C8060 0.1uF
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PEX_TX5*	AK22	PEG_D2R_C_N<5>	C8066 0.1uF
PEX_TX6	AL23	PEG_D2R_C_P<6>	C8067 0.1uF
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PEX_TX7	AM24	PEG_D2R_C_P<7>	C8069 0.1uF
PEX_TX7*	AM25	PEG_D2R_C_N<7>	C8070 0.1uF
PEX_TX8	AL25	PEG_D2R_C_P<8>	C8071 0.1uF
PEX_TX8*	AK25	PEG_D2R_C_N<8>	C8072 0.1uF
PEX_TX9	AL26	PEG_D2R_C_P<9>	C8073 0.1uF
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PEX_TX11*	AK28	PEG_D2R_C_N<11>	C8078 0.1uF
PEX_TX12	AK29	PEG_D2R_C_P<12>	C8079 0.1uF
PEX_TX12*	AL29	PEG_D2R_C_N<12>	C8080 0.1uF
PEX_TX13	AM29	PEG_D2R_C_P<13>	C8081 0.1uF
PEX_TX13*	AM30	PEG_D2R_C_N<13>	C8082 0.1uF
PEX_TX14	AM31	PEG_D2R_C_P<14>	C8083 0.1uF
PEX_TX14*	AM32	PEG_D2R_C_N<14>	C8084 0.1uF
PEX_TX15	AN32	PEG_D2R_C_P<15>	C8085 0.1uF
PEX_TX15*	AP32	PEG_D2R_C_N<15>	C8086 0.1uF
PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK_P	R8060 200 1% 1/10W MF-LF 402
PEX_TSTCLK_OUT*	AJ18	PEX_TSTCLK_N	
PEX_TERMP	AG21	PEX_TERMP_PD	R8050 2.49K 1% 1/10W MF-LF 402
PEX_RFU1	AG19	NC	
PEX_RFU2	AG20	NC	

NV G96 PCI-E

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

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D	051-7546	A.0.0
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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402
C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402
C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT

U8000
NB9P-GS
BGA
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L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17

VDD

V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20

VDD

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B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16

GND

V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30

GND

=PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

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B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16

FBVDDQ

J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31

FBVDDQ

NV G96 Core/FB Power

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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NB9P-GS
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R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402
R8250 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402
L8200 FERR-220-OHM 0402
C8200 1UF 10% 6.3V CERM 402
C8201 0.1UF 20% 10V CERM 402
C8202 0.1UF 20% 10V CERM 402
C8290 0.1UF 20% 10V CERM 402
C8291 0.1UF 20% 10V CERM 402
R8291 33.2 1% 1/16W MF-LF 402
R8292 40.2 1% 1/16W MF-LF 402
R8293 60.4 1% 1/16W MF-LF 402
R8294 60.4 1% 1/16W MF-LF 402
R8295 1.07K 1% 1/16W MF-LF 402
R8290 48.7 1% 1/16W MF-LF 402
R8296 2.49K 1% 1/16W MF-LF 402
R8297 1.02K 1% 1/16W MF-LF 402
C8296 0.1UF 10% 16V X5R 402

PP1V1_GPU_FBPLLAVDD_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V

PLACEMENT_NOTE=Place close to U8000.
PLACEMENT_NOTE=Place close to U8000.
PLACEMENT_NOTE=Place close to U8000.

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

NO STUFF
Q8295
SSM6N15FEAPE
SOT563

NO STUFF

NV G96 Frame Buffer I/F

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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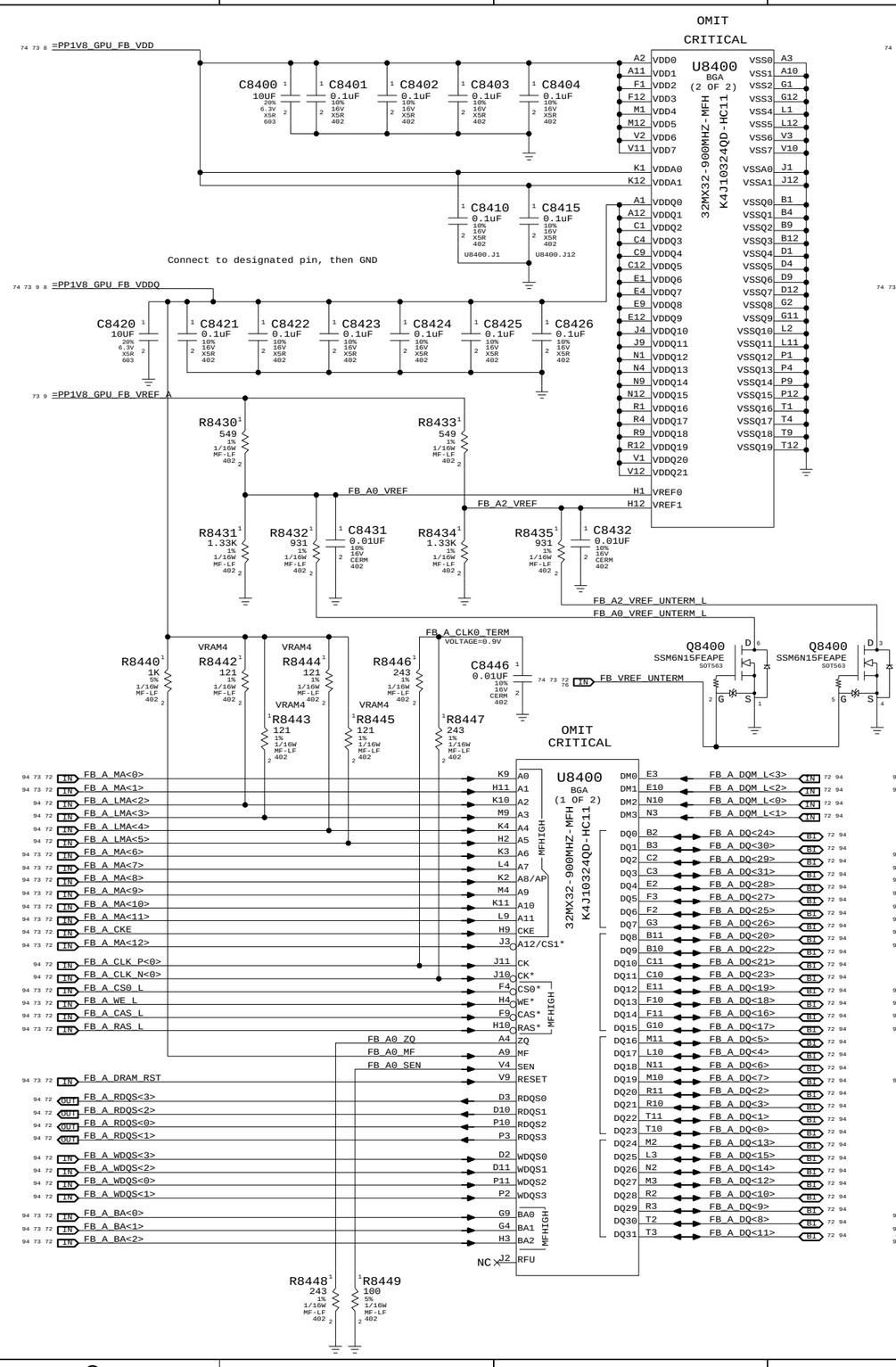
D	051-7546	A.0.0
SCALE: NONE	SHT 72 OF 96	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

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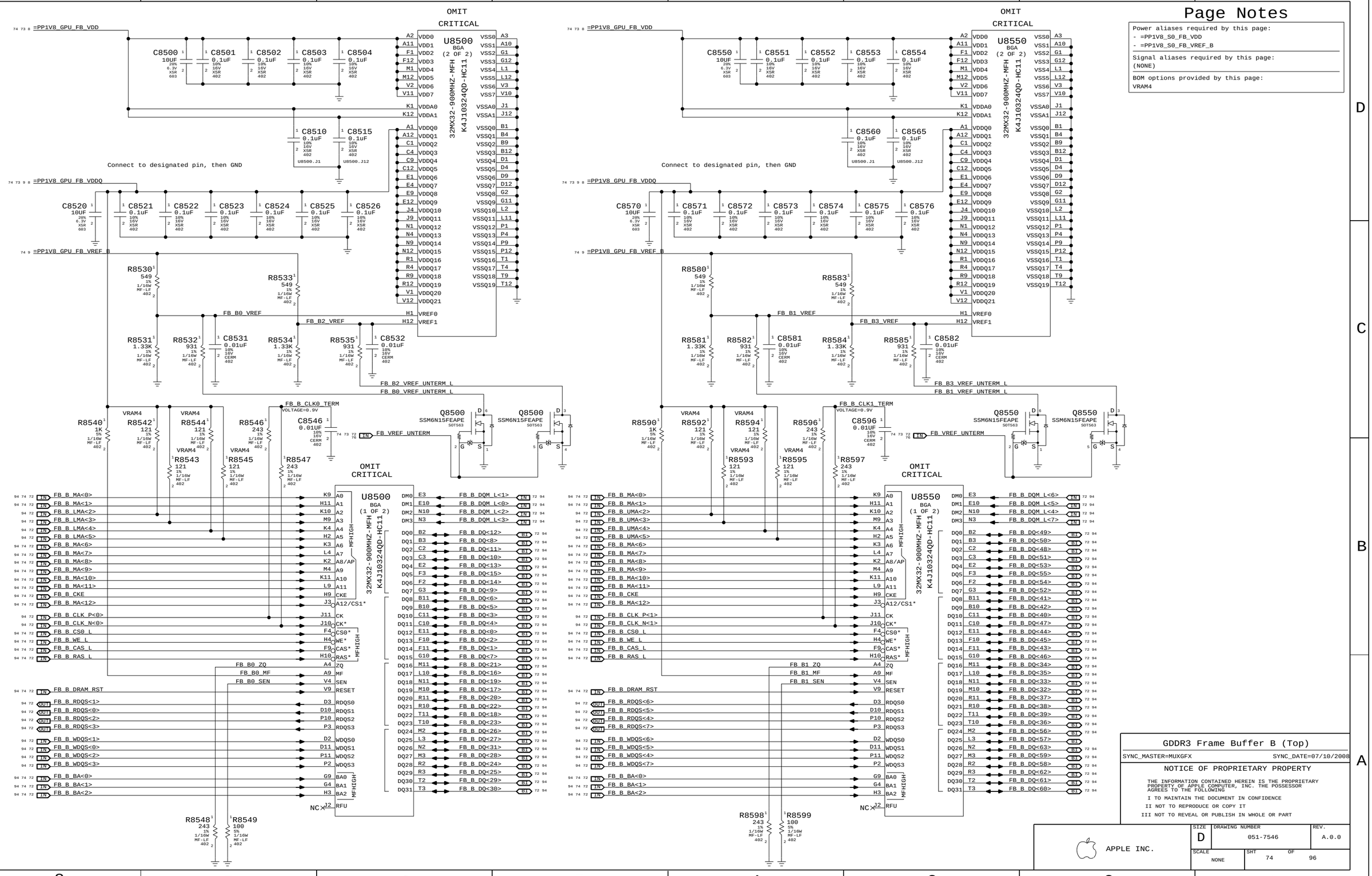

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
=PP3V3_GPU_VDD33

OMIT
U8000
NB9P-GS
BGA
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C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 10% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 10% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

=PP3V3_GPU_MIO
R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402
R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1UF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1UF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

L8630 FERR-220-OHM 0402
=PP1V1_GPU_PLLVDD
PP1V1_GPU_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

L8635 FERR-220-OHM 0402
=PP1V1_GPU_H_PLLVDD
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

L8640 FERR-220-OHM 0402
=PP1V1_GPU_VID_PLLVDD
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

J9	VDD33_1		
J10	VDD33_2		
J11	VDD33_3		
J12	VDD33_4		
J13	VDD33_5		
J25	RFU0	NC	
J26	RFU1	NC	
AK14	RFU0_GND		
K9	RFU1_GND		
C3	ROM_CS*	GPU_ROM_CS_L	76
D4	ROM_SCLK	GPU_ROM_SCLK	76
D3	ROM_SI	GPU_ROM_SI	76
C4	ROM_SO	GPU_ROM_SO	76
N9	STRAP_REF_3V3	GPU_STRAP_REF_3V3_PD	
M9	STRAP_REF_MIOB (1PD)	GPU_STRAP_REF_MIOB_PD	
P9	MIOA_VDDQ_1	=PP3V3_GPU_MIO	76 75 8
R9	MIOA_VDDQ_2		
T9	MIOA_VDDQ_3		
U9	MIOA_VDDQ_4		
AA9	MIOB_VDDQ_1		
AB9	MIOB_VDDQ_2		
W9	MIOB_VDDQ_3		
Y9	MIOB_VDDQ_4		
AP35	TESTMODE	GPU_TESTMODE_PD	
N5	MIOA_VREF	GPU_MIOA_VREF	
AF1	MIOB_VREF	GPU_MIOB_VREF	
U5	MIOA_CAL_PD_VDDQ	GPU_MIOA_PD_VDDQ	75
T5	MIOA_CAL_PU_GND	GPU_MIOA_PU_GND	75
AA7	MIOB_CAL_PD_VDDQ	GPU_MIOB_PD_VDDQ	75
AA6	MIOB_CAL_PU_GND	GPU_MIOB_PU_GND	75
AF9	SP_PLLVDD		
AE9	PLLVDD		
AD9	VID_PLLVDD		
B1	XTAL_IN	GPU_XTALIN	76 IN
B2	XTAL_OUT	GPU_XTALOUT	76 OUT
D1	XTAL_OUTBUFF	GPU_XTALOUTBUFF	76 OUT
D2	XTAL_SSIN	GPU_XTALSSIN	76 IN

K1	GPIO0	GPU_GPIO_0	B1 76
K2	GPIO1	GPU_GPIO_1	B1 76
K3	GPIO2	GPU_GPIO_2	B1 76
H3	GPIO3	GPU_GPIO_3	B1 76
H2	GPIO4	GPU_GPIO_4	B1 76
H1	GPIO5	GPU_GPIO_5	B1 76
H4	GPIO6	GPU_GPIO_6	B1 76
H5	GPIO7	GPU_GPIO_7	B1 76
H6	GPIO8	GPU_GPIO_8	B1 76
J7	GPIO9	GPU_GPIO_9	B1 76
K4	GPIO10	GPU_GPIO_10	B1 76
K5	GPIO11	GPU_GPIO_11	B1 76
H7	GPIO12	GPU_GPIO_12	B1 76
J4	GPIO13	GPU_GPIO_13	B1 76
J6	GPIO14	GPU_GPIO_14	B1 76
L1	GPIO15	GPU_GPIO_15	B1 76
L2	GPIO16	GPU_GPIO_16	B1 76
L4	GPIO17	GPU_GPIO_17	B1 76
M4	GPIO18	GPU_GPIO_18	B1 76
L7	GPIO19	GPU_GPIO_19	B1 76
L5	GPIO20	GPU_GPIO_20	B1 76
K6	GPIO21	GPU_GPIO_21	B1 76
L6	GPIO22	GPU_GPIO_22	B1 76
M6	GPIO23	GPU_GPIO_23	B1 76
C7	HDA_SDI	GPU_HDA_SDI	OUT 76
B7	HDA_SDO	GPU_HDA_SDO	OUT 76
A7	HDA_SYNC	GPU_HDA_SYNC	OUT 76
D7	HDA_BCLK	GPU_HDA_BCLK	OUT 76
D6	HDA_RST*	GPU_HDA_RST_L	OUT 76
A5	SPDIF	GPU_SPDIF	IN 76
A4	BUFRST*	TP_GPU_BUFRST_L	OUT
AP14	JTAG_TCK	GPU_JTAG_TCK	IN 6
AN14	JTAG_TDI	GPU_JTAG_TDI	IN 6
AN16	JTAG_TDO	GPU_JTAG_TDO	OUT 6
AR14	JTAG_TMS	GPU_JTAG_TMS	IN 6
AP16	JTAG_TRST*	GPU_JTAG_TRST_L	IN 6
N4	MIOA_CLKIN	GPU_MIOA_CLKIN	IN 76
R4	MIOA_CLKOUT	GPU_MIOA_CLKOUT_P	B1 76
T4	MIOA_CLKOUT*	GPU_MIOA_CLKOUT_N	B1 76
P5	MIOA_CTL3	GPU_MIOA_CTL3	B1 76
N2	MIOA_DE	GPU_MIOA_DE	B1 76
N1	MIOA_D0	GPU_MIOA_D<0>	B1 76
P4	MIOA_D1	GPU_MIOA_D<1>	B1 76
P1	MIOA_D2	GPU_MIOA_D<2>	B1 76
P2	MIOA_D3	GPU_MIOA_D<3>	B1 76
P3	MIOA_D4	GPU_MIOA_D<4>	B1 76
T3	MIOA_D5	GPU_MIOA_D<5>	B1 76
T2	MIOA_D6	GPU_MIOA_D<6>	B1 76
T1	MIOA_D7	GPU_MIOA_D<7>	B1 76
U4	MIOA_D8	GPU_MIOA_D<8>	B1 76
U1	MIOA_D9	GPU_MIOA_D<9>	B1 76
U2	MIOA_D10	GPU_MIOA_D<10>	B1 76
U3	MIOA_D11	GPU_MIOA_D<11>	B1 76
R6	MIOA_D12	GPU_MIOA_D<12>	B1 76
T6	MIOA_D13	GPU_MIOA_D<13>	B1 76
N6	MIOA_D14	GPU_MIOA_D<14>	B1 76
N3	MIOA_HSYNC	GPU_MIOA_HSYNC	B1 76
L3	MIOA_VSYNC	GPU_MIOA_VSYNC	B1 76
AE1	MIOB_CLKIN	GPU_MIOB_CLKIN	IN 76
V4	MIOB_CLKOUT	GPU_MIOB_CLKOUT_P	B1 76
W4	MIOB_CLKOUT*	GPU_MIOB_CLKOUT_N	B1 76
W3	MIOB_CTL3	GPU_MIOB_CTL3	B1 76
Y5	MIOB_DE	GPU_MIOB_DE	B1 76
Y1	MIOB_D0	GPU_MIOB_D<0>	B1 76
Y2	MIOB_D1	GPU_MIOB_D<1>	B1 76
Y3	MIOB_D2	GPU_MIOB_D<2>	B1 76
AB3	MIOB_D3	GPU_MIOB_D<3>	B1 76
AB2	MIOB_D4	GPU_MIOB_D<4>	B1 76
AB1	MIOB_D5	GPU_MIOB_D<5>	B1 76
AC4	MIOB_D6	GPU_MIOB_D<6>	B1 76
AC1	MIOB_D7	GPU_MIOB_D<7>	B1 76
AC2	MIOB_D8	GPU_MIOB_D<8>	B1 76
AC3	MIOB_D9	GPU_MIOB_D<9>	B1 76
AE3	MIOB_D10	GPU_MIOB_D<10>	B1 76
AE2	MIOB_D11	GPU_MIOB_D<11>	B1 76
U6	MIOB_D12	GPU_MIOB_D<12>	B1 76
W6	MIOB_D13	GPU_MIOB_D<13>	B1 76
Y6	MIOB_D14	GPU_MIOB_D<14>	B1 76
W5	MIOB_D15	GPU_STRAP<0>	B1 76
W7	MIOB_D16	GPU_STRAP<1>	B1 76
V7	MIOB_D17	GPU_STRAP<2>	B1 76
W1	MIOB_HSYNC	GPU_MIOB_HSYNC	B1 76
W2	MIOB_VSYNC	GPU_MIOB_VSYNC	B1 76
B5	THERMDP	GPU_THERMD_P	IN 76
B4	THERMDN	GPU_THERMD_N	OUT 76
C5	PGOOD_OUT*	TP_GPU_PGOOD_OUT_L	OUT

NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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SCALE: NONE	SHT 75 OF 96	

GPIOs

	Native Func		
GPU_GPIO_0	GP	NC_GPU_GPIO_0	MAKE_BASE=TRUE
GPU_GPIO_1	HPDC	DP_EG_HPD	IN 80
GPU_GPIO_2	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM	MAKE_BASE=TRUE
GPU_GPIO_3	LCD0_VDD	EG_LCD_PWR_EN	76 83 MAKE_BASE=TRUE
GPU_GPIO_4	LCD0_BL_EN	EG_BKLT_EN	76 83 MAKE_BASE=TRUE
GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE
GPU_GPIO_7	VID2/MEM_VID	GPIO7_FBVDD_ALTVO	76 82 MAKE_BASE=TRUE
GPU_GPIO_8	THERM	SMC_GFX_OVERTEMP_R_L	76 MAKE_BASE=TRUE
GPU_GPIO_9	FAN_PWM	SMC_GFX_THROTTLE_R_L	76 MAKE_BASE=TRUE
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	72 73 74 76 MAKE_BASE=TRUE
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	OUT 78 MAKE_BASE=TRUE
GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	OUT 78 MAKE_BASE=TRUE
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	OUT 78 MAKE_BASE=TRUE
GPU_GPIO_14	PWR_CTL1	TP_GPU_VCORE_VID3	MAKE_BASE=TRUE

GPIOs

	Native Func		
GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET	76 MAKE_BASE=TRUE
GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE
GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE
GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE
GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE
GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE
GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE
GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE NO_TEST=TRUE

Renamed signals

GPU_XTALOUT	MAKE_BASE=TRUE	GPU_XTALOUT
GPU_CLK27M	MAKE_BASE=TRUE	GPU_XTALIN
GPU_CLK27M_SS	MAKE_BASE=TRUE	GPU_XTALSSIN
GPU_TDIODE_P	MAKE_BASE=TRUE	GPU_THERMD_P
GPU_TDIODE_N	MAKE_BASE=TRUE	GPU_THERMD_N
LVDS_EG_DDC_CLK	MAKE_BASE=TRUE	GPU_I2CA_SCL
LVDS_EG_DDC_DATA	MAKE_BASE=TRUE	GPU_I2CA_SDA
DP_EG_DDC_CLK	MAKE_BASE=TRUE	GPU_I2CB_SCL
DP_EG_DDC_DATA	MAKE_BASE=TRUE	GPU_I2CB_SDA

Unused signals

NC_GPU_SPDIF	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_SPDIF
NC_CPU_HDA_SDI	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_HDA_SDI
NC_CPU_HDA_SD0	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_HDA_SDO
NC_CPU_HDA_SYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_HDA_SYNC
NC_CPU_HDA_BCLK	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_HDA_BCLK
NC_CPU_HDA_RST_L	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_HDA_RST_L
NC_FBA_MA<13>	MAKE_BASE=TRUE NO_TEST=TRUE	FB_A_MA<13>
NC_FBB_MA<13>	MAKE_BASE=TRUE NO_TEST=TRUE	FB_B_MA<13>
NC_FBA_CMD28	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBA_CMD28
NC_FBC_CMD28	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBC_CMD28
NC_FBA_CMD29	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBA_CMD29
NC_FBC_CMD29	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBC_CMD29
NC_FBA_CMD30	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBA_CMD30
NC_FBC_CMD30	MAKE_BASE=TRUE NO_TEST=TRUE	TP_FBC_CMD30
NC_GPU_ROM_CS_L	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_ROM_CS_L
NC_FB_A_CS1_L	MAKE_BASE=TRUE NO_TEST=TRUE	FB_A_CS1_L
NC_FB_B_CS1_L	MAKE_BASE=TRUE NO_TEST=TRUE	FB_B_CS1_L

Unused I2C Buses

NC_GPU_I2CC_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CC_SCL
NC_GPU_I2CC_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CC_SDA
NC_GPU_I2CD_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CD_SCL
NC_GPU_I2CD_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CD_SDA
NC_GPU_I2CE_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CE_SCL
NC_GPU_I2CE_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CE_SDA
NC_GPU_I2CH_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CH_SDA
NC_GPU_I2CH_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_I2CH_SCL

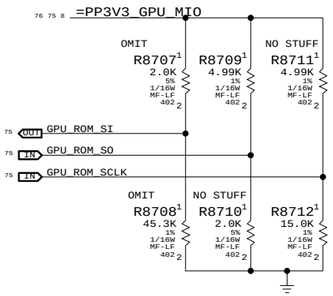
I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

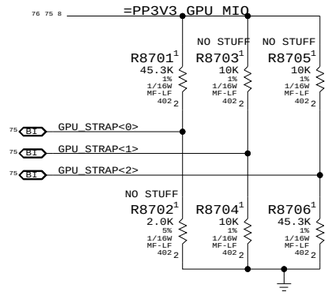
TP_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE	LVDS_EG_B_CLK_P
TP_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE	LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_EG_B_DATA_N<3>

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_CLKOUT_P
NC_GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_CLKOUT_N
NC_GPU_MIOA_CTL3	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_CTL3
TP_GPU_MIOA_DE	MAKE_BASE=TRUE	GPU_MIOA_DE
TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	GPU_MIOA_D<9..0>
NC_GPU_MIOA_CLKIN	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_CLKIN
NC_GPU_MIOA_D<14..10>	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_D<14..10>
NC_GPU_MIOA_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_HSYNC
NC_GPU_MIOA_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_VSYNC
NC_GPU_MIOB_CLKIN	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_CLKIN
NC_GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_CLKOUT_P
NC_GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_CLKOUT_N
NC_GPU_MIOB_CTL3	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_CTL3
NC_GPU_MIOB_DE	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_DE
NC_GPU_MIOB_D<14..0>	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_D<14..0>
NC_GPU_MIOB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_VSYNC
NC_GPU_MIOB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_HSYNC

Config Straps





Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

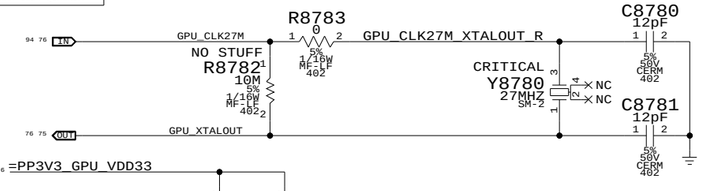
Strap S1/S2 Bit[3:0]	PU/PD	Rval
0 0000	PD	5k
1 0001	PD	10k
2 0010	PD	15k
3 0011	PD	20k
4 0100	PD	25k
5 0101	PD	30k
6 0110	PD	35k
7 0111	PD	45k

Strap S1/S2 Bit[3:0]	PU/PD	Rval
8 1000	PU	5k
9 1001	PU	10k
A 1010	PU	15k
B 1011	PU	20k
C 1100	PU	25k
D 1101	PU	30k
E 1110	PU	35k
F 1111	PU	45k

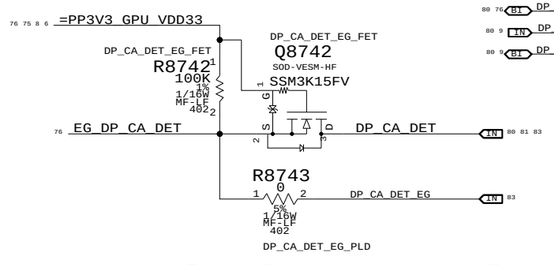
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA

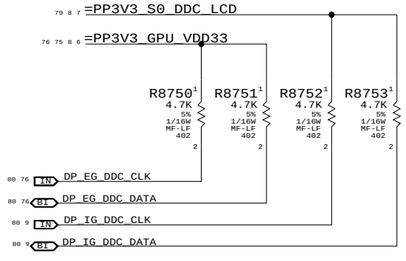
G96 HDCP ROM APN is 341S2272, blank device is 335S0574.

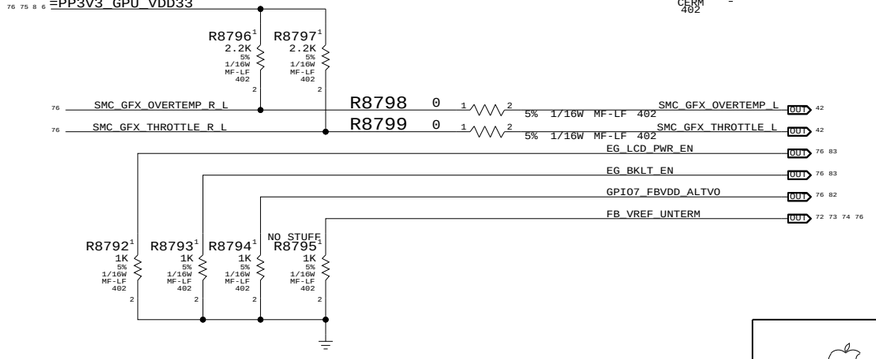
GPU 27MHz Crystal



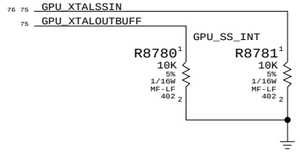
Isolation FETs for DP MUX inputs







Unused Clocks



G96 GPIOs & Straps

SYNC_MASTER=MUXGFX SYNC_DATE=07/09/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 76 OF 96	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 77
GPU_IFPCD_RSET 77
GPU_IFPAB_RSET 77

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

=PP1V1_GPU_IFPCD_IOVDD

L8810 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AJ8
Place at AK8
PP1V1_GPU_IFPCD_IOVDD_F 77
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM 0402
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPCD_PLLVDD_F 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 77
PP1V8_GPU_IFPEF_PLLVDD_F 77

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	
AG10	IFPB_IOVDD	
AJ8	IFPC_IOVDD	
AK8	IFPD_IOVDD	
AE7	IFPE_IOVDD	
AD7	IFPF_IOVDD	
AK9	IFPAB_PLLVDD	
AJ11	IFPAB_RSET	
AJ9	IFPCD_PLLVDD	
AK7	IFPCD_RSET	
AJ6	IFPEF_PLLVDD	
AL1	IFPEF_RSET	
G1	I2CA_SCL	
G4	I2CA_SDA	
E3	I2CC_SCL	
E4	I2CC_SDA	
E2	I2CS_SCL	
E1	I2CS_SDA	
F6	I2CH_SCL	
G6	I2CH_SDA	
G3	I2CB_SCL	
G2	I2CB_SDA	
F4	I2CD_SCL	
G5	I2CD_SDA	
D5	I2CE_SCL	
E5	I2CE_SDA	
AJ12	DACA_VDD	
AK12	DACA_VREF	
AC13	DACA_RSET	
AC6	DACB_VDD	
AC5	DACB_VREF	
AB6	DACB_RSET	
AG7	DACC_VDD	
AK6	DACC_VREF	
AG7	DACC_RSET	

AM11	IFPA_TXC	LVDS_EG_A_CLK_P
AM12	IFPA_TXC*	LVDS_EG_A_CLK_N
AM8	IFPA_TXD0	LVDS_EG_A_DATA_P<0>
AL8	IFPA_TXD0*	LVDS_EG_A_DATA_N<0>
AM10	IFPA_TXD1	LVDS_EG_A_DATA_P<1>
AM9	IFPA_TXD1*	LVDS_EG_A_DATA_N<1>
AK10	IFPA_TXD2	LVDS_EG_A_DATA_P<2>
AL10	IFPA_TXD2*	LVDS_EG_A_DATA_N<2>
AK11	IFPA_TXD3	LVDS_EG_A_DATA_P<3>
AL11	IFPA_TXD3*	LVDS_EG_A_DATA_N<3>
AP13	IFPB_TXC	LVDS_EG_B_CLK_P
AN13	IFPB_TXC*	LVDS_EG_B_CLK_N
AN8	IFPB_TXD4	LVDS_EG_B_DATA_P<0>
AP8	IFPB_TXD4*	LVDS_EG_B_DATA_N<0>
AP10	IFPB_TXD5	LVDS_EG_B_DATA_P<1>
AN10	IFPB_TXD5*	LVDS_EG_B_DATA_N<1>
AR11	IFPB_TXD6	LVDS_EG_B_DATA_P<2>
AR10	IFPB_TXD6*	LVDS_EG_B_DATA_N<2>
AN11	IFPB_TXD7	LVDS_EG_B_DATA_P<3>
AP11	IFPB_TXD7*	LVDS_EG_B_DATA_N<3>
AP2	IFPC_AUX	DP_EG_AUX_CH_P
AN3	IFPC_AUX*	DP_EG_AUX_CH_N
AM7	IFPC_L0	DP_EG_ML_P<0>
AM6	IFPC_L0*	DP_EG_ML_N<0>
AL5	IFPC_L1	DP_EG_ML_P<1>
AM5	IFPC_L1*	DP_EG_ML_N<1>
AM3	IFPC_L2	DP_EG_ML_P<2>
AM4	IFPC_L2*	DP_EG_ML_N<2>
AP1	IFPC_L3	DP_EG_ML_P<3>
AR2	IFPC_L3*	DP_EG_ML_N<3>
AP4	IFPD_AUX	NC
AN4	IFPD_AUX*	NC
AR8	IFPD_L0	NC
AR7	IFPD_L0*	NC
AP7	IFPD_L1	NC
AN7	IFPD_L1*	NC
AN5	IFPD_L2	NC
AP5	IFPD_L2*	NC
AR5	IFPD_L3	NC
AR4	IFPD_L3*	NC
AE4	IFPE_AUX	NC
AD4	IFPE_AUX*	NC
AH6	IFPE_L0	NC
AH5	IFPE_L0*	NC
AH4	IFPE_L1	NC
AG4	IFPE_L1*	NC
AF4	IFPE_L2	NC
AF5	IFPE_L2*	NC
AE6	IFPE_L3	NC
AE5	IFPE_L3*	NC
AF3	IFPF_AUX	NC
AF2	IFPF_AUX*	NC
AL2	IFPF_L0	NC
AL3	IFPF_L0*	NC
AJ2	IFPF_L1	NC
AJ3	IFPF_L1*	NC
AJ1	IFPF_L2	NC
AH1	IFPF_L2*	NC
AH2	IFPF_L3	NC
AH3	IFPF_L3*	NC
AM15	DACA_RED	NC
AM14	DACA_GREEN	NC
AL14	DACA_BLUE	NC
AM13	DACA_HSYNC	NC
AL13	DACA_VSYNC	NC
AA4	DACB_RED	NC
AB4	DACB_GREEN	NC
Y4	DACB_BLUE	NC
AB5	DACB_CSYNC	NC
AK4	DACC_RED	NC
AL4	DACC_GREEN	NC
AJ4	DACC_BLUE	NC
AM1	DACC_HSYNC	NC
AM2	DACC_VSYNC	NC

R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402 NO STUFF

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

NV G96 Video Interfaces

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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D	051-7546	A.0.0
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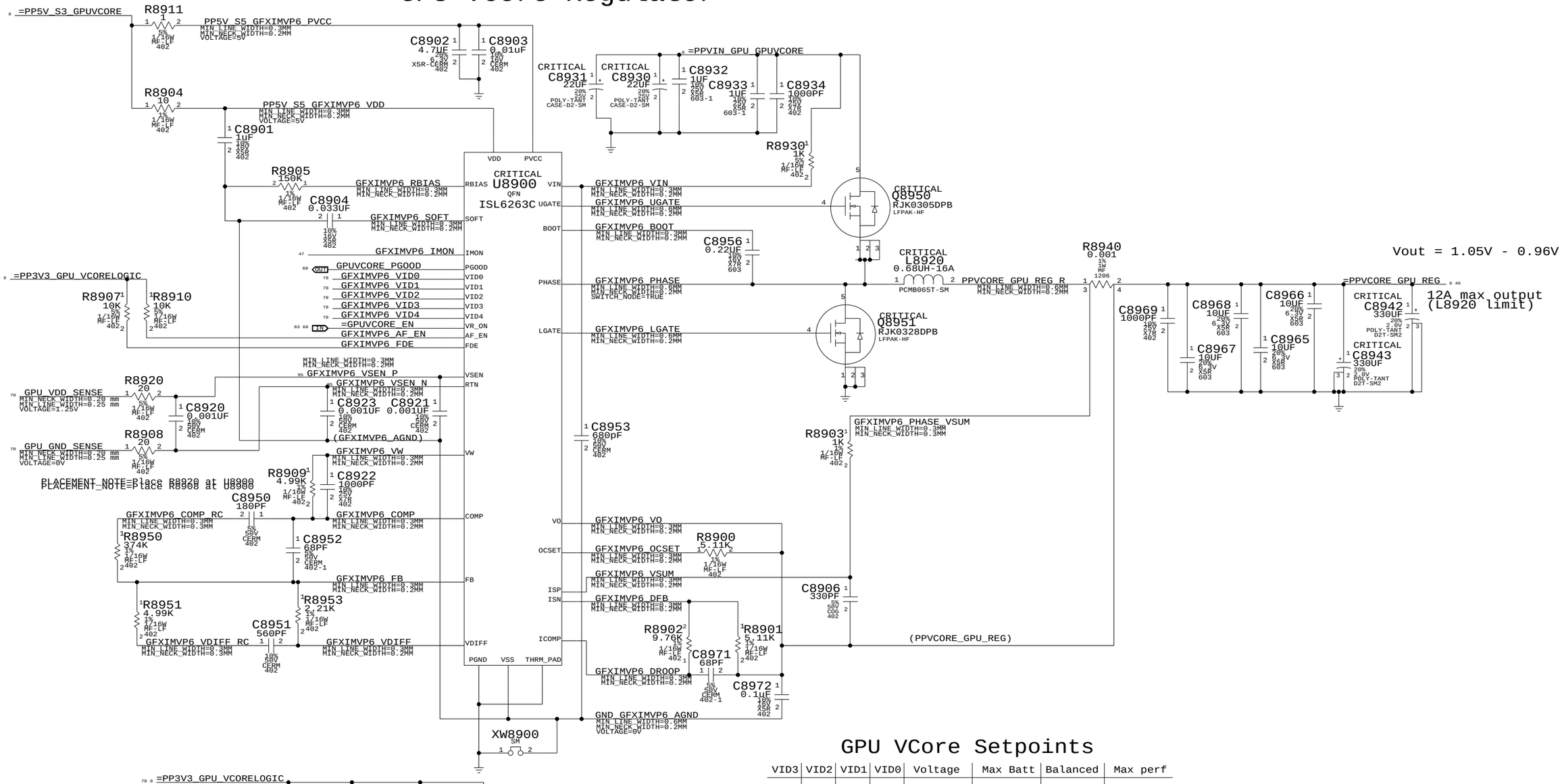
GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	M98		-
1	1	1	0	0.92700V	-	M98	-
1	0	1	1	1.00425V	-	-	M98

Other VID states may not be valid

M98 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G84M) Core Supply

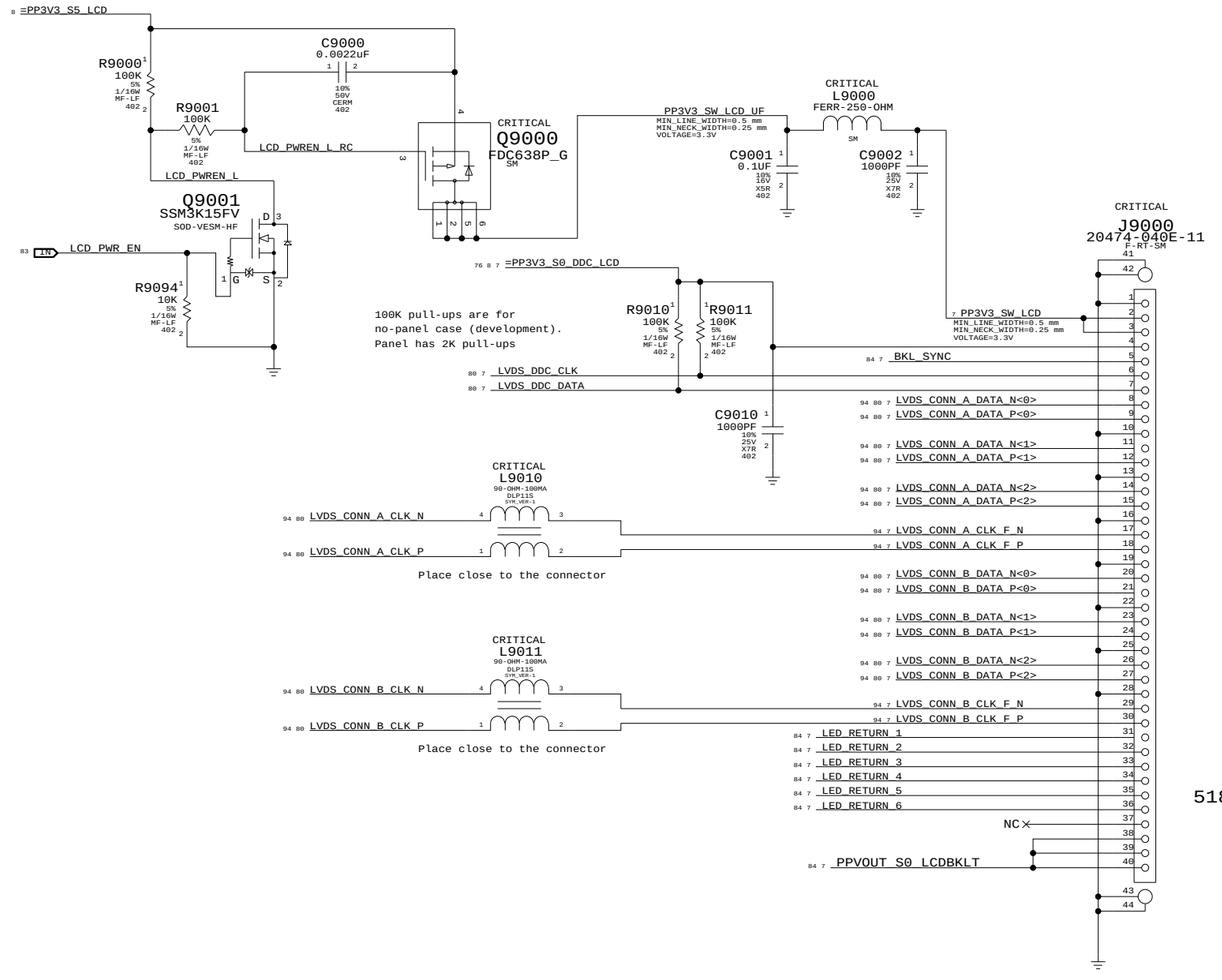
SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 78 OF 96

LCD (LVDS) INTERFACE



518S0651

LVDS Display Connector

SYNC_MASTER=MUXGFX SYNC_DATE=02/25/2008

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D	051-7546	A.0.0
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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9200 (All 24 resistors)

LVDS_A_CLK_P	R9320 270 1% 1/10W MF-LF 402	LVDS_CONN_A_CLK_P	
	R9321 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_A_CLK_N	R9322 270 1% 1/10W MF-LF 402	LVDS_CONN_A_CLK_N	
LVDS_A_DATA_P<0>	R9325 270 1% 1/10W MF-LF 402	LVDS_CONN_A_DATA_P<0>	
	R9326 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_A_DATA_N<0>	R9327 270 1% 1/10W MF-LF 402	LVDS_CONN_A_DATA_N<0>	
LVDS_A_DATA_P<1>	R9330 270 1% 1/10W MF-LF 402	LVDS_CONN_A_DATA_P<1>	
	R9331 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_A_DATA_N<1>	R9332 270 1% 1/10W MF-LF 402	LVDS_CONN_A_DATA_N<1>	
LVDS_A_DATA_P<2>	R9335 270 1% 1/10W MF-LF 402	LVDS_CONN_A_DATA_P<2>	
	R9336 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_A_DATA_N<2>	R9337 270 1% 1/10W MF-LF 402	LVDS_CONN_A_DATA_N<2>	
LVDS_B_CLK_P	R9340 270 1% 1/10W MF-LF 402	LVDS_CONN_B_CLK_P	
	R9341 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_B_CLK_N	R9342 270 1% 1/10W MF-LF 402	LVDS_CONN_B_CLK_N	
LVDS_B_DATA_P<0>	R9345 270 1% 1/10W MF-LF 402	LVDS_CONN_B_DATA_P<0>	
	R9346 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_B_DATA_N<0>	R9347 270 1% 1/10W MF-LF 402	LVDS_CONN_B_DATA_N<0>	
LVDS_B_DATA_P<1>	R9350 270 1% 1/10W MF-LF 402	LVDS_CONN_B_DATA_P<1>	
	R9351 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_B_DATA_N<1>	R9352 270 1% 1/10W MF-LF 402	LVDS_CONN_B_DATA_N<1>	
LVDS_B_DATA_P<2>	R9355 270 1% 1/10W MF-LF 402	LVDS_CONN_B_DATA_P<2>	
	R9356 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY		
LVDS_B_DATA_N<2>	R9357 270 1% 1/10W MF-LF 402	LVDS_CONN_B_DATA_N<2>	

DisplayPort Mux

=PP3V3_S0_DPMUX

MUXGFX U9320 CBTL06141EE BGA CRITICAL SIGNAL_MODEL=DPMUX

DP_IG_ML_P<0>	B4 DIN1_0+	DOUT_0+ B2	DP_ML_P<0>
DP_IG_ML_N<0>	A4 DIN1_0-	DOUT_0- B1	DP_ML_N<0>
DP_IG_ML_P<1>	B5 DIN1_1+	DOUT_1+ D2	DP_ML_P<1>
DP_IG_ML_N<1>	A5 DIN1_1-	DOUT_1- D1	DP_ML_N<1>
DP_IG_ML_P<2>	B6 DIN1_2+	DOUT_2+ E2	DP_ML_P<2>
DP_IG_ML_N<2>	A6 DIN1_2-	DOUT_2- E1	DP_ML_N<2>
DP_IG_ML_P<3>	A8 DIN1_3+	DOUT_3+ F2	DP_ML_P<3>
DP_IG_ML_N<3>	A9 DIN1_3-	DOUT_3- F1	DP_ML_N<3>
DP_IG_AUX_CH_P	C9330 0.1uF H9 DAUX1+	AUX+ H2	DP_AUX_CH_C_P
DP_IG_AUX_CH_N	C9331 0.1uF J9 DAUX1-	AUX- H1	DP_AUX_CH_C_N
DP_IG_DDC_CLK	H8 DDC_CLK1		
DP_IG_DDC_DATA	J8 DDC_DAT1		
DP_IG_HPD	J2 HPD_1		
DP_EG_ML_P<0>	B8 DIN2_0+		
DP_EG_ML_N<0>	B9 DIN2_0-		
DP_EG_ML_P<1>	D8 DIN2_1+		
DP_EG_ML_N<1>	D9 DIN2_1-		
DP_EG_ML_P<2>	E8 DIN2_2+		
DP_EG_ML_N<2>	E9 DIN2_2-		
DP_EG_ML_P<3>	F8 DIN2_3+		
DP_EG_ML_N<3>	F9 DIN2_3-		
DP_EG_AUX_CH_P	C9335 0.1uF H6 DAUX2+		
DP_EG_AUX_CH_N	C9336 0.1uF J6 DAUX2-		
DP_EG_DDC_CLK	H5 DDC_CLK2		
DP_EG_DDC_DATA	J5 DDC_DAT2		
DP_EG_HPD	H3 HPD_2		
DP_MUX_SEL_EG	A1 GPU_SEL	DDC_AUX_SEL C2	DP_CA_DET (MAKE_BASE=TRUE)
DP_MUX_XSD_L	B7 XSD*	TST0 G2	

LO=PORT1 HI=PORT2 — LO=AUX_CH HI=DDC

GND: B3, C8, G8, H4, H7

MUXGFX C9320 0.1UF 20% 16V CERM 402 — MUXGFX C9321 0.1UF 20% 16V CERM 402

VDD

R9306 1K 5% 1/16W MF-LF 402 — DP_IG_AUX_CH_N

R9304 100K 5% 1/16W MF-LF 402 — DP_IG_HPD

R9305 100K 5% 1/16W MF-LF 402 — DP_EG_HPD

DPMUX_EN_HPD: R9301 10K 1% 1/10W MF-LF 402; C9301 1UF 10% 6.3V CERM-X5R 402

DP_HOTPLUG_DET (MAKE_BASE=TRUE)

DP_IG_CA_DET

=PP3V3_S0_DPMUX → DPMUX_EN_S0&DPMUX_EN_PLD → R9302 10K 1% 1/10W MF-LF 402 → DPMUX_EN_PLD → R9303 0 5% 1/10W MF-LF 402 → DP_MUX_EN

PLACEMENT_NOTE=Place at U9320

MUXGFX R9307 1K 5% 1/10W MF-LF 402: HPDIN J1 — DP_HPD_R — DP_HPD

LVDS DDC MUX

=PP3V3_GPU_LVDS_DDC

R9370 20K 5% 1/16W MF-LF 402 — R9371 20K 5% 1/16W MF-LF 402

=PP3V3_S0_LVDSDDCMUX

C9370 0.1UF 20% 16V CERM 402

R9372 20K 5% 1/16W MF-LF 402 — R9373 20K 5% 1/16W MF-LF 402

U9370 SN74LV4066A QFN1 VCC GND_THRM

LVDS_DDC_SEL_EG	C1	A1 LVDS_EG_DDC_CLK
LVDS_DDC_SEL_IG	C2	A2 LVDS_IG_DDC_CLK
		B2 LVDS_DDC_CLK
	C3	A3 LVDS_EG_DDC_DATA
	C4	A4 LVDS_IG_DDC_DATA
		B4 LVDS_DDC_DATA

Muxed Graphics Support

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

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D	051-7546	A.0.0
SCALE: NONE	SHT 80 OF 96	

Port Power Switch

U9480 TPS2051B SOT23 (CRITICAL)
=PP3V3_S5_DP_PORT_PWR, PM_SLP_S3_L
PP3V3_S0_DPILIM (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
TP_DPPWR_OC_L
C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
C9486 22UF 20% 6.3V X5R-CERM 603 (CRITICAL)
L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 20% 50V CERM 603
PP3V3_S0_DPPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
R9420 100K 5% 1/10W MF-LF 402

HDMI_CEC

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402
R9425 1M 5% 1/16W MF-LF 402

DP_ML_P<3> C9414 0.1uF 10% 16V X5R 402 DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF 10% 16V X5R 402 DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

FL9403 12-OHM-100MA TCM1210-4SM

CRITICAL
J9400 DSPLYPRT-M097-2 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS	
2	DP_HPD	GND	1
4	DP_C_A_DET	ML_LANE0P	3
6	HDMI_CEC	ML_LANE0N	5
8	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

SHIELD PINS 22 21

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

R9421 100K 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402
R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402

FL9400 12-OHM-100MA TCM1210-4SM
FL9401 12-OHM-100MA TCM1210-4SM
FL9402 12-OHM-100MA TCM1210-4SM

DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

DP_ML_C_P<0> C9410 0.1uF 10% 16V X5R 402 DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF 10% 16V X5R 402 DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF 10% 16V X5R 402 DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF 10% 16V X5R 402 DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF 10% 16V X5R 402 DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF 10% 16V X5R 402 DP_ML_N<2>

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

R9422 1M 5% 1/16W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/16W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

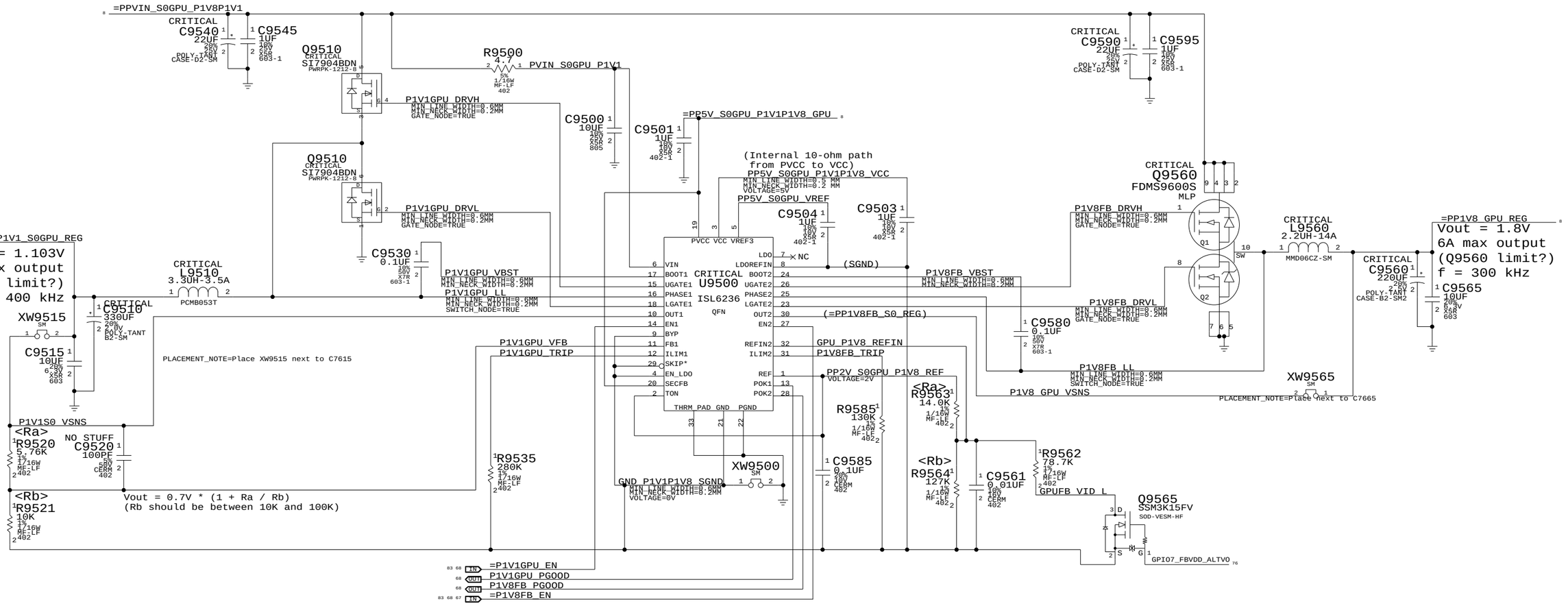
DisplayPort Connector

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 81 OF 96	



1.1V / 1V8 FB Power Supply

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 82 OF 96	

GMUX CPLD

=PP3V3_S0_GMUX
=PP2V5_S0_GMUX
=PP1V2_S0_GMUX

C9610 C9621 C9622 C9623 C9624 C9625 C9626 C9628 C9629 C9630 0.1UF 20% 10V CERM 402
C9611 C9612 C9613 C9614 C9615 C9616 C9617 0.1UF 20% 10V CERM 402
C9600 4.7UF 20% 10V X5R 402
C9604 C9605 C9606 C9607 C9608 C9609 0.1UF 20% 10V CERM 402

L9631 FERR-220-OHM 0402
PP3V3_S0_ULC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C9631 0.1UF 20% 10V CERM 402

L9627 FERR-220-OHM 0402
PP3V3_S0_LRC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C9627 0.1UF 20% 10V CERM 402

R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402
NO STUFF R9641 10K 1% 1/16W MF-LF 402
NO STUFF R9646 10K 1% 1/16W MF-LF 402

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO6 B5 · VCCIO1 B7 · VCCIO2 A12 · VCCIO3 C14 · VCCIO4 F13 · VCCIO5 M12 · VCCIO6 M9 · VCCIO7 M3 · VCCJ N5 · ULC_VCCPLL M1 · LRC_VCCPLL C3 · A4 F2 · P11 K12

OMIT CRITICAL
U9600 XP28 CSBGA-HF

83 6	JTAG_GMUX_TCK	K14	TCK	
9 6 IN	JTAG_GMUX_TDI	L13	TDI	
9 6 OUT	JTAG_GMUX_TDO	K13	TDO	
9 6 IN	JTAG_GMUX_TMS	L12	TMS	
	GMUX_TOE	K2	TOE	
	GMUX_CFG0	K1	CFG0	
9 OUT	LCD_BKLT_EN	P2	PB2A	BANK5
84 83 OUT	LCD_BKLT_PWM	N2	PB2B	
83 80 OUT	LVDS_DDC_SEL_EG	P4	PB14A	
83 80 OUT	LVDS_DDC_SEL_IG	N4	PB14B	
80 OUT	DP_MUX_EN	N3	PB15A (OD)	
83 80 OUT	DP_MUX_SEL_EG	M4	PB15B	
83 9 OUT	EG_RESET_L	P5	PB16A	
83 OUT	EG_RAIL1_EN	M5	PB16B	
83 OUT	EG_RAIL2_EN	P6	PB17A	
83 OUT	EG_RAIL3_EN	M6	PB17B	
83 OUT	EG_RAIL4_EN	P7	PB18A	
83 9 OUT	EG_CLKREQ_OUT_L	M7	PB18B (OD)	
76 OUT	DP_CA_DET_EG	N7	PB19A	
79 OUT	LCD_PWR_EN	N8	PB19B	
90 44 42 19 B1	LPC_AD<0>	P9	PB20A	BANK4
90 44 42 19 B1	LPC_AD<1>	N9	PB20B	
90 44 42 19 B1	LPC_AD<2>	P10	PB30A	
90 44 42 19 B1	LPC_AD<3>	M10	PB30B	
90 44 42 19 B1	LPC_FRAME_L	P12	PB31A	
90 26 19 IN	LPC_RESET_L	P13	PB31B	
26 IN	LPC_CLK33M_GMUX	N12	PB32A	
83 9 OUT	GMUX_INT	P14	PB32B	
89 83 18 IN	LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
89 83 18 IN	LVDS_IG_B_DATA_N<2>	B2	PL2B	
	TP_GMUX_PL10A	C2	PL10A	
	TP_GMUX_PL10B	D3	PL10B	
89 83 18 IN	LVDS_IG_A_DATA_P<0>	D1	PL11A	
89 83 18 IN	LVDS_IG_A_DATA_N<0>	E1	PL11B	
89 83 18 IN	LVDS_IG_A_DATA_P<1>	D2	PL12A	
89 83 18 IN	LVDS_IG_A_DATA_N<1>	E3	PL12B	
89 83 18 IN	LVDS_IG_A_DATA_P<2>	F1	PL13A	
89 83 18 IN	LVDS_IG_A_DATA_N<2>	G1	PL13B	
89 83 18 IN	LVDS_IG_B_DATA_P<0>	F3	PL14A	
89 83 18 IN	LVDS_IG_B_DATA_N<0>	G2	PL14B	
89 83 18 IN	LVDS_IG_B_DATA_P<1>	H2	PL15A	
89 83 18 IN	LVDS_IG_B_DATA_N<1>	G3	PL15B	
89 83 18 IN	LVDS_IG_A_CLK_P	H1	PL16A	
89 83 18 IN	LVDS_IG_A_CLK_N	H3	PL16B	
9 OUT	LVDS_MUX_SEL_EG	L1	PL18A	BANK6
	TP_GMUX_PL18B_VSYNC	L3	PL18B	
26 IN	=GMUX_PCIE_RESET_L	K3	PL19A	
83 IN	GMUX_PM_SLP_S3_L	L2	PL19B	
8 IN	ALL_EG_PGOOD	N1	PL32A	
83 IN	EG_CLKREQ_IN_L	P1	PL32B	

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND: J1 B8 C6 C12 C13 C13 H14 N10 N6 P3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PT2A	A2	LVDS_B_DATA_P<0>	OUT 80 94	BANK0
PT2B	A3	LVDS_B_DATA_N<0>	OUT 80 94	
PT3A	A1	LVDS_B_DATA_P<1>	OUT 80 94	
PT3B	B3	LVDS_B_DATA_N<1>	OUT 80 94	
PT4A	C5	LVDS_B_DATA_P<2>	OUT 80 94	
PT4B	A5	LVDS_B_DATA_N<2>	OUT 80 94	
PT14A	B6	EG_PWRSEQ_EN	IN 83	
PT14B	C7	GMUX_DEBUG_RESET_L	IN 83	
PT15A	A6	LVDS_A_CLK_P	OUT 80 94	
PT15B	A7	LVDS_A_CLK_N	OUT 80 94	
PT16A	C8	LVDS_B_CLK_P	OUT 80 94	
PT16B	C9	LVDS_B_CLK_N	OUT 80 94	
PT17A	A8	LVDS_A_DATA_P<0>	OUT 80 94	
PT17B	B9	LVDS_A_DATA_N<0>	OUT 80 94	
PT18A	A9	LVDS_A_DATA_P<1>	OUT 80 94	
PT18B	C10	LVDS_A_DATA_N<1>	OUT 80 94	
PT19A	B10	LVDS_A_DATA_P<2>	OUT 80 94	
PT19B	A10	LVDS_A_DATA_N<2>	OUT 80 94	
PT20A	A11	TP_GMUX_PT20A		BANK1
PT20B	B12	TP_GMUX_PT20B		
PT32A	B13	TP_GMUX_PT32A		
PT32B	A13	TP_GMUX_PT32B		
PR2A	A14	DP_CA_DET	IN 76 80 81	BANK2
PR2B	B14	DP_HOTPLUG_DET	IN 80	
PR10A	D12	LVDS_EG_A_DATA_P<0>	IN 77 83 94	
PR10B	D13	LVDS_EG_A_DATA_N<0>	IN 77 83 94	
PR11A	D14	LVDS_EG_A_DATA_P<1>	IN 77 83 94	
PR11B	E14	LVDS_EG_A_DATA_N<1>	IN 77 83 94	
PR12A	E12	LVDS_EG_A_DATA_P<2>	IN 77 83 94	
PR12B	F12	LVDS_EG_A_DATA_N<2>	IN 77 83 94	
PR13A	F14	LVDS_EG_B_DATA_P<0>	IN 77 83 94	
PR13B	G14	LVDS_EG_B_DATA_N<0>	IN 77 83 94	
PR14A	G12	LVDS_EG_B_DATA_P<1>	IN 77 83 94	
PR14B	G13	LVDS_EG_B_DATA_N<1>	IN 77 83 94	
PR15A	H13	LVDS_EG_B_DATA_P<2>	IN 77 83 94	
PR15B	H12	LVDS_EG_B_DATA_N<2>	IN 77 83 94	
PR16A	H14	LVDS_EG_A_CLK_P	IN 77 83 94	
PR16B	J12	LVDS_EG_A_CLK_N	IN 77 83 94	
PR18A	L14	IG_LCD_PWR_EN	IN 9	BANK3
PR18B	M13	EG_LCD_PWR_EN	IN 76	
PR30A	N14	IG_BKLT_EN	IN 9	
PR30B	N13	EG_BKLT_EN	IN 76	

PM_SLP_S3_L Isolation

83 8 =PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
42 37 34 21 7 81 68 44 IN PM_SLP_S3_L
EG_PWRSEQ_EN 83
GMUX_PM_SLP_S3_L 83
MAKE_BASE=TRUE

GMUX_JTAG_TCK Inversion

83 6 JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L IN 17

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_8K_BLANK
341S2350	1	IC,CPLD,LATTICE,132CSBGA,M98	U9600	CRITICAL	GMUX_PROG

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

89 83 18 LVDS_IG_A_CLK_P	R9650	100		LVDS_IG_A_CLK_N 18 83 89
89 83 18 LVDS_IG_A_DATA_P<0>	R9651	100		LVDS_IG_A_DATA_N<0> 18 83 89
89 83 18 LVDS_IG_A_DATA_P<1>	R9652	100		LVDS_IG_A_DATA_N<1> 18 83 89
89 83 18 LVDS_IG_A_DATA_P<2>	R9653	100		LVDS_IG_A_DATA_N<2> 18 83 89
89 83 18 LVDS_IG_B_DATA_P<0>	R9654	100		LVDS_IG_B_DATA_N<0> 18 83 89
89 83 18 LVDS_IG_B_DATA_P<1>	R9655	100		LVDS_IG_B_DATA_N<1> 18 83 89
89 83 18 LVDS_IG_B_DATA_P<2>	R9656	100		LVDS_IG_B_DATA_N<2> 18 83 89
94 83 77 LVDS_EG_A_CLK_P	R9660	100		LVDS_EG_A_CLK_N 77 83 94
94 83 77 LVDS_EG_A_DATA_P<0>	R9661	100		LVDS_EG_A_DATA_N<0> 77 83 94
94 83 77 LVDS_EG_A_DATA_P<1>	R9662	100		LVDS_EG_A_DATA_N<1> 77 83 94
94 83 77 LVDS_EG_A_DATA_P<2>	R9663	100		LVDS_EG_A_DATA_N<2> 77 83 94
94 83 77 LVDS_EG_B_DATA_P<0>	R9664	100		LVDS_EG_B_DATA_N<0> 77 83 94
94 83 77 LVDS_EG_B_DATA_P<1>	R9665	100		LVDS_EG_B_DATA_N<1> 77 83 94
94 83 77 LVDS_EG_B_DATA_P<2>	R9666	100		LVDS_EG_B_DATA_N<2> 77 83 94

1% 1/16W MF-LF 402

Required Pullups

SIGNAL_MODEL=EMPTY
=PP3V3_S0_GMUX

83 GMUX_DEBUG_RESET_L	R9680	1K	5% 1/16W MF-LF 402
83 6 JTAG_GMUX_TCK	R9690	4.7K	5% 1/16W MF-LF 402
83 9 EG_CLKREQ_OUT_L	R9695	10K	5% 1/16W MF-LF 402

NO STUFF R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9200

Required Pulldowns

83 80 DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
83 80 LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
83 80 LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF

83 9 EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
83 9 GMUX_INT	R9692	20K	5% 1/16W MF-LF 402
84 83 LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402
83 EG_CLKREQ_IN_L	R9694	100K	5% 1/16W MF-LF 402

EG_PWRSEQ_HW
R9630 0 5% 1/16W MF-LF 402 — EXTGPU_PWR_EN OUT 68

EG_PWRSEQ_GMUX
83 EG_RAIL1_EN — R9631 0 5% 1/16W MF-LF 402 — =P1V1GPU_EN OUT 68 82

EG_PWRSEQ_GMUX
83 EG_RAIL2_EN — R9632 0 5% 1/16W MF-LF 402 — P3V3GPU_EN OUT 68 69

EG_PWRSEQ_GMUX
83 EG_RAIL3_EN — R9633 0 5% 1/16W MF-LF 402 — =GPUVCORE_EN OUT 68 78

EG_PWRSEQ_GMUX
83 EG_RAIL4_EN — R9634 0 5% 1/16W MF-LF 402 — =P1V8FB_EN OUT 67 68 82

The MAKE BASE properties for these signals are on the POWER CONTROL page.

NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

Graphics MUX (GMUX)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 83 OF 96	

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PPBUS_S0_LCDBKLT_PWR
R9730 0.1 1% 1/6W MF 402-HF
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVIN_S0_LCDBKLT_BUF
PPVOUT_S0_LCDBKLT_SW
CRITICAL C9701 10UF 20% 25V X5R 805
PLACEMENT_NOTE=Place near L9701
R9701 100 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near PPVOUT_S0_LCDBKLT_SW
D9701 DX022-SM STPS1H100MF
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near C9710
PLACEMENT_NOTE=Place near J9000
Q9701 FDC5612 SSOT6
BOOST_FET_CNTL
BKL_VIN
CRITICAL C9709 2.2UF 10% 100V X7R 1210
CRITICAL C9710 2.2UF 10% 100V X7R 1210
4 PLACEMENT_NOTE=Place near C9709
XW9701 SM
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9701
C9702 0.1UF 10% 25V X5R 402
BOOST_SINK
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9709 and Q9701
R9704 100 1% 1/16W MF-LF 402
R9702 0.4 1% 1/16W MF 402
R9715 0.4 1% 1/16W MF 402
XW9702 SM
GND_BKL_PWRGND_X
BKL_VREF_4V9
R9731 187K 1% 1/16W MF-LF 402
BKLT_EN
BKL_SYNC
BKLT_PLL
R9734 0 5% 1/16W MF 402
BKL_VSYNC
R9707 3.01K 1% 1/16W MF-LF 402
C9703 1UF 10% 10V X5R 402
C9713 0.1UF 10% 25V X5R 402
R9705 100K 1% 1/16W MF-LF 402
R9706 10K 5% 1/16W MF-LF 402
U9701 QFN GOSHAWK6P
VIN
VREF DRV
ENA ISWSEN
VSYNC ISEN1
ISET ISEN2
RT ISEN3
SSTCMP ISEN4
DIM ISEN5
LPF ISEN6
LRT VSEN
GNDA THRM_PAD
*R9702 AND R9715 PIN 1 SHOULD BE PLACED NEAR C9709 PIN 2
C9712 47PF 5% 16V CERM 402 NOSTUFF
BKL_ISWSEN
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
PPVOUT_S0_LCDBKLT
VOLTAGE=30V
MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.5 mm
R9717 10.2 0.1% 1/10W TF 402
LED_RETURN_6
R9718 10.2 0.1% 1/10W TF 402
LED_RETURN_5
R9719 10.2 0.1% 1/10W TF 402
LED_RETURN_4
R9720 10.2 0.1% 1/10W TF 402
LED_RETURN_3
R9721 10.2 0.1% 1/10W TF 402
LED_RETURN_2
R9722 10.2 0.1% 1/10W TF 402
LED_RETURN_1
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
PLACEMENT_NOTE=Away from Q9701
R9708 100K 1% 1/16W MF-LF 402
R9709 1K 1% 1/16W MF-LF 402
R9703 2.0M 5% 1/16W MF-LF 402
BKL_SSTCMP_RC
C9705 0.01UF 20% 16V CERM 402
BKL_PWM_RC
R9733 0 5% 1/16W MF-LF 402
C9706 0.0022UF 10% 50V CERM 402 NOSTUFF
C9714 1UF 10% 10V X5R 402 NOSTUFF
BKL_PWR_EN_L
CRITICAL Q9702 NTUD3127CXXG SOT-963 N-CHN
LCD_BKL_PWM
CRITICAL Q9702 NTUD3127CXXG SOT-963 P-CHN
BKL_VREF_IN_4V9
R9700 100K 1% 1/16W MF-LF 402
R9710 10K 1% 1/16W MF-LF 402
R9711 30.1K 1% 1/16W MF-LF 402
BKL_VREF_4V9
R9713 0 5% 1/16W MF-LF 402
BKLT_PLL_NOT
BKL_LPF
BKL_LRT
R9714 10K 5% 1/16W MF-LF 402
C9707 2.2UF 20% 6.3V CERM 402-LF
BKL_LRT_RC
C9708 0.1UF 10% 25V X5R 402
R9727 75K 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Away from Q9701
GND_BKL_PWRGND
BKL_VSEN
R9723 1.2M 1% 1/16W MF-LF 603
R9724 71.5K 1% 1/16W MF-LF 402
PPVOUT_S0_LCDBKLT

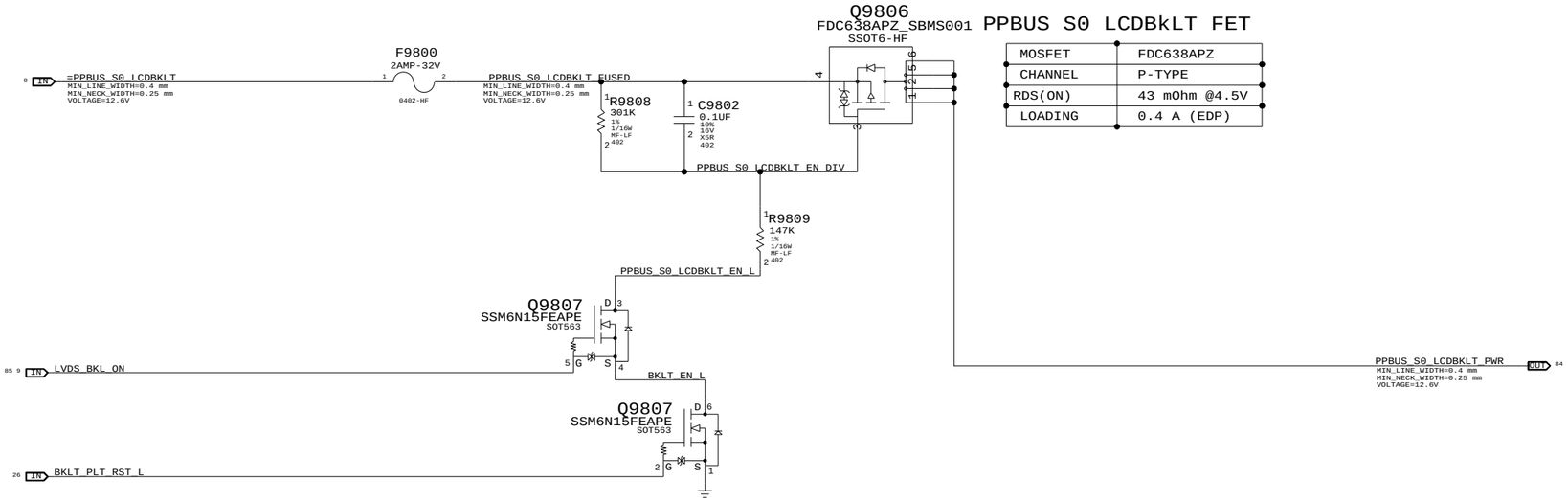
*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

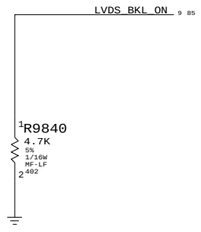
LCD BACKLIGHT DRIVER

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 84 OF 96	





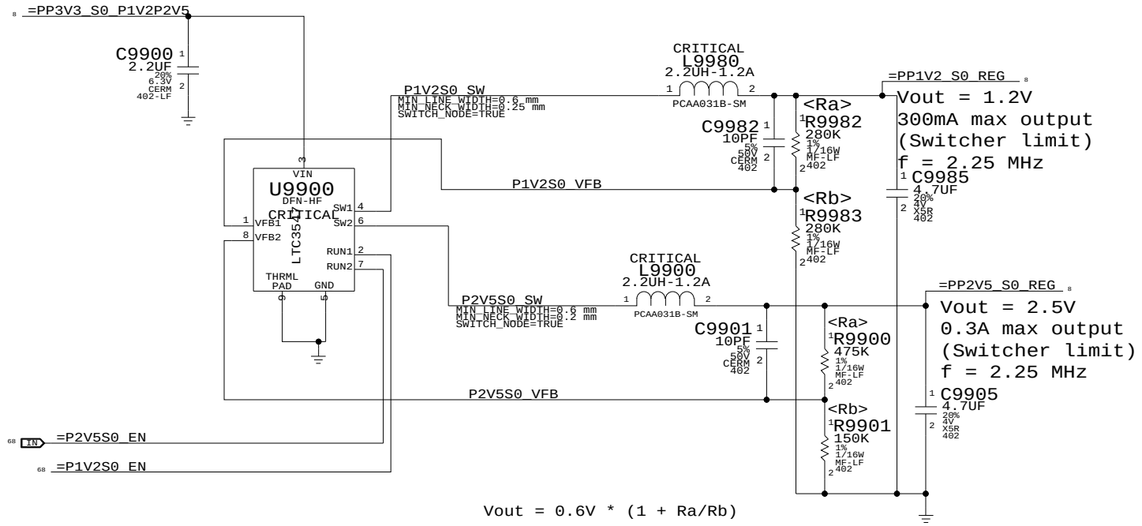
LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 85 OF 96	

2.5V/1.2V S3 Switcher



Vout = 0.6V * (1 + Ra/Rb)

Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 86 OF 96	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 43 62
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 43
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 62
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 62
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 27
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 62
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 62
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 62
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	62
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	62

CPU/FSB Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 87 OF 96

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 88 OF 96	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	70
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	70
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 70
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 70
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 70
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 70
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	70
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	70
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	31 95
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	31 95
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 31
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 31
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 31
	PCIE_90D	PCIE	PCIE_FW_R2D_P	36
	PCIE_90D	PCIE	PCIE_FW_R2D_N	36
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 36
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 36
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	36
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 32 95
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 32 95
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 32
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 32
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 32
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 32
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 70
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 70
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 31
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 36
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 36
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 32
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 32
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 25
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 25
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 25
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 25
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 25
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 25
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 25
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 80
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 80
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 80
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 80
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 25
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 25
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 83
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 83
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 83
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 83
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 83
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 83
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 25
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 25
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 39
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 39
	SATA_100D	SATA	SATA_HDD_R2D_P	39
	SATA_100D	SATA	SATA_HDD_R2D_N	39
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 39
	SATA_100D	SATA	SATA_HDD_D2R_N	20 39
	SATA_100D	SATA	SATA_HDD_D2R_C_P	39
	SATA_100D	SATA	SATA_HDD_D2R_C_N	39
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 39
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 39
	SATA_100D	SATA	SATA_ODD_R2D_P	7 39
	SATA_100D	SATA	SATA_ODD_R2D_N	7 39
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 39
	SATA_100D	SATA	SATA_ODD_D2R_N	20 39
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 39
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 39
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 89 OF 96

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 42 44 83
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 42 44 83
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26 83
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 26
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26 42
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 44
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 40
	USB_90D	USB	USB_EXTA_N	20 40
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 31
	USB_90D	USB	USB_CAMERA_N	20 31
USB_BT	USB_90D	USB	USB_BT_P	20 31
	USB_90D	USB	USB_BT_N	20 31
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
	USB_90D	USB	USB_TPAD_N	20 50
USB_IR	USB_90D	USB	USB_IR_P	20 41
	USB_90D	USB	USB_IR_N	20 41
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 40
	USB_90D	USB	USB_EXTB_N	20 40
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 32
	USB_90D	USB	USB_EXCARD_N	20 32
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
	USB_90D	USB	USB_EXTC_N	9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 45
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 45
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 45
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 54
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 54
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 54
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 54
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 44
	SPI_55S	SPI	SPI_CLK	44 53
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 44
	SPI_55S	SPI	SPI_MOSI	44 53
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 44
	SPI_55S	SPI	SPI_MISO_R	53
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 44
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT: 90 OF 96	

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND 18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R 18 34
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1 33 34
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 18 33
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC 18 33
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R 33
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 18 33
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0> 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0> 18 33
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 18 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 18 33
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK 18 33
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0> 18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1> 18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL 18 33
	ENET_MII_55S	ENET_MII	ENET_RESET_L 18 33
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0> 33 35
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0> 33 35

Ethernet Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE NONE	SHT 91 OF 96	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP

Port 2 Not Used

FW_P0_TPA_P 36 38
FW_P0_TPA_N 36 38
FW_P0_TPB_P 36 38
FW_P0_TPB_N 36 38
FW_P1_TPA_P 36 38
FW_P1_TPA_N 36 38
FW_P1_TPB_P 36 38
FW_P1_TPB_N 36 38

FireWire Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE	SHT	OF
NONE	92	96

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 7 45
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 7 45
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 45
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 45
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 45
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 45
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 45
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 45
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 45
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 45

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 61
	1TO1_DIFFPAIR		CHGR_CSI_N 61
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 61
	1TO1_DIFFPAIR		CHGR_CSO_N 61

SMC Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE NONE	SHT 93 OF 96	

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:
Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	80 83
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	80 83
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	80 83
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	80 83
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	80 83
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	80 83
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	80 83
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	80 83
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 79
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 79
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 79
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 79
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	79 80
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	79 80
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 79 80
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 79 80
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	79 80
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	79 80
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 79 80
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 79 80
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	81
DP_ML	DP_100D	DISPLAYPORT	**DP_ML_P<3..0>**	80 81
DP_ML	DP_100D	DISPLAYPORT	**DP_ML_N<3..0>**	80 81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	80 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	80 81

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	72 73
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	72 73
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	72 73
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	72 73
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	72 73
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	72 73
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	72 73
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	72 73
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	72 73
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	72 73
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	72 73
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	72 73
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	72 73
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	72 73
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	72 73
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	72 73
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	72 73
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	72 73
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	72 73
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	72 73
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	72 73
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	72 73
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	72 73
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	72 73
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	72 73
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	72 73
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	72 73
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	72 73
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	72 73
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	72 73
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	72 73
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	72 73
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	72 73
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	72 73
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	72 73
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	72 73
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	72 73
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	72 73
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	72 73
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	72 73
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	72 73
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	72 73
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	72 73
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	72 73
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	72 73
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	72 73
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	72 73

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M	76
CK505_CLK27M55	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M_SS	76
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	77 83
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	77 83
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	77 83
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	77 83
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	77 83
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	77 83
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_P<3..0>**	77 80
DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_N<3..0>**	77 80
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	77 80
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	77 80
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	80
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	80

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	72 74
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	72 74
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	72 74
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	72 74
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	72 74
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	72 74
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	72 74
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	72 74
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	72 74
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	72 74
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	72 74
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	72 74
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	72 74
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	72 74
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	72 74
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	72 74
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	72 74
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	72 74
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	72 74
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	72 74
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	72 74
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	72 74
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	72 74
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	72 74
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	72 74
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	72 74
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	72 74
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	72 74
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	72 74
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	72 74
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	72 74
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	72 74
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	72 74
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	72 74
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	72 74
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	72 74
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	72 74
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	72 74
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	72 74
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	72 74
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	72 74
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	72 74
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	72 74
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	72 74
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	72 74
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	72 74
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	72 74

GPU (G96) Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

SCALE NONE SHT 94 OF 96

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	35
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	35
U14D	SATA_100D	SATA	SATA_ODD_R2D_UF_P	39
U14F	SATA_100D	SATA	SATA_ODD_R2D_UF_N	39
U14H	SATA_100D	SATA	SATA_ODD_D2R_UF_P	39
U14J	SATA_100D	SATA	SATA_ODD_D2R_UF_N	39
U14K	SATA_100D	SATA	SATA_HDD_D2R_UF_P	39
U14M	SATA_100D	SATA	SATA_HDD_D2R_UF_N	39
U14L	SATA_100D	SATA	SATA_HDD_R2D_UF_P	39
U13P	SATA_100D	SATA	SATA_HDD_R2D_UF_N	39
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	78
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	47 65
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	47 65
CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	48
U12S	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	48
CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 48
U12G	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 48
GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	48
U13S	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	48
GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P	48 76
U12F	THERM_1TO1_55S	THERM	GPU_TDIODE_N	48 76
MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	48
U13R	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	48
MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 48
U13G	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 48
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	47
U15T	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	47
U15S	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	47
U15J	SENSE_1TO1_55S	SENSE	GPUISENS_N	47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	47 66
U15U	SENSE_1TO1_55S	SENSE	1V05CPU_N	47 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	47
U14P	SENSE_1TO1_55S	SENSE	DDRISNS_N	47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	47
U14T	SENSE_1TO1_55S	SENSE	P1V8GPU_N	47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	46
U16P	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	46
U16R		GND	GND	
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
		SB_POWER	PP1V5_S0	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	
U13J	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	47
U13K	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	47

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
U16C (PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 32 89
U16D (PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 32 89
U16G (PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_P	31 89
U16F (PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_N	31 89
U16G	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	31
U16F	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	31
U16C	1TO1_DIFFPAIR		CHGR_CSI_R_P	61
U16D	1TO1_DIFFPAIR		CHGR_CSI_R_N	61
U16E	1TO1_DIFFPAIR		CHGR_CSO_R_P	46 61
U16F	1TO1_DIFFPAIR		CHGR_CSO_R_N	46 61
U18D (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	40
U18C (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	40
U17C (USB_EXTA)	USB_90D	USB	USB2_LT1_P	40
U18C (USB_EXTA)	USB_90D	USB	USB2_LT1_N	40
U17J (USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P	
U17K (USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N	
U17G (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	31
U17F (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	31
U17J	USB_90D	USB	CONN_USB2_BT_P	31
U17K	USB_90D	USB	CONN_USB2_BT_N	31
U17D	USB_90D	USB	USB_LT2_P	40
U17E	USB_90D	USB	USB_LT2_N	40
U16C	USB_90D	USB	USB2_EXCARD_CONN_P	7 32
U17C	USB_90D	USB	USB2_EXCARD_CONN_N	7 32
U18B	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	80
U18A	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	80
U18F MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	9 32
U18E	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	9 32
U18R PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	9 32
U18P	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	9 32
U18N PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	9 32
U18M	PCIE_90D	PCIE	PCIE_FC_D2R_N	9 32
U18J	PCIE_90D	PCIE	PCIE_FC_R2D_P	32
U18K	PCIE_90D	PCIE	PCIE_FC_R2D_N	32
U16B	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 32
U16A	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 32
U19D SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_P_OUT	7 57 58
U19C	DIFFPAIR	AUDIO	SPKRCONN_L_N_OUT	7 57 58
U20D SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_P_OUT	7 57 58
U20C	DIFFPAIR	AUDIO	SPKRCONN_S_N_OUT	7 57 58
U19B SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_P_OUT	7 57 58
U19A	DIFFPAIR	AUDIO	SPKRCONN_R_N_OUT	7 57 58
U20B	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	57
U20A	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	57
U26D	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	57
U26C	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	57
U26B	DIFFPAIR	AUDIO	SPKRAMP_S_P_OUT	57
U26A	DIFFPAIR	AUDIO	SPKRAMP_S_N_OUT	57

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Project Specific Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE: NONE	SHT 95 OF 96	

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	14 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M99_MLB SYNC_DATE=01/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0

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