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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT REV. A

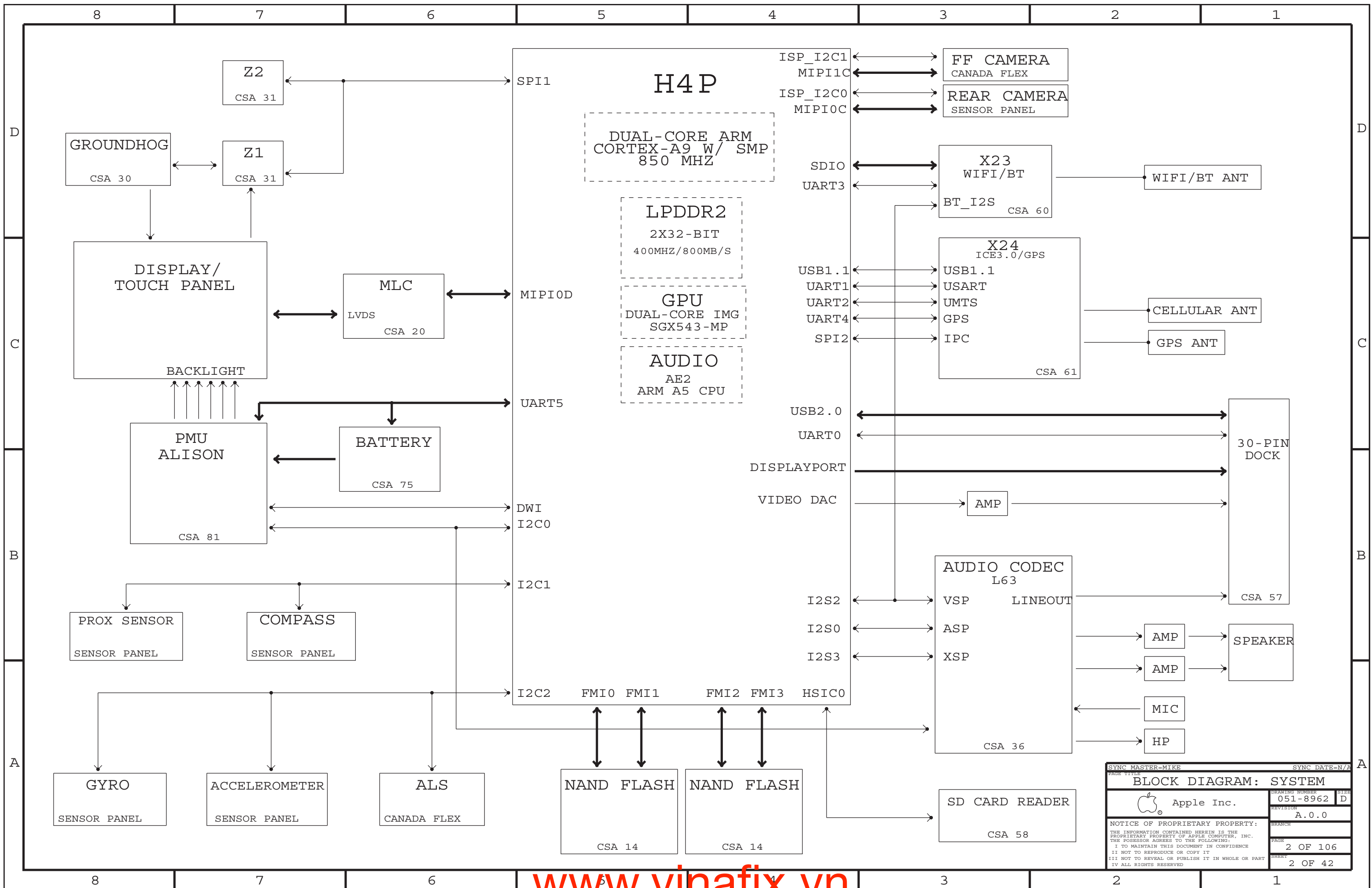
REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0001052699	PRODUCTION RELEASED		2011-01-10

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE
1	1	TABLE OF CONTENTS		MIKE	N/A	32	73	POWER: ALIASES		YOSH	N/A
2	2	BLOCK DIAGRAM: SYSTEM		MIKE	N/A	33	75	POWER: BATTERY CONNECTOR		YOSH	N/A
3	5	BOM TABLE		MIKE	N/A	34	81	POWER: PMU		YOSH	N/A
4	6	AP: MAIN		JAMES	N/A	35	82	POWER: PMU		YOSH	N/A
5	7	AP: I/Os		JAMES	N/A	36	83	POWER: 3.3V VR		YOSH	N/A
6	8	AP: NAND		JAMES	N/A	37	90	DEBUG AND MISC		MIKE	N/A
7	9	AP: TV,DP,MIPI		JAMES	N/A	38	93	FCT/ICT TEST/BRACKETS		MIKE	N/A
8	10	AP: PWR		JAMES	N/A	39	100	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
9	11	AP: PWR		JAMES	N/A	40	101	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
10	12	AP: MISC & ALIASES		JAMES	N/A	41	102	CONSTRAINTS: MLB RULES		MIKE	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES		JAMES	N/A	42	106	CONSTRAINTS: RF RULES		MIKE	N/A
12	14	NAND		JONATHAN	N/A						
13	17	VIDEO: DISPLAY PORT		JAMES	N/A						
14	20	VIDEO: MLC		MIKE	N/A						
15	21	VIDEO: MLC ALIASES		MIKE	N/A						
16	22	VIDEO: LVDS CONNECTOR		ALEX	N/A						
17	30	GRAPE: GROUNDHOG, CONN, BOOST		RAMSIN	N/A						
18	31	GRAPE: Z1, Z2		RAMSIN	N/A						
19	36	AUDIO: L63 CODEC		LENG	N/A						
20	37	AUDIO: SPEAKER AMP		LENG	N/A						
21	38	AUDIO: HEADPHONE OUT		LENG	N/A						
22	39	AUDIO: BLANK		LENG	N/A						
23	42	AUDIO: DETECT/MIC BIAS		LENG	N/A						
24	43	AUDIO: HP/MIC FILTERS		LENG	N/A						
25	54	CONNECTOR: CANADA FLEX CONN, SENSOR PANEL ALIASES		MARK B.	N/A						
26	55	CONNECTOR: CANADA FLEX FILTERS		MARK B.	N/A						
27	56	CONNECTOR: SENSOR PANEL CONNECTOR		MARK B.	N/A						
28	57	IO FLEX: DOCK COMPONENTS		JAMES	N/A						
29	59	IO FELX: B2B Connector		JAMES	N/A						
30	60	CONNECTOR: X23 WIFI/BT		MIKE	N/A						
31	61	CONNECTOR: X24 CELLULAR/GPS		MIKE	N/A						

DRAWING TITLE		CHOPIN MLB	
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ABBREV-DRAWING



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BLOCK DIAGRAM: SYSTEM			
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE
16GB_PROD
32GB_PROD
64GB_PROD
BKLT_PLL
DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP
JTAG_TAP_NOT
SPEAKER
INTERNAL_MIC
PORTRAIT_DOCK
MLC_DEV
MLC_PROD
K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH, CHOPIN_AUDIO, MLB, K94	SCH1	
820-3069	1	PCBF, CHOPIN_AUDIO, MLB, K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE, GRAPE, MLB, K93/K94	FENCE1	
806-1397	1	CAN, GRAPE, MLB, K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE, CPU, MLB, K93/K94	FENCE2	
806-1399	1	CAN, CPU, MLB, K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE, NAND, MLB, K93/K94	FENCE3	
806-1401	1	CAN, NAND, MLB, K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DPC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DPC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DPC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

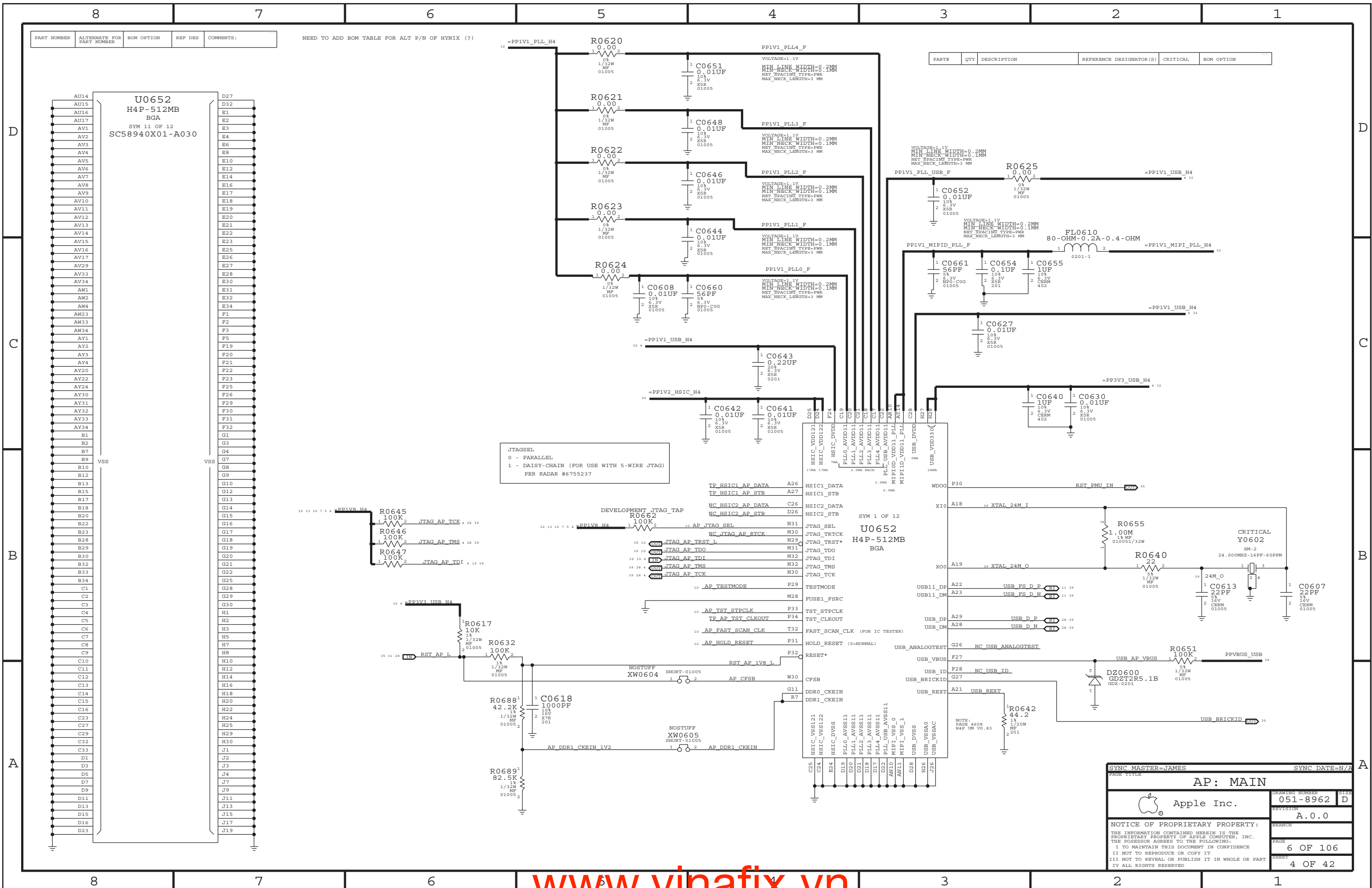
BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE		SYNC DATE=N/A	
BOM TABLE			
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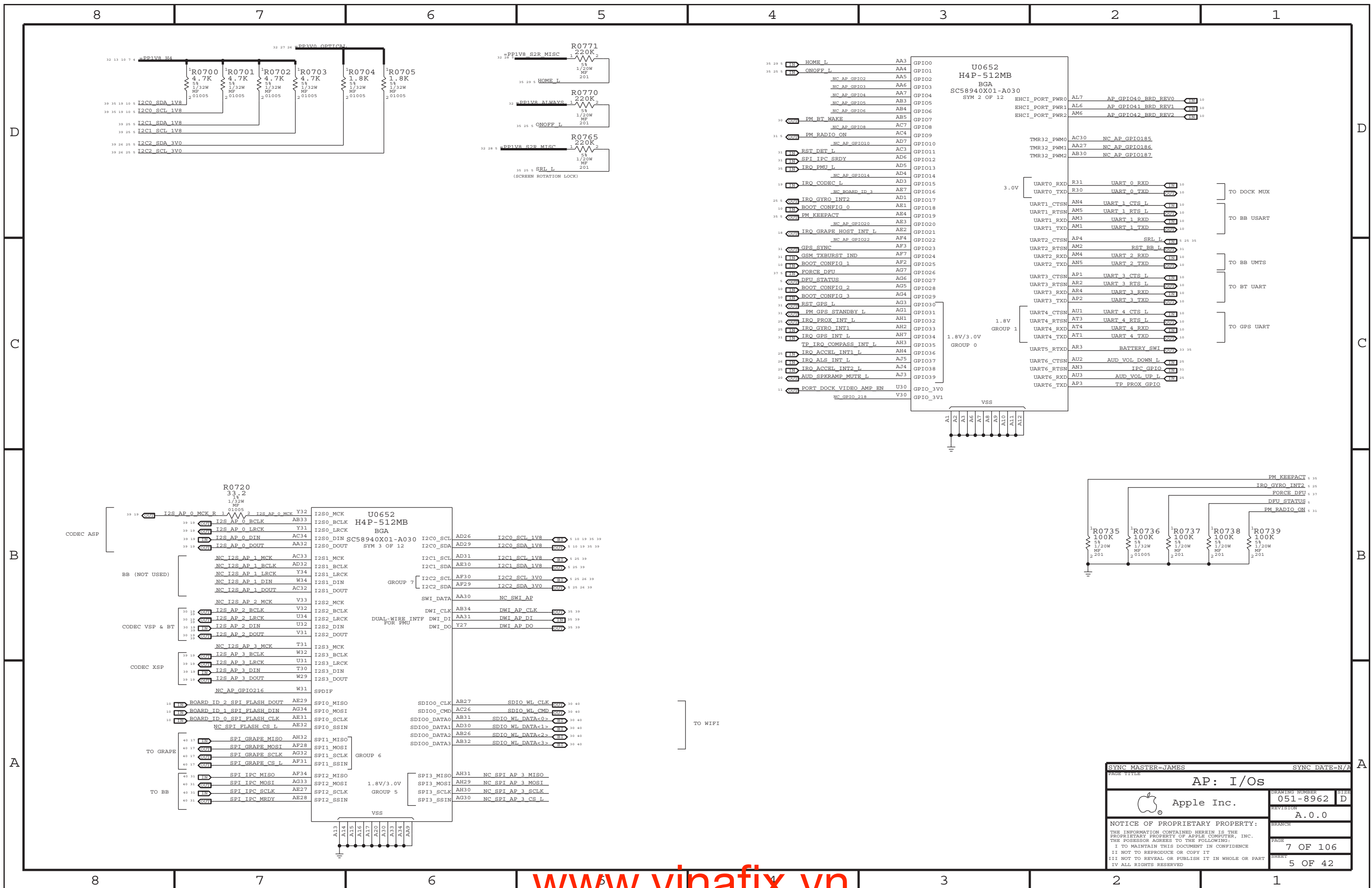
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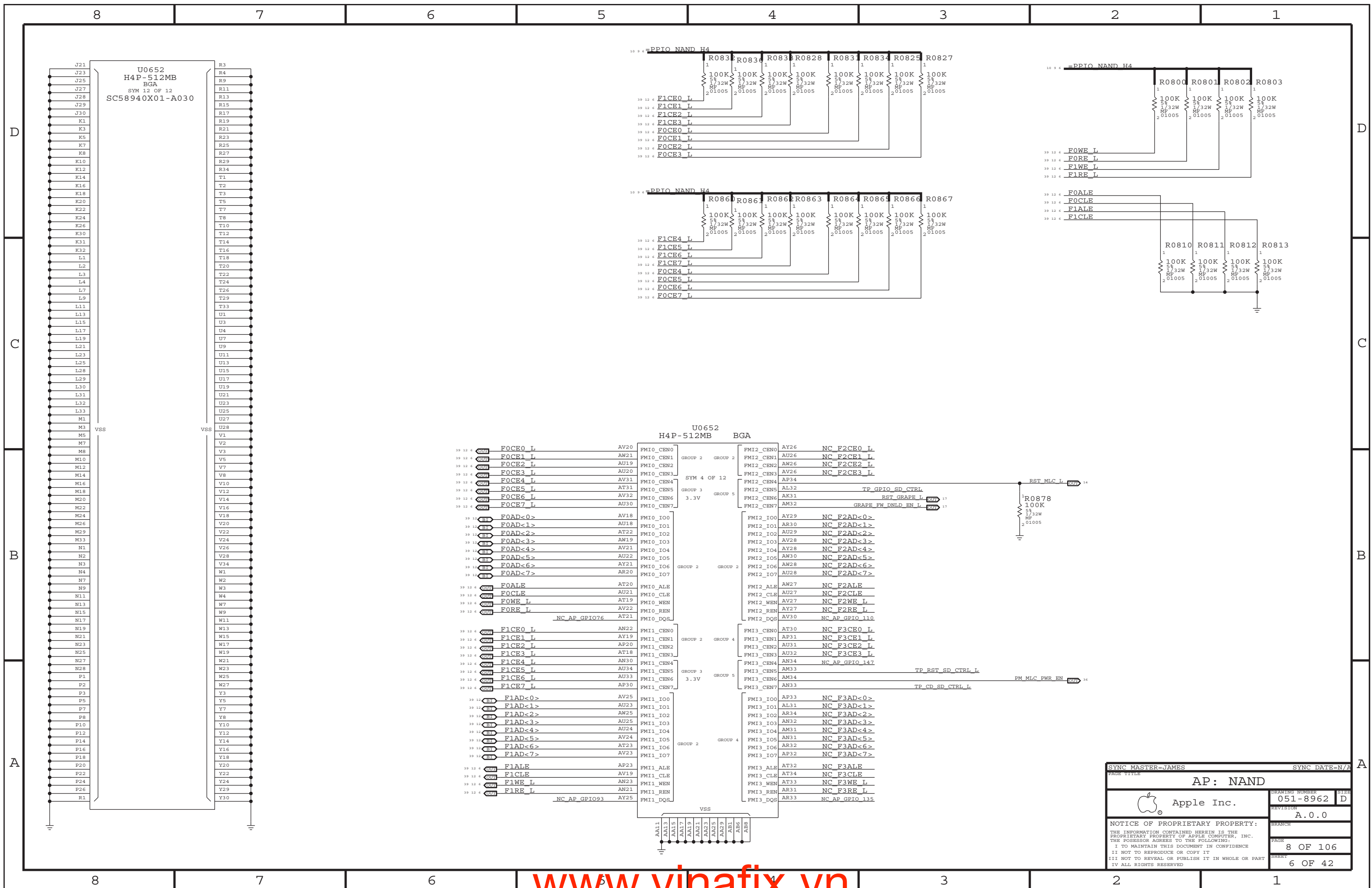
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U0652 H4P-512MB BGA

Pin	Signal	Pin	Signal
39 12 6	FOCE0_L	AV20	FMI0_CEN0
39 12 6	FOCE1_L	AW21	FMI0_CEN1
39 12 6	FOCE2_L	AU19	FMI0_CEN2
39 12 6	FOCE3_L	AU20	FMI0_CEN3
39 12 6	FOCE4_L	AV31	FMI0_CEN4
39 12 6	FOCE5_L	AT31	FMI0_CEN5
39 12 6	FOCE6_L	AV32	FMI0_CEN6
39 12 6	FOCE7_L	AU30	FMI0_CEN7
39 12 6	F0AD<0>	AV18	FMI0_IO0
39 12 6	F0AD<1>	AU18	FMI0_IO1
39 12 6	F0AD<2>	AT22	FMI0_IO2
39 12 6	F0AD<3>	AW19	FMI0_IO3
39 12 6	F0AD<4>	AV21	FMI0_IO4
39 12 6	F0AD<5>	AU22	FMI0_IO5
39 12 6	F0AD<6>	AY21	FMI0_IO6
39 12 6	F0AD<7>	AR20	FMI0_IO7
39 12 6	F0ALE	AT20	FMI0_ALE
39 12 6	F0CLE	AU21	FMI0_CLE
39 12 6	F0WE_L	AT19	FMI0_WEN
39 12 6	F0RE_L	AV22	FMI0_REN
39 12 6		AT21	FMI0_DQS
39 12 6	FICE0_L	AN22	FMI1_CEN0
39 12 6	FICE1_L	AY19	FMI1_CEN1
39 12 6	FICE2_L	AP20	FMI1_CEN2
39 12 6	FICE3_L	AT18	FMI1_CEN3
39 12 6	FICE4_L	AN30	FMI1_CEN4
39 12 6	FICE5_L	AU34	FMI1_CEN5
39 12 6	FICE6_L	AU33	FMI1_CEN6
39 12 6	FICE7_L	AP30	FMI1_CEN7
39 12 6	F1AD<0>	AV25	FMI1_IO0
39 12 6	F1AD<1>	AU23	FMI1_IO1
39 12 6	F1AD<2>	AW25	FMI1_IO2
39 12 6	F1AD<3>	AU25	FMI1_IO3
39 12 6	F1AD<4>	AU24	FMI1_IO4
39 12 6	F1AD<5>	AV24	FMI1_IO5
39 12 6	F1AD<6>	AT23	FMI1_IO6
39 12 6	F1AD<7>	AV23	FMI1_IO7
39 12 6	F1ALE	AP23	FMI1_ALE
39 12 6	F1CLE	AV19	FMI1_CLE
39 12 6	F1WE_L	AN23	FMI1_WEN
39 12 6	F1RE_L	AN21	FMI1_REN
39 12 6		AY25	FMI1_DQS

AP: NAND

Apple Inc.

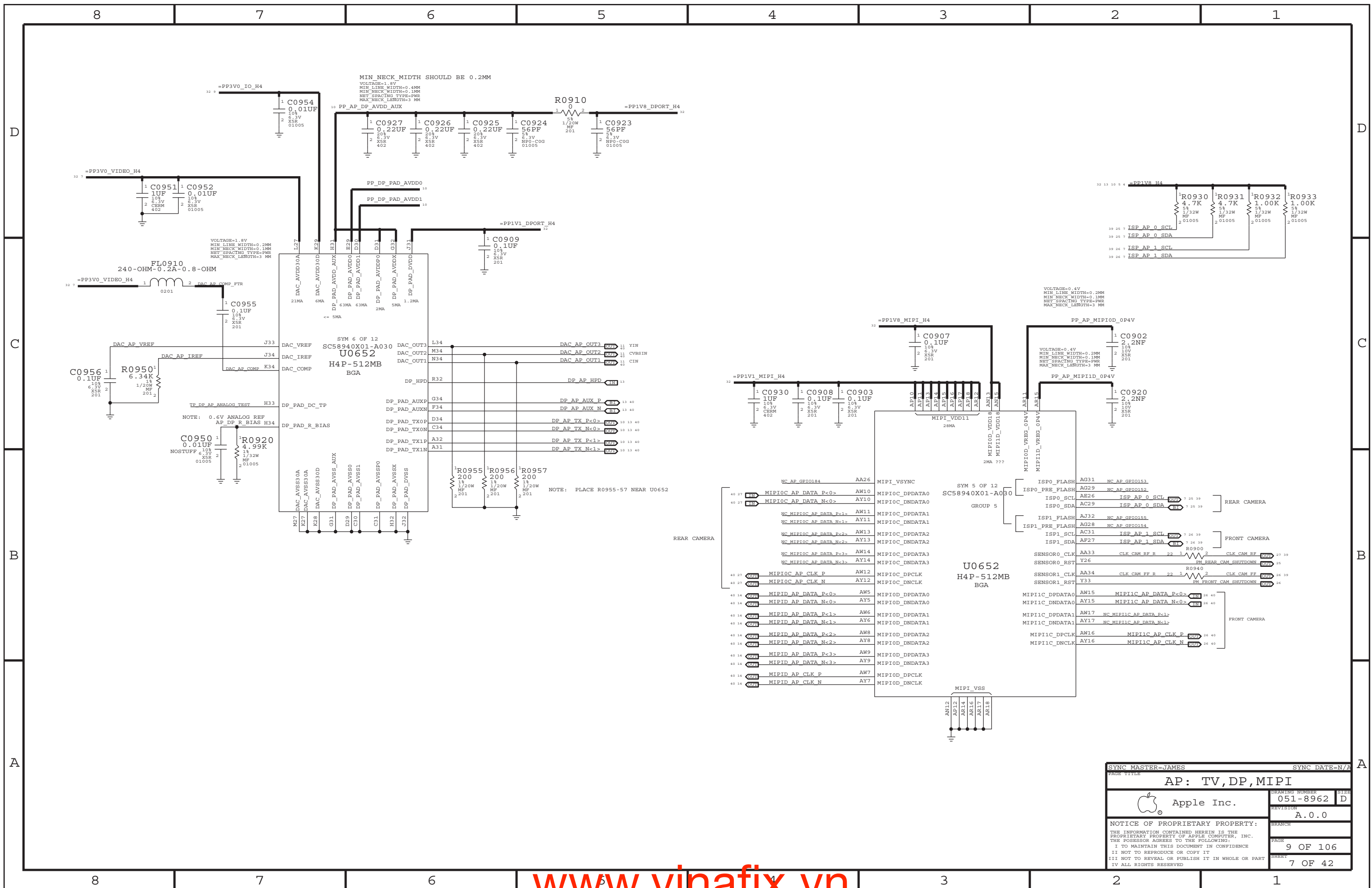
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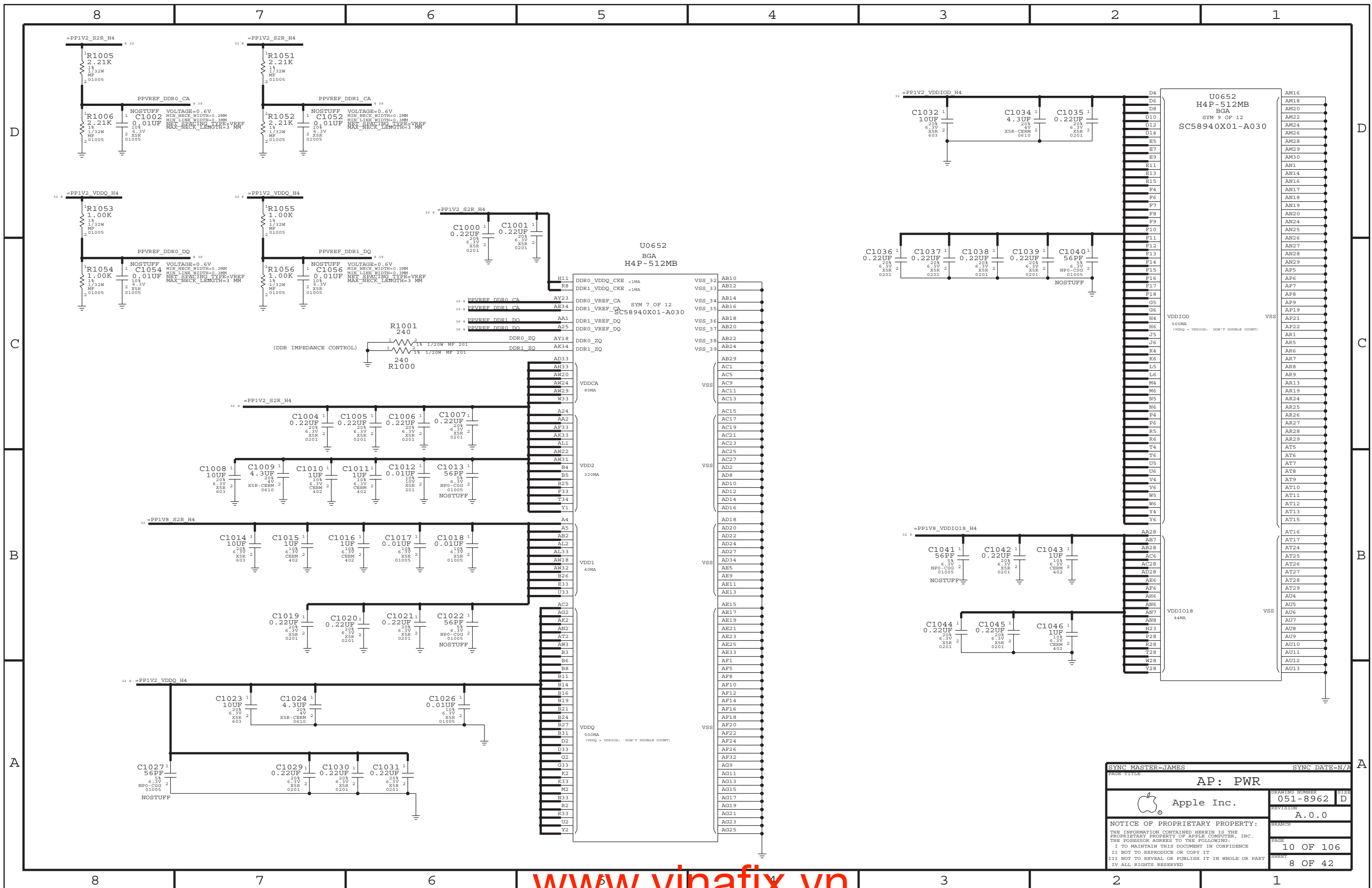
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PAGE TITLE			
AP: TV, DP, MIPI			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
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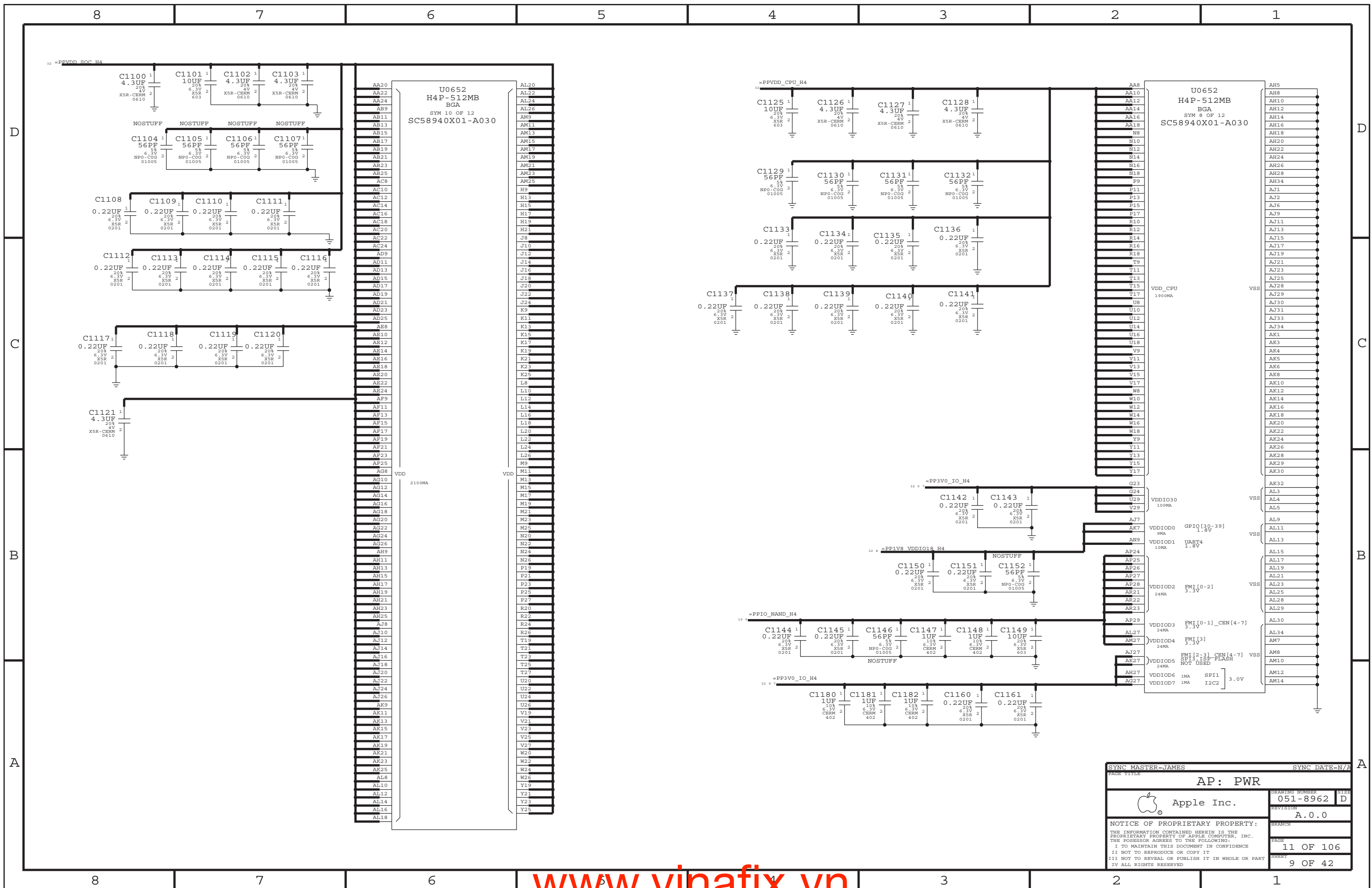


U0652
H4P-512MB
BGA
SYM 9 OF 12
SC58940X01-A030

U0652
BGA
H4P-512MB

SC58940X01-A030

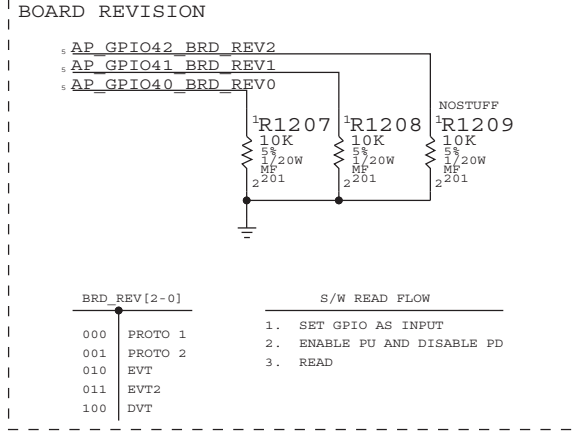
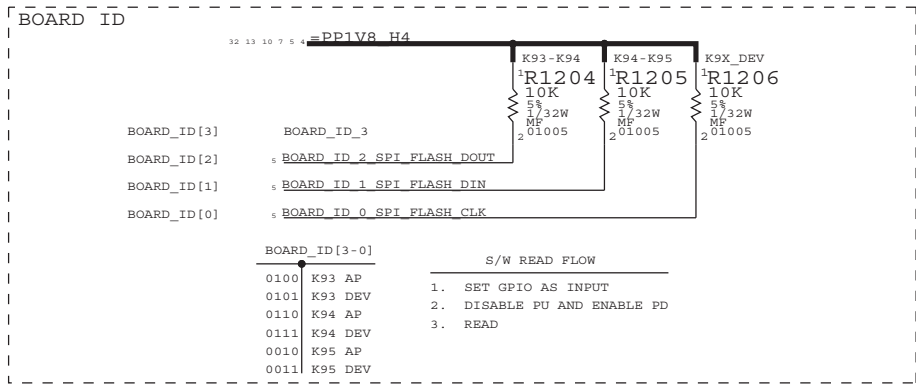
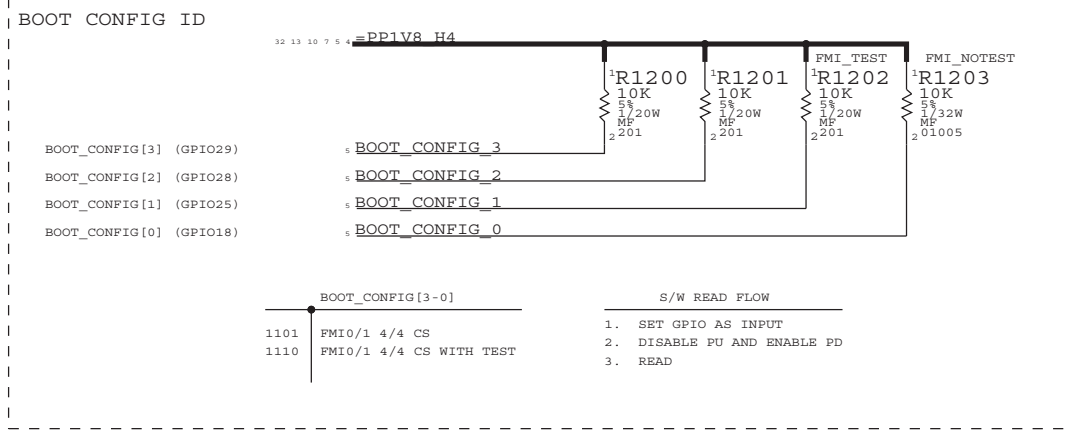
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H4P-512MB
BGA
SYM 10 OF 12
SC58940X01-A030

U0652
H4P-512MB
BGA
SYM 8 OF 12
SC58940X01-A030

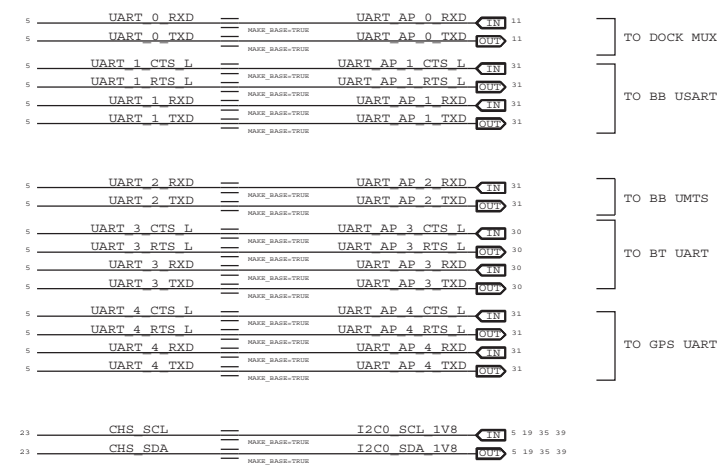
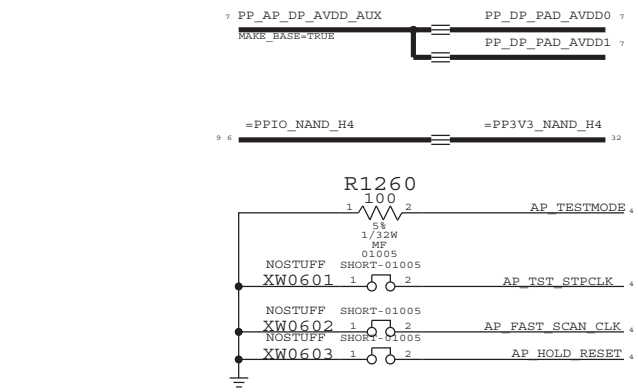
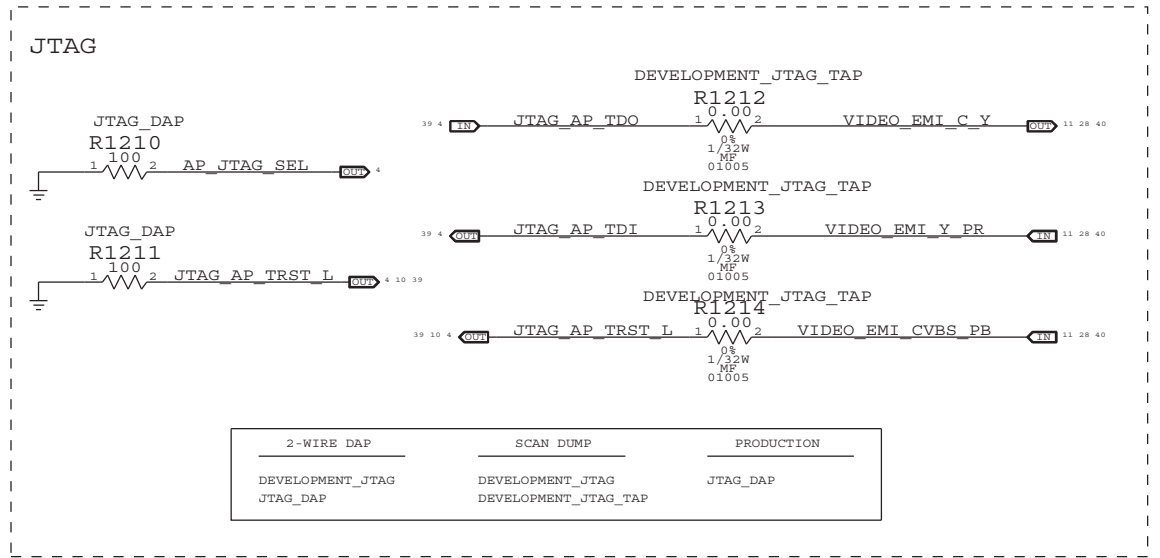
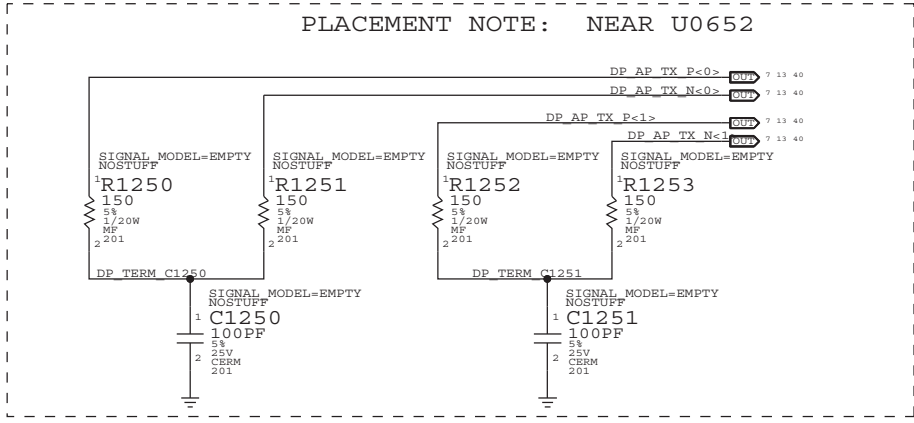
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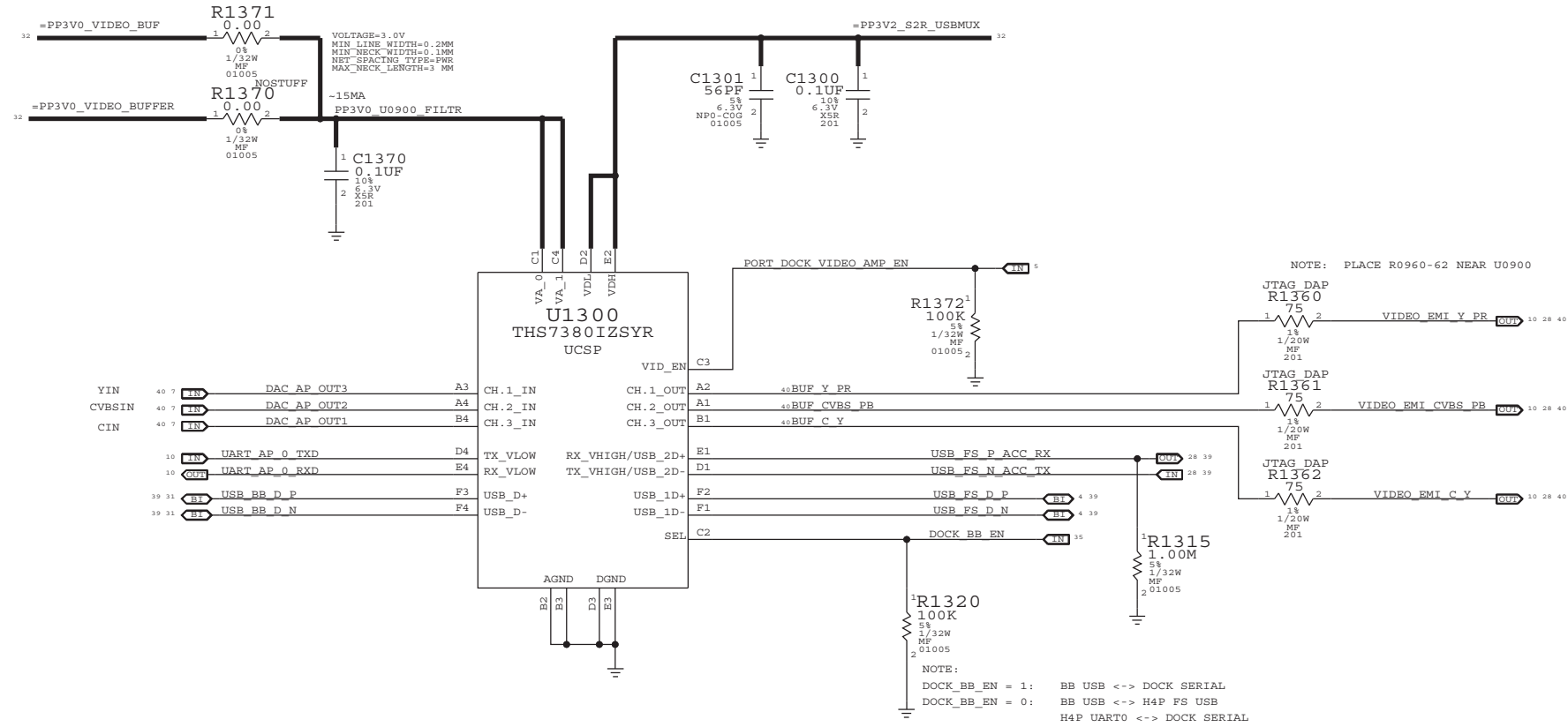
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0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FMII 2 CS
1001	FMII 4 CS
1010	FMII 4CS W/TEST
1011	RESERVED
1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

CURRENT SETTING ->



SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE			
AP: MISC & ALIASES			
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NOTE:
LDO3 PROVIDES 50MA TO BOTH H4P AND U1300
IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370



PAGE TITLE		SYNC DATE=N/A	
AP: VIDEO BUFFER, BB USB MUXES			
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16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

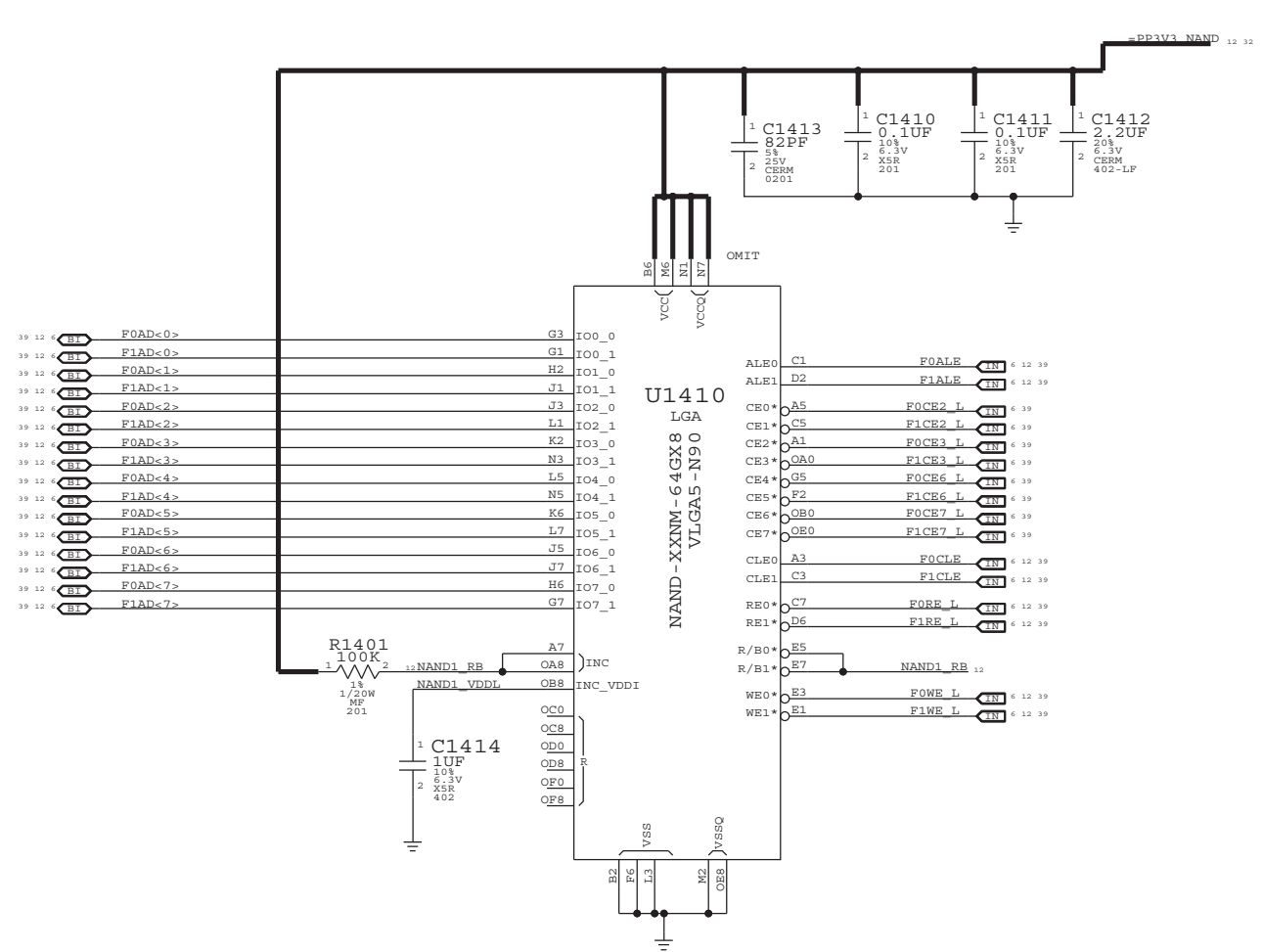
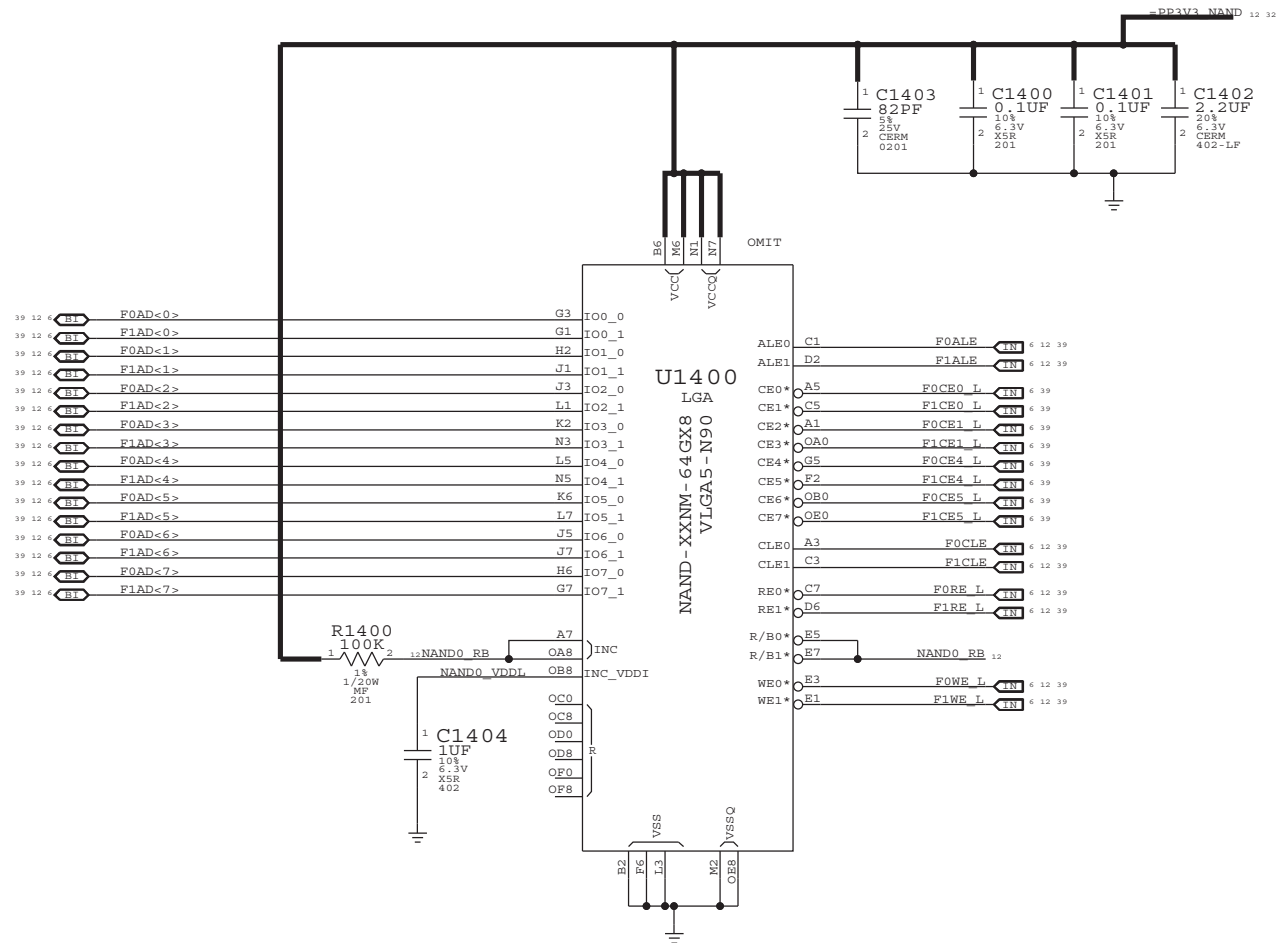
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

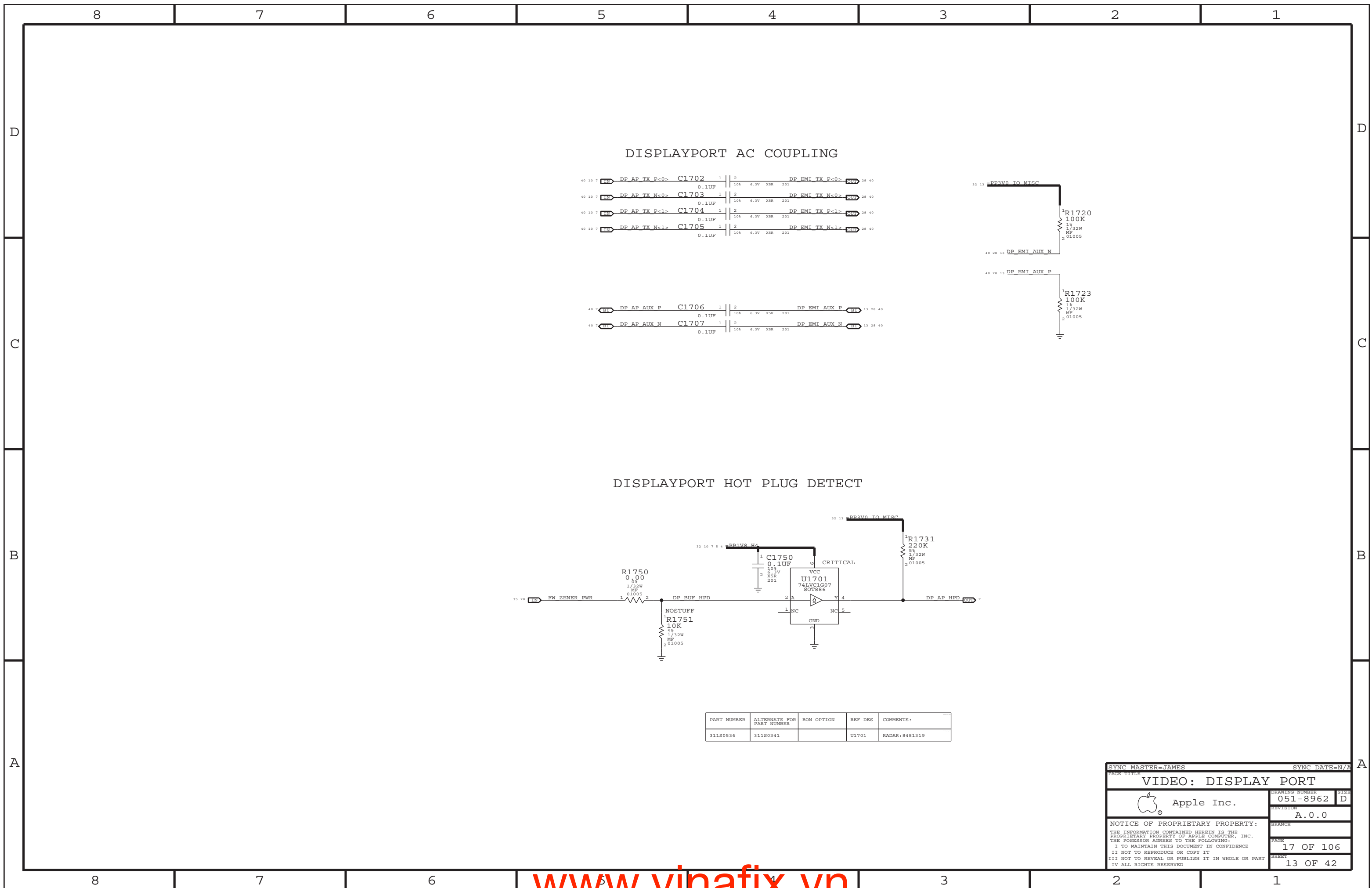
64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

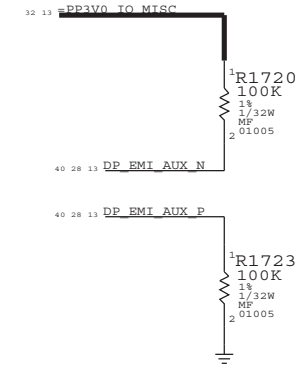
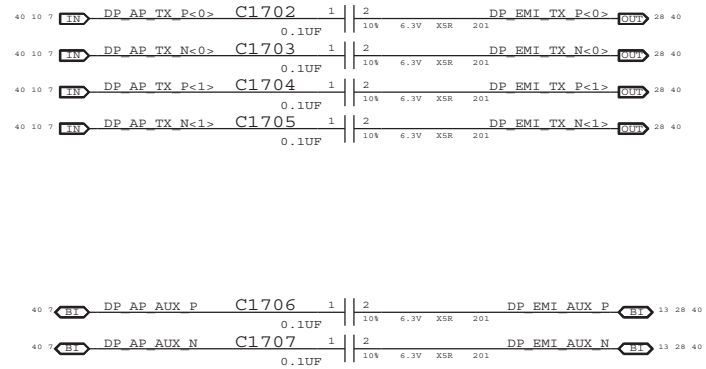
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335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN



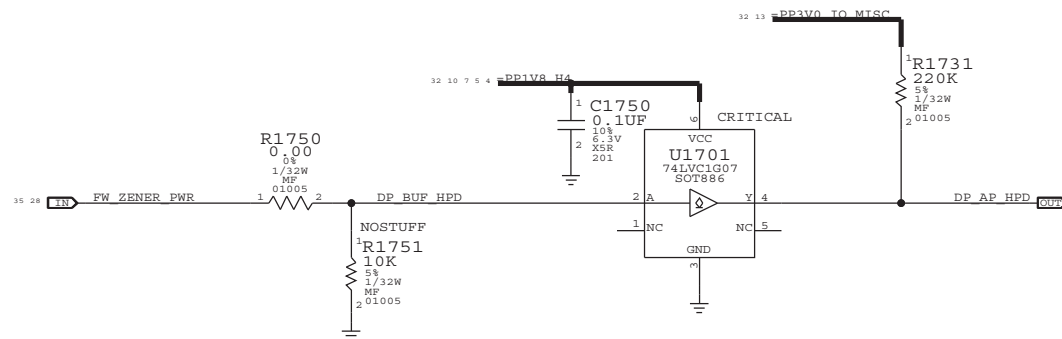
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DISPLAYPORT AC COUPLING



DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE VIDEO: DISPLAY PORT

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

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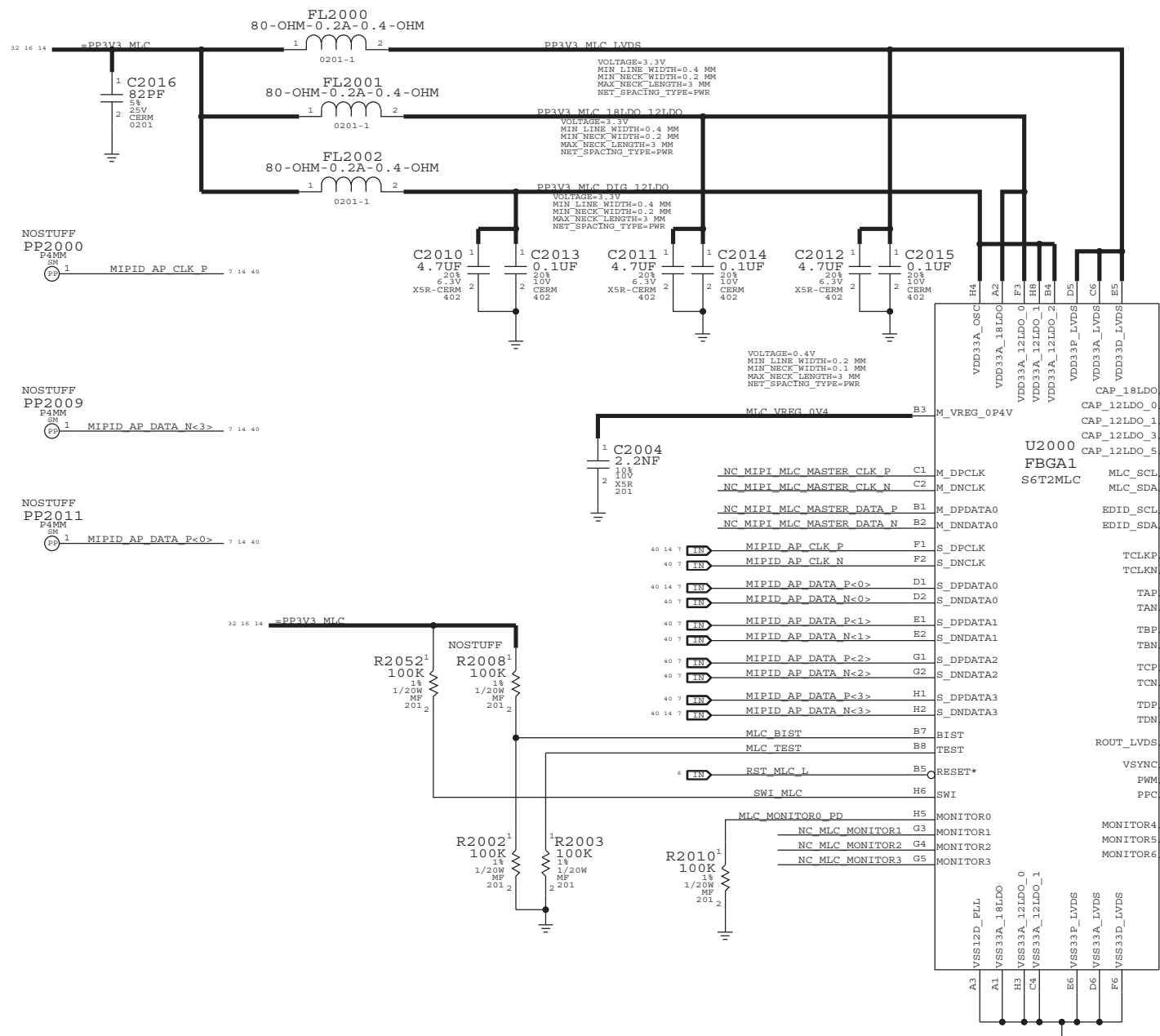
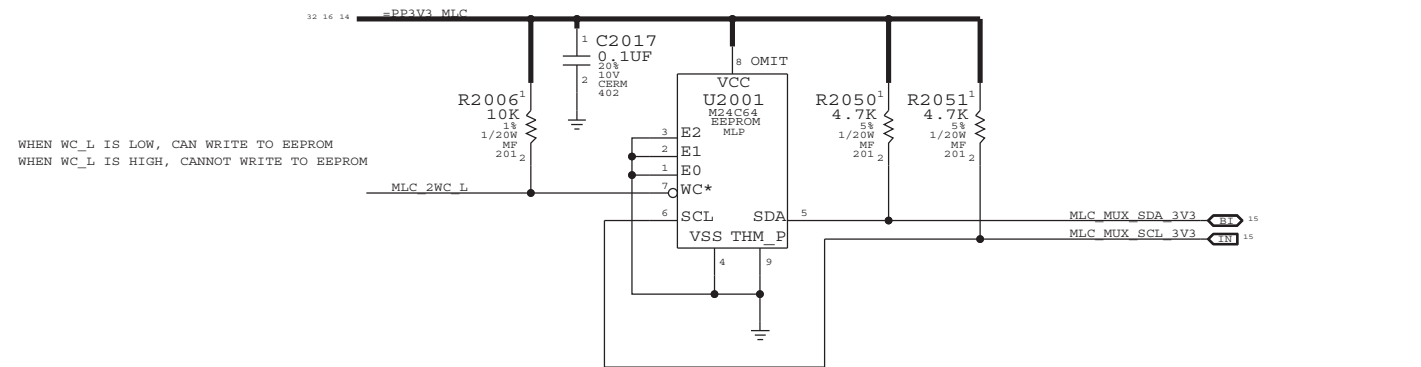
BRANCH

PAGE 17 OF 106

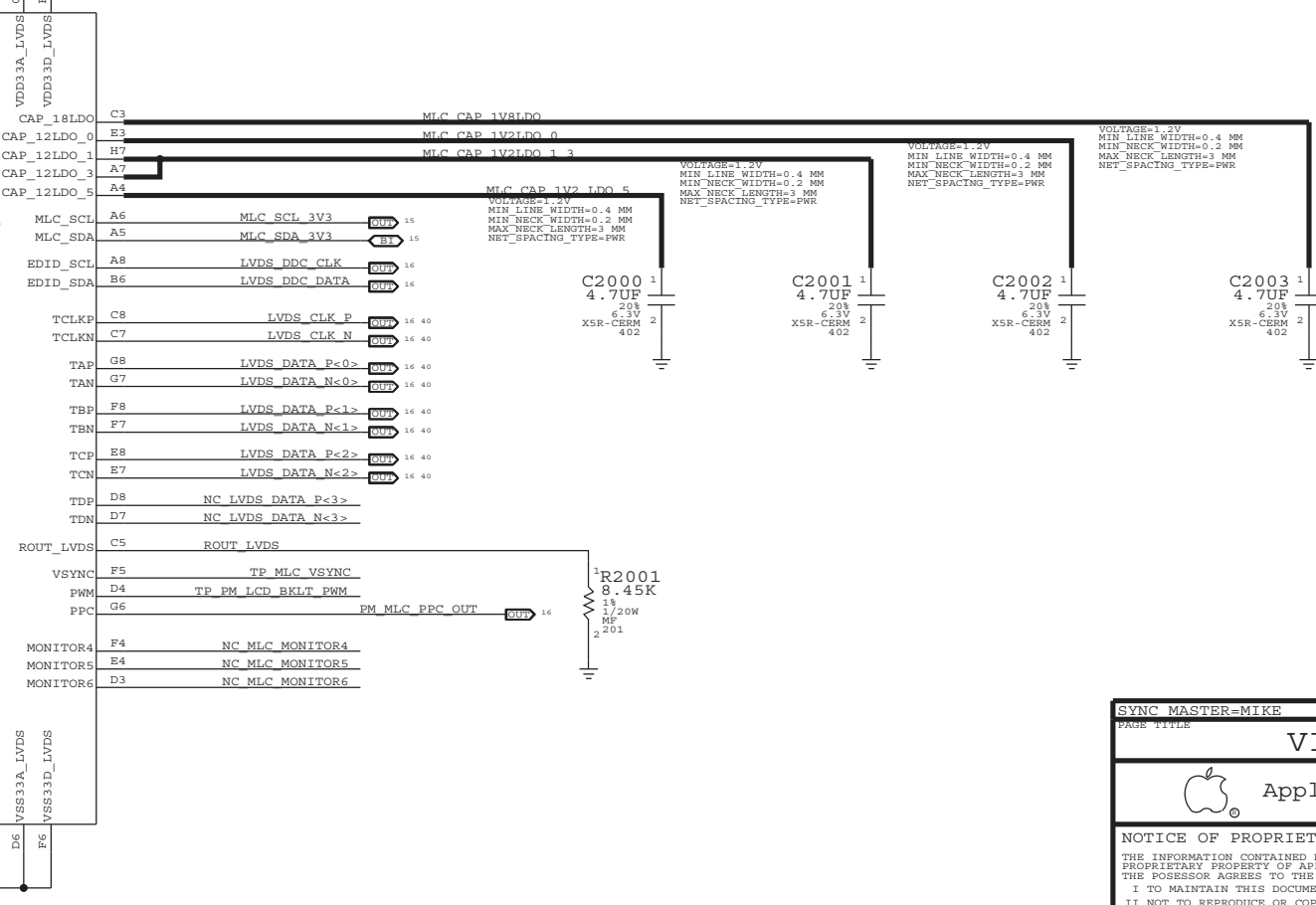
SHEET 13 OF 42

MLC EEPROM:RAW APN 335S0661

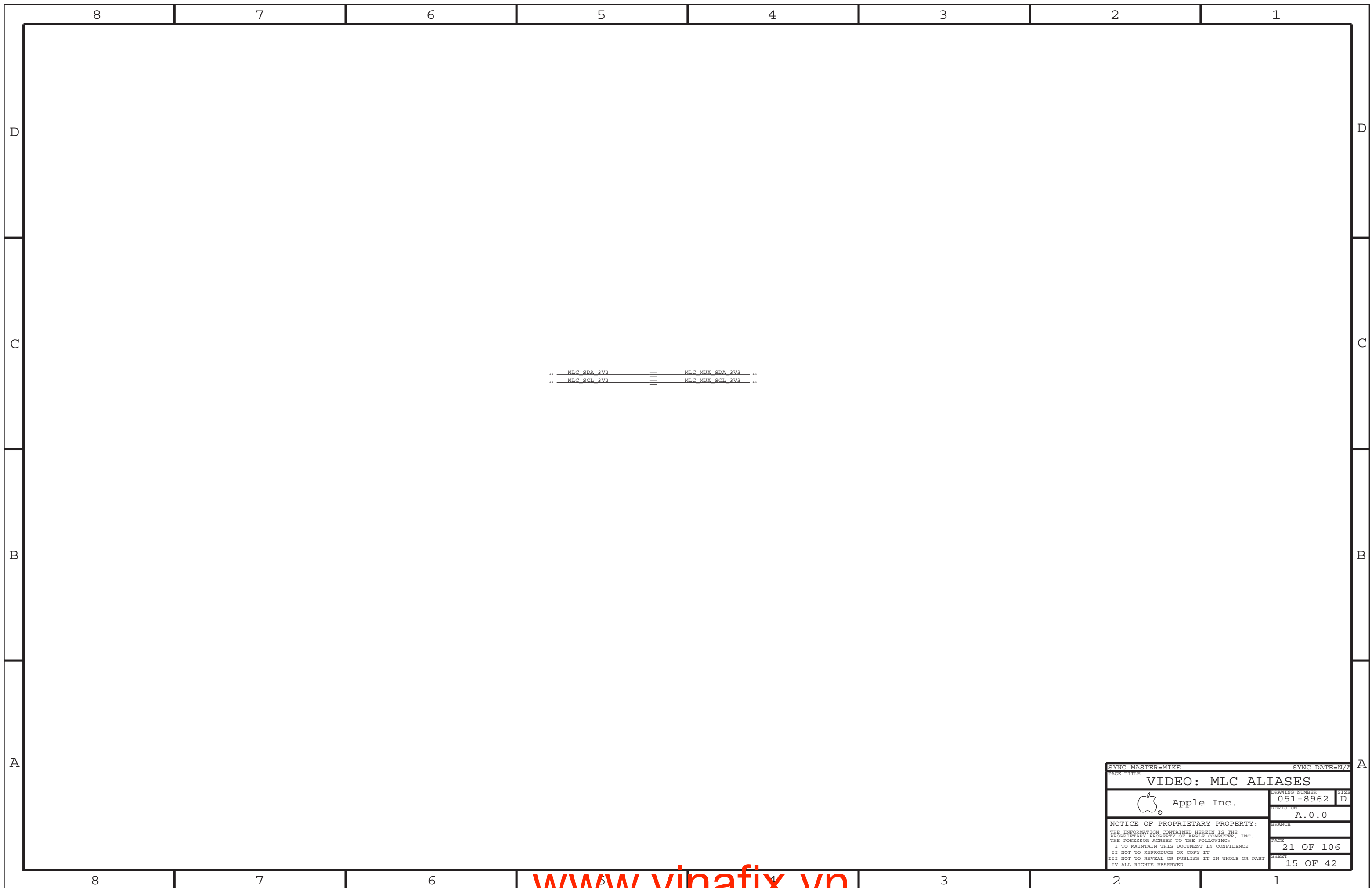
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
138S0652	138S0618			RADAR:8377307



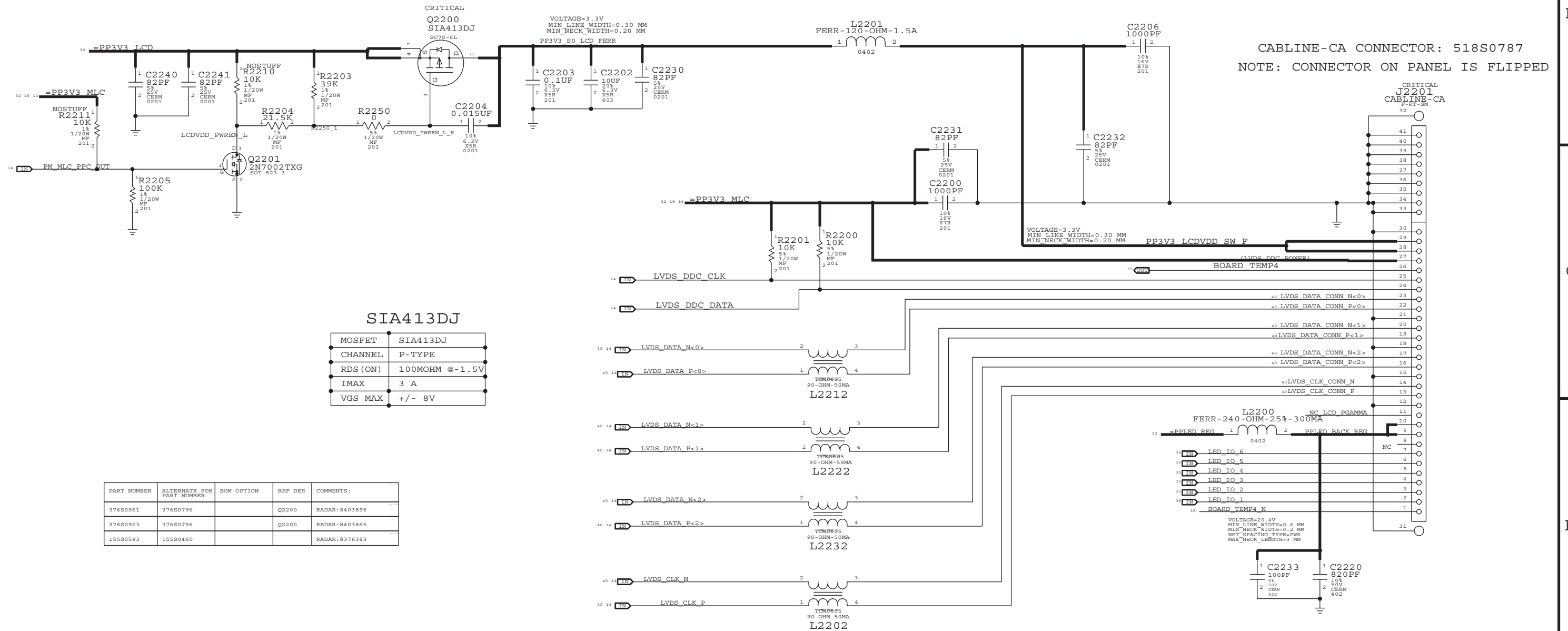
PAGE TITLE		SYNC DATE=N/A	
VIDEO: MLC			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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14 MLC_SDA_3V3 MLC_MUX_SDA_3V3 14
 14 MLC_SCL_3V3 MLC_MUX_SCL_3V3 14

SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE VIDEO: MLC ALIASES			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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LVDS CONNECTOR

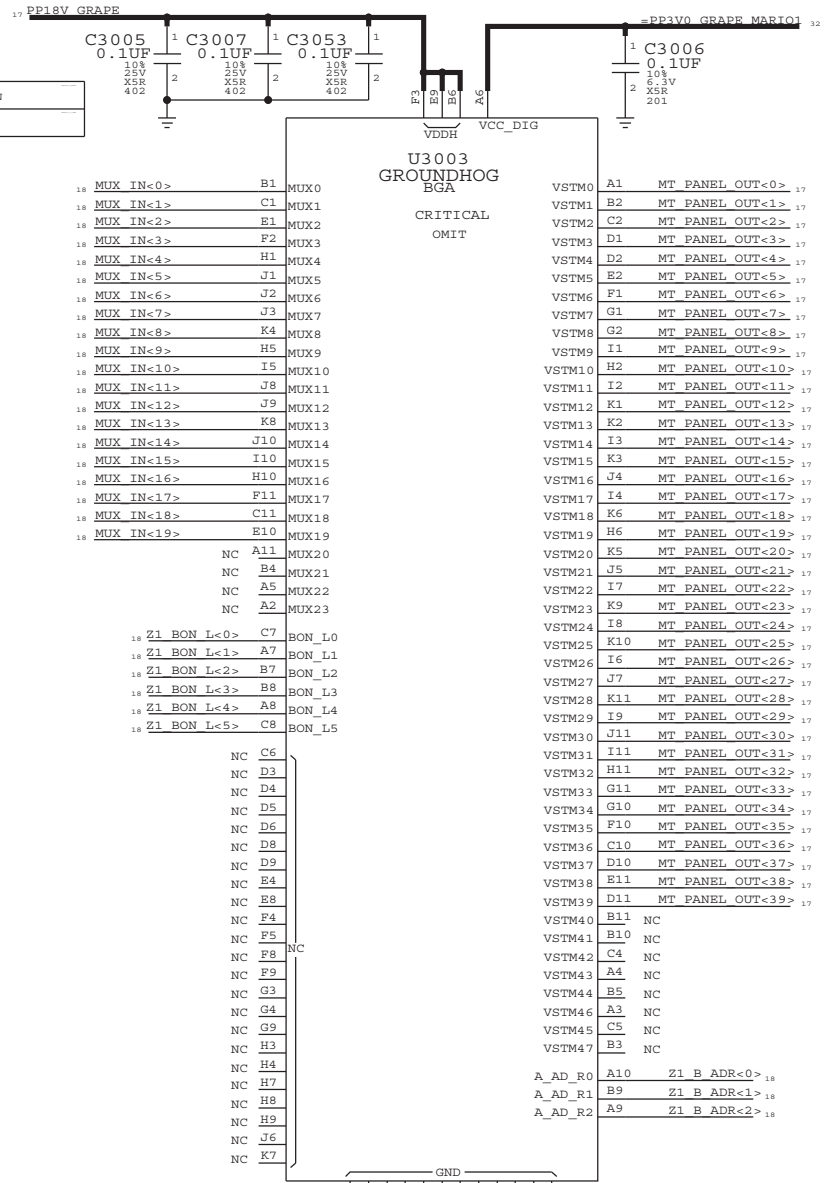


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

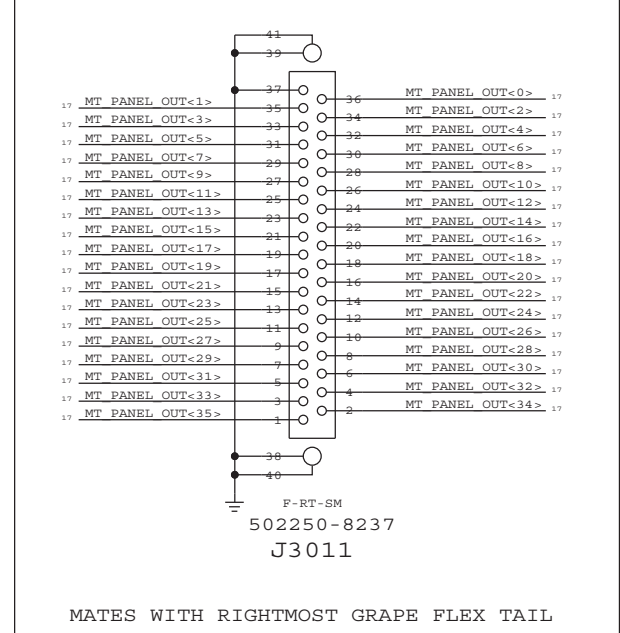
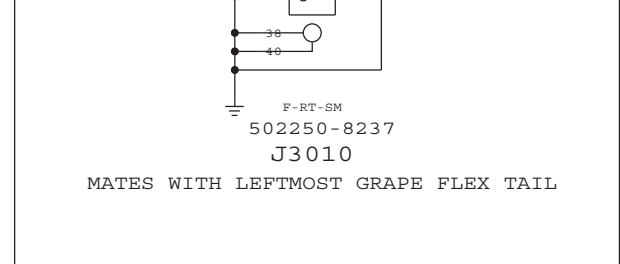
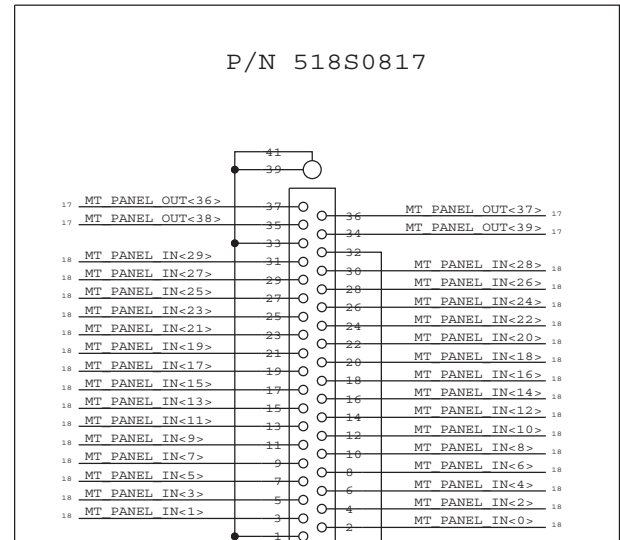
NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC MASTER=ALEX		SYNC DATE=N/A	
VIDEO: LVDS CONNECTOR			
Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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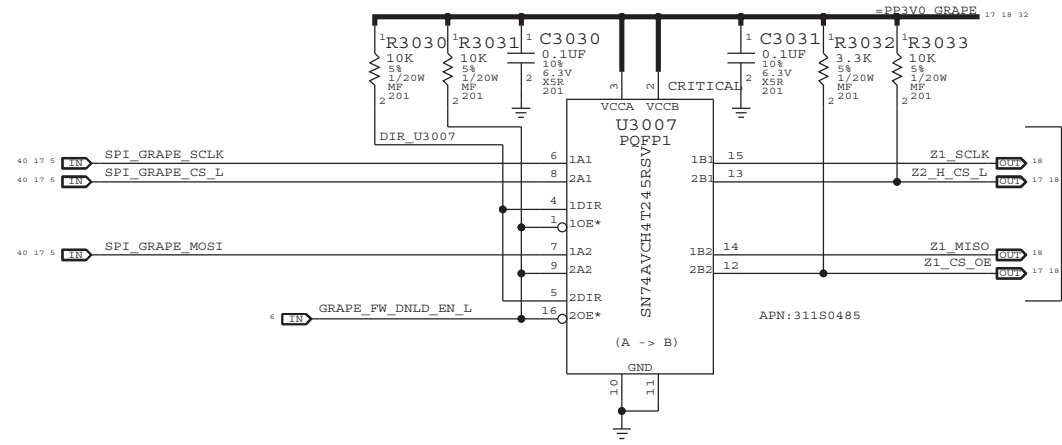
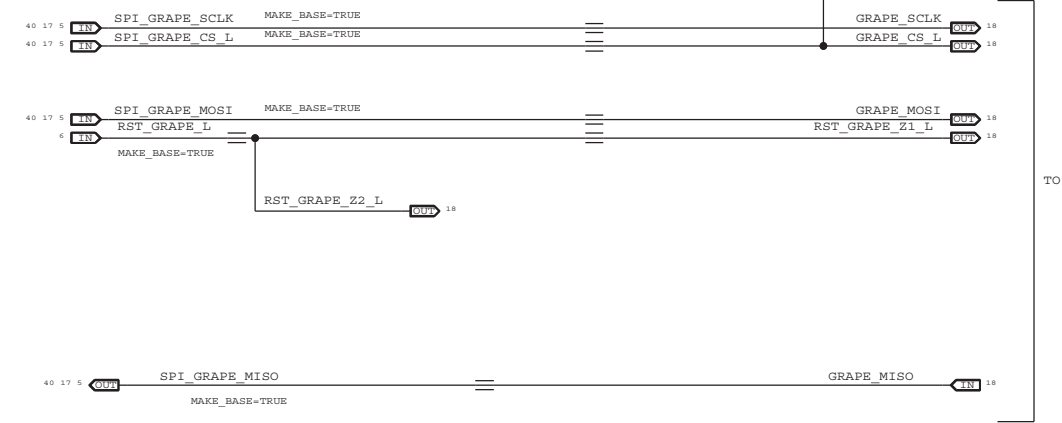
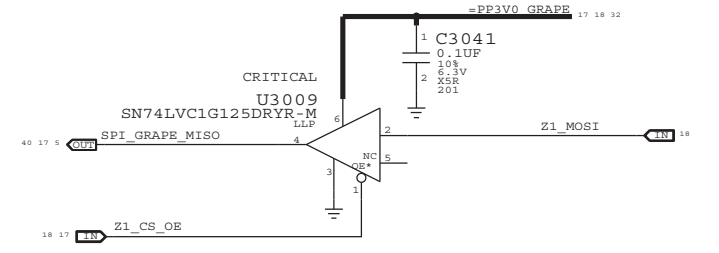
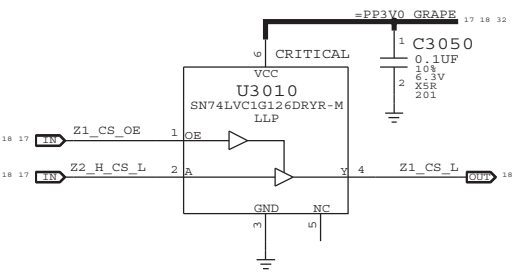
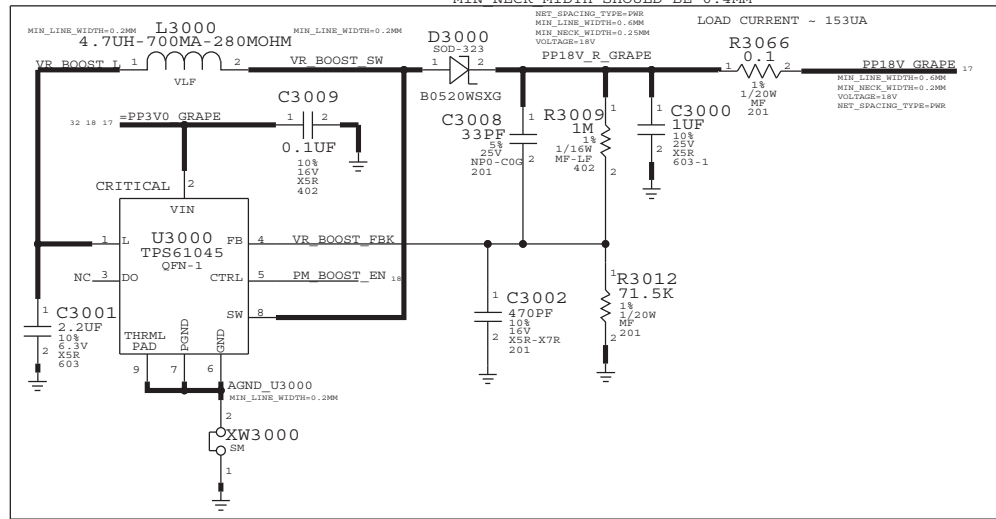
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	



CONNECTORS TO GRAPE FLEX



BOOST CONVERTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31150523	31150485		U3007	
31150524	31150533		U3009	
31150525	31150532		U3010	

SYNC MASTER=RAMSIN SYNC DATE=N/A

GRAPE: GROUNDHOG, CONN, BOOST

Apple Inc.

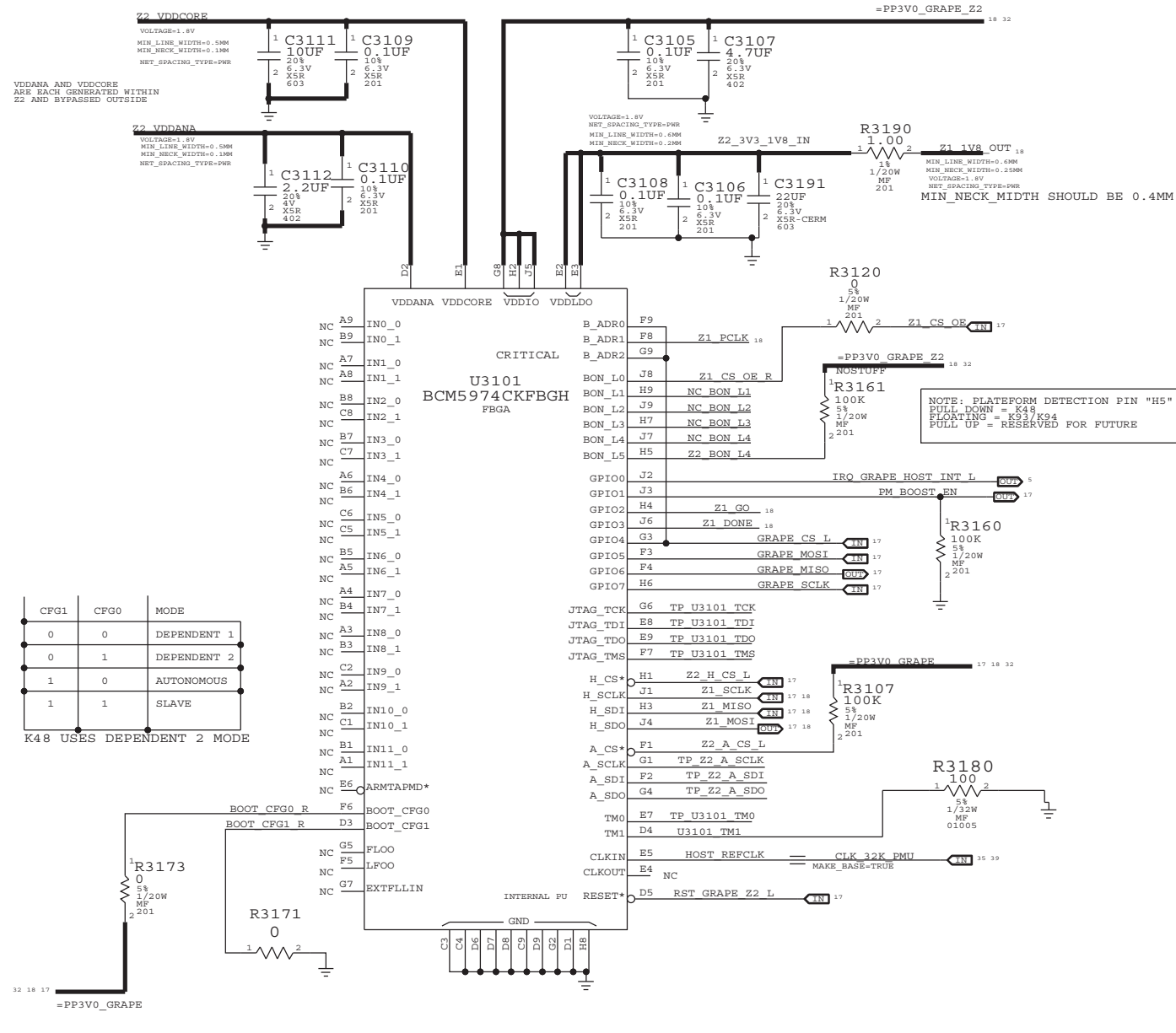
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REVISION: A.0.0

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PAGE: 30 OF 106 SHEET: 17 OF 42

ARM9 MCU (Z2 BASED)

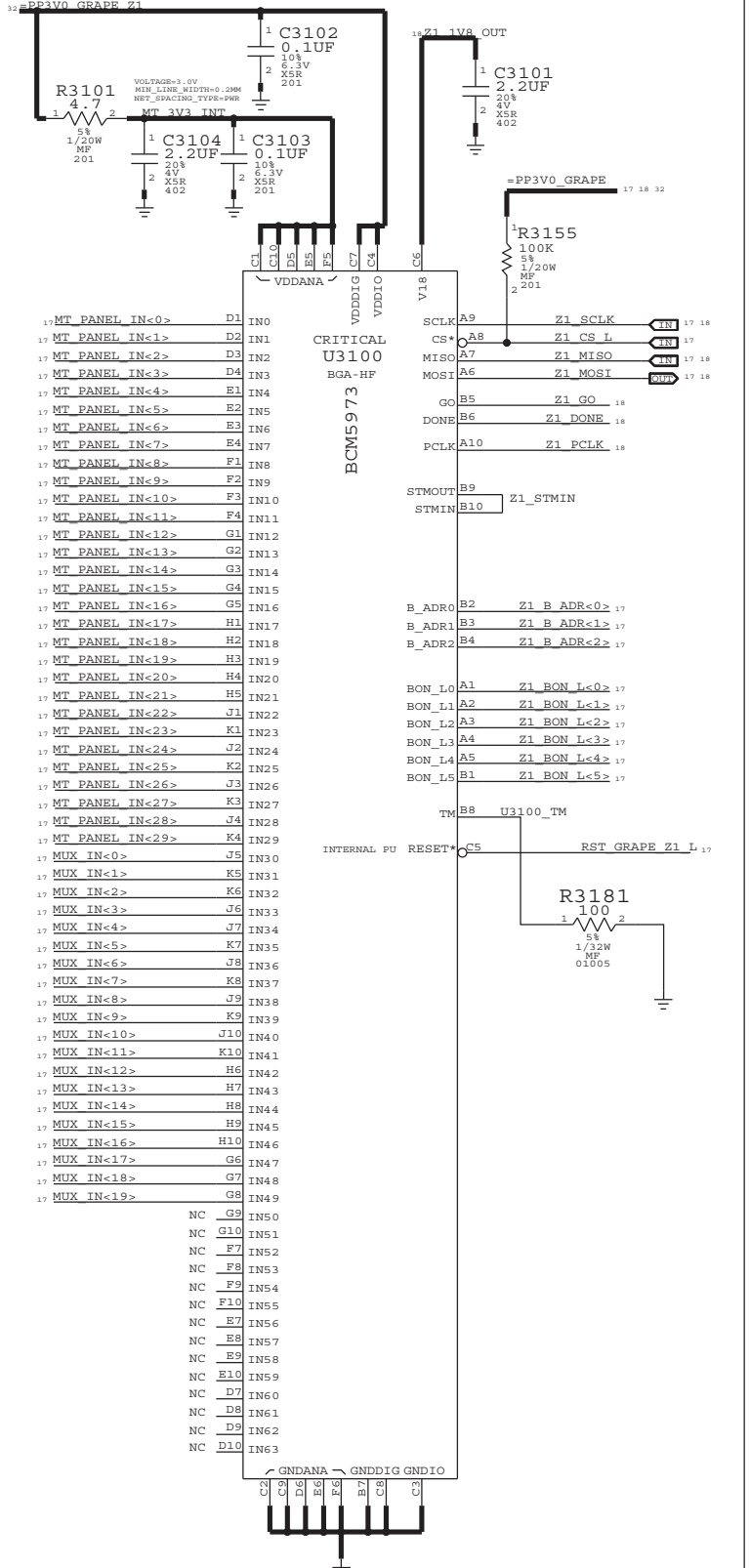


CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USBS DEPENDENT 2 MODE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR: 8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

ZEPHYR 1+ ASIC



SYNC MASTER=RAMSIN SYNC DATE=N/A

GRAPE: Z1, Z2

Apple Inc.

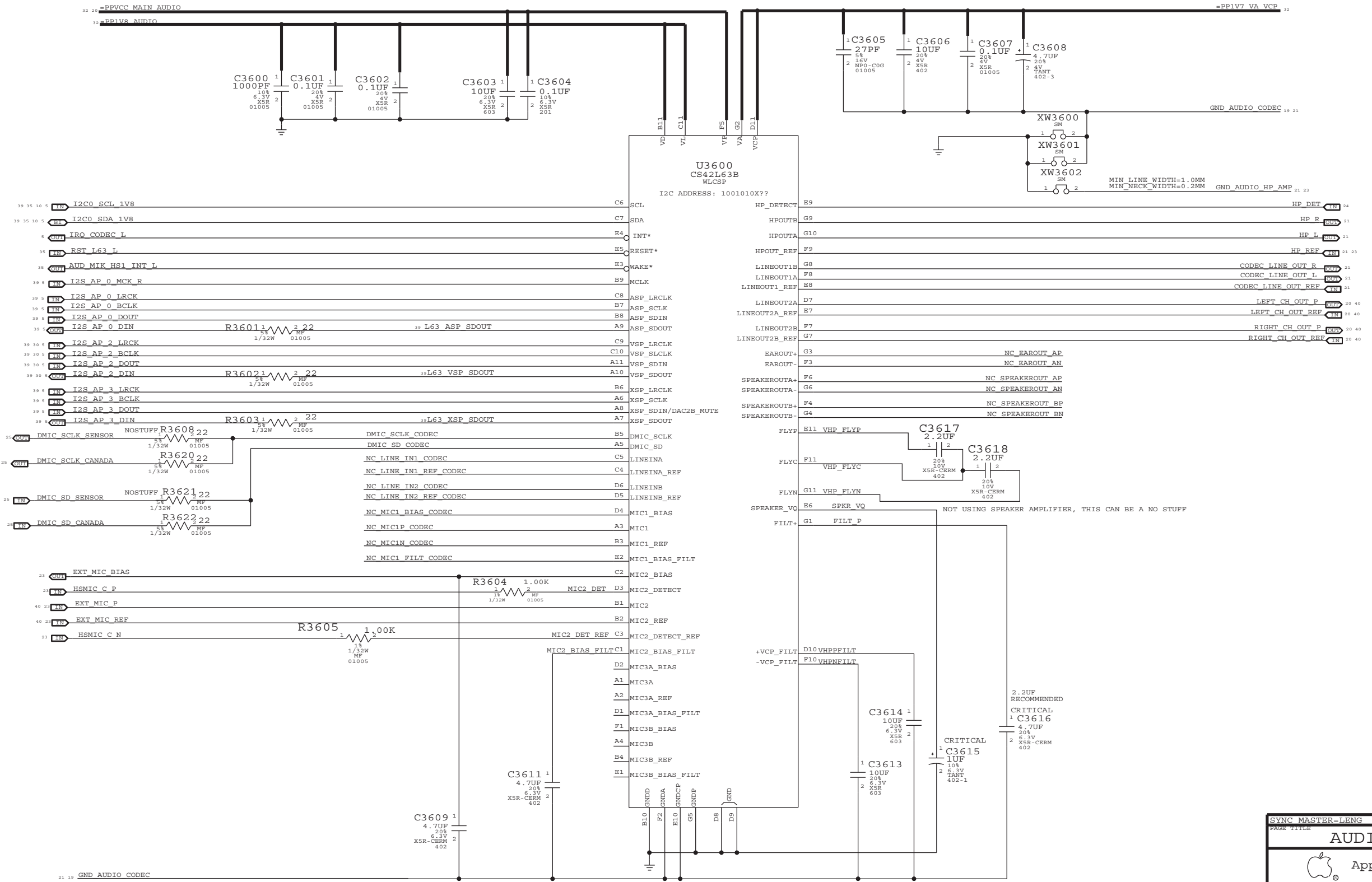
051-8962
REVISION: A.0.0

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L63 AUDIO CODEC

APN:338S0940



MIN LINE WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=75 MM

SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: L63 CODEC			
Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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		PAGE	36 OF 106
		SHEET	19 OF 42

SPEAKER AMPLIFIER

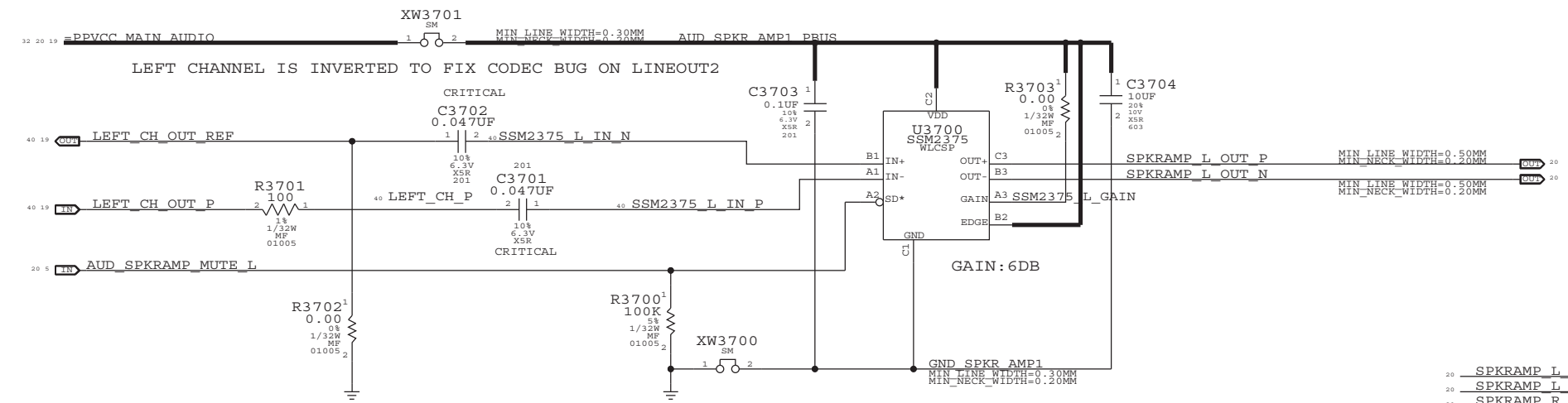
APN:353S2958

TURN ON TIME: 7.5MS

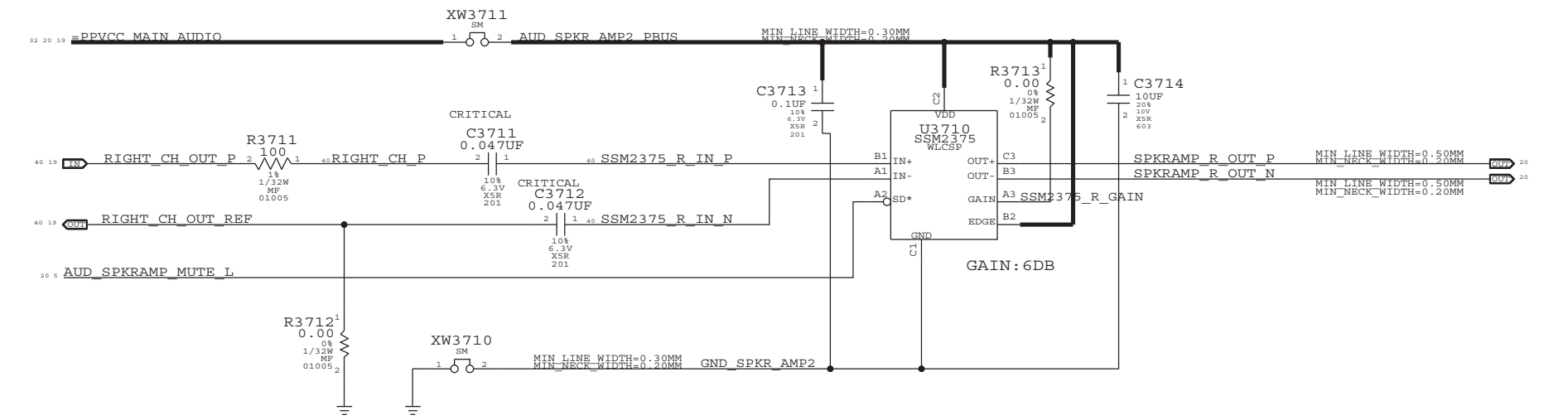
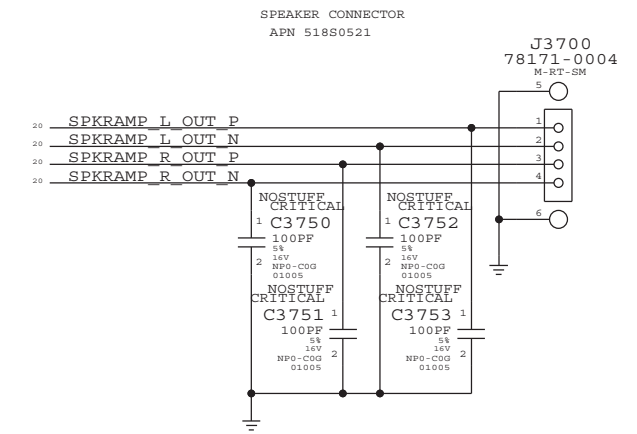
80HZ +/- XXX%

TURN ON DELAY: 20MS

GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT

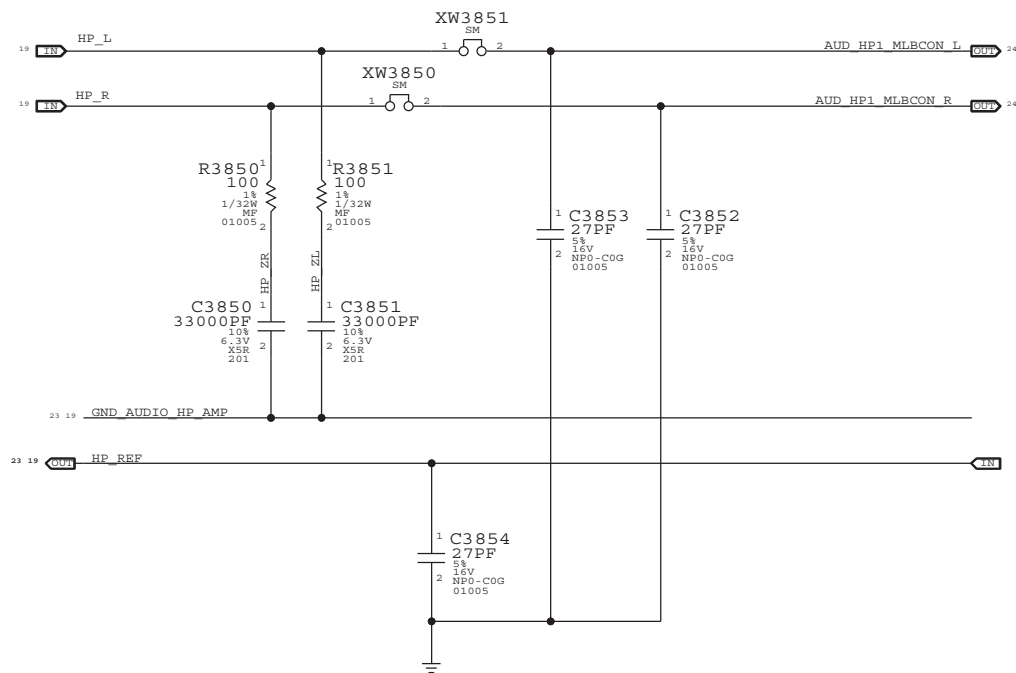


L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710

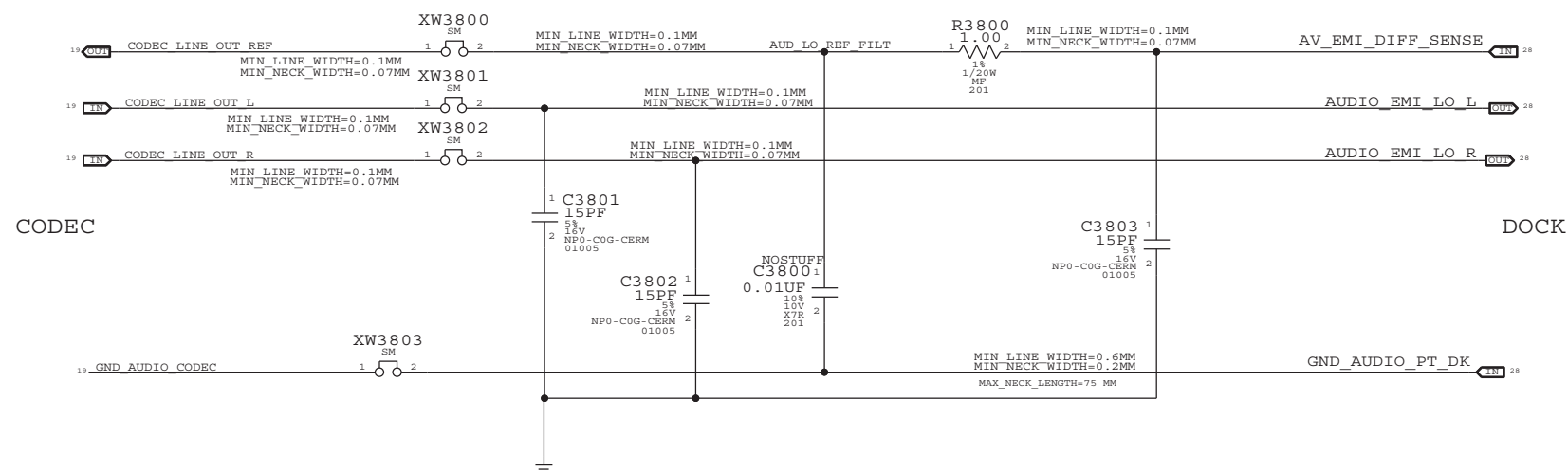


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PAGE TITLE: AUDIO: SPEAKER AMP			
DRAWING NUMBER: 051-8962		SIZE: D	
REVISION: A.0.0		BRANCH:	
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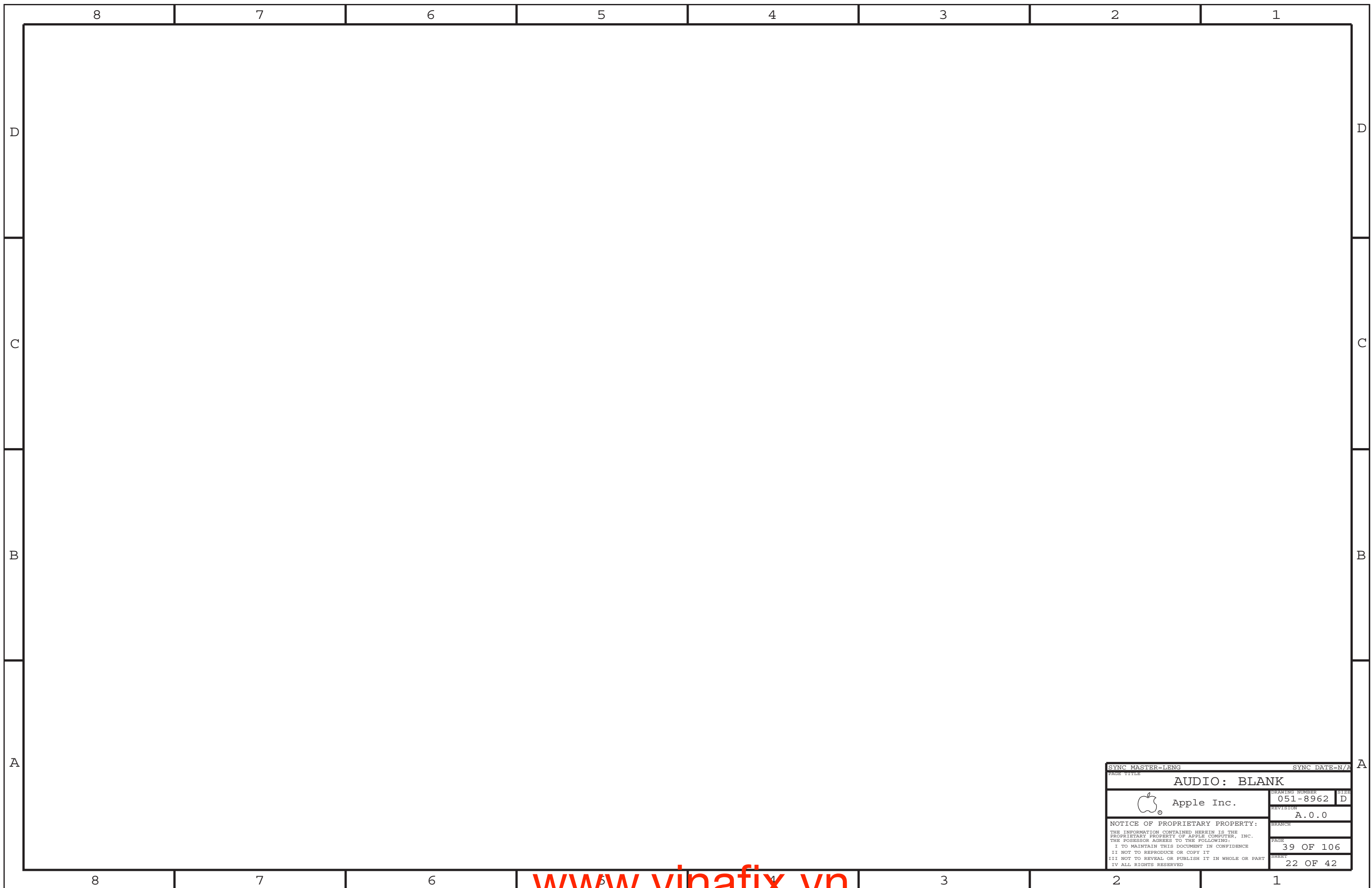
HEADPHONE OUTPUT ZOBEL NETWORK




DOCK LINE OUTPUT

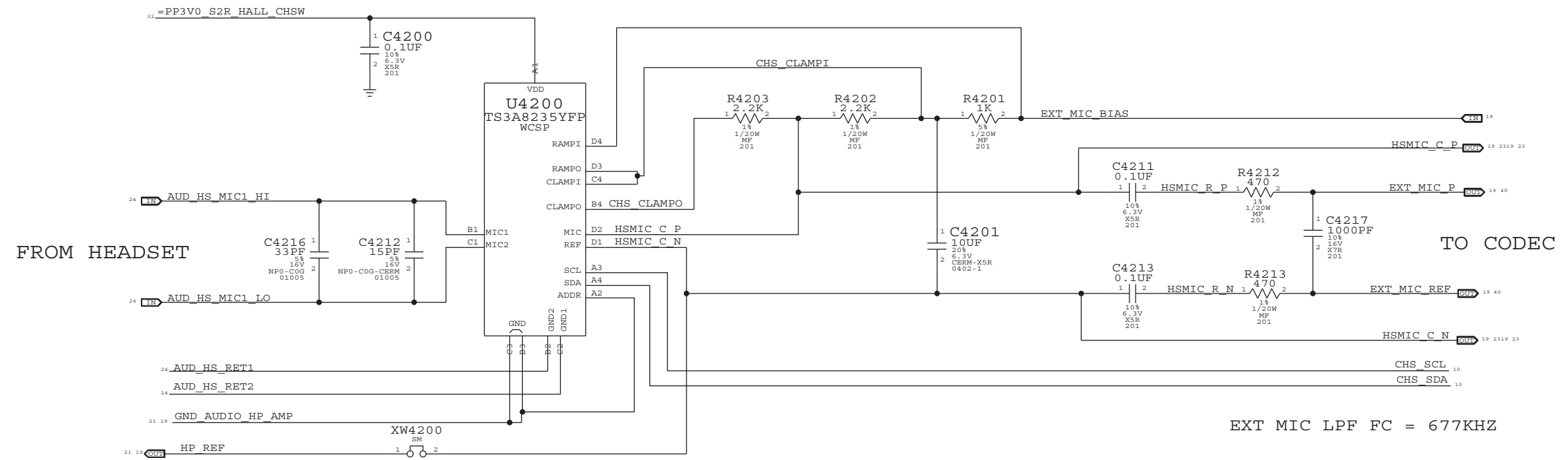


SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: HEADPHONE OUT			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
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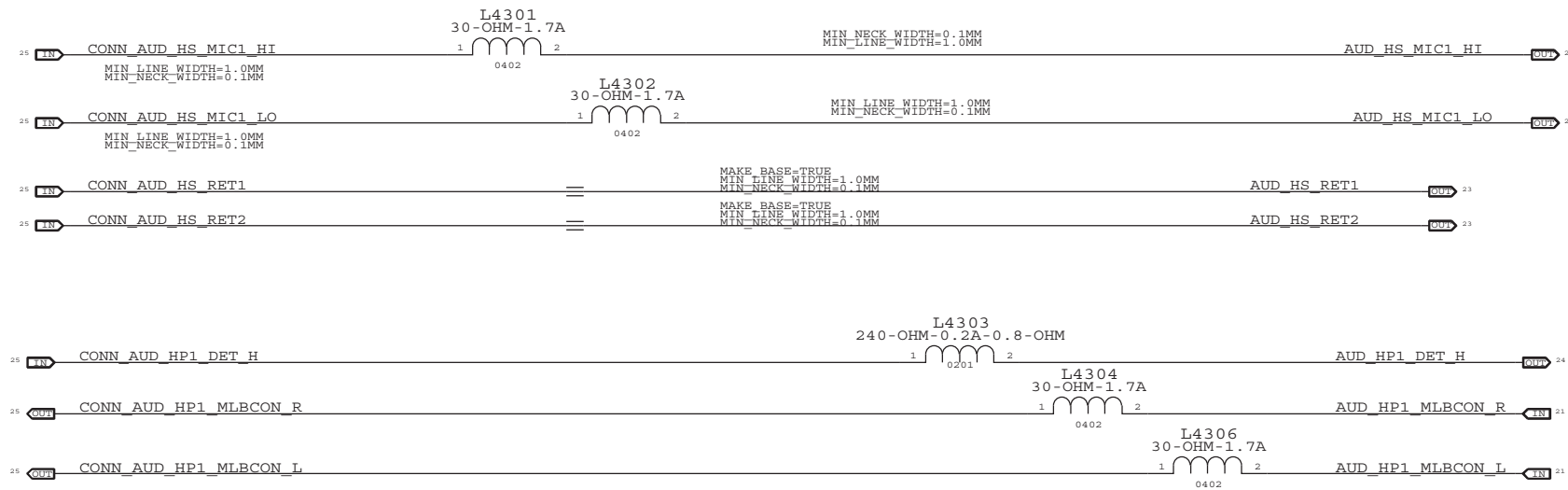
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	REVISION	A.0.0	
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EXTERNAL (HEADSET) MIC INPUT CIRCUITRY

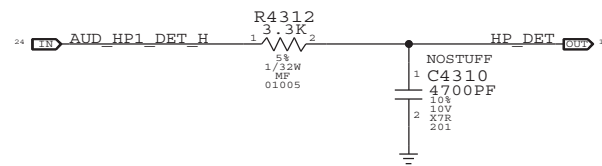


SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE AUDIO: DETECT/MIC BIAS			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
 PLACE ALL COMPONENTS NEAR J5501



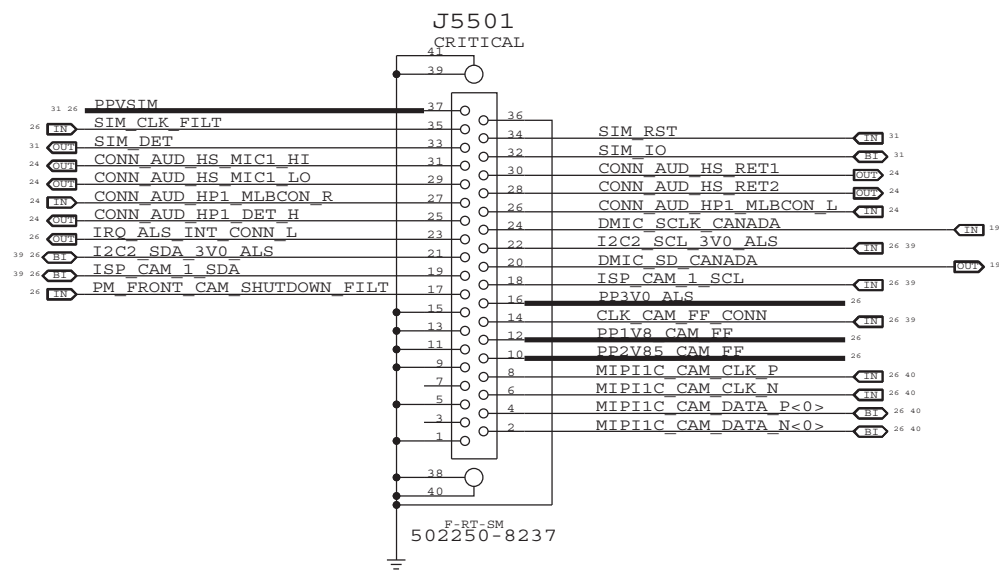
HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: HP/MIC FILTERS			
DRAWING NUMBER		SIZE	
051-8962		D	
REVISION		BRANCH	
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CANADA FLEXES CONN.

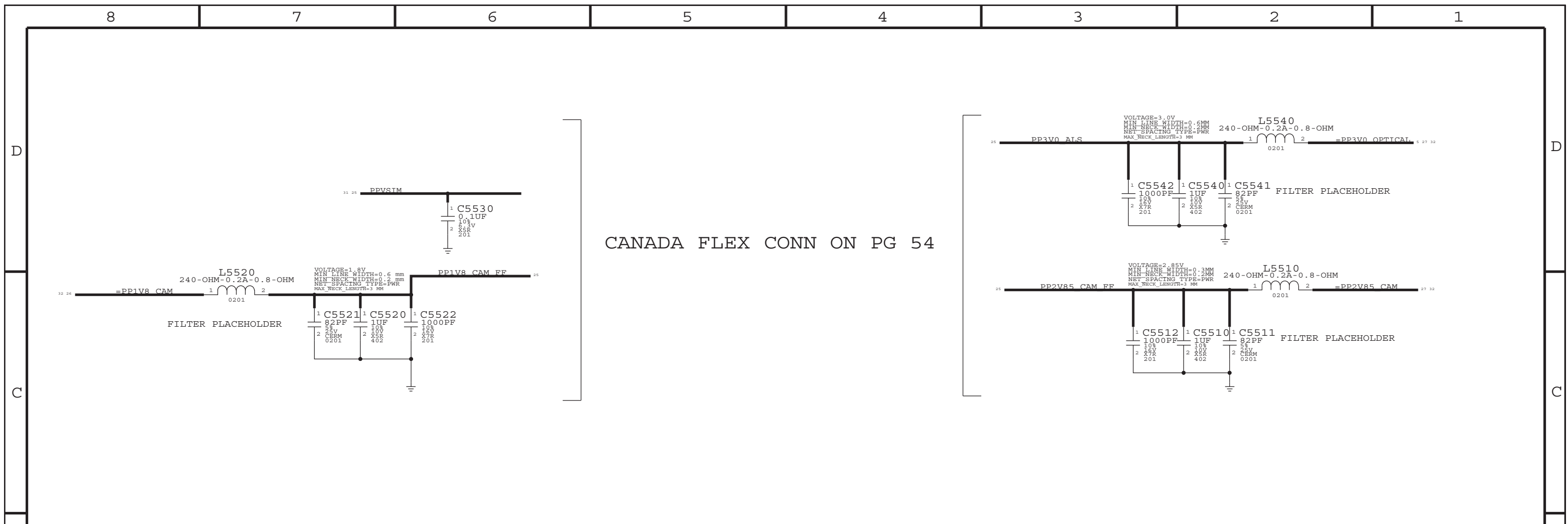
APN: 518S0817



SENSOR BOARD CONN ALIASES

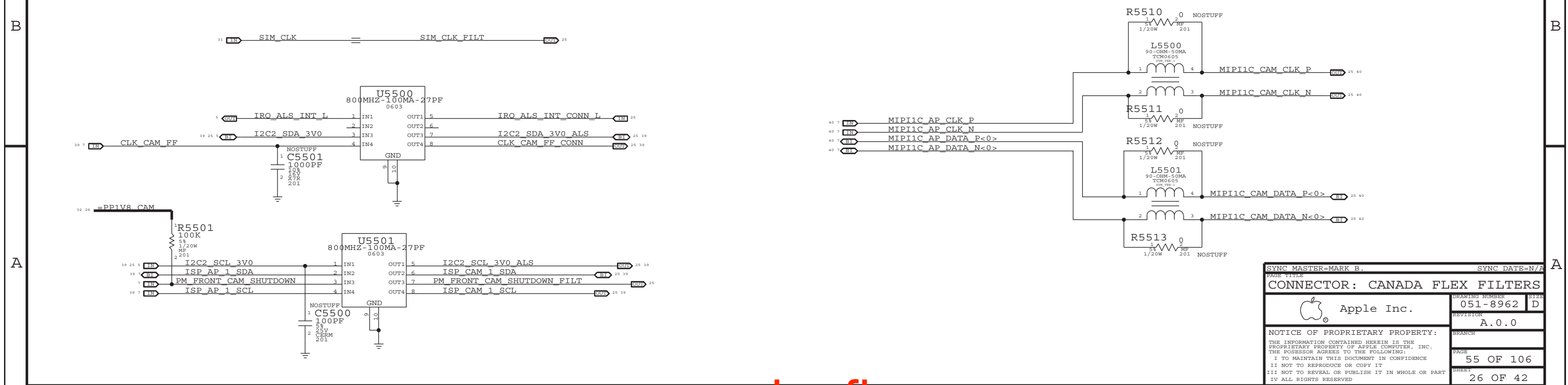
39	CLK_CAM_RF_FILT	==	CONN_CLK_CAM_RF_FILT	27
40	MIP11C_CAM_DATA_N<0>	MAKE_BASE+TRIG	==	CONN_MIP11C_CAM_DATA_N<0>
40	MIP11C_CAM_DATA_P<0>	MAKE_BASE+TRIG	==	CONN_MIP11C_CAM_DATA_P<0>
40	MIP11C_CAM_CLK_N	MAKE_BASE+TRIG	==	CONN_MIP11C_CAM_CLK_N
40	MIP11C_CAM_CLK_P	MAKE_BASE+TRIG	==	CONN_MIP11C_CAM_CLK_P
7	PM_REAR_CAM_SHUTDOWN	MAKE_BASE+TRIG	==	CONN_PM_REAR_CAM_SHUTDOWN
27	PP1V8_SENSOR_FILT	MAKE_BASE+TRIG	==	CONN_PP1V8_SENSOR_FILT
27	PP2V85_CAM_REAR	MAKE_BASE+TRIG	==	CONN_PP2V85_CAM_REAR
19	DMIC_SD_SENSOR	MAKE_BASE+TRIG	==	CONN_DMIC_SD_SENSOR
19	DMIC_SCLK_SENSOR	MAKE_BASE+TRIG	==	CONN_DMIC_SCLK_SENSOR
19	ISP_AP_0_SCL	MAKE_BASE+TRIG	==	CONN_ISP_AP_0_SCL
19	ISP_AP_0_SDA	MAKE_BASE+TRIG	==	CONN_ISP_AP_0_SDA
19	I2C2_SCL_3V0	MAKE_BASE+TRIG	==	CONN_I2C2_SCL_3V0
19	I2C2_SDA_3V0	MAKE_BASE+TRIG	==	CONN_I2C2_SDA_3V0
6	IRQ_ACCEL_INT1_L	MAKE_BASE+TRIG	==	CONN_IRQ_ACCEL_INT1_L
6	IRQ_ACCEL_INT2_L	MAKE_BASE+TRIG	==	CONN_IRQ_ACCEL_INT2_L
6	IRQ_GYRO_INT1	MAKE_BASE+TRIG	==	CONN_IRQ_GYRO_INT1
6	IRQ_GYRO_INT2	MAKE_BASE+TRIG	==	CONN_IRQ_GYRO_INT2
19	I2C1_SCL_1V8	MAKE_BASE+TRIG	==	CONN_I2C1_SCL_1V8
19	I2C1_SDA_1V8	MAKE_BASE+TRIG	==	CONN_I2C1_SDA_1V8
19	IRQ_HALL	MAKE_BASE+TRIG	==	CONN_IRQ_HALL
19	IRQ_PROX_INT_L	MAKE_BASE+TRIG	==	CONN_IRQ_PROX_INT_L
27	PP3V0_S2R_HALL_FILT	MAKE_BASE+TRIG	==	CONN_PP3V0_S2R_HALL
15	ONOFF_L	MAKE_BASE+TRIG	==	CONN_ONOFF_FTR_L
15	SRL_L	MAKE_BASE+TRIG	==	CONN_SRL_FTR_L
15	AUD_VOL_UP_L	MAKE_BASE+TRIG	==	CONN_AUD_VOL_UP_FTR_L
15	AUD_VOL_DOWN_L	MAKE_BASE+TRIG	==	CONN_AUD_VOL_DOWN_FTR_L
27	PP3V0_OPTICAL_SENS	MAKE_BASE+TRIG	==	CONN_PP3V0_OPTICAL_SENS

SYNC MASTER=MARK B.		SYNC DATE=N/A	
CONNECTOR: CANADA FLEX CONN, SENSOR PANEL ALIASES			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
	REVISION	A.0.0	
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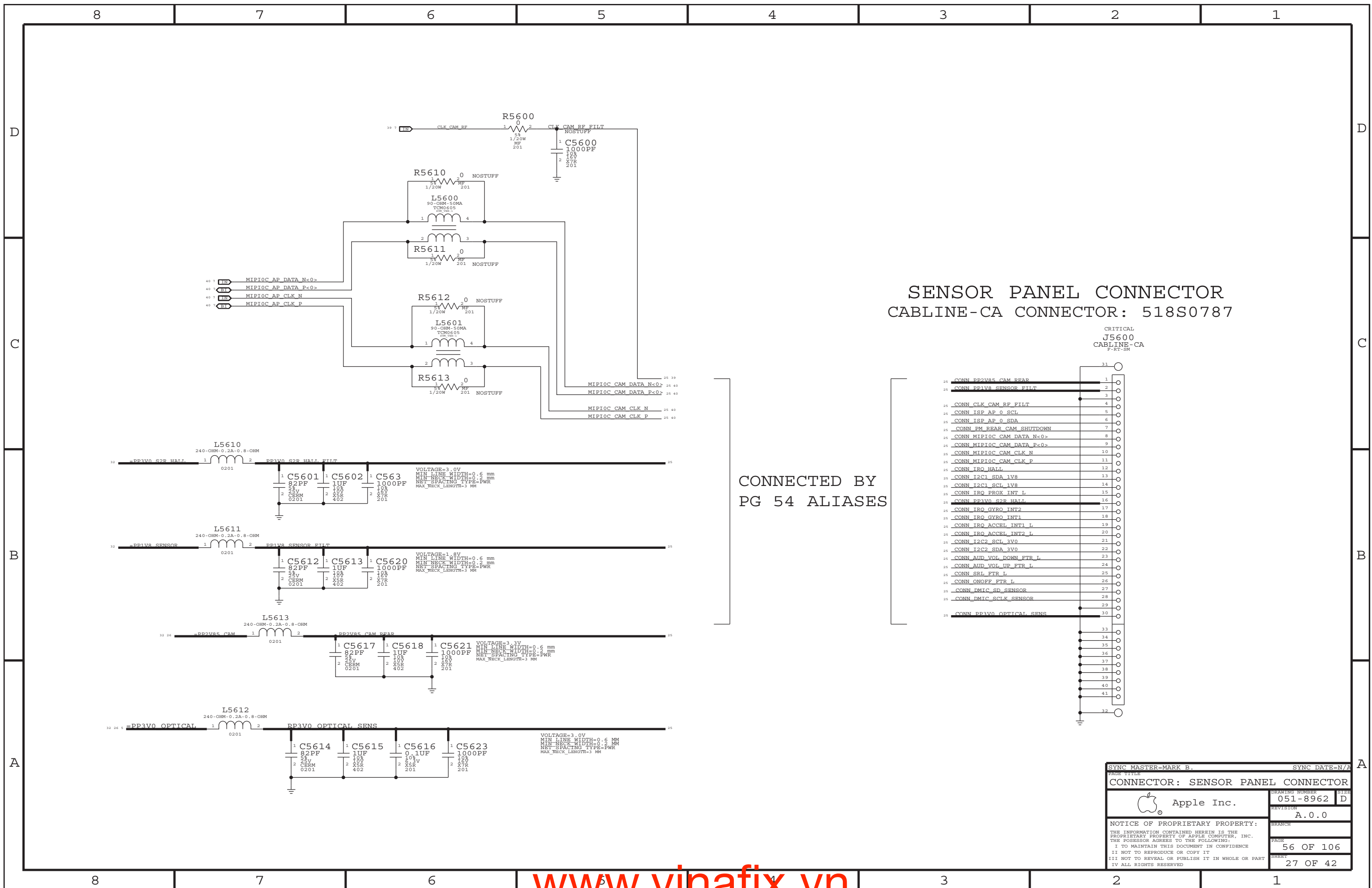


CANADA FLEX CONN ON PG 54

CANADA FLEX SIGNAL FILTERS



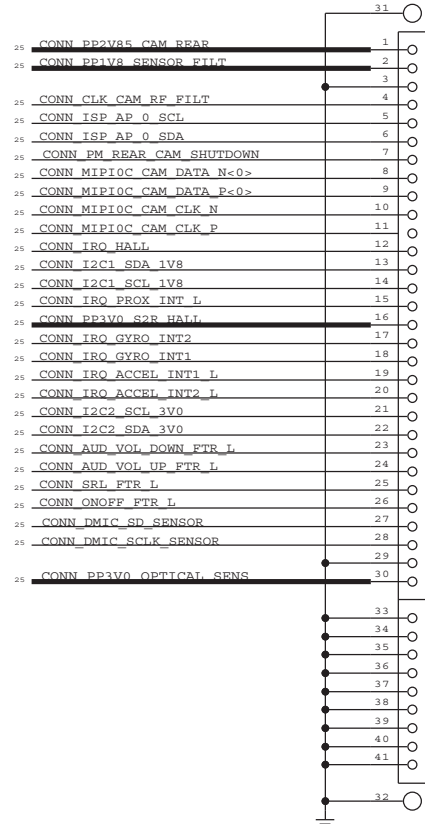
PAGE TITLE		SYNC DATE=N/A	
CONNECTOR: CANADA FLEX FILTERS			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
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BRANCH		PAGE	55 OF 106
SHEET		26 OF 42	



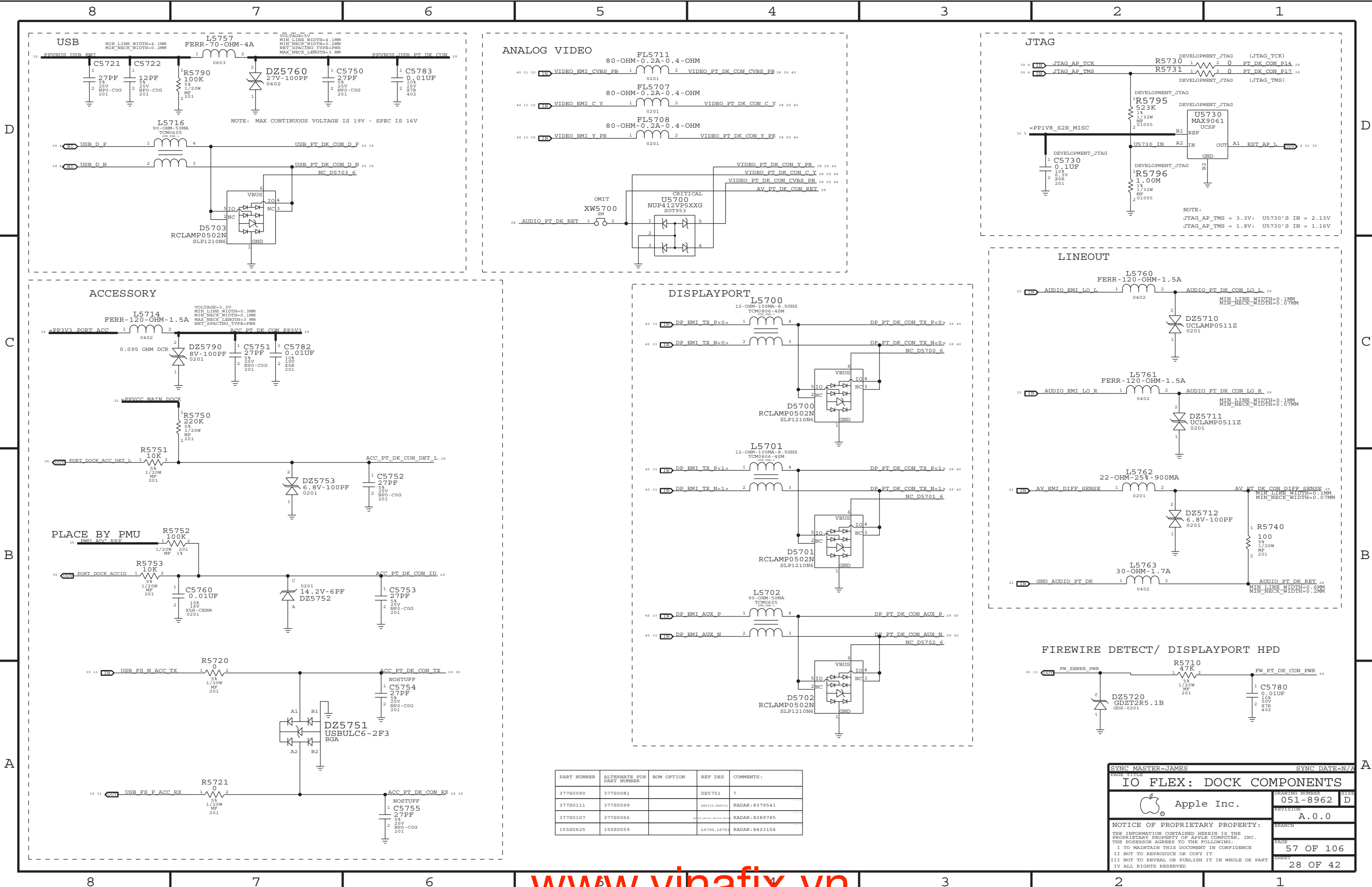
SENSOR PANEL CONNECTOR CABLINE-CA CONNECTOR: 518S0787

CRITICAL
J5600
CABLINE-CA
F-RT-SM

CONNECTED BY
PG 54 ALIASES



PAGE TITLE		SYNC DATE=N/A	
CONNECTOR: SENSOR PANEL CONNECTOR			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
	REVISION	A.0.0	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DBY10, DBY11	RADAR: 8379541
377S0107	377S0066		DBY10, DBY11	RADAR: 8289785
155S0625	155S0559		L5700, L5708	RADAR: 8423156

SYNC MASTER=JAMES SYNC DATE=N/A

IO FLEX: DOCK COMPONENTS

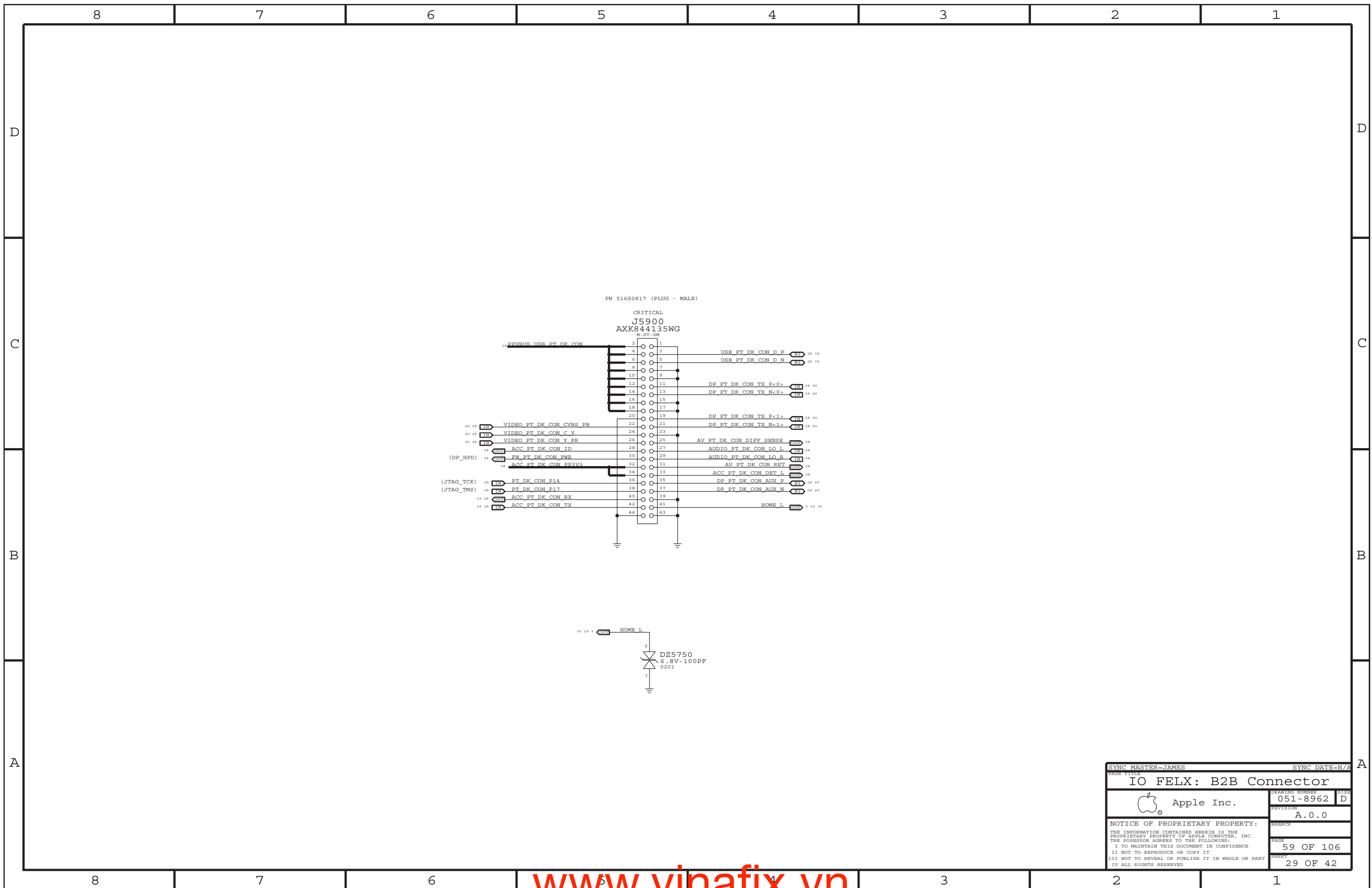
Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

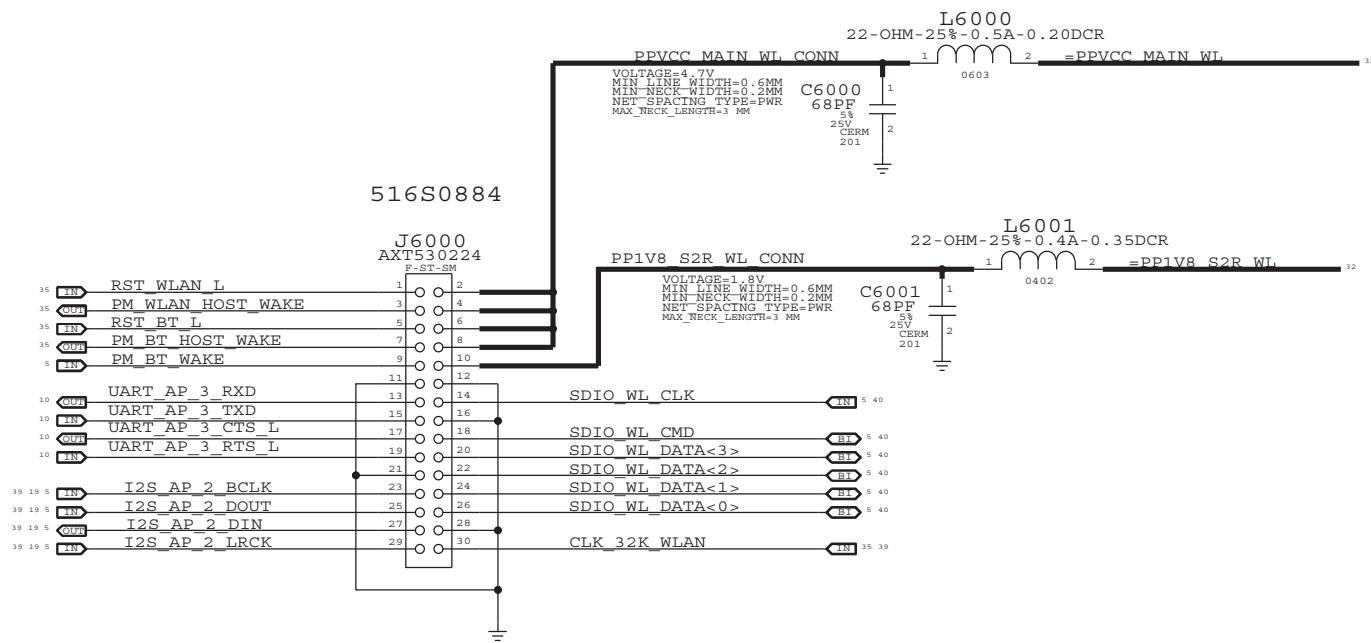
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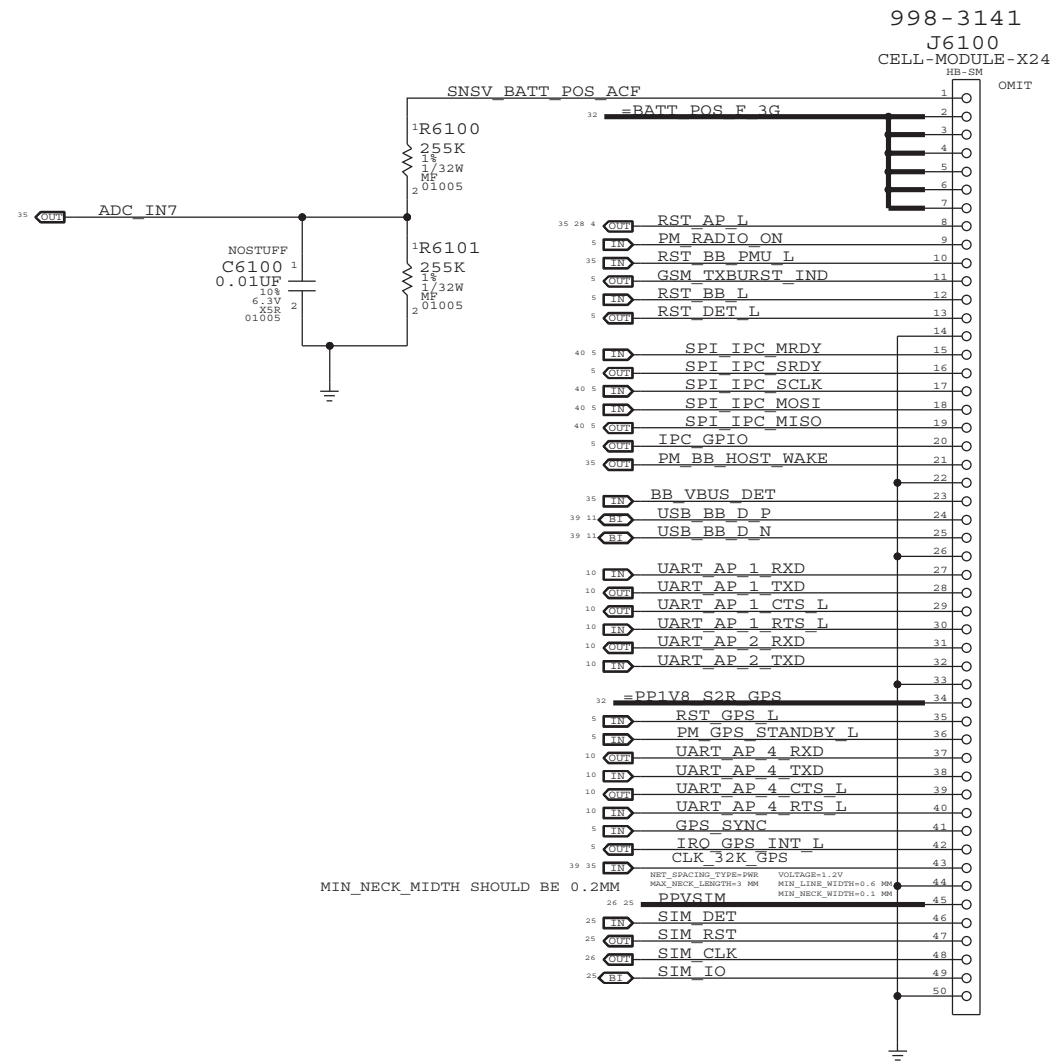
SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE IO FELX: B2B Connector			
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X23 WIFI/BT CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X23 WIFI/BT			
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X24 CELLULAR/GPS CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X24 CELLULAR/GPS			
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POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

BUCK RAILS

CHARGER MAIN

BATTERY

USB POWER INPUT

D

D

C

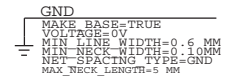
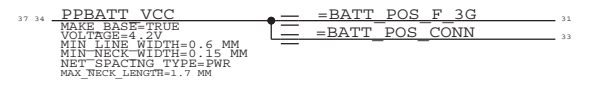
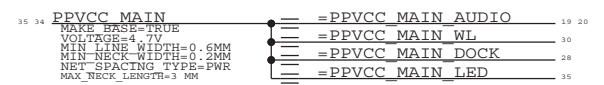
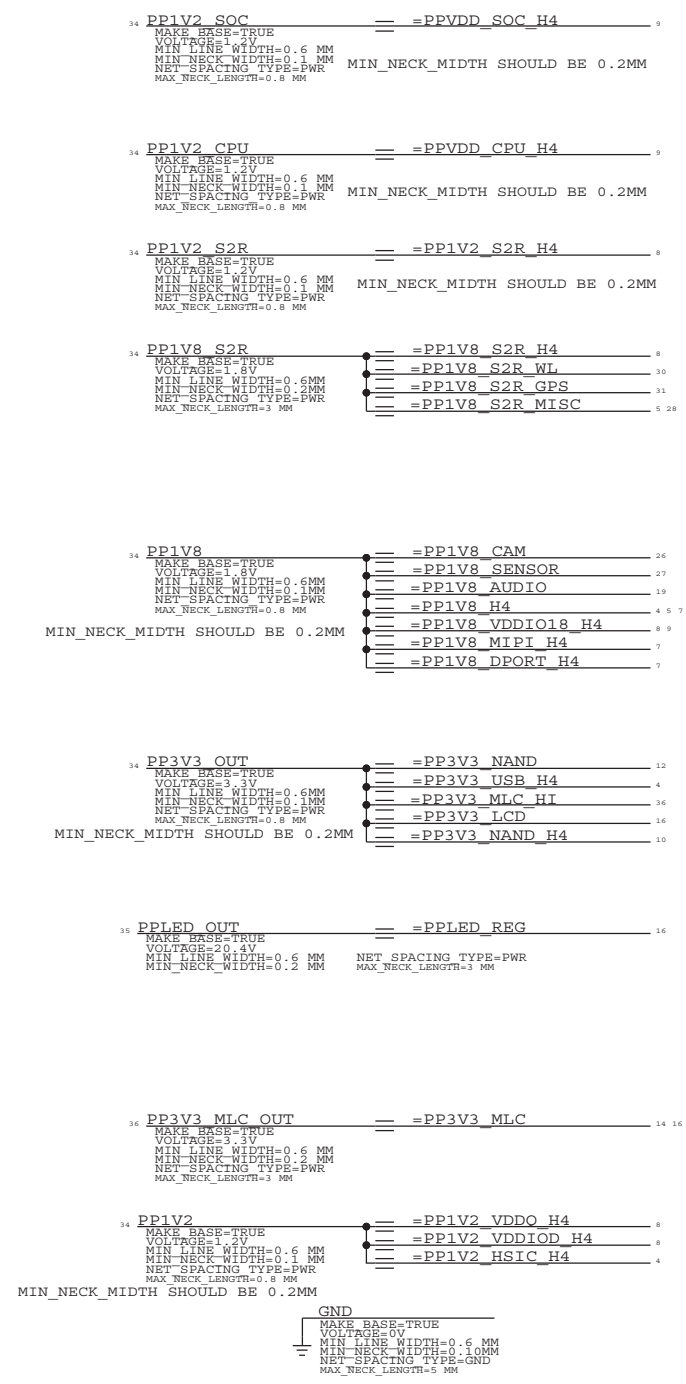
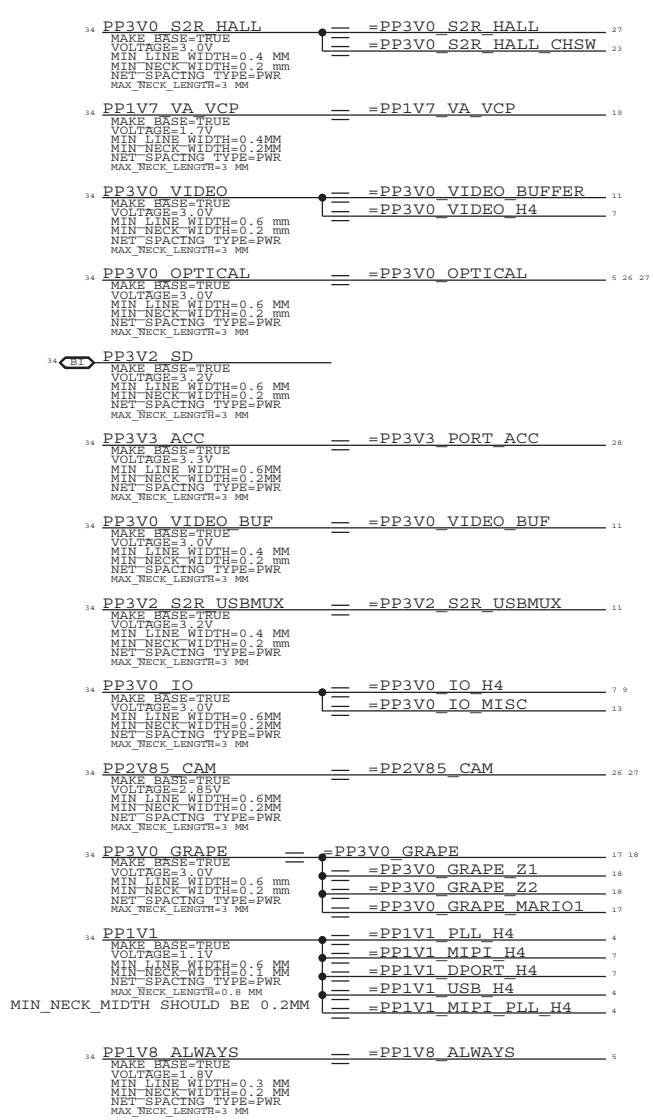
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B

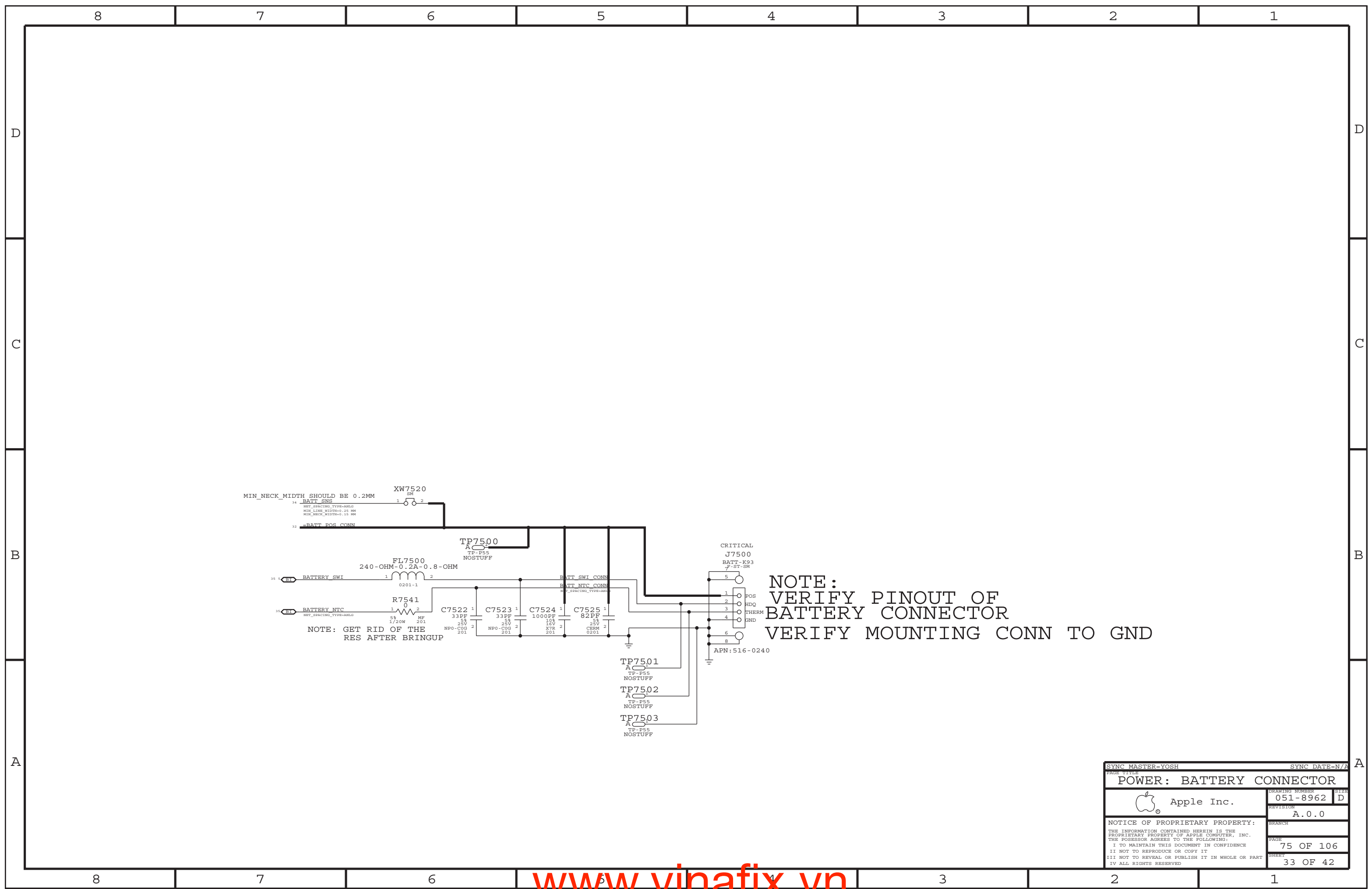
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A

A



SYNC MASTER=YOSH		SYNC DATE=N/A	
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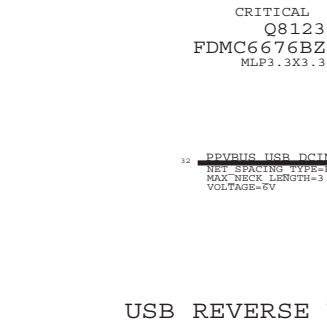
NOTE:
 VERIFY PINOUT OF
 BATTERY CONNECTOR
 VERIFY MOUNTING CONN TO GND

PAGE TITLE		SYNC MASTER=YOSH		SYNC DATE=N/A	
POWER: BATTERY CONNECTOR					
		DRAWING NUMBER	051-8962	SIZE	D
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				SHEET	33 OF 42

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34350542	1	IC, PMU, ALISON, D1946A2, OTPXX, UFBGA292	U8100	CRITICAL	

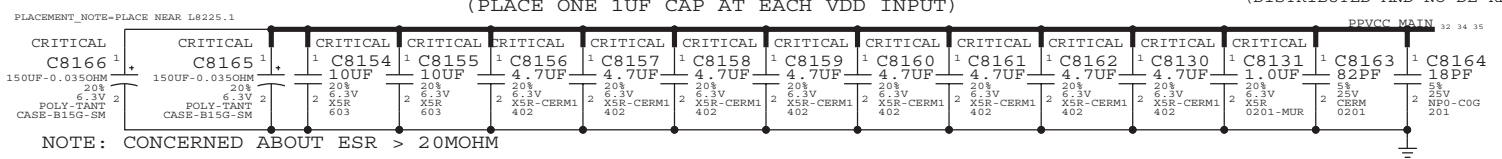
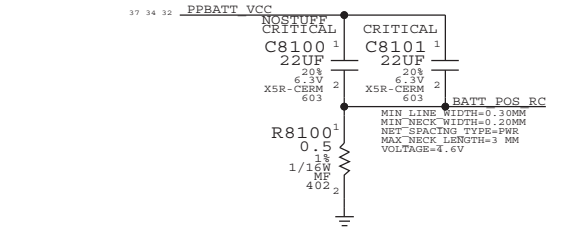
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19750392	19750299		Y8138	ALT FOUNDRY

PARAMETER	VALUE
MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS (ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



USB REVERSE VOLTAGE PROTECTION

NOTE: FOR NO BATTERY SITUATION



NOTE: CONCERNED ABOUT ESR > 20MOHM

PLACEMENT_NOTE-PLACE NEAR L8225.1

(PLACE ONE 1UF CAP AT EACH VDD INPUT)

(DISTRIBUTED AND NO DE-RATING)

U8100
ALISON-A0-OTPXX
D1946A0-110-00
UFBGA
(SYM 2 OF 3)

OMIT

BUCK0_LXL A11

BUCK0_LXM A9

BUCK0_FB D9

BUCK2_LXL A7

BUCK2_LXM H25

BUCK2_LXR A6

BUCK2_LX A4

BUCK2_FB D7

BUCK3_LX A16

BUCK3_FB D16

BUCK4_LXL A14

BUCK4_LXM B1

BUCK4_LXR D14

BUCK5_LX F2

BUCK5_LXM H1

BUCK5_LXR J1

BUCK5_FB G4

BUCK5_BY (BYPASS RON=0.14 OHM MAX)

BUCK5_FB G4

VLD01 L1 (150MA; 2.5-3.55V) PP3V0 GRABE

VLD02 P3 (100MA; 1.65-1.805V; BUCK3) PP1V7 VA VCP

VLD03 P9 (50MA; 2.5-3.3V) PP3V0 VIDEO

VLD04 N5 (100MA; 1.8-3.3V) PP3V0 OPTICAL

VLD05 P10 (300MA; 2.5-3.6V) PP3V2 SD

VLD06 K1 (150MA; 2.5-3.6V) PP3V3 ACC

VLD07 P4 (100MA; 1.5-3.3V) PP3V0 VIDEO BUF

VLD08 P8 (10MA; 2.0-3.55V) PP1V2 S2R USBMIX

VLD09 P11 (300MA; 1.2-3.0V) PP3V0 TO

VLD010 P5 (200MA; 2.5-3.55V) PP3V0 S2R HALL

VLD011 M1 (200MA; 1.7-3.0V) PP2V85 CAM

VLD012 P6 (150MA; 0.6-1.3V) PP1V1

ON_BUF M2 (PP1V8 ALWAYS)

VBUCK4 B17

CPUIV2_SW A18 (RON=0.1 OHM MAX)

DSP_SW B20 (RON=1 OHM MAX)

VBUCK3 A19

CPUIV8_SW A20 (RON=0.2 OHM MAX)

WDIQ_SW B19 (RON=0.5 OHM MAX)

VBUCK0_SW_G B21 NC PMU VBUCK0_SW_G

VBUCK0_SW_S A21 NC PMU VBUCK0_SW_S

VPUMP B18 PMU VPUMP

C8137 0.01UF

C8138 1UF

C8140 1UF

C8139 1UF

C8141 1UF

C8137 0.01UF

C8138 1UF

C8140 1UF

C8139 1UF

C8141 1UF

C8137 0.01UF

C8138 1UF

C8140 1UF

C8139 1UF

C8141 1UF

C8137 0.01UF

C8138 1UF

C8140 1UF

C8139 1UF

C8141 1UF

C8137 0.01UF

C8138 1UF

C8140 1UF

C8139 1UF

C8141 1UF

C8137 0.01UF

C8138 1UF

C8140 1UF

C8139 1UF

C8141 1UF

C8137 0.01UF

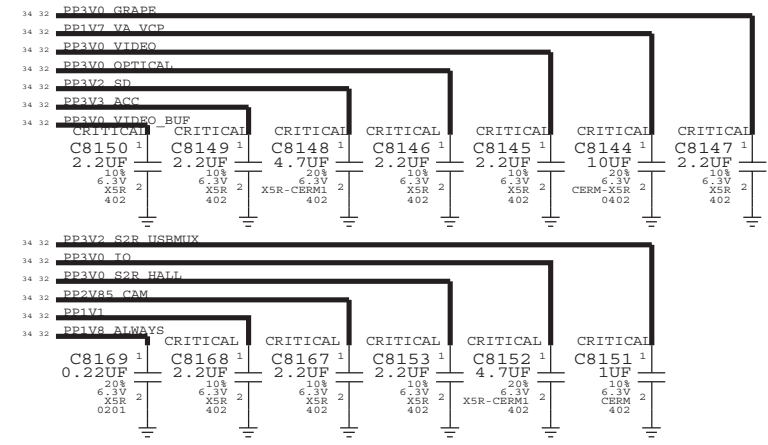
C8138 1UF

C8140 1UF

C8139 1UF

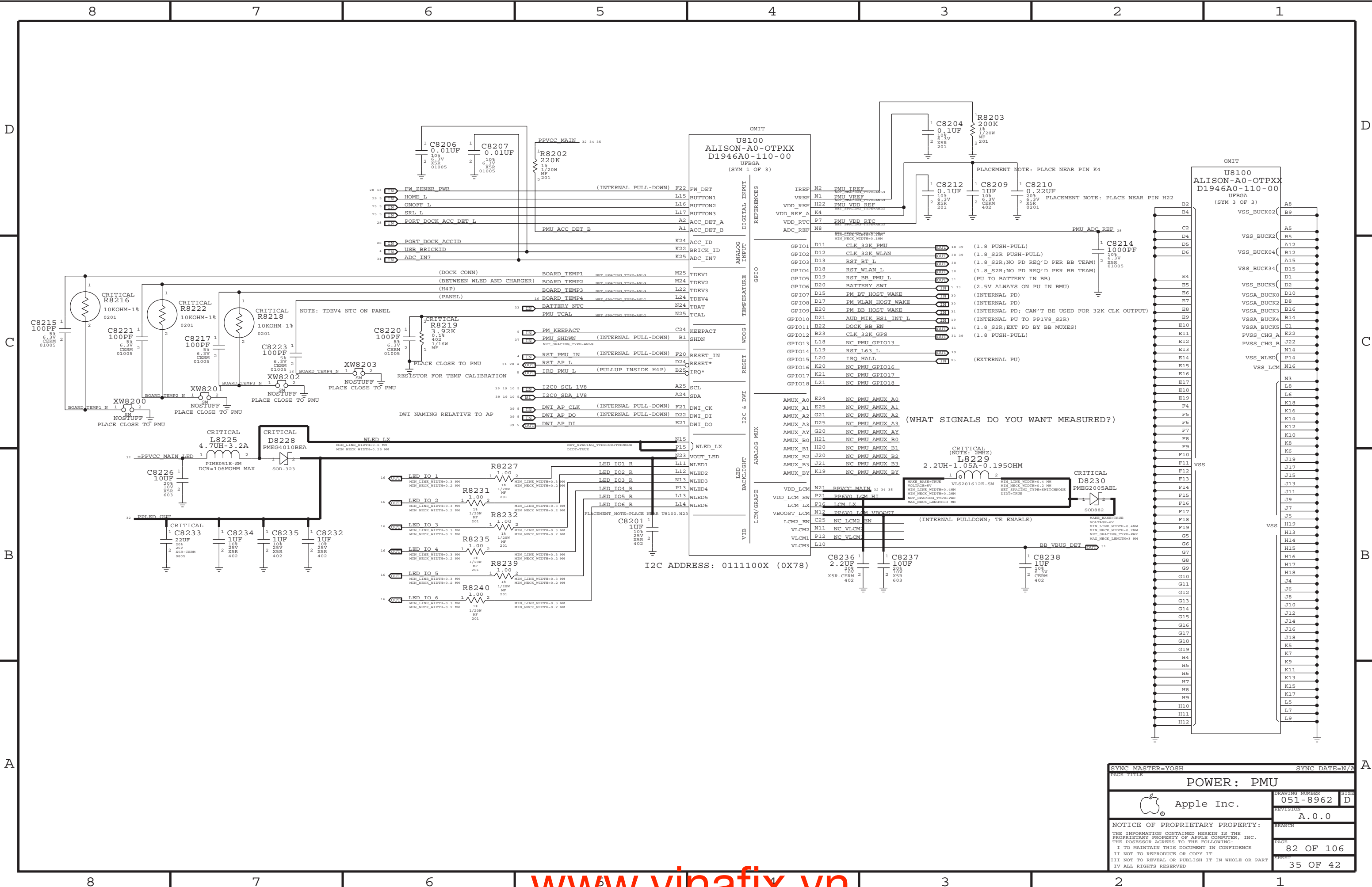
C8141 1UF

LDO BYPASS

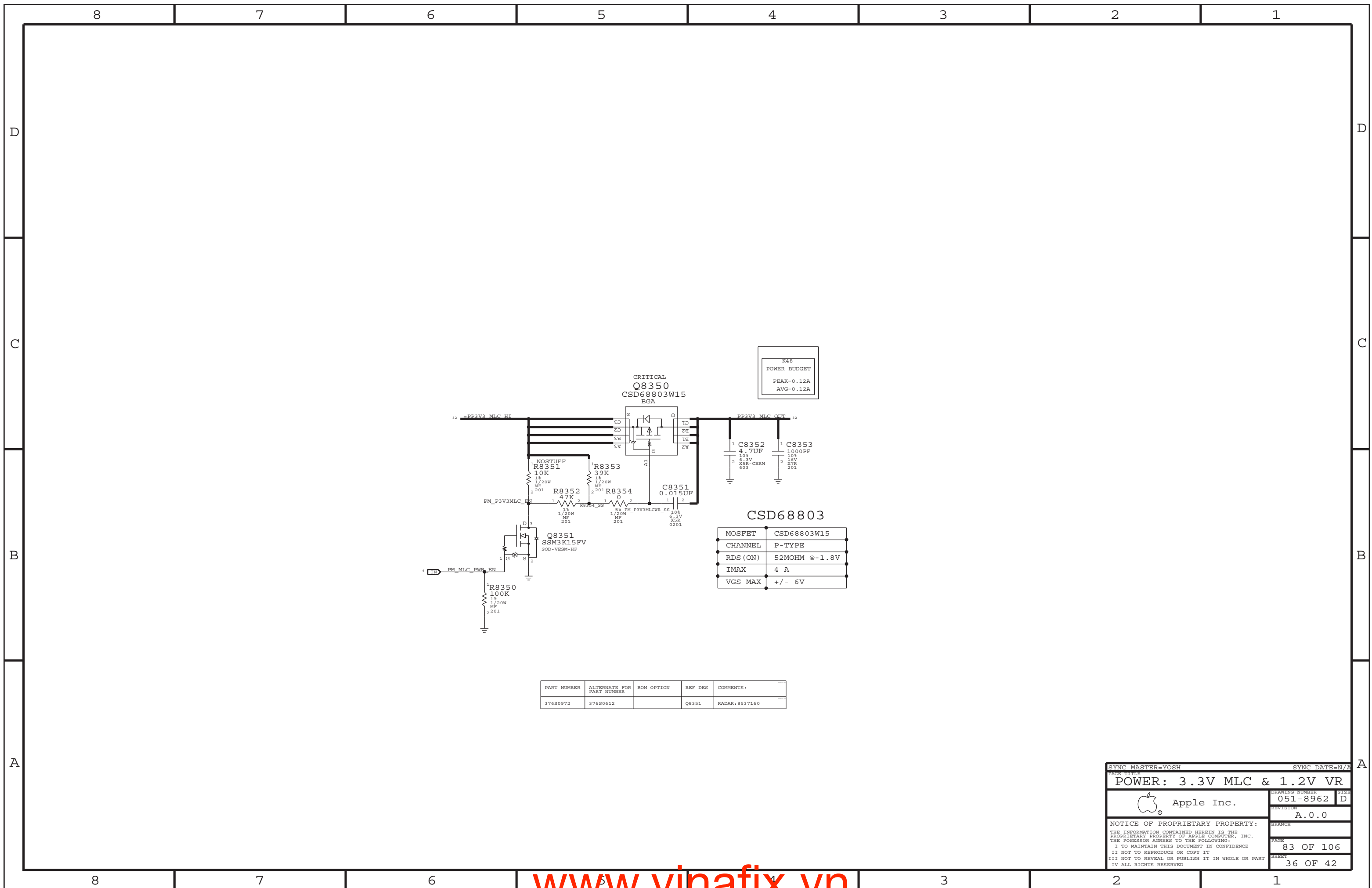


ADDITIONAL DISTRIBUTED:
PP1V2: 30UF (NO DE-RATING)
PP1V8: 6UF (NO DE-RATING)

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K48
POWER BUDGET
PEAK=0.12A
AVG=0.12A

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS (ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0972	376S0612		Q8351	RADAR: 8537160

SYNC MASTER=YOSH SYNC DATE=N/A

POWER: 3.3V MLC & 1.2V VR

Apple Inc.

051-8962 D

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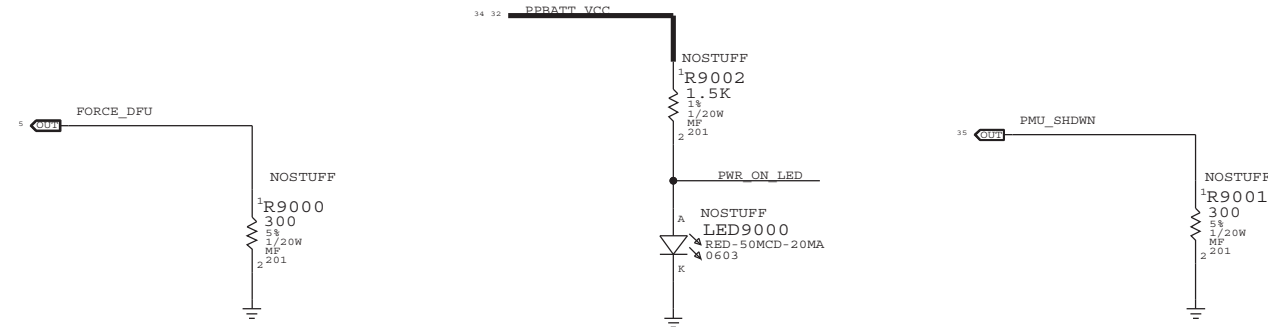
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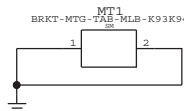
36 OF 42

DEBUG RESET ACCESS

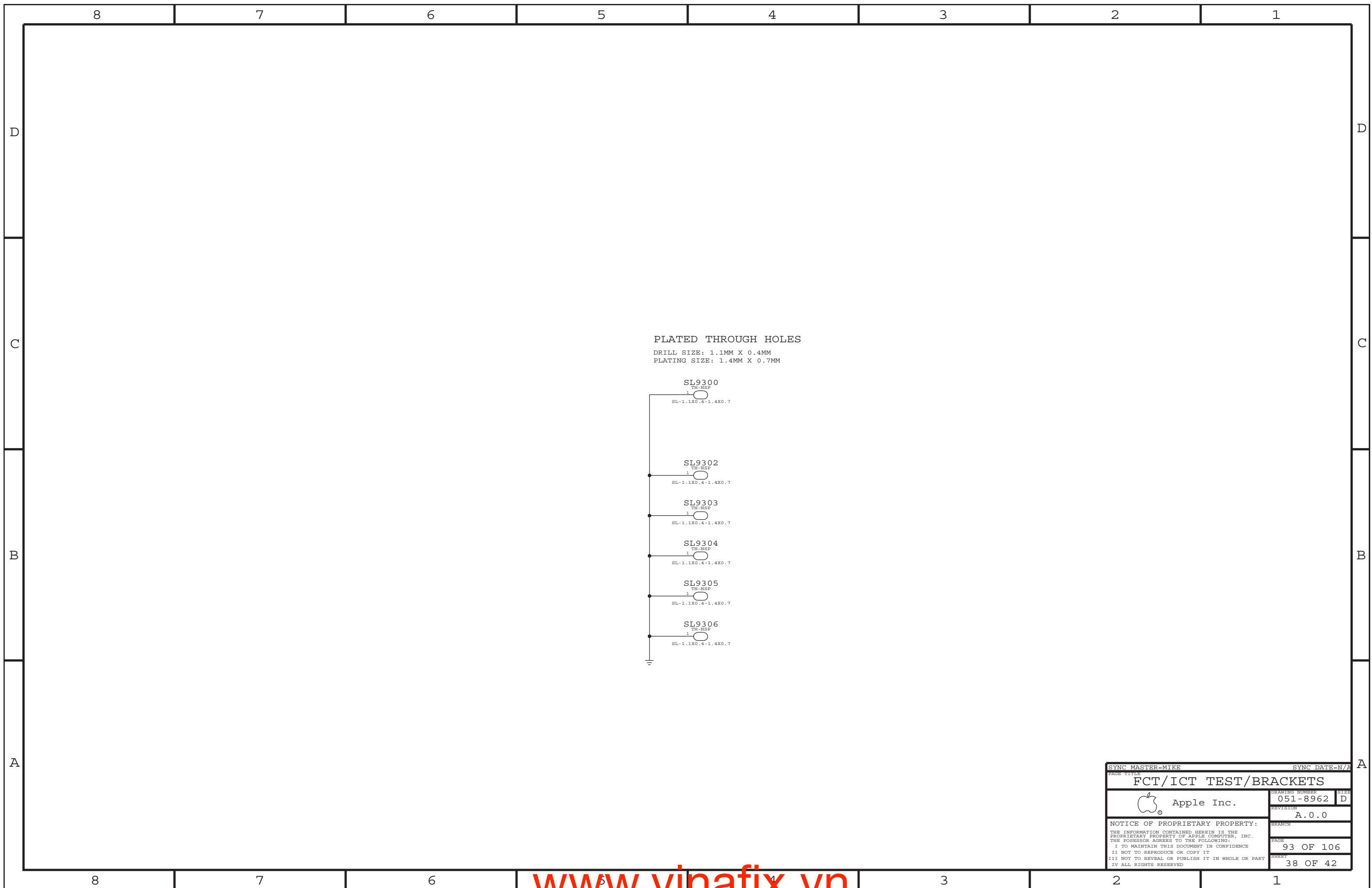
PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS

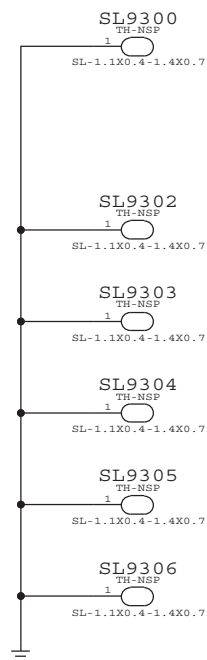



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PAGE TITLE DEBUG AND MISC			
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PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
 PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=MIKE		SYNC DATE=N/A	
FCT/ICT TEST/BRACKETS			
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		SHEET	38 OF 42
		SIZE	D

ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	VID_50S	ANALOG_VIDEO	DAC AP OUT1 7 11
1230	VID_50S	ANALOG_VIDEO	DAC AP OUT2 7 11
1230	VID_50S	ANALOG_VIDEO	DAC AP OUT3 7 11
1230	VID_50S	ANALOG_VIDEO	BUF C Y 11
1230	VID_50S	ANALOG_VIDEO	BUF CVBS PB 11
1230	VID_50S	ANALOG_VIDEO	BUF Y PR 11
1230	VID_50S	ANALOG_VIDEO	VIDEO EMI CVBS PB 10 11 28
1230	VID_50S	ANALOG_VIDEO	VIDEO EMI C Y 10 11 28
1230	VID_50S	ANALOG_VIDEO	VIDEO EMI Y PR 10 11 28
1230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON CVBS PB 28 29
1230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON C Y 28 29
1230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON Y PR 28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	MIPI_100D	MIPT	MIPI AP DATA P<0> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA N<0> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA P<1> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA N<1> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA P<2> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA N<2> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA P<3> 7 14
1230	MIPI_100D	MIPT	MIPI AP DATA N<3> 7 14
1230	MIPI_100D	MIPT	MIPI AP CLK P 7 14
1230	MIPI_100D	MIPT	MIPI AP CLK N 7 14
1230	MIPI_100D	MIPT	MIPI OC AP DATA P<0> 7 27
1230	MIPI_100D	MIPT	MIPI OC AP DATA N<0> 7 27
1230	MIPI_100D	MIPT	MIPI OC AP CLK P 7 27
1230	MIPI_100D	MIPT	MIPI OC AP CLK N 7 27
1230	MIPI_100D	MIPT	MIPI OC CAM DATA P<0> 25 27
1230	MIPI_100D	MIPT	MIPI OC CAM DATA N<0> 25 27
1230	MIPI_100D	MIPT	MIPI OC CAM CLK P 25 27
1230	MIPI_100D	MIPT	MIPI OC CAM CLK N 25 27
1230	MIPI_100D	MIPT	MIPI IC AP DATA P<0> 7 26
1230	MIPI_100D	MIPT	MIPI IC AP DATA N<0> 7 26
1230	MIPI_100D	MIPT	MIPI IC AP CLK P 7 26
1230	MIPI_100D	MIPT	MIPI IC AP CLK N 7 26
1230	MIPI_100D	MIPT	MIPI IC CAM DATA P<0> 25 26
1230	MIPI_100D	MIPT	MIPI IC CAM DATA N<0> 25 26
1230	MIPI_100D	MIPT	MIPI IC CAM CLK P 25 26
1230	MIPI_100D	MIPT	MIPI IC CAM CLK N 25 26

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	LVDS_100D	LVDS	LVDS DATA P<2>.0> 14 16
1230	LVDS_100D	LVDS	LVDS DATA N<2>.0> 14 16
1230	LVDS_100D	LVDS	LVDS DATA CONN P<2..0> 16
1230	LVDS_100D	LVDS	LVDS DATA CONN N<2..0> 16
1230	LVDS_100D	LVDS	LVDS CLK P 14 16
1230	LVDS_100D	LVDS	LVDS CLK N 14 16
1230	LVDS_100D	LVDS	LVDS CLK CONN P 16
1230	LVDS_100D	LVDS	LVDS CLK CONN N 16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	DP_100D	DP	DP AP TX P<0> 7 10 13
1230	DP_100D	DP	DP AP TX N<0> 7 10 13
1230	DP_100D	DP	DP AP TX P<1> 7 10 13
1230	DP_100D	DP	DP AP TX N<1> 7 10 13
1230	DP_100D	DP	DP AP AUX P 7 13
1230	DP_100D	DP	DP EMI TX P<0> 13 28
1230	DP_100D	DP	DP EMI TX N<0> 13 28
1230	DP_100D	DP	DP EMI TX P<1> 13 28
1230	DP_100D	DP	DP EMI TX N<1> 13 28
1230	DP_100D	DP	DP EMI AUX P 13 28
1230	DP_100D	DP	DP EMI AUX N 13 28
1230	DP_100D	DP	DP PT DK CON TX P<0> 28 29
1230	DP_100D	DP	DP PT DK CON TX N<0> 28 29
1230	DP_100D	DP	DP PT DK CON TX P<1> 28 29
1230	DP_100D	DP	DP PT DK CON TX N<1> 28 29
1230	DP_100D	DP	DP PT DK CON AUX P 28 29
1230	DP_100D	DP	DP PT DK CON AUX N 28 29

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
1230	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
1230	AUDIO	AUDIO	LEFT_CH_P 20
1230	AUDIO	AUDIO	SSM2375_L_IN_P 20
1230	AUDIO	AUDIO	SSM2375_L_IN_N 20
1230	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
1230	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
1230	AUDIO	AUDIO	RIGHT_CH_P 20
1230	AUDIO	AUDIO	SSM2375_R_IN_P 20
1230	AUDIO	AUDIO	SSM2375_R_IN_N 20
1230	AUDIO	AUDIO	EXT_MIC_P 19 23
1230	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
1230	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R 5 30
1230	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
1230	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
1230	SPT_50S	SPT	SPI GRAPE MISO 5 17
1230	SPT_50S	SPT	SPI GRAPE MOSI 5 17
1230	SPT_50S	SPT	SPI GRAPE SCLK 5 17
1230	SPT_50S	SPT	SPI GRAPE CS_L 5 17
1230	SPT_50S	SPT	SPI IPC MISO 5 31
1230	SPT_50S	SPT	SPI IPC MOSI 5 31
1230	SPT_50S	SPT	SPI IPC SCLK 5 31
1230	SPT_50S	SPT	SPI IPC MRDY 5 31

SYNC MASTER=MIKE		SYNC DATE=N/A	
CONSTRAINTS: ASSIGNMENTS			
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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL3, ISL8, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2, ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES

100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP, BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL3, ISL8, ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS


POWER/GND SPACING RULES

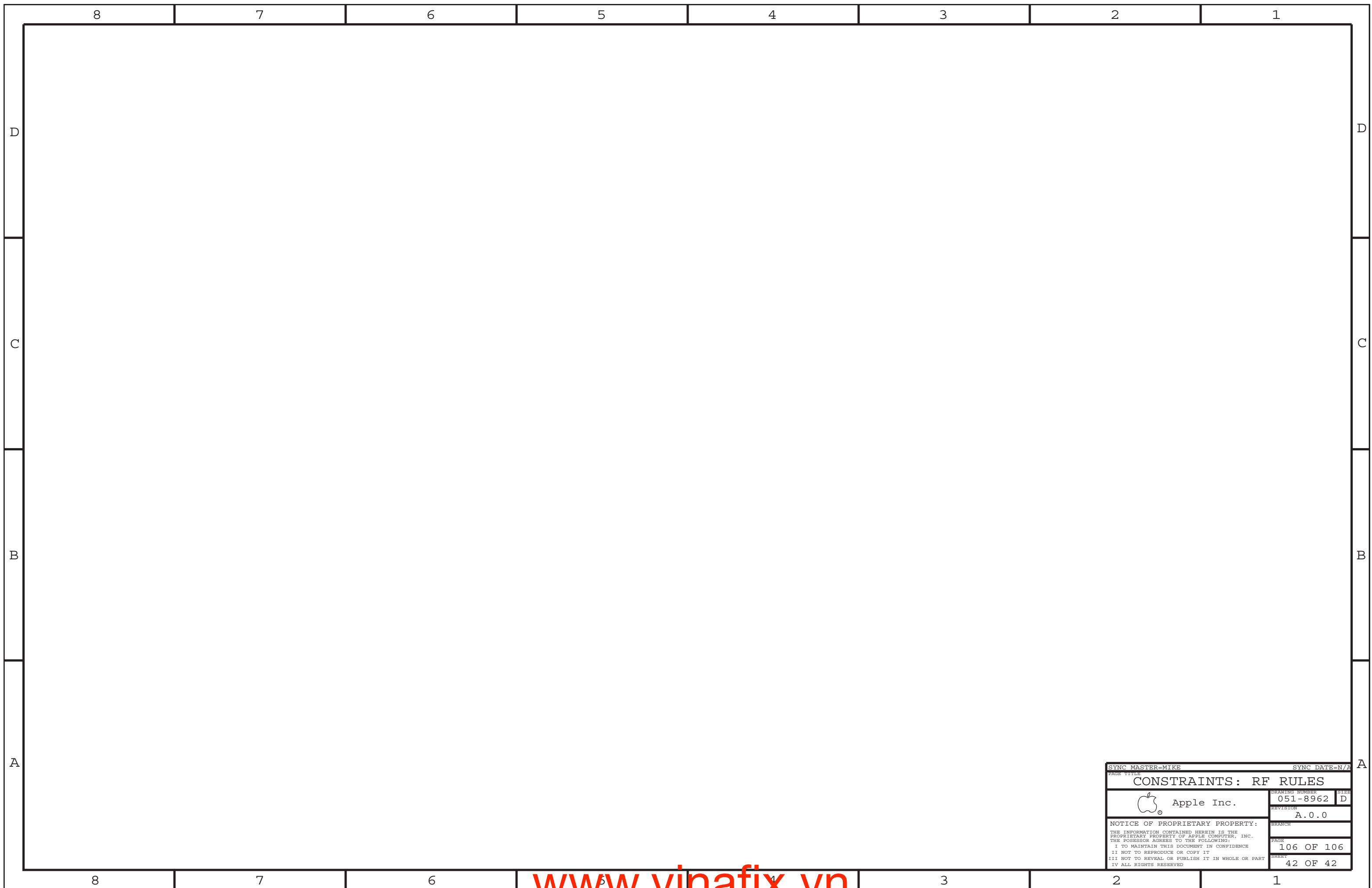
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

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