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<th>Drawing Title</th>
<th>PRODUCTION RELEASED 2010-02-26</th>
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<tr>
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<td>branch</td>
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<tr>
<td>REVISION</td>
<td></td>
</tr>
<tr>
<td>DATE</td>
<td></td>
</tr>
</tbody>
</table>

### Table: Table of Contents

<table>
<thead>
<tr>
<th>Contents</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>
### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>138S0603</td>
<td>NEW IMPROVED INTERSIL PART AS ALTERNATE</td>
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<tr>
<td>152S0796</td>
<td>MURATA AS ALTERNATE</td>
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<tr>
<td>152S0685</td>
<td>ALL</td>
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### Programmable Parts

<table>
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<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>514-0718</td>
<td>IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR</td>
<td></td>
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<tr>
<td>514-0706</td>
<td>IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR</td>
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<tr>
<td>514-0705</td>
<td>IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS</td>
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</tr>
<tr>
<td>514-0704</td>
<td>IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR</td>
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### BOM Groups (project phase-dependent)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>353S2718</td>
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<td>353S2719</td>
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<td>353S2720</td>
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<tr>
<td>353S2721</td>
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### Part Substitutions (differences with K6/K69)

<table>
<thead>
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<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
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<tbody>
<tr>
<td>1341S2677</td>
<td>U5701 WELLSPRING:PROG</td>
<td></td>
</tr>
<tr>
<td>1 U6100</td>
<td>CRITICAL BOOTROM:BLANK</td>
<td></td>
</tr>
<tr>
<td>1 U4900</td>
<td>SMC:PROG_K86</td>
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</tr>
<tr>
<td>1 U4900</td>
<td>SMC:PROG_K87</td>
<td></td>
</tr>
<tr>
<td>3870-1938</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>3870-1939</td>
<td>CRITICAL</td>
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<tr>
<td>3870-1940</td>
<td>CRITICAL</td>
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</tr>
<tr>
<td>1516-0201</td>
<td>FOX_DDR_CONN CRITICAL</td>
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</tr>
<tr>
<td>337S3876</td>
<td>U1400 CRITICAL</td>
<td></td>
</tr>
<tr>
<td>337S3792</td>
<td>IC, SMC, HS8/2117, 9X9MM, TLP, HF</td>
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<tr>
<td>337S3866</td>
<td>IC, MCP89M-A02, 31X31MM, BGA1168</td>
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<tr>
<td>1337S3876</td>
<td>U1400 CRITICAL</td>
<td></td>
</tr>
<tr>
<td>1337S3680</td>
<td>IC, PSOC+ W/ USB, 56 PIN, MLF, CY8C24794</td>
<td></td>
</tr>
<tr>
<td>CDC, SLGYW</td>
<td>PRQ, 1.2, 10W, 800, R0, 1M, BGA</td>
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<td>1337S3680</td>
<td>IC, MCP83M-A02, 31X31MM, BGA1168</td>
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<tr>
<td>1</td>
<td>MCP89M:A01</td>
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<tr>
<td>1</td>
<td>MCP89M:A02</td>
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<tr>
<td>IC, WELLSPRING CONTROLLER, K87</td>
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<tr>
<td>IC, PSOC+ W/ USB, 56 PIN, MLF, CY8C24794</td>
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<tr>
<td>CDC, SLGYW</td>
<td>PRQ, 1.2, 10W, 800, R0, 1M, BGA</td>
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<td>1337S3876</td>
<td>U1400 CRITICAL</td>
<td></td>
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<td>1337S3680</td>
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<tr>
<td>1</td>
<td>MCP89M:A01</td>
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<tr>
<td>1</td>
<td>MCP89M:A02</td>
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<tr>
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<td>IC, PSOC+ W/ USB, 56 PIN, MLF, CY8C24794</td>
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<td>CDC, SLGYW</td>
<td>PRQ, 1.2, 10W, 800, R0, 1M, BGA</td>
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</table>

### K86/K87 BOARD STACK-UP

<table>
<thead>
<tr>
<th>SIGNAL(High Speed)</th>
<th>GROUND</th>
<th>POWER</th>
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</thead>
<tbody>
<tr>
<td>2</td>
<td>SIGNAL(High Speed)</td>
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</tr>
<tr>
<td>3</td>
<td>SIGNAL(High Speed)</td>
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<td>4</td>
<td>SIGNAL(High Speed)</td>
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<tr>
<td>5</td>
<td>POWER</td>
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<tr>
<td>6</td>
<td>POWER</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>GROUND</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>GROUND</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>SIGNAL(High Speed)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>SIGNAL(High Speed)</td>
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<tr>
<td>11</td>
<td>GROUND</td>
<td></td>
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</table>

### Background

- **Part Substitutions (differences with K6/K69)**: These parts are used to replace the original parts in the K6/K69 models. The new parts are indicated with different part numbers and descriptions.
- **Programmable Parts**: These parts are designed to be programmed with specific functions, such as audio connectors and Mini DP connectors, and are marked as programmable parts.
- **Alternate Parts**:

---

**Note**: The image contains detailed diagrams and tables that are not fully transcribed here due to the complexity and nature of the content. The transcribed information includes key parts and their descriptions, along with notes on part substitutions and programmable parts.
csa 37: Per <rdar://problem/7554342> K86/K87: Change L3720 to 152S1182.

csa 34: Added BOM entry under Module Parts table to include CULV processor (337S3779) to minimize delta on this page between K86 and K87 per Diana.

csa 2: Updated CPU block text to include CPU description for both K86 and K87.

csa 98: Deleted net properties for =PPBUS_S0_LCDBKLT.

Changed component color to Green.

Added IMVP6:2PHASE to R7413 per Intersil.

csa 74: Changed C7434 from NOSTUFF to IMVP6:2PHASE per Intersil.

csa 3: Added BOM table entry for MCP83M (337S3876).

csa 55: Added parentheses for SYNC_DATE property on all pages that have broken sync.


T27: Changed RC balance on BATT_ISENSE, same time constant (pg. 54).

T27: Added gain note for U5402 and SMC_BATT_ISENSE (pg. 54).

csa 54: Began syncing from T27 per <radar:7432091 > BATT_ISENSE filter change to address lower max sink current on ISL6259 BMON pin (K17 auto-shutdown issue).

csa 69: Added OMIT to J6955, BOM table to stuff K84 Hall effect connector.

Added C4585, C4586 (10pF, 5%, 131S0029) and NOSTUFFed multiple.

Added parentheses for SYNC_DATE property on all pages that have broken sync.

csa 45: Added passive deemphasis to SATA HDD D2R lines:

- Added BOM table entry for MCP83M (337S3876).

csa 20; T27: Added CKPLUS_WAIVE properties to dismiss false errors (pg. 20). <radar:7368529> TASK: Waive false CheckPlus errors

- MCO: 056-3515
- PCBF: 820-2801
- BOM: 639-0680

Created SMC:PROG_K87 pointing to 341T0252 (SUBASSY, IC, SMC, K87).

Changed BOOTROM:PROG to call out 341T0251 (SUBASSY, IC, BOOT ROM, K86/K87).

Per <rdar://problem/7495072> K87: Call out LED:K86_K87 BOMOPTION in the K87_MISC BOM group.

This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86.

Added BOM table entry for MCP83M (337S3876).
Functional Test Points

- Microwave Connectors Func_Test
- Mic Func_Test
- Speaker Func_Test
- PVR Func_Test
- LVDS Func_Test
- USB Camera Conn
- DC Power Conn

- Power Supply Func_Test
- JPLP SPI+SPI Conn Func_Test

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CPU VCore HF and Bulk Decoupling

**PLACEMENT_NOTE (C1240-C1243):**
Place inside socket cavity on secondary side.

**PLACEMENT_NOTE (C1200-C1209):**
CPU VCore HF and Bulk Decoupling

**VCCP (CPU I/O) DECOUPLING**

1. C1223, CRITICAL, 4.7UF, 4V, X5R-1, 20%
2. C1207, CRITICAL, 4.7UF, 4V, X5R-1, 20%
3. C1215, CRITICAL, 4.7UF, 4V, X5R-1, 20%
4. C1245, CRITICAL, 22UF, 402, 20%
5. C1219, CRITICAL, 4.7UF, 4V, X5R-1, 20%
6. C1209, 4.7UF, 22UF, 22UF, 20%
7. C1251, 4.7UF, 4V, X5R-1, 20%
8. C1232, 22UF, 402, 20%
9. C1220, CRITICAL, 4.7UF, 4V, X5R-1, 20%

**VCCA (CPU AVdd) DECOUPLING**

1. C1225, CRITICAL, 0.1UF, 402, 10V
2. C1223, CRITICAL, 0.1UF, 402, 10V
3. C1240, CRITICAL, 4.7UF, 402, 20%
4. C1219, CRITICAL, 4.7UF, 402, 20%
5. C1264, 4.7UF, 402, 20%

---

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
USE WITH XSB-0722 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP89-SPECIFIC PINOUT

Direction of XDP module
Please avoid any obstructions
ON ODD-NUMBERED SIDE OF J1300

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.
Loop-back clock for delay matching.

---

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---

**SYNC_MASTER=K87_MLB  SYNC_DATE=02/26/2010**

---

**APPLE INC. 361-8407-A  A.O. S**

---

**MCP CPU Interface**

---

**www.vinafix.vn**

PCi Express

MCP PCIe Interfaces

Apple Inc.


MCP PCIe Interfaces

Apple Inc.


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MCP PCIe Interfaces

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DDC Mode Pull-downs

NOTE: If dual-mode DisplayPort (DP+), if unused no pull-ups are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

GPIO Pull-Ups

NOTE: SMBus pull-downs required if SMBUS_DET/MIKEY_MG_DET are not used.

TMDS: Power +VDD_IFPx at 3.3V
LVDS: Power +VDD_IFPx at 1.8V

NOTE: No Composite/S-Video/Component Video support on MCP89.
Connect +3.3V_RGBDAC pin to GND.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).

NOTE: TMDS/HDMI not supported on IFPA/B for MCP89 A01.

MCP Signal

TMDS_IG_DDC_CLK
TMDS_IG_DDC_DATA
TMDS_IG_TXD_P/N<5>
TMDS_IG_TXD_P/N<3>
TMDS_IG_TXD_P/N<1>
TMDS_IG_TXD_P/N<0>
(UNUSED)
(UNUSED)
TMDS_IG_TXD_P/N<1>
TMDS_IG_TXD_P/N<0>
LVDS_IG_A_DATA_P/N<0>
LVDS_IG_B_DATA_P/N<0>
LVDS_IG_B_DATA_P/N<1>
LVDS_IG_B_DATA_P/N<2>
LVDS

NOTE: Only pull-ups are necessary, if used for TMDS/HDMI only then DDC Mode Pull-downs are required for use as GPIOs.
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89.
Connect +3.3V_RGBDAC pin to GND.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).

NOTE: TMDS/HDMI not supported on IFPA/B for MCP89 A01.

VDD_COREx_SENSE signals should NOT be used for remote sensing unless regulators are powered by separate regulators. Non-core regulator sense point as close to Core FET as possible.

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless regulators are powered by separate regulators. Non-core regulator sense point as close to Core FET as possible.

MCP89M-A01
OMIT

NOTE: "SN" rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.
C2300 helps reduce input rail drop during Q2300 turn-on.

Approx. Ramp Time (EN to 1.35V, us): 7.91 + 0.0678 * R1 (Kohms)

Drift during Q2300 turn-on.

C2300 helps reduce input rail drop during Q2300 turn-on.

Approx. Ramp Time (EN to 1.35V, us): 7.91 + 0.0678 * R1 (Kohms)

Drift during Q2300 turn-on.

**DIMM CKE Clamps**

- CKE must be held low to keep memory in self-refresh.
- Clamps enable before MCP89 MEMVDD rail switched off.
- Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
- Clamps are necessary because MEMVDD is used by CKE signals. A 100k termination resistor on each CKE signal on DIMM is chosen for low output capacitance.

**NOTE:**

- Gated Rail Savings: 120mW
- Infineon BSC030N03MS for Q2300.
- **C2400 helps reduce input rail droop during GFX02 fast turn-on.**
  
- **Max Ramp-Up Time:** 1500 uS (ENABLE to 90%)
  
- **Min Ramp-Up Time:** 100 uS (10% to 90%)
  
- **FET Ron <= 2.5 mOhms**
  
- **Gated Rail Savings:** 860mW

### NV Requirements:
- Fast Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

**NOTE:** NVIDIA recommends INFINEON BSC020N03MS for Q2400.

- **Q2400** helps reduce input rail droop during fast turn-on.

---

### Critical Components:

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Loading</th>
<th>Rds(on)</th>
<th>Remarks</th>
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</thead>
<tbody>
<tr>
<td>XW2400</td>
<td>SO-8</td>
<td>SM</td>
<td>3.2 mOhm @2.5V</td>
<td></td>
</tr>
<tr>
<td>XW2401</td>
<td>SO-8</td>
<td>SM</td>
<td>20% 6.3V</td>
<td></td>
</tr>
<tr>
<td>C2400</td>
<td>TDFN</td>
<td>CRITICAL</td>
<td>20% 6.3V</td>
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</tbody>
</table>

**Component Placement:**
- **PLACE_NEAR=C2400.2:1 mm**
- **PLACE_NEAR=C2400.3:1 mm**
- **PLACE_NEAR=C2400.5:2 mm**

**Capacitor Specifications:**

<table>
<thead>
<tr>
<th>Type</th>
<th>Part</th>
<th>Value</th>
<th>Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>CERM-X5R 1206-1</td>
<td>C2405</td>
<td>20% 6.3V</td>
<td></td>
</tr>
<tr>
<td>CERM-1 402 820PF</td>
<td>C2406</td>
<td>10% 50V</td>
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</table>

**Resistor Specifications:**

<table>
<thead>
<tr>
<th>Type</th>
<th>Part</th>
<th>Value</th>
<th>Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1&gt; 0.1UF</td>
<td>U2405</td>
<td>8020%</td>
<td></td>
</tr>
<tr>
<td>820PF</td>
<td>U2406</td>
<td>8020%</td>
<td></td>
</tr>
</tbody>
</table>

- **MCP 3.3V RGBDAC Power**
  - If RGBDAC is not used, tie to GND.
  - Plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.
  - If RGBDAC is used, requires ferrite (155S0382)

- **MCP Graphics Core Power**
  - 15350 mA (0.85V)

- **MCP 1.05V DisplayPort Power**
  - 140 mA

- **MCP IFP PLL Power**
  - 60 mA

- **MCP IFP AB RSET**
  - MCP_IFPAB_RSET

- **MCP IFP AB VPROBE**
  - MCP_IFPAB_VPROBE

- **MCP TMDS0_VPROBE**
  - MCP_TMDS0_VPROBE

- **MCP TMDS0_RSET**
  - MCP_TMDS0_RSET

- **PP1V05_S0_MCP_PLL_IFP**
  - =PP1V05_S0_MCP_PLL_VDD

- **PP1V05_S0_MCP_DP0_VDD**
  - =PP1V05_S0_MCP_DP0_VDD

- **PP3V3_S0_MCP_DAC**

- **PPVCORE_SW_MCP_GFX**

- **SYNC_DATE=02/26/2010**
  - SYNC_MASTER=K87_MLB

- **MAKE_BASE=TRUE**

- **MIN_LINE_WIDTH=0.4 MM**
  - MIN_NECK_WIDTH=0.2 MM

- **VOLTAGE=0V**
  - GND_MCP_DAC_P3V3

- **PP3V3_S0_MCP_DAC**
RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

System Reset Circuit

Platform Reset Connections
LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

DO NOT SYNC WITH T27, REMOVED PCIE RESET SIGNALS +CAESAR XTAL

Apple Inc.

SYNC_DATE=02/26/2010

SYNC_MASTER=K87_MLB

SB Misc
We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
CPU Voltage Sense / Filter

MCP Voltage Sense / Filter

PBUS Voltage Sense Enable & Filter
MCP MEM VDD Current Sense / Filter

MCP VCore Current Sense Filter

MCP CPU 1.05V AND CPU VCore High-Side Current Sense / Filter

CPU VCore Load Side Current Sense / Filter

Battery (BMON) Current Sense, MUX & Filter

DC-IN (AMON) Current Sense Filter

Current Sensing

Apple Inc.
CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR

Placement note: Place close to J4501 in a convenient location.

DETECT HDD TEMPERATURE

DETECT CPU DIE TEMPERATURE

DETECT FIN-STACK TEMPERATURE

MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR

Placement note: Place close to J4502 in a convenient location.

DETECT MCP DIE TEMPERATURE

DETECT MCP PROXIMITY TEMPERATURE

DETECT HDD TEMPERATURE
PSOC USB CONTROLLER

TPAD Buttons Disable

SMC Manual Reset & Isolation

Keyboard Connector
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROP LINE REGULATION
- Ripple to meet EMI
- Start-up time less than 2ms
- R5812,R5813,C5818 MODIFIED

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROP LINE REGULATION
- Ripple to meet EMI
- Start-up time less than 2ms
- R5812,R5813,C5818 MODIFIED

IPD Flex Connector

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DO NOT SYNC FROM T27. REMOVED KEYBOARD BKLIGHT CIRCUIT

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R5921 Pulls up SEL pins to enter standby mode when pin is not being driven by SMC.

Analog SMS

C5923: 0.033uF 16V 10%
C5924: 0.033uF 16V 10%
C5926: 0.01uF CERM402 10%

PLACE_NEAR=U4900.M10:2.54MM
PLACE_NEAR=U4900.K10:2.54MM
PLACE_NEAR=U4900.N9:2.54MM

R5922: 10K MF-LF 402 5% 1/16W
R5921 Pulls up SEL pins to enter standby mode when pin is not being driven by SMC.

DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923, C5924, C5925. ADDED PLACE NEARS.

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NOTE: If HOLD* is asserted, ROM will ignore SPI cycles.

NOTE: 42 & 62 MHz use FAST_READ command.

MCP89 SPI Frequency Select:

- Frequency | SPI_MOSI | SPI_CLK
- 25.0 MHz  | 0       | 0
- 31.2 MHz  | 0       | 1
- 41.7 MHz  | 1       | 0
- 62.5 MHz  | 1       | 1

NOTE: 42 & 62 MHz use FAST_READ command.
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.15K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HF = 3.6 HZ
FC_LO = 43KHZ
VIN = 2V RMS, CODEC VIN = 1.14V RMS

CODEC RIN = 20K OHMS
NET RIN = 10.15K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HF = 3.6 HZ
FC_LO = 43KHZ
VIN = 2V RMS, CODEC VIN = 1.14V RMS

LINE INPUT FILTER

AUD_LI_REF
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
AUD_LI_GND
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
AUD_LI_L_DIV AUD_LI_P_L
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
AUD_LI_R
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
AUD_LI_P_R
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
AUD_LI_L
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
AUD_LI_R_DIV
MIN LINE WIDTH=.1MM
MIN NECK WIDTH=.1MM
GND_AUDIO_CODEC
5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

PLACE_NEAR=Q7260.2:1.5 MM

0.001UF CERM 50V 20%

PLACE_NEAR=XW7203 by Pin 1 OF L7260.

PLACE_NEAR=XW7202 by C7292.

CRITICAL

XW7204

PLACE_NEAR=Q7221.2:1.5 MM

CRITICAL

R7220

DIDT=TRUE

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.6 MM

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.6 MM

ROUTE NOTE:

MAX CURRENT = 13.3A
PWM FREQ. = 300 KHZ

RJK0384DPA 4.7UH-10A

CRITICAL

XW7205

PLACE_NEAR=XW7201 between Pin 15 and Pin 25 of U7200.

ROUTE NOTE:

MAX CURRENT = 9.1A
PWM FREQ. = 375 KHZ

SYNC_MASTER=K87_MLB
SYNC_DATE=02/26/2010

5V/3.3V SUPPLY

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3.3V S3 FET

1.5V S0 FET

3.3V S0 FET

0.9V ENET FET

5.0V S0 FET

5.0V LT S0 FET

DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT
DO NOT SYNC. K6 PAGE WITH K84 CONNECTOR
13.3 Inch, K84 Panel (9 LEDs per string)

TARGET: ISET = 15 mA, VSET = 2.5 V
ACTUAL: ISET = 153 mA, VSET = 3.5 V

10.2 ohm resistors for current measurement on LED strings.
MCP89 drives them low.

MCP79 had internal 10K pull-up for these signals.

MCP 89 drives them low.

MCP 79 had internal 10K pull-up for these signals.

LVDS_IG_BKL_ON

LVDS_IG_BKL_PWM

SYNC_DATE=02/26/2010

SYNC_MASTER=K87_MLB

LCD Backlight Support

Critical FDC638APZ_SBMS001

Q9807 SSM6N15FEAPE SOT563

www.vinafix.vn
Some signals require 27.4-ohm single-ended impedance.

CPU Signal Constraints

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Signals within each 4x group should be matched within 5 ps of strobe.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

CPU / FSB Net Properties

MCP FSB COMP

CPU_VCCSENSE * 25 MIL

FSB_ADSTB *

CPU_VCCSENSE * 27P4_OHM_SE

FSB_DSTB * =50_OHM_SE

FSB_DATA * =50_OHM_SE

FSB_50S =50_OHM_SE

CPU_IERR_L CPU_50S

CPU_ASYNC

CPU_DPRSTP_L

FSB_CPUSLP_L

CPU_ASYNC

CPU_SMI_L

CPU_PWRGD

CPU_PROCHOT_L

CPU_FERR_L

CPU_BSEL

FSB_1X

CPU_VCCSENSE

CPU_GTLREF

CPU_COMP

CPU_50S

MCP_CPU_COMP_GND

MCP_CPU_COMP_VCC

MCP_50S

CLK_FSB_100D

CLK_FSB

CLK_FSB_100D

CLK_FSB

FSB_CLK_CPU_N

CPU_50S

CPU_50S

CPU_AGTLCPU_50S

CPU_AGTLCPU_50S

CPU_AGTLCPU_50S

CPU_AGTLCPU_50S

CPU_AGTLCPU_INIT_L

CPU_AGTLCPU_50S

FSB_1X

FSB_50S

FSB_50S

FSB_50S

FSB_DSTB_50S

PHYSICAL

CPU_COMP<1>

CPU_VCCSENSECPU_27P4S

CPU_VCCSENSECPU_VCCSENSE

CPU_8MIL

XDP_TCK

XDP_BPM_T<4..0>

CPU_ITPXDP_TCK

CPU_ITPXDP_TMS

CPU_ITPXDP_DX

CPU_VCCSENSEL

CPU_VCCSENSEL

CPU_VCCSENSEL

CPU_VCCSENSEL

CPU_VCCSENSEL

CPU_VCCSENSEL

CPU_VCCSENSEL

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CPU_VCCSENSEL

CPU_VCCSENSE
Memory Bus Constraints

CMD/CTRL signals should be matched within 150 ps.
No DQS to clock matching requirement.
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps.

Memory Net Properties

Memory Bus Spacing Group Assignments

DDR3: No signals should be matched within 6 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 560 ps.
No DQS to clock matching requirement.
DQS intra-pair matching should be within 2 ps, inter-pair matching should be within 100 ps.

SOURCE: MCP89 Interface DG (ID:004613-001_V7.9), Section 2.2.2
SOURCE: Apple Inc. 
SYNC_DATE=02/26/2010
SYNC_MASTER=K87_MLB

MCP MEM COMP Signal Constraints
NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

Digital Video Signal Constraints

SATA Interface Constraints

PCI-Express

MCP89 Net Properties

MCP Constraints

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### Ethernet Constraints

**Table 1: Ethernet PHY Constraints**

<table>
<thead>
<tr>
<th>Constraint Description</th>
<th>Min/Max Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENET_MDI_100D</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>ENET_MII_100S</td>
<td>55_OHM_SE</td>
</tr>
<tr>
<td>ENET_CLK125M_RXCLK</td>
<td>=100_OHM_DIFF</td>
</tr>
<tr>
<td>ENET_CLK125M_TXCLK</td>
<td>=55_OHM_SE</td>
</tr>
<tr>
<td>ENET_TXD0</td>
<td>ENET_RESET_L</td>
</tr>
<tr>
<td>ENET_RXD&lt;3..0&gt;</td>
<td>ENET_RXD&lt;3..0&gt;</td>
</tr>
<tr>
<td>ENET_MDC</td>
<td>MCP_MII_COMP</td>
</tr>
<tr>
<td>ENET_MDI_P&lt;3..0&gt;</td>
<td>MCP_MII_COMP</td>
</tr>
<tr>
<td>ENET_MDI_N&lt;3..0&gt;</td>
<td>MCP_MII_COMP</td>
</tr>
</tbody>
</table>

**Table 2: Electrical Constraints**

<table>
<thead>
<tr>
<th>Constraint Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENET_MII_55S</td>
<td>ENET_MII</td>
</tr>
<tr>
<td>ENET_MII</td>
<td>ENET_MII</td>
</tr>
<tr>
<td>ENET_TXD&lt;3..1&gt;</td>
<td>ENET_MII</td>
</tr>
<tr>
<td>ENET_CLK125M_RXCLK</td>
<td>=100_OHM_DIFF</td>
</tr>
<tr>
<td>ENET_CLK125M_TXCLK</td>
<td>=55_OHM_SE</td>
</tr>
<tr>
<td>ENET_INTR_L</td>
<td>ENET_INTR_L</td>
</tr>
<tr>
<td>MCP_CLK25M_BUF0_R</td>
<td>MCP_CLK25M_BUF0_R</td>
</tr>
<tr>
<td>MCP_MII_COMP</td>
<td>MCP_MII_COMP</td>
</tr>
<tr>
<td>MCP_MII_COMP_GND</td>
<td>MCP_MII_COMP</td>
</tr>
<tr>
<td>MCP_MII_COMP_VDD</td>
<td>MCP_MII_COMP</td>
</tr>
</tbody>
</table>

**Notes:**
- SYNC_MASTER = K87_MLB
- SYNC_DATE = 02/26/2010
- Source: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4
### K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

<table>
<thead>
<tr>
<th>LAYER MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ON LAYER?</strong></td>
<td><strong>Y</strong></td>
<td><strong>0.244 MM</strong></td>
<td><strong>0.100 MM</strong></td>
</tr>
</tbody>
</table>

- **ISL3, ISL4, ISL9, ISL10**
  - 100_OHM_DIFF:
    - TOP, BOTTOM:
      - Y:
        - **0.091 MM**
      - N:
        - **0.230 MM**
  - 90_OHM_DIFF:
    - **=STANDARD**
  - 70_OHM_DIFF:
    - **=STANDARD**
  - 55_OHM_SE:
    - **=STANDARD**
  - 50_OHM_SE:
    - **=STANDARD**
  - 77P4_OHM_SE:
    - **=STANDARD**
  - 70_OHM_DIFF (TOP, BOTTOM):
    - **0.185 MM**
  - 55_OHM_SE (TOP, BOTTOM):
    - **=STANDARD**
  - 50_OHM_SE (TOP, BOTTOM):
    - **=STANDARD**
  - 77P4_OHM_SE (TOP, BOTTOM):
    - **=STANDARD**

- **MINIMUM LINE WIDTH**:
  - ALLOW ROUTE:
    - **=STANDARD**
  - **=STANDARD**

- **LINE-TO-LINE SPACING**:
  - **=DEFAULT**
  - **=DEFAULT**

- **NET_SPACING**:
  - **=DEFAULT**
  - **=DEFAULT**
  - **=DEFAULT**

- **AREA_TYPE**:  
  - **=DEFAULT**

- **SUPERPOSITION**  
  - **=DEFAULT**

- **VERSION**:  
  - **=DEFAULT**