1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,MLB,PBG4

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		193222	PRODUCTION RELEASE	11/27/01	?

11/27/2001

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6223	1	SCHEMATIC,MLB,PBG4	SCH1	
820-1263	1	PCBF,MLB,PBG4	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

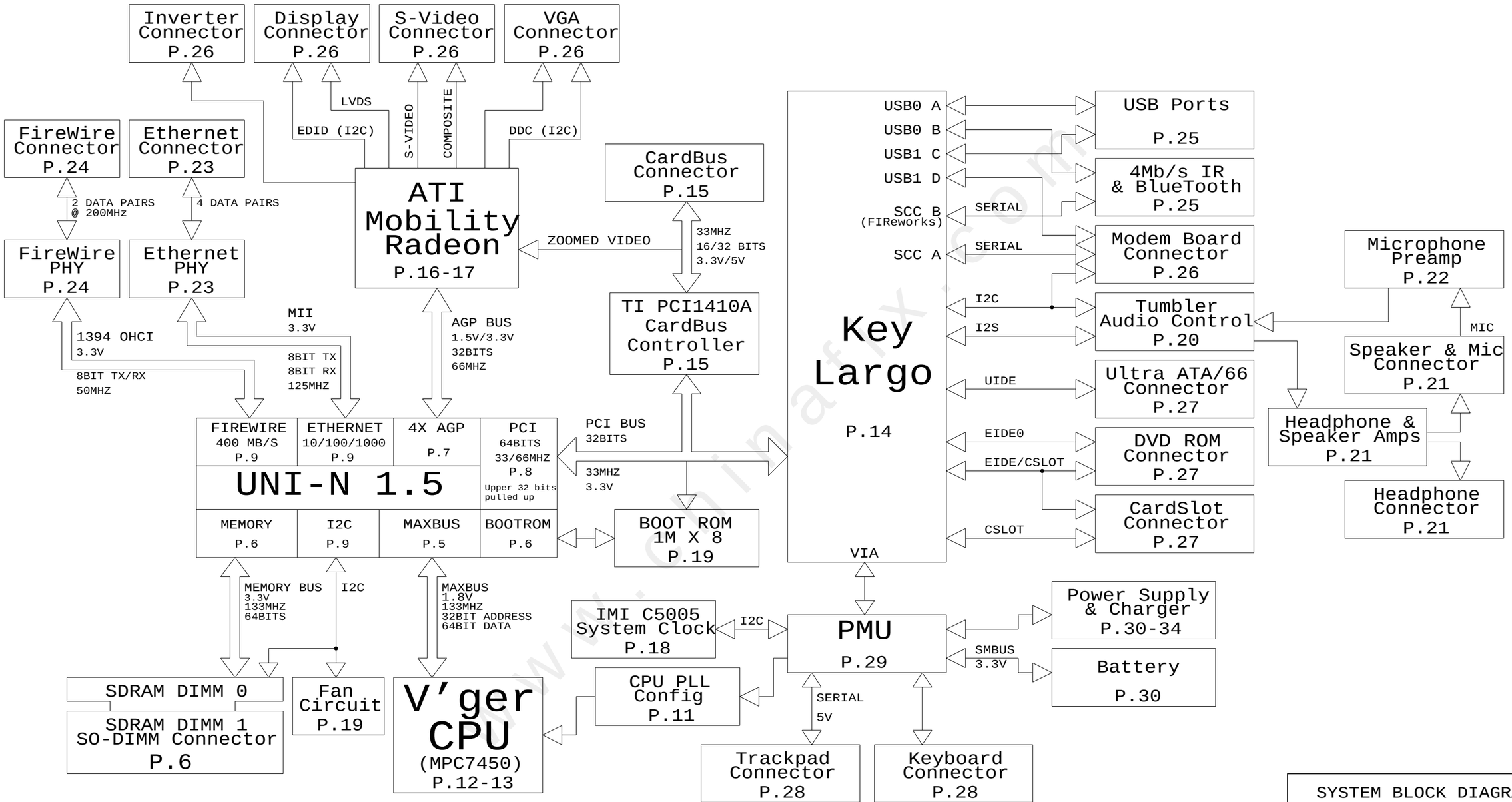
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEMATIC,MLB,PBG4

DRAWING NUMBER 051-6223 REV. A

SHT 1 OF 41



SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 2 OF 41	

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN

INPUT14_24V

BUCK REGULATOR CHARGER (LTC1625)

PBUS

BACKLIGHT INVERTER

DCDC_EN

$\overline{SD}$
ON3
ON5

MAIN 3V/5V DC/DC CONVERTER (MAX785)

+3.3V

+5V

DC/DC (MAX1717) $\overline{SHDN}$

CPU_VCORE (+1.4V)

DCDC_EN
SLEEP

DC/DC (MAX1644B) $\overline{SHDN}$

+1.8V MAX BUS INTERFACE
CPU I/O
ATI M6 CORE

DCDC_EN

DC/DC (MAX1644B) $\overline{SHDN}$

+2.5V ATI M6 DDR I/O

DCDC_EN

BACKUP BATTERY CIRCUIT DESIGNED TO CHARGE BATTERY OFF PBUS, AND KEEP PBUS FROM DROPPING BELOW 6V UNTIL BACKUP BATTERY IS DRAINED

BACKUP BATTERY

CHARGER & BOOST OUTPUT

BBATT_ENABLE
(OUTPUT)

4S 2P LITHIUM ION

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A

SCALE: NONE

SHT 3 OF 41

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
PREPREG THICKNESS: 3 - 6 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1 SIGNAL (1/2 OZ)

2 GROUND (1/2 OZ)

3 SIGNAL (1/2 OZ)

4 SIGNAL (1 OZ)

5 GROUND (1 OZ)

6 CUT POWER PLANE(DEFAULT 5V) POWER/SIGNAL (1 OZ)

7 CUT POWER PLANE(DEFAULT 3V) POWER (1 OZ)

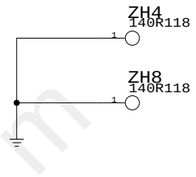
8 SIGNAL (1/2 OZ)

9 GROUND (1/2 OZ)

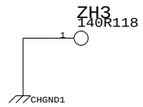
10 SIGNAL (1/2 OZ)

BOARD HOLES

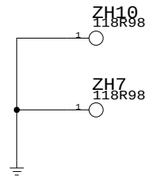
CPU HEATSINK MOUNTS

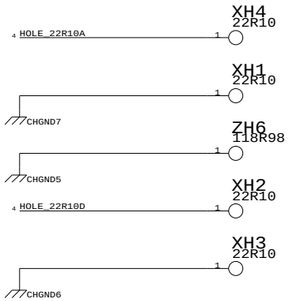


TIED TO CHGND1

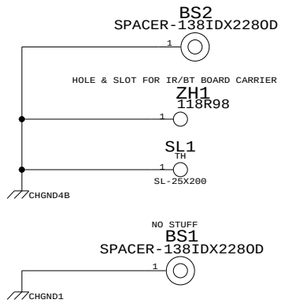


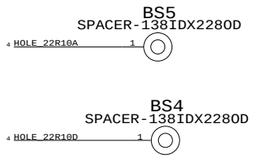
CARDBUS CONN MOUNTS



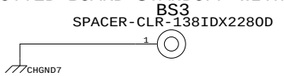


PCB BOARD STANDOFFS





SLOTTED BOARD STANDOFF WITH COLLAR



MISC. INFORMATION

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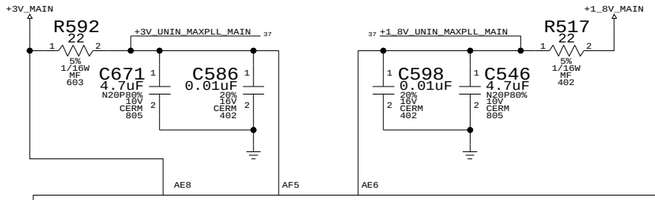
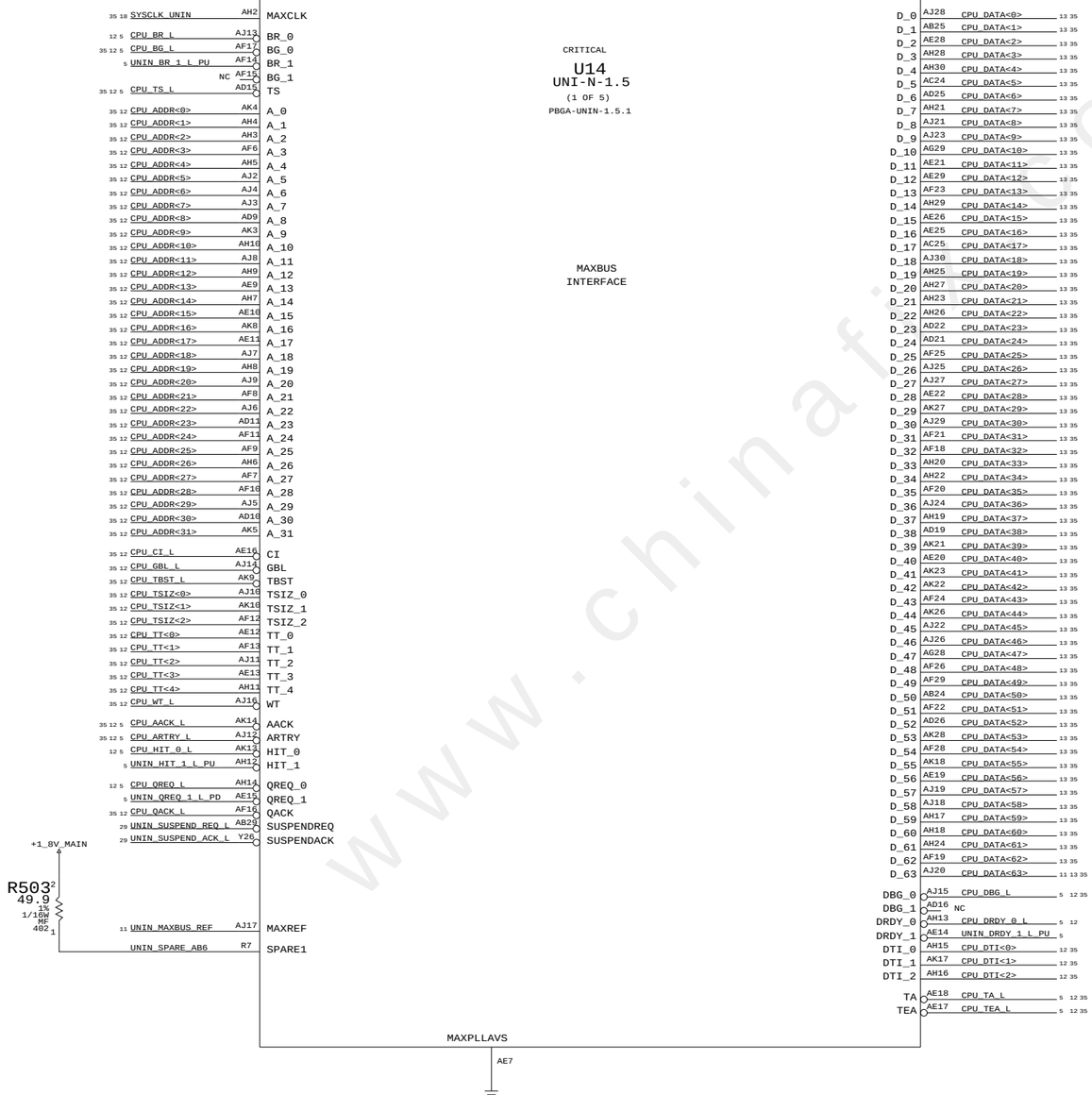
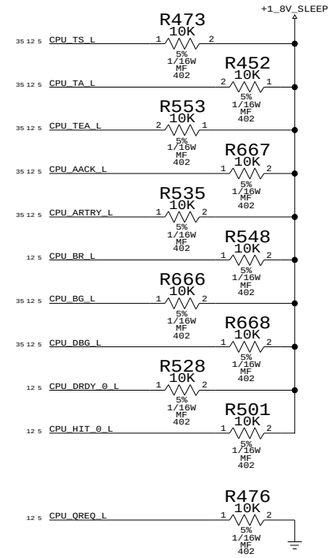
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6223	REV. A
	SCALE NONE	SHT 4 OF 41	

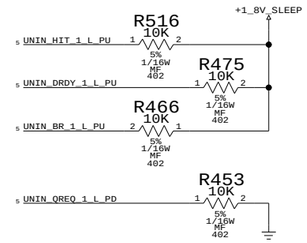




MAXBUS PULL-UPS



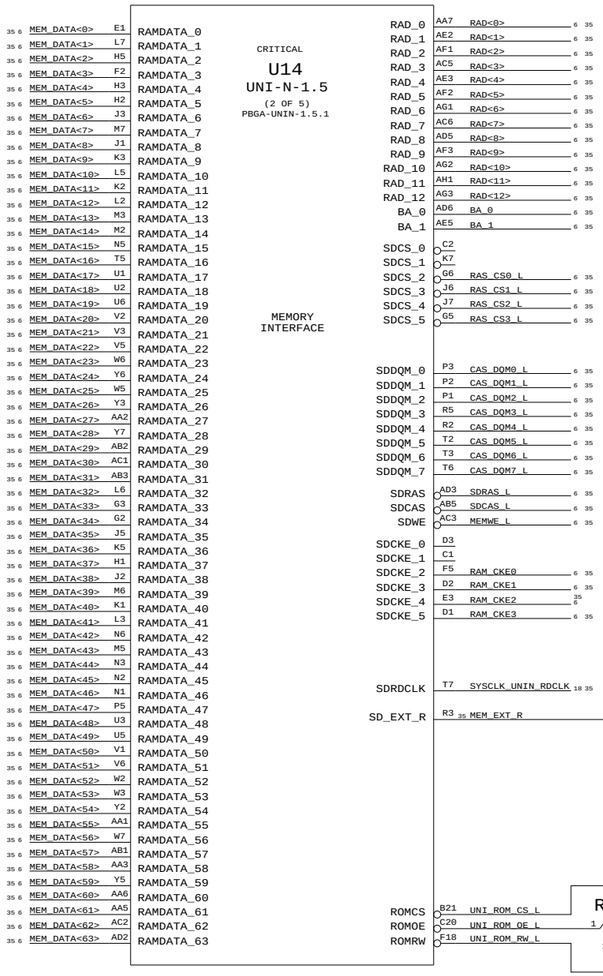
UNI-N SECONDARY PROCESSOR SUPPORT

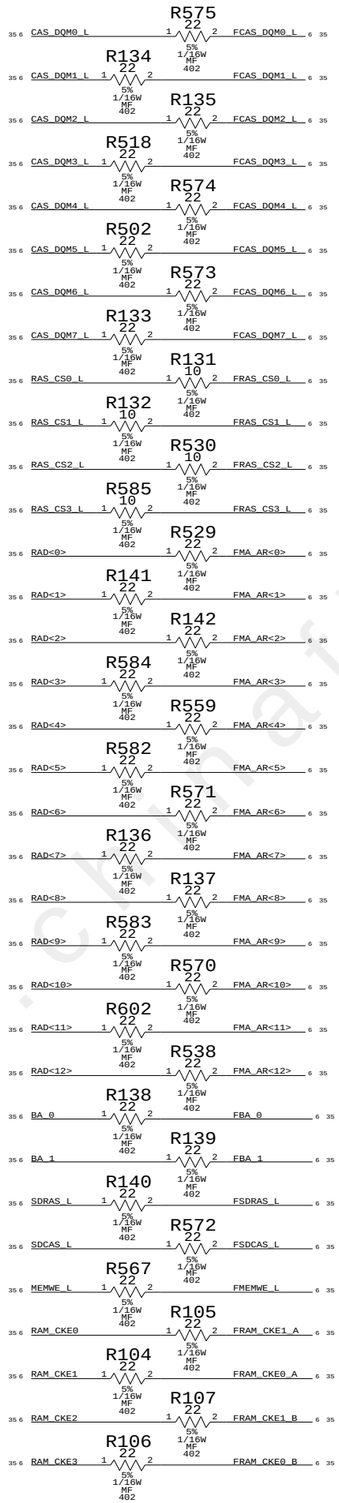


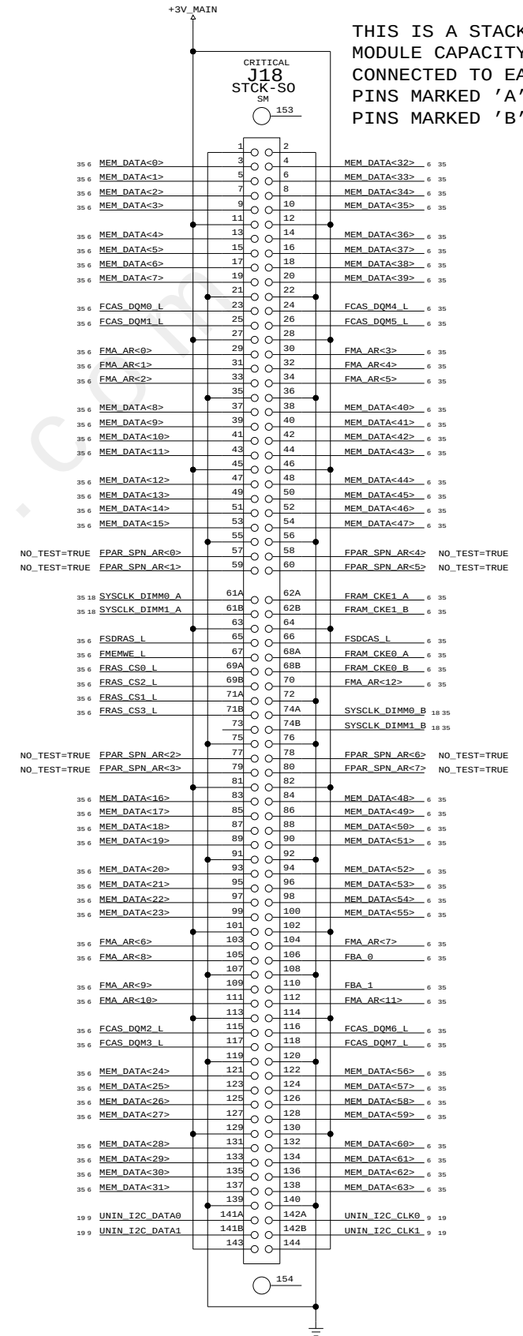
UNI-N MAXBUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 5 OF 41	





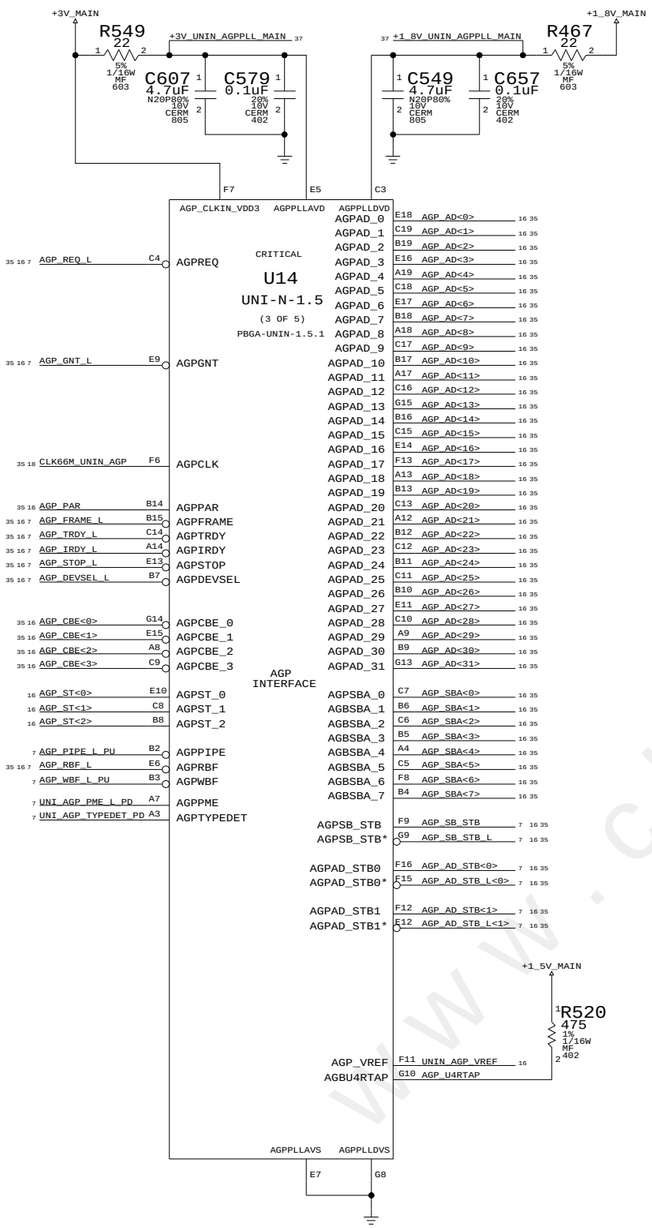


THIS IS A STACKED DIMM CONNECTOR WITH A 2 MODULE CAPACITY. PINS THAT HAVE AN A/B ARE CONNECTED TO EACH OF THE SEPARATE DIMMS. PINS MARKED 'A' GO TO THE TOP MODULE AND PINS MARKED 'B' GO TO THE BOTTOM MODULE.

UNI-N MEMORY

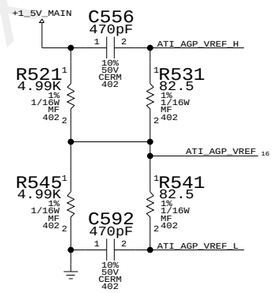
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 6 OF 41	

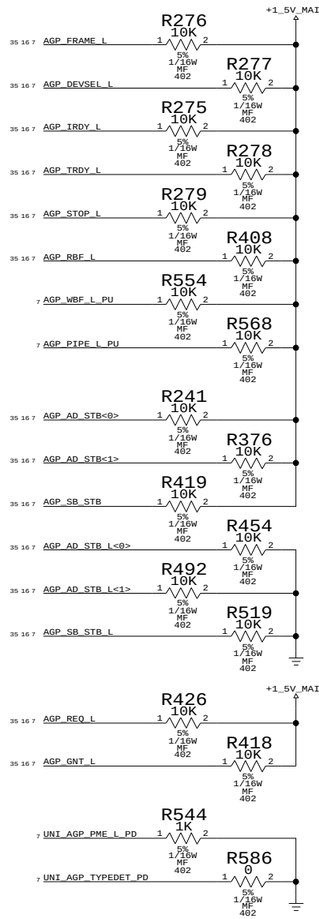


ATI AGP I/O REFERENCE

(PLACE CLOSE TO UNI-N AGP BALLS)



AGP PULL-UPS



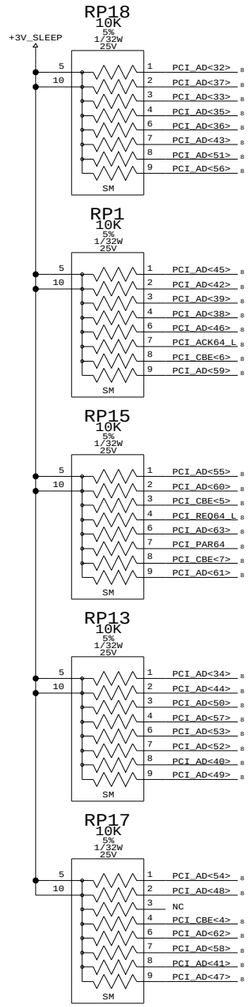
UNI-N AGP

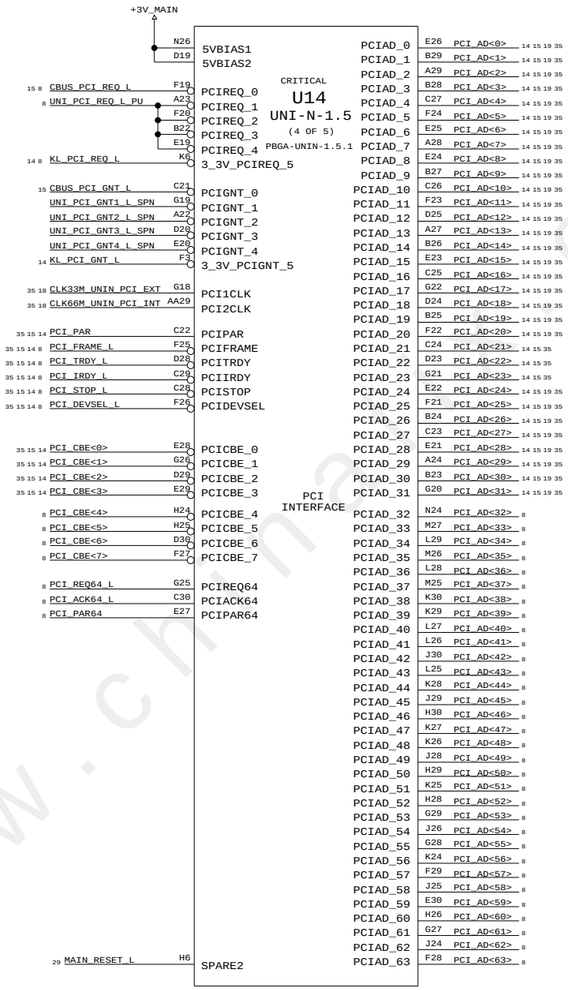
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A

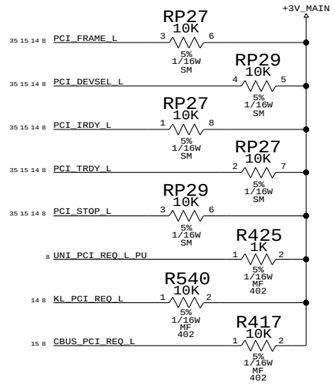
SCALE	SHT	OF
NONE	7	41

64-BIT PCI SUPPORT





PCI PULL-UPS



UNI-N PCI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 8 OF 41	

UNI-N I2C PULL-UPS

+3V_MAIN

R249 10K 5% 1/16W MF 402 — UNIN_I2C_CLK0 (6 9 19)
R288 10K 5% 1/16W MF 402 — UNIN_I2C_DATA0 (6 9 19)
R238 10K 5% 1/16W MF 402 — UNIN_I2C_CLK1 (6 9 19)
R287 10K 5% 1/16W MF 402 — UNIN_I2C_DATA1 (6 9 19)

UNI-N ETHERNET TERMINATION

ENET_PHY_TX_EN (36 23)	R240 33 5% 1/16W MF 402	
ENET_PHY_TX_ER (36 23)	R202 33 5% 1/16W MF 402	
ENET_PHY_TXD<0> (36 23)	R224 33 5% 1/16W MF 402	
ENET_PHY_TXD<1> (36 23)	R251 33 5% 1/16W MF 402	
ENET_PHY_TXD<2> (36 23)	R252 33 5% 1/16W MF 402	
ENET_PHY_TXD<3> (36 23)	R203 33 5% 1/16W MF 402	
ENET_PHY_TXD<4> (36 23)	R396 33 5% 1/16W MF 402	
ENET_PHY_TXD<5> (36 23)	R274 33 5% 1/16W MF 402	
ENET_PHY_TXD<6> (36 23)	R239 33 5% 1/16W MF 402	
ENET_PHY_TXD<7> (36 23)	R375 33 5% 1/16W MF 402	
ENET_PHY_GTX_CLK (35 23)	R334 33 5% 1/16W MF 402	

+1_8V_MAIN — VDDC X 18 (N13 N15 N17 P13 P15 P17 R13 R15 R17 T13 T15 T17 U13 U15 U17 V13 V15 V17)
+3V_MAIN — VDD_RAM X 18 (AB4 AC7 AD1 AE4 AJ1 B1 F1 G4 H7 K4 L1 N4 N7 R1 T4 U7 W1 W4 R24 F6 AB6 AD12 AE23 R25 R6 AB7)
+1_5V_MAIN — V3P X 5 (AA24 AD8 AD14 AD18 AD23 AD27 AE30 AG6 AG9 AG12 AG15 AG18 AG21 AG24 AG27 AG30 AK2 AK7 AK12 AK16 AK20 AK25 AK30)
V3I X 3 (A2 A5 A10)
VDD_AGP X 11 (A15 D4 D7 D10 D13 D16 G11 G16 F17 F14 F10)
VDD_MAX X 23 (AE24 AD26)
V2I X 2
V3AGP X 4 (E8 A20 A25 A30)
VDD_MISC X 16 (AA27 AA30 D21 D26 F30 G23 H27 L24 L30 N27 T24 T30 V27)

CRITICAL
U14
UNI-N-1.5
(5 OF 5)
PBGA-UNIN-1.5.1

GB ETHERNET

CLK_ENET_LINK_TX (35 23)	V24	TX_CLK
ENET_TX_EN (36)	T28	TX_EN
ENET_TX_ER (36)	R30	TX_ER
ENET_TX_D<0> (36)	T27	TXD_0
ENET_TX_D<1> (36)	T29	TXD_1
ENET_TX_D<2> (36)	U29	TXD_2
ENET_TX_D<3> (36)	T26	TXD_3
ENET_TX_D<4> (36)	R26	TXD_4
ENET_TX_D<5> (36)	V29	TXD_5
ENET_TX_D<6> (36)	V30	TXD_6
ENET_TX_D<7> (36)	U27	TXD_7
CLK_ENET_LINK_RX (35 23)	V25	RX_CLK
ENET_RX_DV (23)	Y27	RX_DV
ENET_RX_ER (23)	W30	RX_ER
ENET_RXD<0> (36 23)	U26	RXD_0
ENET_RXD<1> (36 23)	V26	RXD_1
ENET_RXD<2> (36 23)	Y29	RXD_2
ENET_RXD<3> (36 23)	W26	RXD_3
ENET_RXD<4> (36 23)	Y30	RXD_4
ENET_RXD<5> (36 23)	W28	RXD_5
ENET_RXD<6> (36 23)	W24	RXD_6
ENET_RXD<7> (36 23)	W25	RXD_7
ENET_GBE_REFCLK (35 23)	U25	GBE_REFCLK
ENET_GTX_CLK (35)	T25	GTX_CLK
ENET_CRS (23)	Y28	CRS
ENET_COL (23)	W29	COL
ENET_MDIO (36 23)	V28	MDIO
ENET_MDC (36 23)	U28	MDC

MISC

	AA25	INTDATA
	AC30	INTSYNC
	AA28	INTCLK
	AA26	RESET
	Y25	PURESET

MPIC_DATA_L (14) — MPIC_SYNC_L (14) — MPIC_CLK (14) — UNIN_RESET_L (19 29) — UNIN_PU_RESET_L (29)

FIREWIRE

	P26	PHY_DATA_0
	N28	PHY_DATA_1
	P24	PHY_DATA_2
	N29	PHY_DATA_3
	N30	PHY_DATA_4
	P25	PHY_DATA_5
	P28	PHY_DATA_6
	P29	PHY_DATA_7
	R28	PHY_LPS
	P30	PHY_CTL_0
	R27	PHY_CTL_1
	R29	PHY_LREQ
	N25	PHY_SCLK
	M29	GPIO_0
	M28	GPIO_1
	E2	SPARE3

FW_LINK_DATA<0> (24 36) — FW_LINK_DATA<1> (24 36) — FW_LINK_DATA<2> (24 36) — FW_LINK_DATA<3> (24 36) — FW_LINK_DATA<4> (24 36) — FW_LINK_DATA<5> (24 36) — FW_LINK_DATA<6> (24 36) — FW_LINK_DATA<7> (24 36)
FW_PHY_LPS (24) — FW_LINK_CNTL<0> (24 36) — FW_LINK_CNTL<1> (24 36) — FW_LINK_LREQ (24 36) — CLK_UNIN_FW (24 35) — FW_C_LKON (14 24) — FW_TEST (9) — PMU_PME_L (14 29)

TEST

JTAG_ASIC_TDI (9)	AC26	TDI
JTAG_KL_TDI (14)	AD28	TDO
JTAG_ASIC_TCK (23 14 9)	AC28	TCK
JTAG_ASIC_TMS (23 14 9)	AD29	TMS
JTAG_ASIC_TRST_L (23 14 9)	AB26	TRSTN
UNIN_JTAG_TEI (9)	B20	TEI
UNIN_I2C_CLK0 (19 9 6)	AD30	ISCL0
UNIN_I2C_DATA0 (19 9 6)	AB27	ISDA0
UNIN_I2C_CLK1 (19 9 6)	AC29	ISCL1
UNIN_I2C_DATA1 (19 9 6)	AB28	ISDA1

U14 T18 T16 T14 T1 R18 R16 R14 R4 P27 P18 P16 P14 P7 N18 N16 N14 M30 M24 M4 M1 J27
Y24 Y1 W27 V18 V16 V14 V7 V4 U30 U24 U18 U16
VSS X 82
A1 A6 A11 A16 A21 A26 AA4 AA8 AA38 AC27 AD4 AD7 AD13 AD17 AD24 AE1 AF27 AF38 AG4 AG7 AG10 AG13 AG16 AG19 AG22 AG25 AK1 AK6 AK11 AK15 AK19 AK24 AK29 B38 D6 D9 D12 D15 D18 D22 D27 F4 G1 G7 G12 G17 G24 G30 J4

TEST PULL-UPS

+3V_MAIN

R250 10K 5% 1/16W MF 402 — JTAG_ASIC_TMS (9 14 23)
R273 10K 5% 1/16W MF 402 — JTAG_ASIC_TDI (9)
R236 10K 5% 1/16W MF 402 — JTAG_ASIC_TCK (9 14 23)
R237 1K 5% 1/16W MF 402 — JTAG_ASIC_TRST_L (9 14 23)
R356 10K 5% 1/16W MF 402 — UNIN_JTAG_TEI (9)
R289 1K 5% 1/16W MF 402 — FW_TEST (9)

UNI-N MISC I/O

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 9 OF 41	

NOTE: NUMBER AND VALUE OF CAPS BASED ON TANGENT DESIGN

UNI-N CORE DECOUPLING (18 0.1UF CAPS)

+1_8V_MAIN

C531 2.2uF N20P80% 16V CERM 805
C443 2.2uF N20P80% 16V CERM 805
C411 2.2uF N20P80% 16V CERM 805
C375 2.2uF N20P80% 16V CERM 805

C405 C406 C447 C448 C407 C449 C408 C409 C489 C490 C410 0.1uF 20% 10V CERM 402
C491 C444 C445 C493 C446 C494 C492 0.1uF 20% 10V CERM 402

MAXBUS INTERFACE DECOUPLING (70 0.1UF CAPS)

C373 C442 C232 C611 2.2uF N20P80% 16V CERM 805

C202 C486 C285 C525 C282 C264 C322 C573 C203 C177 C283
C287 C370 C585 C572 C204 C217 C335 C176 C284 C488 C304
C403 C372 C205 C336 C649 C438 C487 C288 C404 C509 C190
C337 C648 C437 C245 C402 C263 C439 C371 C383 C583 C234
C323 C440 C584 C384 C582 C369 C218 C324 C367 C441 C545
C385 C581 C524 C206 C191 C647 C436 C543 C544 C508 C526
C368 C233 C574 C286
0.1uF 20% 10V CERM 402

AGP I/O DECOUPLING (25 0.1UF CAPS)

+1_5V_MAIN

C450 C510 C618 C514 2.2uF N20P80% 16V CERM 805

C642 C606 C631 C630 C540 C451 C539 C590 C591 C643 C458
C554 C512 C605 C457 C553 C454 C456 C511 C452 C513 C453
C555 C455 C533
0.1uF 20% 10V CERM 402

+3V_MAIN

C374 C352 C530 C532 2.2uF N20P80% 16V CERM 805

SDRAM DECOUPLING (44 0.1UF CAPS)

C565 C637 C614 C627 C603 C636 C617 C616 C575 C638 C661
C623 C629 C628 C587 C653 C654 C656 C568 C652 C599 C660
C639 C663 C600 C641 C612 C624 C547 C576 C640 C613 C604
C577 C566 C655 C625 C615 C567 C662 C588 C602 C601 C659
0.1uF 20% 10V CERM 402

PCI DECOUPLING (11 0.1UF CAPS)

C650 C651 C589 C578 C321 C665 C528 C529 C527 C548 C626
0.1uF 20% 10V CERM 402

1394/ETHERNET DECOUPLING (61 0.1UF CAPS)

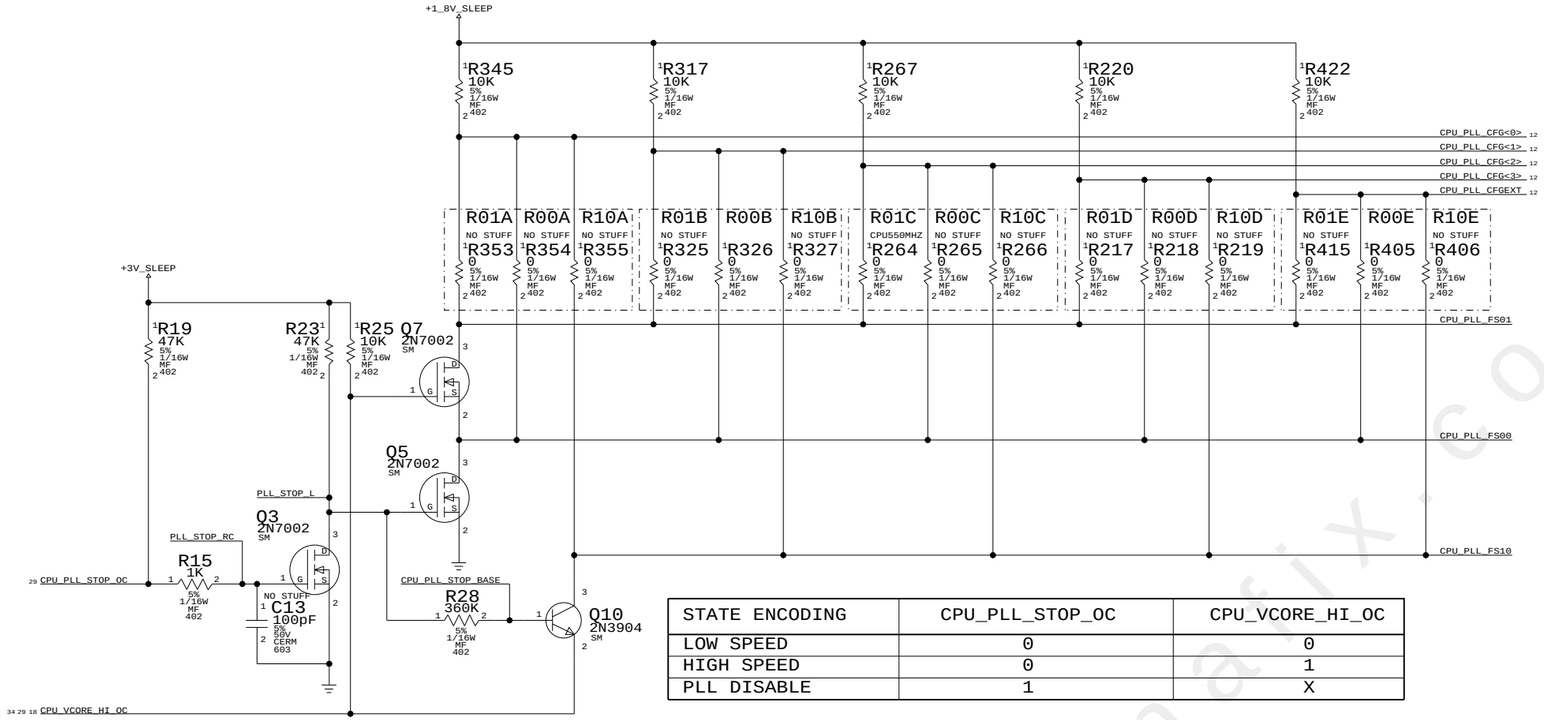
C265 C290 C236 C221 C238 C251 C355 C658 C247 C306 C305
C237 C249 C354 C664 C179 C309 C353 C495 C193 C289 C325
C310 C270 C496 C207 C171 C210 C248 C413 C250 C269 C414
C180 C178 C196 C412 C497 C268 C194 C192 C182 C266 C340
C246 C550 C308 C208 C220 C209 C291 C339 C235 C551 C267
C181 C307 C338 C219 C552 C195
0.1uF 20% 10V CERM 402

UNI-N BYPASSING

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 10 OF 41	

CPU PLL CONFIG CIRCUITRY



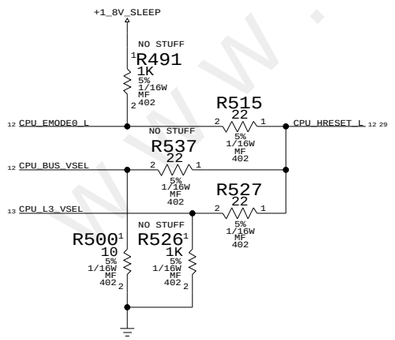
STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

CPU FREQUENCY CONFIGURATION

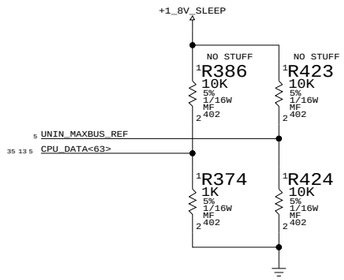
	MULTIPLIER	CORE FREQUENCY (AT BUS FREQUENCY) 100MHZ	133MHZ	CPU_PLL_CFG	
	(Bus-to-Core)	(MHZ)		E	ABCD HEX
	0.0X	PLL OFF		0	1111 0F
	0.5X	50	67	0	0000 00
	1.0X	PLL BYPASS		0	0011 03
	2.0X	200	267	0	0100 04
	2.5X	250	333	0	0110 06
	3.0X	300	400	0	1000 08
	3.5X	350	467	0	1110 0E
	4.0X	400	533	0	1010 0A
	4.5X	450	600	0	0111 07
BEST (667)	5.0X	500	667	0	1011 0B
BETTER (550)	5.5X	550	733	0	1001 09
	6.0X	600	800	0	1101 0D
	6.5X	650	867	0	0101 05
	7.0X	700	933	0	0010 02
	7.5X	750	1000	0	0001 01
	8.0X	800	1067	0	1100 0C
	9.0X	900	1200	1	0111 17
	10.0X	1000	1333	1	1010 1A
	11.0X	1100	1467	1	1001 19
	12.0X	1200	1600	1	1011 1B
	13.0X	1300	1733	1	0101 15
	14.0X	1400	1867	1	1100 1C
	15.0X	1500	2000	1	0001 11
	16.0X	1600	2133	1	1101 1D

CPU CONFIGURATION

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
CPU_L3_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE



UNIN CPU BUS CONFIGURATION



SIGNAL	TIED	APPLICATION
CPU_DATA<63> (UNIN)	HIGH	60X BUS MODE
	LOW	MAX BUS MODE
UNIN_MAXBUS_REF (UNIN)	HIGH	2.5V INTERFACE
	LOW	1.8V INTERFACE

APPLE COMPUTER INC.

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D	051-6223	A
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CPU_VCORE DECOUPLING NETWORK

37 34 12 CPU_VCORE_SLEEP

R557 470 5% 1/10W MF 402

C756 10uF 20% 6.3V CERM 805	C757 10uF 20% 6.3V CERM 805	C758 10uF 20% 6.3V CERM 805	C759 10uF 20% 6.3V CERM 805
C760 10uF 20% 6.3V CERM 805	C761 10uF 20% 6.3V CERM 805	C762 10uF 20% 6.3V CERM 805	C763 10uF 20% 6.3V CERM 805
C764 10uF 20% 6.3V CERM 805	C765 10uF 20% 6.3V CERM 805	C766 10uF 20% 6.3V CERM 805	C767 10uF 20% 6.3V CERM 805
C768 10uF 20% 6.3V CERM 805	C769 10uF 20% 6.3V CERM 805	C770 10uF 20% 6.3V CERM 805	C771 10uF 20% 6.3V CERM 805
C772 10uF 20% 6.3V CERM 805	C773 10uF 20% 6.3V CERM 805	C774 10uF 20% 6.3V CERM 805	C775 10uF 20% 6.3V CERM 805
C781 10uF 20% 6.3V CERM 805	C782 10uF 20% 6.3V CERM 805	C783 10uF 20% 6.3V CERM 805	C784 10uF 20% 6.3V CERM 805

C400 0.1uF 20% 10V CERM 402	C365 0.1uF 20% 10V CERM 402	C474 0.1uF 20% 10V CERM 402	C434 0.1uF 20% 10V CERM 402
C484 0.1uF 20% 10V CERM 402	C382 0.1uF 20% 10V CERM 402	C399 0.1uF 20% 10V CERM 402	C433 0.1uF 20% 10V CERM 402
C507 0.1uF 20% 10V CERM 402	C366 0.1uF 20% 10V CERM 402	C421 0.1uF 20% 10V CERM 402	C485 0.1uF 20% 10V CERM 402

CPU_OVDD DECOUPLING NETWORK

+1_8V_SLEEP

R328 470 5% 1/10W MF 402

C431 0.1uF 20% 10V CERM 402	C435 0.1uF 20% 10V CERM 402	C562 0.1uF 20% 10V CERM 402	C595 0.1uF 20% 10V CERM 402
C475 0.1uF 20% 10V CERM 402	C596 0.1uF 20% 10V CERM 402	C320 0.1uF 20% 10V CERM 402	C563 0.1uF 20% 10V CERM 402
C432 0.1uF 20% 10V CERM 402	C303 0.1uF 20% 10V CERM 402	C564 0.1uF 20% 10V CERM 402	C281 0.1uF 20% 10V CERM 402

CPU INTERNAL PLL FILTERING

CPU_VCORE_SLEEP 12 34 37

R543 10 5% 1/16W MF 603

37 CPU_AVDD

C597 0.1uF 20% 10V CERM 402

C580 2.2uF N20P80% 10V CERM 805

VDD

OVDD

5 CPU_BR_L	K1	BR
35 5 CPU_BG_L	R3	BG
NC	F2	HPR
35 5 CPU_TS_L	P5	TS
12 CPU_PULLDOWN	E10	A0
	N4	A1
	E8	A2
	N5	A3
35 5 CPU_ADDR<0>	C8	A4
35 5 CPU_ADDR<1>	R2	A5
35 5 CPU_ADDR<2>	A7	A6
35 5 CPU_ADDR<3>	M2	A7
35 5 CPU_ADDR<4>	A6	A8
35 5 CPU_ADDR<5>	M1	A9
35 5 CPU_ADDR<6>	A10	A10
35 5 CPU_ADDR<7>	U2	A11
35 5 CPU_ADDR<8>	N2	A12
35 5 CPU_ADDR<9>	P8	A13
35 5 CPU_ADDR<10>	M8	A14
35 5 CPU_ADDR<11>	W4	A15
35 5 CPU_ADDR<12>	N6	A16
35 5 CPU_ADDR<13>	U6	A17
35 5 CPU_ADDR<14>	R5	A18
35 5 CPU_ADDR<15>	Y4	A19
35 5 CPU_ADDR<16>	P1	A20
35 5 CPU_ADDR<17>	P4	A21
35 5 CPU_ADDR<18>	R6	A22
35 5 CPU_ADDR<19>	M7	A23
35 5 CPU_ADDR<20>	N7	A24
35 5 CPU_ADDR<21>	AA3	A25
35 5 CPU_ADDR<22>	U4	A26
35 5 CPU_ADDR<23>	W2	A27
35 5 CPU_ADDR<24>	W1	A28
35 5 CPU_ADDR<25>	W3	A29
35 5 CPU_ADDR<26>	V4	A30
35 5 CPU_ADDR<27>	AA1	A31
35 5 CPU_ADDR<28>	D10	A32
35 5 CPU_ADDR<29>	J4	A33
35 5 CPU_ADDR<30>	G10	A34
35 5 CPU_ADDR<31>	D9	A35
NC	L5	AP0
NC	L6	AP1
NC	J1	AP2
NC	H2	AP3
NC	G5	AP4
35 5 CPU_TT<0>	F1	TT0
35 5 CPU_TT<1>	F4	TT1
35 5 CPU_TT<2>	K8	TT2
35 5 CPU_TT<3>	A5	TT3
35 5 CPU_TT<4>	E1	TT4
35 5 CPU_TBST_L	B7	TBST
35 5 CPU_TSIZ<0>	L1	TSIZ0
35 5 CPU_TSIZ<1>	H3	TSIZ1
35 5 CPU_TSIZ<2>	D1	TSIZ2
35 5 CPU_GBL_L	M4	GBL
35 5 CPU_WT_L	L2	WT
35 5 CPU_CI_L	R1	CI
35 5 CPU_AACK_L	U1	AACK
35 5 CPU_ARTRY_L	T2	ARTRY
12 CPU_SHD0_L	L4	SHD0
12 CPU_SHD1_L	L8	SHD1
5 CPU_HIT_0_L	K2	HIT

OMIT

U15

SCVger

CBGA-483

(1 OF 3)

AVDD					
BVSEL	G6	CPU_BUS_VSEL	11		
SYSCLK	D6	SYSCLK_CPU	18 35		
CLK_OUT	N1	CPU_CLKOUT_SPN			
PLL_CFG0	A2	CPU_PLL_CFG<0>	11		
PLL_CFG1	F7	CPU_PLL_CFG<1>	11		
PLL_CFG2	C2	CPU_PLL_CFG<2>	11		
PLL_CFG3	D4	CPU_PLL_CFG<3>	11		
PLL_CFG4	H8	CPU_PLL_CFGEXT	11		
DBG	V1	CPU_DBG_L	5 35		
DRDY	T6	CPU_DRDY_0_L	5		
DTI0	P2	CPU_EDTI	12		
DTI1	T5	CPU_DTI<0>	5 35		
DTI2	U3	CPU_DTI<1>	5 35		
DTI3	P6	CPU_DTI<2>	5 35		
TDI	E4	JTAG_CPU_TDI	12		
TDO	H1	JTAG_CPU_TDO_TP			
TMS	K4	JTAG_CPU_TMS	12		
TCK	J7	JTAG_CPU_TCK	12		
TRST	C1	JTAG_CPU_RST_L	12		
LSSD_MODE	F6	CPU_LSSD_MODE	12		
L1_TSTCLK	H4	CPU_L1TSTCLK	12		
L2_TSTCLK	J2	CPU_L2TSTCLK	12		
TA	N8	CPU_TA_L	5 35		
TEA	T1	CPU_TEA_L	5 35		
TBEN	L3	CPU_TBEN	12		
QREQ	Y1	CPU_QREQ_L	5		
QACK	K7	CPU_QACK_L	5 35		
CKSTP_IN	F3				
CKSTP_OUT	K6	CHKSTP_OUT_L	12		
CHKS	B10	CPU_CHKS_L	12		
INT	J6	MPIC_CPU_INT_L	12 14		
SMI	G8	CPU_SMI_L	12 29		
MCP	B8	CPU_MCP_L	12		
SRESET	G1	CPU_SRESET_L	12 14		
HRESET	A3	CPU_HRESET_L	11 12 29		
PMON_IN	E6	CPU_PMONIN_L	12 14		
PMON_OUT	B4	NC			
BMODE0	C6	CPU_EMODE0_L	11		
BMODE1	C4	CPU_EMODE1_L	12		
DX	A9	CPU_PULLDOWN	12		
EXT_QUAL	B9				
IARTRY0	H6	CPU_PULLUP	12		
IARTRY1	H10				
OSHD	B6	NC			
SRW0	D8	CPU_SRWX_L	12		
SRW1	F9				
WAIT	F8				
SPARE0	A8	NC			
SPARE1	B1	NC			
SPARE2	H9	NC			
SPARE3	J8	NC			
NC1	A11	NC			
NC2	B11	NC			
NC3	C11	NC			
NC4	D5	NC			
NC5	D11	NC			
NC6	E7	NC			
NC7	E11	NC			
NC8	F11	NC			
NC9	G7	NC			
NC10	G11	NC			
NC11	H11	NC			

GND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2822	1	IC,VGER,2.1 NODE 3,550MHZ,1.4V,85C	U15	CRITICAL	CPU550MHZ
337S2823	1	IC,VGER,2.1 NODE 3,667MHZ,1.4V,85C	U15	CRITICAL	CPU667MHZ

MPC7450 PULL-UPS

+1_8V_SLEEP

12 CPU_TBEN	R499 1K	R451 10K	
12 CPU_CHKS_L	R481 10K	R416 10K	
12 CPU_SHD0_L	R474 10K	R490 10K	
12 CPU_SHD1_L	R514 10K	R464 1K	
12 CPU_MCP_L	R465 10K	R450 10K	
12 CPU_LSSD_MODE	R536 10K	R440 1K	
12 CPU_L2TSTCLK	R483 10K	R542 10K	
12 CPU_PMONIN_L	R439 10K	R449 10K	
12 CPU_EMODE1_L	R448 10K	R489 10K	
12 CPU_PULLUP	R482 10K	R558 200	
29 12 11 CPU_HRESET_L	R498 10K	R524 10K	
14 12 CPU_SRESET_L	R525 470		
14 12 MPIC_CPU_INT_L			
29 12 CPU_SMI_L			
12 JTAG_CPU_TDI			
12 JTAG_CPU_TMS			
12 JTAG_CPU_TCK			
12 JTAG_CPU_RST_L			
12 CPU_L1TSTCLK			
12 CPU_EDTI			
12 CPU_PULLDOWN			

All: 5% 1/16W MF 402

MPC7450 MAXBUS

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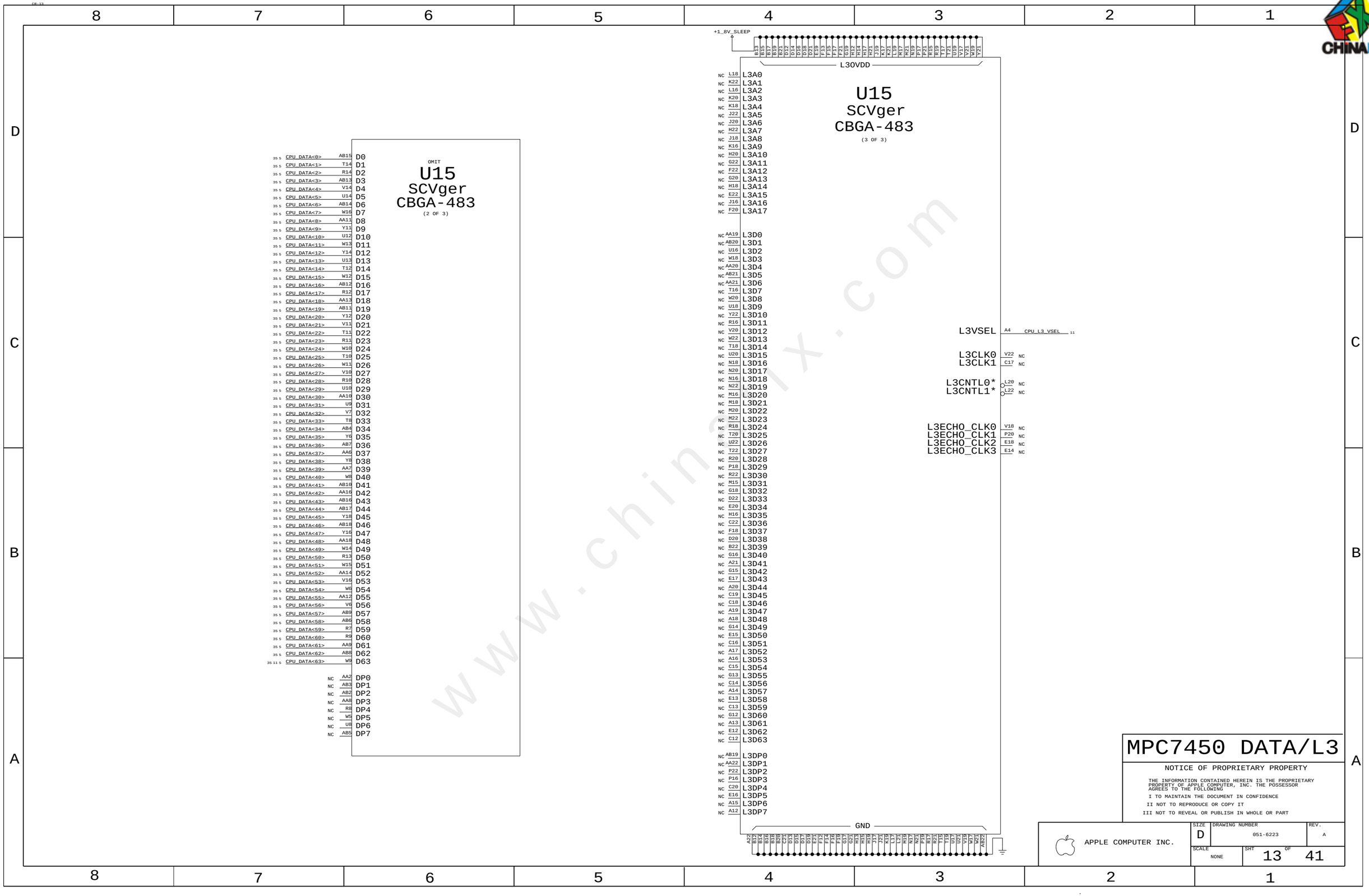
OMIT
U15
SCVger
CBGA-483
(2 OF 3)
CPU_DATA<0> AB15 D0
CPU_DATA<1> T14 D1
CPU_DATA<2> R14 D2
CPU_DATA<3> AB13 D3
CPU_DATA<4> V14 D4
CPU_DATA<5> U14 D5
CPU_DATA<6> AB14 D6
CPU_DATA<7> W16 D7
CPU_DATA<8> AA11 D8
CPU_DATA<9> Y11 D9
CPU_DATA<10> U12 D10
CPU_DATA<11> W13 D11
CPU_DATA<12> Y14 D12
CPU_DATA<13> U13 D13
CPU_DATA<14> T12 D14
CPU_DATA<15> W12 D15
CPU_DATA<16> AB12 D16
CPU_DATA<17> R12 D17
CPU_DATA<18> AA13 D18
CPU_DATA<19> AB11 D19
CPU_DATA<20> Y12 D20
CPU_DATA<21> V11 D21
CPU_DATA<22> T11 D22
CPU_DATA<23> R11 D23
CPU_DATA<24> W10 D24
CPU_DATA<25> T10 D25
CPU_DATA<26> W11 D26
CPU_DATA<27> V10 D27
CPU_DATA<28> R10 D28
CPU_DATA<29> U10 D29
CPU_DATA<30> AA10 D30
CPU_DATA<31> U9 D31
CPU_DATA<32> V7 D32
CPU_DATA<33> T8 D33
CPU_DATA<34> AB4 D34
CPU_DATA<35> Y6 D35
CPU_DATA<36> AB7 D36
CPU_DATA<37> AA6 D37
CPU_DATA<38> Y8 D38
CPU_DATA<39> AA7 D39
CPU_DATA<40> W8 D40
CPU_DATA<41> AB10 D41
CPU_DATA<42> AA16 D42
CPU_DATA<43> AB16 D43
CPU_DATA<44> AB17 D44
CPU_DATA<45> Y18 D45
CPU_DATA<46> AB18 D46
CPU_DATA<47> Y16 D47
CPU_DATA<48> AA18 D48
CPU_DATA<49> W14 D49
CPU_DATA<50> R13 D50
CPU_DATA<51> W15 D51
CPU_DATA<52> AA14 D52
CPU_DATA<53> V16 D53
CPU_DATA<54> W6 D54
CPU_DATA<55> AA12 D55
CPU_DATA<56> V6 D56
CPU_DATA<57> AB9 D57
CPU_DATA<58> AB6 D58
CPU_DATA<59> R7 D59
CPU_DATA<60> R9 D60
CPU_DATA<61> AA9 D61
CPU_DATA<62> AB8 D62
CPU_DATA<63> W9 D63
NC AA2 DP0
NC AB3 DP1
NC AB2 DP2
NC AA8 DP3
NC R8 DP4
NC W5 DP5
NC U8 DP6
NC AB5 DP7
+1_8V_SLEEP
L30VDD
U15
SCVger
CBGA-483
(3 OF 3)
NC L18 L3A0
NC K22 L3A1
NC L16 L3A2
NC K20 L3A3
NC K18 L3A4
NC J22 L3A5
NC J20 L3A6
NC H22 L3A7
NC J18 L3A8
NC K16 L3A9
NC H20 L3A10
NC G22 L3A11
NC F22 L3A12
NC G20 L3A13
NC H18 L3A14
NC E22 L3A15
NC J16 L3A16
NC F20 L3A17
NC AA19 L3D0
NC AB20 L3D1
NC U16 L3D2
NC W18 L3D3
NC AA20 L3D4
NC AB21 L3D5
NC AA21 L3D6
NC T16 L3D7
NC W20 L3D8
NC U18 L3D9
NC Y22 L3D10
NC R16 L3D11
NC V20 L3D12
NC W22 L3D13
NC T18 L3D14
NC U20 L3D15
NC N18 L3D16
NC N20 L3D17
NC N16 L3D18
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NC M16 L3D20
NC M18 L3D21
NC M20 L3D22
NC M22 L3D23
NC R18 L3D24
NC T20 L3D25
NC U22 L3D26
NC T22 L3D27
NC R20 L3D28
NC P18 L3D29
NC R22 L3D30
NC M15 L3D31
NC G18 L3D32
NC D22 L3D33
NC E20 L3D34
NC H16 L3D35
NC C22 L3D36
NC F18 L3D37
NC D20 L3D38
NC B22 L3D39
NC G16 L3D40
NC A21 L3D41
NC G15 L3D42
NC E17 L3D43
NC A20 L3D44
NC C19 L3D45
NC C18 L3D46
NC A19 L3D47
NC A18 L3D48
NC G14 L3D49
NC E15 L3D50
NC C16 L3D51
NC A17 L3D52
NC A16 L3D53
NC C15 L3D54
NC G13 L3D55
NC C14 L3D56
NC A14 L3D57
NC E13 L3D58
NC C13 L3D59
NC G12 L3D60
NC A13 L3D61
NC E12 L3D62
NC C12 L3D63
NC AB19 L3DP0
NC AA22 L3DP1
NC P22 L3DP2
NC P16 L3DP3
NC C20 L3DP4
NC E16 L3DP5
NC A15 L3DP6
NC A12 L3DP7
L3VSEL A4 CPU_L3_VSEL 11
L3CLK0 V22 NC
L3CLK1 C17 NC
L3CNTL0* L20 NC
L3CNTL1* L22 NC
L3ECHO_CLK0 V18 NC
L3ECHO_CLK1 P20 NC
L3ECHO_CLK2 E18 NC
L3ECHO_CLK3 E14 NC
GND
MPC7450 DATA/L3
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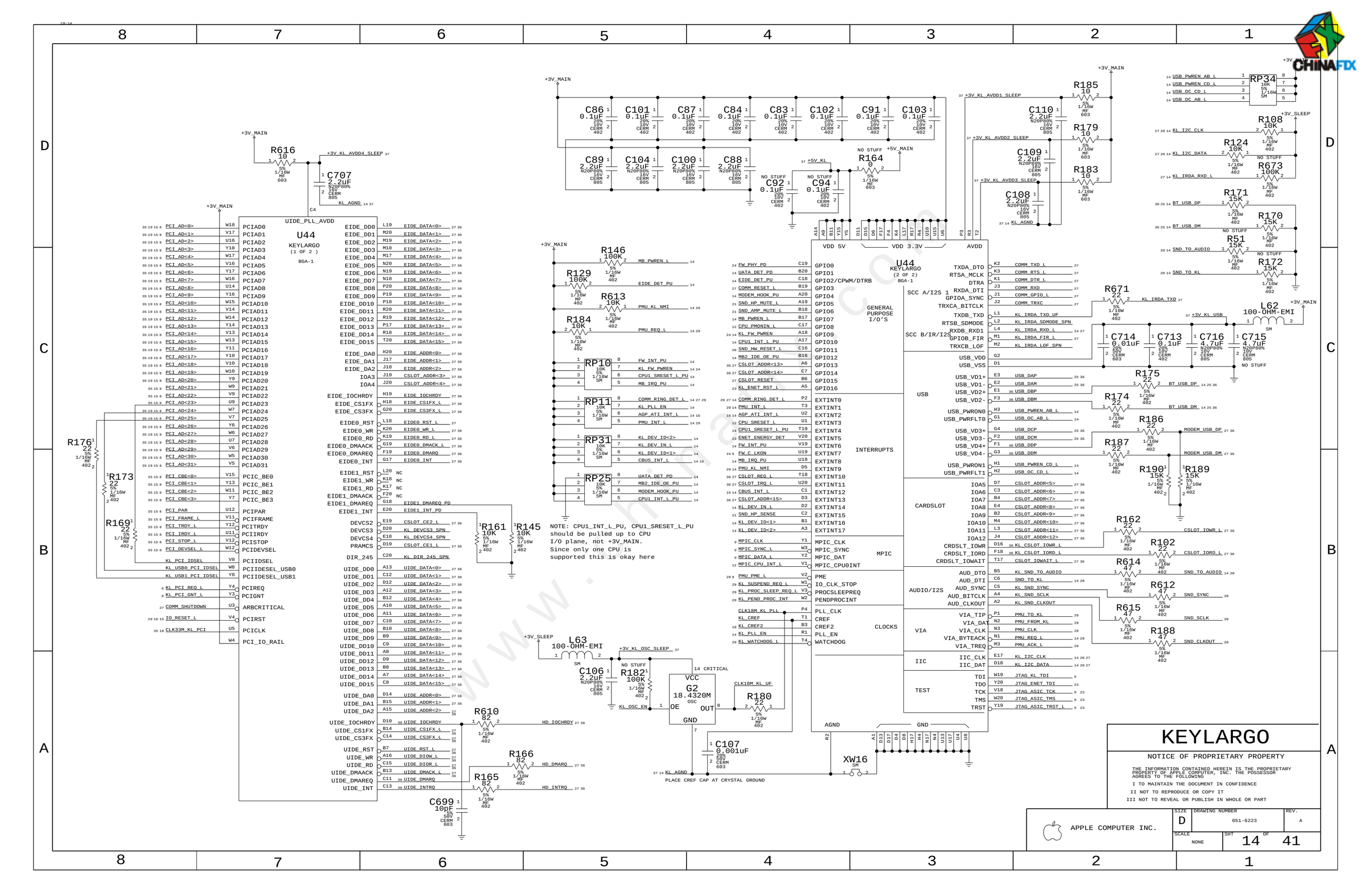
U44
KEYLARGO
(1 OF 2)
BGA-1
UIDE_PLL_AVDD
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PCIAD1
PCIAD2
PCIAD3
PCIAD4
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PCIAD29
PCIAD30
PCIAD31
PCIC_BE0
PCIC_BE1
PCIC_BE2
PCIC_BE3
PCIPAR
PCIFRAME
PCITRDY
PCIIRDY
PCISTOP
PCIDEVSEL
PCIIDSEL
PCIIDESEL_USB0
PCIIDESEL_USB1
PCIREQ
PCIGNT
ARBCRITICAL
PCIRST
PCICLK
PCI_IO_RAIL
EIDE_DD0
EIDE_DD1
EIDE_DD2
EIDE_DD3
EIDE_DD4
EIDE_DD5
EIDE_DD6
EIDE_DD7
EIDE_DD8
EIDE_DD9
EIDE_DD10
EIDE_DD11
EIDE_DD12
EIDE_DD13
EIDE_DD14
EIDE_DD15
EIDE_DA0
EIDE_DA1
EIDE_DA2
IOA3
IOA4
EIDE_IOCHRDY
EIDE_CS1FX
EIDE_CS3FX
EIDE0_RST
EIDE0_WR
EIDE0_RD
EIDE0_DMAACK
EIDE0_DMAREQ
EIDE0_INT
EIDE1_RST
EIDE1_WR
EIDE1_RD
EIDE1_DMAACK
EIDE1_DMAREQ
EIDE1_INT
DEVCS2
DEVCS3
DEVCS4
PRAMCS
DIR_245
UIDE_DD0
UIDE_DD1
UIDE_DD2
UIDE_DD3
UIDE_DD4
UIDE_DD5
UIDE_DD6
UIDE_DD7
UIDE_DD8
UIDE_DD9
UIDE_DD10
UIDE_DD11
UIDE_DD12
UIDE_DD13
UIDE_DD14
UIDE_DD15
UIDE_DA0
UIDE_DA1
UIDE_DA2
UIDE_IOCHRDY
UIDE_CS1FX
UIDE_CS3FX
UIDE_RST
UIDE_WR
UIDE_RD
UIDE_DMAACK
UIDE_DMAREQ
UIDE_INT
R616 10
C707 2.2uF
KL_AGND
C4
R176 22
R173 22
R169 22
R610 82
R166 82
R165 82
C699 10pF
R161 10K
R145 10K
NOTE: CPU1_INT_L_PU, CPU1_SRESET_L_PU should be pulled up to CPU I/O plane, not +3V_MAIN. Since only one CPU is supported this is okay here
C86 C101 C87 C84 C83 C102 C91 C103 0.1uF
C89 C104 C100 C88 2.2uF
C92 C94 0.1uF NO STUFF
R164 0
R146 100K
R129 100K
R613 10K
R184 10K
RP10 10K
RP11 10K
RP31 10K
RP25 10K
L63 100-OHM-EMI
C106 2.2uF NO STUFF
R182 100K NO STUFF
18.4320M OSC
R180 22
C107 0.001uF
XW16
FW_PHY_PD
UATA_DET_PD
EIDE_DET_PU
COMM_RESET_L
MODEM_HOOK_PU
SND_HP_MUTE_L
SND_AMP_MUTE_L
MB_PWREN_L
CPU_PMONIN_L
KL_FW_PWREN
CPU1_INT_L_PU
SND_HW_RESET_L
MB2_IDE_OE_PU
CSLOT_ADDR<13>
CSLOT_ADDR<14>
CSLOT_RESET_L
KL_ENET_RST_L
COMM_RING_DET_L
KL_PLL_EN
AGP_ATI_INT_L
PMU_INT_L
KL_DEV_ID<2>
KL_DEV_IN_L
KL_DEV_ID<1>
CBUS_INT_L
UATA_DET_PD
MB2_IDE_OE_PU
MODEM_HOOK_PU
CPU1_INT_L_PU
CPU_SRESET_L
CPU1_SRESET_L_PU
ENET_ENERGY_DET
FW_INT_PU
FW_C_LKON
MB_IRQ_PU
PMU_KL_NMI
CSLOT_REG_L
CSLOT_IRQ_L
CBUS_INT_L
CSLOT_ADDR<15>
KL_DEV_IN_L
SND_HP_SENSE
KL_DEV_ID<1>
KL_DEV_ID<2>
MPIC_CLK
MPIC_SYNC_L
MPIC_DAT
MPIC_CPU_INT_L
PMU_PME_L
KL_SUSPEND_REQ_L
KL_PROC_SLEEP_REQ_L
KL_PEND_PROC_INT
CLK18M_KL_PLL
KL_CREF
KL_CREF2
KL_PLL_EN
KL_WATCHDOG_L
GPIO0
GPIO1
GPIO2/CPWM/DTRB
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
EXTINT0
EXTINT1
EXTINT2
EXTINT3
EXTINT4
EXTINT5
EXTINT6
EXTINT7
EXTINT8
EXTINT9
EXTINT10
EXTINT11
EXTINT12
EXTINT13
EXTINT14
EXTINT15
EXTINT16
EXTINT17
PME
IO_CLK_STOP
PROCSLEEPREQ
PENDPROCINT
PLL_CLK
CREF
CREF2
PLL_EN
WATCHDOG
GENERAL PURPOSE I/O'S
INTERRUPTS
MPIC
CLOCKS
VDD 5V
VDD 3.3V
AVDD
SCC A/I2S 1
SCC B/IR/I2S
USB
CARDSLOT
AUDIO/I2S
VIA
IIC
TEST
TXDA_DTO
RTSA_MCLK
DTRA
GPIOA_SYNC
TRXCA_BITCLK
TXDB_TXD
RTSB_SDMODE
RXDB_RXD1
GPIOB_FIR
TRXCB_LOF
USB_VDD
USB_VSS
USB_VD1+
USB_VD1-
USB_VD2+
USB_VD2-
USB_PWRON0
USB_PWRFLT0
USB_VD3+
USB_VD3-
USB_VD4+
USB_VD4-
USB_PWRON1
USB_PWRFLT1
IOA5
IOA6
IOA7
IOA8
IOA9
IOA10
IOA11
IOA12
CRDSLT_IOWR
CRDSLT_IORD
CRDSLT_IOWAIT
AUD_DTO
AUD_DTI
AUD_SYNC
AUD_BITCLK
AUD_CLKOUT
VIA_TIP
VIA_DAT
VIA_CLK
VIA_BYTEACK
VIA_TREQ
IIC_CLK
IIC_DAT
TDI
TDO
TCK
TMS
TRST
COMM_TXD_L
COMM_RTS_L
COMM_DTR_L
COMM_RXD
COMM_GPIO_L
COMM_TRXC
KL_IRDA_TXD_UF
KL_IRDA_SDMODE_SPN
KL_IRDA_RXD_L
KL_IRDA_FIR_L
KL_IRDA_LOF_SPN
USB_DAP
USB_DAM
USB_DBP
USB_DBM
USB_PWREN_AB_L
USB_OC_AB_L
USB_DCP
USB_DCM
USB_DDP
USB_DDM
USB_PWREN_CD_L
USB_OC_CD_L
CSLOT_ADDR<5>
CSLOT_ADDR<6>
CSLOT_ADDR<7>
CSLOT_ADDR<8>
CSLOT_ADDR<9>
CSLOT_ADDR<10>
CSLOT_ADDR<11>
CSLOT_ADDR<12>
KL_CSLOT_IOWR_L
KL_CSLOT_IORD_L
CSLOT_IOWAIT_L
SND_TO_AUDIO
SND_TO_KL
KL_SND_SYNC
KL_SND_SCLK
KL_SND_CLKOUT
PMU_TO_KL
PMU_FROM_KL
PMU_CLK
PMU_REQ_L
PMU_ACK_L
KL_I2C_CLK
KL_I2C_DATA
JTAG_KL_TDI
JTAG_ENET_TDI
JTAG_ASIC_TCK
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L
KL_IRDA_TXD
BT_USB_DP
BT_USB_DM
MODEM_USB_DP
MODEM_USB_DM
KL_IRDA_RXD_L
BT_USB_DP
BT_USB_DM
SND_TO_AUDIO
SND_TO_KL
KL_I2C_CLK
KL_I2C_DATA
R185 10
R110 2.2uF
R179 10
R109 2.2uF
R183 10
R108 10K
R124 10K
R673 100K NO STUFF
R171 15K
R170 15K
R51 15K NO STUFF
R172 15K
RP34 10K
R671 22
L62 100-OHM-EMI
C714 0.01uF
C713 0.1uF
C716 4.7uF
C715 4.7uF NO STUFF
R175 22
R174 22
R186 22
R187 22
R190 15K
R189 15K
R162 22
R102 22
R614 47
R612 47
R615 47
R188 47
+3V_MAIN
+3V_SLEEP
+3V_KL_AVDD4_SLEEP
+3V_KL_AVDD1_SLEEP
+3V_KL_AVDD2_SLEEP
+3V_KL_AVDD3_SLEEP
+5V_KL
+3V_KL_OSC_SLEEP
+3V_KL_USB
KL_AGND
AGND
GND
PLACE CREF CAP AT CRYSTAL GROUND
KEYLARGO
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REV. A
SCALE NONE
SHT 14 OF 41

PCI1410A PULL-UPS

+3V_MAIN

R177 10K 5% 1/16W MF 402 — PCI_PERR_L
R178 10K 5% 1/16W MF 402 — PCI_SERR_L
R618 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU

R181 10K 5% 1/16W MF 402 — CBUS_MFUNC1_PD
R191 10K 5% 1/16W MF 402 — CBUS_MFUNC2_PD
RP35 10K 5% 1/16W SM — CBUS_MFUNC3_PD, CBUS_MFUNC4_PD, CBUS_MFUNC5_PD, CBUS_MFUNC6_PD

+3V_MAIN

C112 0.1uF 20% 10V CERM 402
C111 0.1uF 20% 10V CERM 402
C711 0.1uF 20% 10V CERM 402
C704 0.1uF 20% 10V CERM 402
C98 0.1uF 20% 10V CERM 402
C95 0.1uF 20% 10V CERM 402
C706 0.1uF 20% 10V CERM 402
C709 0.1uF 20% 10V CERM 402

C113 0.001uF 20% 50V CERM 603
C114 0.001uF 20% 50V CERM 603
C712 0.001uF 20% 50V CERM 603
C705 0.001uF 20% 50V CERM 603
C97 0.001uF 20% 50V CERM 603
C96 0.001uF 20% 50V CERM 603
C708 0.001uF 20% 50V CERM 603
C710 0.001uF 20% 50V CERM 603

14 30 50 86 102 122 138 — VCC

+3V_MAIN +5V_MAIN

R634 10K 5% 1/16W MF 402

U46 TPS2211 SSOI

V_12	9	AVPP	10 — +VPP_CBUS_SW
V_5_1	5		
V_5_2	6	AVCC0	11 — +VCC_CBUS_SW
V_3_1	3	AVCC1	12 — +VCC_CBUS_SW
V_3_2	4	AVCC2	13 — +VCC_CBUS_SW
VCCD0	1		
VCCD1	2		
VPPD0	15		
VPPD1	14		
SHTDWN	16		
GND	7	OC	8

TPS2211_SHDN_L_PU

C717 4.7uF N20P80% 16V CERM 1206

U45
PCI1410APGE
PQFP

VCCP1	18		
VCCP2	44		
VCCI	63		
AD0	57	PCI_AD<0>	35 19 14 8
AD1	56	PCI_AD<1>	35 19 14 8
AD2	55	PCI_AD<2>	35 19 14 8
AD3	54	PCI_AD<3>	35 19 14 8
AD4	53	PCI_AD<4>	35 19 14 8
AD5	52	PCI_AD<5>	35 19 14 8
AD6	51	PCI_AD<6>	35 19 14 8
AD7	49	PCI_AD<7>	35 19 14 8
AD8	47	PCI_AD<8>	35 19 14 8
AD9	46	PCI_AD<9>	35 19 14 8
AD10	45	PCI_AD<10>	35 19 14 8
AD11	43	PCI_AD<11>	35 19 14 8
AD12	41	PCI_AD<12>	35 19 14 8
AD13	40	PCI_AD<13>	35 19 14 8
AD14	39	PCI_AD<14>	35 19 14 8
AD15	38	PCI_AD<15>	35 19 14 8
AD16	26	PCI_AD<16>	35 19 14 8
AD17	25	PCI_AD<17>	35 19 14 8
AD18	24	PCI_AD<18>	35 19 14 8
AD19	23	PCI_AD<19>	35 19 14 8
AD20	19	PCI_AD<20>	35 19 14 8
AD21	17	PCI_AD<21>	35 14 8
AD22	16	PCI_AD<22>	35 14 8
AD23	15	PCI_AD<23>	35 14 8
AD24	11	PCI_AD<24>	35 19 14 8
AD25	10	PCI_AD<25>	35 19 14 8
AD26	9	PCI_AD<26>	35 19 14 8
AD27	8	PCI_AD<27>	35 19 14 8
AD28	7	PCI_AD<28>	35 19 14 8
AD29	5	PCI_AD<29>	35 19 14 8
AD30	4	PCI_AD<30>	35 19 14 8
AD31	3	PCI_AD<31>	35 19 14 8
C_BE0	48	PCI_CBE<0>	35 14 8
C_BE1	37	PCI_CBE<1>	35 14 8
C_BE2	27	PCI_CBE<2>	35 14 8
C_BE3	12	PCI_CBE<3>	35 14 8
PAR	36	PCI_PAR	35 14 8
IRDY	29	PCI_IRDY_L	35 14 8
SERR	35	PCI_SERR_L	15
IDSEL	13	CBUS_PCI_IDSEL	
PERR	34	PCI_PERR_L	15
FRAME	28	PCI_FRAME_L	35 14 8
STOP	33	PCI_STOP_L	35 14 8
TRDY	31	PCI_TRDY_L	35 14 8
DEVSEL	32	PCI_DEVSEL_L	35 14 8
RST	20	CBUS_PCI_RESET_L	
REQ	1	CBUS_PCI_REQ_L	8
GNT	2	CBUS_PCI_GNT_L	8
PCLK	21	CLK33M_CBUS	35 18
GRST	66		
SPKROUT	62		
RI_OUT_PME	59		
SUSPEND	70	CBUS_SUSPEND_PU	15
MFUNC0	60	CBUS_INT_L	14
MFUNC1	61	CBUS_MFUNC1_PD	15
MFUNC2	64	CBUS_MFUNC2_PD	15
MFUNC3	65	CBUS_MFUNC3_PD	15
MFUNC4	67	CBUS_MFUNC4_PD	15
MFUNC5	68	CBUS_MFUNC5_PD	15
MFUNC6	69	CBUS_MFUNC6_PD	15
VCCCB1	90		
VCCCB2	126		
VCCD0	73	CBUS_VCCD0_L	
VCCD1	74	CBUS_VCCD1_L	
VPPD0	71	CBUS_VPPD0	
VPPD1	72	CBUS_VPPD1	
CD1_CCD1	75	CBUS_DET_1_L	15
CD2_CCD2	137	CBUS_DET_2_L	15
IORD_CAD13	93	CBUS_IORD_L	15
IOWR_CAD15	96	CBUS_IOWR_L	15
OE_CAD11	92	CBUS_OE_L	15
CE1_CC_BE0	88	CBUS_CE1_L	15
VS1_CVS1	131	CBUS_VS1	15
VS2_CVS2	117	CBUS_VS2	15
WE_CGNT	106	CBUS_WE_L	15
RDY_IREQ_CINT	132	CBUS_READY	15
RESET_CRST	119	CBUS_RESET_L	15
REG_CC_BE3	125	CBUS_REG_L	15
BVD1_STSCHG_RI_CS	135	CBUS_BVD1_L	15
BVD2_SPKR_CAUDIO	134	CBUS_BVD2_L	15
WP_IOIS16_CCLKRU	136	CBUS_WP_L	15 16
CE2_CAD10	91	CBUS_CE2_L	15
INPACK_CREQ	123	CBUS_INPACK_L	15
WAIT_CSERR	133	CBUS_WAIT_L	15
A0_CAD26	129	CBUS_ADDR<0>	15
A1_CAD25	128	CBUS_ADDR<1>	15
A2_CAD24	127	CBUS_ADDR<2>	15
A3_CAD23	124	CBUS_ADDR<3>	15
A4_CAD22	121	CBUS_ADDR<4>	15
A5_CAD21	120	CBUS_ADDR<5>	15
A6_CAD20	118	CBUS_ADDR<6>	15
A7_CAD18	115	CBUS_ADDR<7>	15
A8_CC_BE1	99	CBUS_ADDR<8>	15 16
A9_CAD14	97	CBUS_ADDR<9>	15 16
A10_CAD9	89	CBUS_ADDR<10>	15 16
A11_CAD12	95	CBUS_ADDR<11>	15 16
A12_CC_BE2	112	CBUS_ADDR<12>	15 16
A13_CPAR	101	CBUS_ADDR<13>	15 16
A14_CPERR	104	CBUS_ADDR<14>	15 16
A15_CIRDY	110	CBUS_ADDR<15>	15 16
A16_CCLK	108	CBUS_ADDR_16_UF	
A17_CAD16	98	CBUS_ADDR<17>	15 16
A18_RSVD	100	CBUS_ADDR<18>	15 16
A19_CBLOCK	103	CBUS_ADDR<19>	15 16
A20_CSTOP	105	CBUS_ADDR<20>	15 16
A21_CDEVSEL	107	CBUS_ADDR<21>	15 16
A22_CTRDY	109	CBUS_ADDR<22>	15 16
A23_CFRAME	111	CBUS_ADDR<23>	15 16
A24_CAD17	113	CBUS_ADDR<24>	15 16
A25_CAD19	116	CBUS_ADDR<25>	15 16
D0_CAD27	139	CBUS_DATA<0>	15
D1_CAD29	141	CBUS_DATA<1>	15
D2_RSVD	143	CBUS_DATA<2>	15
D3_CAD0	76	CBUS_DATA<3>	15
D4_CAD1	79	CBUS_DATA<4>	15
D5_CAD3	81	CBUS_DATA<5>	15
D6_CAD5	83	CBUS_DATA<6>	15
D7_CAD7	85	CBUS_DATA<7>	15
D8_CAD28	140	CBUS_DATA<8>	15
D9_CAD30	142	CBUS_DATA<9>	15
D10_CAD31	144	CBUS_DATA<10>	15
D11_CAD2	77	CBUS_DATA<11>	15
D12_CAD4	80	CBUS_DATA<12>	15
D13_CAD6	82	CBUS_DATA<13>	15
D14_RSVD	84	CBUS_DATA<14>	15
D15_CAD8	87	CBUS_DATA<15>	15

R167 22 5% 1/16W MF 402 — PCI_AD<26>

R168 47 5% 1/16W MF 402 — IO_RESET_L

R627 47 5% 1/16W MF 402 — CBUS_ADDR<16>

6 22 42 58 78 94 114 130 — GND

PC CARD/CARDBUS PULL-UPS

+3V_SLEEP

RP33 39K 5% 1/16W SM NO STUFF — CBUS_DET_1_L, CBUS_DET_2_L, CBUS_VS2, CBUS_VS1
RP12 39K 5% 1/16W SM NO STUFF — CBUS_READY, CBUS_ADDR<14>, CBUS_ADDR<20>, CBUS_ADDR<19> — +VCC_CBUS_SW
RP30 39K 5% 1/16W SM NO STUFF — CBUS_INPACK_L, CBUS_BVD2_L, CBUS_BVD1_L, CBUS_WP_L
RP32 39K 5% 1/16W SM NO STUFF — CBUS_WAIT_L, CBUS_ADDR<15>, CBUS_ADDR<22>, CBUS_ADDR<21>
R665 39K 5% 1/16W MF 402 — CBUS_WP_L

PC CARD/CARDBUS CONNECTOR

C105 AND C683 USED AS GLITCH FILTERS

NO STUFF C683 1.0uF N20P80% 16V CERM 805

CRITICAL
J16
M-ST-55055
SM

80	1	CBUS_DATA<3>	15
79	2	CBUS_DATA<4>	15
78	3	CBUS_DATA<5>	15
77	4	CBUS_DATA<6>	15
76	5		
75	6	CBUS_DATA<7>	15
74	7	CBUS_CE1_L	15
73	8	CBUS_ADDR<10>	15 16
72	9	CBUS_OE_L	15
71	10		
70	11	CBUS_ADDR<11>	15 16
69	12	CBUS_ADDR<9>	15 16
68	13	CBUS_ADDR<8>	15 16
67	14	CBUS_ADDR<13>	15 16
66	15		
65	16	CBUS_ADDR<14>	15 16
64	17	CBUS_WE_L	15
63	18	CBUS_READY	15
62	19	+VCC_CBUS_SW	15 37
61	20		
60	21	+VPP_CBUS_SW	15 37
59	22	CBUS_ADDR<16>	15 16
58	23	CBUS_ADDR<15>	15 16
57	24	CBUS_ADDR<12>	15 16
56	25		
55	26	CBUS_ADDR<7>	15
54	27	CBUS_ADDR<6>	15
53	28	CBUS_ADDR<5>	15
52	29	CBUS_ADDR<4>	15
51	30		
50	31	CBUS_ADDR<3>	15
49	32	CBUS_ADDR<2>	15
48	33	CBUS_ADDR<1>	15
47	34	CBUS_ADDR<0>	15
46	35		
45	36	CBUS_DATA<0>	15
44	37	CBUS_DATA<1>	15
43	38	CBUS_DATA<2>	15
42	39	CBUS_WP_L	15 16
41	40		

37 15 +VCC_CBUS_SW

C93 0.1uF 20% 10V CERM 402
C90 3.3uF N20P80% 16V CERM 1206
C99 4.7uF N20P80% 16V CERM 1206

37 15 +VPP_CBUS_SW

C700 0.1uF 20% 10V CERM 402

NO STUFF C105 1uF 20% 10V CERM 805

CARDBUS

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D	051-6223	A
SCALE: NONE	SHT 15 OF 41	

ATI PULL-UPS

+3V_MAIN
R468 10K 5% 1/16W MF 402 — AGP_SUS_STAT_L_PU 16
R457 10K 5% 1/16W MF 402 — AGP_BUSY_L_PU 16
R443 10K 5% 1/16W MF 402 — ATI_AUXWIN_PU 16

+1_8V_MAIN
R346 10K 5% 1/16W MF 402 — ATI_MEMVMODE 16
SETUP FOR 2.5V MEMORY

R242 45.3 1% 1/16W MF 402 — ATI_AGP_TEST 16
R470 1K 5% 1/16W MF 402 — ATI_TESTEN 16

UNI-N AGP I/O REFERENCE

(PLACE CLOSE TO ATI AGP BALLS)

+1_5V_MAIN
C212 470pF 10% 50V CERM 402
R309[1] 4.99K 1% 1/16W MF 402
[1]R310 82.5 1% 1/16W MF 402
UNIN_AGP_VREF_H
UNIN_AGP_VREF 7
R320[1] 4.99K 1% 1/16W MF 402
[1]R311 82.5 1% 1/16W MF 402
C222 470pF 10% 50V CERM 402
UNIN_AGP_VREF_L

R442 47 5% 1/16W MF 402 — IO_RESET_L 29 15 14

+2_5V_ATI_VDDR 37 17
R358[1] 10K 1% 1/16W MF 402
ATI DDR I/O REFERENCE
R377[1] 10K 1% 1/16W MF 402
C312 0.1uF 20% 10V CERM 402

R458 47 5% 1/16W MF 402 — SYSTEM_CLK_EN 29 18

OMIT
U4
RAGE_MOBILITY_M6_35X35
PBGA
(1 OF 3)

AGP_AD<31> 35 7	T25	AD31	D63	R3	NC
AGP_AD<30> 35 7	T23	AD30	D62	R2	NC
AGP_AD<29> 35 7	R26	AD29	D61	R1	NC
AGP_AD<28> 35 7	R24	AD28	D60	P4	NC
AGP_AD<27> 35 7	R25	AD27	D59	P3	NC
AGP_AD<26> 35 7	P24	AD26	D58	P2	NC
AGP_AD<25> 35 7	P26	AD25	D57	P1	NC
AGP_AD<24> 35 7	P23	AD24	D56	N4	NC
AGP_AD<23> 35 7	N26	AD23	D55	N1	NC
AGP_AD<22> 35 7	M25	AD22	D54	M3	NC
AGP_AD<21> 35 7	N25	AD21	D53	M2	NC
AGP_AD<20> 35 7	M24	AD20	D52	M1	NC
AGP_AD<19> 35 7	M26	AD19	D51	L4	NC
AGP_AD<18> 35 7	L24	AD18	D50	L3	NC
AGP_AD<17> 35 7	L26	AD17	D49	L2	NC
AGP_AD<16> 35 7	L23	AD16	D48	L1	NC
AGP_AD<15> 35 7	H25	AD15	D47	J3	NC
AGP_AD<14> 35 7	H26	AD14	D46	J2	NC
AGP_AD<13> 35 7	H24	AD13	D45	J1	NC
AGP_AD<12> 35 7	G26	AD12	D44	H3	NC
AGP_AD<11> 35 7	G24	AD11	D43	H2	NC
AGP_AD<10> 35 7	G25	AD10	D42	H1	NC
AGP_AD<9> 35 7	G23	AD9	D41	G3	NC
AGP_AD<8> 35 7	F26	AD8	D40	G2	NC
AGP_AD<7> 35 7	E26	AD7	D39	F1	NC
AGP_AD<6> 35 7	E24	AD6	D38	E2	NC
AGP_AD<5> 35 7	E25	AD5	D37	E1	NC
AGP_AD<4> 35 7	E23	AD4	D36	D2	NC
AGP_AD<3> 35 7	D26	AD3	D35	D1	NC
AGP_AD<2> 35 7	D25	AD2	D34	C2	NC
AGP_AD<1> 35 7	C26	AD1	D33	C1	NC
AGP_AD<0> 35 7	D24	AD0	D32	B1	NC
AGP_CBE<3> 35 7	N23	CBEB3	D31	C13	NC
AGP_CBE<2> 35 7	L25	CBEB2	D30	D13	NC
AGP_CBE<1> 35 7	J25	CBEB1	D29	A14	NC
AGP_CBE<0> 35 7	F23	CBEB0	D28	B14	NC
CLK66M_AGP_ATI 35 18	AA26	PCICLK	D27	C14	NC
AGP_FRAME_L 35 7	K25	FRAMEB	D26	D14	NC
AGP_IRDY_L 35 7	K26	IRDYB	D25	A15	NC
AGP_TRDY_L 35 7	K24	TRDYB	D24	B15	NC
AGP_STOP_L 35 7	J24	STOPB	D23	B16	NC
AGP_DEVSEL_L 35 7	J26	DEVSELB	D22	C16	NC
AGP_PAR 35 7	J23	PAR	D21	D16	NC
AGP_REQ_L 35 7	AA25	REQB	D20	A17	NC
AGP_GNT_L 35 7	Y24	GNTB	D19	B17	NC
AGP_ATI_INT_L 14	AA24	INTAB	D18	C17	NC
AGP_ATI_RESET_L	AA23	RSTB	D17	A18	NC
NC	W24	SERRB	D16	B18	NC
AGP_SUS_STAT_L_PU 16	AE25	STEREOSYNC	D15	C19	NC
+1_25V_ATI_VREF 37	T2	VREF	D14	A20	NC
			D13	B20	NC
			D12	C20	NC
			D11	D20	NC
			D10	A21	NC
			D9	B21	NC
			D8	C21	NC
			D7	B22	NC
			D6	C22	NC
			D5	A23	NC
			D4	B23	NC
			D3	A24	NC
			D2	A25	NC
			D1	B25	NC
			D0	A26	NC
AGP_AD_STB<0> 35 7	F25	AD_STB0	DQMB7	N3	NC
AGP_AD_STB<1> 35 7	P25	AD_STB1	DQMB6	N2	NC
AGP_AD_STB_L<0> 35 7	F24	AD_STBB0	DQMB5	G1	NC
AGP_AD_STB_L<1> 35 7	N24	AD_STBB1	DQMB4	F2	NC
AGP_BUSY_L_PU 16	AB26	AGP_BUSYB	DQMB3	C15	NC
ATI_AGP_VREF 7	B26	AGPREF	DQMB2	A16	NC
ATI_AGP_TEST 16	C25	AGPTEST	DQMB1	D21	NC
ATI_AUXWIN_PU 16	AC22	AUXWIN	DQMB0	A22	NC
AGP_ST<0> 7	Y26	ST0	RASB	A9	NC
AGP_ST<1> 7	Y23	ST1	CASB	C8	NC
AGP_ST<2> 7	Y25	ST2	CKE	A8	NC
AGP_SBA<7> 35 7	T24	SBA7/IDSEL	WEB	D8	NC
AGP_SBA<6> 35 7	T26	SBA6	CLK0	A6	35 ATI_CLK0
AGP_SBA<5> 35 7	U24	SBA5	CLK1	A4	35 ATI_CLK1
AGP_SBA<4> 35 7	U26	SBA4	CLK0_IN	A7	35 ATI_CLK0_IN
AGP_SBA<3> 35 7	V23	SBA3	CLK1_IN	A5	35 ATI_CLK1_IN
AGP_SBA<2> 35 7	V26	SBA2	CLK0B	B6	35 ATI_CLK0_L
AGP_SBA<1> 35 7	V24	SBA1	CLK1B	B4	35 ATI_CLK1_L
AGP_SBA<0> 35 7	W25	SBA0	CLK0B_IN	B7	35 ATI_CLK0_L_IN
AGP_RBF_L 35 7	W26	RBFB	CLK1B_IN	B5	35 ATI_CLK1_L_IN
AGP_STP_L 35 7	AB25	STP_AGPB	CLKFB	B3	NC
AGP_SB_STB 35 7	V25	SB_STB	CSB0	B9	NC
AGP_SB_STB_L 35 7	U25	SB_STBB	CSB1	B8	NC
NC	C9	A13	MEMVMODE	T1	ATI_MEMVMODE 16
NC	D9	A12			
NC	A10	A11			
NC	B10	A10			
NC	C10	A9			
NC	A11	A8			
NC	B11	A7			
NC	C11	A6			
NC	D11	A5			
NC	A12	A4			
NC	B12	A3			
NC	C12	A2			
NC	A13	A1			
NC	B13	A0			

ATI_16MB
[1]R229 33 5% 1/16W MF 402
[1]R228 33 5% 1/16W MF 402
[1]R255 33 5% 1/16W MF 402
[1]R256 33 5% 1/16W MF 402

VGA SYNC BUFFERS

+3V_MAIN
74AHC1G32 SM
R2 33 5% 1/16W MF 402 — VGA_VSYNC 26
ATI_VSYNC_BUF
U1 32
ATI_VSYNC 16

PLACE THESE PARTS CLOSE TO ATI CHIP

+3V_MAIN
74AHC1G32 SM
R193 33 5% 1/16W MF 402 — VGA_HSYNC 26
ATI_HSYNC_BUF
U22 32
ATI_HSYNC 16

+3V_MAIN
NO STUFF
R400[1] 10K 5% 1/16W MF 402
R399[1] 10K 5% 1/16W MF 402
R359[1] 10K 5% 1/16W MF 402
R387[1] 10K 5% 1/16W MF 402
R378[1] 10K 5% 1/16W MF 402
R336[1] 10K 5% 1/16W MF 402
R337[1] 10K 5% 1/16W MF 402
R402[1] 10K 5% 1/16W MF 402
R401[1] 10K 5% 1/16W MF 402
R360[1] 10K 5% 1/16W MF 402
R388[1] 10K 5% 1/16W MF 402
R379[1] 10K 5% 1/16W MF 402
R335[1] 10K 5% 1/16W MF 402
R338[1] 10K 5% 1/16W MF 402

+3V_SLEEP
L57 100-OHM-EMI SM
+3V_ATI_OSC_SLEEP 37
NO STUFF
R564 100K 5% 1/16W MF 402
CRITICAL 14
VCC
G1 27.0000M OSC SM-1
ATI_OSC_OE
OE
OUT 8 — CLK27M_ATI_UF
GND 7
C644 0.1uF 20% 10V CERM 402
C645 4.7uF N20P80% 10V CERM 805

R550[1] 301 1% 1/16W MF 402
CLK27M_ATI_LS1 8
R532[1] 365 1% 1/16W MF 402
R533 22 5% 1/16W MF 402 — CLK27M_ATI AF25

OMIT
U4
RAGE_MOBILITY_M6_35X35
PBGA
(2 OF 3)

CBUS_ADDR<9> 15	AA4	ZV_LCDDATA0	ROMCSB	Y3 NC
CBUS_ADDR<17> 15	AB1	ZV_LCDDATA1	R	AF24 ATI_R 26
CBUS_ADDR<8> 15	AB2	ZV_LCDDATA2	G	AF23 ATI_G 26
CBUS_ADDR<18> 15	AB3	ZV_LCDDATA3	B	AF22 ATI_B 26
CBUS_ADDR<13> 15	AB4	ZV_LCDDATA4		
CBUS_ADDR<19> 15	AC1	ZV_LCDDATA5		
CBUS_ADDR<14> 15	AC2	ZV_LCDDATA6	VSYNC	AE23 ATI_VSYNC 16
CBUS_ADDR<20> 15	AC3	ZV_LCDDATA7	V2SYNC	AF13 NC
CBUS_ADDR<21> 15	AD1	ZV_LCDDATA8		
CBUS_ADDR<22> 15	AD2	ZV_LCDDATA9	HSYNC	AE24 ATI_HSYNC 16
CBUS_ADDR<16> 15	AD3	ZV_LCDDATA10	H2SYNC	AE14 NC
CBUS_ADDR<23> 15	AE1	ZV_LCDDATA11		
CBUS_ADDR<15> 15	AE2	ZV_LCDDATA12	RSET	AE22 ATI_RSET 17
CBUS_ADDR<24> 15	AF1	ZV_LCDDATA13	R2SET	AE16 ATI_R2SET 17
CBUS_ADDR<12> 15	AF2	ZV_LCDDATA14		
CBUS_ADDR<25> 15	AF3	ZV_LCDDATA15		
NC	AE3	ZV_LCDDATA16	Y_G	AF15 ATI_Y 26
NC	AF4	ZV_LCDDATA17	C_R	AF16 ATI_C 26
NC	AE4	ZV_LCDDATA18	COMP_B	AF14 ATI_COMP 26
NC	AD4	ZV_LCDDATA19		
NC	AF5	ZV_LCDDATA20		
NC	AE5	ZV_LCDDATA21	DIGON	AB10 ATI_DIGON 26
NC	AD5	ZV_LCDDATA22	BLONB	AB9 ATI_INV_ON_L 26
NC	AC5	ZV_LCDDATA23	HPD	AD21 NC
HREF 15	Y4	ZV_LCDCNTL0		
VSYNC 15	AA1	ZV_LCDCNTL1		
ATI_LCDCNTL2_SPN	AA2	ZV_LCDCNTL2	LTGIO0	AD7 NC
PCLK 15	AA3	ZV_LCDCNTL3	LTGIO1	AD6 LVDS_DDC_CLK 26
			LTGIO2	AC7 LVDS_DDC_DATA 26
ATI_AGP_FBSKEW<0>	Y2	GPIO0	MONID0	AD24 ATI_MONID<0> 26
ATI_AGP_FBSKEW<1>	Y1	GPIO1	MONID1	AD25 ATI_MONID<3> 26
ATI_X1CLK_SKEW<0>	W3	GPIO2		
ATI_X1CLK_SKEW<1>	W2	GPIO3	VGADDCCLK	AC25 ATI_MONID<1> 26
ATI_BUS_CFG<0>	W1	GPIO4	VGADDCDATA	AC26 ATI_MONID<2> 26
ATI_BUS_CFG<1>	V4	GPIO5		
ATI_BUS_CFG<2>	V3	GPIO6	DVIDDCCLK	AD20 NC
ATI_GPIO7 16	V2	GPIO7	DVIDDCDATA	AC20 NC
ATI_GPIO8_SPN	V1	GPIO8		
ATI_GPIO9 16	U3	GPIO9	CRT2DDCCLK	AF6 NC
ATI_GPIO10 16	U2	GPIO10	CRT2DDCDAT	AF7 NC
ATI_GPIO11_SPN	U1	GPIO11		
ATI_GPIO12_SPN	T4	GPIO12	TXOUT_U0N	AD11 NC
ATI_GPIO13_SPN	T3	GPIO13	TXOUT_U0P	AC11 NC
			TXOUT_U1N	AE11 NC
NC	A19	QS0	TXOUT_U1P	AF11 NC
NC	B19	QS1	TXOUT_U2N	AD12 NC
NC	D18	QS2	TXOUT_U2P	AC12 NC
NC	C18	QS3	TXOUT_U3N	AD13 NC
NC	J4	QS4	TXOUT_U3P	AE13 NC
NC	K1	QS5	TXCLK_UN	AE12 NC
NC	K2	QS6	TXCLK_UP	AF12 NC
NC	K3	QS7	TXOUT_L0N	AC8 LVDS_L0N 26 36
NC	AE19	TX0M	TXOUT_L0P	AD8 LVDS_L0P 26 36
NC	AF19	TX0P	TXOUT_L1N	AC9 LVDS_L1N 26 36
NC	AE20	TX1M	TXOUT_L1P	AD9 LVDS_L1P 26 36
NC	AF20	TX1P	TXOUT_L2N	AE8 LVDS_L2N 26 36
NC	AE21	TX2M	TXOUT_L2P	AF8 LVDS_L2P 26 36
NC	AF21	TX2P	TXOUT_L3N	AC10 LVDS_L3N_SPN
NC	AE18	TXCM	TXOUT_L3P	AD10 LVDS_L3P_SPN
NC	AF18	TXCP	TXCLK_LN	AE9 CLKLVDS_N 26 36
			TXCLK_LP	AF9 CLKLVDS_P 26 36
	AF25	XTALIN		
	AF26	XTALOUT		
ATI_TESTEN 16	AC6	TESTEN		
ATI_SSIN 16	AE6	SSIN	SSOUT	AE7 ATI_SSOUT 16

SPREAD SPECTRUM SUPPORT

+3V_MAIN
ATI_SS
L51 100-OHM-EMI SM
+3V_ATI_SS 37
ATI_SS
C462 0.1uF 20% 10V CERM 402
C426 4.7uF N20P80% 10V CERM 805
ATI_SS 2 CRITICAL
VDD
ICLK U18 MK1708 SOI
ATI_SSOUT 16
ATI_GPIO7 16
ATI_GPIO9 16
ATI_GPIO10 16
S0
S1
PD
CLK 4
NC 5 NC
GND 3
ATI_SS
R459 33 5% 1/16W MF 402 — ATI_SSIN 16
ATI_SSIN_UF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0001	1	ATI RAGE MOBILITY M6-M	U4	CRITICAL	ATI_8MB
338S0002	1	ATI RAGE MOBILITY M6-D	U4	CRITICAL	ATI_16MB

MOBILITY RADEON AGP&I/O

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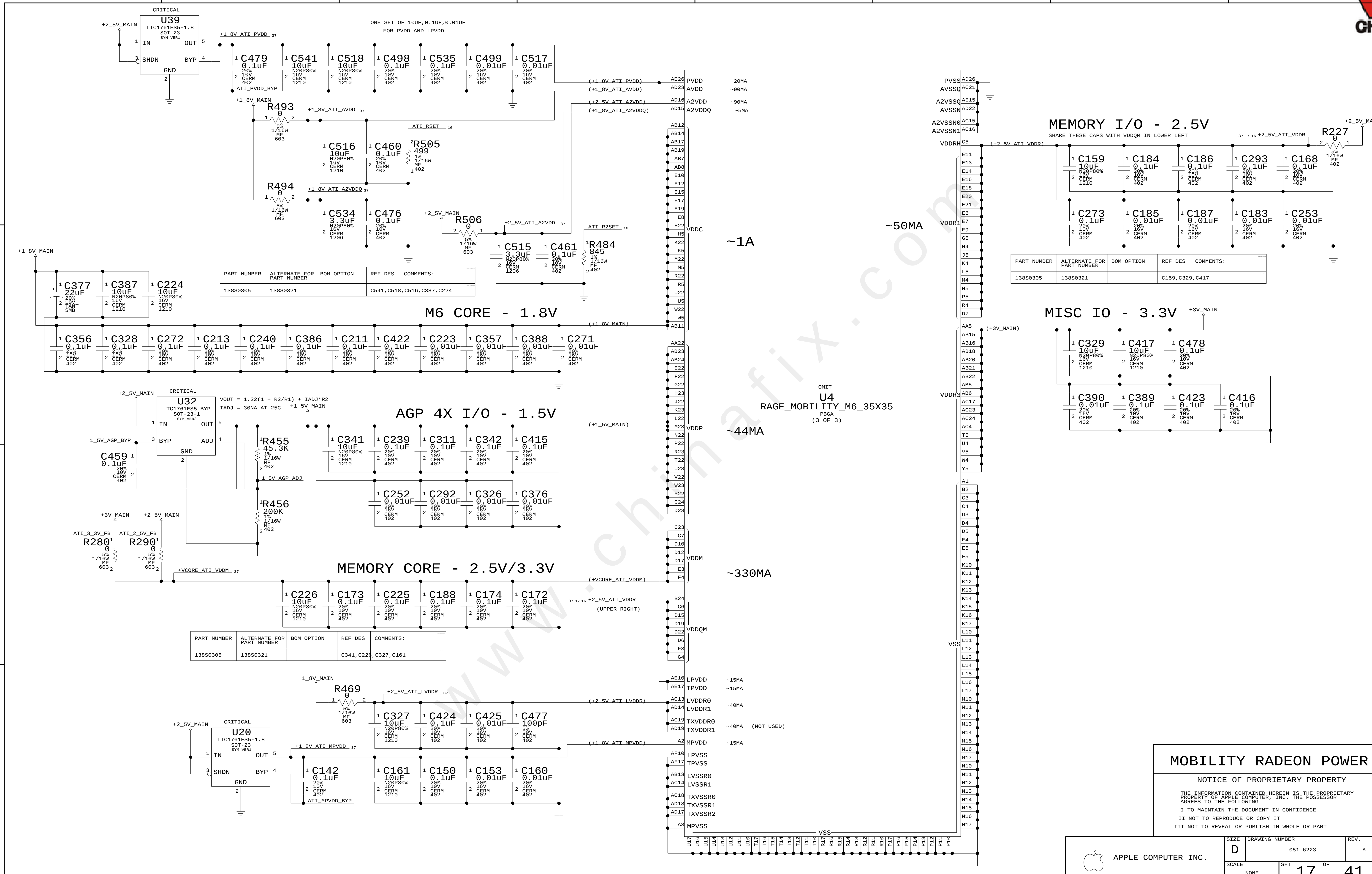
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 16 OF 41	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C541,C518,C516,C387,C224	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C159,C329,C417	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C341,C226,C327,C161	

MOBILITY RADEON POWER

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SCALE NONE | SHT 17 OF 41

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C476,C490	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0702	197S0602		Y5	

S2	S1	S0	CPU(0,1)	SDRAM(0:3)	3V66(0:2)	PCI(0:6)	48M0	48M1	REF
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	100.23	100.23	66.82	33.41	Low	Low	14.318
0	1	0	100.02	100.02	66.68	33.34	48	Low	14.318
0	1	1	100.02	100.02	66.68	33.34	48	48	14.318
1	0	0	XIN/2	XIN/2	XIN/3	XIN/6	XIN/2	XIN	XIN
1	0	1	133.16	133.16	66.58	33.29	Low	Low	14.318
1	1	0	133.25	133.25	66.63	33.31	48	Low	14.318
1	1	1	133.25	133.25	66.63	33.31	48	48	14.318

Allows the PMU to control the bus speed

PLACE OSCILLATOR CLOSE TO PLL.
LOAD CAPACITANCE IS MATCHED TO THE INTERNAL CAPACITANCE(32/2) OF THE PLL AT 16PF.

PLACE CLOSE TO C5005 GROUND

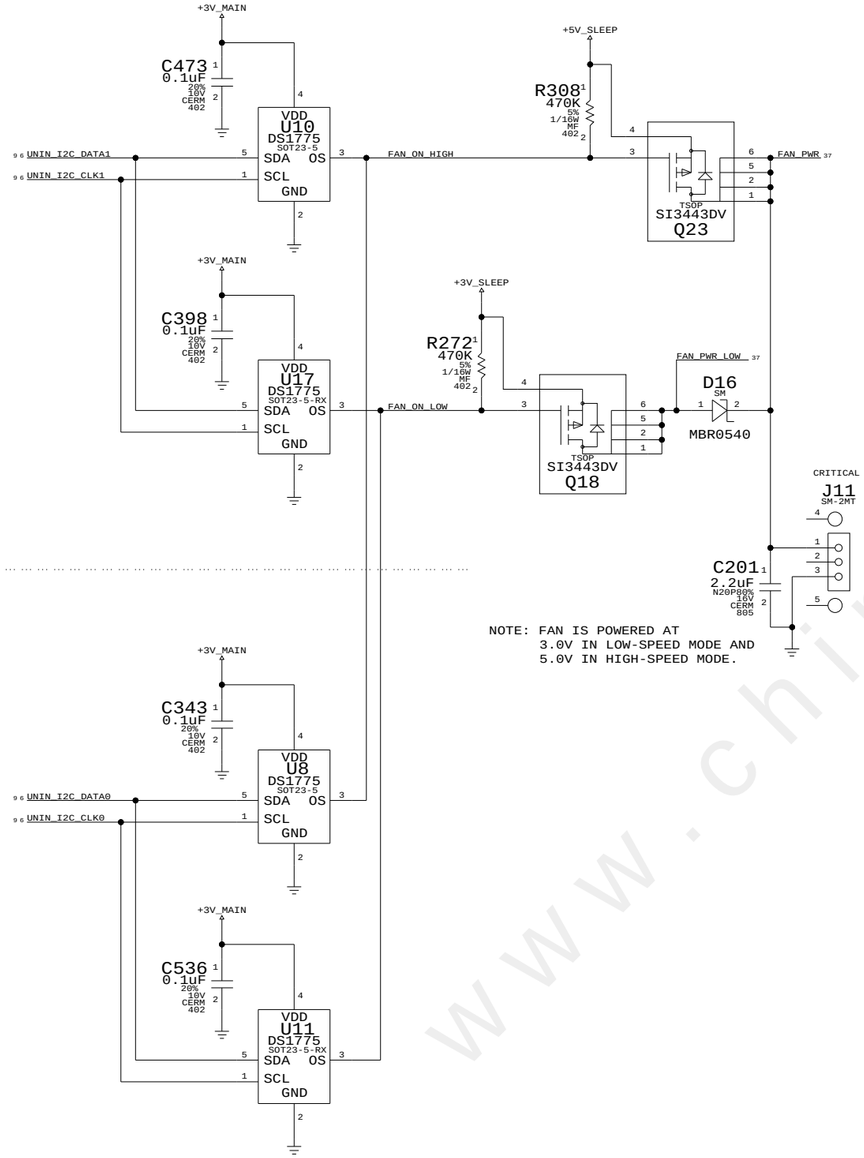
SYSTEM CLOCK GENERATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 18 OF 41	

DUAL-SPEED FAN CIRCUIT

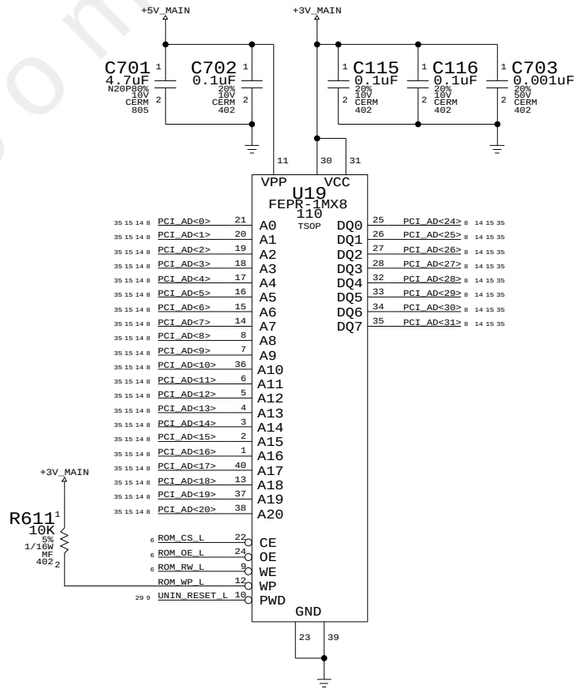
NOTE: PLACE THESE SENSORS NEAR V'GER(U15)



NOTE: FAN IS POWERED AT
3.0V IN LOW-SPEED MODE AND
5.0V IN HIGH-SPEED MODE.

NOTE: PLACE THESE SENSORS NEAR MOBILITY RADEON(U4)

FLASH ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S0976	1	IC,BOOTROM,V4.2.9F1	U19	

BOOTROM/FAN CIRCUIT

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 19 OF 41	

DIGITAL EQUALIZER

L47 1000-OHM-EMI PLACE THESE CAPS NEAR TAS3001C
L49 1000-OHM-EMI
XW11
U30 TAS3001C TSSOP CRITICAL
R347 2.21K
R652 NO STUFF 0
R653 47K
R654 10K
R655 NO STUFF 0
R656 47K
R39 47K
Q68 2N7002
Q69 2N7002
C743 100pF

DIGITAL TO ANALOG CONVERTER

L9 1000-OHM-EMI PLACE THESE CAPS NEAR TLC320
L8 1000-OHM-EMI
U33 TLC320AD77C SOI CRITICAL
R48 R50 R34 R47 R49 R33 NO STUFF 10K
NEED TO ADD STUFFING OPTIONS
R35 10
C55 15uF
C56 47uF
L54 1000-OHM-EMI

AUDIO POWER SUPPLIES

U16 PLUS5VTAP LP2951 SOI
U36 PLUS5VTAP LP2951 SOI
R669 49.9K
R670 20K
R69 100K
R70 60.4K

TUMBLER CONTROL

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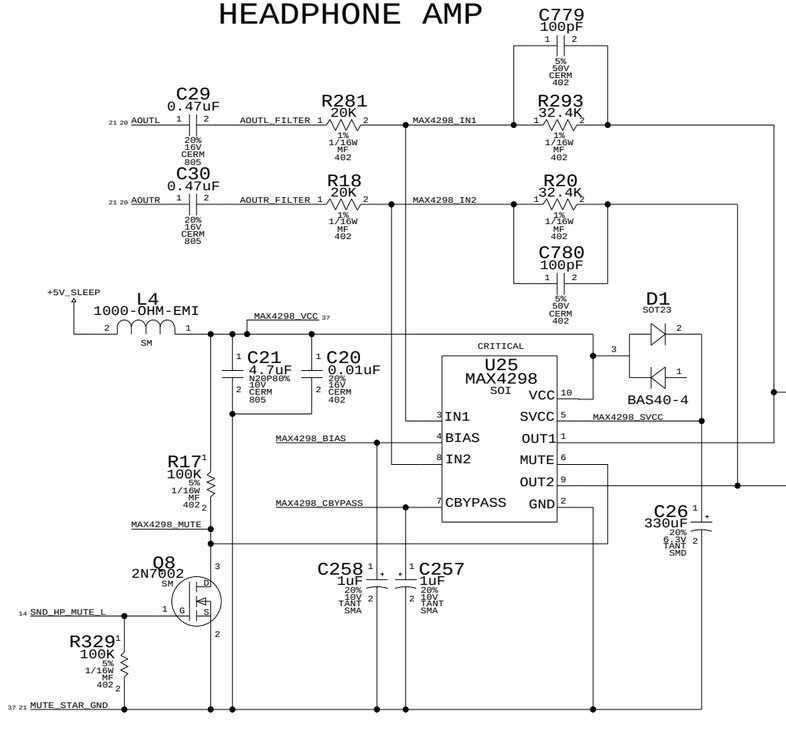
D	051-6223	A

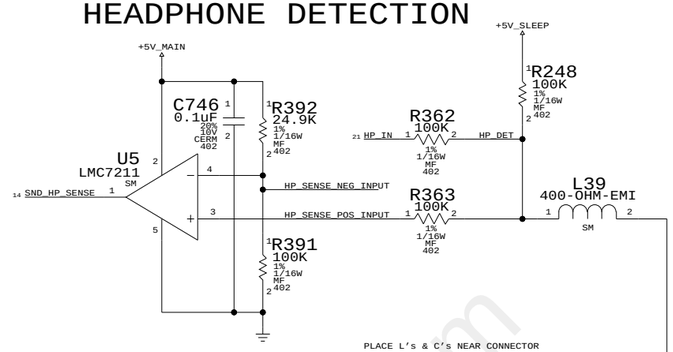
SCALE NONE

SHT 20 OF 41

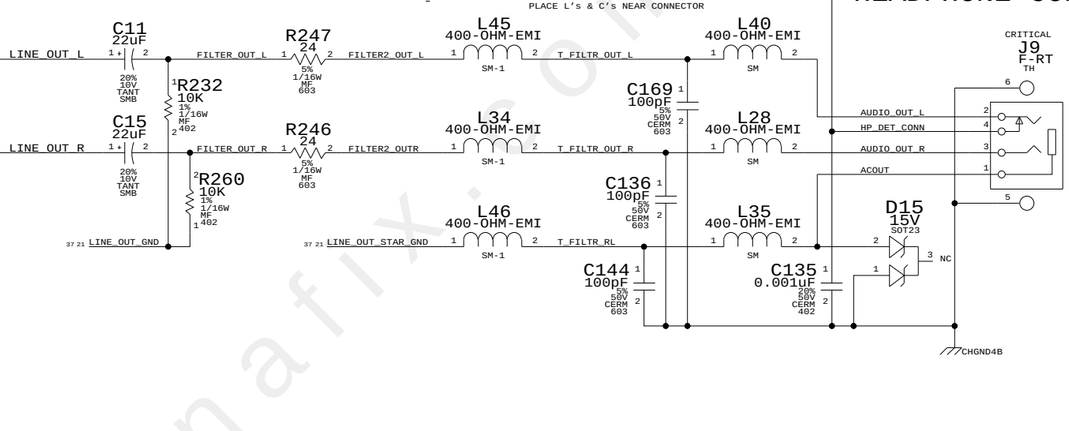
HEADPHONE AMP



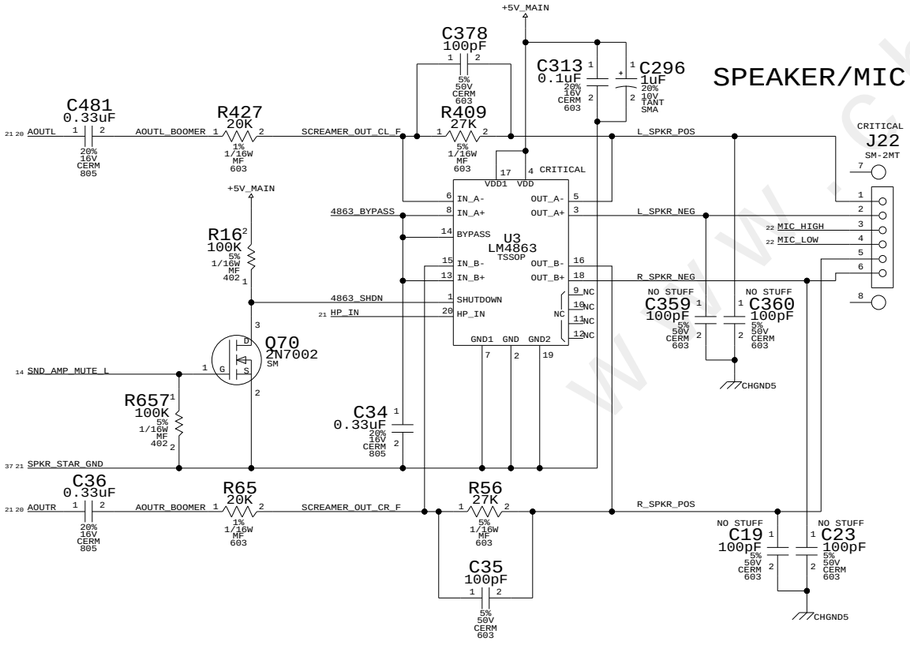
HEADPHONE DETECTION



HEADPHONE CONNECTOR

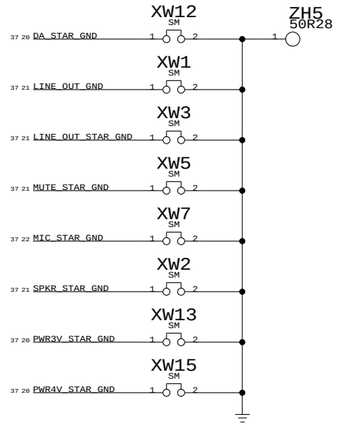


BOOMER SPEAKER AMP



SPEAKER/MIC CONNECTOR

AUDIO STAR GROUND

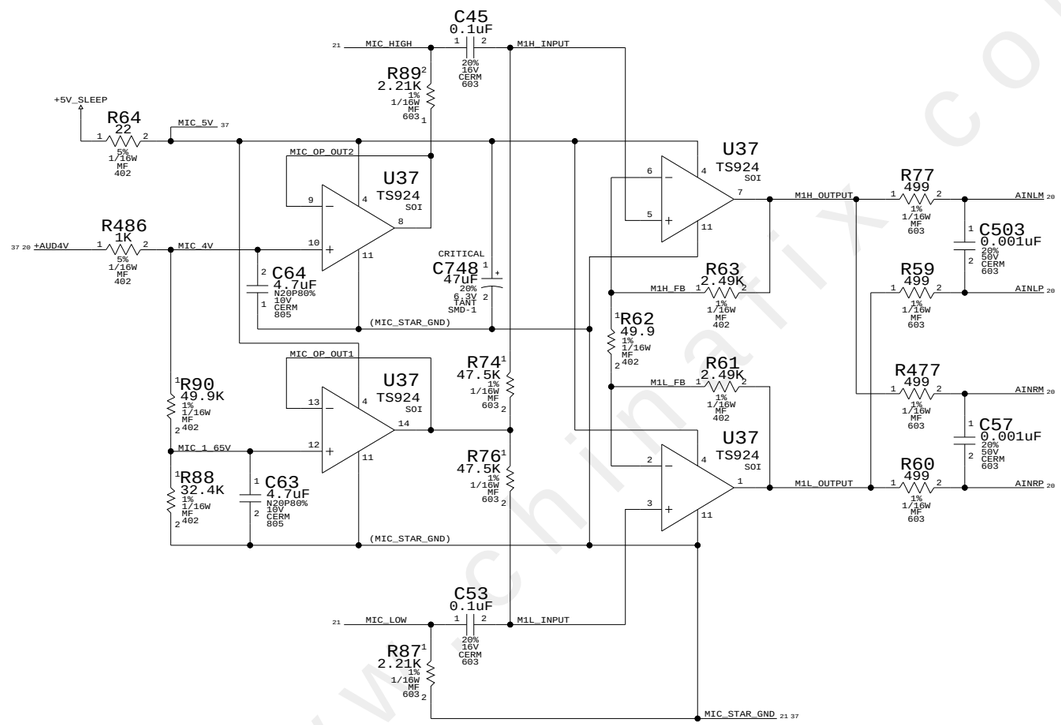


HEADPHONE/SPEAKERS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE		SHT 21 OF 41

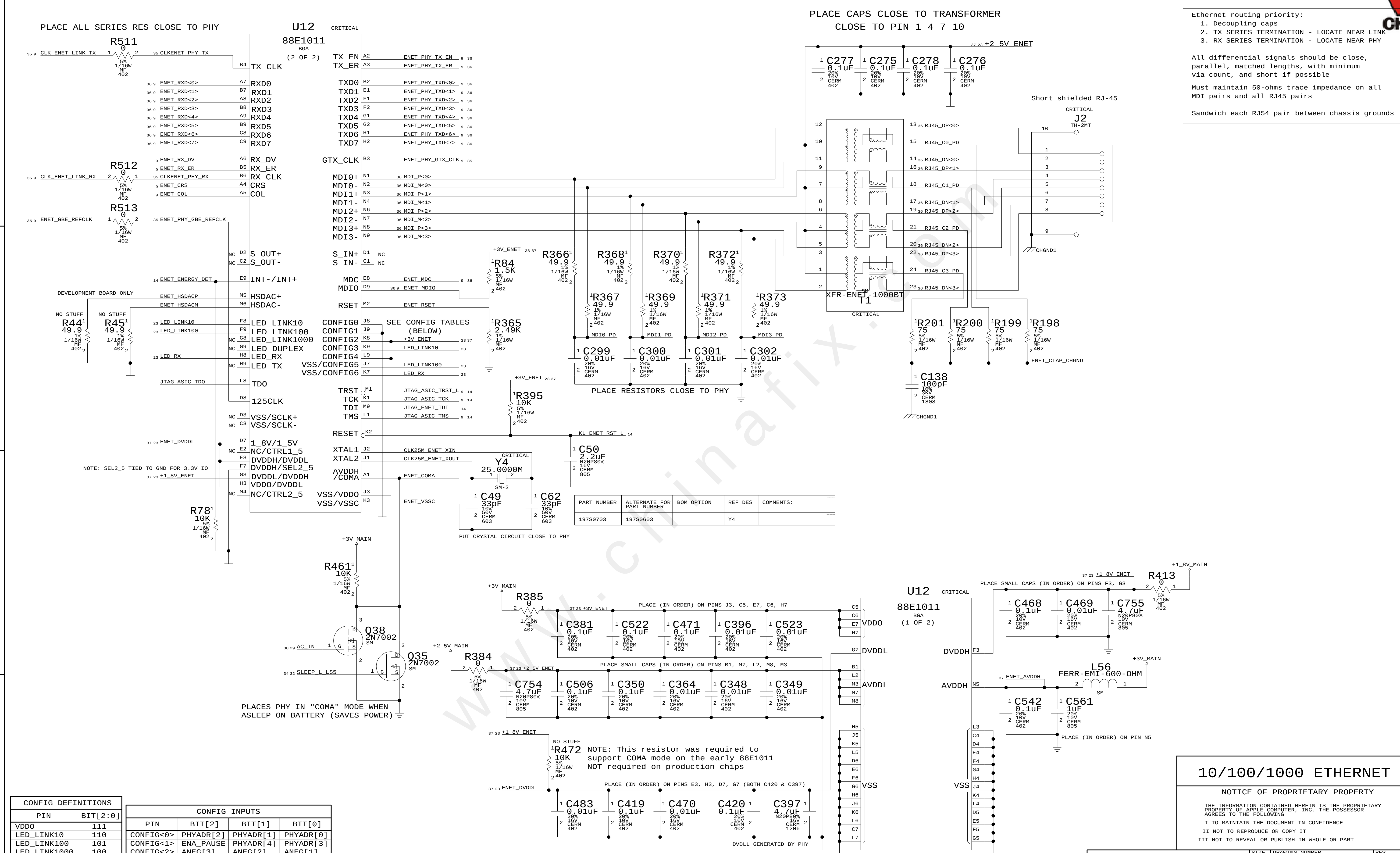
MICROPHONE AMPLIFIER



MICROPHONE INPUT

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 22 OF 41	



Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0603		Y4	

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_I2C	INT_POL	75/50 OHM

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6223 | REV. A | SCALE NONE

PORT POWER SWITCH

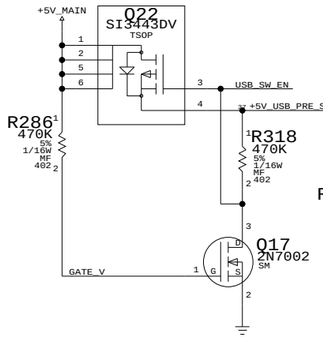
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0706	197S0606		Y3	

FIREWIRE

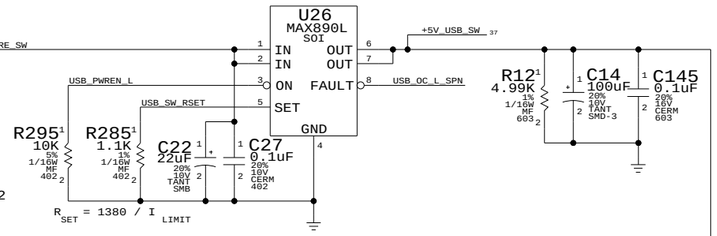
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 24 OF 41	

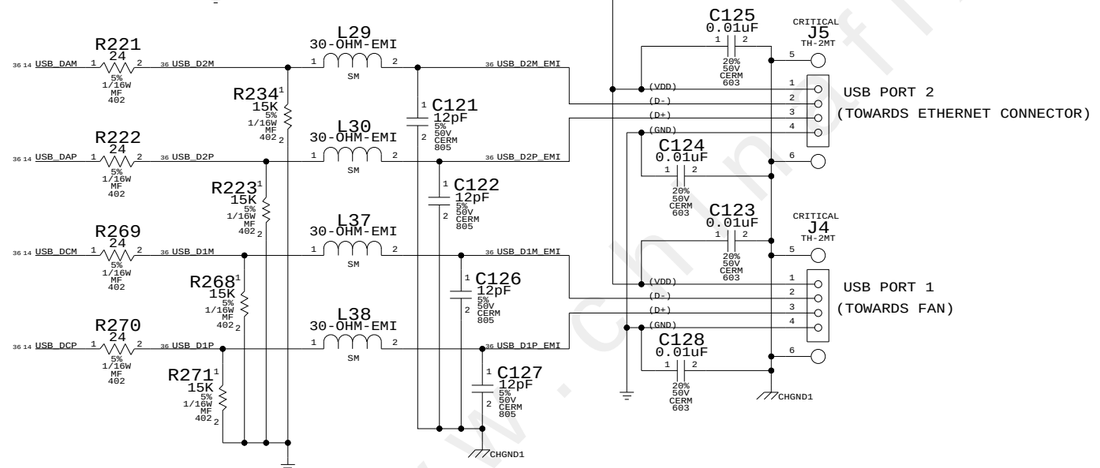
USB BACKFEED PROTECTION



USB CURRENT LIMITER

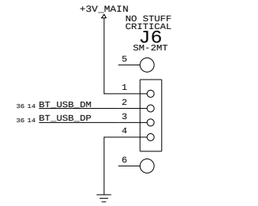


USB PORTS



BLUETOOTH INTERFACE

(4-pin Wire-to-Board Connector)

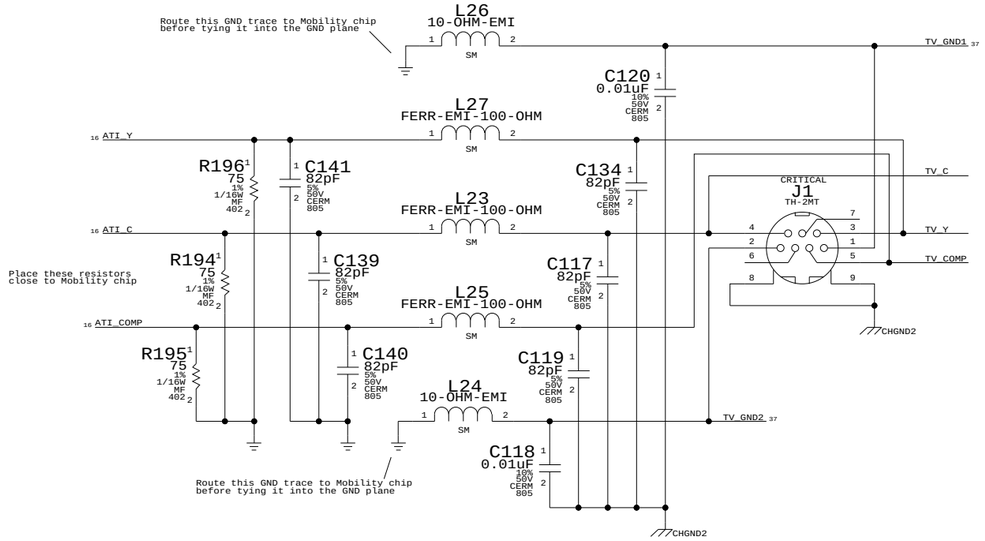


USB & BLUETOOTH

APPLE COMPUTER INC.

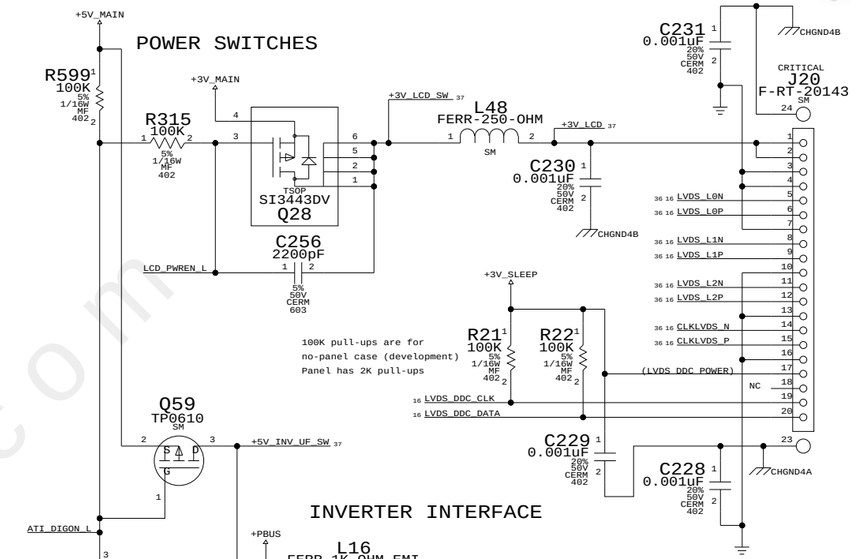
SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 25 OF 41	

S-VIDEO/COMP OUT INTERFACE



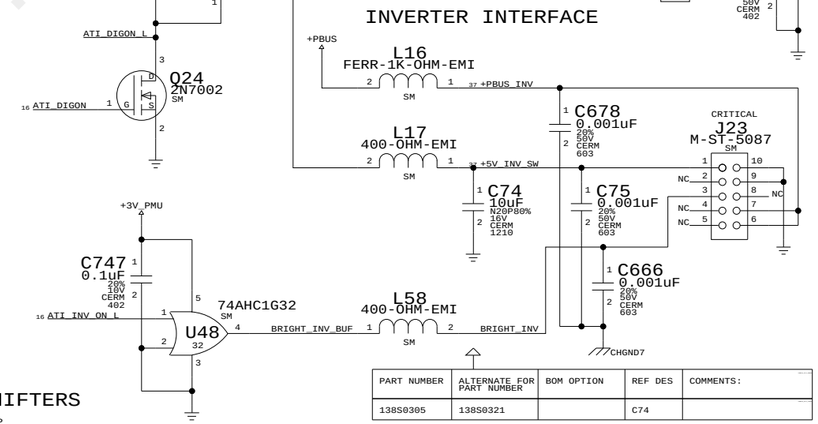
LCD INTERFACE

POWER SWITCHES



LVDS INTERFACE

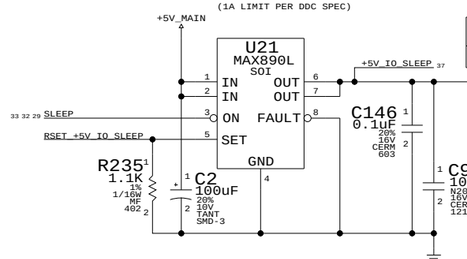
INVERTER INTERFACE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C74	

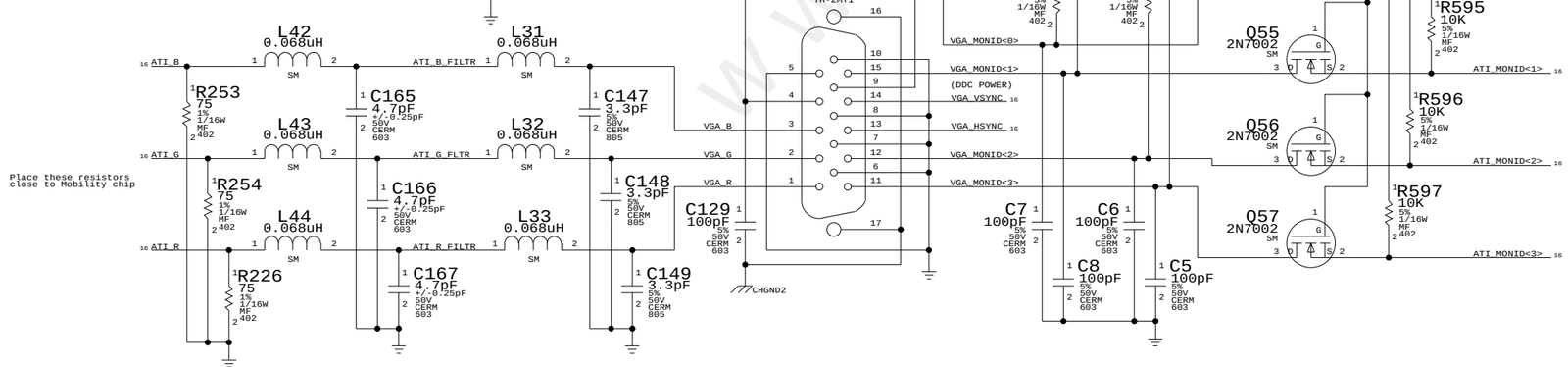
VGA DDC CURRENT LIMIT

(1A LIMIT PER DDC SPEC)



EXTERNAL VIDEO (VGA) INTERFACE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C9	



3V LEVEL SHIFTERS

VIDEO CONNECTORS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 26 OF 41	

CARDSLOT/EIDE SERIES TERMINATION

THESE LINES ARE SHARED BETWEEN THE CARDSLOT AND EIDE INTERFACES
PLEASE PLACE THESE TERMINATORS CLOSE TO KEYLARGO AND MINIMIZE THE LENGTH OF THE T

Place resistor packs close to KeyLargo (U45)

RP8, RP7, RP6, RP5, RP9: 33 5% 1/16W SM

EIDE_DATA	CSLOT_DATA
EIDE_DATA<2>	CSLOT_DATA<2>
EIDE_DATA<1>	CSLOT_DATA<1>
EIDE_DATA<0>	CSLOT_DATA<0>
EIDE_DATA<3>	CSLOT_DATA<3>
EIDE_DATA<6>	CSLOT_DATA<6>
EIDE_DATA<7>	CSLOT_DATA<7>
EIDE_DATA<4>	CSLOT_DATA<4>
EIDE_DATA<5>	CSLOT_DATA<5>
EIDE_DATA<11>	CSLOT_DATA<11>
EIDE_DATA<9>	CSLOT_DATA<9>
EIDE_DATA<10>	CSLOT_DATA<10>
EIDE_DATA<8>	CSLOT_DATA<8>
EIDE_DATA<15>	CSLOT_DATA<15>
EIDE_DATA<13>	CSLOT_DATA<13>
EIDE_DATA<14>	CSLOT_DATA<14>
EIDE_DATA<12>	CSLOT_DATA<12>
EIDE_ADDR<0>	CSLOT_ADDR<0>
EIDE_ADDR<2>	CSLOT_ADDR<2>
EIDE_ADDR<1>	CSLOT_ADDR<1>
EIDE_CS1FX_L	CSLOT_CS1FX_L

R103 33 5% 1/16W MF 402: EIDE_CS3FX_L — CSLOT_CS3FX_L

PLACE TERMINATORS NEAR KEY LARGO

RP24, RP21, RP22, RP23: 33 5% 1/16W SM

EIDE_DB	EIDE_DATA
EIDE_DB_<8>	EIDE_DB_<8>
EIDE_DB_<10>	EIDE_DB_<10>
EIDE_DB_<9>	EIDE_DB_<9>
EIDE_DB_<11>	EIDE_DB_<11>
EIDE_DB_<12>	EIDE_DB_<12>
EIDE_DB_<14>	EIDE_DB_<14>
EIDE_DB_<13>	EIDE_DB_<13>
EIDE_DB_<15>	EIDE_DB_<15>
EIDE_DB_<2>	EIDE_DATA<2>
EIDE_DB_<1>	EIDE_DATA<1>
EIDE_DB_<0>	EIDE_DATA<0>
EIDE_DB_<3>	EIDE_DATA<3>
EIDE_DB_<6>	EIDE_DATA<6>
EIDE_DB_<7>	EIDE_DATA<7>
EIDE_DB_<4>	EIDE_DATA<4>
EIDE_DB_<5>	EIDE_DATA<5>

R581, R579, R580, R578, R577: 33 5% 1/16W MF 402

EIDE_ADDR<0>	EIDE_ADDR_<0>
EIDE_ADDR<1>	EIDE_ADDR_<1>
EIDE_ADDR<2>	EIDE_ADDR_<2>
EIDE_CS1FX_L	EIDE_CS1FX*
EIDE_CS3FX_L	EIDE_CS3FX*

R158 82, R156 22, R154 22, R143 22, R155 82, R157 82, R160 33: 5% 1/16W MF 402

EIDE0_DMARQ	EIDE0_DMA_RQ
EIDE0_DMACK_L	EIDE0_DMA_ACK_L
EIDE0_RD_L	EIDE0_READ_L
EIDE0_WR_L	EIDE0_WR*
EIDE_IOCHRDY	EIDE_IO_CHRDY
EIDE0_INT	EIDE0_INTR
EIDE0_RST_L	EIDE0_RST*

R563 10K 5% 1/16W MF 402

CARDSLOT (WIRELESS) INTERFACE

+3V_SLEEP

RP28, RP26: 10K 5% 1/16W SM

CRITICAL J25 SM-M M70SM_5MM

CSLOT_DATA<3>	Card Detect #1
CSLOT_DATA<4>	CSLOT_DATA<11>
CSLOT_DATA<5>	CSLOT_DATA<12>
CSLOT_DATA<6>	CSLOT_DATA<13>
CSLOT_DATA<7>	CSLOT_DATA<14>
CSLOT_CE1_L	CSLOT_DATA<15>
CSLOT_ADDR<10>	CSLOT_CE2_L
CSLOT_CS1FX_L	Voltage Sense #1
CSLOT_ADDR<11>	CSLOT_IORD_L
CSLOT_ADDR<9>	CSLOT_IOWR_L
CSLOT_ADDR<8>	
CSLOT_ADDR<13>	
CSLOT_ADDR<14>	
CSLOT_CS3FX_L	
CSLOT_IRQ_L	
(ADDR<16>)	
CSLOT_ADDR<15>	(VOLTAGE SENSE #2)
CSLOT_ADDR<12>	CSLOT_RESET
CSLOT_ADDR<7>	CSLOT_IOWAIT_L
CSLOT_ADDR<6>	(INPUT PORT ACK)
CSLOT_ADDR<5>	CSLOT_REG_L
CSLOT_ADDR<4>	(SPEAKER)
CSLOT_ADDR<3>	(CARD STATUS CHANGED)
CSLOT_ADDR<2>	CSLOT_DATA<8>
CSLOT_ADDR<1>	CSLOT_DATA<9>
CSLOT_ADDR<0>	CSLOT_DATA<10>
CSLOT_DATA<0>	+5V_TOL
CSLOT_DATA<1>	
CSLOT_DATA<2>	
(IOCS16_L)	

+5V_SLEEP

R163 470 5% 1/16W MF 402

DVD INTERFACE

+5V_SLEEP

R112 100K 5% 1/16W MF 402; R111 10K 5% 1/16W MF 402; R110 10K 5% 1/16W MF 402

CRITICAL J24 SM-M

EIDE_DB_<8>	EIDE0_RST*
EIDE_DB_<9>	EIDE_DB_<7>
EIDE_DB_<10>	EIDE_DB_<6>
EIDE_DB_<11>	EIDE_DB_<5>
EIDE_DB_<12>	EIDE_DB_<4>
EIDE_DB_<13>	EIDE_DB_<3>
EIDE_DB_<14>	EIDE_DB_<2>
EIDE_DB_<15>	EIDE_DB_<1>
EIDE0_DMA_RQ	EIDE_DB_<0>
EIDE0_READ_L	
	EIDE0_WR*
EIDE0_DMA_ACK_L	EIDE_IO_CHRDY
PIN 30 NOT USED	EIDE0_INTR
PIN 32 NOT USED	EIDE_ADDR_<1>
EIDE_ADDR_<2>	EIDE_ADDR_<0>
EIDE_CS3FX*	EIDE_CS1FX*

R109 20K 5% 1/16W MF 402; R569 10K 5% 1/16W MF 402

IRDA INTERFACE

+3V_SLEEP

CRITICAL J12 M-ST-5087 SM

KL_IRDA_RXD_L	
KL_IRDA_FIR_L	NC
KL_IRDA_TXD	

INTERNAL HARD DRIVE INTERFACE

RP37, RP36, RP38, RP39: 33 5% 1/16W SM

UIDE_DATA	HD_DATA
UIDE_DATA<0>	HD_DATA<0>
UIDE_DATA<1>	HD_DATA<1>
UIDE_DATA<2>	HD_DATA<2>
UIDE_DATA<3>	HD_DATA<3>
UIDE_DATA<4>	HD_DATA<4>
UIDE_DATA<5>	HD_DATA<5>
UIDE_DATA<6>	HD_DATA<6>
UIDE_DATA<7>	HD_DATA<7>
UIDE_DATA<8>	HD_DATA<8>
UIDE_DATA<9>	HD_DATA<9>
UIDE_DATA<10>	HD_DATA<10>
UIDE_DATA<11>	HD_DATA<11>
UIDE_DATA<12>	HD_DATA<12>
UIDE_DATA<13>	HD_DATA<13>
UIDE_DATA<14>	HD_DATA<14>
UIDE_DATA<15>	HD_DATA<15>

R631 33 5% 1/16W MF 402: UIDE_RST_L — HD_RESET_L

R621 22 5% 1/16W MF 402: UIDE_DIOW_L — HD_DIOW_L

R622 22 5% 1/16W MF 402: UIDE_DIOR_L — HD_DIOR_L

R623 22 5% 1/16W MF 402: UIDE_DMACK_L — HD_DMACK_L

R624 33 5% 1/16W MF 402: UIDE_ADDR<1> — HD_ADDR<1>

R625 33 5% 1/16W MF 402: UIDE_ADDR<0> — HD_ADDR<0>

R626 33 5% 1/16W MF 402: UIDE_CS1FX_L — HD_CS1_L

R636 33 5% 1/16W MF 402: UIDE_ADDR<2> — HD_ADDR<2>

R635 33 5% 1/16W MF 402: UIDE_CS3FX_L — HD_CS3_L

R620 10K 5% 1/16W MF 402

R628 10K 5% 1/16W MF 402; R630 10K 5% 1/16W MF 402; R629 100K 5% 1/16W MF 402

CRITICAL J26 SM-M M50SM_5MM

+5V_HD_SLEEP

HD_RESET_L	
HD_DATA<7>	HD_DATA<8>
HD_DATA<6>	HD_DATA<9>
HD_DATA<5>	HD_DATA<10>
HD_DATA<4>	HD_DATA<11>
HD_DATA<3>	HD_DATA<12>
HD_DATA<2>	HD_DATA<13>
HD_DATA<1>	HD_DATA<14>
HD_DATA<0>	HD_DATA<15>
HD_DMARQ	
HD_DIOW_L	
HD_DIOR_L	
HD_IOCHRDY	
HD_DMACK_L	
HD_INTRQ	NC
HD_ADDR<1>	
HD_ADDR<0>	HD_ADDR<2>
HD_CS1_L	HD_CS3_L
NC	NC

R633 10K 5% 1/16W MF 402; R632 20K 5% 1/16W MF 402

MODEM BOARD INTERFACE

+3V_MAIN

C500 10uF N20P80% 16V CERM 1210; C537 0.1uF 20% 16V CERM 603

CRITICAL J13 F-ST-5047 SM

R485 10K 5% 1/16W MF 402

	COMM_RESET_L
COMM_SHUTDOWN	COMM_RTS_L
	COMM_DTR_L
COMM_RXD	
COMM_GPIO_L	COMM_TXD_L
	COMM_TRXC
COMM_RING_DET_L	
DAA_OUT_1/MODEM_HOOK_RELAY	MODEM_USB_DM
	MODEM_USB_DP
KL_I2C_CLK	
	KL_I2C_DATA
I2C_ADDR_S0	I2C_ADDR_S1
COMM_ANALOG_SND	+5V_MAIN
COMM_ANALOG_SND_RET	

R444 10K 5% 1/16W MF 402

C538 0.1uF 20% 16V CERM 603; C501 10uF N20P80% 16V CERM 1210

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C500,C501	

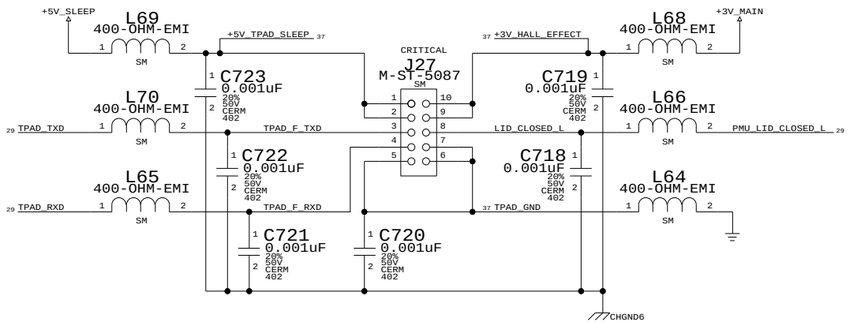
INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.

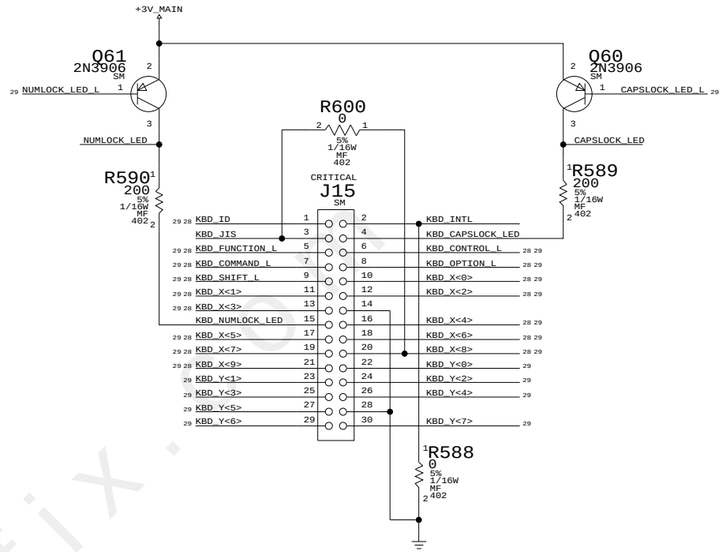
SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 27 OF 41	

TRACKPAD/SLEEP SWITCH INTERFACE

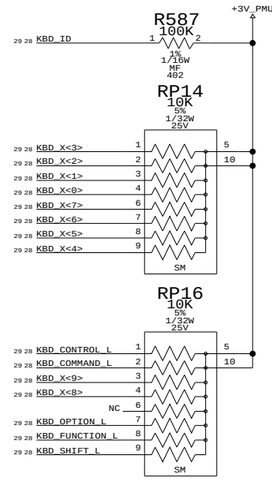
Place discretes close to connector



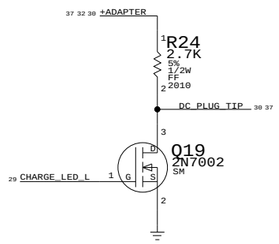
KEYBOARD INTERFACE



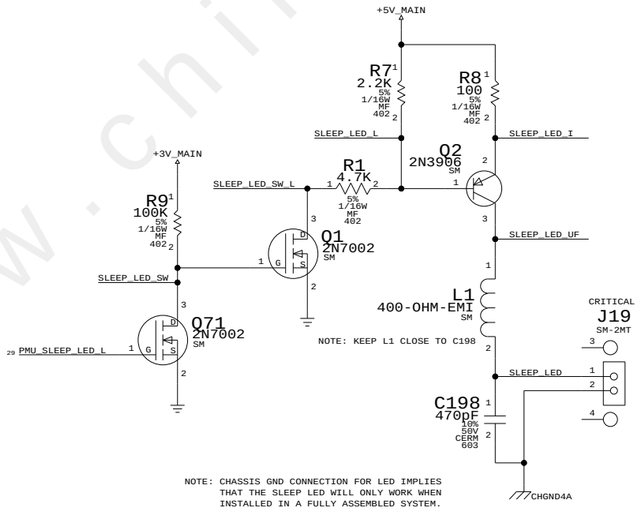
KEYBOARD PULLUPS



CHARGE LED SUPPORT

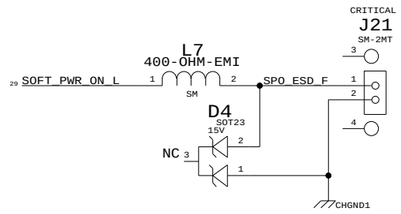


SLEEP LED



NOTE: CHASSIS GND CONNECTION FOR LED IMPLIES THAT THE SLEEP LED WILL ONLY WORK WHEN INSTALLED IN A FULLY ASSEMBLED SYSTEM.

POWER BUTTON INTERFACE



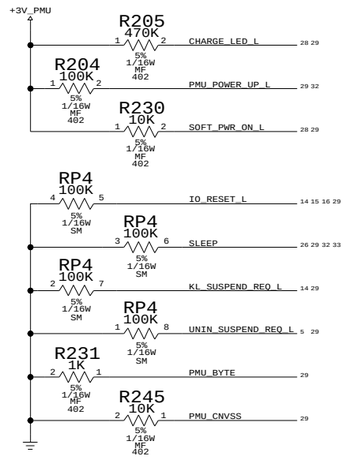
NOTE: CURRENT RETURN PATH IS VIA CHGND1, R192, AND L3 AT DC JACK

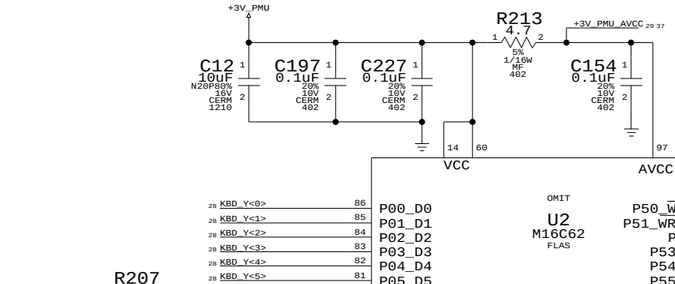
PMU INTERFACES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A

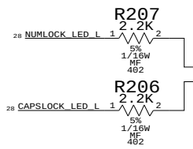
SCALE	SHT	OF
NONE	28	41

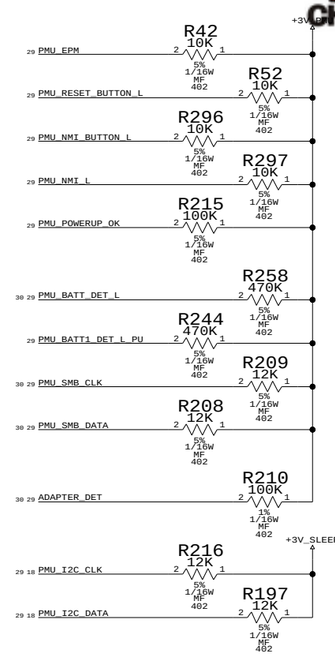




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S0618	1	IC,PMU BASE IMAGE 66B,64K FLSH	U2	

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

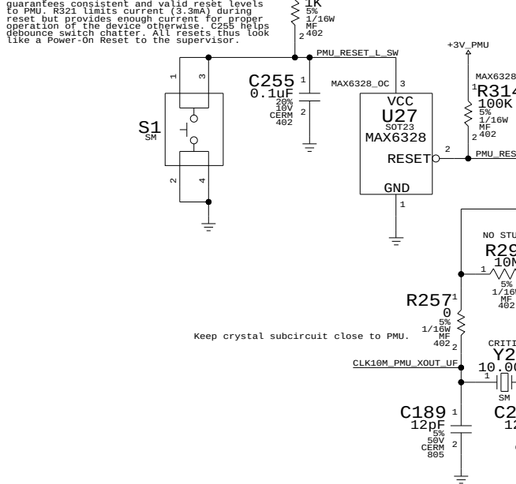




UNDERVOLTAGE RESET CIRCUIT

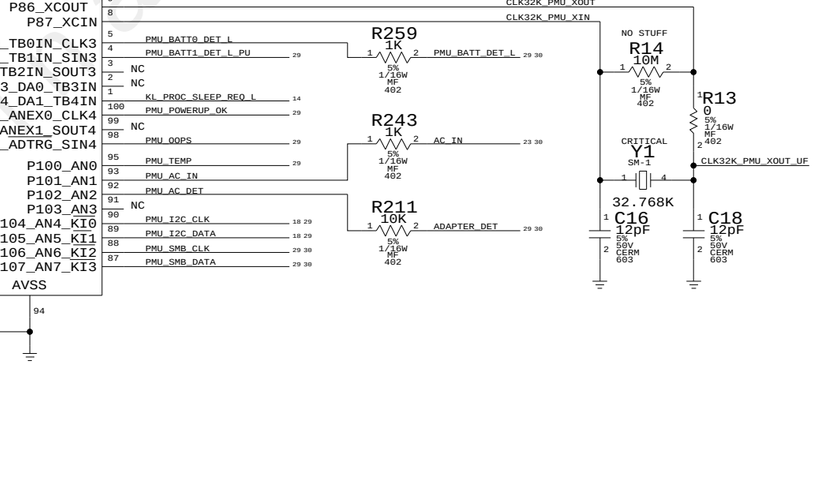
PMU RESET SWITCH

Placing switch on input to reset supervisor guarantees consistent and valid reset levels to PMU. R321 limits current (3.3mA) during reset but provides enough current for proper operation of the device otherwise. C255 helps debounce switch chatter. All resets thus look like a Power-On Reset to the supervisor.

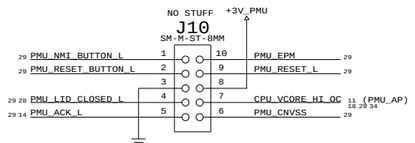


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0604		Y2	Alt crystal size

Keep crystal subcircuit close to PMU.



PMU DOWNLOAD CONNECTOR



NOTE: PMU Undervoltage circuit supports MAX6328 (open-drain) as well as MAX6326 (push-pull)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0255	1	IC, MAX6326 RESET, 2.63V, SOT23-3	U27	MAX6326_PP
116S1473	1	RES, 4.7K, 5%, 1/16W, MF, 402	R292	MAX6326_PP

R2237 IS NO STUFFED FOR MAX6326_PP!!!

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0809	353S0255	MAX6326_PP	U27	MAX809S

PMU INTERFACE

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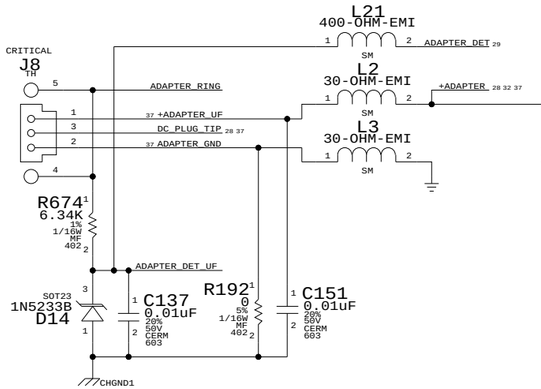
APPLE COMPUTER INC.

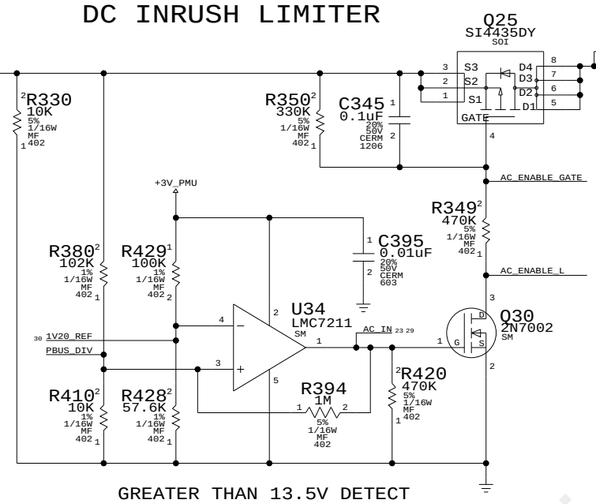
SIZE	DRAWING NUMBER	REV.
D	051-6223	A

SCALE	SHT	OF
NONE	29	41

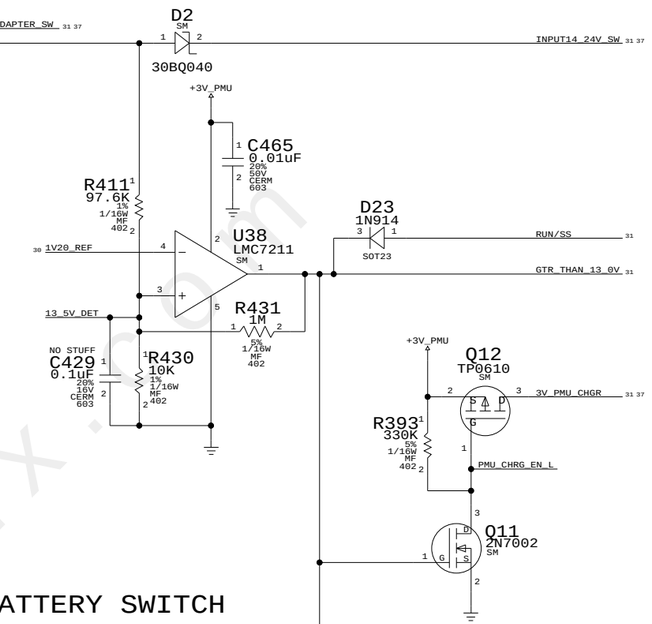
DC POWER JACK



DC INRUSH LIMITER

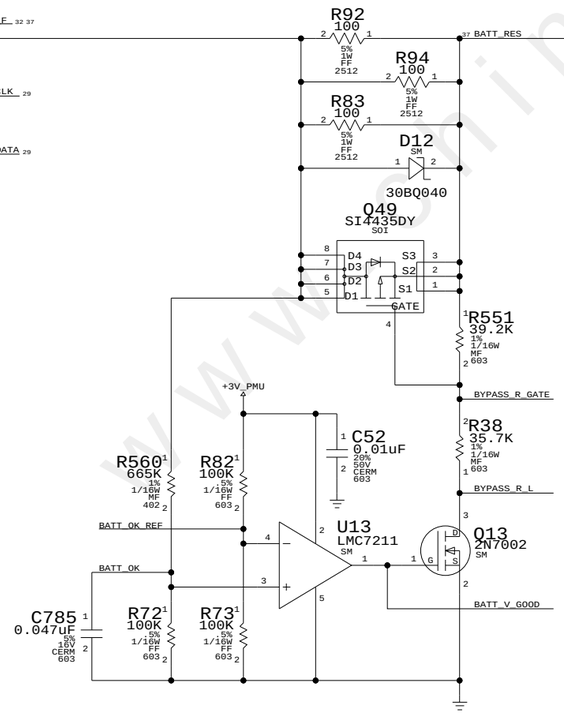


DC POWER SEQUENCING

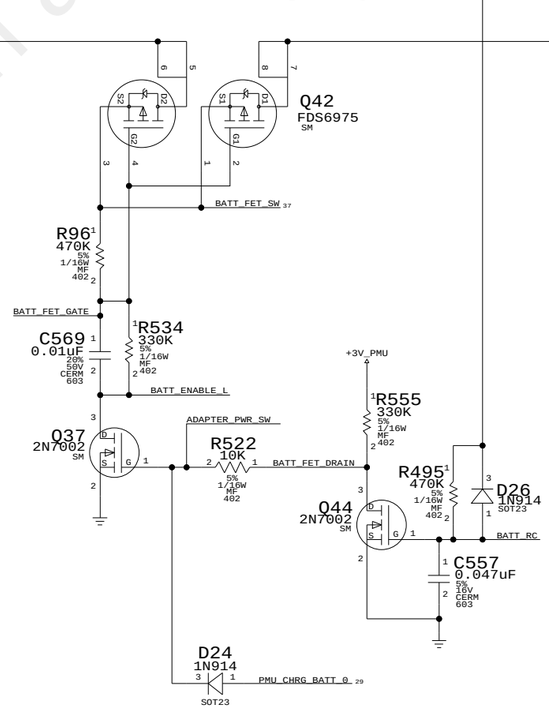


BATTERY CONNECTOR

LOW-VOLTAGE CHARGE LIMITER



BATTERY SWITCH



ADAPTER & BATTERY INTERFACES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 30 OF 41	

BATTERY CHARGING CURRENT LIMIT

TO BATTERY <-
FROM BATTERY ->

BATT_LINE — R294 0.025 2% 1W MF 2512 — BATT_ISNS — F2 5AMP-125V SM-2

PBUS hold-up cap: C1 220uF 20% 35V ELEC SM

+PBUS -> TO SYSTEM

3V_PMU_CHGR — IBATT_RC_COMP — C314 0.1uF 20% 16V CERM 603

PWRBUS_14_24V — C175 0.01uF 20% 50V CERM 603

U23 MAX4172 SOI: V+, RS-, RS+, PG, NC1, OUT, NC2, GND

U29 LMC6462 SOI

R352 1K 1% 1/16W MF 603

R322 20.5K 1% 1/16W MF 402

R344 10K 1% 1/16W MF 603

R316 15.8K 1% 1/16W MF 402

R233 2.61K 1% 1/16W MF 402

D22 1N914 SOT23

ITH 1625 — IBATT_FB — IBATT_SERVO — IBATTX0_65 — ICHRG_REG

CRITICAL J14 SM-2MT

TO BACKUP BATTERY <-
FROM BACKUP BATTERY ->

BBATT_ENABLE

ADAPTER CURRENT LIMIT

-> FROM ADAPTER

INPUT14_24V_SW — R261 0.05 1% 1W MF 2512 — PWRBUS_14_24V

3V_PMU_CHGR — C199 0.1uF 20% 25V CERM 805

R300 24.9K 0.1% 1/16W MF 603

IAC_RC_COMP — C330 0.1uF 20% 16V CERM 603

IAC_FB — R351 1K 1% 1/16W MF 603

IINX0_62 — R343 100K 1% 1/16W MF 603

1_02V_AUX — R263 32.4K 0.1% 1/16W FF 603 — R283 14.3K 0.1% 1/16W FF 603

U24 MAX4172 SOI: V+, RS+, RS-, NC1, PG, NC2, OUT, GND

C162 0.01uF 20% 50V CERM 603

R262 1.1K 1% 1/16W MF 603

+ADAPTER_SW — CURRENT_ADJ — D18 1N5248B SOT23 — ZENER_GTR_THAN_18V

Q20 2N7002 SM

R299 3.3K 5% 1/16W MF 402

ADJUSTS CURRENT LIMIT
FOR 15V AIRLINE ADAPTER
VS. 24V WALL ADAPTER

D21 1N914 SOT23 — ADAPTER_I_REG

KEEP VIN/TK LOOP SHORT

CONNECT LTC1625 TK PIN AT TOP-SIDE FET

R46 1 5% 1/16W MF 603

R80 150 1% 1/16W MF 603

R81 4.99K 1% 1/16W MF 603

C43 0.1uF 20% 50V CERM 805

C59 4700pF 5% 25V CERM 603

C60 470pF 10% 50V CERM 603

C61 4700pF 5% 25V CERM 603

COMP_RC

U9 LTC1625: EXTVCC, VIN, SSOP, BG, TK, TG, SYNC, VOSENSE, RUN/SS, INTVCC, ITH, FCB, BOOST, VPROG, SW, SGND, PGND

1625_VIN — RUN/SS — 1625_COMP — 1625_SGND

1625_INTVCC — 1625_TG — 1625_BST — 1625_BG — 1625_VFB

D5 MBR0540 SM

C28 0.33uF 20% 16V CERM 805

C44 4.7uF 20% 10V TANT SMB

R71 0 5% 1/16W MF 603

Q4 SI4410DY SOI CRITICAL

Q6 SI4410DY SOI CRITICAL

C4 100uF 20% 35V ELEC SM-1

C132 1.5uF 20% 50V CERM 1812

C131 1.5uF 20% 50V CERM 1812

C130 1.5uF 20% 50V CERM 1812

C133 1.5uF 20% 50V CERM 1812

C155 1.5uF 20% 50V CERM 1812

C158 1.5uF 20% 50V CERM 1812

C157 1.5uF 20% 50V CERM 1812

C156 1.5uF 20% 50V CERM 1812

L5 15uH SM-2

CHGR_VSW — CHGR_OUT

D3 MBRS140T3 SM

CRITICAL C17 4.7uF 20% 25V CERM 1210

CRITICAL C10 4.7uF 20% 25V CERM 1210

C3 100uF 20% 35V ELEC SM-1

Q027 SI4435DY SOI

D4 D3 D2 D1 S3 S2 S1 GATE

R323 470K 5% 1/16W MF 402

BF_FET_G — R324 330K 5% 1/16W MF 402

C243 0.01uF 20% 16V CERM 402

FET_DRAIN — Q21 2N7002 SM

R284 330K 5% 1/16W MF 402

D17 1N914 SOT23 — GTR_THAN_13_0V

PWR_STABLE_DELAY

C200 0.047uF 5% 16V CERM 603

R331 49.3K 0.1% 1/16W FF 603

PBUS_DIV1

R342 100K 1% 1/16W MF 805

R381 11.3K 0.1% 1/16W MF 805

VCHRG — Q26 2N7002 SM — PMU_CHARGE_V

R341 150 1% 1/16W MF 603

PRIMARY REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A

SCALE	SHT	OF
NONE	31	41

POWER MANAGEMENT SUPPLY

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	State
0	0	1	Run
X	1	1	Sleep
1	0	0	Shutdown

ROUTE AS PAIR SHORT TRACE

NOTE: Place Rsense RC filter (R561/C646) close to MAX785 pins

ROUTE AS PAIR SHORT TRACE

+5V_SLEEP LOADS

1) Fan - High speed supply
2) Headphone amplifier
3) Modem - call progress ADC
4) DVD ROM
5) CardSlot - 5V tolerance
6) Trackpad

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C303	

SLEEP LEVEL SHIFTER (3V -> 5V)

+3V_SLEEP LOADS

1) CPU PLL Config Control
2) Fan - Low speed supply
3) KeyLargo - IIC Pull-ups & Oscillator
4) CardBus - Card detect pull-ups
5) Mobility Radeon - Oscillator
6) C5005 - Core, I/O
7) IRDA - VCC, LEDA, FIR_SEL pull-up
8) LVDS DDC Pull-ups
9) VGA MonID Level Shifters & Pull-ups
10) CardSlot
11) PMU - IIC Pull-ups

BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY

PROVIDES PATH TO +3V_PMU FROM BACKUP BATTERY WHEN PRESENT

SUPERCAP CHARGER

SUPERCAP

3.3V/5V SUPPLIES

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.

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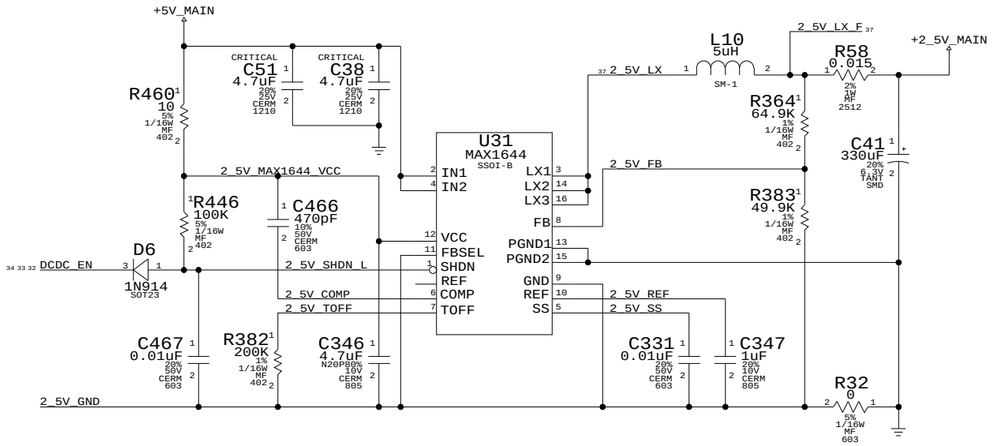
D	051-6223	A
SCALE: NONE	SHT 32 OF 41	

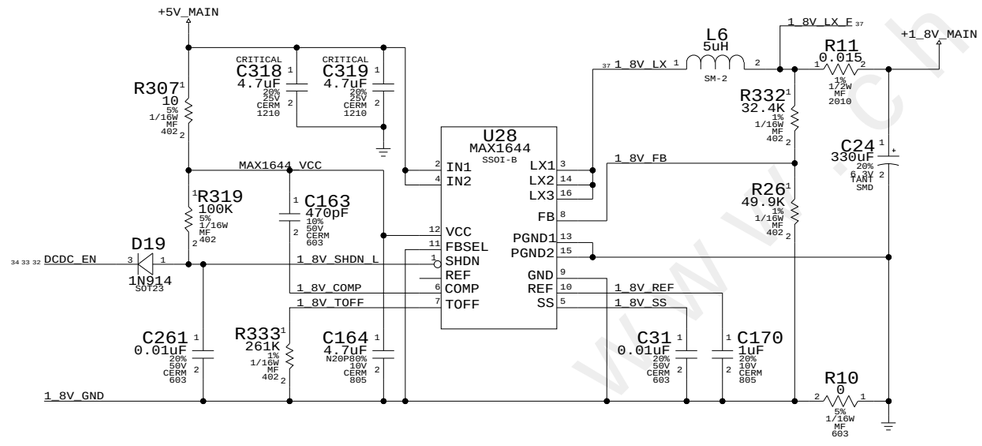
2.5V SWITCHER



+2_5V_MAIN LOADS

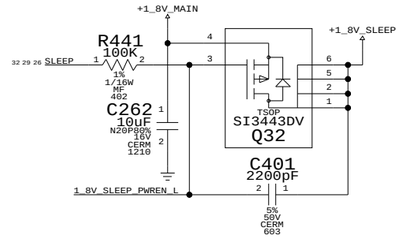
1) Mobility Radeon - AVDDs and DDR I/O
2) Gigabit Ethernet - AVDDL

1.8V SWITCHER



+1_8V_MAIN LOADS

1) Uni-N - Core, PLL DVDDs, MaxBus I/O
2) Mobility Radeon - Core, AVDDs
3) Gigabit Ethernet - DVDDH
4) +1_8V_SLEEP loads ->



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0305	138S0321		C262	

+1_8V_SLEEP LOADS

1) MPC7450 - MaxBus I/O, L3 I/O
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) C5005 VDDCPU0

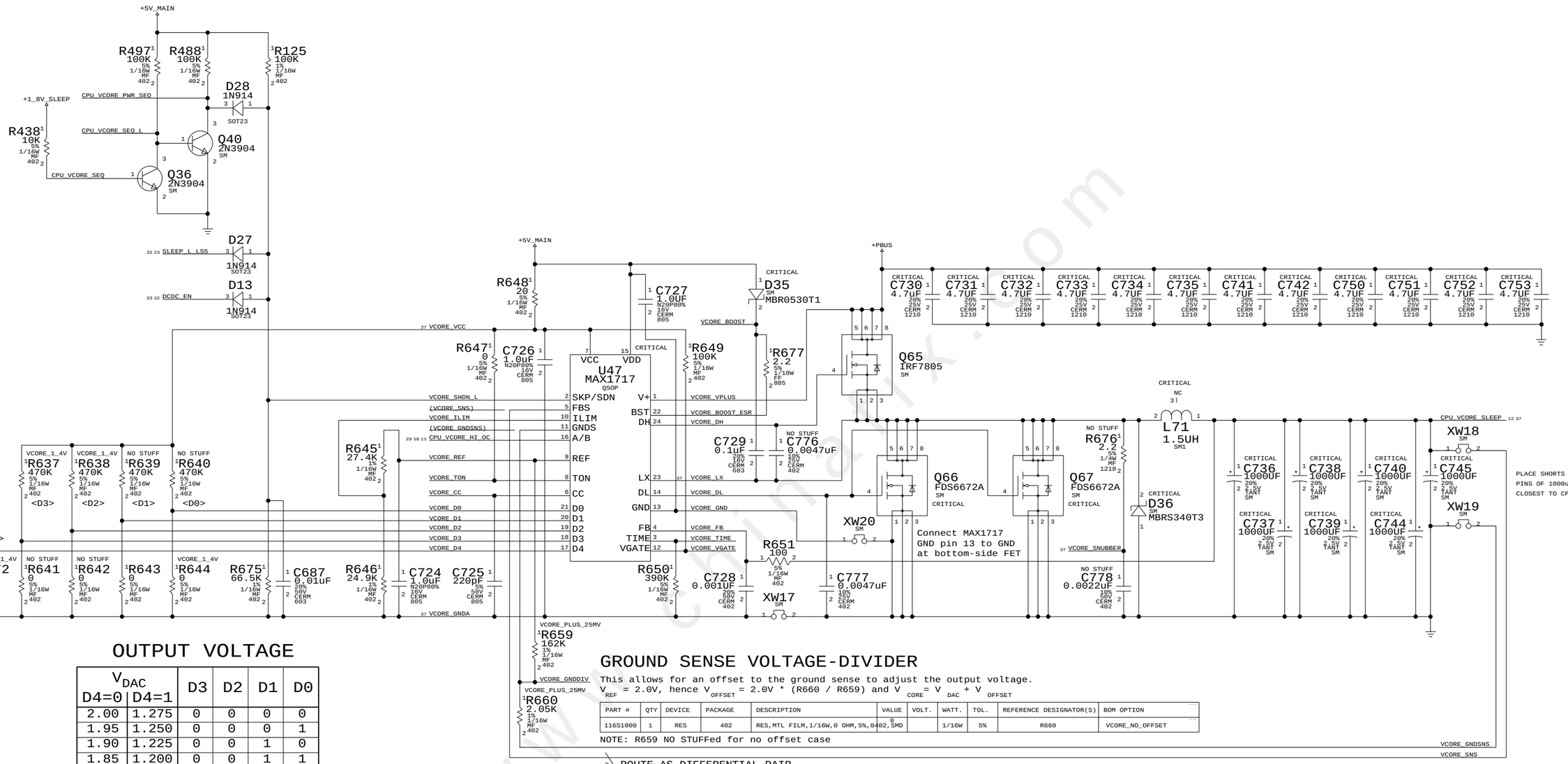
1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 33 OF 41	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)



ROUTE AS DIFFERENTIAL PAIR

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

GROUND SENSE VOLTAGE-DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
V_{REF} = 2.0V, hence V_{OFFSET} = 2.0V * (R660 / R659) and V_{CORE} = V_{DAC} + V_{OFFSET}

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1000	1	RES	402	RES,MTL FILM,1/16W,0 OHM,5%,0402,SMD	0		1/16W	5%	R660	VCORE_NO_OFFSET

NOTE: R659 NO STUFFed for no offset case

FOR V-STEP:

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1000	2	RES	402	RESISTOR	0		1/16W	5%	R637,R638	VCORE_1_4V_1_25V
116S1475	2	RES	402	RESISTOR	470K		1/16W	5%	R644,R672	VCORE_1_4V_1_25V

VCORE SUPPLY

APPLE COMPUTER INC.

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D	051-6223	A
SCALE: NONE	SHT 34 OF 41	

DIGITAL SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MIN_DAISY_CHAIN	
MAXBUS	CPU_ADDR<31..0>	::800:3300	6	500	200	4 MIL SPACING	TRUE	133MHZ		5 12
	CPU_DATA<62..0>	::800:3300	6	500	200	4 MIL SPACING	TRUE	133MHZ		5 13
	CPU_DATA<63>	::800:3300	6	500	200	4 MIL SPACING		133MHZ		5 11 13
	CPU_BG_L	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_DBG_L	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_TT<4..0>	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_TBST_L						TRUE			5 12
	CPU_TSIZ<2..0>						TRUE			5 12
	CPU_GBL_L	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_WT_L	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_CI_L	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_AACK_L	::800:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_DTI<2..0>	::300:3300	6	500	200	4 MIL SPACING	TRUE			5 12
	CPU_QACK_L						TRUE			5 12
	CPU_TS_L	U14.AD15:U15.P5:800:3300	6	500	200	4 MIL SPACING				5 12
	CPU_TA_L	U14.AE18:U15.N8:800:3300	6	500	200	4 MIL SPACING				5 12
	CPU_ARTRY_L	U14.AJ12:U15.T2:800:3300	6	500	200	4 MIL SPACING				5 12
	CPU_TEA_L	U14.AE17:U15.T1:800:3300	6	500	200	4 MIL SPACING				5 12
MAIN MEMORY	MEM_DATA<63..0>	::2400:5050	6	500	200	4 MIL SPACING		133MHZ		6
	RAD<12..0>	:::1350		500		4 MIL SPACING		133MHZ		6
	FMA_AR<12..0>	::2200:4000	6	500	200	4 MIL SPACING				6
	BA_0	::1300:1800		500		4 MIL SPACING				6
	FBA_0	::2000:3100	6	500	200	4 MIL SPACING				6
	BA_1	::1300:1800		500		4 MIL SPACING				6
	FBA_1	::2000:3100	6	500	200	4 MIL SPACING				6
	RAS_CS0_L	:::1197		500		4 MIL SPACING				6
	FRAS_CS0_L	::2000:4000	6	500	200	4 MIL SPACING				6
	RAS_CS1_L	:::749		500		4 MIL SPACING				6
	FRAS_CS1_L	::2000:4000	6	500	200	4 MIL SPACING				6
	RAS_CS2_L	:::600		500		4 MIL SPACING				6
	FRAS_CS2_L	::2000:4000	6	500	200	4 MIL SPACING				6
	RAS_CS3_L	:::600		500		4 MIL SPACING				6
	FRAS_CS3_L	::2000:4000	6	500	200	4 MIL SPACING				6
	CAS_DQM0_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM0_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM1_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM1_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM2_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM2_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM3_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM3_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM4_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM4_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM5_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM5_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM6_L	:::1000		500		4 MIL SPACING				6
	FCAS_DQM6_L	::2000:5000	6	500	200	4 MIL SPACING				6
	CAS_DQM7_L	:::1122		500		4 MIL SPACING				6
	FCAS_DQM7_L	::2000:4500	6	500	200	4 MIL SPACING				6
	SDRAS_L	:::1000		500	200	4 MIL SPACING				6
	FSDRAS_L	::1900:4000	6	500	200	4 MIL SPACING				6
	SDCAS_L	:::1000		500	200	4 MIL SPACING				6
	FSDCAS_L	::2000:4000	6	500	200	4 MIL SPACING				6
	MEMWE_L	:::1000		500	200	4 MIL SPACING				6
	FMEMWE_L	::2000:4000	6	500	200	4 MIL SPACING				6
	RAM_CKE0	:::600		500	200	4 MIL SPACING				6
	FRAM_CKE1_A	::2000:4000	6	500	200	4 MIL SPACING				6
	RAM_CKE1	:::600		500	200	4 MIL SPACING				6
	FRAM_CKE0_A	::2000:4000	6	500	200	4 MIL SPACING				6
	RAM_CKE2	:::650		500	200	4 MIL SPACING				6
	FRAM_CKE1_B	::2000:4000	6	500	200	4 MIL SPACING				6
	RAM_CKE3	:::600		500	200	4 MIL SPACING				6
	FRAM_CKE0_B	::2000:4000	6	500	200	4 MIL SPACING				6
	MEM_EXT_R	:::500								6
AGP BYTES 0-1	AGP_AD<15..0>	::850:1350	4	500	100	4 MIL SPACING		66MHZ		7 16
	AGP_CBE<1..0>	::1100:1600	4	500	100	4 MIL SPACING		66MHZ		7 16
	AGP_AD_STB<0>	U4.F25:U14.F16:1250:1500	6	500	90	8 MIL SPACING		66MHZ		7 16
	AGP_AD_STB_L<0>	U4.F24:U14.F15:1250:1500	6	500	90	8 MIL SPACING		66MHZ		7 16
AGP BYTES 2-3	AGP_AD<31..16>	::855:1355	4	500	100	4 MIL SPACING		66MHZ		7 16
	AGP_CBE<3..2>	::900:1400	4	500	100	4 MIL SPACING		66MHZ		7 16
	AGP_AD_STB<1>	U4.P25:U14.F12:1350:1600	6	500	90	8 MIL SPACING		66MHZ		7 16
	AGP_AD_STB_L<1>	U4.N24:U14.F12:1350:1600	6	500	90	8 MIL SPACING		66MHZ		7 16
AGP SIDEBAND	AGP_SBA<7..0>	::900:1400	4	500	100	4 MIL SPACING		66MHZ		7 16
	AGP_SB_STB	U4.V25:U14.F9:1500:1750	6	500	90	8 MIL SPACING		66MHZ		7 16
	AGP_SB_STB_L	U4.U25:U14.G9:1500:1750	6	500	90	8 MIL SPACING		66MHZ		7 16
AGP CONTROL	AGP_FRAME_L	U4.K25:U14.B15:900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_IRDY_L	U4.K26:U14.A14:850:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_TRDY_L	U4.K24:U14.C14:900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_DEVSEL_L	U4.J26:U14.B7:900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_STOP_L	U4.J24:U14.E13:900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_PAR	::900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_REQ_L	U4.AA25:U14.C4:900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_GNT_L	U4.Y24:U14.E9:900:1400	6	500	490	4 MIL SPACING		66MHZ		7 16
	AGP_RBF_L	U4.W26:U14.E6:900:1450	6	500	490	4 MIL SPACING		66MHZ		7 16
PCI	PCI_AD<31..0>	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15 19
	PCI_CBE<3..0>	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15
	PCI_FRAME_L	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15
	PCI_IRDY_L	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15
	PCI_TRDY_L	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15
	PCI_DEVSEL_L	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15
	PCI_STOP_L	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15
	PCI_PAR	::3500:6900		1000		4 MIL SPACING		33MHZ	MIN_DAISY_CHAIN	8 14 15

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	DELAY_RULE	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
CLOCK CKT (C5005)	SYSCLK_CPU_UF	:::150					133MHZ	18
	SYSCLK_CPU	::4400:4500	3	250	200	10 MIL SPACING	133MHZ	12 18
	SYSCLK_UNIN_UF	:::150					133MHZ	18
	SYSCLK_UNIN	::1500:1650	3	250	200	10 MIL SPACING	133MHZ	6 18
	SYSCLK_UNIN_RDCLK_UF	:::150					133MHZ	18
	SYSCLK_UNIN_RDCLK	::6400:6500	3	250	200	10 MIL SPACING	133MHZ	6 18
	SYSCLK_DIMM0_A_UF	:::150					133MHZ	18
	SYSCLK_DIMM0_A	::4500:4600	3	250	200	10 MIL SPACING	133MHZ	6 18
	SYSCLK_DIMM0_B_UF	:::225					133MHZ	18
	SYSCLK_DIMM0_B	::4500:4600	3	250	200	10 MIL SPACING	133MHZ	6 18
	SYSCLK_DIMM1_A_UF	:::150					133MHZ	18
	SYSCLK_DIMM1_A	::4500:4600	3	250	200	10 MIL SPACING	133MHZ	6 18
	SYSCLK_DIMM1_B_UF	:::207					133MHZ	18
	SYSCLK_DIMM1_B	::4500:4600	3	250	200	10 MIL SPACING	133MHZ	6 18
	CLK66M_UNIN_AGP_UF	:::200		250	200		66MHZ	18
	CLK66M_UNIN_AGP	::2250:2750	4	250	200	10 MIL SPACING	66MHZ	7 18
	CLK66M_AGP_UF	:::210		250	200		66MHZ	18
	CLK66M_AGP_ATI	::1800:2300	4	250	200	10 MIL SPACING	66MHZ	16 18
	CLK66M_UNIN_PCI_INT_UF	:::200		250	200		66MHZ	18
	CLK66M_UNIN_PCI_INT	::2250:2750	4	250	200	10 MIL SPACING	66MHZ	8 18
	CLK33M_UNIN_PCI_EXT_UF	:::200		250	200		33MHZ	18
	CLK33M_UNIN_PCI_EXT	::2300:2800	4	250	200	10 MIL SPACING	33MHZ	8 18
	CLK33M_KL_UF	:::200		250	200		33MHZ	18
	CLK33M_KL_PCI	::1600:2100	4	250	200	10 MIL SPACING	33MHZ	14 18
	CLK33M_CBUS_UF	:::200		250	200		33MHZ	18
	CLK33M_CBUS	::500:1000	4	250	200	10 MIL SPACING	33MHZ	15 18
	CLK14M_IMI_XIN	::300:636						18
	CLK14M_IMI_XOUT	::300:636						18
MOBILITY RADEON	ATI_CLK0	::50:200						16
	ATI_CLK0_L	::50:207						16
	ATI_CLK1	::50:200						16
	ATI_CLK1_L	::50:200						16
	ATI_CLK0_IN	::50:200						16
	ATI_CLK0_L_IN	::50:200						16
	ATI_CLK1_IN	::50:200						16
	ATI_CLK1_L_IN	::50:200						16
ETHERNET	CLKENET_PHY_RX	:::200						23
	CLK_ENET_LINK_RX	::4200:5400						9 23
	CLKENET_PHY_TX	:::200						23
	CLK_ENET_LINK_TX	::5000:5500						9 23
	ENET_GTX_CLK	:::200						9
	ENET_PHY_GTX_CLK	::5000:5500						9 23
	ENET_PHY_GBE_REFCLK	:::327						23
	ENET_GBE_REFCLK	::4900:5400						9 23
FIREWIRE	CLK_PHY_FW	:::200						24
	CLK_UNIN_FW	::6100:6600						9 24

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

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D	051-6223	A
SCALE: NONE	SHT 35 OF 41	

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
	EIDE_DATA<15..0>	::300:777					TRUE	33MHZ 14 27
	EIDE_ADDR<2..0>	::300:700						33MHZ 14 27
	EIDE_CS1FX_L	::300:700						33MHZ 14 27
	EIDE_CS3FX_L	::300:700						33MHZ 14 27
	EIDE0_RD_L	::300:700						33MHZ 14 27
EIDE / KEYLARGO	EIDE0_WR_L	::300:700						33MHZ 14 27
	EIDE_IOCHRDY	::300:700						33MHZ 14 27
	EIDE0_INT	::200:500						33MHZ 14 27
	EIDE0_DMACK_L	::200:500						33MHZ 14 27
	EIDE0_DMARQ	::200:500						33MHZ 14 27
	KL_CSLOT_IORD_L	::300:700						33MHZ 14
	KL_CSLOT_IOWR_L	::300:700						33MHZ 14
	CSLOT_DATA<15..0>	::3000:5600						33MHZ 27
	CSLOT_ADDR<2..0>	::3200:5300						33MHZ 27
	CSLOT_CS1FX_L	::3300:5400						33MHZ 27
EIDE / CARDSLOT	CSLOT_CS3FX_L	::3300:5400						33MHZ 27
	CSLOT_IORD_L	::3300:4900						33MHZ 14 27
	CSLOT_IOWR_L	::3300:4904						33MHZ 14 27
	CSLOT_ADDR<15>	U44.D3:J25.20:3300:5600						33MHZ 14 27
	CSLOT_ADDR<14>	U44.C7:J25.14:3300:5600						33MHZ 14 27
CARDSLOT	CSLOT_ADDR<13>	U44.A6:J25.13:3300:5600						33MHZ 14 27
	CSLOT_ADDR<12..3>	::3300:5600						33MHZ 14 27
	CSLOT_CE1_L	::3300:5400						33MHZ 14 27
	CSLOT_CE2_L	::3300:5400						33MHZ 14 27
	CSLOT_IRQ_L	U44.U20:J25.16:3300:5600						33MHZ 14 27
	CSLOT_IOWAIT_L	U44.T17:J25.46:2608:5600						33MHZ 14 27
	CSLOT_REG_L	U44.T18:J25.44:2914:5600						33MHZ 14 27
	EIDE_DB_<15..0>	::5200:6800						33MHZ 27
	EIDE_ADDR_<2..0>	::5200:6800						33MHZ 27
	EIDE_CS1FX*	::5200:6800						33MHZ 27
	EIDE_CS3FX*	::5200:6800						33MHZ 27
	EIDE0_READ_L	::5200:6800						33MHZ 27
EIDE / DVD	EIDE0_WR*	::5200:6800						33MHZ 27
	EIDE_IO_CHRDY	::5200:6800						33MHZ 27
	EIDE0_INTR	::5200:6800						33MHZ 27
	EIDE0_DMA_ACK_L	::5200:6800						33MHZ 27
	EIDE0_DMA_RQ	::5200:6800						33MHZ 27
	UIDE_DATA<15..13>	::1000:1800	6	500	200	4 MIL SPACING	TRUE	66MHZ 14 27
	UIDE_DATA<12>	::1000:1800	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DATA<11..9>	::1000:1800	6	500	200	4 MIL SPACING	TRUE	66MHZ 14 27
	UIDE_DATA<8>	::1000:1800	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DATA<7>	U44.C10:RP36.4:1000:1800	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DATA<6..1>	::1000:1800	6	500	200	4 MIL SPACING	TRUE	66MHZ 14 27
	UIDE_DATA<0>	::1000:1800	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_ADDR<2..0>	::1000:2602	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_RST_L	::1000:1800	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DIOW_L	::1000:2012	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DIOR_L	::1000:2096	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DMACK_L	::1000:1936	6	500	200	4 MIL SPACING		66MHZ 14 27
ULTRA ATA/66	UIDE_CS1FX_L	::1000:2703	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_CS3FX_L	::1000:2441	6	500	200	4 MIL SPACING		66MHZ 14 27
	UIDE_DMARQ	::300:500	6	500	200	4 MIL SPACING		66MHZ 14
	UIDE_IOCHRDY	U44.D10:R610.1:300:500	6	500	200	4 MIL SPACING		66MHZ 14
	UIDE_INTRQ	::300:500	6	500	200	4 MIL SPACING		66MHZ 14
	HD_DATA<15..0>	::300:506				4 MIL SPACING		66MHZ 27
	HD_ADDR<2..0>	::300:500				4 MIL SPACING		66MHZ 27
	HD_RESET_L					4 MIL SPACING		66MHZ 27
	HD_DIOW_L	::300:500				4 MIL SPACING		66MHZ 27
	HD_DIOR_L	::300:500				4 MIL SPACING		66MHZ 27
	HD_DMACK_L	R623.2:J26.8:300:500				4 MIL SPACING		66MHZ 27
	HD_CS1_L	::300:500				4 MIL SPACING		66MHZ 27
	HD_CS3_L	::300:500				4 MIL SPACING		66MHZ 27
	HD_DMARQ	R166.2:J26.12:1000:2000				4 MIL SPACING		66MHZ 14 27
	HD_IOCHRDY	R610.2:J26.9:1000:2150				4 MIL SPACING		66MHZ 14 27
	HD_INTRQ	R165.2:J26.7:1000:2147				4 MIL SPACING		66MHZ 14 27
	ENET_RXD<7..0>	::4000:5682						9 23
	ENET_TX_D<7..0>	::::671						9
	ENET_PHY_TXD<7..0>	::4700:5400	6					9 23
	ENET_TX_EN	::::500						9
ETHERNET MII	ENET_PHY_TX_EN	::4700:5300	6					9 23
	ENET_TX_ER	::::500						9
	ENET_PHY_TX_ER	::4700:5300	6					9 23
	ENET_MDIO	U14.V28:U12.D9:4500:5100	6					9 23
	ENET_MDC	::4500:5100	6					9 23
	FW_LINK_DATA<7..0>	::3500:4100	6	500				9 24
	FW_PHY_DATA<7..0>	::1850:3008						24
FIREWIRE MII	FW_LINK_CNTL<1..0>	::3400:4100		500				9 24
	FW_PHY_CNTL<1..0>	::1900:2200						24
	FW_LINK_LREQ	::200:319						9 24
	FW_PHY_LREQ	::5100:6600		500				24

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MIN_LINE_WIDTH	STUB_LENGTH	MAX_EXPOSED_LENGTH
	MDI_P<0>	ENET_TRD0	ENET_TRD0:U12.N1:T1.12:100	5	150	500 23
	MDI_M<0>	ENET_TRD0	ENET_TRD0:U12.N2:T1.11:100	5	150	500 23
	RJ45_DP<0>	RJ45_DP0	RJ45_DP0:T1.13:J2.1:100	5	150	23
	RJ45_DN<0>	RJ45_DP0	RJ45_DP0:T1.14:J2.2:100	5	150	23
	MDI_P<1>	ENET_TRD1	ENET_TRD1:U12.N3:T1.9:100	5	150	500 23
	MDI_M<1>	ENET_TRD1	ENET_TRD1:U12.N4:T1.8:100	5	150	500 23
	RJ45_DP<1>	RJ45_DP1	RJ45_DP1:T1.16:J2.3:100	5	150	23
	RJ45_DN<1>	RJ45_DP1	RJ45_DP1:T1.17:J2.6:100	5	150	23
ETHERNET	MDI_P<2>	ENET_TRD2	ENET_TRD2:U12.N6:T1.6:100	5	150	500 23
	MDI_M<2>	ENET_TRD2	ENET_TRD2:U12.N7:T1.5:100	5	150	500 23
	RJ45_DP<2>	RJ45_DP2	RJ45_DP2:T1.19:J2.4:100	5	150	23
	RJ45_DN<2>	RJ45_DP2	RJ45_DP2:T1.20:J2.5:100	5	150	23
	MDI_P<3>	ENET_TRD3	ENET_TRD3:U12.N8:T1.3:100	5	150	500 23
	MDI_M<3>	ENET_TRD3	ENET_TRD3:U12.N9:T1.2:100	5	150	500 23
	RJ45_DP<3>	RJ45_DP3	RJ45_DP3:T1.22:J2.7:100	5	150	23
	RJ45_DN<3>	RJ45_DP3	RJ45_DP3:T1.23:J2.8:100	5	150	23
	FW_TPA0N	FW_TPA0	FW_TP0_PHY:::4%		0	500 24
	FW_TPA0P	FW_TPA0	FW_TP0_PHY:::4%		0	500 24
	FW_TPB0N	FW_TPB0	FW_TP0_PHY:::4%		0	500 24
FIREWIRE	FW_TPB0P	FW_TPB0	FW_TP0_PHY:::4%		0	500 24
	FW_TPI1N	FW_TPI1	FW_TP1_PORT:::4%		0	24
	FW_TPI1P	FW_TPI1	FW_TP1_PORT:::4%		0	24
	FW_TPO1N	FW_TPO1	FW_TP1_PORT:::4%		0	24
	FW_TPO1P	FW_TPO1	FW_TP1_PORT:::4%		0	24
	CLKLVDS_N	CLKLVDS	LVDS:::100			16 26
	CLKLVDS_P	CLKLVDS	LVDS:::100			16 26
	LVDS_L0N	LVDS_L0	LVDS:::100			16 26
LVDS	LVDS_L0P	LVDS_L0	LVDS:::100			16 26
	LVDS_L1N	LVDS_L1	LVDS:::100			16 26
	LVDS_L1P	LVDS_L1	LVDS:::100			16 26
	LVDS_L2N	LVDS_L2	LVDS:::100			16 26
	LVDS_L2P	LVDS_L2	LVDS:::100			16 26
	USB_DAM	USB_DA	USB_DA:::200			14 25
	USB_DAP	USB_DA	USB_DA:::200			14 25
	USB_DBM	USB_DB	USB_DB:::200			14
	USB_DBP	USB_DB	USB_DB:::200			14
	USB_DCM	USB_DC	USB_DC:::200			14 25
	USB_DCP	USB_DC	USB_DC:::200			14 25
	USB_DDM	USB_DD	USB_DD:::200			14
	USB_DDP	USB_DD	USB_DD:::200			14
	BT_USB_DM	BT_USB_D	BT_USB:::200			14 25
	BT_USB_DP	BT_USB_D	BT_USB:::200			14 25
USB	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:::200			14 27
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:::200			14 27
	USB_D1M	USB_D1	USB_D1:R269.2:L37.1:200			25
	USB_D1P	USB_D1	USB_D1:R277.2:L38.1:200			25
	USB_D1M_EMI	USB_D1_EMI	USB_D1_EMI:L37.2:J4.2:200			25
	USB_D1P_EMI	USB_D1_EMI	USB_D1_EMI:L38.2:J4.3:200			25
	USB_D2M	USB_D2	USB_D2:R221.2:L29.1:200			25
	USB_D2P	USB_D2	USB_D2:R222.2:L30.1:200			25
	USB_D2M_EMI	USB_D2_EMI	USB_D2_EMI:L29.2:J5.2:200			25
	USB_D2P_EMI	USB_D2_EMI	USB_D2_EMI:L30.2:J5.3:200			25

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 36 OF 41	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	/+PBUS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	/+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	/+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER/ BATTERY	+ADAPTER_UF	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	28 30 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31
	INPUT14_24V_SW	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 31
	PWRBUS_14_24V	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	CHGR_VSW	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	CHGR_OUT	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	BATT_FET_SW	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	BATT_ISNS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	BATT_LINE	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 31
	BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	BATT_POS_F	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 32
	BATT_RES	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	1625_INTVCC	VOLTAGE=5.3V	MIN_LINE_WIDTH=10		31
	3V_PMU_CHGR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		30 31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	ADAPTER_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
BACKUP	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+BBATT_BYPASS	VOLTAGE=16.8V	MIN_LINE_WIDTH=10		32
	+5_5V_RAW	VOLTAGE=5.5V	MIN_LINE_WIDTH=10		32
	+5_5V_BU	VOLTAGE=5.5V	MIN_LINE_WIDTH=10		32
	+SUPERCAP	VOLTAGE=5.5V	MIN_LINE_WIDTH=10		32
POWER SUPPLIES	PS_VL	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		34
	PS_LX_5V	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	PS_LX_3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	PS_CS_3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	1_8V_LX	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	1_8V_LX_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_SNUBBER	VOLTAGE=1.4V	MIN_LINE_WIDTH=10		34
	VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		34
MISC	DC_PLUG_TIP	VOLTAGE=24V	MIN_LINE_WIDTH=10		28 30
	+PBUS_INV	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 32
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+5V_IO_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		28
	+5V_USB_PRE_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
	+5V_USB_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
	+5V_VGA_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	FAN_PWR_LOW	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		28
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	26
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		29
	TPAD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		28
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		26
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		26

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
UNIN	+3V_UNIN_MAXPLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	+3V_UNIN_AGPPLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	7
	+1_8V_UNIN_MAXPLL_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	+1_8V_UNIN_AGPPLL_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	7
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	12 34
	CPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12
KEY LARGO	+3V_KL_AVDD1_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+3V_KL_AVDD2_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+3V_KL_AVDD3_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+3V_KL_AVDD4_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+3V_KL_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+3V_KL_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+5V_KL	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	KL_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	15
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	15
MOBILITY RADEON	+VCORE_ATI_VDDM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	16
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	16
	+2_5V_ATI_VDDR	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16 17
	+2_5V_ATI_LVDDR	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	17
	+2_5V_ATI_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		17
	+1_8V_ATI_A2VDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	17
	+1_8V_ATI_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
	+1_8V_ATI_MPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	17
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	17
	+1_25V_ATI_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		16
IMI C5005	+3V_IMI_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	PLL_SDRAM_CPU1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	PLL_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
	PLL_VCC_CPU0	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
ETHERNET	+3V_ENET	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	ENET_AVDDH	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23
	+2_5V_ENET	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+1_8V_ENET	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	ENET_DVDDL	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
FW	+PBUS_FW_SW	VOLTAGE=16.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	24
	+FW_VP_FUSE	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	24
	+FW_VP_UF	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	24
	FW_VP	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	24
	+3V_FW_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
	FW_VGND	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	24
AUDIO	MIC_5V	VOLTAGE=5V	MIN_LINE_WIDTH=10		22
	MAX4298_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+AUD4V	VOLTAGE=4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20 22
	+AUD3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20
	FIL_AUD3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20
	FIL2_AUD3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20
	FIL_DIG3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20
	FIL2_DIG3V	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20
	DA_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20 21
	LINE_OUT_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	LINE_OUT_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	MUTE_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	MIC_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21 22
	SPKR_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	PWR3V_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20 21
	PWR4V_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20 21
	FIL_AUD_STAR	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20
	TI_AVSS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20

/GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
/CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
/CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
/CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
/CHGND4A	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4A
/CHGND4B	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4B
/CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
/CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
/CHGND7	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND7

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 37 OF 41	

REVISION HISTORY

03/14/2001

INITIAL RELEASE
03/15/2001 - Deleted +2_5V_SLEEP switch, no 2.5V switched devices left (was for L2)
03/15/2001 - Moved BootROM and Fan circuitry to formerly blank page 14
03/15/2001 - Modified VCore circuit to 1.5V/1.5V operation for bring-up
03/15/2001 - Minor net name changes
03/16/2001 - Updated to new board spacers
03/16/2001 - Connected fourth (unused) USB pair to IR connector
03/16/2001 - Moved page 14 to page 19, shifted other pages down
03/19/2001 - Moved 1.8V power supply input from 3V to 5V

03/19/2001

SECOND RELEASE (FOR DESIGN REVIEW)
03/19/2001 - Feedback from Design Review:
Moved CKEs to follow shifted CS signals on Uni-N
Added test points on CPU parity signals
Corrected mistakes in ATI pinout
Swapped one GPIO on ATI SS circuit
Grounded reserved TAS signals
Updated modem ACP circuit to latest iBook design
Added C for ethernet reset RC circuit
Moved 1.8V supply to +5V_MAIN
Wiring corrections to 1.8V and 2.5V supplies

03/28/2001

DESIGN FORKED FROM PROTO BOARD PRE-RENAME
CHANGES APPLIED FROM PROTO BOARD AFTER RENAME:
Moved AGP REQ/GNT pull-ups to +1_5V_MAIN
USB Soft Power-On circuit removed
Final cleanups for proto build release
03/28/2001 - Added 100MHz FSB option resistor
04/09/2001 - Changed AGP_TYPEDET pull-down from 1K to 0-ohm
04/09/2001 - Remove CPU SYSCLK pull-down
04/09/2001 - Remove +3V_KL plane cut
04/09/2001 - Correct inverter flex connector pinout
04/09/2001 - Break up IRDA/BT connector into two separate connectors
04/09/2001 - Add connector for backup battery
04/11/2001 - Add new board hole for IR/BT board carrier
04/11/2001 - Update +3V_PMU circuit for backup battery support
04/12/2001 - Update board slots to latest MCO
04/12/2001 - Board reference designator renumbering

04/13/2001 - 051-6103-02

PROTO SYSTEM BUILD RELEASE

04/30/2001 - Replaced VCore supply with MAX1717 circuit
05/04/2001 - Replaced CardBus controller with TI PCI1410A
05/04/2001 - Added workaround for 88E1011 rev 01 DVDDL issue
05/05/2001 - Audio subsystem updates to match latest architecture
05/09/2001 - Added ability to adjust Vcore using voltage divider
05/09/2001 - Added two more Vcore bulk caps for tighter regulation
05/10/2001 - Isolated MAX1717 GND to connect at bottom-side FET
05/18/2001 - Trying Hirose low-profile connector at IR location
05/18/2001 - Smaller package for LM4863 (Boomer) IC
05/18/2001 - Buffer added to inverter backlight PWM signal
05/18/2001 - Added bypass for headphone sense circuit, moved ground
05/18/2001 - Added ability to adjust bus speed during v-step
05/23/2001 - Removed ZH2 as it is now unplated hole for ICT
05/23/2001 - First pass at BOM consolidations

05/23/2001 - 051-6103-03

PROTO II BUILD RELEASE

06/11/2001 - Removed 88E1010 support from ethernet circuit
06/11/2001 - Hirose connector failed, back to Elco at IR location
06/11/2001 - Removed RJ11 shield in preparation for new RJ11 connector
06/11/2001 - All but one CardBus pullup no longer necessary
06/14/2001 - Merged CHGND3 and CHGND4B
06/14/2001 - Redesign of backlight PWM buffer for better performance
06/15/2001 - Adjusted some clock constraints for better timing
06/15/2001 - Changed +3VAUD input from +6V_AUDIO to +5V_MAIN
06/19/2001 - Changed +1_8V_MAIN power resistor to 2010 package
06/19/2001 - Length constraint tweaks for rev 04 release
06/19/2001 - C5005 terminator changes for rev B part

06/19/2001 - 051-6103-04

EVT BUILD RELEASE

07/13/2001 - Revised audio circuitry to remove +6V_AUDIO
07/13/2001 - Added pullups required on Uni-N 1.5 MAXBUS interface
07/13/2001 - FireWire PD signal tied to KeyLargo GPIO 12
07/16/2001 - Added series terminator on KeyLargo IrDA transmit line
07/16/2001 - FireWire PD signal moved to KeyLargo GPIO 0
07/16/2001 - Added VCore ILIM circuit to limit inrush
07/19/2001 - Added support to modify MAX1717 D4 signal
07/20/2001 - Added pulldown on IR RX line for P49 stuffing
07/20/2001 - Changed from 8x 10uF caps to 12x 4.7uF on VCore for MCO
07/27/2001 - Added series resistor to protect adapter shell clamp diode
07/30/2001 - Added 20x 10uF 0805 caps for CPU VCore droop stability
07/31/2001 - Added diode in sleep LED circuit for shutdown current
08/01/2001 - Numerous VCore power supply changes
08/06/2001 - Added low-pass filter on headphone amp
08/06/2001 - Called out correct BootROM part number
08/06/2001 - Modified sleep LED shutdown current fix
08/07/2001 - Called out correct PMU part number
08/07/2001 - Added 4 more 10uF 0805 caps on CPU VCore
08/10/2001 - VCore BOM changes (FETs & some discretes to adjust)

08/10/2001 - 051-6103-05

DVT BUILD RELEASE

08/22/2001 - Series resistor value tweaks on PCI clock lines
08/22/2001 - Moved 64-bit PCI pullups from +3V_MAIN to +3V_SLEEP (sleep current)
08/22/2001 - Replaced +1_8V_MAIN MAX1644 with MAX1623
08/23/2001 - Backed-out previous +1_8V_MAIN change
08/25/2001 - +1_8V_MAIN regulator changed to MAX1644B (3 Amp min. current limit)
08/25/2001 - ATI VDDC 0-ohm resistor removed to reduce voltage drop
08/29/2001 - Added cap on battery voltage comparator to reduce glitches
08/29/2001 - Changed +2_5V_MAIN ESR resistor to reduce voltage drop
08/29/2001 - Modified 88E1011 output series resistance (part has 50-ohm drivers)
08/31/2001 - BOM changes to PBUS input current limiter to slow response
08/31/2001 - BOM changes to adjust low-frequency roll-off of internal speakers
09/04/2001 - Description / notes updates for production release

09/04/2001 - 051-6103-A

PRODUCTION RELEASE

09/10/2001 - Corrected V'ger part descriptions
09/10/2001 - NO STUFFed 88E1011 1.8V -> 1.5V resistor at Marvell's request
09/10/2001 - BOM: ATI M6-D stuffed on both configs

RE-ARCHIVE TO PRODUCTION RELEASE RFA - 09/10/2001

09/17/2001 - BOM: NO STUFF BS1, will now be nylon spacer

RE-ARCHIVE TO PRODUCTION RELEASE RFA - 09/17/2001

10/02/2001 - BOM: Correct wrong BootROM Apple Part Number

RE-ARCHIVE TO PRODUCTION RELEASE RFA - 10/02/2001

11/14/2001 - 051-6223

11/14/2001 - BOM: Changed FlashROM to 341S0976 JMD

REVISION HISTORY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6223	A
SCALE: NONE	SHT 38 OF 41	

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      *** Signal Cross-Reference ***
         --- for the entire design --

+1_8V_ATI_A2VDDQ 17D6 37C3
+1_8V_ATI_AVDD  17D6 37C3
+1_8V_ATI_MPVDD 17A6 37C3
+1_8V_ATI_PVDD  17D7 37C3
+1_8V_ENET      23A6 23B2 23B8 37C3
+1_8V_UNIN_AGPPLL_MAIN 7D6 37D3
+1_8V_UNIN_MAXPLL_MAIN 5D5 37D3
+1_25V_ATI_VREF 16B6 37C3
+2_5V_ATI_A2VDD 17C5 37C3
+2_5V_ATI_LVDDR 17A6 37C3
+2_5V_ATI_VDDR  16B7 17B5 17D1 37C3
+2_5V_ENET      23A6 23D3 37C3
+3V_ATI_OSC_SLEEP 16B3 37C3
+3V_ATI_SS      16A3 37C3
+3V_ENET        23B5 23C5 23C6 37C3
+3V_FW_VDD      24D4 37B3
+3V_HALL_EFFECT 28D6 37B6
+3V_IMI_SLEEP   18C7 37C3
+3V_KL_AVDD1_SLEEP 14D3 37D3
+3V_KL_AVDD2_SLEEP 14D3 37D3
+3V_KL_AVDD3_SLEEP 14D3 37D3
+3V_KL_AVDD4_SLEEP 14D6 37D3
+3V_KL_OSC_SLEEP 14A5 37D3
+3V_KL_USB      14C1 37D3
+3V_LCD         26D1 37B6
+3V_LCD_SW      26D2 37B6
+3V_PMU_AVCC    29B6 29D5 37B6
+3V_PMU_ESR     32A3
+3V_UNIN_AGPPLL_MAIN 7D6 37D3
+3V_UNIN_MAXPLL_MAIN 5D5 37D3
+5V_HD_SLEEP    27D1 32D1 37B6
+5V_INV_SW      26C2 37B6
+5V_INV_UF_SW   26C2 37B6
+5V_IO_SLEEP    26B7 37B6
+5V_KL          14D4 37D3
+5V_RSNS        32D4 37C6
+5V_TOL         27B5
+5V_TPAD_SLEEP  28D7 37B6
+5V_USB_PRE_SW  25C7 37B6
+5V_USB_SW      25C6 37B6
+5V_VGA_SLEEP   26B6 37B6
+5_5V_BU        32A5 37C6
+5_5V_RAW       32A5 37C6
+ADAPTER        28B7 30D6 32A8 37D6
+ADAPTER_ILIM   32A7 37C6
+ADAPTER_OR_BATT 32A7 37C6
+ADAPTER_SW     30D4 31B8 37D6
+ADAPTER_UF     30D7 37D6
+AUD3V          20A3 20D5 20D8 37B3
+AUD4V          20B3 22C6 37B3
+BBATT_BYPASS   32A7 37C6
+FW_VP_FUSE     24C5 37C3
+FW_VP_UF       24D5 37B3
+PBUS_FW_SW     24D5 37C3
+PBUS_INV       26C2 37B6
+SUPERCAP       32A5 37C6
+VCC_CBUS_SW    15B1 15B3 15D1 15D3 37D3
+VCORE_ATI_VDDM 17B7 37C3
+VPP_CBUS_SW    15B1 15B3 15D3 37D3
/+1_5V_MAIN     37D6
/+1_8V_MAIN     37D6
/+1_8V_SLEEP    37D6
/+2_5V_MAIN     37D6
/+3V_MAIN       37D6
/+3V_PMU        37D6
/+3V_SLEEP      37D6
/+5V_MAIN       37D6
/+5V_SLEEP      37D6
/+PBUS          37D6
/CHGND1         37A6
/CHGND2         37A6
/CHGND3         37A6
/CHGND4A        37A6
/CHGND4B        37A6
/CHGND5         37A6
/CHGND6         37A6
/CHGND7         37A6
/GND            37A6
1V20_REF        30C4 30C6
1_02V_AUX       31B7
1_5V_AGP_ADJ    17B7
1_5V_AGP_BYP    17B8
1_8V_COMP       33A7
1_8V_FB         33B6
1_8V_GND        33A8
1_8V_LX         33B6 37B6
1_8V_LX_F       33B5 37B6
1_8V_REF        33A6
1_8V_SHDN_L     33A7
1_8V_SLEEP_PWREN_L 33B3
1_8V_SS         33A6
1_8V_TOFF       33A7
2_5V_COMP       33C7
2_5V_FB         33C6
2_5V_GND        33C8
2_5V_LX         33D6 37C6
2_5V_LX_F       33D5 37B6
2_5V_MAX1644_VCC 33C7
2_5V_REF        33C6
2_5V_SHDN_L     33C7
2_5V_SS         33C6
2_5V_TOFF       33C7
3V_PMU_CHGR     30C2 31C7 31D6 37C6
3V_PMU_SENSE    32A4
3V_PMU_VTAP     32B4
3V_SLEEP_PWREN_L 32B3
5V_HD_PWREN     32D2
5V_SLEEP_PWREN  32D2
13_5V_DET       30C4
1625_BG         31B4
1625_BST        31C4
1625_COMP       31C5
1625_INTVCC     31C4 37C6
1625_SGND       31B6 37C6
1625_TG         31C4
1625_VFB        31B4
1625_VIN        31C5 37D6
4863_BYPASS     21B7
4863_SHDN       21A7
ACOUT           21C2
AC_ENABLE_GATE  30D4
AC_ENABLE_L     30C4
AC_IN           23B7 29B3 30C5
ADAPTER_DET     29B3 29C2 30D6
ADAPTER_DET_UF  30D7
ADAPTER_GND     30D7 37C6
ADAPTER_I_REG   31B6
ADAPTER_PWR_SW  30A4
ADAPTER_RING    30D7
AGP_AD<31..0>   7B5 7C5 7D5 16C6 16D6 35A5 35B5
AGP_AD_STB<1..0> 7B5 7C2 16B6 35A5 35B5
AGP_AD_STB_L<1..0> 7B5 7C2 16B6 35A5 35B5
AGP_ATI_INT_L   14C4 16B6
AGP_ATI_RESET_L 16B6
AGP_BUSY_L_PU   16B6 16D7
AGP_CBE<3..0>   7B7 16C6 35A5 35B5
AGP_DEVSEL_L    7C7 7D2 16C6 35A5
AGP_FRAME_L     7C7 7D2 16C6 35A5
AGP_GNT_L       7B2 7C7 16B6 35A5
AGP_IRDY_L      7C7 7D2 16C6 35A5
AGP_PAR         7C7 16C6 35A5
AGP_PIPE_L_PU   7B7 7C2
AGP_RBF_L       7B7 7D2 16A6 35A5
AGP_REQ_L       7B2 7C7 16C6 35A5
AGP_SBA<7..0>   7B5 16A6 16B6 35A5
AGP_SB_STB      7B5 7C2 16A6 35A5
AGP_SB_STB_L    7B5 7C2 16A6 35A5
AGP_ST<2..0>    7B7 16B6
AGP_STOP_L      7C7 7D2 16C6 35A5
AGP_STP_L       16A6
AGP_SUS_STAT_L_PU 16B6 16D7
AGP_TRDY_L      7C7 7D2 16C6 35A5
AGP_U4RTAP      7A6
AGP_WBF_L_PU    7B7 7C2
AINLM           20C3 22C3
AINLP           20C3 22C3
AINRM           20C3 22B3
AINRP           20C3 22B3
AOUTL           20C2 21B8 21D7
AOUTL_BOOMER    21B7
AOUTL_FILTER    21D7
AOUTR           20C2 21A8 21D7
AOUTR_BOOMER    21A7
AOUTR_FILTER    21D7
ATI_AGP_FBSKEW<1..0> 16C2
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ATI_AGP_TEST    16B6 16D7
ATI_AGP_VREF    7B3 16B6
ATI_AGP_VREF_H  7C3
ATI_AGP_VREF_L  7B3
ATI_AUXWIN_PU   16B6 16D7
ATI_B           16D1 26A8
ATI_BUS_CFG<2..0> 16C2
ATI_B_FILTR     26A7
ATI_C           16C1 26D8
ATI_CLK0        16A5 35C1
ATI_CLK0_IN     16A5 35C1
ATI_CLK0_L      16A5 35C1
ATI_CLK0_L_IN   16A5 35C1
ATI_CLK1        16A5 35C1
ATI_CLK1_IN     16A5 35C1
ATI_CLK1_L      16A5 35C1
ATI_CLK1_L_IN   16A5 35C1
ATI_COMP        16C1 26C8
ATI_DIGON       16C1 26C4
ATI_DIGON_L     26C3
ATI_G           16D1 26A8
ATI_GPIO7       16A4 16C2
ATI_GPIO8_SPN   16C2
ATI_GPIO9       16A4 16C2
ATI_GPIO10      16A4 16C2
ATI_GPIO11_SPN  16C2
ATI_GPIO12_SPN  16C2
ATI_GPIO13_SPN  16C2
ATI_G_FLTR      26A7
ATI_HSYNC       16D1 16D3
ATI_HSYNC_BUF   16C4
ATI_INV_ON_L    16C1 26B3
ATI_LCDCNTL2_SPN 16C2
ATI_MEMVMODE    16A5 16D7
ATI_MONID<3..0> 16C1 26A3 26B3
ATI_MPVDD_BYP   17A6
ATI_OSC_OE      16B4
ATI_PVDD_BYP    17D7
ATI_R           16D1 26A8
ATI_R2SET       16D1 17C5
ATI_RSET        16D1 17D6
ATI_R_FILTR     26A7
ATI_SSIN        16A3 16B2
ATI_SSIN_UF     16A3
ATI_SSOUT       16A4 16B1
ATI_TESTEN      16B2 16C7
ATI_VSYNC       16D1 16D3
ATI_VSYNC_BUF   16D4
ATI_X1CLK_SKEW<1..0> 16C2
ATI_Y           16D1 26D8
AUD3V_FDBK      20A4
AUD4V_FDBK      20B4
AUDIO_OUT_L     21C2
AUDIO_OUT_R     21C2
BATT_CLK        30B7
BATT_DATA       30B7
BATT_ENABLE_L   30A4
BATT_FET_DRAIN  30A4
BATT_FET_GATE   30B4
BATT_FET_SW     30B4 37C6
BATT_IN_PD      30B7
BATT_ISNS       31D4 37C6
BATT_LINE       30B2 31D5 37C6
BATT_NEG        30B7 37C6
BATT_OK         30A6
BATT_OK_REF     30A6
BATT_POS        30B7 37C6
BATT_POS_F      30B6 32A8 37C6
BATT_RC         30A3
BATT_RES        30B5 37C6
BATT_V_GOOD     30A4
BA_0            6A5 6C6 35C5
BA_1            6A5 6C6 35C5
BBATT_ENABLE    31C2 32A8
BBATT_EN_L      32A7
BF_FET_G        31B2
BRIGHT_INV      26B2
BRIGHT_INV_BUF  26B3
BT_USB_DM       14C1 14D1 25B2 36B2
BT_USB_DP       14C1 14D1 25B2 36B2
BYPASS_R_GATE   30A4
BYPASS_R_L      30A4
CAPSLOCK_LED    28D2
CAPSLOCK_LED_L  28D2 29C7
CAS_DQM0_L      6C6 6D5 35C5
CAS_DQM1_L      6C6 6D5 35C5
CAS_DQM2_L      6C6 6D5 35C5
CAS_DQM3_L      6C6 6D5 35C5
CAS_DQM4_L      6C6 6D5 35C5
CAS_DQM5_L      6C6 6D5 35C5
CAS_DQM6_L      6C6 6D5 35B5
CAS_DQM7_L      6C6 6D5 35B5
CBUS_ADDR<25..0> 15A4 15B1 15B2 15B4 15C1 15C2 15D2
                16C2 16D2
CBUS_ADDR_16_UF 15B5
CBUS_BVD1_L     15B2 15C4 15D2
CBUS_BVD2_L     15B2 15C4 15D2
CBUS_CE1_L      15C1 15C4
CBUS_CE2_L      15C2 15C4
CBUS_DATA<15..0> 15A2 15A4 15B1 15B2 15C1 15C2
CBUS_DET_1_L    15C2 15C4 15D2
CBUS_DET_2_L    15A2 15C4 15D2
CBUS_INPACK_L   15B2 15C4 15D2
CBUS_INT_L      14B4 15A7
CBUS_IORD_L     15C2 15C4
CBUS_IOWR_L     15B2 15C4
CBUS_MFUNC1_PD  15A7 15D7
CBUS_MFUNC2_PD  15A7 15D7
CBUS_MFUNC3_PD  15A7 15C7
CBUS_MFUNC4_PD  15A7 15C7
CBUS_MFUNC5_PD  15A7 15C7
CBUS_MFUNC6_PD  15A7 15C7
CBUS_OE_L       15C1 15C4
CBUS_PCI_GNT_L  8C5 15A7
CBUS_PCI_IDSEL  15B7
CBUS_PCI_REQ_L  8C2 8D5 15A7
CBUS_PCI_RESET_L 15B7
CBUS_READY      15B1 15C4 15D2
CBUS_REG_L      15B2 15C4
CBUS_RESET_L    15B2 15C4
CBUS_SUSPEND_PU 15A7 15D7
CBUS_VCCD0_L    15C5
CBUS_VCCD1_L    15C5
CBUS_VPPD0      15C5
CBUS_VPPD1      15C5
CBUS_VS1        15C2 15C4 15D2
CBUS_VS2        15B2 15C4 15D2
CBUS_WAIT_L     15B2 15C4 15D2
CBUS_WE_L       15B1 15C4
CBUS_WP_L       15A1 15C2 15C4 15D2 16C2
CHARGE_LED_L    28B7 29C6 29D7
CHGR_OUT        31B2 37D6
CHGR_VSW        31B4 37D6
CHKSTP_OUT_L    12B3 12C2
CLK10M_PMU_XIN  29B6
CLK10M_PMU_XOUT 29B6
CLK10M_PMU_XOUT_UF 29B7
CLK14M_IMI_XIN  18C6 35C1
CLK14M_IMI_XOUT 18C6 35C1
CLK18M_KL_PLL   14B4
CLK18M_KL_UF    14A4
CLK24M_FW_XIN   24C6
CLK24M_FW_XOUT  24C6
CLK25M_ENET_XIN 23B6
CLK25M_ENET_XOUT 23B6
CLK27M_ATI      16B2
CLK27M_ATI_LS1_8 16B3
CLK27M_ATI_UF   16B3
CLK32K_PMU_XIN  29B3
CLK32K_PMU_XOUT 29B3
CLK32K_PMU_XOUT_UF 29B2
CLK33M_CBUS     15A7 18B2 35C1
CLK33M_CBUS_UF  18B4 35C1
CLK33M_KL_PCI   14A8 18B2 35C1
CLK33M_KL_UF    18B4 35C1
CLK33M_UNIN_PCI_EXT 8C5 18B2 35C1
CLK33M_UNIN_PCI_EXT_UF 18B4 35C1
CLK66M_AGP_ATI  16C6 18C2 35D1
CLK66M_AGP_UF   18B4 35D1
CLK66M_UNIN_AGP 7C7 18C2 35D1
CLK66M_UNIN_AGP_UF 18B4 35D1
CLK66M_UNIN_PCI_INT 8C5 18C2 35C1
CLK66M_UNIN_PCI_INT_UF 18B4 35D1
CLKENET_PHY_RX  23D8 35C1
CLKENET_PHY_TX  23D8 35C1
CLKLVDS_N       16B1 26C1 36C2
CLKLVDS_P       16B1 26C1 36C2
CLK_ENET_LINK_RX 9C6 23D8 35C1
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CLK_ENET_LINK_TX 9C6 23D8 35C1
CLK_PHY_FW      24B6 35B1
CLK_UNIN_FW     9B2 24B7 35B1
COMM_ANALOG_SND 27B2
COMM_ANALOG_SND_RET 27B2
COMM_DTR_L      14C2 27B1
COMM_GPIO_L     14C2 27B2
COMM_RESET_L    14C4 27B1
COMM_RING_DET_L 14C4 27B2 29C6
COMM_RTS_L      14C2 27B1
COMM_RXD        14C2 27B2
COMM_SHUTDOWN   14B8 27B2
COMM_TRXC       14C2 27B1
COMM_TXD_L      14C2 27B1
COMP_RC         31B6
CPU1_INT_L_PU   14B4 14C4
CPU1_SRESET_L_PU 14B4 14C4
CPU_AACK_L      5B7 5D2 12A6 35D5
CPU_ADDR<31..0> 5B7 5C7 12B6 12C6 35D5
CPU_ARTRY_L     5B7 5D2 12A6 35D5
CPU_AVDD        12D3 37D3
CPU_BG_L        5C2 5D7 12C6 35D5
CPU_BR_L        5D2 5D7 12C6
CPU_BUS_VSEL    11A6 12C3
CPU_CHKS_L      12B3 12D2
CPU_CI_L        5B7 12A6 35D5
CPU_CLKOUT_SPN  12C3
CPU_CLK_EN      18B6 18C4 29C4
CPU_DATA<63..0> 5A3 5B3 5C3 5D3 11A4 13A7 13B7 13C7
                13D7 35D5
CPU_DBG_L       5A3 5C2 12C3 35D5
CPU_DRDY_0_L    5A3 5C2 12C3
CPU_DTI<2..0>   5A3 12C3 35D5
CPU_EDTI        12A2 12C3
CPU_EMODE0_L    11A6 12A3
CPU_EMODE1_L    12A3 12C2
CPU_GBL_L       5B7 12A6 35D5
CPU_HIT_0_L     5B7 5C2 12A6
CPU_HRESET_L    11A5 12B3 12C2 29C4
CPU_L1TSTCLK    12B2 12B3
CPU_L2TSTCLK    12B3 12D2
CPU_L3_VSEL     11A6 13C2
CPU_LSSD_MODE   12B3 12D2
CPU_MCP_L       12B3 12D2
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CPU_PLL_CFGEXT  11D3 12C3
CPU_PLL_FS00    11C3
CPU_PLL_FS01    11C3
CPU_PLL_FS10    11C4
CPU_PLL_STOP_BASE 11C7
CPU_PLL_STOP_OC 11C8 29B6
CPU_PMONIN_L    12B3 12C2 14C4
CPU_PULLDOWN    12A2 12A3 12C6
CPU_PULLUP      12A3 12C2
CPU_QACK_L      5A7 12B3 35D5
CPU_QREQ_L      5A7 5C2 12B3
CPU_SHD0_L      12A6 12D2
CPU_SHD1_L      12A6 12D2
CPU_SMI_L       12B2 12B3 29C4
CPU_SRESET_L    12B3 12C2 14C4
CPU_SRWX_L      12A3 12C2
CPU_TA_L        5A3 5D2 12B3 35D5
CPU_TBEN        12B3 12D2
CPU_TBST_L      5B7 12A6 35D5
CPU_TEA_L       5A3 5D2 12B3 35D5
CPU_TSIZ<2..0>  5B7 12A6 35D5
CPU_TS_L        5C7 5D2 12C6 35D5
CPU_TT<4..0>    5B7 12A6 35D5
CPU_VCORE_HI_OC 11B8 18B6 29A4 29D4 34C6
CPU_VCORE_PWR_SEQ 34D8
CPU_VCORE_SEQ   34D8
CPU_VCORE_SEQ_L 34D8
CPU_VCORE_SLEEP 12D3 12D8 34C1 37D3
CPU_WT_L        5B7 12A6 35D5
CSLOT_ADDR<15..0> 14B2 14B4 14C4 14C6 27C6 27C7
               36C5 36D5
CSLOT_CE1_L     14B6 27C6 36C5
CSLOT_CE2_L     14B6 27C5 36C5
CSLOT_CS1FX_L   27C6 27C7 36D5
CSLOT_CS3FX_L   27C6 27C7 36D5
CSLOT_DATA<15..0> 27C5 27C6 27D5 27D6 27D7 36D5
CSLOT_IORD_L    14B1 27C5 36D5
CSLOT_IOWAIT_L  14B2 27C5 36C5
CSLOT_IOWR_L    14B1 27C5 36D5
CSLOT_IRQ_L     14B4 27C6 36C5
CSLOT_REG_L     14B4 27C5 36C5
CSLOT_RESET     14C4 27C5
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DCDC_EN_L       32D7
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EIDE0_DMARQ     14B6 27B8 36D5
EIDE0_DMA_ACK_L 27A6 27B7 36C5
EIDE0_DMA_RQ    27A6 27B7 36C5
EIDE0_INT       14B6 27A8 36D5
EIDE0_INTR      27A5 27A7 36C5
EIDE0_RD_L      14B6 27A8 36D5
EIDE0_READ_L    27A6 27A7 36C5
EIDE0_RST*      27A7 27B5
EIDE0_RST_L     14C6 27A8
EIDE0_WR*       27A5 27A7 36C5
EIDE0_WR_L      14B6 27A8 36D5
EIDE1_DMAREQ_PD 14B6
EIDE1_INT_PD    14B6
EIDE_ADDR<2..0> 14C6 27B8 27C8 36D5
EIDE_ADDR_<2..0> 27A5 27A6 27B7 36C5
EIDE_CS1FX*     27A5 27B7 36C5
EIDE_CS1FX_L    14C6 27B8 27C8 36D5
EIDE_CS3FX*     27A6 27B7 36C5
EIDE_CS3FX_L    14C6 27B8 27C8 36D5
EIDE_DATA<15..0> 14C6 14D6 27B7 27C7 27C8 27D8 36D5

EIDE_DB_<15..0> 27A5 27A6 27B5 27B6 27B8 27C7 27C8
               36C5
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EIDE_IOCHRDY    14C6 27A8 36D5
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ENET_GBE_REFCLK 9B6 23C8 35B1
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ENET_MDIO       9B6 23C6 36A5
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ENET_PHY_GTX_CLK 9B7 23D6 35C1
ENET_PHY_TXD<7..0> 9B7 9C7 23D6 36A5
ENET_PHY_TX_EN  9C7 23D6 36A5
ENET_PHY_TX_ER  9C7 23D6 36A5
ENET_RSET       23C6
ENET_RXD<7..0>  9B6 23D8 36B5
ENET_RX_DV      9C6 23D8
ENET_RX_ER      9B6 23D8
ENET_TX_D<7..0> 9C6 36A5
ENET_TX_EN      9C6 36A5
ENET_TX_ER      9C6 36A5
ENET_VSSC       23B6
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FAN_ON_LOW      19C6
FAN_PWR         19D5 37B6
FAN_PWR_LOW     19C5 37B6
FBA_0           6A4 6B2 35C5
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FBSEL1          18B4
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FCAS_DQM1_L     6C3 6D4 35C5
FCAS_DQM2_L     6B3 6D4 35C5
FCAS_DQM3_L     6B3 6D4 35C5
FCAS_DQM4_L     6C2 6D4 35C5
FCAS_DQM5_L     6C2 6D4 35B5
FCAS_DQM6_L     6B2 6D4 35B5
FCAS_DQM7_L     6B2 6D4 35B5
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FIL2_DIG3V      20D4 37B3
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FILTER_OUT_R    21C4
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FIL_AUD_STAR    20C2 37B3
FIL_DIG3V       20D7 37B3
FMA_AR<12..0>   6B2 6B3 6B4 6C2 6C3 6C4 35C5
FMEMWE_L        6A4 6C3 35B5
FPAR_SPN_AR<7..0> 6B2 6B3 6C2 6C3
FRAM_CKE0_A     6A4 6C2 35B5
FRAM_CKE0_B     6A4 6C2 35B5
FRAM_CKE1_A     6A4 6C2 35B5
FRAM_CKE1_B     6A4 6C2 35B5
FRAS_CS0_L      6C3 6C4 35C5
FRAS_CS1_L      6B3 6C4 35C5
FRAS_CS2_L      6C3 6C4 35C5
FRAS_CS3_L      6B3 6C4 35C5
FSDCAS_L        6A4 6C2 35B5
FSDRAS_L        6A4 6C3 35B5
FW_BIAS0        24B4
FW_C_LKON       9B2 14B4 24B4
FW_F0           24C5
FW_F1           24C5
FW_INT_PU       14B4 14C4
FW_LINK_CNTL<1..0> 9B2 24B7 36A5
FW_LINK_DATA<7..0> 9B2 9C2 24B7 36A5
FW_LINK_LREQ    9B2 24B7 36A5
FW_PHY_CNTL<1..0> 24B6 36A5
FW_PHY_CPS      24C5
FW_PHY_DATA<7..0> 24B6 36A5
FW_PHY_LPS      9B2 24B6
FW_PHY_LREQ     24B6 36A5
FW_PHY_PD       14C4 24B6
FW_PHY_RST_L    24B6
FW_PHY_SE       24B6
FW_PWREN        24C7
FW_PWREN_L      24C6
FW_PWR_GATE     24D7
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FW_TPA0N        24B4 36D2
FW_TPA0P        24B4 36C2
FW_TPB0         24B3
FW_TPB0N        24B4 36C2
FW_TPB0P        24B4 36C2
FW_TPI1N        24B2 36C2
FW_TPI1P        24B2 36C2
FW_TPO1N        24B2 36C2
FW_TPO1P        24B2 36C2
FW_VGND         24B2 37B3
FW_VP           24B2 37B3
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HD_ADDR<2..0>   27C1 27C2 27C3 36B5
HD_CS1_L        27C2 27C3 36B5
HD_CS3_L        27C1 27C3 36B5
HD_DATA<15..0>  27D1 27D2 27D3 36B5
HD_DIOR_L       27C2 27C3 36B5
HD_DIOW_L       27C2 27C3 36B5
HD_DMACK_L      27C2 27C3 36B5
HD_DMARQ        14A5 27D2 36B5
HD_INTRQ        14A5 27C2 36B5
HD_IOCHRDY      14A5 27C2 36B5
HD_RESET_L      27D2 27D3 36B5
HOLE_22R10A     4B2 4C3
HOLE_22R10D     4B2 4C3
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HP_DET_CONN     21C2
HP_IN           21A7 21D3
HP_SENSE_NEG_INPUT 21D3
HP_SENSE_POS_INPUT 21D4
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IAC_RC_COMP     31C6
IBATTX0_65      31D4
IBATT_FB        31D5
IBATT_RC_COMP   31D6
IBATT_SERVO     31D5
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JTAG_ASIC_TDI   9A7 9B6
JTAG_ASIC_TDO   23C8
JTAG_ASIC_TMS   9A7 9B6 14A2 23C6
JTAG_ASIC_TRST_L 9A7 9B6 14A2 23C6
JTAG_CPU_RST_L  12B2 12B3
JTAG_CPU_TCK    12B2 12C3
JTAG_CPU_TDI    12B2 12C3
JTAG_CPU_TDO_TP 12C3
JTAG_CPU_TMS    12B2 12C3
JTAG_ENET_TDI   14A2 23C6
JTAG_KL_TDI     9B6 14A2
KBD_CAPSLOCK_LED 28D3
KBD_COMMAND_L   28C1 28C4 29C6
KBD_CONTROL_L   28C1 28C2 29C6
KBD_FUNCTION_L  28C1 28C4 29B6
KBD_ID          28D1 28D4 29B6
KBD_INTL        28D3
KBD_JIS         28D4
KBD_NUMLOCK_LED 28C4
KBD_OPTION_L    28C1 28C2 29B6
KBD_SHIFT_L     28C1 28C4 29C6
KBD_X<9..0>     28C1 28C2 28C4 28D1 29C6
KBD_Y<7..0>     28C2 28C4 29C6 29D6
KL_AGND         14A5 14D3 14D6 37D3
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KL_CREF2        14B4 18B6
KL_CSLOT_IORD_L 14B2 36D5
KL_CSLOT_IOWR_L 14B2 36D5
KL_DEVCS3_SPN   14B6
KL_DEVCS4_SPN   14B6
KL_DEV_ID<2..1> 14B4
KL_DEV_IN_L     14B4
KL_DIR_245_SPN  14B6
KL_ENET_RST_L   14C4 23B5
KL_FW_PWREN     14C4 24C7
KL_I2C_CLK      14A2 14D1 20C7 27B2
KL_I2C_DATA     14A2 14D1 20C7 27B1
KL_IRDA_FIR_L   14C2 27A4
KL_IRDA_LOF_SPN 14C2
KL_IRDA_RXD_L   14C2 14D1 27A4
KL_IRDA_SDMODE_SPN 14C2
KL_IRDA_TXD     14C1 27A4
KL_IRDA_TXD_UF  14C2
KL_OSC_EN       14A5
KL_PCI_GNT_L    8C5 14B8
KL_PCI_IDSEL    14B8
KL_PCI_REQ_L    8C2 8C5 14B8
KL_PEND_PROC_INT 14B4 29C4
KL_PLL_EN       14A4 14C4
KL_PROC_SLEEP_REQ_L 14B4 29B4
KL_SND_CLKOUT   14B2
KL_SND_SCLK     14B2
KL_SND_SYNC     14B2
KL_SND_TO_AUDIO 14B2
KL_SUSPEND_REQ_L 14B4 29B6 29D7
KL_USB0_PCI_IDSEL 14B8
KL_USB1_PCI_IDSEL 14B8
KL_WATCHDOG_L   14A4 29C6
LCD_PWREN_L     26D3
LED_LINK10      23C6 23C8
LED_LINK100     23C6 23C8
LED_RX          23C6 23C8
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LINE_OUT_GND    21B3 21C5 37B3
LINE_OUT_L      21C5
LINE_OUT_R      21C5
LINE_OUT_STAR_GND 21B3 21C4 37B3
LVDS_DDC_CLK    16C1 26C2
LVDS_DDC_DATA   16C1 26C2
LVDS_L0N        16B1 26D1 36C2
LVDS_L0P        16B1 26D1 36C2
LVDS_L1N        16B1 26D1 36C2
LVDS_L1P        16B1 26D1 36C2
LVDS_L2N        16B1 26D1 36C2
LVDS_L2P        16B1 26C1 36C2
LVDS_L3N_SPN    16B1
LVDS_L3P_SPN    16B1
L_SPKR_NEG      21B6
L_SPKR_POS      21B6
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M1H_INPUT       22C5
M1H_OUTPUT      22C4
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M1L_INPUT       22B5
M1L_OUTPUT      22B4
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MAX785_EN       32C7
MAX1644_VCC     33B7
MAX4298_BIAS    21C7
MAX4298_CBYPASS 21C7
MAX4298_IN1     21D6
MAX4298_IN2     21D6
MAX4298_MUTE    21C7
MAX4298_SVCC    21C6
MAX4298_VCC     21D7 37B3
MB2_IDE_OE_PU   14B4 14C4
MB_IRQ_PU       14B4 14C4
MB_PWREN_L      14C4
MDI0_PD         23C5
MDI1_PD         23C5
MDI2_PD         23C4
MDI3_PD         23C4
MDI_M<3..0>     23C6 23D6 36D2
MDI_P<3..0>     23C6 23D6 36D2
MEMWE_L         6A5 6B6 35B5
MEM_DATA<63..0> 6A2 6A3 6A8 6B2 6B3 6B8 6C2 6C3 6C8
                6D2 6D3 6D8 35C5
MEM_EXT_R       6B7 35B5
MIC_1_65V       22B6
MIC_4V          22C6
MIC_5V          22C6 37B3
MIC_HIGH        21B5 22C5
MIC_LOW         21B5 22B5
MIC_OP_OUT1     22C6
MIC_OP_OUT2     22C6
MIC_STAR_GND    21A3 22B4 37B3
MODEM_HOOK_PU   14B4 14C4
MODEM_USB_DM    14B1 27B1 36B2
MODEM_USB_DP    14B1 27B1 36B2
MPIC_CLK        9C2 14B4
MPIC_CPU_INT_L  12B2 12B3 14B4
MPIC_DATA_L     9C2 14B4
MPIC_SYNC_L     9C2 14B4
MUTE_STAR_GND   21A3 21B8 37B3
NUMLOCK_LED     28D4
NUMLOCK_LED_L   28D4 29C7
PBUS_DIV        30C6
PBUS_DIV1       31B2
PCI_ACK64_L     8B5 8C7
PCI_AD<63..0>   8A4 8B4 8B7 8C4 8C7 8D4 8D7 14B8
                14C8 14D8 15B7 15C7 19B3 19C2 19C3
                35A5
PCI_CBE<7..0>   8B5 8B7 8C5 8C7 14B8 15B7 35A5
PCI_DEVSEL_L    8C5 8D2 14B8 15B7 35A5
PCI_FRAME_L     8C5 8D2 14B8 15B7 35A5
PCI_IRDY_L      8C5 8D2 14B8 15B7 35A5
PCI_PAR         8C5 14B8 15B7 35A5
PCI_PAR64       8B5 8C7
PCI_PERR_L      15B7 15D7
PCI_REQ64_L     8B5 8C7
PCI_SERR_L      15B7 15D7
PCI_STOP_L      8C5 8D2 14B8 15B7 35A5
PCI_TRDY_L      8C5 8D2 14B8 15B7 35A5
PLL_AVDD        18C5 37C3
PLL_SDRAM_CPU1  18C6 37C3
PLL_STOP_L      11C7
PLL_STOP_RC     11C8
PLL_VCC_CPU0    18D5 37C3
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PMU_AC_DET      29B4
PMU_AC_IN       29B4
PMU_BACKUP_SELECT_SPN 29C6
PMU_BATT0_DET_L 29B4
PMU_BATT1_DET_L_PU 29B4 29C2
PMU_BATT_DET_L  29B3 29D2 30B7
PMU_BYTE        29B6 29C7
PMU_CAPSLOCK_LED_L 29C6
PMU_CHARGE_V    29C4 31A3
PMU_CHRG_BATT_0 29C4 30A3
PMU_CHRG_EN_L   30C2
PMU_CLK         14A2 29C4
PMU_CNVSS       29A4 29B6 29C7
PMU_EPM         29A4 29D2 29D4
PMU_FROM_KL     14B2 29C4
PMU_I2C_CLK     18B6 29B4 29C2
PMU_I2C_DATA    18B6 29B4 29C2
PMU_INT_L       14C4 29B6
PMU_KL_NMI      14B4 14C4 29D4
PMU_LID_CLOSED_L 28D5 29A5 29B2 29C4
PMU_NMI_BUTTON_L 29A5 29C4 29D2
PMU_NMI_L       29C4 29D2
PMU_NUMLOCK_LED_L 29C6
PMU_OOPS        29B2 29B4
PMU_PME_L       9B2 14B4 29B2 29C4
PMU_POWERUP_OK  29B4 29D2
PMU_POWER_UP_L  29C6 29D7 32D8
PMU_REQ_L       14A2 14C4 29C4
PMU_RESET_BUTTON_L 29A5 29C4 29D2
PMU_RESET_L     29A4 29B6
PMU_RESET_L_SW  29B7
PMU_RESET_UF_L  29B7
PMU_SLEEP_LED_L 28A5 29C4
PMU_SMB_CLK     29B4 29C2 30B6
PMU_SMB_DATA    29B4 29C2 30B6
PMU_TEMP        29B2 29B4
PMU_TO_KL       14B2 29C4
POWER_VALID     29B2 29C4
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PS_BST_5V       32C6
PS_CS_3V        32C6 37C6
PS_CS_5V        32C6
PS_FB_3V        32C6
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PS_LX_3V        32B5 37C6
PS_LX_5V        32D5 37C6
PS_NGATE_3V     32C6
PS_NGATE_5V     32C6
PS_PGATE_3V     32C6
PS_PGATE_5V     32C6
PS_REF          32C7
PS_SS_3V        32C7
PS_SS_5V        32C7
PS_SYNC         32C7
PS_VL           32D7 37C6
PWR3V_STAR_GND  20A3 21A3 37B3
PWR4V_STAR_GND  20A3 21A3 37B3
PWRBUS_14_24V   31C7 31D5 37D6
PWR_STABLE_DELAY 31B1
RAD<12..0>      6B5 6C5 6C6 6D6 35C5
RAM_CKE0        6A5 6B6 35B5
RAM_CKE1        6A5 6B6 35B5
RAM_CKE2        6A5 6B6 35B5
RAM_CKE3        6A5 6B6 35B5
RAS_CS0_L       6C5 6C6 35C5
RAS_CS1_L       6C5 6C6 35C5
RAS_CS2_L       6C5 6C6 35C5
RAS_CS3_L       6C5 6C6 35C5
RJ45_C0_PD      23D3
RJ45_C1_PD      23D3
RJ45_C2_PD      23C3
RJ45_C3_PD      23C3
RJ45_DN<3..0>   23C3 23D3 36D2
RJ45_DP<3..0>   23C3 23D3 36D2
ROM_CS_L        6B6 19B3
ROM_OE_L        6A6 19B3
ROM_RW_L        6A6 19B3
ROM_WP_L        19B3
RSET_+5V_IO_SLEEP 26B8
RUN/SS          30C2 31C5
R_SPKR_NEG      21B6
R_SPKR_POS      21A6
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SDCAS_L         6A5 6C6 35B5
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SLEEP           26B8 29B6 29D7 32B3 32C8 33B3
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SLEEP_LED_L     28B4
SLEEP_LED_SW    28B5
SLEEP_LED_SW_L  28B5
SLEEP_LED_UF    28B3
SLEEP_LS5       32D3
SLEEP_LS5_EN_L  32C2
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SND_CLKOUT      14A1 20C7 20D3
SND_HP_MUTE_L   14C4 21C8
SND_HP_SENSE    14B4 21D5
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SND_SCLK        14B1 20C7 20D3
SND_SYNC        14B1 20C7 20D3
SND_TO_AUDIO    14B1 14C1 20C7
SND_TO_KL       14B2 14C1 20C2
SOFT_PWR_ON_L   28B2 29C6 29D7
SPKR_STAR_GND   21A3 21A8 37B3
SPO_ESD_F       28B2
SYSCLK_CPU      12C3 18D2 35D1
SYSCLK_CPU_UF   18C4 35D1
SYSCLK_DIMM0_A  6C3 18C2 35D1
SYSCLK_DIMM0_A_UF 18C4 35D1
SYSCLK_DIMM0_B  6B2 18C2 35D1
SYSCLK_DIMM0_B_UF 18C4 35D1
SYSCLK_DIMM1_A  6C3 18C2 35D1
SYSCLK_DIMM1_A_UF 18C4 35D1
SYSCLK_DIMM1_B  6B2 18C2 35D1
SYSCLK_DIMM1_B_UF 18C4 35D1
SYSCLK_UNIN     5D7 18C2 35D1
SYSCLK_UNIN_RDCLK 6B6 18C2 35D1
SYSCLK_UNIN_RDCLK_UF 18B4 35D1
SYSCLK_UNIN_UF  18C4 35D1
SYSTEM_CLK_EN   16A7 18B6 29C4
TAS_RESET_L     20B6
TAS_RESET_RC    20B6
TI_AVSS         20D7 37A3
TI_CAP_PLL      20D6
TI_CS1          20C7
TI_CS2          20C7
TI_LOWPWR       20C5
TI_MOD0         20C3
TI_MOD1         20C3
TI_MOD2         20C3
TI_SDO          20C2
TI_TI_SD        20C5
TI_VCOM         20C2
TPAD_F_RXD      28C7
TPAD_F_TXD      28D7
TPAD_GND        28C6 37B6
TPAD_RXD        28C8 29B2 29C4
TPAD_TXD        28D8 29B2 29C4
TPS2211_SHDN_L_PU 15D5
TV_C            26D5
TV_COMP         26D5
TV_GND1         26D5 37B6
TV_GND2         26C6 37B6
TV_Y            26D5
T_FILTR_OUT_L   21C3
T_FILTR_OUT_R   21C3
T_FILTR_RL      21C3
UATA_DET_PD     14B4 14C4
UIDE_ADDR<2..0> 14A6 27C4 36B5
UIDE_CS1FX_L    14A6 27C4 36B5
UIDE_CS3FX_L    14A6 27C4 36B5
UIDE_DATA<15..0> 14A6 14B6 27D4 36B5 36C5
UIDE_DIOR_L     14A6 27C4 36B5
UIDE_DIOW_L     14A6 27C4 36B5
UIDE_DMACK_L    14A6 27C4 36B5
UIDE_DMARQ      14A6 36B5
UIDE_INTRQ      14A6 36B5
UIDE_IOCHRDY    14A6 36B5
UIDE_RST_L      14A6 27D4 36B5
UNIN_AGP_VREF   7A5 16C7
UNIN_AGP_VREF_H 16C7
UNIN_AGP_VREF_L 16B7
UNIN_BR_1_L_PU  5B2 5C7
UNIN_DRDY_1_L_PU 5A3 5B2
UNIN_HIT_1_L_PU 5A7 5B2
UNIN_I2C_CLK0   6A2 9B6 9D7 19B7
UNIN_I2C_CLK1   6A2 9A6 9D7 19C7
UNIN_I2C_DATA0  6A3 9B6 9D7 19B7
UNIN_I2C_DATA1  6A3 9A6 9D7 19D7
UNIN_JTAG_TEI   9A7 9B6
UNIN_MAXBUS_REF 5A7 11B4
UNIN_PU_RESET_L 9C2 29A2 29C4
UNIN_QREQ_1_L_PD 5A7 5B2
UNIN_RESET_L    9C2 19B3 29A2 29D4
UNIN_SPARE_AB6  5A7
UNIN_SUSPEND_ACK_L 5A7 29B6
UNIN_SUSPEND_REQ_L 5A7 29B6 29C7
UNI_AGP_PME_L_PD 7B2 7B7
UNI_AGP_TYPEDET_PD 7B2 7B7
UNI_PCI_GNT1_L_SPN 8C5
UNI_PCI_GNT2_L_SPN 8C5
UNI_PCI_GNT3_L_SPN 8C5
UNI_PCI_GNT4_L_SPN 8C5
UNI_PCI_REQ_L_PU 8C2 8D5
UNI_ROM_CS_L    6A7
UNI_ROM_OE_L    6A7
UNI_ROM_RW_L    6A7
USB_D1M         25B6 36B2
USB_D1M_EMI     25B5 36B2
USB_D1P         25B6 36B2
USB_D1P_EMI     25B5 36B2
USB_D2M         25C6 36B2
USB_D2M_EMI     25C5 36B2
USB_D2P         25B6 36B2
USB_D2P_EMI     25B5 36B2
USB_DAM         14C2 25C7 36C2
USB_DAP         14C2 25B7 36C2
USB_DBM         14C2 36C2
USB_DBP         14C2 36C2
USB_DCM         14B2 25B7 36C2
USB_DCP         14B2 25B7 36C2
USB_DDM         14B2 36C2
USB_DDP         14B2 36C2
USB_OC_AB_L     14C2 14D1
USB_OC_CD_L     14B2 14D1
USB_OC_L_SPN    25C6
USB_PWREN_AB_L  14C2 14D1
USB_PWREN_CD_L  14B2 14D1
USB_PWREN_L     25C7
USB_SW_EN       25C7
USB_SW_RSET     25C7
VCORE_BOOST     34C5
VCORE_BOOST_ESR 34C5
VCORE_CC        34B6
VCORE_D0        34B6
VCORE_D1        34B6
VCORE_D2        34B6
VCORE_D3        34B6
VCORE_D4        34B6
VCORE_DH        34C5
VCORE_DL        34B5
VCORE_FB        34B5
VCORE_GND       34B5
VCORE_GNDA      34B6 37B6
VCORE_GNDDIV    34B5
VCORE_GNDSNS    34A1
VCORE_ILIM      34C6
VCORE_LX        34B5 37B6
VCORE_REF       34B6
VCORE_SHDN_L    34C6
VCORE_SNS       34A1
VCORE_SNUBBER   34B3 37B6
VCORE_TIME      34B5
VCORE_TON       34B6
VCORE_VCC       34C6 37C6
VCORE_VGATE     34B5
VCORE_VPLUS     34C5
VGA_B           26A6
VGA_G           26A6
VGA_HSYNC       16D4 26A5
VGA_MONID<3..0> 26A5
VGA_R           26A6
VGA_VSYNC       16D4 26A5
VREFM           20D2
VREFP           20D2
VRFILT          20D2
ZENER_GTR_THAN_18V 31B8
_VCHRG          31B3
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*** Unit Cross-Reference ***
--- for the entire design --

BS1	PCB_STANDOFF	4A3
BS2	PCB_STANDOFF	4B3
BS3	PCB_STANDOFF	4B1
BS4	PCB_STANDOFF	4B1
BS5	PCB_STANDOFF	4B1
C1	CAP_P	31D2
C2	CAP_P	26B7
C3	CAP_P	31B2
C4	CAP_P	31C3
C5	CAP	26A4
C6	CAP	26A5
C7	CAP	26A5
C8	CAP	26A5
C9	CAP	26B7
C10	CAP	31B3
C11	CAP_P	21C5
C12	CAP	29D6
C13	CAP	11C7
C14	CAP_P	25C5
C15	CAP_P	21C5
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C17	CAP	31B3
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C615	CAP	10C3
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C692	CAP	18C6
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C743	CAP	20B6
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D1	DIODE_SCHOT_3P	21D6
D2	DIODE_SCHOT	30D3
D3	DIODE	31B3
D4	ZENER_MMBZ15VDLT1	28B2
D5	DIODE_SCHOT	31C4
D6	DIODE	33C7
D8	DIODE_SCHOT	32A4
D10	DIODE_SCHOT	32C4
D11	DIODE_SCHOT	32A7
D12	DIODE_SCHOT	30B5
D13	DIODE	34C7
D14	ZENER	30C7
D15	ZENER_MMBZ15VDLT1	21C2
D16	DIODE_SCHOT	19C5
D17	DIODE	31B1
D18	ZENER	31B7
D19	DIODE	33B7
D20	DIODE_SCHOT	24D6
D21	DIODE	31B6
D22	DIODE	31D6
D23	DIODE	30D3
D24	DIODE	30A4
D25	DIODE	32A5
D26	DIODE	30A3
D27	DIODE	34C7
D28	DIODE	34D7
D29	DIODE	32D5
D30	DIODE	32D6
D31	DIODE_SCHOT	32B5
D33	DIODE_SCHOT	32B7
D34	DIODE_SCHOT	32A7
D35	DIODE_SCHOT	34C5
D36	DIODE_SCHOT	34B3
F1	FUSE	24D5
F2	FUSE	31D4
FL1	FILTER_CHOKE_DUAL	24C3
G1	OSC	16B3
G2	OSC	14A4
J1	CON_F7RT_MINIDIN	26D6
J2	CON_RJ45_SHORT	23D2
J3	CON_F15RT_DB_RFL	26B6
J4	CON_F4RT_USBKINK	25B4
J5	CON_F4RT_USBKINK	25C4
J6	CON_4RT_WRIB	25C2
J7	CON_FWVERT_SKT	24C2
J8	CON_F3RT_PWRJ	30D8
J9	CON_F4RT_SDOUT	21C2
J10	CON_10	29A4
J11	CON_M3SM_WRIB	19C5
J12	CON_10STSM_5087	27B3
J13	CON_F30STSM_5047	27B2
J14	CON_M3SM_WRIB	31D2
J15	CON_F30SM_LPS_J3_PCT	28D3
J16	CON_M80STSM_55055	15C2
J17	CON_M6ST_BTRY	30B8
J18	CON_152SM_STCKSO	6D3
J19	CON_2RTSM_125	28A3
J20	CON_F20RTSM_20143	26D1
J21	CON_2RTSM_125	28B1
J22	CON_6RTSM_125	21B5
J23	CON_10STSM_5087	26C1
J24	CON_M50SM_5MM	27B5
J25	CON_M70SM_5MM	27D5
J26	CON_M50SM_5MM	27D2
J27	CON_10STSM_5087	28D7
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L3	IND	30D6
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L5	IND	31C3
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L70	IND	28D8
L71	IND_3P	34C3
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Q2	TRA_2N3906	28B4
Q3	TRA_2N7002	11C7
Q4	TRA_SI4410DY	31C4
Q5	TRA_2N7002	11C7
Q6	TRA_SI4410DY	31B4
Q7	TRA_2N7002	11C7
Q8	TRA_2N7002	21C7
Q10	TRA_2N3904	11C6
Q11	TRA_2N7002	30C2
Q12	TRA_TP0610	30C2
Q13	TRA_2N7002	30A5
Q14	TRA_2N7002	32A7
Q15	TRA_TP0610	32A7
Q16	TRA_2N7002	32C2
Q17	TRA_2N7002	25C7
Q18	TRA_SI3443DV	19C5
Q19	TRA_2N7002	28B6
Q20	TRA_2N7002	31B7
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Q23	TRA_SI3443DV	19C5
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Q25	TRA_SI4435DY	30D4
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Q34	TRA_NDS9407	24D6
Q35	TRA_2N7002	23A6
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Q37	TRA_2N7002	30A4
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Q40	TRA_2N3904	34D7
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Q44	TRA_2N7002	30A3
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Q53	TRA_SI3443DV	32D2
Q54	TRA_2N7002	32C7
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Q56	TRA_2N7002	26A4
Q57	TRA_2N7002	26A4
Q58	TRA_2N7002	26B4
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Q65	TRA_IRF7805	34C4
Q66	TRA_FDS6672A	34B4
Q67	TRA_FDS6672A	34B3
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R63	RES	22C4
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R230	RES	29D8
R231	RES	29C8
R232	RES	21C5
R233	RES	31C5
R234	RES	25C6
R235	RES	26B8

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R236	RES	9A8
R237	RES	9A8
R238	RES	9D8
R239	RES	9C6
R240	RES	9C6
R241	RES	7C1
R242	RES	16D7
R243	RES	29B3
R244	RES	29C1
R245	RES	29C8
R246	RES	21C4
R247	RES	21C4
R248	RES	21D3
R249	RES	9D8
R250	RES	9A8
R251	RES	9C6
R252	RES	9C6
R253	RES	26A8
R254	RES	26A8
R255	RES	16A5
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R257	RES	29B7
R258	RES	29D1
R259	RES	29B3
R260	RES	21C4
R261	RES	31C8
R262	RES	31B7
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R312	RES	29B1
R313	RES	29C1
R314	RES	29B7
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R332	RES	33B5
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R338	RES	16C3
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R385	RES	23B5
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R387	RES	16C3
R388	RES	16C3
R391	RES	21D4
R392	RES	21D4
R393	RES	30C3
R394	RES	30C5
R395	RES	23C6
R396	RES	9C6
R397	RES	6B6
R398	RES	6A6
R399	RES	16C4
R400	RES	16C4
R401	RES	16C4
R402	RES	16C4
R405	RES	11D4
R406	RES	11D4
R407	RES	6A6
R408	RES	7D1
R409	RES	21B6
R410	RES	30C6
R411	RES	30D3

R413	RES	23B2
R415	RES	11D4
R416	RES	12D1
R417	RES	8C1
R418	RES	7B1
R419	RES	7C1
R420	RES	30C5
R421	RES	24B5
R422	RES	11D4
R423	RES	11B3
R424	RES	11A3
R425	RES	8C1
R426	RES	7B1
R427	RES	21B7
R428	RES	30C5
R429	RES	30C5
R430	RES	30C3
R431	RES	30C3
R438	RES	34D8
R439	RES	12C1
R440	RES	12C1
R441	RES	33B3
R442	RES	16B7
R443	RES	16D7
R444	RES	27B2
R445	RES	32B3
R446	RES	33C7
R448	RES	12B1
R449	RES	12B1
R450	RES	12C1
R451	RES	12D1
R452	RES	5D1
R453	RES	5B1
R454	RES	7C1
R455	RES	17B7
R456	RES	17B7
R457	RES	16D8
R458	RES	16A7
R459	RES	16A3
R460	RES	33D7
R461	RES	23B6
R464	RES	12C1
R465	RES	12C1
R466	RES	5B1
R467	RES	7D5
R468	RES	16D7
R469	RES	17A6
R470	RES	16C8
R472	RES	23A5
R473	RES	5D1
R474	RES	12D1
R475	RES	5B1
R476	RES	5C1
R477	RES	22B4
R478	RES	32D4
R479	RES	24D7
R480	RES	32A5
R481	RES	12D1
R482	RES	12B1
R483	RES	12C1
R484	RES	17C5
R485	RES	27B1
R486	RES	22C6
R487	RES	24C6
R488	RES	34D7
R489	RES	12B1
R490	RES	12D1
R491	RES	11B6
R492	RES	7C1
R493	RES	17D7
R494	RES	17D7
R495	RES	30A3
R497	RES	34D7
R498	RES	12B1
R499	RES	12D1
R500	RES	11A6
R501	RES	5C1
R502	RES	6D5
R503	RES	5A7
R504	RES	6B6
R505	RES	17D6
R506	RES	17C6
R507	RES	32D7
R511	RES	23D8
R512	RES	23D8
R513	RES	23C8
R514	RES	12D1
R515	RES	11B5
R516	RES	5B1
R517	RES	5D4
R518	RES	6D5
R519	RES	7C1
R520	RES	7A5
R521	RES	7C4
R522	RES	30A4
R523	RES	32A5
R524	RES	12A1
R525	RES	12A1
R526	RES	11A6
R527	RES	11A5
R528	RES	5C1
R529	RES	6C5
R530	RES	6C5
R531	RES	7C3
R532	RES	16B3
R533	RES	16B2
R534	RES	30B4
R535	RES	5D1
R536	RES	12C1
R537	RES	11A6
R538	RES	6B5
R539	RES	6B6
R540	RES	8C1
R541	RES	7B3
R542	RES	12C1
R543	RES	12D3
R544	RES	7B1
R545	RES	7B4
R546	RES	24C6
R547	RES	32C2
R548	RES	5D1
R549	RES	7D7
R550	RES	16B3
R551	RES	30B5
R552	RES	32D3
R553	RES	5D1
R554	RES	7C1
R555	RES	30A3
R556	RES	32A5
R557	RES	12D8
R558	RES	12B1
R559	RES	6C5
R560	RES	30A6
R561	RES	32D4
R562	RES	32D3
R563	RES	27A7
R564	RES	16B4
R565	RES	32D7
R566	RES	32D8
R567	RES	6A5
R568	RES	7C1
R569	RES	27A5
R570	RES	6B5
R571	RES	6B5
R572	RES	6A5
R573	RES	6D5
R574	RES	6D5
R575	RES	6D5
R577	RES	27B7
R578	RES	27B7
R579	RES	27B7
R580	RES	27B7
R581	RES	27B7
R582	RES	6B5
R583	RES	6B5
R584	RES	6C5
R585	RES	6C5
R586	RES	7B1
R587	RES	28D1
R588	RES	28C3
R589	RES	28D2
R590	RES	28D4
R592	RES	5D6
R594	RES	26B3
R595	RES	26A3
R596	RES	26A4
R597	RES	26A4
R599	RES	26D3

R600	RES	28D3
R602	RES	6B5
R603	RES	18C5
R609	RES	18C5
R610	RES	14A6
R611	RES	19B3
R612	RES	14B2
R613	RES	14C5
R614	RES	14B2
R615	RES	14B2
R616	RES	14D7
R618	RES	15D8
R619	RES	30B7
R620	RES	27C3
R621	RES	27C3
R622	RES	27C3
R623	RES	27C3
R624	RES	27C3
R625	RES	27C3
R626	RES	27C3
R627	RES	15B4
R628	RES	27D2
R629	RES	27D2
R630	RES	27D2
R631	RES	27D3
R632	RES	27C2
R633	RES	27C2
R634	RES	15D4
R635	RES	27C3
R636	RES	27C3
R637	RES	34B8
R638	RES	34B8
R639	RES	34B8
R640	RES	34B7
R641	RES	34B8
R642	RES	34B8
R643	RES	34B8
R644	RES	34B7
R645	RES	34C6
R646	RES	34B6
R647	RES	34C6
R648	RES	34C6
R649	RES	34C5
R650	RES	34B5
R651	RES	34B5
R652	RES	20C5
R653	RES	20B6
R654	RES	20B5
R655	RES	20B6
R656	RES	20B6
R657	RES	21A7
R659	RES	34B6
R660	RES	34B6
R661	RES	18B6
R662	RES	18C4
R665	RES	15C2
R666	RES	5C1
R667	RES	5D1
R668	RES	5C1
R669	RES	20B3
R670	RES	20A3
R671	RES	14C2
R672	RES	34B8
R673	RES	14D1
R674	RES	30D7
R675	RES	34B7
R676	RES	34C3
R677	RES	34C5
RP1	RPAK10P2C	8D8
RP2	RPAK4P	24B6
RP3	RPAK4P	24B6
RP4	RPAK4P	29D8
RP5	RPAK4P	27D7
RP6	RPAK4P	27D7
RP7	RPAK4P	27D7
RP8	RPAK4P	27D7
RP9	RPAK4P	27C7
RP10	RPAK4P	14C5
RP11	RPAK4P	14C5
RP12	RPAK4P	15D2
RP13	RPAK10P2C	8C8
RP14	RPAK10P2C	28D1
RP15	RPAK10P2C	8C8
RP16	RPAK10P2C	28C1
RP17	RPAK10P2C	8B8
RP18	RPAK10P2C	8D8
RP21	RPAK4P	27C7
RP22	RPAK4P	27C7
RP23	RPAK4P	27B7
RP24	RPAK4P	27C7
RP25	RPAK4P	14B5
RP26	RPAK4P	27D5
RP27	RPAK4P	8D1
RP28	RPAK4P	27D6
RP29	RPAK4P	8D1
RP30	RPAK4P	15D2
RP31	RPAK4P	14B5
RP32	RPAK4P	15D2
RP33	RPAK4P	15D2
RP34	RPAK4P	14D1
RP35	RPAK4P	15C8
RP36	RPAK4P	27D3
RP37	RPAK4P	27D3
RP38	RPAK4P	27D3
RP39	RPAK4P	27D3
S1	SWI_RESET_4PSM	29B8
SL1	SLOT	4B3
T1	XFR_ENET_1000BT	23C4
U1	741G32	16D3
U2	M16C62	29D5
U3	AUDIO_LM4863	21B6
U4	RAGE_MOBILITY_M6_35X35	16D2 16D6 17C4
U5	COMPARATOR_LMC7211	21D4
U6	TSB41AB1	24C5
U8	DS1775	19B6
U9	LTC1625	31C5
U10	DS1775	19D6
U11	DS1775	19A6
U12	TRANSCEIVER_88E1010_1011	23B3 23D7
U13	COMPARATOR_LMC7211	30A5
U14	UNI_N_658P	5C5 6D7 7C6 8D4 9D4
U15	SCVGER483	12C5 13D3 13D6
U16	VREG_LP2951	20B4
U17	DS1775	19C6
U18	CLK_GEN_MK1708	16A4
U19	FEPR_1MX8	19C2
U20	LTC1761	17A7
U21	SWI_PWR_MAX890L	26B7
U22	741G32	16D3
U23	AMP_MAX4172	31D4
U24	AMP_MAX4172	31C8
U25	MAX4298	21C6
U26	SWI_PWR_MAX890L	25C6
U27	MAX6328	29B7
U28	MAX1644	33B6
U29	OPAMP_LMC6462	31B7 31D6
U30	TAS3001C	20D6
U31	MAX1644	33C6
U32	LTC1761	17C7
U33	ADDAC_TLC320AD77C	20D3
U34	COMPARATOR_LMC7211	30C5
U35	VREG_LP2951	32A4
U36	VREG_LP2951	20A4
U37	OPAMP_TS924	22B4 22B5 22C4 22C5
U38	COMPARATOR_LMC7211	30C3
U39	LTC1761	17D7
U40	MAX785	32C6
U41	VREG_LP2951	32A6
U43	CLK_GEN_C5005	18C5
U44	KEYLARGO	14C3 14C7
U45	PCI1410APGE	15C6
U46	PWR_CNTRL_TPS2211	15D4
U47	MAX1717	34C5
U48	741G32	26B3
XH1	MTGHOLE	4C2
XH2	MTGHOLE	4C2
XH3	MTGHOLE	4C2
XH4	MTGHOLE	4C2
XW1	SHORT	21B3
XW2	SHORT	21A3
XW3	SHORT	21B3
XW5	SHORT	21A3
XW7	SHORT	21A3
XW8	SHORT	32D4
XW9	SHORT	32C4
XW11	SHORT	20C7
XW12	SHORT	21B3
XW13	SHORT	21A3

XW15	SHORT	21A3
XW16	SHORT	14A3
XW17	SHORT	34B5
XW18	SHORT	34C1
XW19	SHORT	34B1
XW20	SHORT	34B4
Y1	CRYSTAL_4PIN	29B3
Y2	CRYSTAL	29B7
Y3	CRYSTAL	24C6
Y4	CRYSTAL	23B6
Y5	CRYSTAL	18C6
ZH1	MTGHOLE	4B3
ZH3	MTGHOLE	4D2
ZH4	MTGHOLE	4D3
ZH5	MTGHOLE	21B3
ZH6	MTGHOLE	4C2
ZH7	MTGHOLE	4D1
ZH8	MTGHOLE	4D3
ZH9	MTGHOLE	18C7
ZH10	MTGHOLE	4D1

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