### Table 5

<table>
<thead>
<tr>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>PART#</th>
</tr>
</thead>
<tbody>
<tr>
<td>820-1372</td>
<td>1 PCBF, ENTERPRISE, P84 PCB</td>
<td>1</td>
</tr>
<tr>
<td>051-6278</td>
<td>1 SCHEM, ENTERPRISE, P84 SCH</td>
<td>1</td>
</tr>
</tbody>
</table>

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

---

**System Block Diagram**

- **MPC7450 Maxbus Interface**
- **MPC7450 Data / L3 Cache Interfaces / L3 LDO**
- **CPU PLL and Configuration Straps**
- **DDR L3 Cache**
- **Intrepid Maxbus and Boot Straps**
- **Intrepid Memory Interface / Boot ROM**
- **DDR Memory Mixes**
- **200Pin DDR Memory SODIMM Connectors**
- **Intrepid AGP 4x/PCI**
- **Intrepid EMT/FW/EIDE Interfaces**
- **Intrepid GPIOs/Serial/USB Interfaces / SSCG**
- **Intrepid Power Rails / 1.5V LDO**
- **Intrepid Decoupling**
- **Cardbus Controller (PCI11510)**
- **MAP17/31 AGP & Frame Buffer**
- **MAP17/31 LVDS / TMDS / GPIO & GPU Vcore**
- **MAP17/31 Analog, DVO Interface, GND**

**Contents**

- **Titles and Contents**
- **MPC7450 Maxbus Interface**
- **MPC7450 Data / L3 Cache Interfaces / L3 LDO**
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**Map 17 / Map 31**

- **Component Locations**
- **Signal Names**
- **Revision History (1 of 1)**

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**Metric**

Apple Computer Inc.

**Schem, Enterprise, P84**

**DVT**

12/03/2002
POWER SYSTEM ARCHITECTURE

DC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

BATTERY CHARGER (MAX1772) PG 31

+3V_PMU LDO PG 32

+3V_MAIN LDO PG 32

AC ADAPTER IN PG 31

BACKLIGHT INVERTER

MAIN 2.5V/1.5V DC/DC (MAX1715)

VCC

+PBUS (12.8V)

GPU_VCORE

1.35V/+1.2V

DC/DC (MAX1717)

CPU_VCORE

(+1.4V/+1.5V)

POWER BLOCK DIAGRAM

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1  PREPREG (3MIL)
  SIGNAL (1/3 OZ + COPPER PLATING)
  GROUND (1/2 OZ)
2  LAMINATE (4MIL)
3  PREPREG (3MIL)
  SIGNAL (1/2 OZ)
4  LAMINATE (4MIL)
5  PREPREG (2MIL)
  SIGNAL (1/2 OZ)
6  LAMINATE (4MIL)
7  PREPREG (2MIL)
  CUT POWER PLANE (1 OZ)
8  LAMINATE (3MIL)
9  PREPREG (3MIL)
  GROUND (1/2 OZ)
10  LAMINATE (4MIL)
11  PREPREG (3MIL)
  SIGNAL (1/2 OZ)
12  LAMINATE (4MIL)
13  PREPREG (3MIL)
  SIGNAL (1/3 OZ + COPPER PLATING)

NOTE: 135 AND 125 PADS WERE CREATED BECAUSE THESE MOUNTING HOLES HANG OFF THE BOARD.
SEL = LOW; HOST = B PORT; A PORT = 1000OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG
1.5V LDO GENERATOR

THIS LDO WAS ADDED IN CASE INTREPID CORE DOES NOT RUN AT 1.5V
### POWER NET CONSTRAINTS

<table>
<thead>
<tr>
<th>NET NAME</th>
<th>DC IN</th>
<th>VOLTAGE (V)</th>
<th>MIN NECK WIDTH</th>
<th>MIN LINE WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>CPU</td>
<td>2.5V</td>
<td>40</td>
<td>25</td>
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<tr>
<td>L3 CACHE</td>
<td>L3</td>
<td>1.8V</td>
<td>40</td>
<td>25</td>
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<tr>
<td>DDR RAM</td>
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<td>1.8V</td>
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<td>25</td>
</tr>
<tr>
<td>INTREPID</td>
<td>INT</td>
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<td>MAX1715</td>
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<td>LTC1778</td>
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<tr>
<td>VCORE VCC</td>
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<tr>
<td>VCORE BOOST</td>
<td>VCORE BOOST</td>
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<tr>
<td>VCORE DL</td>
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<td>25</td>
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<tr>
<td>1_5V DL</td>
<td>1_5V DL</td>
<td>1.5V</td>
<td>40</td>
<td>25</td>
</tr>
<tr>
<td>1_5V BIST</td>
<td>1_5V BIST</td>
<td>1.5V</td>
<td>40</td>
<td>25</td>
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<tr>
<td>2_5V LIX</td>
<td>2_5V LIX</td>
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<td>25</td>
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<tr>
<td>5V_RSNS</td>
<td>5V_RSNS</td>
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<tr>
<td>1625_VSW</td>
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### SIGNAL CONSTRAINTS

<table>
<thead>
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<td>USB 2.0</td>
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<td>25</td>
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<td>1.8V</td>
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</tr>
<tr>
<td>SSCG</td>
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<td>1.8V</td>
<td>40</td>
<td>25</td>
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