1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
01		?	?	?	?

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3	POWER BLOCK DIAGRAM
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7	CPU PLL AND CONFIGURATION STRAPS
8	DDR L3 CACHE
9	INTREPID MAXBUS AND BOOT STRAPS
10	INTREPID MEMORY INTERFACE / BOOT ROM
11	DDR MEMORY MUXES
12	200PIN DDR MEMORY SODIMM CONNECTORS
13	INTREPID AGP 4X/PCI
14	INTREPID ENET/FW/UATA/EIDE INTERFACES
15	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
16	INTREPID POWER RAILS/1.5V LDO
17	INTREPID DECOUPLING
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23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
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30	PMU (POWER MANAGEMENT UNIT)
31	BATTERY CHARGER AND CONNECTOR
32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
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ENTERPRISE

12/03/2002

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG	✓	
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB		✓
INTREPID_USB	✓	
BBANG		✓
NO_BBANG	✓	
MAP31		✓
MAP17	✓	
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
NO_4XVCORE	✓	
4X_VCORE		✓

DVT

MAP17/MAP31

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0076	1	IC,ASSP,MAP17-464,GRPHCS CTLR,548 BGA	U43	CRITICAL	MAP17
338S0094	1	IC,ASSP,MAP31-464,GRPHCS CTLR,548 BGA	U43	CRITICAL	MAP31

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6278	1	SCHEM,ENTERPRISE,P84	SCH1	
820-1372	1	PCBF,ENTERPRISE,P84	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

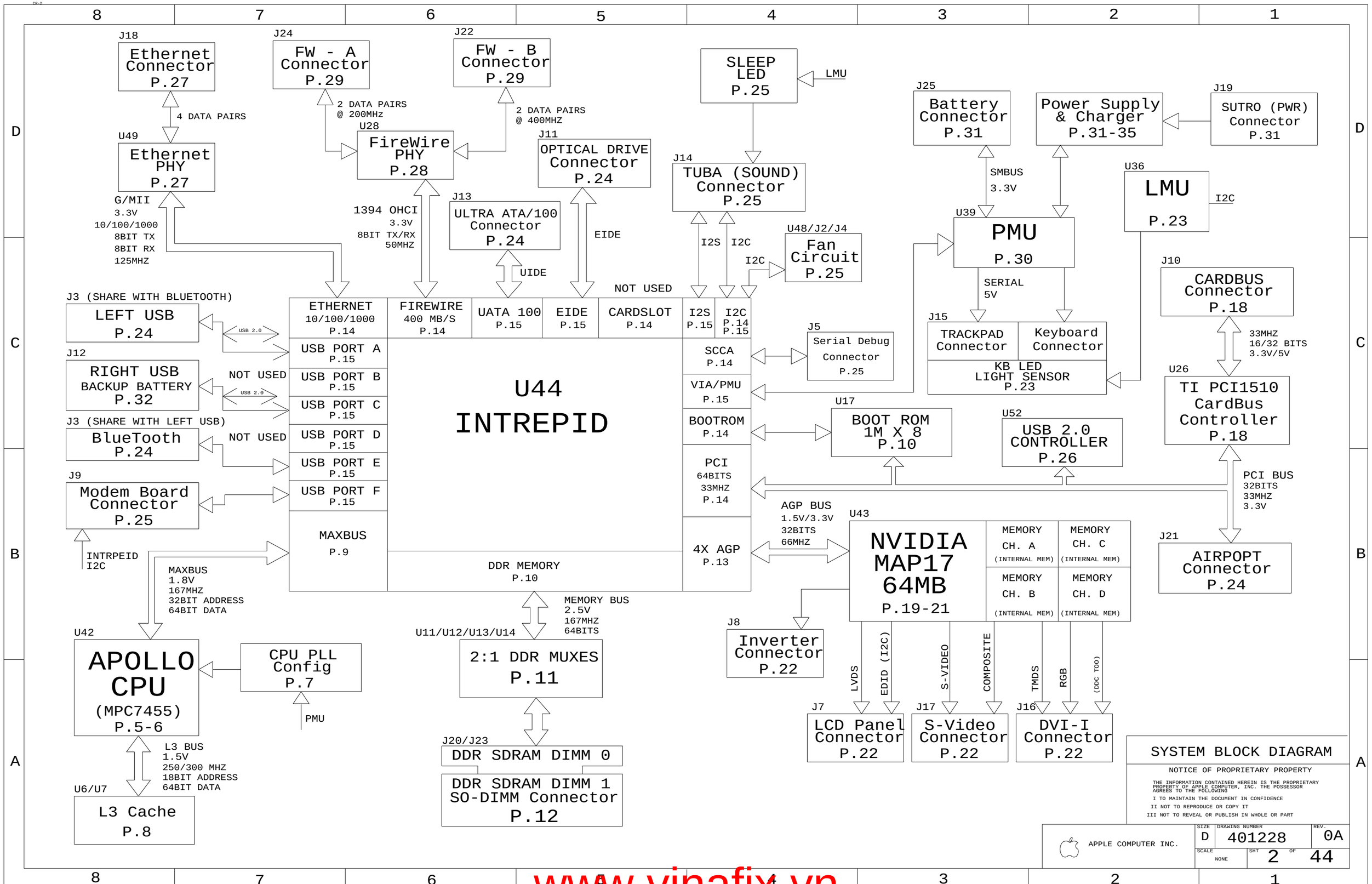
SIZE D

Apple Computer Inc.

TITLE
SCHEM,ENTERPRISE,P84

DRAWING NUMBER 401228 REV. 0A

SHT 1 OF 44



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF

>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

U21 PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715)
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2
PGOOD
1_5V_2_5V_OK

MAP17 DDR CORE
MAP17 DDR I/O
L3 CORE
DDR POWER
+2.5V_MAIN

+1.5V_MAIN
INTREPID CORE
AGP I/O
L3 I/O

DCDC_EN_L
AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707)
VCC
STBYMD
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

+5V_MAIN
EXT_VCC
VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.35V/+1.2V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

MAXBUS SEQUENCING
DCDC_EN
SLEEP

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.4V/+1.5V)

+PBUS
BACKUP BATTERY PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 32

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

BATTERY CHARGER (MAX1772) PG 31

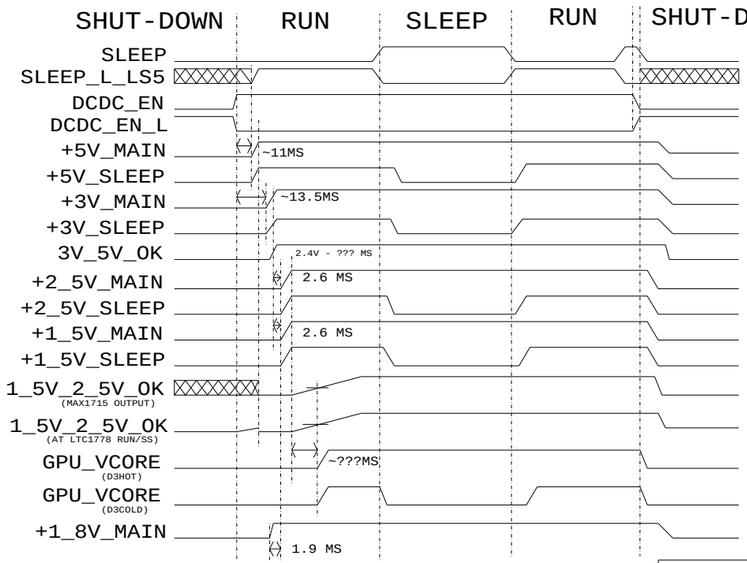
DC/DC (LTC3411)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A

SCALE	SHT	OF
NONE	3	44

CR-4

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

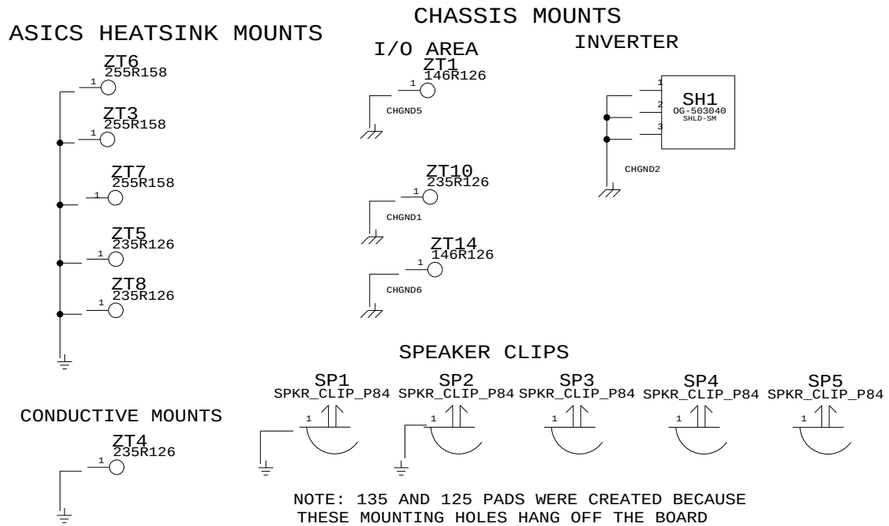
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

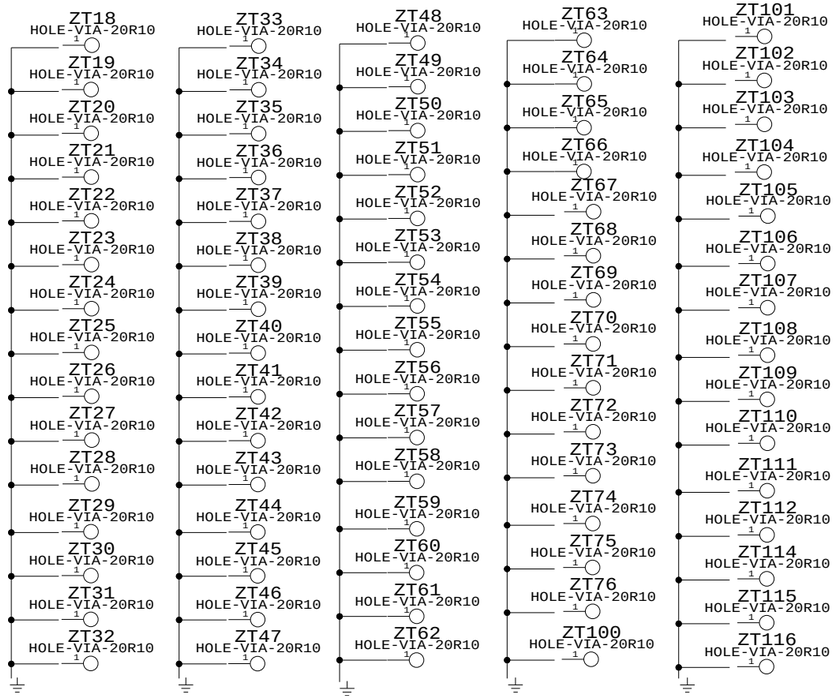
20R10 TH VIA OR VIA IN PAD

1			SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)		GROUND (1/2 OZ)
3	LAMINATE (4MIL)		SIGNAL (1/2 OZ)
4	PREPREG (3MIL)		SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)		GROUND (1/2 OZ)
6	PREPREG (2MIL)		CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)		CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)		GROUND (1/2 OZ)
9	LAMINATE (4MIL)		SIGNAL (1/2 OZ)
10	PREPREG (3MIL)		SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)		GROUND (1/2 OZ)
12	PREPREG (3MIL)		SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A

SCALE	SHT	OF
NONE	4	44

CR-5

CPU_VCORE DECOUPLING NETWORK

39 38 34 5 CPU_VCORE_SLEEP

R175 470 5% 1/10W MF 402

C153 10UF 20% 6.3V CERM 805 — C141 10UF 20% 6.3V CERM 805

C239 10UF 20% 6.3V CERM 805 — C255 10UF 20% 6.3V CERM 805

C204 2.2UF 20% 10V CERM 805 — C180 2.2UF 20% 10V CERM 805

C108 C200 C173 C140 0.1UF 20% 10V CERM 402

C138 C109 C201 C174 0.1UF 20% 10V CERM 402

C172 C139 C110 C202 0.1UF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 32)

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 5 7 9 16 17 23 34 38

R50 470 5% 1/16W MF 402

C31 C73 C51 C203 0.1UF 20% 10V CERM 402

C74 C76 C111 C238 0.1UF 20% 10V CERM 402

C30 C45 C95 C75 0.1UF 20% 10V CERM 402

CPU INTERNAL PLL FILTERING

CPU_VCORE_SLEEP 5 34 38 39

R5 10 5% 1/16W MF 402

38 CPU_AVDD

C29 0.1UF 20% 10V CERM 402 — C9 2.2UF 20% 10V CERM 805

MPC7450 PULL-UPS

+1_5V_SLEEP — 1_5V_MAXBUS — R606 0 5% 1/16W MF 603

+1_8V_SLEEP — 1_8V_MAXBUS — R602 0 5% 1/16W MF 603

38 34 23 17 16 9 7 5 MAXBUS_SLEEP

9 5 CPU_TBEN	R39 10K	5% 1/16W MF 402
5 CPU_CHKS_L	R90 10K	5% 1/16W MF 402
5 CPU_SHD0_L	R518 10K	5% 1/16W MF 402
5 CPU_SHD1_L	R66 10K	5% 1/16W MF 402
5 CPU_MCP_L	R73 10K	5% 1/16W MF 402
5 CPU_LSSD_MODE	RP11 10K	5% 1/16W SM1
5 CPU_L2TSTCLK	R24 10K	5% 1/16W MF 402
39 5 CPU_CHKSTP_OUT_L	R38 1K	5% 1/16W MF 402
5 CPU_SRWX_L	R84 10K	5% 1/16W MF 402
5 CPU_PMONIN_L	R55 10K	5% 1/16W MF 402
5 CPU_EMODE1_L	R44 10K	5% 1/16W MF 402
5 CPU_PULLUP	R56 1K	5% 1/16W MF 402
39 23 7 5 CPU_HRESET_L	R37 10K	5% 1/16W MF 402
30 5 CPU_SMI_L	R74 10K	5% 1/16W MF 402
4700HM FOR BOOT BANGER — 39 23 5 JTAG_CPU_TMS	R13 470	5% 1/16W MF 402
4700HM FOR BOOT BANGER — 39 23 5 JTAG_CPU_TDI	R12 470	5% 1/16W MF 402
15 5 MPIC_CPU_INT_L	RP11 10K	5% 1/16W SM1
39 5 CPU_SRESET_L	RP11 10K	5% 1/16W SM1
5 CPU_L1TSTCLK	RP11 10K	5% 1/16W SM1
5 CPU_EDTI	R32 10K	5% 1/16W MF 402
39 23 5 JTAG_CPU_TCK	R65 10K	5% 1/16W MF 402
5 CPU_PULLDOWN	R91 470	5% 1/16W MF 402

J9 J11 J13 J15 K12 K14 L9 L11 L13 L15 M10 M12 M14 N9 N11 N13 N15 P10 P12 P14 — VDD

B3 C5 C7 C10 D2 E3 E9 F5 G3 G9 H7 J5 K3 L7 M5 N3 P7 R4 T3 U5 U7 U11 U15 V3 V9 V13 Y2 Y5 Y7 Y10 Y17 AA4 AA15 — OVDD

GND — J10 J12 J14 K9 K11 K13 K15 L10 L12 L14 M9 M11 M13 N10 N12 N14 P9 P11 P13 P15 B1 B5 C3 C9 D7 E2 E5 F10 G4 G7 H5 J3 K5 M3 M6 P3 T4 T7 T9 T13 V2 V5 V8 V12 V15 W7 Y3 Y9 Y13 Y15 Y20 AA5 AA17 AB1

U42
APOLLO
1GHZ-1.4V
V3.3-NDE5-85C-BGA
(1 OF 3)

36 9 CPU_BR_L	K1	BR	
36 9 CPU_BG_L	R3	BG	
NC	F2	NC12	
36 9 CPU_TS_L	P5	TS	
5 CPU_PULLDOWN	E10	A0	
	N4	A1	
	E8	A2	
	N5	A3	
36 9 CPU_ADDR<0>	C8	A4	
36 9 CPU_ADDR<1>	R2	A5	
36 9 CPU_ADDR<2>	A7	A6	
36 9 CPU_ADDR<3>	M2	A7	
36 9 CPU_ADDR<4>	A6	A8	
36 9 CPU_ADDR<5>	M1	A9	
36 9 CPU_ADDR<6>	A10	A10	
36 9 CPU_ADDR<7>	U2	A11	
36 9 CPU_ADDR<8>	N2	A12	
36 9 CPU_ADDR<9>	P8	A13	
36 9 CPU_ADDR<10>	M8	A14	
36 9 CPU_ADDR<11>	W4	A15	
36 9 CPU_ADDR<12>	N6	A16	
36 9 CPU_ADDR<13>	U6	A17	
36 9 CPU_ADDR<14>	R5	A18	
36 9 CPU_ADDR<15>	Y4	A19	
36 9 CPU_ADDR<16>	P1	A20	
36 9 CPU_ADDR<17>	P4	A21	
36 9 CPU_ADDR<18>	R6	A22	
36 9 CPU_ADDR<19>	M7	A23	
36 9 CPU_ADDR<20>	N7	A24	
36 9 CPU_ADDR<21>	AA3	A25	
36 9 CPU_ADDR<22>	U4	A26	
36 9 CPU_ADDR<23>	W2	A27	
36 9 CPU_ADDR<24>	W1	A28	
36 9 CPU_ADDR<25>	W3	A29	
36 9 CPU_ADDR<26>	V4	A30	
36 9 CPU_ADDR<27>	AA1	A31	
36 9 CPU_ADDR<28>	D10	A32	
36 9 CPU_ADDR<29>	J4	A33	
36 9 CPU_ADDR<30>	G10	A34	
36 9 CPU_ADDR<31>	D9	A35	
NC	L5	AP0	
NC	L6	AP1	
NC	J1	AP2	
NC	H2	AP3	
NC	G5	AP4	
36 9 CPU_TT<0>	F1	TT0	
36 9 CPU_TT<1>	F4	TT1	
36 9 CPU_TT<2>	K9	TT2	
36 9 CPU_TT<3>	A5	TT3	
36 9 CPU_TT<4>	E1	TT4	
36 9 CPU_TBST_L	B7	TBST	
36 9 CPU_TSIZ<0>	L1	TSIZ0	
36 9 CPU_TSIZ<1>	H3	TSIZ1	
36 9 CPU_TSIZ<2>	D1	TSIZ2	
36 9 CPU_GBL_L	M4	GBL	
36 9 CPU_WT_L	L2	WT	
36 9 CPU_CI_L	R1	CI	
36 9 CPU_AACK_L	U1	AACK	
36 9 CPU_ARTRY_L	T2	ARTRY	
5 CPU_SHD0_L	L4	SHD0	
5 CPU_SHD1_L	L8	SHD1	
36 9 CPU_HIT_L	K2	HIT	

AVDD	B2	
BVSEL	G6	CPU_BUS_VSEL 7
SYSCLK	D6	SYSCLK_CPU 9 36
CLK_OUT	N1	CPU_CLKOUT_SPN
PLL_CFG0	A2	CPU_PLL_CFG<0> 7
PLL_CFG1	F7	CPU_PLL_CFG<1> 7
PLL_CFG2	C2	CPU_PLL_CFG<2> 7
PLL_CFG3	D4	CPU_PLL_CFG<3> 7
PLL_EXT	H8	CPU_PLL_CFGEXT 7
DBG	V1	CPU_DBG_L 9 36
DRDY	T6	36 CPU_DRDY_L_UF
DTI0	P2	CPU_EDTI 5
DTI1	T5	CPU_DTI<0> 9 36
DTI2	U3	CPU_DTI<1> 9 36
DTI3	P6	CPU_DTI<2> 9 36
TDI	E4	JTAG_CPU_TDI 5 23 39
TDO	H1	JTAG_CPU_TDO_TP 39
TMS	K4	JTAG_CPU_TMS 5 23 39
TCK	J7	JTAG_CPU_TCK 5 23 39
TRST	C1	JTAG_CPU_TRST_L 5 23 39
LSSD_MODE	F6	CPU_LSSD_MODE 5
L1_TSTCLK	H4	CPU_L1TSTCLK 5
L2_TSTCLK	J2	CPU_L2TSTCLK 5
TA	N8	CPU_TA_L 9 36
TEA	T1	CPU_TEA_L 9 36
TBEN	L3	CPU_TBEN 5 9
QREQ	Y1	CPU_QREQ_L 9 36
QACK	K7	CPU_QACK_L 9 36
CKSTP_IN	F3	
CKSTP_OUT	K6	CPU_CHKSTP_OUT_L 5 39
TEST0	B10	CPU_CHKS_L 5
INT	J6	MPIC_CPU_INT_L 5 15
SMI	G8	CPU_SMI_L 5 30
MCP	B8	CPU_MCP_L 5
SRESET	G1	CPU_SRESET_L 5 39
HRESET	A3	CPU_HRESET_L 5 7 23 39
PMON_IN	E6	CPU_PMONIN_L 5
PMON_OUT	B4	NC
BMODE0	C6	CPU_EMODE0_L 7
BMODE1	C4	CPU_EMODE1_L 5
TEST6	A9	CPU_PULLDOWN 5
EXT_QUAL	B9	
TEST1	H6	CPU_PULLUP 5
TEST2	H10	
NC13	B6	NC
TEST3	D8	CPU_SRWX_L 5
TEST4	F9	
TEST5	F8	

SPARE0 A8 NC; SPARE1 D3 NC; SPARE2 H9 NC; SPARE3 J8 NC; NC1 A11 NC; NC2 B11 NC; NC3 C11 NC; NC4 D6 NC; NC5 D11 NC; NC6 E7 NC; NC7 E11 NC; NC8 F11 NC; NC9 G2 NC; NC10 G11 NC; NC11 K11 NC

RC GLITCH FILTER PLACE CLOSE TO PIN

R51 0 5% 1/16W MF 402 — CPU_DRDY_L 9 36

C77 10PF 5% 50V CERM 402

MAXBUS_SLEEP 5 7 9 16 17 23 34 38

BBANG

4700HM FOR BOOT BANGER — R19 470 5% 1/16W MF 402 — 39 23 5 JTAG_CPU_TRST_L

NO_BBANG — R23 200 5% 1/16W MF 402

MPC7450 MAXBUS

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II NOT TO REPRODUCE OR COPY IT

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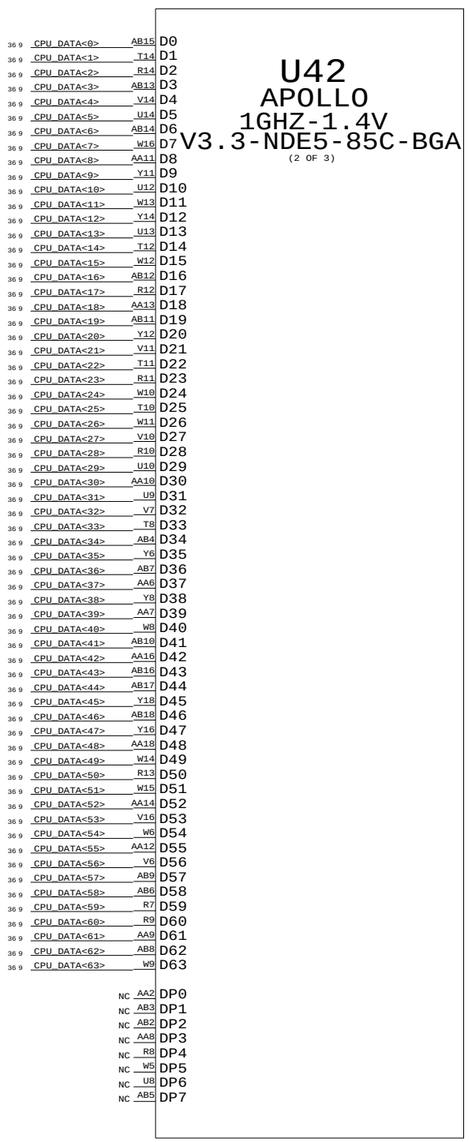
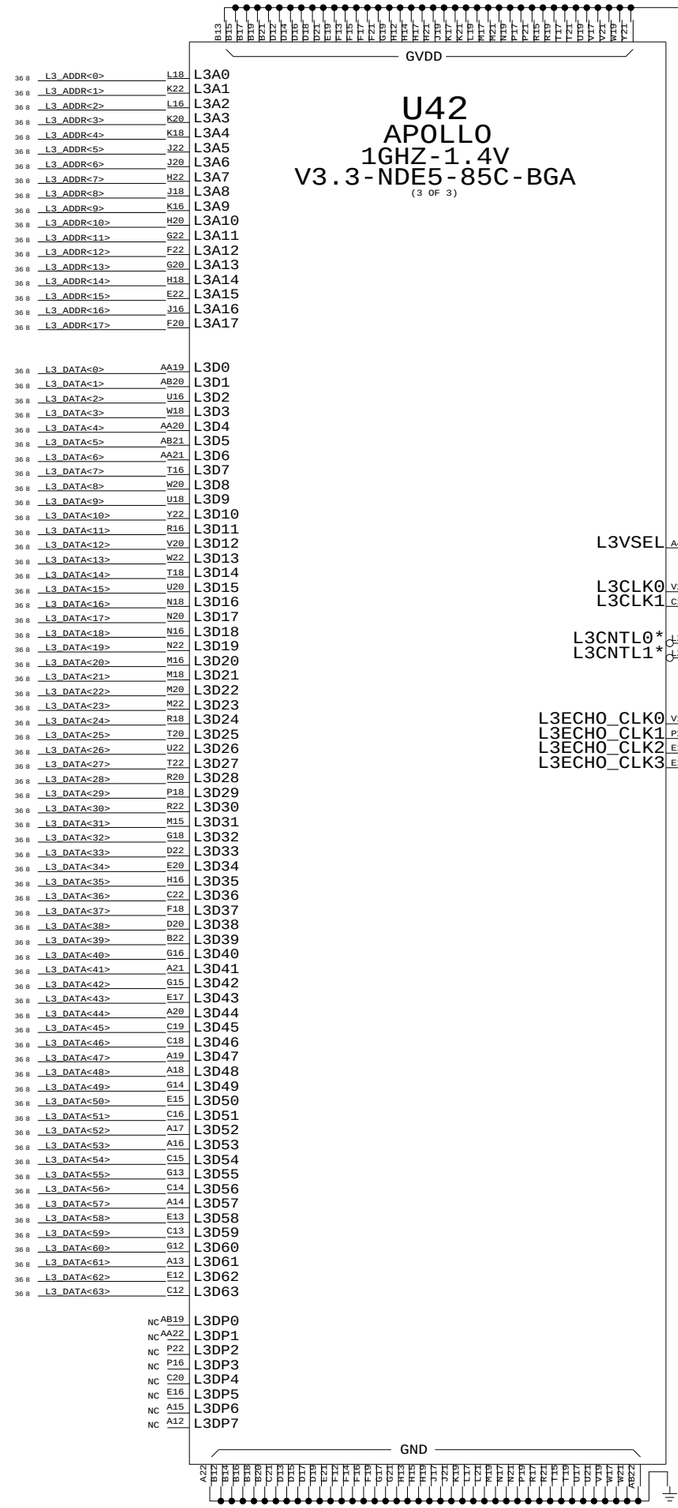
APPLE COMPUTER INC.

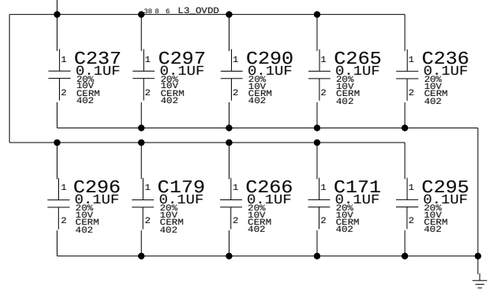
SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 5 OF 44	





L3 DECOUPLING CAPS

PLACE 1 EACH NEAR PINS B15, D12, E19, F15, H17, K17, M19, R15, T17, AND V21 OF CPU

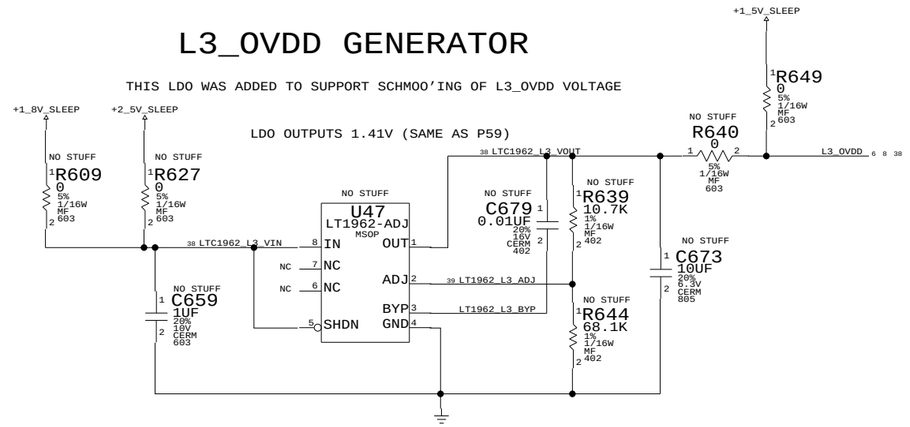


NO STUFF ALL IF NOT USED BY PVT!!!

L3_OVDD GENERATOR

THIS LDO WAS ADDED TO SUPPORT SCHMOO'ING OF L3_OVDD VOLTAGE

LDO OUTPUTS 1.41V (SAME AS P59)



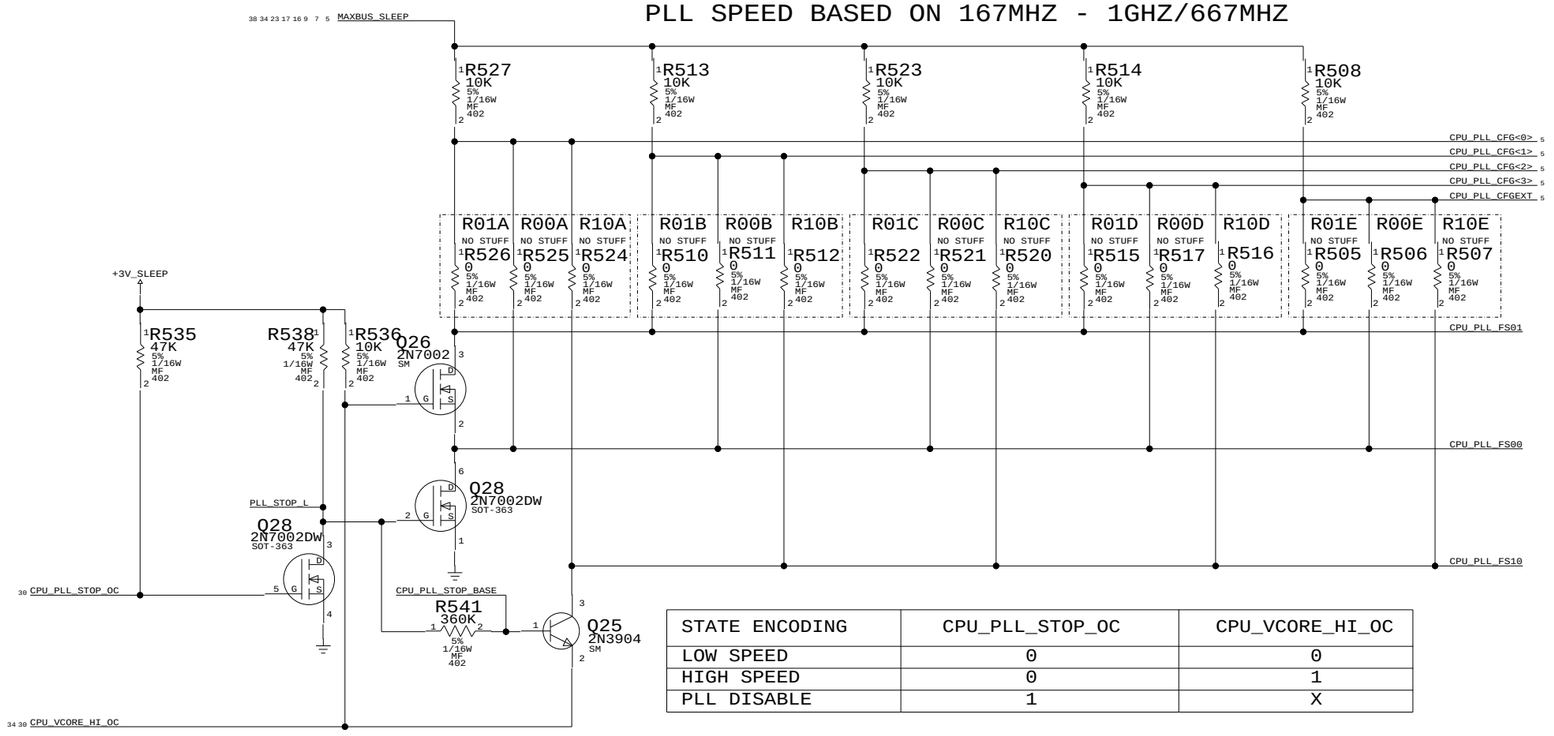
MPC7450 - L3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY

PLL SPEED BASED ON 167MHZ - 1GHZ/667MHZ



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

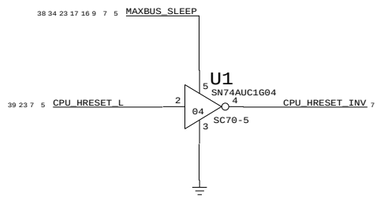
CPU FREQUENCY CONFIGURATION

APOLLO REV 3.0

MULTIPLIER	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ	133MHZ	CPU_PLL_CFG E	ABCD HEX
(Bus-to-Core)	(MHZ)			
0.0X	PLL OFF		0	1111 0F
1.0X	PLL BYPASS		0	0011 03
2.0X	333	267	0	0100 04
3.0X	500	400	0	1000 08
4.0X	667	533	0	1010 0A
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
8.5X	1417	1133	0	0110 06
9.0X	1500	1200	1	0111 17
9.5X	1583	1267	0	0111 07
10.0X	1667	1333	1	1010 1A
10.5X	1750	1400	1	1000 18
11.0X	1833	1467	1	1001 19
11.5X	1917	1533	0	0000 00
12.0X	2000	1600	1	1011 1B
12.5X	2083	1667	1	1111 1F
13.0X	2167	1733	1	0101 15
13.5X	2250	1800	0	1110 0E
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D
17.0X	2833	2267	1	0000 10
18.0X	3000	2400	1	0010 12
20.0X	3333	2667	1	0011 13
21.0X	3500	2800	1	0100 14
24.0X	4000	3200	1	0110 16
28.0X	4667	3733	1	1110 1E

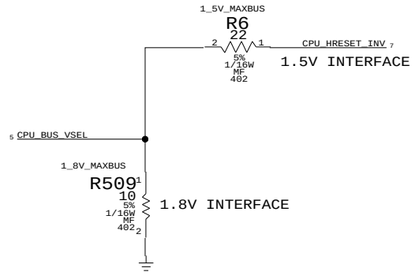
CPU CONFIGURATION

INVERTED HRESET_L

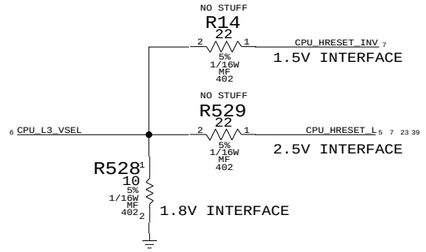


DESKTOP HAD PROBLEM USING
INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

MAXBUS VSEL



L3 VSEL



BUSTYPE SELECT

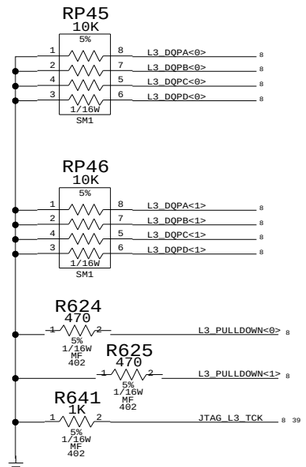
APOLLO ONLY SUPPORTS MAXBUS

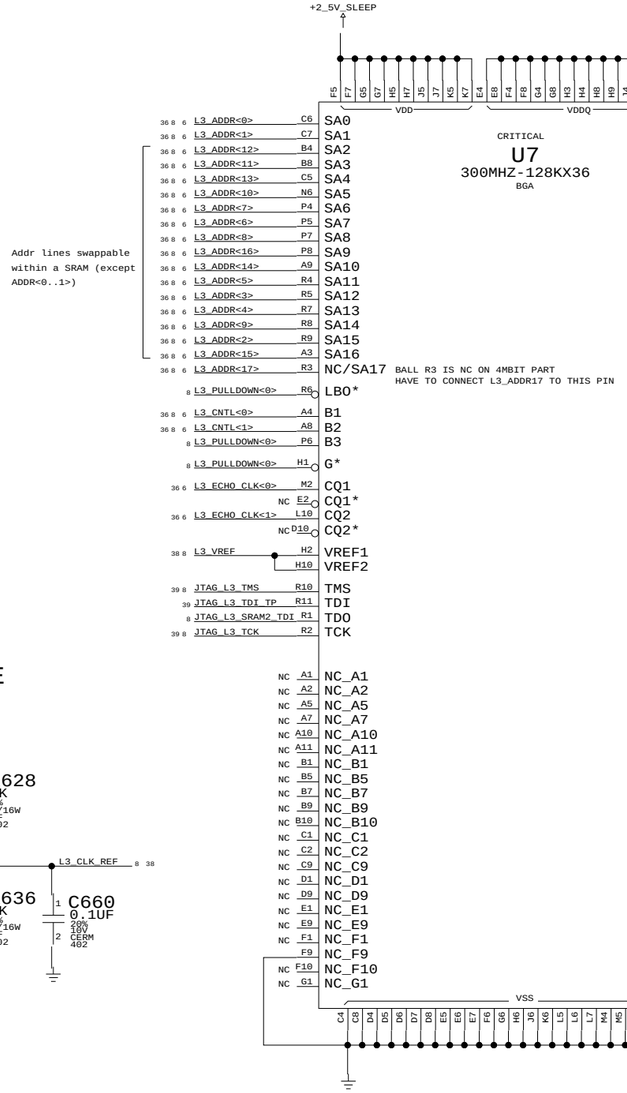
SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE
CPU_L3_VSEL (PROCESSOR)	CPU_HRESET_L or INT. PU	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

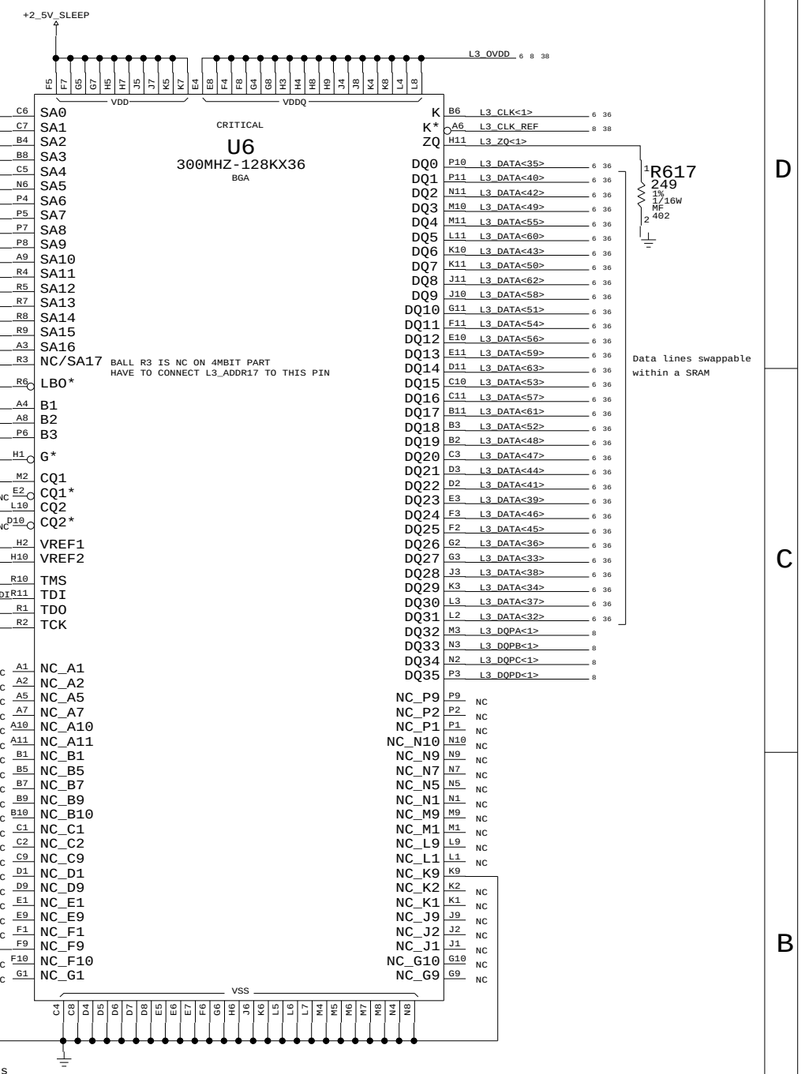
CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 7 OF 44	

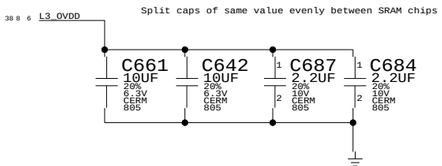






L3 REFERENCE VOLTAGE

SAMSUNG VERIFIED THAT ALL NC PINS ARE
NOT CONNECTED IN THE SUBSTRATE
BALL F9, K9 CONNECTED TO GND
SO BYPASS CAP CAN BE PLACED
DIRECTLY UNDERNEATH THE CHIPS



L3 CACHE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 8 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R557 NO STUFF 10K	R96 NO STUFF 10K	R87 NO STUFF 10K	R111 NO STUFF 10K	R121 NO STUFF 10K	R134 NO STUFF 10K	R565 NO STUFF 10K	R133 NO STUFF 10K
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
R97 10K	R558 10K	R554 10K	R571 10K	R578 10K	R586 10K	R103 10K	R587 10K
PCI_TRDY_ENABLE_L (PCI) 1: TRDY output (PCI)	0: Analyzerclk Enable 1: Active	0: PCI_TRDY_L Push Pull 1: Active low	0: ExtPLL_VDDA_Pdl 1: Active low	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

R86 NO STUFF 10K	R102 NO STUFF 10K	R119 NO STUFF 10K	R95 NO STUFF 10K	R139 NO STUFF 10K	R132 NO_SSCG 10K	R110 NO STUFF 10K	R120 NO STUFF 10K
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>
R555 NO_SSCG 10K	R566 NO STUFF 10K	R579 NO STUFF 10K	R559 NO STUFF 10K	R595 NO STUFF 10K	R588 SSCG 10K	R572 NO STUFF 10K	R580 NO STUFF 10K
Spare	Spare	BIT2	BIT1	BIT0	0: Internal SpreadEn 1: Active	0: PCI Source Clock 0: PLL4 (NO SPREAD)	1: PCI Source Clock 0: PLL5 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

R94 SSCG 10K	R85 SSCG 10K	R118 NO STUFF 10K	R109 NO STUFF 10K	R117 NO STUFF 10K	R101 NO STUFF 10K	R138 NO STUFF 10K	R131 NO STUFF 10K
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>
R560 NO_SSCG 10K	R556 NO_SSCG 10K	R582 NO STUFF 10K	R573 NO STUFF 10K	R581 NO STUFF 10K	R567 NO STUFF 10K	R596 NO STUFF 10K	R589 NO STUFF 10K
BUF_REF_CLK_OUTEnable_L 0: Active 1: Active	0: PLL4ExtSrc 1: External source	Spare	Spare	BIT2	BIT1	BIT0	Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R178 4.7 5% 1/16W MF 402
C291 0.22UF 20% 6.3V CERM 402
+1.5V_INTREPID_PLL → +1.5V_INTREPID_PLL7

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCIISPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

VDD15A_7 (PLL6) H26

CRITICAL

U44 INTREPID-REV2.1 BGA

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER

(1 OF 9)

CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	

MAXBUS INTERFACE

CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - ?
			NO BUS KEEPER - ?
			NO BUS KEEPER - PU
			NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	INTREPID OUTPUTS HIGH BY DEFAULT
			NO BUS KEEPER - PU

VSSA_7 (PLL6) H25

D_0	D10	CPU_DATA<0>	
D_1	G12	CPU_DATA<1>	
D_2	E11	CPU_DATA<2>	
D_3	H11	CPU_DATA<3>	
D_4	B9	CPU_DATA<4>	
D_5	B8	CPU_DATA<5>	
D_6	A9	CPU_DATA<6>	
D_7	A8	CPU_DATA<7>	
D_8	E12	CPU_DATA<8>	
D_9	D11	CPU_DATA<9>	
D_10	B10	CPU_DATA<10>	
D_11	J13	CPU_DATA<11>	
D_12	A10	CPU_DATA<12>	
D_13	D12	CPU_DATA<13>	
D_14	E13	CPU_DATA<14>	
D_15	G13	CPU_DATA<15>	
D_16	B11	CPU_DATA<16>	
D_17	D13	CPU_DATA<17>	
D_18	A11	CPU_DATA<18>	
D_19	G14	CPU_DATA<19>	
D_20	H14	CPU_DATA<20>	
D_21	E14	CPU_DATA<21>	
D_22	B12	CPU_DATA<22>	
D_23	G15	CPU_DATA<23>	
D_24	B13	CPU_DATA<24>	
D_25	H15	CPU_DATA<25>	
D_26	D14	CPU_DATA<26>	
D_27	B14	CPU_DATA<27>	
D_28	A12	CPU_DATA<28>	
D_29	G16	CPU_DATA<29>	
D_30	E15	CPU_DATA<30>	
D_31	J16	CPU_DATA<31>	
D_32	D15	CPU_DATA<32>	
D_33	A14	CPU_DATA<33>	
D_34	A13	CPU_DATA<34>	
D_35	D16	CPU_DATA<35>	
D_36	E16	CPU_DATA<36>	
D_37	G17	CPU_DATA<37>	
D_38	B15	CPU_DATA<38>	
D_39	H17	CPU_DATA<39>	
D_40	A15	CPU_DATA<40>	
D_41	B16	CPU_DATA<41>	
D_42	E17	CPU_DATA<42>	
D_43	A16	CPU_DATA<43>	
D_44	J18	CPU_DATA<44>	
D_45	H18	CPU_DATA<45>	
D_46	D17	CPU_DATA<46>	
D_47	G18	CPU_DATA<47>	
D_48	A17	CPU_DATA<48>	
D_49	B17	CPU_DATA<49>	
D_50	E18	CPU_DATA<50>	
D_51	B18	CPU_DATA<51>	
D_52	D18	CPU_DATA<52>	
D_53	A18	CPU_DATA<53>	
D_54	A19	CPU_DATA<54>	
D_55	H19	CPU_DATA<55>	
D_56	B19	CPU_DATA<56>	
D_57	J19	CPU_DATA<57>	
D_58	A20	CPU_DATA<58>	
D_59	D19	CPU_DATA<59>	
D_60	E19	CPU_DATA<60>	
D_61	G19	CPU_DATA<61>	
D_62	B20	CPU_DATA<62>	
D_63	G20	CPU_DATA<63>	
DBG	A30	CPU_DBG_L	
DRDY	G28	CPU_DRDY_L	
DTI_0	K25	CPU_DTI<0>	
DTI_1	D29	CPU_DTI<1>	
DTI_2	B30	CPU_DTI<2>	
TA	E27	CPU_TA_L	
TEA	E28	CPU_TEA_L	

R152 249 1% 1/16W MF 402
R104 0 5% 1/16W MF 402 (SYSCLK_CPU)
R98 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT	R122 0	INT_CPUFB_OUT_SHORT	R168 0	INT_CPUFB_OUT_NORM
			R161 NO STUFF 0	INT_CPUFB_LONG
INT_CPUFB_IN	R176 NO STUFF 0		R177 0	INT_CPUFB_IN_NORM
	R162 0		R151 NO STUFF 0	

All 5% 1/16W MF 402

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP22 10K
CPU_TA_L	RP22 10K
CPU_ARTRY_L	RP22 10K
CPU_BR_L	RP24 10K
CPU_HIT_L	RP25 10K
CPU_DRDY_L	RP24 10K
CPU_TEA_L	RP24 10K
CPU_AACK_L	RP24 10K
CPU_DBG_L	RP25 10K
CPU_BG_L	RP22 10K
CPU_QREQ_L	RP25 10K

All 5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R100 NO STUFF 10K	R116 NO STUFF 10K	R130 NO STUFF 10K	R93 NO STUFF 10K	R92 NO STUFF 10K	R108 NO STUFF 10K	R129 NO STUFF 10K	R137 NO STUFF 10K
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>
R568 10K	R583 10K	R590 10K	R561 10K	R562 10K	R574 10K	R591 NO STUFF 10K	R597 10K
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 0: GPIOs 1:	PCI1_REQ1_L / PCI1_GNT1_L 0: GPIOs 1:	PCI1_REQ0_L / PCI1_GNT0_L 0: GPIOs 1:	Firewire PHY interface 0: Legacy interface 1: B-Mode interface	Processor Bus Mode 0: 60X bus 1: (G3)

All 5% 1/16W MF 402

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 9 OF 44	

CR-10

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

CRITICAL

U44
INTREPID-REV2.1
BGA
(2 OF 9)

DDR MEMORY INTERFACE

MEM_DATA<0>	AK32	DDR_DATA_0	
MEM_DATA<1>	AK33	DDR_DATA_1	
MEM_DATA<2>	AK31	DDR_DATA_2	
MEM_DATA<3>	AK35	DDR_DATA_3	
MEM_DATA<4>	AK36	DDR_DATA_4	
MEM_DATA<5>	AJ32	DDR_DATA_5	
MEM_DATA<6>	AJ34	DDR_DATA_6	
MEM_DATA<7>	AJ36	DDR_DATA_7	
MEM_DATA<8>	AG33	DDR_DATA_8	
MEM_DATA<9>	AG35	DDR_DATA_9	
MEM_DATA<10>	AH35	DDR_DATA_10	
MEM_DATA<11>	AG36	DDR_DATA_11	
MEM_DATA<12>	AH36	DDR_DATA_12	
MEM_DATA<13>	AH32	DDR_DATA_13	
MEM_DATA<14>	AG32	DDR_DATA_14	
MEM_DATA<15>	AG31	DDR_DATA_15	
MEM_DATA<16>	AE32	DDR_DATA_16	
MEM_DATA<17>	AF35	DDR_DATA_17	
MEM_DATA<18>	AF36	DDR_DATA_18	
MEM_DATA<19>	AE36	DDR_DATA_19	
MEM_DATA<20>	AE35	DDR_DATA_20	
MEM_DATA<21>	AE33	DDR_DATA_21	
MEM_DATA<22>	AD36	DDR_DATA_22	
MEM_DATA<23>	AD35	DDR_DATA_23	
MEM_DATA<24>	AA36	DDR_DATA_24	
MEM_DATA<25>	AA35	DDR_DATA_25	
MEM_DATA<26>	AA33	DDR_DATA_26	
MEM_DATA<27>	AB36	DDR_DATA_27	
MEM_DATA<28>	AB35	DDR_DATA_28	
MEM_DATA<29>	AC36	DDR_DATA_29	
MEM_DATA<30>	AA32	DDR_DATA_30	
MEM_DATA<31>	AB33	DDR_DATA_31	
MEM_DATA<32>	V36	DDR_DATA_32	
MEM_DATA<33>	U33	DDR_DATA_33	
MEM_DATA<34>	U32	DDR_DATA_34	
MEM_DATA<35>	V35	DDR_DATA_35	
MEM_DATA<36>	T36	DDR_DATA_36	
MEM_DATA<37>	U36	DDR_DATA_37	
MEM_DATA<38>	U35	DDR_DATA_38	
MEM_DATA<39>	T35	DDR_DATA_39	
MEM_DATA<40>	P33	DDR_DATA_40	
MEM_DATA<41>	R36	DDR_DATA_41	
MEM_DATA<42>	P35	DDR_DATA_42	
MEM_DATA<43>	P36	DDR_DATA_43	
MEM_DATA<44>	R35	DDR_DATA_44	
MEM_DATA<45>	R33	DDR_DATA_45	
MEM_DATA<46>	R32	DDR_DATA_46	
MEM_DATA<47>	N35	DDR_DATA_47	
MEM_DATA<48>	M36	DDR_DATA_48	
MEM_DATA<49>	L35	DDR_DATA_49	
MEM_DATA<50>	M35	DDR_DATA_50	
MEM_DATA<51>	M33	DDR_DATA_51	
MEM_DATA<52>	L36	DDR_DATA_52	
MEM_DATA<53>	N33	DDR_DATA_53	
MEM_DATA<54>	M32	DDR_DATA_54	
MEM_DATA<55>	J32	DDR_DATA_55	
MEM_DATA<56>	J33	DDR_DATA_56	
MEM_DATA<57>	J35	DDR_DATA_57	
MEM_DATA<58>	K32	DDR_DATA_58	
MEM_DATA<59>	K33	DDR_DATA_59	
MEM_DATA<60>	J36	DDR_DATA_60	
MEM_DATA<61>	K36	DDR_DATA_61	
MEM_DATA<62>	K35	DDR_DATA_62	
MEM_DATA<63>		DDR_DATA_63	

H35	MEM_ADDR<0>	DDR_A_0	
G35	MEM_ADDR<1>	DDR_A_1	
G36	MEM_ADDR<2>	DDR_A_2	
F36	MEM_ADDR<3>	DDR_A_3	
F35	MEM_ADDR<4>	DDR_A_4	
E35	MEM_ADDR<5>	DDR_A_5	
E36	MEM_ADDR<6>	DDR_A_6	
G32	MEM_ADDR<7>	DDR_A_7	
D36	MEM_ADDR<8>	DDR_A_8	
H36	MEM_ADDR<9>	DDR_A_9	
G33	MEM_ADDR<10>	DDR_A_10	
H33	MEM_ADDR<11>	DDR_A_11	
D35	MEM_ADDR<12>	DDR_A_12	
L30	MEM_BA<0>	DDR_BA_0	
M29	MEM_BA<1>	DDR_BA_1	
AN34	MEM_CS_L<0>	DDRCS_0	
AN36	MEM_CS_L<1>	DDRCS_1	
AL35	MEM_CS_L<2>	DDRCS_2	
AL33	MEM_CS_L<3>	DDRCS_3	
AJ31	MEM_DQS<0>	DDR_DQS_0	
AH31	MEM_DQS<1>	DDR_DQS_1	
AD32	MEM_DQS<2>	DDR_DQS_2	
AB30	MEM_DQS<3>	DDR_DQS_3	
V36	MEM_DQS<4>	DDR_DQS_4	
P32	MEM_DQS<5>	DDR_DQS_5	
N29	MEM_DQS<6>	DDR_DQS_6	
L32	MEM_DQS<7>	DDR_DQS_7	
AJ33	MEM_DQM<0>	DDR_DM_0	
AH33	MEM_DQM<1>	DDR_DM_1	
AD33	MEM_DQM<2>	DDR_DM_2	
AC35	MEM_DQM<3>	DDR_DM_3	
T35	MEM_DQM<4>	DDR_DM_4	
T33	MEM_DQM<5>	DDR_DM_5	
N32	MEM_DQM<6>	DDR_DM_6	
L33	MEM_DQM<7>	DDR_DM_7	
L29	MEM_RAS_L	DDRRAS	
H32	MEM_CAS_L	DDRCAS	
K30	MEM_WE_L	DDRWE	
AN35	MEM_CKE<0>	DDRCKE0	
AM35	MEM_CKE<1>	DDRCKE1	
AM36	MEM_CKE<2>	DDRCKE2	
AL36	MEM_CKE<3>	DDRCKE3	
AB32	MEM_MUXSEL_H<0>	DDR_SELHI_0	
AE29	MEM_MUXSEL_H<1>	DDR_SELHI_1	
N30	MEM_MUXSEL_L<0>	DDR_SELLO_0	
T32	MEM_MUXSEL_L<1>	DDR_SELLO_1	
Y32	SYSCLK_DDRCLK_A0_UF	DDR_MCLK_0_P	
Y33	SYSCLK_DDRCLK_A0_L_UF	DDR_MCLK_0_N	
Y35	SYSCLK_DDRCLK_A1_UF	DDR_MCLK_1_P	
Y36	SYSCLK_DDRCLK_A1_L_UF	DDR_MCLK_1_N	
Y30	INT_DDRCLK2_P_TP	DDR_MCLK_2_P	
W30	INT_DDRCLK2_N_TP	DDR_MCLK_2_N	
W32	SYSCLK_DDRCLK_B0_UF	DDR_MCLK_3_P	
W33	SYSCLK_DDRCLK_B0_L_UF	DDR_MCLK_3_N	
V33	SYSCLK_DDRCLK_B1_UF	DDR_MCLK_4_P	
V32	SYSCLK_DDRCLK_B1_L_UF	DDR_MCLK_4_N	
W35	INT_DDRCLK5_P_TP	DDR_MCLK_5_P	
W36	INT_DDRCLK5_N_TP	DDR_MCLK_5_N	
AA22	INT_MEM_REF_H	DDR_REF	
Y22	INT_MEM_VREF	DDR_VREF_0	
T22		DDR_VREF_1	

’0’ & ’1’ GO TO SLOT A
’2’ & ’3’ GO TO SLOT B

’0’S ARE SAME POLARITY (ACTIVE-LO)
’1’S ARE SAME POLARITY (ACTIVE-HI)

R154 1K 1% 1/16W MF 402

MEM_VREF

+2_5V_INTREPID

R153 10K 1% 1/16W MF 402

R144 10K 1% 1/16W MF 402

C224 0.1UF 20% 10V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP31	4	5
SYSCLK_DDRCLK_A1_L_UF	RP31	3	6
SYSCLK_DDRCLK_A0_UF	RP32	1	8
SYSCLK_DDRCLK_A0_L_UF	RP32	2	7
SYSCLK_DDRCLK_B1_UF	RP31	2	7
SYSCLK_DDRCLK_B1_L_UF	RP31	1	8
SYSCLK_DDRCLK_B0_UF	RP32	3	6
SYSCLK_DDRCLK_B0_L_UF	RP32	4	5

RP31 22 5% 1/16W SM1
RP32 22 5% 1/16W SM1

SYSCLK_DDRCLK_A1	RP31	4	5
SYSCLK_DDRCLK_A1_L	RP31	3	6
SYSCLK_DDRCLK_A0	RP32	1	8
SYSCLK_DDRCLK_A0_L	RP32	2	7
SYSCLK_DDRCLK_B1	RP31	2	7
SYSCLK_DDRCLK_B1_L	RP31	1	8
SYSCLK_DDRCLK_B0	RP32	3	6
SYSCLK_DDRCLK_B0_L	RP32	4	5

CS

MEM_CS_L<0>	RP34	1	8
MEM_CS_L<1>	RP34	3	6
MEM_CS_L<2>	RP33	4	5
MEM_CS_L<3>	RP33	2	7

RP34 22 5% 1/16W SM1
RP33 22 5% 1/16W SM1

RAM_CS_L<0>	RP34	1	8
RAM_CS_L<1>	RP34	3	6
RAM_CS_L<2>	RP33	4	5
RAM_CS_L<3>	RP33	2	7

CKE

MEM_CKE<0>	RP34	2	7
MEM_CKE<1>	RP34	4	5
MEM_CKE<2>	RP33	1	8
MEM_CKE<3>	RP33	3	6

RP34 22 5% 1/16W SM1
RP33 22 5% 1/16W SM1

RAM_CKE<0>	RP34	2	7
RAM_CKE<1>	RP34	4	5
RAM_CKE<2>	RP33	1	8
RAM_CKE<3>	RP33	3	6

ADDR

MEM_ADDR<0>	RP30	1	8
MEM_ADDR<1>	RP26	1	8
MEM_ADDR<2>	RP26	2	7
MEM_ADDR<3>	RP26	4	5
MEM_ADDR<4>	RP26	3	6
MEM_ADDR<5>	RP29	1	8
MEM_ADDR<6>	RP29	2	7
MEM_ADDR<7>	RP30	3	6
MEM_ADDR<8>	RP29	4	5
MEM_ADDR<9>	RP30	2	7
MEM_ADDR<10>	RP30	4	5
MEM_ADDR<11>	RP27	4	5
MEM_ADDR<12>	RP29	3	6

RP30 22 5% 1/16W SM1
RP26 22 5% 1/16W SM1
RP29 22 5% 1/16W SM1
RP27 22 5% 1/16W SM1

RAM_ADDR<0>	RP30	1	8
RAM_ADDR<1>	RP26	1	8
RAM_ADDR<2>	RP26	2	7
RAM_ADDR<3>	RP26	4	5
RAM_ADDR<4>	RP26	3	6
RAM_ADDR<5>	RP29	1	8
RAM_ADDR<6>	RP29	2	7
RAM_ADDR<7>	RP30	3	6
RAM_ADDR<8>	RP29	4	5
RAM_ADDR<9>	RP30	2	7
RAM_ADDR<10>	RP30	4	5
RAM_ADDR<11>	RP27	4	5
RAM_ADDR<12>	RP29	3	6

BA

MEM_BA<0>	RP27	2	7
MEM_BA<1>	RP27	1	8

RP27 22 5% 1/16W SM1

RAM_BA<0>	RP27	2	7
RAM_BA<1>	RP27	1	8

CNTL

MEM_WE_L	RP27	3	6
MEM_CAS_L	R199	1	2
MEM_RAS_L	R188	1	2

RP27 22 5% 1/16W SM1
R199 22 5% 1/16W MF 402
R188 22 5% 1/16W MF 402

RAM_WE_L	RP27	3	6
RAM_CAS_L	R199	1	2
RAM_RAS_L	R188	1	2

1MB BOOT ROM

+3V_MAIN

C441 2.2UF 20% 16V CERM 805
C451 0.1UF 20% 16V CERM 402
C459 0.1UF 20% 16V CERM 402

U17
FEPR-1MX8
3.3V
TSOP
OMIT

VPP 11, VCC 30, 31

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		

PCI_AD<0>	DQ0	PCI_AD<24>
PCI_AD<1>	DQ1	PCI_AD<25>
PCI_AD<2>	DQ2	PCI_AD<26>
PCI_AD<3>	DQ3	PCI_AD<27>
PCI_AD<4>	DQ4	PCI_AD<28>
PCI_AD<5>	DQ5	PCI_AD<29>
PCI_AD<6>	DQ6	PCI_AD<30>
PCI_AD<7>	DQ7	PCI_AD<31>

ROM_CS_L
ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L

GND 23, 39

+3V_MAIN

R268 10K 5% 1/16W MF 402
R312 10K 5% 1/16W MF 402
R280 1K 5% 1/16W MF 402

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1193	1	BOOTROM,P84	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R770 10K 5% 1/16W MF 402
R771 10K 5% 1/16W MF 402
R772 10K 5% 1/16W MF 402
R773 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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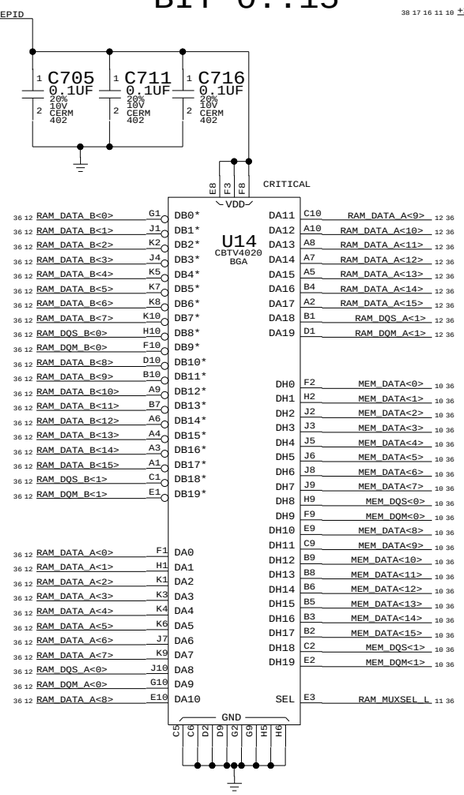
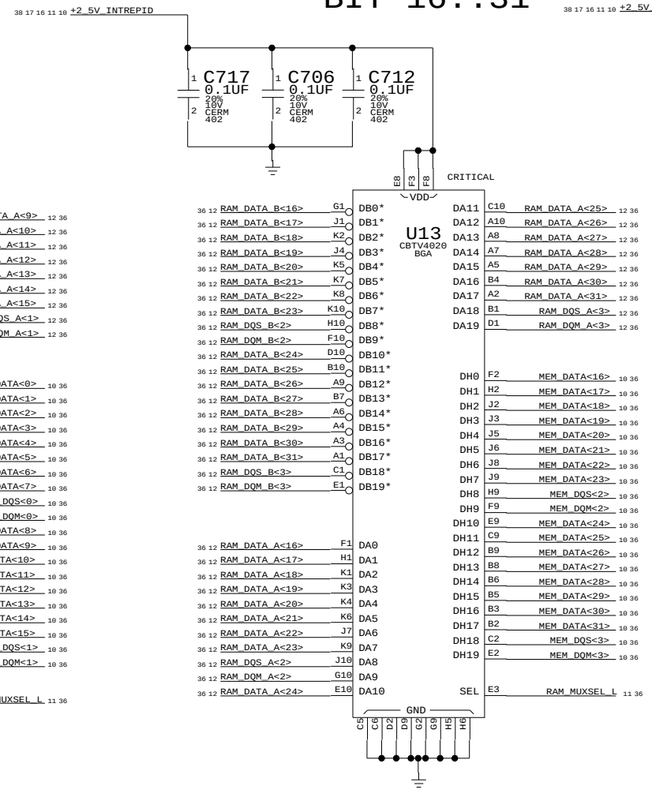
SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 10 OF 44	

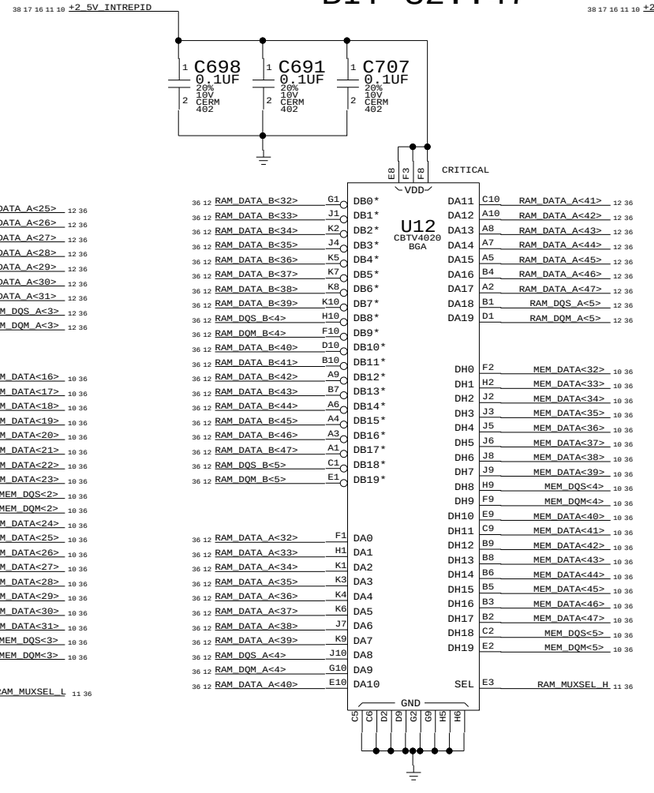
BIT 0..15



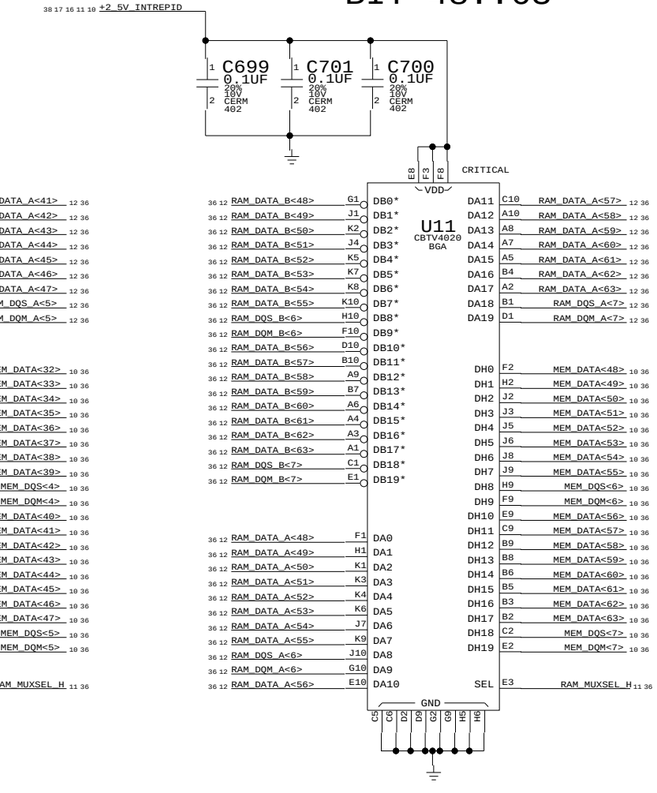
BIT 16..31



BIT 32..47



BIT 48..63



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

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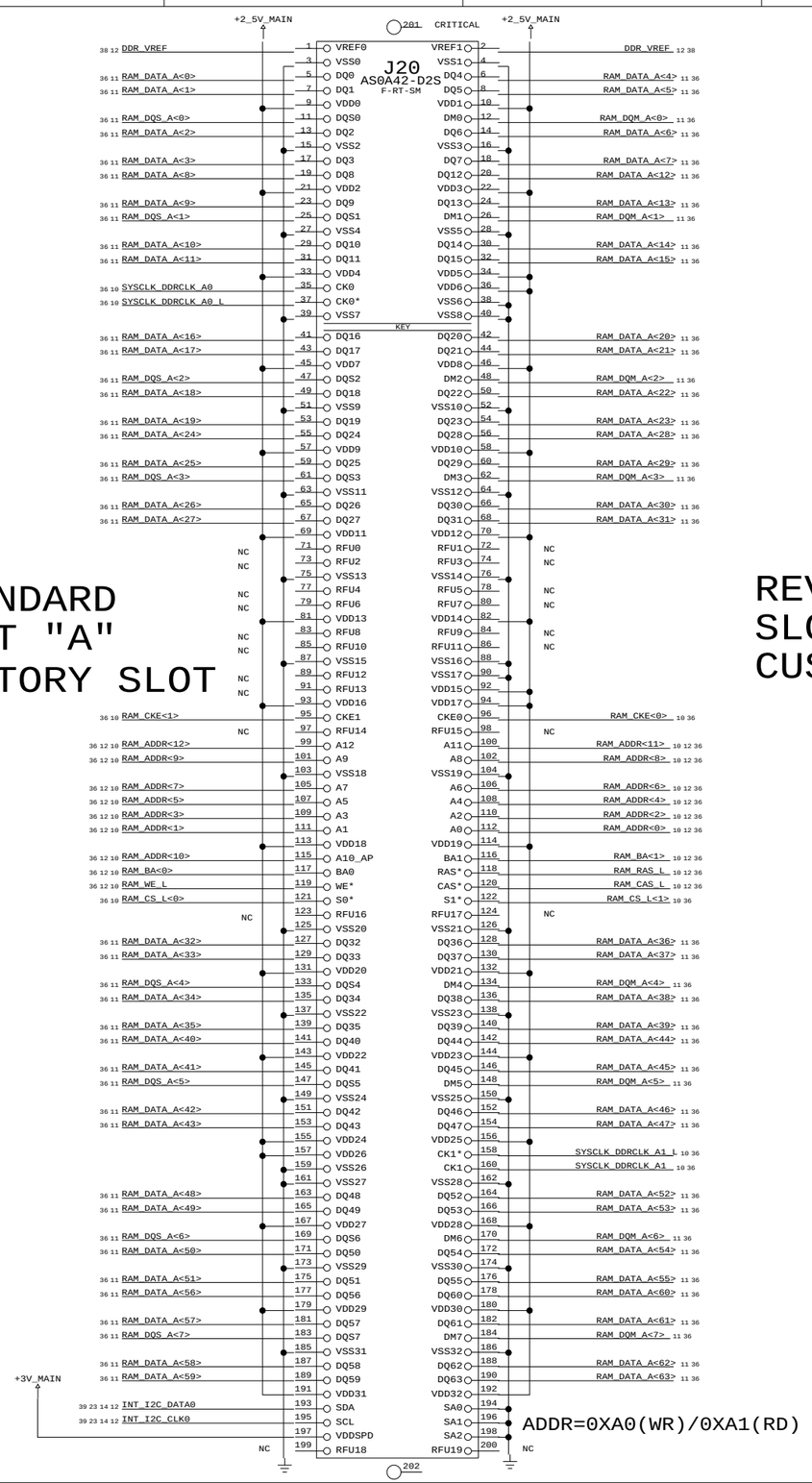
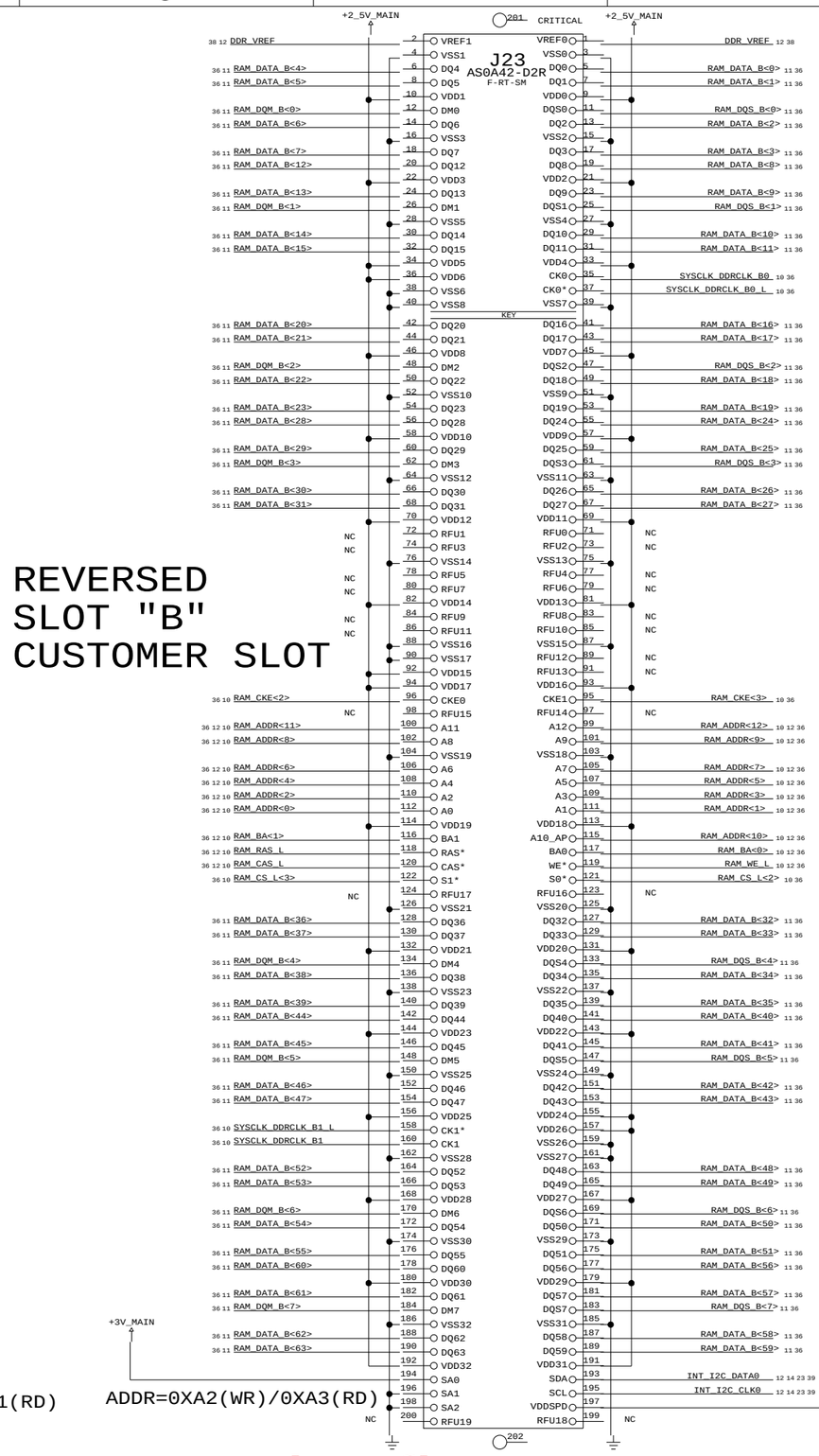
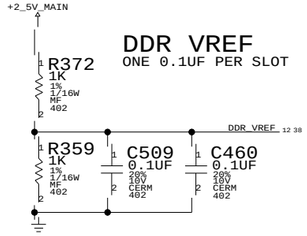
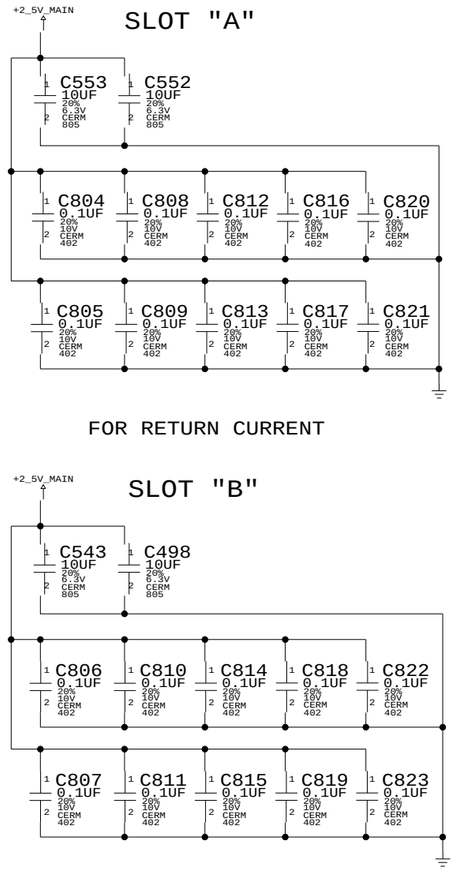


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

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SCALE: NONE	SHT 12 OF 44	

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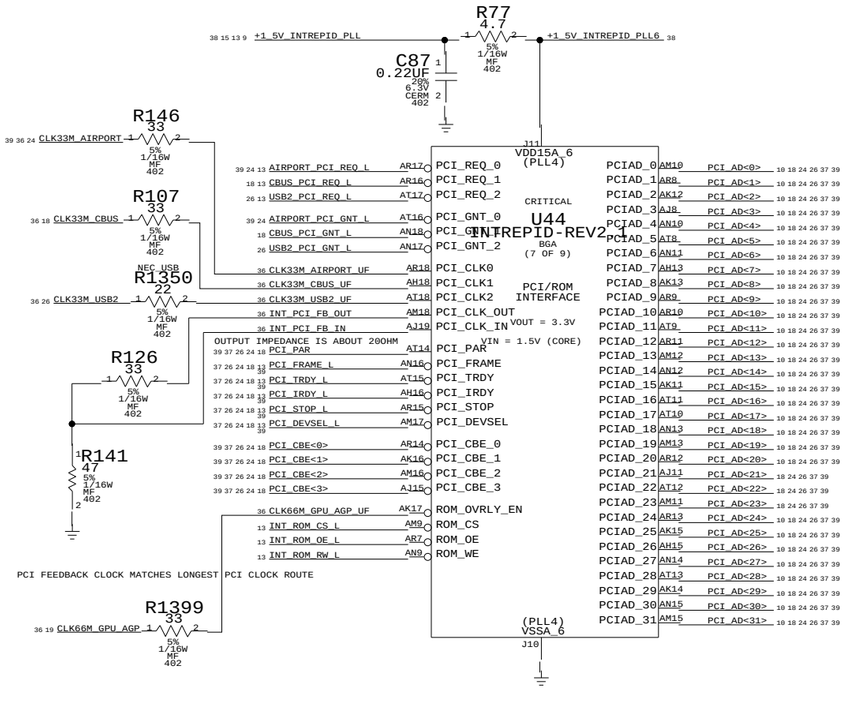
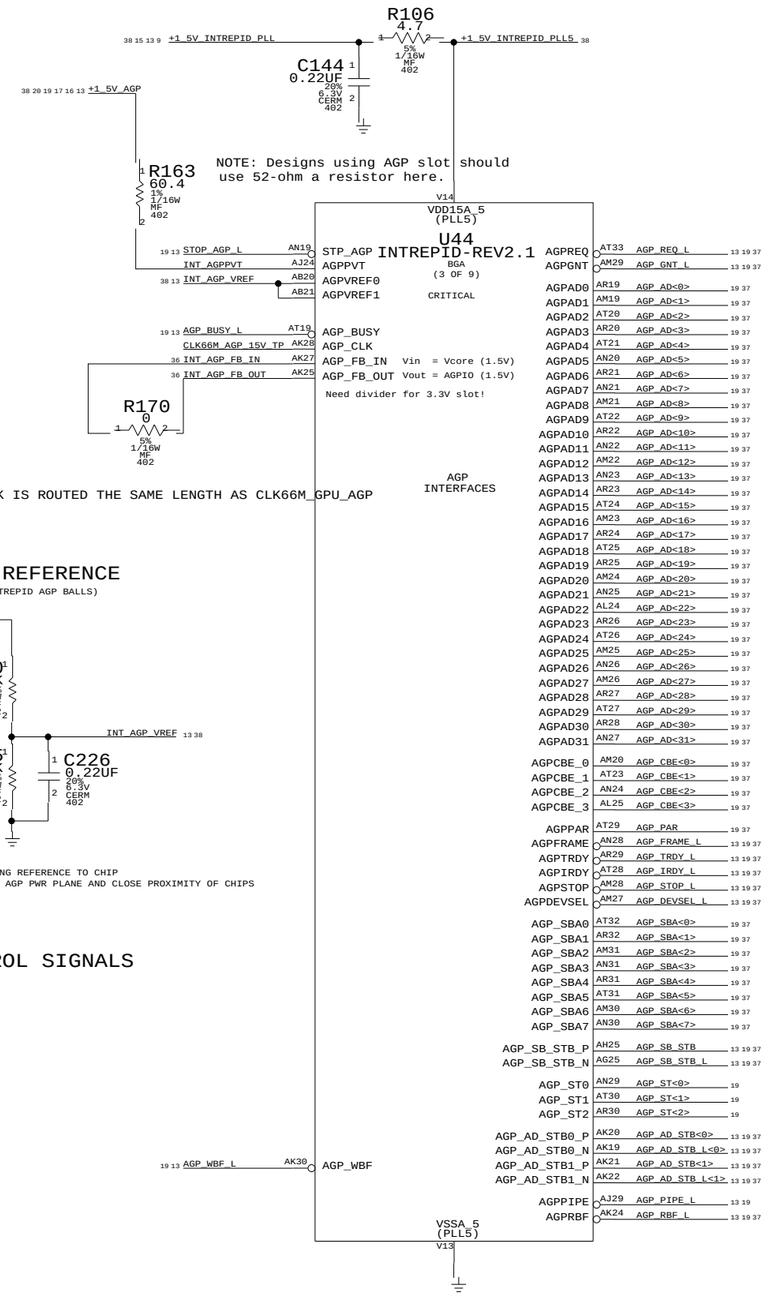
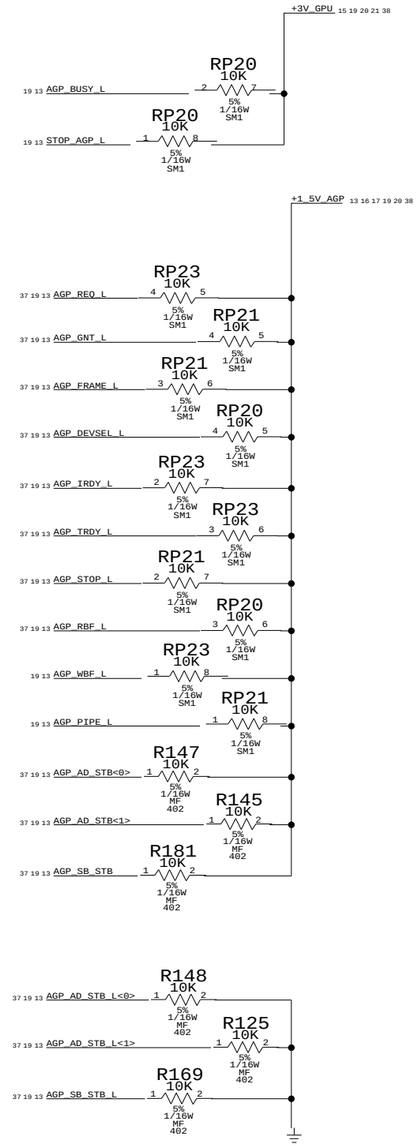




AGP PULL-UPS/PULL DOWNS

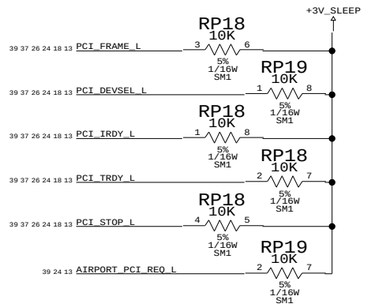


AGP I/O REFERENCE

(PLACE CLOSE TO INTREPID AGP BALLS)

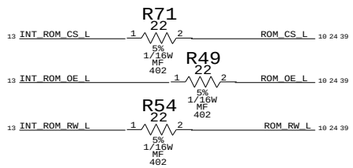
SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

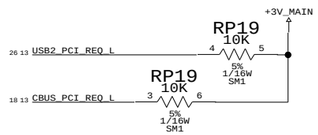
PCI PULL-UPS



SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

PLACE CLOSE TO INTREPID SIDE





USB2 AND CBUS REQ REMAINS ON
+3V_MAIN BECAUSE THESE CHIPS
ARE POWERED IN SLEEP

INTREPID AGP/PCI

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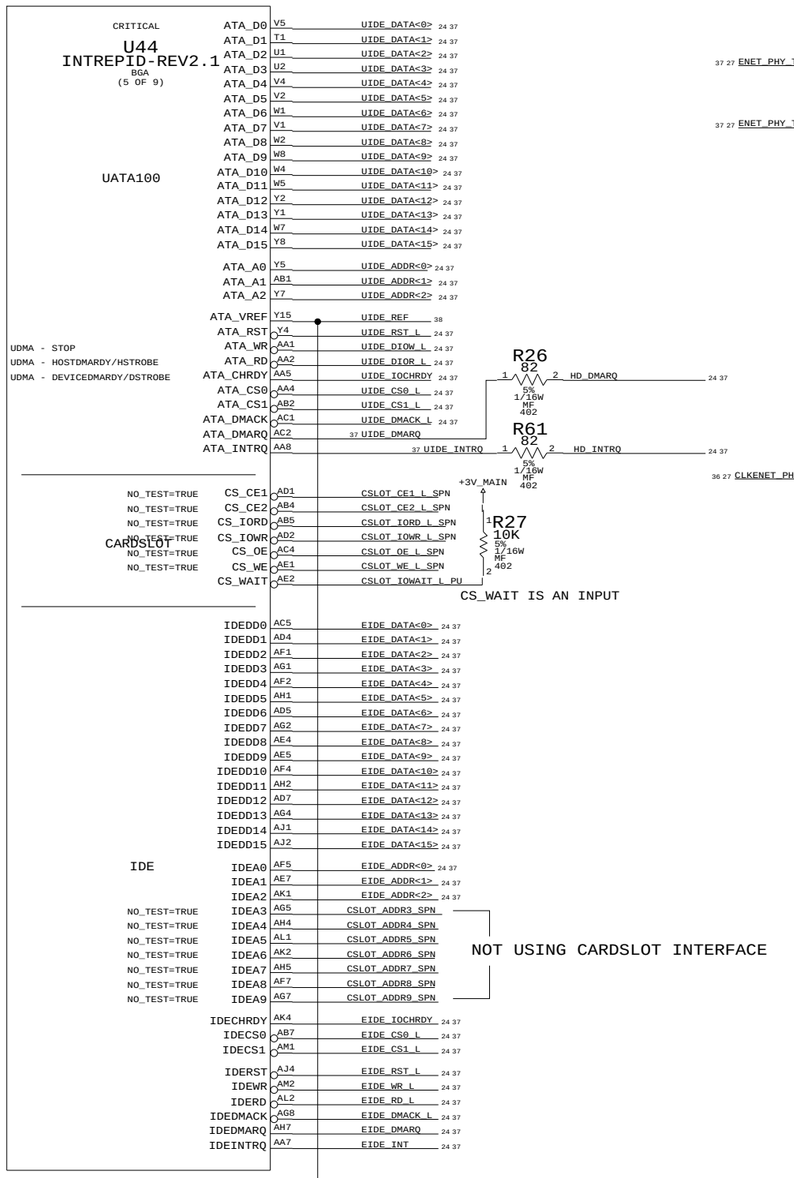
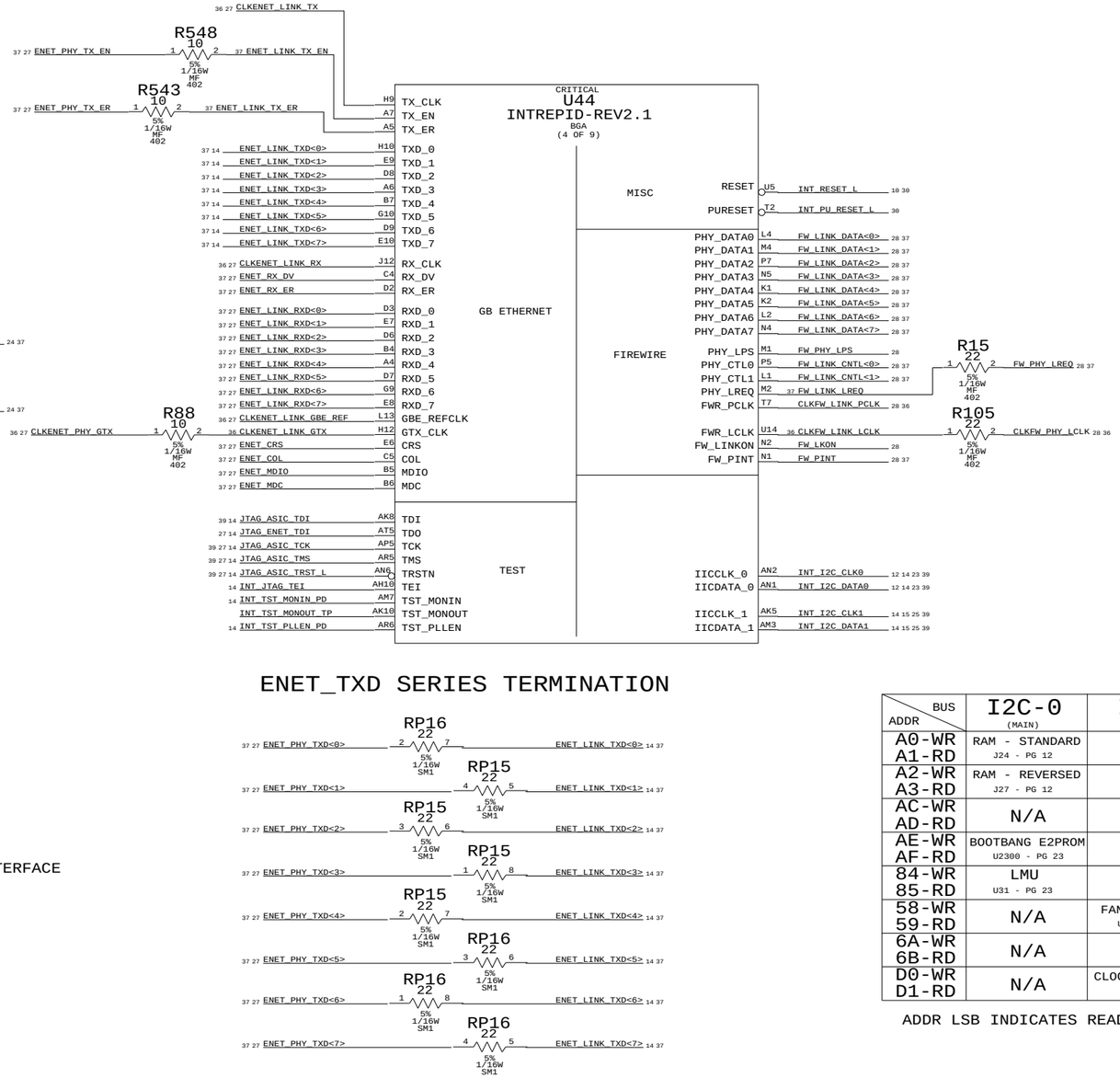
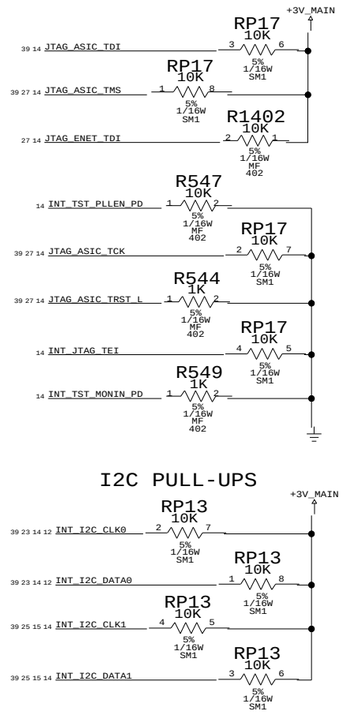
SCALE: NONE	SHT 13 OF 44	







ENET_TXD SERIES TERMINATION

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J24 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J27 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J10 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U2300 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U31 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U38 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J16 - PG 23	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

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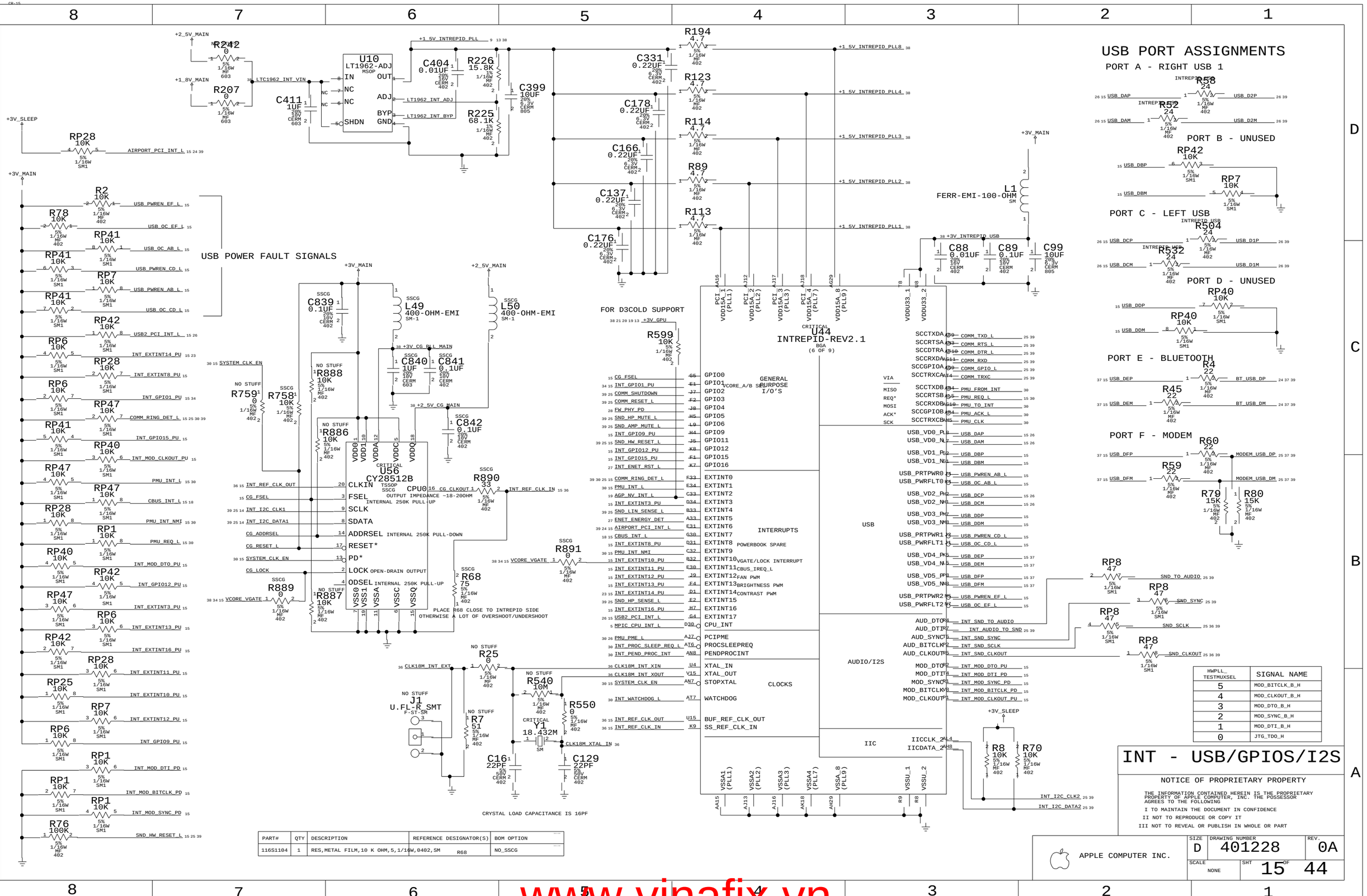
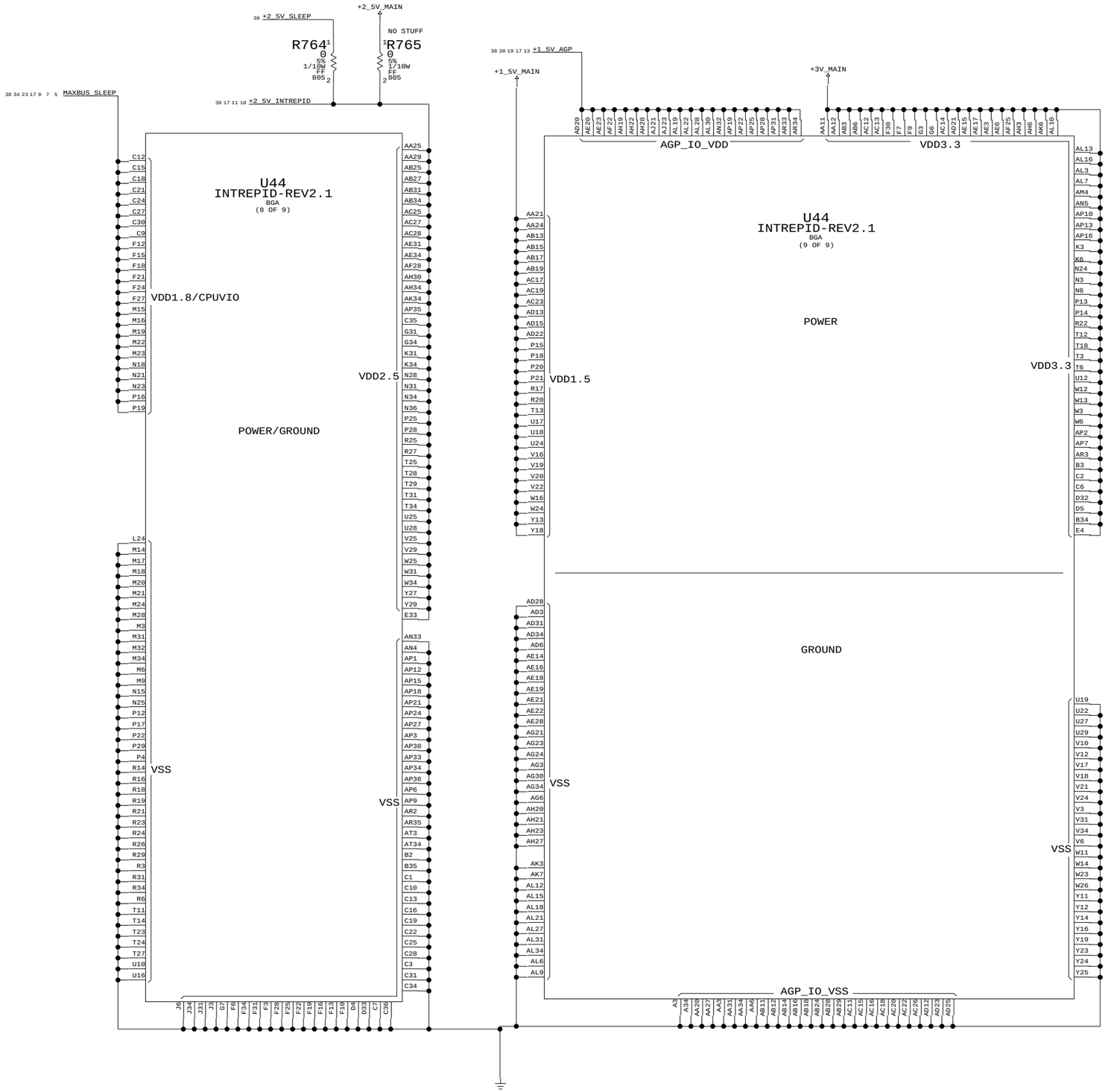
SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 14 OF 44	

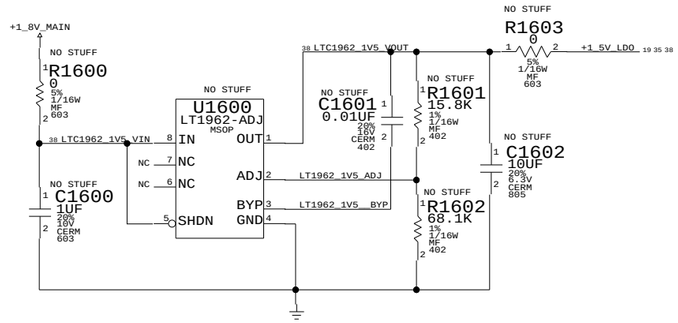


CR-16



1.5V LDO GENERATOR

THIS LDO WAS ADDED IN CASE INTREPID CORE DOES NOT RUN AT 1.5V



Intrepid Power

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D	401228	0A
SCALE: NONE	SHT 16 OF 44	

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INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

MAXBUS_SLEEP

C11 10uF 20% 6.3V CERM 805
C326 10uF 20% 6.3V CERM 805
C218 0.22uF 20% 6.3V CERM 402
C219 0.22uF 20% 6.3V CERM 402
C328 0.22uF 20% 6.3V CERM 402
C298 0.22uF 20% 6.3V CERM 402
C160 0.22uF 20% 6.3V CERM 402
C269 0.22uF 20% 6.3V CERM 402
C299 0.22uF 20% 6.3V CERM 402
C96 0.22uF 20% 6.3V CERM 402
C267 0.22uF 20% 6.3V CERM 402
C142 0.22uF 20% 6.3V CERM 402
C215 10uF 20% 6.3V CERM 805
C181 10uF 20% 6.3V CERM 805
C158 0.22uF 20% 6.3V CERM 402
C183 0.22uF 20% 6.3V CERM 402
C240 0.22uF 20% 6.3V CERM 402
C216 0.22uF 20% 6.3V CERM 402
C217 0.22uF 20% 6.3V CERM 402
C97 0.22uF 20% 6.3V CERM 402
C113 0.22uF 20% 6.3V CERM 402
C220 0.22uF 20% 6.3V CERM 402
C241 0.22uF 20% 6.3V CERM 402
C300 0.22uF 20% 6.3V CERM 402
C157 0.22uF 20% 6.3V CERM 402
C155 0.22uF 20% 6.3V CERM 402
C159 0.22uF 20% 6.3V CERM 402
C205 0.22uF 20% 6.3V CERM 402
C156 0.22uF 20% 6.3V CERM 402
C184 0.22uF 20% 6.3V CERM 402
C114 0.22uF 20% 6.3V CERM 402
C268 0.22uF 20% 6.3V CERM 402
C115 0.22uF 20% 6.3V CERM 402
C327 0.22uF 20% 6.3V CERM 402
C182 0.22uF 20% 6.3V CERM 402
C186 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

+1_5V_AGP

C336 10uF 20% 6.3V CERM 805
C210 10uF 20% 6.3V CERM 805
C334 0.22uF 20% 6.3V CERM 402
C279 0.22uF 20% 6.3V CERM 402
C249 0.22uF 20% 6.3V CERM 402
C194 0.22uF 20% 6.3V CERM 402
C333 0.22uF 20% 6.3V CERM 402
C248 0.22uF 20% 6.3V CERM 402
C229 0.22uF 20% 6.3V CERM 402
C280 0.22uF 20% 6.3V CERM 402
C357 0.22uF 20% 6.3V CERM 402
C193 0.22uF 20% 6.3V CERM 402
C262 10uF 20% 6.3V CERM 805
C374 10uF 20% 6.3V CERM 805
C207 0.22uF 20% 6.3V CERM 402
C209 0.22uF 20% 6.3V CERM 402
C246 0.22uF 20% 6.3V CERM 402
C358 0.22uF 20% 6.3V CERM 402
C335 0.22uF 20% 6.3V CERM 402
C208 0.22uF 20% 6.3V CERM 402
C311 0.22uF 20% 6.3V CERM 402
C373 0.22uF 20% 6.3V CERM 402
C310 0.22uF 20% 6.3V CERM 402
C309 0.22uF 20% 6.3V CERM 402
C230 0.22uF 20% 6.3V CERM 402
C247 0.22uF 20% 6.3V CERM 402
C228 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

+2_5V_INTREPID

C403 10uF 20% 6.3V CERM 805
C397 10uF 20% 6.3V CERM 805
C389 0.22uF 20% 6.3V CERM 402
C371 0.22uF 20% 6.3V CERM 402
C293 0.22uF 20% 6.3V CERM 402
C303 0.22uF 20% 6.3V CERM 402
C272 0.22uF 20% 6.3V CERM 402
C370 0.22uF 20% 6.3V CERM 402
C350 0.22uF 20% 6.3V CERM 402
C306 0.22uF 20% 6.3V CERM 402
C345 0.22uF 20% 6.3V CERM 402
C346 0.22uF 20% 6.3V CERM 402
C398 10uF 20% 6.3V CERM 805
C402 10uF 20% 6.3V CERM 805
C347 0.22uF 20% 6.3V CERM 402
C274 0.22uF 20% 6.3V CERM 402
C277 0.22uF 20% 6.3V CERM 402
C385 0.22uF 20% 6.3V CERM 402
C273 0.22uF 20% 6.3V CERM 402
C330 0.22uF 20% 6.3V CERM 402
C308 0.22uF 20% 6.3V CERM 402
C372 0.22uF 20% 6.3V CERM 402
C365 0.22uF 20% 6.3V CERM 402
C356 0.22uF 20% 6.3V CERM 402
C307 0.22uF 20% 6.3V CERM 402
C304 0.22uF 20% 6.3V CERM 402
C381 0.22uF 20% 6.3V CERM 402
C392 0.22uF 20% 6.3V CERM 402
C321 0.22uF 20% 6.3V CERM 402
C349 0.22uF 20% 6.3V CERM 402
C364 0.22uF 20% 6.3V CERM 402
C276 0.22uF 20% 6.3V CERM 402
C388 0.22uF 20% 6.3V CERM 402
C387 0.22uF 20% 6.3V CERM 402
C386 0.22uF 20% 6.3V CERM 402
C382 0.22uF 20% 6.3V CERM 402
C366 0.22uF 20% 6.3V CERM 402
C270 0.22uF 20% 6.3V CERM 402
C367 0.22uF 20% 6.3V CERM 402
C383 0.22uF 20% 6.3V CERM 402
C332 0.22uF 20% 6.3V CERM 402
C369 0.22uF 20% 6.3V CERM 402
C292 0.22uF 20% 6.3V CERM 402
C380 0.22uF 20% 6.3V CERM 402
C323 0.22uF 20% 6.3V CERM 402
C271 0.22uF 20% 6.3V CERM 402
C384 0.22uF 20% 6.3V CERM 402
C379 0.22uF 20% 6.3V CERM 402
C348 0.22uF 20% 6.3V CERM 402
C320 0.22uF 20% 6.3V CERM 402
C368 0.22uF 20% 6.3V CERM 402
C275 0.22uF 20% 6.3V CERM 402
C305 0.22uF 20% 6.3V CERM 402
C322 0.22uF 20% 6.3V CERM 402
C302 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C124 10uF 20% 6.3V CERM 805
C103 10uF 20% 6.3V CERM 805
C136 0.22uF 20% 6.3V CERM 402
C222 0.22uF 20% 6.3V CERM 402
C243 0.22uF 20% 6.3V CERM 402
C221 0.22uF 20% 6.3V CERM 402
C206 0.22uF 20% 6.3V CERM 402
C165 0.22uF 20% 6.3V CERM 402
C131 0.22uF 20% 6.3V CERM 402
C192 0.22uF 20% 6.3V CERM 402
C259 0.22uF 20% 6.3V CERM 402
C245 0.22uF 20% 6.3V CERM 402
C154 10uF 20% 6.3V CERM 805
C301 10uF 20% 6.3V CERM 805
C223 0.22uF 20% 6.3V CERM 402
C189 0.22uF 20% 6.3V CERM 402
C162 0.22uF 20% 6.3V CERM 402
C163 0.22uF 20% 6.3V CERM 402
C161 0.22uF 20% 6.3V CERM 402
C143 0.22uF 20% 6.3V CERM 402
C145 0.22uF 20% 6.3V CERM 402
C146 0.22uF 20% 6.3V CERM 402
C261 0.22uF 20% 6.3V CERM 402
C260 0.22uF 20% 6.3V CERM 402
C133 0.22uF 20% 6.3V CERM 402
C225 0.22uF 20% 6.3V CERM 402
C188 0.22uF 20% 6.3V CERM 402
C244 0.22uF 20% 6.3V CERM 402
C164 0.22uF 20% 6.3V CERM 402
C190 0.22uF 20% 6.3V CERM 402
C175 0.22uF 20% 6.3V CERM 402
C185 0.22uF 20% 6.3V CERM 402
C191 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C148 10uF 20% 6.3V CERM2 805
C377 10uF 20% 6.3V CERM2 805
C355 0.22uF 20% 6.3V CERM 402
C329 0.22uF 20% 6.3V CERM 402
C56 0.22uF 20% 6.3V CERM 402
C46 0.22uF 20% 6.3V CERM 402
C23 0.22uF 20% 6.3V CERM 402
C169 0.22uF 20% 6.3V CERM 402
C38 0.22uF 20% 6.3V CERM 402
C132 0.22uF 20% 6.3V CERM 402
C119 0.22uF 20% 6.3V CERM 402
C117 0.22uF 20% 6.3V CERM 402
C12 10uF 20% 6.3V CERM2 805
C10 10uF 20% 6.3V CERM2 805
C40 0.22uF 20% 6.3V CERM 402
C168 0.22uF 20% 6.3V CERM 402
C47 0.22uF 20% 6.3V CERM 402
C42 0.22uF 20% 6.3V CERM 402
C242 0.22uF 20% 6.3V CERM 402
C63 0.22uF 20% 6.3V CERM 402
C55 0.22uF 20% 6.3V CERM 402
C177 0.22uF 20% 6.3V CERM 402
C60 0.22uF 20% 6.3V CERM 402
C21 0.22uF 20% 6.3V CERM 402
C17 0.22uF 20% 6.3V CERM 402
C106 0.22uF 20% 6.3V CERM 402
C58 0.22uF 20% 6.3V CERM 402
C39 0.22uF 20% 6.3V CERM 402
C121 0.22uF 20% 6.3V CERM 402
C49 0.22uF 20% 6.3V CERM 402
C79 0.22uF 20% 6.3V CERM 402
C258 0.22uF 20% 6.3V CERM 402
C35 0.22uF 20% 6.3V CERM 402
C33 0.22uF 20% 6.3V CERM 402
C41 0.22uF 20% 6.3V CERM 402
C26 0.22uF 20% 6.3V CERM 402
C116 0.22uF 20% 6.3V CERM 402
C135 0.22uF 20% 6.3V CERM 402
C130 0.22uF 20% 6.3V CERM 402
C37 0.22uF 20% 6.3V CERM 402
C134 0.22uF 20% 6.3V CERM 402
C98 0.22uF 20% 6.3V CERM 402
C57 0.22uF 20% 6.3V CERM 402
C53 0.22uF 20% 6.3V CERM 402
C78 0.22uF 20% 6.3V CERM 402
C118 0.22uF 20% 6.3V CERM 402
C54 0.22uF 20% 6.3V CERM 402
C62 0.22uF 20% 6.3V CERM 402
C147 0.22uF 20% 6.3V CERM 402
C122 0.22uF 20% 6.3V CERM 402
C100 0.22uF 20% 6.3V CERM 402
C107 0.22uF 20% 6.3V CERM 402
C59 0.22uF 20% 6.3V CERM 402
C34 0.22uF 20% 6.3V CERM 402
C278 0.22uF 20% 6.3V CERM 402
C227 0.22uF 20% 6.3V CERM 402
C187 0.22uF 20% 6.3V CERM 402
C61 0.22uF 20% 6.3V CERM 402
C25 0.22uF 20% 6.3V CERM 402
C22 0.22uF 20% 6.3V CERM 402
C64 0.22uF 20% 6.3V CERM 402
C48 0.22uF 20% 6.3V CERM 402
C36 0.22uF 20% 6.3V CERM 402
C27 0.22uF 20% 6.3V CERM 402
C167 0.22uF 20% 6.3V CERM 402
C19 0.22uF 20% 6.3V CERM 402
C52 0.22uF 20% 6.3V CERM 402
C43 0.22uF 20% 6.3V CERM 402
C18 0.22uF 20% 6.3V CERM 402
C101 0.22uF 20% 6.3V CERM 402
C378 0.22uF 20% 6.3V CERM 402
C120 0.22uF 20% 6.3V CERM 402
C123 0.22uF 20% 6.3V CERM 402
C102 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 17 OF 44	

PCI1510 PULL-UPS

+3V_MAIN

R670 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 18
R669 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 18
R662 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 18

+3V_MAIN

C579 10UF 20% 6.3V CERM 805
C761 0.22UF 20% 6.3V CERM 402
C764 0.22UF 20% 6.3V CERM 402
C755 0.22UF 20% 6.3V CERM 402
C762 0.22UF 20% 6.3V CERM 402
C763 0.22UF 20% 6.3V CERM 402
C756 0.22UF 20% 6.3V CERM 402

R676 10K 5% 1/16W MF 402

+2_5V_MAIN

C754 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11 — VCC

39 30 26 24 21 19 18 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R774 47 5% 1/16W MF 402

+3V_MAIN
+5V_MAIN

NO STUFF
R299 10K 5% 1/16W MF 402

U20
TPS2211 SSOI

NC 9	V_12	AVPP	10
5	V_5_1		
6	V_5_2	AVCC0	11
3	V_3_1	AVCC1	12
4	V_3_2	AVCC2	13
1	VCCD0		
2	VCCD1		
15	VPPD0		
14	VPPD1		
16	SHTDWN		
7	GND	OC	8 NC

10 — +VPP_CBUS_SW 18 38
11 — +VCC_CBUS_SW 18 38

TPS2211_SHDN_L_PU

C739 0.1UF 20% 16V CERM 402
C448 0.1UF 20% 16V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L D4	VR_EN*	
L8	VR_PORT	
39 37 26 24 13 16 PCI_AD<0> N8	AD0	
39 37 26 24 13 16 PCI_AD<1> M7	AD1	
39 37 26 24 13 16 PCI_AD<2> L7	AD2	
39 37 26 24 13 16 PCI_AD<3> N6	AD3	
39 37 26 24 13 16 PCI_AD<4> K4	AD4	
39 37 26 24 13 16 PCI_AD<5> M6	AD5	
39 37 26 24 13 16 PCI_AD<6> L6	AD6	
39 37 26 24 13 16 PCI_AD<7> N5	AD7	
39 37 26 24 13 16 PCI_AD<8> N4	AD8	
39 37 26 24 13 16 PCI_AD<9> M2	AD9	
39 37 26 24 13 16 PCI_AD<10> M5	AD10	
39 37 26 24 13 16 PCI_AD<11> L4	AD11	
39 37 26 24 13 16 PCI_AD<12> N3	AD12	
39 37 26 24 13 16 PCI_AD<13> K5	AD13	
39 37 26 24 13 16 PCI_AD<14> L5	AD14	
39 37 26 24 13 16 PCI_AD<15> M4	AD15	
39 37 26 24 13 16 PCI_AD<16> J4	AD16	
39 37 26 24 13 16 PCI_AD<17> H1	AD17	
39 37 26 24 13 16 PCI_AD<18> H3	AD18	
PCI_AD<19> H2	AD19	
39 37 26 24 13 16 PCI_AD<20> G2	AD20	
39 37 26 24 13 PCI_AD<21> G4	AD21	
39 37 26 24 13 PCI_AD<22> F1	AD22	
39 37 26 24 13 PCI_AD<23> C3	AD23	
39 37 26 24 13 16 PCI_AD<24> F3	AD24	
39 37 26 24 13 16 PCI_AD<25> E2	AD25	
39 37 26 24 13 16 PCI_AD<26> F4	AD26	
39 37 26 24 13 16 PCI_AD<27> B1	AD27	
39 37 26 24 13 16 PCI_AD<28> D2	AD28	
39 37 26 24 13 16 PCI_AD<29> E4	AD29	
39 37 26 24 13 16 PCI_AD<30> D3	AD30	
39 37 26 24 13 16 PCI_AD<31> E3	AD31	
39 37 26 24 13 PCI_CBE<0> K6	C/BE0*	
39 37 26 24 13 PCI_CBE<1> M3	C/BE1*	
39 37 26 24 13 PCI_CBE<2> J2	C/BE2*	
39 37 26 24 13 PCI_CBE<3> A1	C/BE3*	
39 37 26 24 13 PCI_PAR N1	PAR	
39 37 26 24 13 PCI_IRDY_L K1	IRDY	
18 CBUS_PCI_SERR_L L2	SERR	
CBUS_PCI_IDSEL F2	IDSEL	
18 CBUS_PCI_PERR_L K3	PERR	
39 37 26 24 13 PCI_FRAME_L J1	FRAME	
39 37 26 24 13 PCI_STOP_L L1	STOP	
39 37 26 24 13 PCI_TRDY_L J3	TRDY	
39 37 26 24 13 PCI_DEVSEL_L K2	DEVSEL	
CBUS_PCI_RESET_L G3	PRST	
13 CBUS_PCI_REQ_L C2	REQ	
13 CBUS_PCI_GNT_L C1	GNT	
36 13 CLK33M_CBUS G1	PCLK	
NC M9	SPKROUT	
NC M8	RI_OUT/PME	
16 CBUS_SUSPEND_PU N10	SUSPEND	
15 CBUS_INT_L K7	MFUNC0	
16 CBUS_MFUNC1_PD N9	MFUNC1	
16 CBUS_MFUNC2_PD L9	MFUNC2	
16 CBUS_MFUNC3_PD K10	MFUNC3	
16 CBUS_MFUNC4_PD M10	MFUNC4	
16 CBUS_MFUNC5_PD N12	MFUNC5	
16 CBUS_MFUNC6_PD L10	MFUNC6	
L11	GRST	

R684 22 5% 1/16W MF 402

NO STUFF
R675 47 5% 1/16W MF 402 — 30 27 26 19 IO_RESET_L

R763 47 5% 1/16W MF 402 — 39 30 26 24 21 19 18 MAIN_RESET_L

RP38 10K 5% 1/32W 25W SM

5	6	CBUS_MFUNC1_PD 18
10	4	CBUS_MFUNC2_PD 18
	7	CBUS_MFUNC3_PD 18
	3	CBUS_MFUNC4_PD 18
	9	CBUS_MFUNC5_PD 18
	8	CBUS_MFUNC6_PD 18
	2	
	1	

GND
A2 A11 D1 F13 H4 K8 M13 N2

VCCCB B11		
VCCP L3		
VCCD0* N13	CBUS_VCCD0_L	
VCCD1* L12	CBUS_VCCD1_L	
VPPD0 K9	CBUS_VPPD0	
VPPD1 M11	CBUS_VPPD1	
CD1*/CCD1* L13	CBUS_DET_1_L	18 39
CD2*/CCD2* B5	CBUS_DET_2_L	18 39
IORD*/CAD13 F12	CBUS_IORD_L	18
IOWR*/CAD15 C11	CBUS_IOWR_L	18
OE*/CAD11 G10	CBUS_OE_L	18
CE1*/CC/BE0* H13	CBUS_CE1_L	18
VS1*/CVS1 B2	CBUS_VS1	18
VS2*/CVS2 A9	CBUS_VS2	18
WE*/CGNT* D13	CBUS_WE_L	18
RDY/IREQ*/CINT* A6	CBUS_READY	18
RESET/CRST* D8	CBUS_RESET_L	18
REG*/CC/BE3* A8	CBUS_REG_L	18
BVD1/CSTSCHG/STSCHG*/RI* C6	CBUS_BVD1_L	18
BVD2/SPKR*/CAUDIO D6	CBUS_BVD2_L	18
INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN* A5	CBUS_WP_L	18
CE2/CAD10* G13	CBUS_CE2_L	18
INPACK/CREQ* B8	CBUS_INPACK_L	18
WAIT/CSERR* B6	CBUS_WAIT_L	18
A0/CAD26 C7	CBUS_ADDR<0>	18
A1/CAD25 D7	CBUS_ADDR<1>	18
A2/CAD24 B7	CBUS_ADDR<2>	18
A3/CAD23 D10	CBUS_ADDR<3>	18
A4/CAD22 B12	CBUS_ADDR<4>	18
A5/CAD21 C8	CBUS_ADDR<5>	18
A6/CAD20 C9	CBUS_ADDR<6>	18
A7/CAD18 A12	CBUS_ADDR<7>	18
A8/CC/BE1* E11	CBUS_ADDR<8>	18
A9/CAD14 F11	CBUS_ADDR<9>	18
A10/CAD9 G11	CBUS_ADDR<10>	18
A11/CAD12 G12	CBUS_ADDR<11>	18
A12/CC/BE2* D9	CBUS_ADDR<12>	18
A13/CPAR E12	CBUS_ADDR<13>	18
A14/CPERR* D12	CBUS_ADDR<14>	18
A15/CIRDY* C10	CBUS_ADDR<15>	18
A16/CCLK B13	CBUS_ADDR_16_UF	
A17/CAD16 F10	CBUS_ADDR<17>	18
A18/RSVD E13	CBUS_ADDR<18>	18
A19/CBLOCK* A13	CBUS_ADDR<19>	18
A20/CSTOP* E10	CBUS_ADDR<20>	18
A21/CDEVSEL* D11	CBUS_ADDR<21>	18
A22/CTRDY* C12	CBUS_ADDR<22>	18
A23/CFRAME* A10	CBUS_ADDR<23>	18
A24/CAD17 B10	CBUS_ADDR<24>	18
A25/CAD19 B9	CBUS_ADDR<25>	18
D0/CAD27 A4	CBUS_DATA<0>	18
D1/CAD29 C4	CBUS_DATA<1>	18
D2/RSVD A3	CBUS_DATA<2>	18
D3/CAD0 K11	CBUS_DATA<3>	18
D4/CAD1 K12	CBUS_DATA<4>	18
D5/CAD3 J13	CBUS_DATA<5>	18
D6/CAD5 J10	CBUS_DATA<6>	18
D7/CAD7 H12	CBUS_DATA<7>	18
D8/CAD28 C5	CBUS_DATA<8>	18
D9/CAD30 B4	CBUS_DATA<9>	18
D10/CAD31 B3	CBUS_DATA<10>	18
D11/CAD2 M12	CBUS_DATA<11>	18
D12/CAD4 J11	CBUS_DATA<12>	18
D13/CAD6 K13	CBUS_DATA<13>	18
D14/RSVD J12	CBUS_DATA<14>	18
D15/CAD8 H11	CBUS_DATA<15>	18

R661 47 5% 1/16W MF 402 — CBUS_ADDR<16> 18

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C748 2.2UF 20% 16V CERM 805
C742 2.2UF 20% 16V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL
J10
QT500806-L111
M-ST-SM

	84	81	
	2	1	CBUS_DATA<3> 18
39 18 CBUS_DET_1_L	4	3	CBUS_DATA<4> 18
18 CBUS_DATA<11>	6	5	CBUS_DATA<5> 18
18 CBUS_DATA<12>	8	7	CBUS_DATA<6> 18
18 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 18
18 CBUS_DATA<14>	14	13	CBUS_CE1_L 18
18 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 18
18 CBUS_CE2_L	18	17	CBUS_OE_L 18
18 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 18
18 CBUS_IORD_L	24	23	CBUS_ADDR<9> 18
18 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 18
18 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 18
18 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 18
18 CBUS_ADDR<19>	34	33	CBUS_WE_L 18
18 CBUS_ADDR<20>	36	35	CBUS_READY 18
18 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 18 38
38 18 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 18 38
38 18 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 18
18 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 18
18 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 18
18 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 18
18 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 18
18 CBUS_VS2	56	55	CBUS_ADDR<5> 18
18 CBUS_RESET_L	58	57	CBUS_ADDR<4> 18
18 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 18
18 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 18
18 CBUS_REG_L	66	65	CBUS_ADDR<1> 18
18 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 18
18 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 18
18 CBUS_DATA<8>	74	73	CBUS_DATA<1> 18
18 CBUS_DATA<9>	76	75	CBUS_DATA<2> 18
18 CBUS_DATA<10>	78	77	CBUS_WP_L 18
39 18 CBUS_DET_2_L	80	79	
	83	82	

CARDBUS

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 18 OF 44	

IMPORTANT NOTES ON MAP17

NEED TO RESET GRAPHIC CHIP DURING RESTARTS

MEMORY CORE - 2.5V

+2_5V_GPU_FB 19 38

C264 10UF 20% 6.3V CERM 805 | C289 0.1UF 20% 10V CERM 402 | C283 0.1UF 20% 10V CERM 402 | C288 0.1UF 20% 10V CERM 402 | C104 0.1UF 20% 10V CERM 402 | C93 0.1UF 20% 10V CERM 402 | C84 0.1UF 20% 10V CERM 402 | C251 0.1UF 20% 10V CERM 402 | C94 0.1UF 20% 10V CERM 402

AGP 4X I/O - 1.5V

U43 MAP31-64MB BGA (1 OF 5)

OMIT

AGP_AD<0>	AD30	PCIAD0	
AGP_AD<1>	AE30	PCIAD1	
AGP_AD<2>	AD29	PCIAD2	
AGP_AD<3>	AE29	PCIAD3	
AGP_AD<4>	AD28	PCIAD4	
AGP_AD<5>	AG30	PCIAD5	
AGP_AD<6>	AF28	PCIAD6	
AGP_AD<7>	AG29	PCIAD7	
AGP_AD<8>	AH30	PCIAD8	
AGP_AD<9>	AC28	PCIAD9	
AGP_AD<10>	AH29	PCIAD10	
AGP_AD<11>	AE28	PCIAD11	
AGP_AD<12>	AJ30	PCIAD12	
AGP_AD<13>	AG28	PCIAD13	
AGP_AD<14>	AK30	PCIAD14	
AGP_AD<15>	AG27	PCIAD15	
AGP_AD<16>	AH23	PCIAD16	
AGP_AD<17>	AJ24	PCIAD17	
AGP_AD<18>	AH22	PCIAD18	
AGP_AD<19>	AK24	PCIAD19	
AGP_AD<20>	AH21	PCIAD20	
AGP_AD<21>	AJ22	PCIAD21	
AGP_AD<22>	AH20	PCIAD22	
AGP_AD<23>	AK22	PCIAD23	
AGP_AD<24>	AG21	PCIAD24	
AGP_AD<25>	AJ19	PCIAD25	
AGP_AD<26>	AG18	PCIAD26	
AGP_AD<27>	AK19	PCIAD27	
AGP_AD<28>	AG19	PCIAD28	
AGP_AD<29>	AJ18	PCIAD29	
AGP_AD<30>	AF19	PCIAD30	
AGP_AD<31>	AK18	PCIAD31	

		VDDAGP0	AF30
		VDDAGP1	AG14
		VDDAGP2	AG17
		VDDAGP3	AG20
		VDDAGP4	AK14
		VDDAGP5	AK17
		VDDAGP6	AK20
		VDDAGP7	AK23
		VDDAGP8	AK26
		VDDAGP9	AK29

38 20 19 17 16 13 +1_5V_AGP

BULK CAP ON INTREPID SIDE

C44 0.1UF 20% 10V CERM 402 | C92 0.1UF 20% 10V CERM 402 | C125 0.1UF 20% 10V CERM 402 | C150 0.1UF 20% 10V CERM 402

C65 0.01UF 20% 16V CERM 402 | C149 0.01UF 20% 16V CERM 402 | C196 0.01UF 20% 16V CERM 402 | C28 0.01UF 20% 16V CERM 402

MEMORY I/O - 2.5V

38 19 +2_5V_GPU_FB

C170 10UF 20% 6.3V CERM 805 | C80 0.1UF 20% 10V CERM 402 | C67 0.1UF 20% 10V CERM 402 | C81 0.1UF 20% 10V CERM 402

C317 0.1UF 20% 10V CERM 402 | C85 0.1UF 20% 10V CERM 402 | C72 0.1UF 20% 10V CERM 402

C282 0.1UF 20% 10V CERM 402 | C318 0.1UF 20% 10V CERM 402 | C254 0.1UF 20% 10V CERM 402 | C313 0.1UF 20% 10V CERM 402

C105 0.01UF 20% 16V CERM 402 | C314 0.01UF 20% 16V CERM 402 | C294 0.01UF 20% 16V CERM 402 | C66 0.01UF 20% 16V CERM 402

U43 MAP31-64MB BGA (3 OF 5)

OMIT

		VDDFBIO0	AB27
			AD27
			AD4
			AE26
			AE5
			AF25
			AF27
			AF4
			AF6
			AG24
			AG26
			AG5
			AG7
			D22
			D24
			D26
			D5
			D7
			D9
			E25
			E27
			E4
			E6
			F26
			F5
			G27
			G4
			J27
			J4

		VDDFBC	AB25
			AB6
			AD25
			AD6
			AE22
			AE24
			AE7
			AE9
			F22
			F24
			F7
			F9
			G25
			G6
			J25
			J6

HARDWARE DEBUG PORT

VIPD	K4	GPU_VIPD0_TP	
	J3	GPU_VIPD1_TP	
	H3	GPU_VIPD2_ROMTYPE<1>	21
	K5	GPU_VIPD3_PCI_DEVID<2>	21
	G2	GPU_VIPD4_PCI_DEVID<0>	21
	G1	GPU_VIPD5_PCI_DEVID<1>	21
	F1	GPU_VIPD6_CRYSTAL<1>	21
	G3	GPU_VIPD7_TP	
VIPHAD0	C8	GPU_VIPHAD0_TP	
VIPHAD1	C7	GPU_VIPHAD1_TP	
VIPHCLK	A5	GPU_VIPHCLK_TP	
VIPHCTL	B6	GPU_VIPHTCL_TP	
VIPPCLK	B7	VIPPCLK_PD	

+2_5V_GPU_FB 19 38

MAP31 R31 49.9 1% 1/16W MF 402

MEM_CAL_PD	G30	MEM_CAL_PD	
MEM_CAL_PU	J30	MEM_CAL_PU	
MEM_CAL_CLK	K30	MEM_CAL_CLK	

MAP31 R173 10K 5% 1/16W MF 402 | MAP31 R30 49.9 1% 1/16W MF 402 | MAP31 R29 49.9 1% 1/16W MF 402

AGP I/O REFERENCE

(PLACE CLOSE TO NV17M AGP BALLS)

38 20 19 17 16 13 +1_5V_AGP

R22 4.99K 1% 1/16W MF 402

GPU_AGP_VREF 19 38

R28 4.99K 1% 1/16W MF 402 | C13 0.22UF 20% 6.3V CERM 402

USE SIMPLE REFERENCE TO CHIP

BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

FB SIGNALS USED FOR INTERNAL TESTING ONLY

CHANGE TO NC FOR NEXT SYMBOL UPDATE

NC	A24	FBAA0_0	
NC	B10	FBAA0_1	
36 19 GPU_FBCLK0	C21	FBCLK0	
36 19 GPU_FBCLK0_L	C20	FBCLK0*	
36 19 GPU_FBCLK1	B4	FBCLK1	
36 19 GPU_FBCLK1_L	A4	FBCLK1*	
GPU_FBACKE	N28	FBACKE	
FBACKE PULL-DOWN IS NEEDED	D28	FBD1	
NC	D13	FBD33	
NC	AA27	FBD8_0	
NC	J28	FBD8_1	
38 GPU_FB_VREF	A18	FBVREF	
NC	C11	FBAWE*	
GPU_ROMA14_TP	J1	ROMA14	
GPU_ROMA15_TP	F2	ROMA15	
GPU_ROMCS_TP	AH2	ROMCS*	

THERE'S NO ON-CHIP VOLTAGE DIVIDER

FBDQS0	F28	NC	
FBDQS1	AA26	NC	
FBDQS2	K28	NC	
FBDQS3	E12	NC	

R1900 10K 5% 1/16W MF 402 | R1901 10K 5% 1/16W MF 402 | R35 10K 5% 1/16W MF 402

FRAME BUFFER CLOCK TERMINATION

+2_5V_GPU_FB 19 38

NO STUFF R72 120 5% 1/16W MF 402 — GPU_FBCLK0 19 36

NO STUFF R82 100 5% 1/16W MF 402

NO STUFF R83 120 5% 1/16W MF 402 — GPU_FBCLK0_L 19 36

+2_5V_GPU_FB 19 38

NO STUFF R186 120 5% 1/16W MF 402 — GPU_FBCLK1 19 36

NO STUFF R185 100 5% 1/16W MF 402

NO STUFF R191 120 5% 1/16W MF 402 — GPU_FBCLK1_L 19 36

D3HOT VS. D3COLD POWER INTAKE

3V

+3V_MAIN: D3HOT R245 0 5% 1/10W FF 805

+3V_SLEEP: D3COLD R244 0 5% 1/10W FF 805 — +3V_GPU 13 15 20 21 38

1.5V

38 35 16 +1_5V_LDO

NO STUFF R1605 0 5% 1/16W MF 603

+1_5V_MAIN: D3HOT R635 0 5% 1/16W MF 603

+1_5V_SLEEP: D3COLD R634 0 5% 1/16W MF 603 — +1_5V_AGP 13 16 17 19 20 38

INTREPID AGP IS ALSO CONNECTED TO +1_5V_AGP

2.5V

+2_5V_MAIN: D3HOT R648 0 5% 1/10W FF 805

+2_5V_SLEEP: D3COLD R647 0 5% 1/10W FF 805 — +2_5V_GPU_FB 19 38

FOR AGP 8X

		NC	AH19
		NC	AK13
38 19 GPU_AGP_VREF	AC30	AGPVREF	
37 13 AGP_SBA<0>	AJ15	AGPSBA0	
37 13 AGP_SBA<1>	AF15	AGPSBA1	
37 13 AGP_SBA<2>	AK15	AGPSBA2	
37 13 AGP_SBA<3>	AG16	AGPSBA3	
37 13 AGP_SBA<4>	AK16	AGPSBA4	
37 13 AGP_SBA<5>	AF16	AGPSBA5	
37 13 AGP_SBA<6>	AJ16	AGPSBA6	
37 13 AGP_SBA<7>	AH18	AGPSBA7	
37 13 AGP_SB_STB	AH16	AGPSBSTB	
37 13 AGP_SB_STB_L	AH17	AGPSBSTB*	

37 13 AGP_CBE<0>	AH28	PCICBE0*	
37 13 AGP_CBE<1>	AJ27	PCICBE1*	
37 13 AGP_CBE<2>	AK25	PCICBE2*	
37 13 AGP_CBE<3>	AF21	PCICBE3*	
36 13 CLK66M_GPU_AGP	AJ12	PCICLK	
AGP_GPU_RESET_L	AH11	PCIRST*	
37 13 AGP_GNT_L	AG12	PCIGNT*	
37 13 AGP_REQ_L	AK12	PCIREQ*	
37 13 AGP_FRAME_L	AH24	PCIFRAME*	
37 13 AGP_IRDY_L	AJ25	PCIIRDY*	
37 13 AGP_TRDY_L	AH25	PCITRDY*	
37 13 AGP_DEVSEL_L	AK27	PCIDEVSEL*	
37 13 AGP_STOP_L	AH26	PCISTOP*	
37 13 AGP_PAR	AH27	PCIPAR	
15 AGP_NV_INT_L	AK11	PCIINTA*	
37 13 AGP_RBF_L	AJ13	AGPRBF*	
AGP_NV_WBF_L	AG15	AGPWBF*	
AGP_NV_PIPE_L	AF18	AGPPIPE*	
13 AGP_ST<0>	AF12	AGPST0	
13 AGP_ST<1>	AF13	AGPST1	
13 AGP_ST<2>	AG13	AGPST2	
37 13 AGP_AD_STB<1>	AK21	AGPADSTB1	
37 13 AGP_AD_STB_L<1>	AJ21	AGPADSTB1*	
37 13 AGP_AD_STB<0>	AK28	AGPADSTB0	
37 13 AGP_AD_STB_L<0>	AJ28	AGPADSTB0*	
13 AGP_BUSY_L	AF10	AGPBUSY*	
13 STOP_AGP_L	AG10	AGPSTOP*	
AGP_CAL_PD	AH15	AGP_CAL_PD	
AGP_CAL_PU	AH14	AGP_CAL_PU	

		NC	A1
		NC	A10
		NC	A11
		NC	A13
		NC	A14
		NC	A15
		NC	A16
		NC	A17
		NC	A2
		NC	A20
		NC	A21
		NC	A22
		NC	A23
		NC	A25
		NC	A26
		NC	A27
		NC	A28
		NC	A3
		NC	AA28
		NC	AA29
		NC	AA30
		NC	AA4
		NC	AA5
		NC	AB28
		NC	AB29
		NC	AB30
		NC	B1
		NC	B13
		NC	B15
		NC	B16
		NC	B18
		NC	B19
		NC	B21
		NC	B22
		NC	B24
		NC	B25
		NC	B27
		NC	B28
		NC	B3
		NC	C1
		NC	C10
		NC	C13
		NC	C14
		NC	C15
		NC	C16

D3COLD R601 47 5% 1/16W MF 402 — MAIN_RESET_L 39 30 26 24 21 18

D3HOT R155 47 5% 1/16W MF 402 — IO_RESET_L 30 27 26 18

MAIN_RESET_L IS TOGGLED FOR SLEEP

IO_RESET_L IS NOT TOGGLED FOR SLEEP

R115 0 5% 1/16W MF 402 — AGP_WBF_L 13

R99 0 5% 1/16W MF 402 — AGP_PIPE_L 13

38 20 19 17 16 13 +1_5V_AGP

MAP31 R128 49.9 1% 1/16W MF 402

MAP31 R136 49.9 1% 1/16W MF 402

U43 MAP31-64MB BGA (4 OF 5)

OMIT

GND

GND

MAP17 AGP/DDR RAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A

SCALE	SHT	OF
NONE	19	44

GPU VCORE SUPPLY

2.8V IFP PLL SUPPLY

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

I2C1 PULL-UP

U43 MAP31-64MB BGA (5 OF 5) OMIT

ALL I2C ARE 5V TOLERANT

GPIOS HAVE CLAMP TO 5V
GPIOS ARE PLACED IN TRISTATE DURING SLEEP
ONLY GPIO6 IS ENABLED

NVIDIA CONFIRMED NO CONNECT ON BUFRST*
THIS IS A BUFFERED VERSION OF PCI RESET

2.8V IS DEPENDENT ON CORE VOLTAGE

PLACE VREF AND RSET DISCRETE CLOSE TO PIN

'1' DURING SHUTDOWN
'0' DURING SLEEP/RUN

57.6K IN PARALLEL => VOUT = 1.338V
53.6K IN PARALLEL => VOUT = 1.35V
49.9K IN PARALLEL => VOUT = 1.36V

VOUT = 0.8V * (1 + UPPER R / LOWER R)

WHEN LOW => 1.2V
WHEN HIGH => 1.36V

VOUT = 1.22(1 + R2/R1) + IADJ*R2
IADJ = 30NA AT 25C

ONE SET OF ,0.1UF,0.01UF FOR IFP0 AND IFP1 SHARES 10UF

CHANGE TO FERRITE IF NECESSARY

MAP17 PWR/LVDS/TMDS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 20 OF 44	

3.3V IO SUPPLY

C394 10UF 20% 6.3V CERM 805 · C344 0.1UF 20% 10V CERM 402 · C316 0.1UF 20% 10V CERM 402 · C338 0.1UF 20% 10V CERM 402 · C315 0.1UF 20% 10V CERM 402 · C319 0.1UF 20% 10V CERM 402 · C232 0.1UF 20% 10V CERM 402

R183 0 5% 1/16W MF 603 — REPLACE WITH FERRITE IF NECESSARY

C324 10UF 20% 6.3V CERM 805 · C325 0.1UF 20% 10V CERM 402 · C312 0.01UF 20% 16V CERM 402

R228 0 5% 1/16W MF 603 — REPLACE WITH FERRITE IF NECESSARY

C395 10UF 20% 6.3V CERM 805 · C359 0.1UF 20% 10V CERM 402 · C352 0.01UF 20% 16V CERM 402

R166 33 5% 1/16W MF 402 — VGA_VSYNC
R156 33 5% 1/16W MF 402 — VGA_HSYNC

R127 0 5% 1/16W MF 603 — REPLACE WITH FERRITE IF NECESSARY

C211 10UF 20% 6.3V CERM 805 · C231 0.1UF 20% 10V CERM 402 · C250 0.01UF 20% 16V CERM 402

U43 MAP31-64MB BGA (2 OF 5) OMIT

AK5	PLLVDD	
Y3	CRT2VSYNC	GPU_CRT2VSYNC_TP
AA3	CRT2HSYNC	GPU_CRT2HSYNC_TP
AA1	DAC2VDD	
W1	DAC2GND	
W3	DAC2BLUE	GPU_COMP
AA2	DAC2GREEN	GPU_Y
Y2	DAC2RED	GPU_C
W2	DAC2RSET	GPU_RSET2
Y1	DAC2VREF	GPU_DACVREF2
AB1	DVOVREF	GPU_DVO_VREF
AK1	DVODE	GPU_DVO_DE
AD2	DVOCLKOUT	
AD1	DVOCLKOUT*	GPU_DVO_CLKN_TP
AB2	DVOCLKIN	GPU_DVO_CLKIN
AB3	DVOHSYNC	GPU_DVO_HSYNC
AC3	DVOVSYNC	GPU_DVO_VSYNC
AK2	DVOD0	GPU_DVOD<0>
AK3	DVOD1	GPU_DVOD<1>
AH3	DVOD2	GPU_DVOD<2>
AJ1	DVOD3	GPU_DVOD<3>
AG1	DVOD4	GPU_DVOD<4>
AG2	DVOD5	GPU_DVOD<5>
AD3	DVOD6	GPU_DVOD<6>
AE1	DVOD7	GPU_DVOD<7>
AE3	DVOD8	GPU_DVOD<8> — TESTCTL0_TP
AE2	DVOD9	GPU_DVOD<9> — TESTCTL1_TP
AG3	DVOD10	GPU_DVOD<10> — TESTCTL2_TP
AH1	DVOD11	GPU_DVOD<11> — TESTCTL3_TP
AF3	VDDDVO_0	+3V_GPU_DVO
AG4	VDDDVO_1	
AC1	VDD 3.3V	+3V_GPU
AF1	VDD 3.3V	+3V_GPU
E1	VDD 3.3V	+3V_GPU
H1	VDD 3.3V	+3V_GPU
L4	VDD 3.3V	+3V_GPU
A12	VDD(MAP31) 3.3V	+3V_GPU
K19	VDD(MAP31) 3.3V	+3V_GPU
D17	VDD(MAP31) 3.3V	+3V_GPU
G22	VDD(MAP31) 3.3V	+3V_GPU
H15	VDD(MAP31) 3.3V	+3V_GPU
K8	VDD(MAP31) 3.3V	+3V_GPU
M20	VDD(MAP31) 3.3V	+3V_GPU
AG1	VDD 5V	+5V
L4	VDD 5V	+5V
AK6	PTREEOUT	GPU_FBACAS_TP
AK4	NC	
AK7	NC	
AL1	NC	
AL2	NC	
AL3	NC	
AL4	NC	
AL5	NC	
AL6	NC	
AL7	NC	
AL8	NC	
AL9	NC	
AL10	NC	
AL11	NC	
AL12	NC	
AL13	NC	
AL14	NC	
AL15	NC	
AL16	NC	
AL17	NC	
AL18	NC	
AL19	NC	
AL20	NC	
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AL22	NC	
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AL26	NC	
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AL38	NC	
AL39	NC	
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AM3	NC	
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AP30	NC	
AP31	NC	
AP32	NC	
AP33	NC	
AP34	NC	
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AP36	NC	
AP37	NC	
AP38	NC	
AP39	NC	
AR1	NC	
AR2	NC	
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AR8	NC	
AR9	NC	
AR10	NC	
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AR37	NC	
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AT2	NC	
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AT7	NC	
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AT9	NC	
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AU1	NC	
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AU34	NC	
AU35	NC	
AU36	NC	
AU37	NC	
AU38	NC	
AU39	NC	
AV1	NC	
AV2	NC	
AV3	NC	
AV4	NC	
AV5	NC	
AV6	NC	
AV7	NC	
AV8	NC	
AV9	NC	
AV10	NC	
AV11	NC	
AV12	NC	
AV13	NC	
AV14	NC	
AV15	NC	
AV16	NC	
AV17	NC	
AV18	NC	
AV19	NC	
AV20	NC	
AV21	NC	
AV22	NC	
AV23	NC	
AV24	NC	
AV25	NC	
AV26	NC	
AV27	NC	
AV28	NC	
AV29	NC	
AV30	NC	
AV31	NC	
AV32	NC	
AV33	NC	
AV34	NC	
AV35	NC	
AV36	NC	
AV37	NC	
AV38	NC	
AV39	NC	
AW1	NC	
AW2	NC	
AW3	NC	
AW4	NC	
AW5	NC	
AW6	NC	
AW7	NC	
AW8	NC	
AW9	NC	
AW10	NC	
AW11	NC	
AW12	NC	
AW13	NC	
AW14	NC	
AW15	NC	
AW16	NC	
AW17	NC	
AW18	NC	
AW19	NC	
AW20	NC	
AW21	NC	
AW22	NC	
AW23	NC	
AW24	NC	
AW25	NC	
AW26	NC	
AW27	NC	
AW28	NC	
AW29	NC	
AW30	NC	
AW31	NC	
AW32	NC	
AW33	NC	
AW34	NC	
AW35	NC	
AW36	NC	
AW37	NC	
AW38	NC	
AW39	NC	
AY1	NC	
AY2	NC	
AY3	NC	
AY4	NC	
AY5	NC	
AY6	NC	
AY7	NC	
AY8	NC	
AY9	NC	
AY10	NC	
AY11	NC	
AY12	NC	
AY13	NC	
AY14	NC	
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AY23	NC	
AY24	NC	
AY25	NC	
AY26	NC	
AY27	NC	
AY28	NC	
AY29	NC	
AY30	NC	
AY31	NC	
AY32	NC	
AY33	NC	
AY34	NC	
AY35	NC	
AY36	NC	
AY37	NC	
AY38	NC	
AY39	NC	
BA1	NC	
BA2	NC	
BA3	NC	
BA4	NC	
BA5	NC	
BA6	NC	
BA7	NC	
BA8	NC	
BA9	NC	
BA10	NC	
BA11	NC	
BA12	NC	
BA13	NC	
BA14	NC	
BA15	NC	
BA16	NC	
BA17	NC	
BA18	NC	
BA19	NC	
BA20	NC	
BA21	NC	
BA22	NC	
BA23	NC	
BA24	NC	
BA25	NC	
BA26	NC	
BA27	NC	
BA28	NC	
BA29	NC	
BA30	NC	
BA31	NC	
BA32	NC	
BA33	NC	
BA34	NC	
BA35	NC	
BA36	NC	
BA37	NC	
BA38	NC	
BA39	NC	
AK10	DACVDD	
AK8	DACGND	
AH8	DACBLUE	GPU_B
AJ10	DACGREEN	GPU_G
AJ9	DACRED	GPU_R
AJ8	DACRSET	GPU_RSET1
AK9	DACVREF	GPU_DACVREF1
D3	THERMDC	GPU_THERMDC_TP
E3	THERMDA	GPU_THERMDA_TP
B30	MSTRAPSEL0	GPU_MSTRAPSEL<0>
B29	MSTRAPSEL1	GPU_MSTRAPSEL<1>
A30	MSTRAPSEL2	GPU_MSTRAPSEL<2>
A29	MSTRAPSEL3	GPU_MSTRAPSEL<3>
AH7	XTALSSIN	GPU_SSCLK_IN
AJ7	XTALIN	CLK27M_GPU_XIN
AK7	XTALOUT	CLK27M_GPU_XOUT
AH6	XTALOUTBUFF	GPU_CLK27M_UF

DVOCLKOUT* NOT USED IN HIGH SWING
DVOCLKIN IS USED ONLY FOR EXTERNAL TV OUT SUPPORT
DVO<7..0> HARDWARE DEBUG PORT
XTALOUTBUFF GENERATED INTERNALLY
EXTERNAL SPREAD SPECTRUM CLOCK INPUT

C263 0.01UF 20% 16V CERM 402

R164 113 1% 1/16W MF 402 · R605 75 1% 1/16W MF 402 · R149 75 1% 1/16W MF 402 · R165 75 1% 1/16W MF 402

DVO VREF

PLACE CLOSE TO PIN

R631 10K 5% 1/16W MF 402 · R633 10K 5% 1/16W MF 402 · R632 10K 5% 1/16W MF 402

R204 75 1% 1/16W MF 402 · R203 75 1% 1/16W MF 402 · R205 75 1% 1/16W MF 402 · R196 63.4 1% 1/16W MF 402 · C353 0.01UF 20% 16V CERM 402

R760 0 5% 1/16W MF 603 · C337 0.1UF 20% 10V CERM 402

R179 33 5% 1/16W MF 402 — GPU_CLK27M_OUT

R172 10M 5% 1/16W MF 402 (NO STUFF)
R171 0 5% 1/16W MF 402
Y2 SM-3 27.000M CRITICAL
C281 27PF 5% 50V CERM2 402 · C351 27PF 5% 50V CERM 402
Y2 LOAD CAPACITANCE IS 18PF

+3V_SLEEP
GPU_SS L19 FERR-EMI-100-OHM SM
SPREAD SPECTRUM SUPPORT

C629 10UF 20% 6.3V CERM 805 · C634 0.1UF 20% 10V CERM 402

R614 0 5% 1/16W MF 402 (NO STUFF) · R623 0 5% 1/16W MF 402
R613 0 5% 1/16W MF 402 (NO STUFF) · R180 0 5% 1/16W MF 402 (NO STUFF)
R615 0 5% 1/16W MF 402 (NO STUFF) · R619 0 5% 1/16W MF 402 (NO STUFF)

U46 CY25811 SOI
XIN/CLKIN · XOUT · SSCLK · FRSEL · S1 · S0 · VSS
CRITICAL
CY25811_S1 · CY25811_S0

R620 33 5% 1/16W MF 402

THERE'S 20K (10K/10K) RESISTOR DIVIDER ON CHIP - SO M IS TO FLOAT THE LINES
S0=1;S1=M => -1.5% DOWN-SPREAD

MAP17 BOOT STRAPS

R233 10K · R210 10K · R213 10K · R200 10K · R238 10K · R184 10K (NO STUFF) · R211 10K · R234 10K · R222 10K (NO STUFF) · R159 10K (NO STUFF) · R223 10K · R195 10K

R232 10K · R209 10K · R214 10K (NO STUFF) · R197 10K · R235 10K (NO STUFF) · R221 10K · R212 10K · R239 10K · R190 10K · R243 10K · R160 10K · R224 10K (NO STUFF) · R208 10K

ROM TYPE <1..0> = 00: ONLY (NVIDIA CONFIRMED OKAY)
BUS TYPE = 1: AGP
PCI_DEVID<3..0> = 1001: MAP17(464)
RAM CONFIG<3..0> = 1101: 4MX32, 1 DQS PER BYTE, LOW DRIVE STRENGTH
SUBVENDOR = 0: NO VIDEO BIOS ROM
PCI_AD = 1: NORMAL AGP PIN OUT
CRYSTAL = 2: 27MHZ CRYSTAL

MSTRAPSEL WILL BE CONNECTED TO GND OR UNCONNECTED ON SUBSTRATE

GPU_MSTRAPSEL<3>	
GPU_MSTRAPSEL<2>	
GPU_MSTRAPSEL<1>	
GPU_MSTRAPSEL<0>	
GPU_VIPD6_CRYSTAL<1>	CRYSTAL<1>
GPU_DVOD<6>	CRYSTAL<0>
GPU_VIPD2_ROMTYPE<1>	
GPU_DVOD<10>	ROMTYPE<0>
GPU_DVOD<11>	BUSTYPE
GPU_DVO_HSYNC	DEVID<3>
GPU_VIPD3_PCI_DEVID<2>	DEVID<2>
GPU_VIPD5_PCI_DEVID<1>	DEVID<1>
GPU_VIPD4_PCI_DEVID<0>	DEVID<0>
GPU_DVOD<1>	SUBVENDOR
GPU_DVOD<0>	PCI_AD
GPU_DVOD<5>	RAMCFG<3>
GPU_DVOD<4>	RAMCFG<2>
GPU_DVOD<3>	RAMCFG<1>
GPU_DVOD<2>	RAMCFG<0>

L4 400-OHM-EMI SM-1 · L5 400-OHM-EMI SM-1 · L53 400-OHM-EMI SM-1

C844 10UF 20% 6.3V CERM 805 · C846 100PF 5% 50V CERM 402 · C848 100PF 5% 50V CERM 402
C845 10UF 20% 6.3V CERM 805 · C847 100PF 5% 50V CERM 402 · C849 100PF 5% 50V CERM 402
C850 100PF 5% 50V CERM 402 · C851 100PF 5% 50V CERM 402 · C852 10UF 20% 6.3V CERM 805
C24 10UF 20% 6.3V CERM 2 805

PLL NOISE SHOULD BE LESS THAN 100MV PEAK-TO-PEAK

R752 330 5% 1/16W MF 402

R748 10K · R749 10K · R750 10K 5% 1/16W MF 402 (NO STUFF)

U55 SIL1162 TSSOP

SI_DK<1>	27	SCL/DK1 IPD
SI_DK<0>	26	SDA/DK0 IPD
NC	24	CTL3/A2 IPD
SI_I2C_OFF	25	ISEL/RST*
MAIN_RESET_L	47	PD*
SI_EDGE	44	EDGE/HTPLG
GPU_DVOD<0>	18	D0
GPU_DVOD<1>	17	D1
GPU_DVOD<2>	16	D2
GPU_DVOD<3>	15	D3
GPU_DVOD<4>	14	D4
GPU_DVOD<5>	13	D5
GPU_DVOD<6>	10	D6
GPU_DVOD<7>	9	D7
GPU_DVOD<8>	8	D8
GPU_DVOD<9>	7	D9
GPU_DVOD<10>	6	D10
GPU_DVOD<11>	5	D11
GPU_DVO_DE	19	DE
GPU_DVO_HSYNC	20	HSYNC
GPU_DVO_VSYNC	21	VSYNC
GPU_DVO_CLKP	12	IDCK+
	11	IDCK-
	48	MSEN
	24	NC
	28	PVCC1
	46	PVCC2
	34	AVCC
	22	AVCC
	3	VCC
	2	VCC
	33	TXC+
	32	TXC-
	36	TX0+
	35	TX0-
	39	TX1+
	38	TX1-
	42	TX2+
	41	TX2-
	30	EXT_SWING
	2	VREF
	29	PGND
	45	PGND
	31	PGND
	43	AGND
	37	AGND
	1	GND
	23	GND
	4	GND
	49	THRML PAD

R757 10K · R751 10K 5% 1/16W MF 402 (NO STUFF)

SI_TMDS_DP<0> → TMDS_DP<0> · SI_TMDS_DN<0> → TMDS_DN<0> · SI_TMDS_CLKP → TMDS_CLKP · SI_TMDS_CLKN → TMDS_CLKN

SILICON IMAGE 1162 TMDS

RP55 0K 5% 1/16W SM1

MAP TMDS

RP57 0K 5% 1/16W SM1 (NO STUFF)

GPU_TMDS_CLKN	TMDS_CLKN
GPU_TMDS_CLKP	TMDS_CLKP
GPU_TMDS_DN<0>	TMDS_DN<0>
GPU_TMDS_DP<0>	TMDS_DP<0>

RP56 0K 5% 1/16W SM1 (OKAY PER ICT, NO_TEST=TRUE)

SI_TMDS_DP<2>	TMDS_DP<2>
SI_TMDS_DN<2>	TMDS_DN<2>
SI_TMDS_DP<1>	TMDS_DP<1>
SI_TMDS_DN<1>	TMDS_DN<1>

RP58 0K 5% 1/16W SM1 (NO STUFF)

GPU_TMDS_DN<1>	TMDS_DN<1>
GPU_TMDS_DP<1>	TMDS_DP<1>
GPU_TMDS_DN<2>	TMDS_DN<2>
GPU_TMDS_DP<2>	TMDS_DP<2>

SI_TMDS_CLKN	SI_CLKTMDS	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_CLKP	SI_CLKTMDS	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_DN<0>	SI_TMDS_D0	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_DP<0>	SI_TMDS_D0	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_DN<1>	SI_TMDS_D1	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_DP<1>	SI_TMDS_D1	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_DN<2>	SI_TMDS_D2	SI_TMDS:::50 8 MIL SPACING
SI_TMDS_DP<2>	SI_TMDS_D2	SI_TMDS:::50 8 MIL SPACING

SHOULD BE 10MIL SPACING
CHANGED TO 8MIL BECAUSE OF PACKAGE PWR PINS

GPU_TMDS_CLKN	GPU_CLKTMDS	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_CLKP	GPU_CLKTMDS	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_DN<0>	GPU_TMDS_D0	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_DP<0>	GPU_TMDS_D0	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_DN<1>	GPU_TMDS_D1	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_DP<1>	GPU_TMDS_D1	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_DN<2>	GPU_TMDS_D2	GPU_TMDS:::50 10 MIL SPACING
GPU_TMDS_DP<2>	GPU_TMDS_D2	GPU_TMDS:::50 10 MIL SPACING

MAP17 ANALOG DAC/BOOT STRAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L16 0.068uH SM — GPU_B — GPU_B_FILTR
L15 0.068uH SM — VGA_B
C618 4.7PF 5% 50V CERM 402
C616 3.3PF 0.25% 50V CERM 402
L11 0.068uH SM — GPU_G — GPU_G_FILTR
L10 0.068uH SM — VGA_G
C609 4.7PF 5% 50V CERM 402
C608 3.3PF 0.25% 50V CERM 402
L13 0.068uH SM — GPU_R — GPU_R_FILTR
L12 0.068uH SM — VGA_R
C617 4.7PF 5% 50V CERM 402
C615 3.3PF 0.25% 50V CERM 402

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

CRITICAL
L17 165-OHM SM SYM_VER-1
TMDS_CLKP — TMDS_CONN_CLKP
TMDS_CLKN — TMDS_CONN_CLKN

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP — F1 0.5AMP-13.2V F-RT-TH SM CRITICAL — +5V_DDC_SLEEP_UF — L18 400-OHM-EMI SM-1 — +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 MBR0530 SM — DDC_CLK_ISO

J16 QH1112 F-RT-TH

TMDS_DN<0> TMDS_DP<0> TMDS_DN<1> TMDS_DP<1> TMDS_DN<2> TMDS_DP<2> TMDS_DN<3> TMDS_DP<3> TMDS_DN<4> TMDS_DP<4> TMDS_DN<5> TMDS_DP<5>
DVI_DDC_CLK_UF (+5V_DDC_SLEEP) DVI_DDC_DATA_UF
TMDS_CONN_CLKP TMDS_CONN_CLKN
VGA_VSYNC DVI_HPD_UF
VGA_B VGA_HSYNC VGA_R VGA_G

R575 4.7K 5% 1/16W MF 402
R570 4.7K 5% 1/16W MF 402
R584 100 5% 1/16W MF 402
R563 100 5% 1/16W MF 402
R564 100 5% 1/16W MF 402
C633 100pF 5% 50V CERM 402
C604 100pF 5% 50V CERM 402
C603 100pF 5% 50V CERM 402
C657 0.01UF 20% 50V CERM 603
R618 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R500 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND1 CHGND5

3V LEVEL SHIFTERS

+3V_SLEEP
Q29 2N7002DW SOT-363 — DVI_DDC_CLK — GPU_DVI_DDC_CLK
Q29 2N7002DW SOT-363 — DVI_DDC_DATA — GPU_DVI_DDC_DATA
Q68 2N7002DW SOT-363 — DVI_HPD — GPU_HPD
R576 10K 5% 1/16W MF 2402
R585 10K 5% 1/16W MF 2402
R607 100K 5% 1/16W MF 2402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

Q32 TP0610 SM — DVI_DDC_CLK_UF — DVI_TURN_ON — DVI_TRUN_ON_ILIM — DVI_TURN_ON_BASE — +5V_DDC_SLEEP
R603 680 5% 1/16W MF 402
R604 10K 5% 1/16W MF 402
R600 330 5% 1/16W MF 402
Q34 2N3904 SM — SOFT_PWR_ON_L

Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R593 68.1K 1% 1/16W MF 402
C625 0.1UF 20% 10V CERM 402
HPD_4V_REF
U45 LMC7211 SM — HPD_PWR_SW
DVI_HPD_UF — R577 10K 1% 1/16W MF 402 — DVI_HPD_DIV
R598 10K 1% 1/16W MF 402
R594 100K 1% 1/16W MF 402
Q33 2N7002DW SOT-363 — HPD_ON
+PBUS
Q70 TP0610 SM — COMP_ENABLE
R611 100K 5% 1/16W MF 402 — COMP_DISABLE
R754 100K 5% 1/16W MF 402
R755 330 5% 1/16W MF 402
R610 20K 5% 1/16W MF 402 — HPD_BASE
Q36 2N3904 SM
HPD_ON_RC
C853 47UF 20% 6.3V CERM 1210
R756 68K 5% 1/16W MF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN — R671 100K 5% 1/16W MF 402
Q33 2N7002DW SOT-363

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R272 100K 5% 1/16W MF 402
R267 100K 5% 1/16W MF 402
C865 0.001uF 20% 50V CERM 402 — NO STUFF
C433 0.001uF 20% 50V CERM 402
C405 0.001uF 20% 50V CERM 402
CHGND4

LVDS_DDC_CLK LVDS_DDC_DATA
+3V_LCD (LVDS DDC POWER)
NC

CRITICAL
J7 G-501973 FFC-SM

LVDS_L0N LVDS_L0P LVDS_L1N LVDS_L1P LVDS_L2N LVDS_L2P CLKLVDS_LN CLKLVDS_LP LVDS_U0N LVDS_U0P LVDS_U1N LVDS_U1P LVDS_U2N LVDS_U2P CLKLVDS_UN CLKLVDS_UP

C473 0.001uF 20% 50V CERM 402

INVERTER INTERFACE

+PBUS
L26 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q1 FDG6324L SC70-6
+5V_INV_UF_SW
L28 400-OHM-EMI SM-1
R256 100K 5% 1/16W MF 402
C418 10UF 20% 6.3V CERM 805
C709 0.001UF 20% 50V CERM 402
CRITICAL
J8 SM-2MT
FP_PWR_EN_L
Q1 FDG6324L SC70-6 — FP_PWR_EN
+5V_INV_SW
C713 0.001UF 20% 50V CERM 402
L29 400-OHM-EMI SM-1 — BRIGHT_PWM
C721 0.001UF 20% 50V CERM 402
+3V_PMU
C594 0.1UF 20% 10V CERM 402
INV_ON_PWM — 74LVC32 TSSOP — U32 — BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R2200 0 5% 1/16W MF 402
C601 0.01uF 20% 50V CERM 603

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW14 SM — GPU_TV_GND1 — L21 FERR-10-OHM-500MA SM — TV_GND1
C656 0.01UF 20% 50V CERM 603
L20 FERR-EMI-100-OHM SM — GPU_Y
C643 82PF 5% 50V CERM 402
C632 82PF 5% 50V CERM 402
CRITICAL J17 MINIDIN RT-TH MH1177 — TV_C — TV_Y — TV_COMP
L24 FERR-EMI-100-OHM SM — GPU_C
C690 82PF 5% 50V CERM 402
C688 82PF 5% 50V CERM 402
L22 FERR-EMI-100-OHM SM — GPU_COMP
C678 82PF 5% 50V CERM 402
C677 82PF 5% 50V CERM 402
XW15 SM — GPU_TV_GND2 — L23 FERR-10-OHM-500MA SM — TV_GND2
C676 0.01UF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

LCD POWER SWITCHES

+3V_MAIN
R320 100K 5% 1/16W MF 402
C462 2200pF 5% 50V CERM 603
R313 100K 5% 1/16W MF 402 — LCD_DIGON_L — LCD_PWREN_L
TSOP SI3443DV Q5
+3V_LCD_SW
L2 FERR-250-OHM SM
C443 0.001uF 20% 50V CERM 402
Q2 2N7002 SM — FP_PWR_EN
CHGND4

VIDEO CONNECTORS

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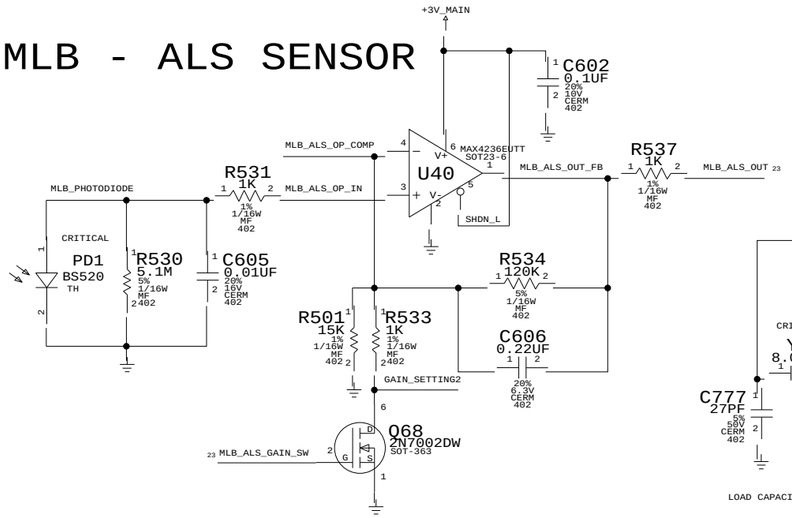
APPLE COMPUTER INC.

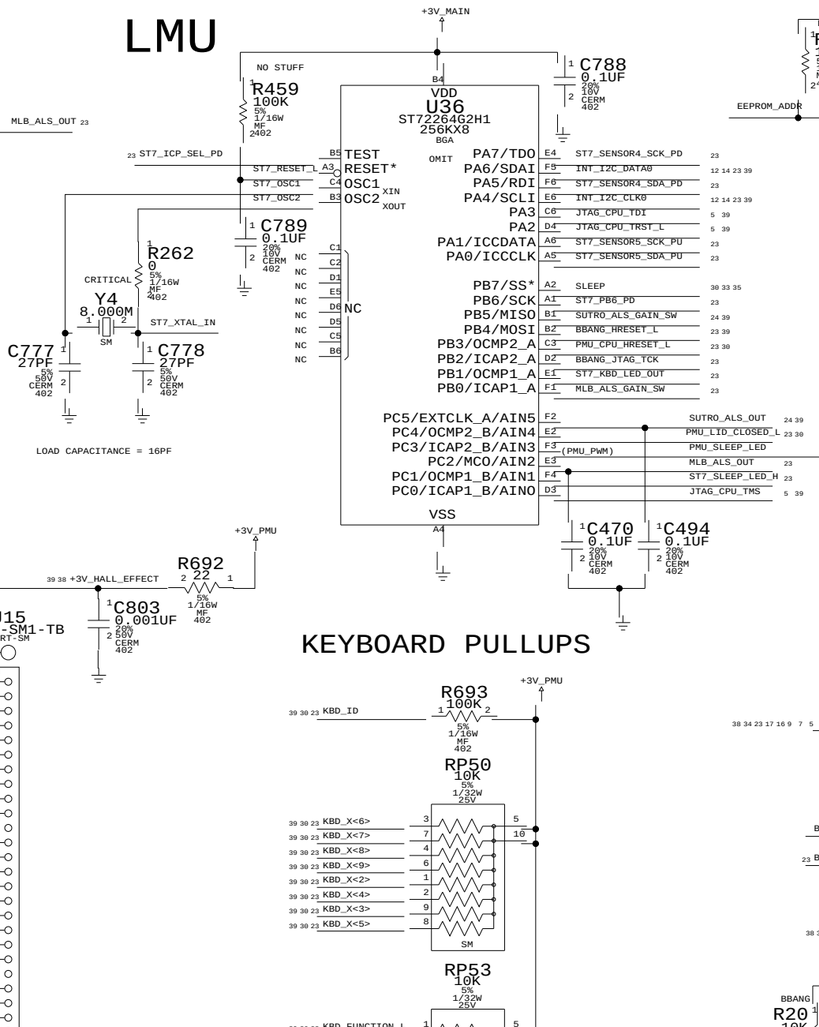
SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 22 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U36	CRITICAL	?

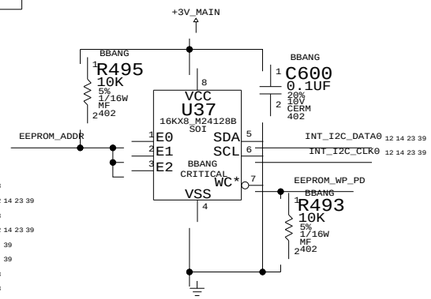
MLB - ALS SENSOR



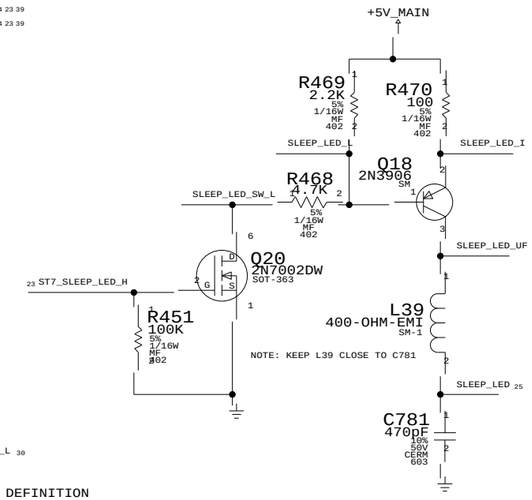
LMU



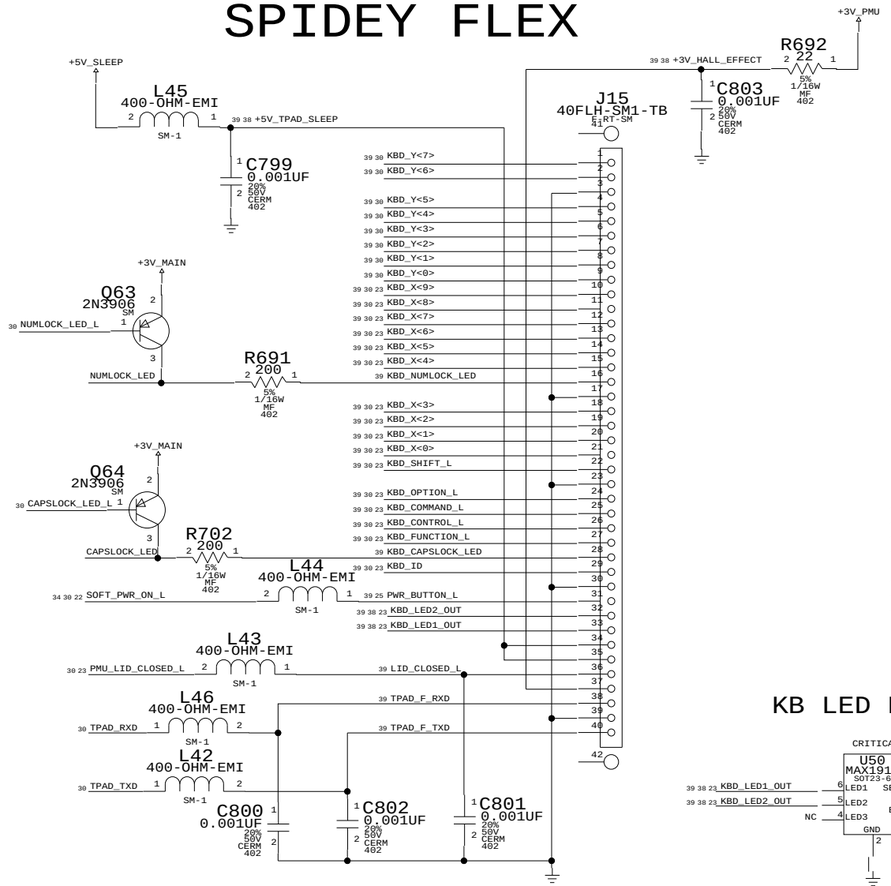
BOOT BANGER E2PROM



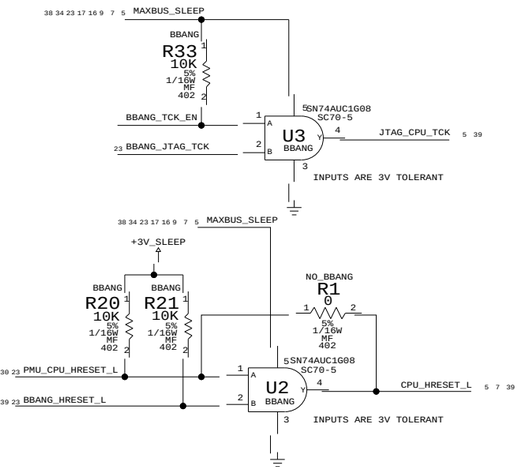
SLEEP LED



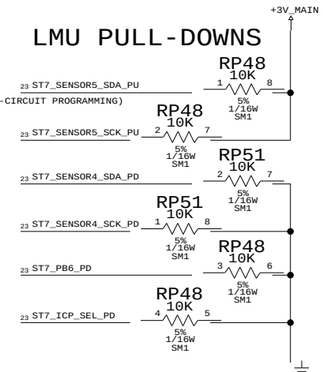
SPIDEY FLEX



KEYBOARD PULLUPS



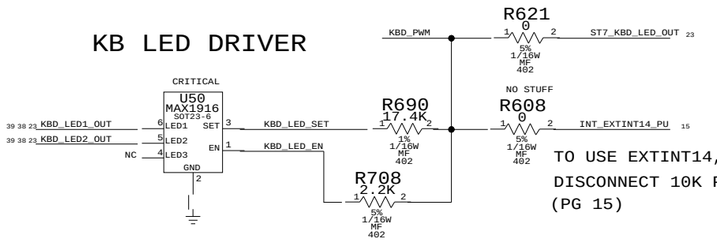
LMU PULL-DOWNS



BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

KB LED DRIVER



TO USE EXTINT14, NEED TO DISCONNECT 10K PULL-UP (PG 15)

LMU/BOOTBANGER/SPIDEY

APPLE COMPUTER INC.

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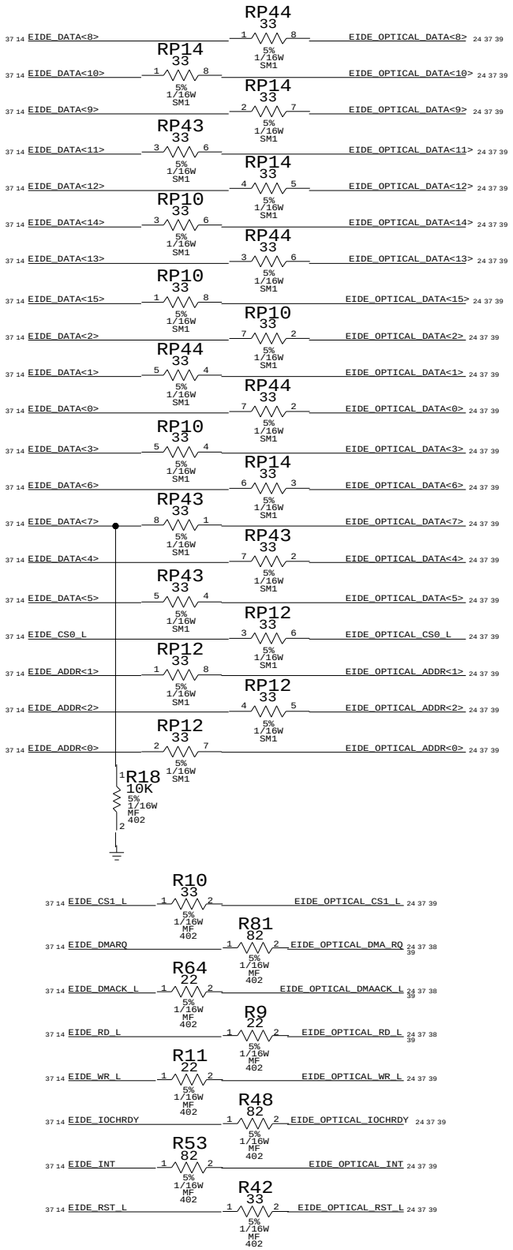
D	401228	0A
SCALE: NONE	SHT 23 OF 44	

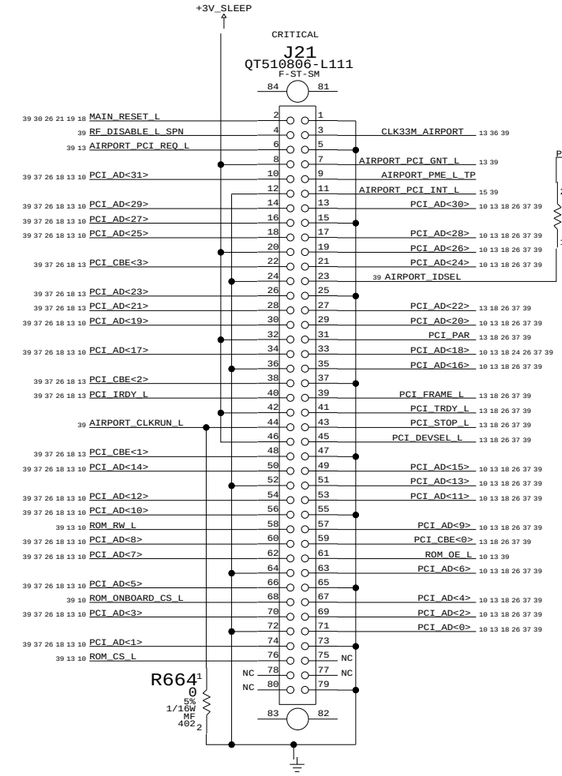
HARD DRIVE INTERFACE (UATA100)

EIDE SERIES TERMINATION

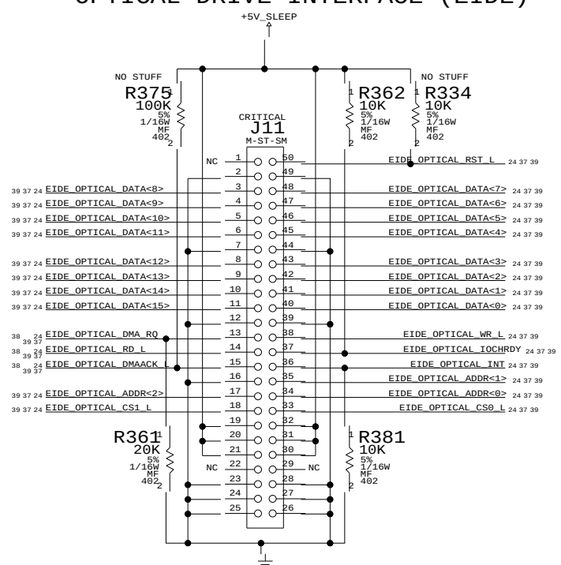
PLACE TERMINATORS NEAR INTREPID



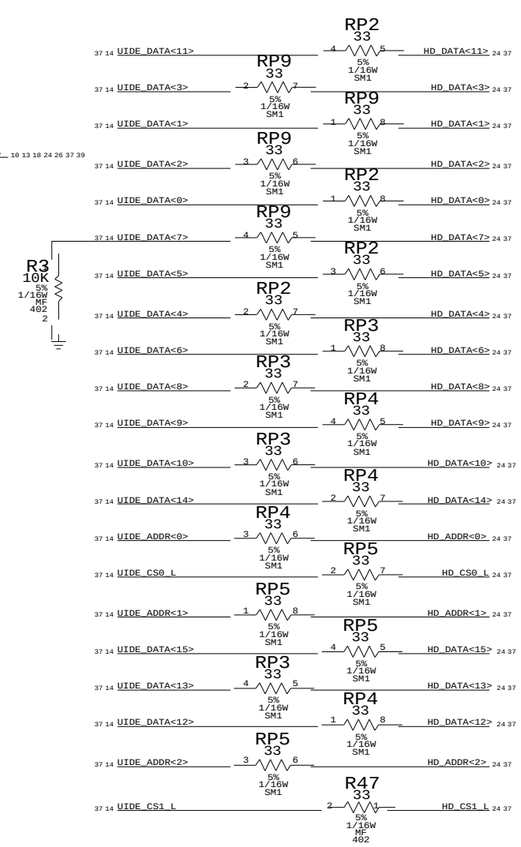
WIRELESS INTERFACE



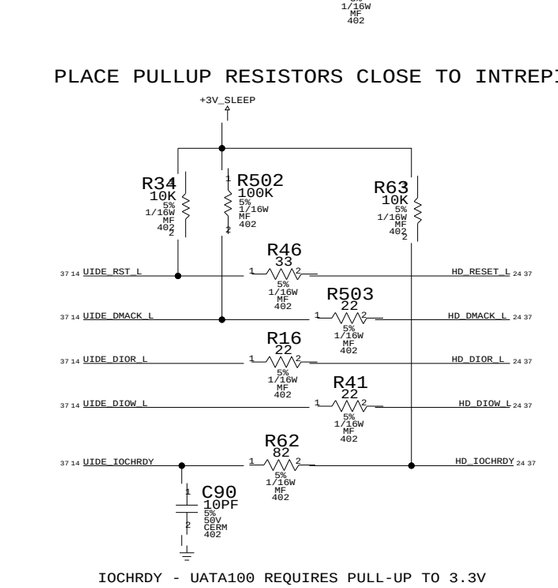
OPTICAL DRIVE INTERFACE (EIDE)



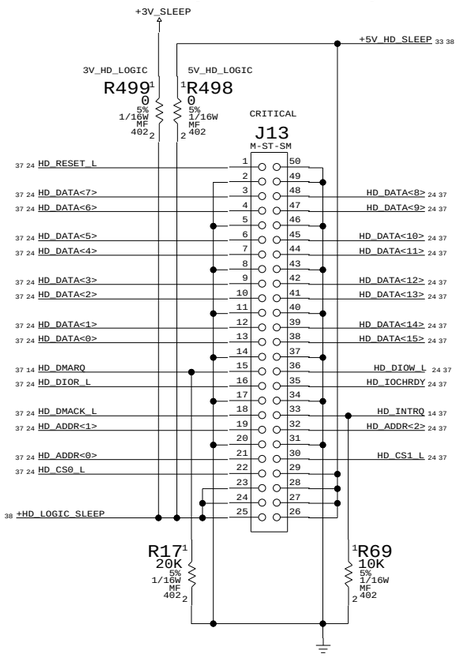
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

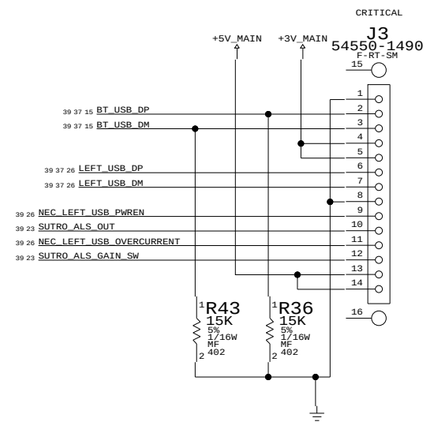


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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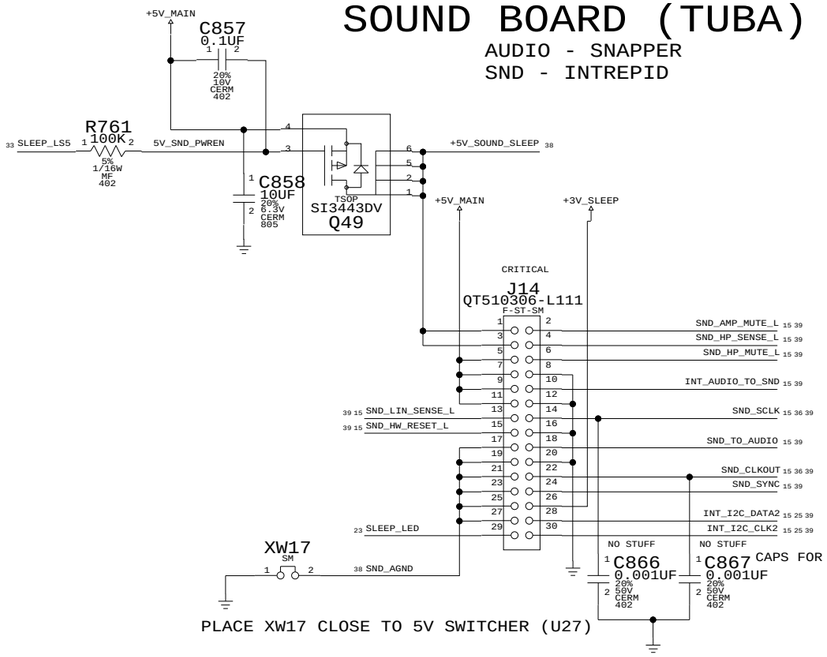
CR-25

SOUND BOARD (TUBA)

AUDIO - SNAPPER
SND - INTREPID

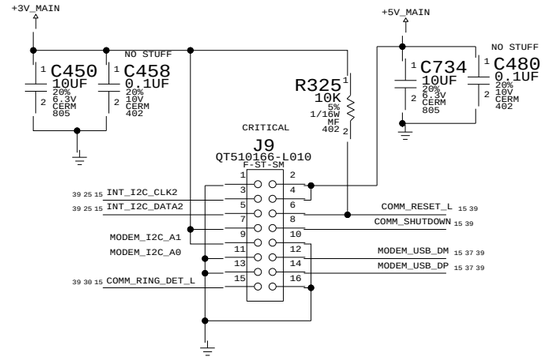


PLACE XW17 CLOSE TO 5V SWITCHER (U27)

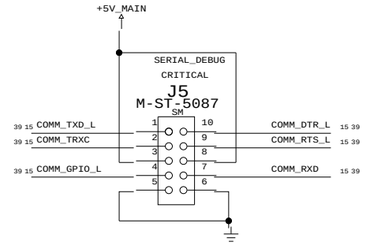
CAPS FOR EMI EXPERIMENTATION ONLY

MODEM

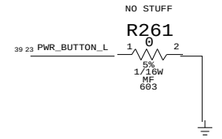
ARE THE 0.1UF NECESSARY ON A CONNECTOR?



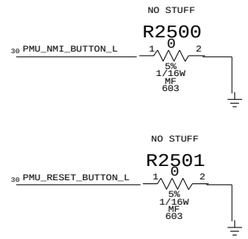
SERIAL DEBUG INTERFACE



DEBUG POWER BUTTON

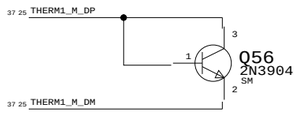


DEBUG JUMPERS

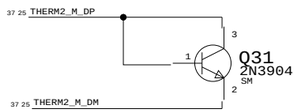


FAN INTERFACE

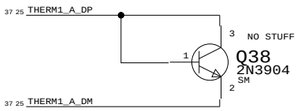
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN1



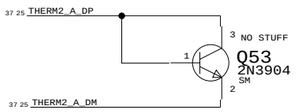
PLACE CLOSE TO CPU
MAIN2



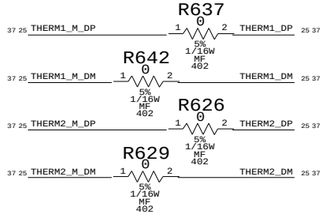
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



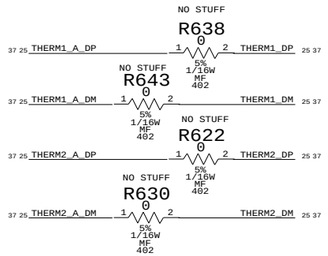
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



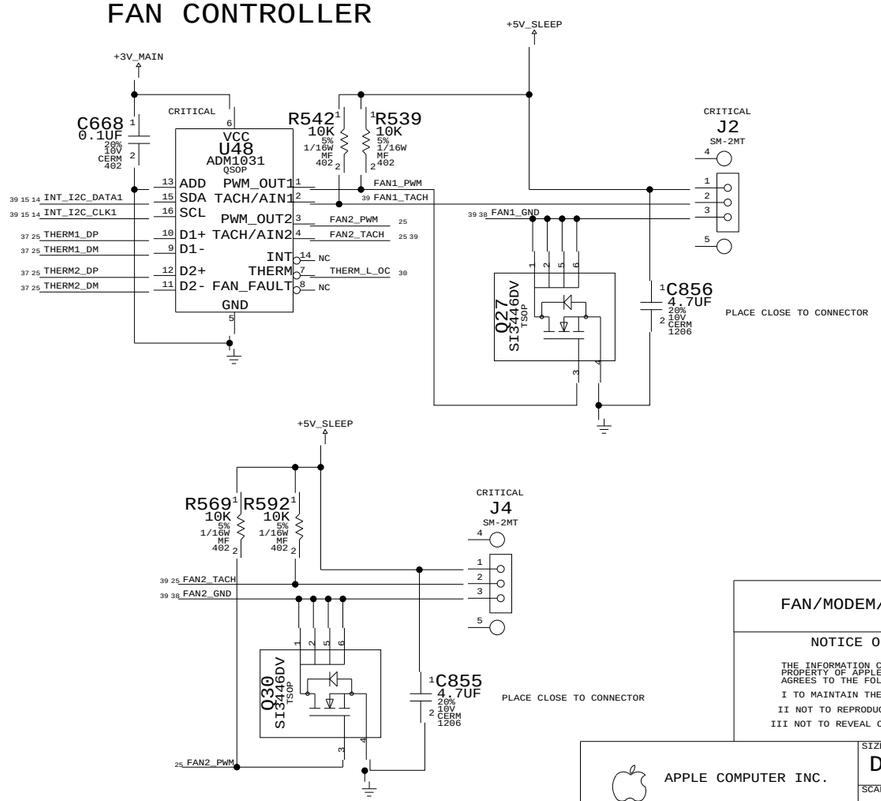
KEEP STUFFING RESISTORS CLOSE TO ADM1031 CONTROLLER



KEEP STUFFING RESISTORS CLOSE TO ADM1031 CONTROLLER



FAN CONTROLLER



FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

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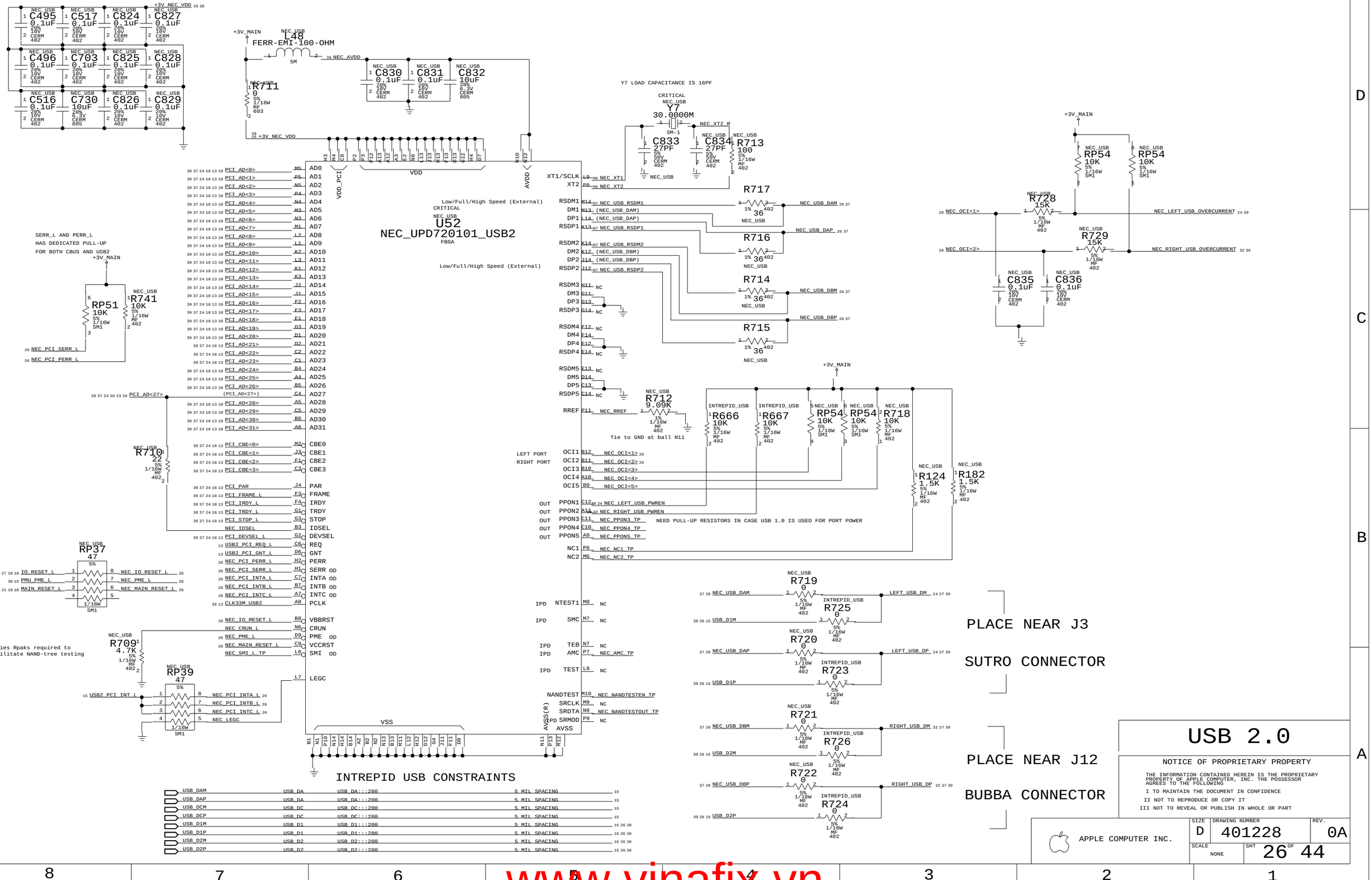

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

NO STUFF R703 0 5% 1/16W MF 402

C427 10uF 20% 6.3V CERM 805

U51 LTC3405 SOT23-6 (VIN, RUN, MODE, GND, SW, VFB)

3405_MODE

R704 0 5% 1/16W MF 402

LTC3405_SW

CRITICAL L47 3.3uH SM1

R705 665K 1% 1/16W MF 402 R2A

C456 22pF 5% 50V CERM 402

R706 49.9K 1% 1/16W MF 402 R2B

C464 10uF 20% 6.3V CERM 805

+1_0V_MARVELL

3405_VFB

R707 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R331 0 5% 1/16W MF 402 — CLKENET_LINK_TX / CLKENET_PHY_TX

R288 0 5% 1/16W MF 402 — CLKENET_LINK_RX / CLKENET_PHY_RX

R278 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF / CLKENET_PHY_GBE_REF

CRITICAL U49 88E1111 BCC

TX_CLK	CTRL10	NC
RX_CLK	DVDD	
125CLK	VDDO	
TXD0	VDDOH	
TXD1	VDDOX	
TXD2	AVDD	
TXD3	MDI0+	MDI_P<0>
TXD4	MDI0-	MDI_M<0>
TXD5	MDI1+	MDI_P<1>
TXD6	MDI1-	MDI_M<1>
TXD7	MDI2+	MDI_P<2>
TX_EN	MDI2-	MDI_M<2>
TX_ER	MDI3+	MDI_P<3>
GTX_CLK	MDI3-	MDI_M<3>
RXD0	LED_LINK10	LED_LINK10
RXD1	LED_LINK100	LED_LINK100
RXD2	LED_LINK1000	NC
RXD3	LED_DUPLEX	NC
RXD4	LED_RX	LED_RX_SPN
RXD5	LED_TX	NC
RXD6	CONFIG0	(000)
RXD7	CONFIG1	(000)
RX_DV	CONFIG2	(111)
RX_ER	CONFIG3	(110)
CRS	CONFIG4	(111)
COL	CONFIG5	(101)
MDC	CONFIG6	(000)
MDIO	TDI	JTAG_ENET_TDI
INT-/INT+	TDO	JTAG_ASIC_TDO_TP
RESET	TCK	JTAG_ASIC_TCK
COMA	TMS	JTAG_ASIC_TMS
S_IN+	TRST	JTAG_ASIC_TRST_L
S_IN-	RSET	ENET_RSET
S_OUT+	SEL_OSC	NC
S_OUT-	SEL_2.5V	
S_CLK+	GND	
S_CLK-		
HSDAC+		
HSDAC-		
XTAL1		
XTAL2		
VSSC		

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C452 0.1UF, C455 0.01UF, C710 0.1UF, C483 0.01UF, C484 0.1UF, C438 0.01UF

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C485 0.1UF, C428 0.01UF, C435 0.1UF, C466 0.01UF, C486 0.1UF, C479 10uF 6.3V CERM 805

+2_5V_MARVELL

R259 0 5% 1/16W MF 603

C457 0.1UF, C447 0.1UF, C474 0.1UF, C487 0.1UF

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

+2_5V_MARVELL_AVDD

L27 FERR-EMI-600-OHM SM

C719 0.1UF, C727 0.01UF, C702 0.1UF, C726 0.01UF, C718 10uF 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

CRITICAL J18 RJ45 RT-TH

RJ45_DP<0>, RJ45_C0_PD, RJ45_DN<0>, RJ45_DP<1>, RJ45_C1_PD, RJ45_DN<1>, RJ45_DP<2>, RJ45_C2_PD, RJ45_DN<2>, RJ45_DP<3>, RJ45_C3_PD, RJ45_DN<3>

Short shielded RJ-45

CHGND1

CRITICAL XFR-ENET-1000BT T1 SM

R289 49.9 1% 1/16W MF 402, R305 49.9, R315 49.9, R327 49.9

R297 49.9, R298 49.9, R323 49.9, R326 49.9

MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD

C426 0.01UF, C465 0.01UF, C431 0.01UF, C434 0.01UF

PLACE RESISTORS CLOSE TO PHY

R345 75, R328 75, R307 75, R290 75 5% 1/16W MF 402

ENET_CTAP_CHGND

C725 100pF 10% 3KV CERM 1808

CHGND1

SEE CONFIG TABLES (BELOW)

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

Q65 2N7002DW SOT-363 (x2)

D1 1N914 SOT23

R311 10K, R377 10K, R263 1.5K 5% 1/16W MF 402

R287 1K 5% 1/16W MF 402

INT_ENET_RST_L, IO_RESET_L, AC_IN, SLEEP_L_LS5, ENET_ENERGY_DET, ENET_RST_L, ENET_COMA

C425 2.2uF 20% 16V CERM 805

ENET_HSDACP, ENET_HSDACM

CLK25M_ENET_XIN, CLK25M_ENET_XOUT, ENET_VSSC

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R342 20K 5% 1/16W MF 402

R344 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M SM-2

CLK25M_XTAL_IN

C430 33pF 5% 50V CERM 402, C429 33pF

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R253 49.9 1% 1/16W MF 402, NO STUFF R254 49.9, R343 10K 5% 1/16W MF 402

R438 4.99K 1% 1/16W MF 402

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0603		Y3	

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

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D	401228	0A

SCALE: NONE — SHT 27 OF 44

DSX STRAP OPTIONS

0 -> BILINGUAL PORT
1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

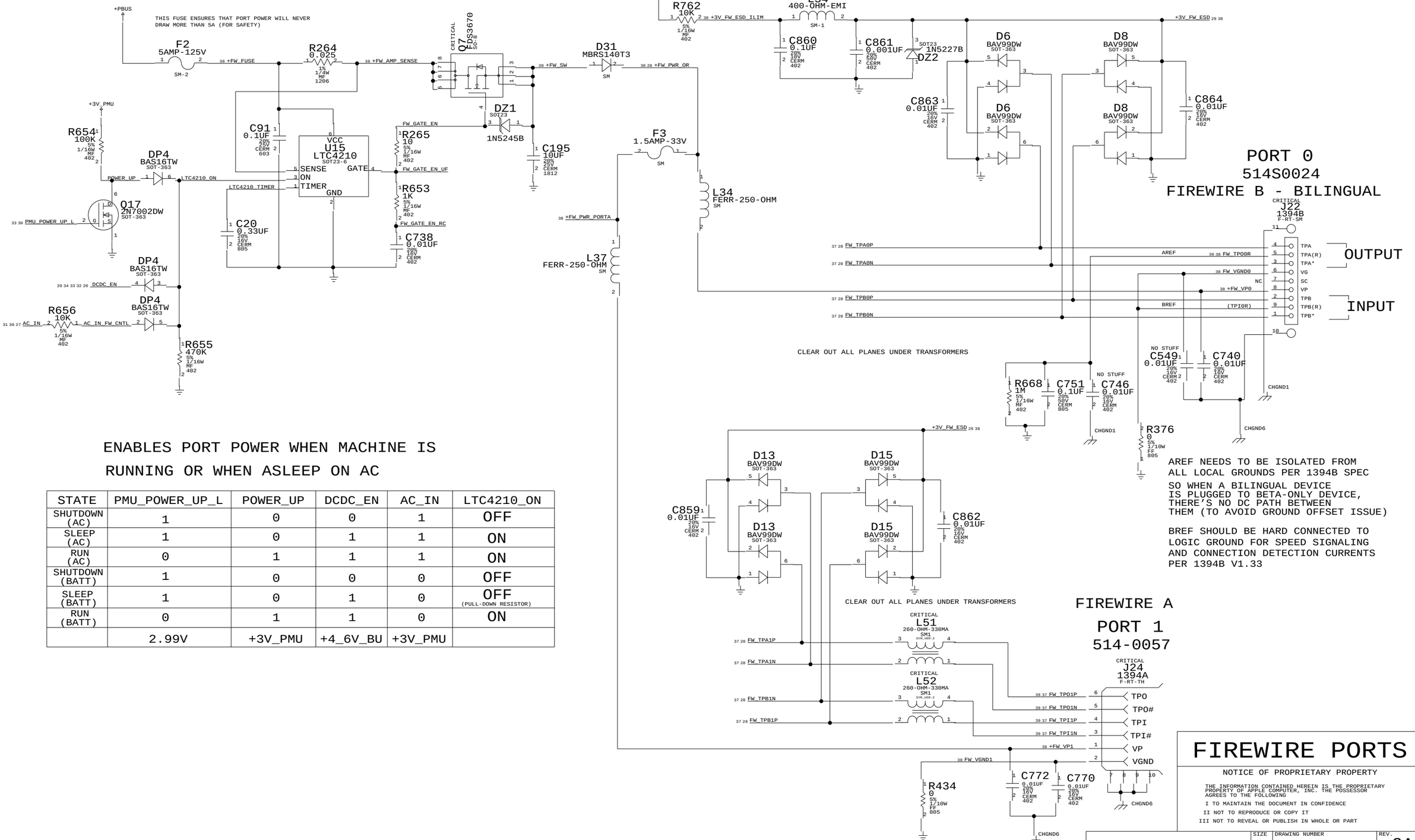
SPEC SAID TO USE 10K

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 401228 | REV. 0A

SCALE NONE | SHT 28 OF 44

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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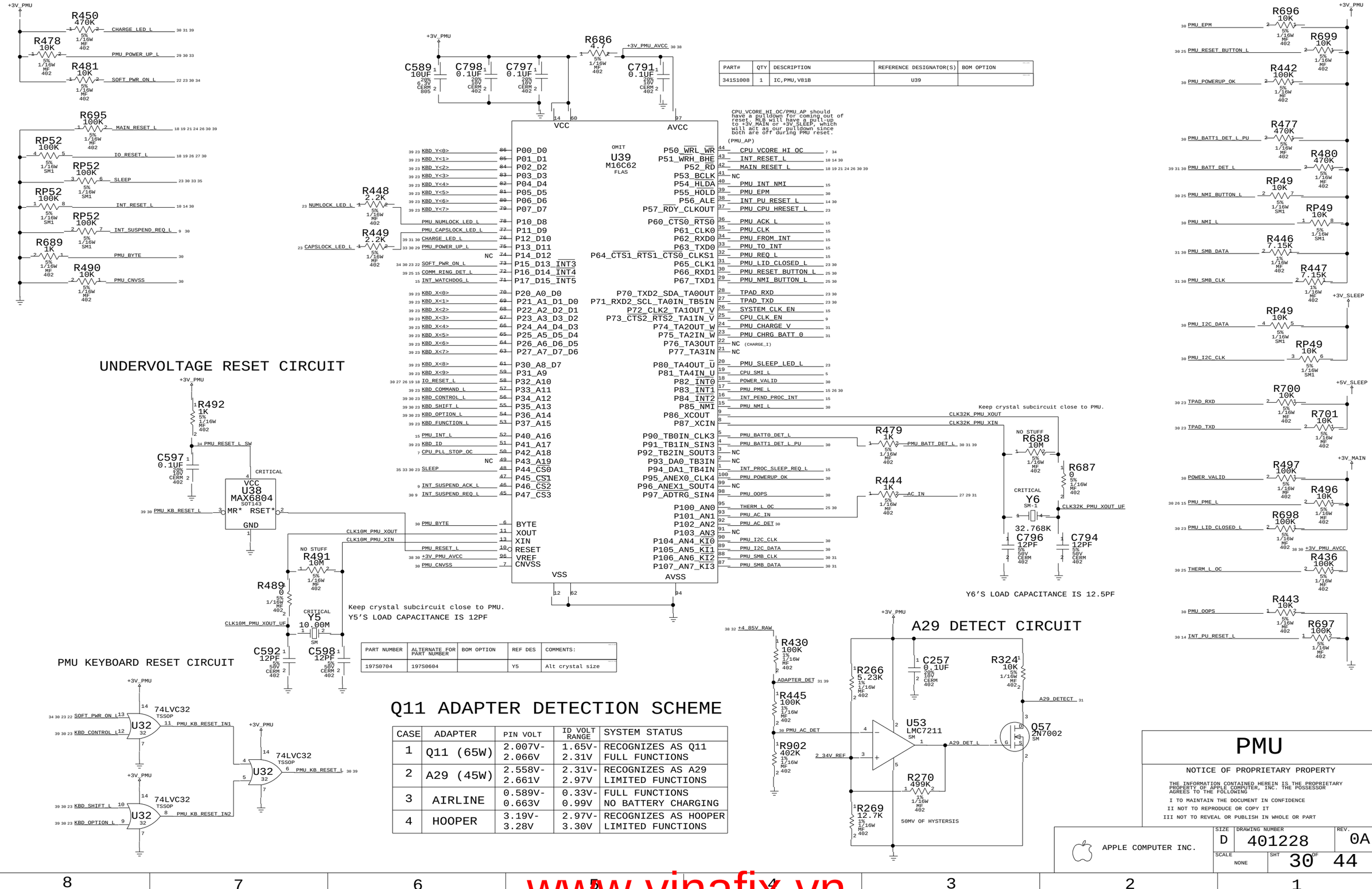
SCALE: NONE	SHT 29 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U39	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0604		Y5	Alt crystal size

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PMU

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APPLE COMPUTER INC.

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SCALE: NONE	SHT 30 OF 44	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J19
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET
R473 20K 1% 1/16W MF 402

DC INRUSH LIMITER

Q8 SI4435DY SOI
Q10 SI4435DY SOI
+ADAPTER_SW
+ADAPTER_SENSE
R336 330K 5% 1/16W MF 402
C439 0.1UF 20% 50V CERM 805
GATE
AC_ENABLE_GATE
R394 47K 5% 1/16W MF 402
R300 470K 5% 1/16W MF 402
AC_ENABLE_L
BCKFD_PROT_GATE
C843 0.1UF 20% 50V CERM 805
R414 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q14 2N7002DW SOT-363
AC_IN
C532 0.01UF 20% 50V CERM 603

+3V_PMU
R309 102K 1% 1/16W MF 402
R292 100K 1% 1/16W MF 402
C449 0.01UF 10% 100V CERM 402
R291 10K 1% 1/16W MF 402
1V20_REF
U16 LMC7211 SM
AC_DIV
R301 10K 1% 1/16W MF 402
R293 57.6K 1% 1/16W MF 402
R316 1M 5% 1/16W MF 402
AC_IN_L
Q4 2N7002DW SOT-363
R308 470K 5% 1/16W MF 402
GREATER THAN 13.5V DETECT

PLACE U24 NEXT TO R382
U24 SENSE VOLTAGE DROP ACROSS R382

U24 MAX4172 SOI
RS+ RS- PG NC NC1 NC2 OUT GND
MAX4172_OUT
R384 2.21K 0.1% 1/16W MF 603
CRITICAL

1MSEC INTEGRATION TIME
R744 1K 1% 1/16W MF 402
IAC_RC_COMP
C757 0.1UF 20% 10V CERM 402
+3V_PMU
C472 0.1UF 20% 10V CERM 402
CRITICAL
R745 42.2K 0.1% 1/16W FF 603
IAC_FB
U54 LMC7111 SOT23-5
R742 10K 1% 1/16W MF 402
CURRENT_THRESHOLD
CRITICAL
R743 42.2K 0.1% 1/16W FF 603
CRITICAL
R371 82.5K 0.1% 1/16W FF 603
A29_CURRENT_ADJ
Q3100 2N7002DW SOT-363
A29_DETECT
+3V_PMU
R747 100K 5% 1/16W MF 402
AC_GTR_18V
Q66 2N7002DW SOT-363
1772_ACOK_L

PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
DP3 BAS16TW SOT-363
LTC1625_ITH
R383 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG
CRITICAL
R746 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
OVER_18V_ADJ
Q3100 2N7002DW SOT-363
C838 1UF 20% 10V CERM 603

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

CRITICAL
R382 0.025 1% 1W MF 2512
R406 4.7 5% 1/16W MF 402
R413 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
C534 0.47UF 20% 50V CERM 1206
C535 0.47UF 20% 50V CERM 1206
CSSP
CSSN
R663 100K 1% 1/16W MF 402
D10 1N914 SOT23
C550 1UF 20% 50V CERM 1210
R665 12.7K 1% 1/16W MF 402
1772_DCIN
1772_ACIN
1772_ACOK_L
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
U30 MAX1772 QSOP
DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS CSSP CSSN CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT REF 4.096V GND
CRITICAL
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN
R678 33 5% 1/8W FF 1206
D11 1N914 SOT23
1772_BST_ESR
R458 100K 5% 1/10W MF 402
C490 0.1UF 20% 25V CERM 603
R685 4.7 5% 1/16W MF 603
C557 0.1UF 20% 50V CERM 805
C773 1UF 20% 10V CERM 603
C782 0.1UF 20% 25V CERM 603
C768 0.1UF 20% 25V CERM 603
R435 1K 1% 1/16W MF 402
C570 0.01UF 20% 16V CERM 402
C565 0.01UF 20% 16V CERM 402
1772_CCV_RC
1772_REF
R412 1K 1% 1/16W MF 402
C569 0.1UF 20% 10V CERM 402
C580 1UF 20% 10V CERM 603
R683 10K 1% 1/16W MF 402
1772_CLS
R679 4.12K 1% 1/16W MF 402
R465 100K 5% 1/16W MF 402
1772_GND
+BATT_VSNS
XW20 SM
R455 1K 1% 1/16W MF 402
BATT_LOW_L
R475 1K 1% 1/16W MF 402
R474 48.7K 1% 1/16W MF 402
R466 4.12K 1% 1/16W MF 402
R476 27.4K 1% 1/16W MF 402
R464 10K 1% 1/16W MF 402
R457 10K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V

BATTV_HIGH
Q19 2N7002DW SOT-363
R488 5.23K 1% 1/16W MF 402
BATTV_LOW
Q19 2N7002DW SOT-363
PMU_CHARGE_V
Q22 2N7002DW SOT-363
Q22 2N7002DW SOT-363
R467 100K 5% 1/16W MF 402

+3V_PMU
R486 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q23 2N7002DW SOT-363
PMU_CHRG_BATT_0
Q23 2N7002DW SOT-363

SWITCHER VOLTAGE CONTROL
PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL
CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU
C564 0.1UF 20% 16V CERM 402
U35 LMC7211 SM
BATT_LOW
R680 100K 1% 1/16W MF 402
R487 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R682 100K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
C774 0.047UF 10% 16V CERM 402

R332 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q66 2N7002DW SOT-363
A29_DETECT

V_{BATT} = CELLS X (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))
For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN
I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})

BATTERY CONNECTOR
CRITICAL
J25
87438-0833
M-RT-SM
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG
L7 FERR-EMI-100-OHM SM
L9 FERR-50-OHM SM
L8 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L6 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L40 FERR-50-OHM SM

+24V_PBUS
C515 2.2UF 20% 50V CERM 1812
C524 2.2UF 20% 50V CERM 1812
C525 2.2UF 20% 50V CERM 1812
C526 2.2UF 20% 50V CERM 1812
C527 2.2UF 20% 50V CERM 1812
CRITICAL
Q54 IRF7805 SM
CRITICAL
Q55 IRF7811W SO-8
+BATT_RSNS
CRITICAL
L36 10uH SM1
CRITICAL
R677 0.05 1% 1W MF 2512
D29 MBRS140T3 SM
+BATT_24V_FUSE
C568 4.7UF 20% 25V CERM 1210
C582 4.7UF 20% 25V CERM 1210
C581 4.7UF 20% 25V CERM 1210
C583 4.7UF 20% 25V CERM 1210
C566 4.7UF 20% 25V CERM 1210
C567 4.7UF 20% 25V CERM 1210
C795 33UF 20% 25V ELEC SM1
R441 1 5% 1/16W MF 603
R421 1 5% 1/16W MF 603

BATTERY SWITCH-OVER CIRCUIT

+BATT
F5 5AMP-125V SM-2
F4 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE
D30 RS3AB SM
D28 RS3AB SM
Q16 SI4435DY SOI
Q60 SI4435DY SOI
R407 47K 5% 1/16W MF 402
R660 47K 5% 1/16W MF 402
BATT_24V_GATE
BATT_14V_GATE
R422 10K 1% 1/16W MF 402
R657 10K 1% 1/16W MF 402
DP3 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
Q14 2N7002DW SOT-363
AC_IN_L
DP3 BAS16TW SOT-363
R415 470K 5% 1/16W MF 402
AC_IN_L_RC
C551 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

BATTERY CHARGER

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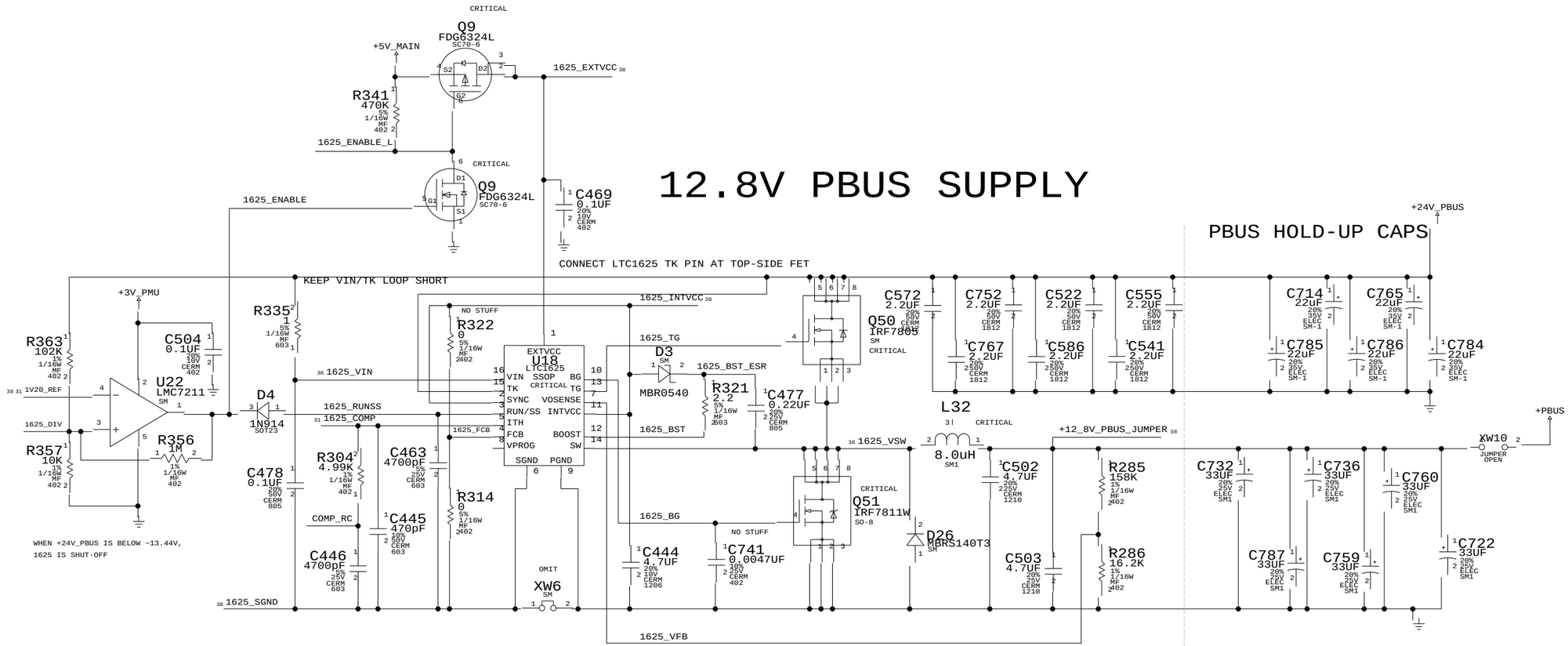
APPLE COMPUTER INC.

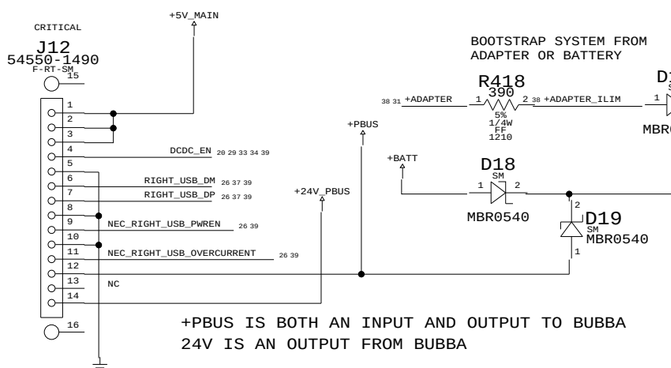
SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 31 OF 44	

CR-32

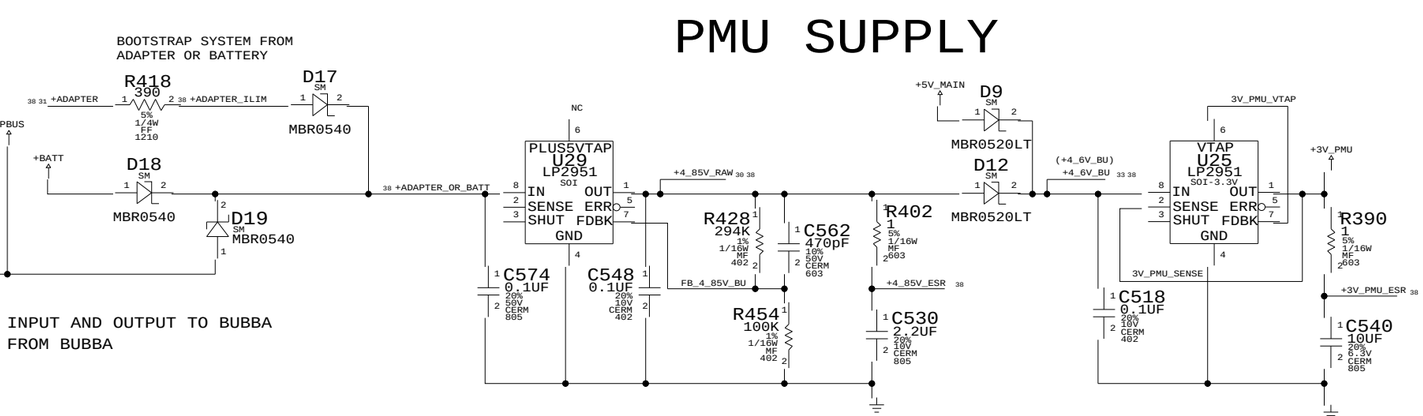
12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY



12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 32 OF 44	

3.3V/5V MAIN SUPPLY

+24V_PBUS

C492 2.2UF 20% 50V CERM 1812
C468 2.2UF 20% 50V CERM 1812
C729 2.2UF 20% 50V CERM 1812
C737 2.2UF 20% 50V CERM 1812
38 5V_RSNS
L33 CRITICAL
R651 0.005 1% 1/4W FF 1206
+5V_MAIN
XW5 JUMPER OPEN
38 +5V_MAIN_JUMPER
C720 330UF 20% 6.3V TANT SMD
C723 22UF 20% 6.3V CERM 1210
C724 22UF 20% 10V CERM 1210
R303 10 5% 1/16W MF 402
R296 10 5% 1/16W MF 402
D22 MBRS1401T3 SM
CRITICAL Q52 SI4888DY SOI
CRITICAL Q43 SI4888DY SOI
C454 0.001UF 10% 50V CERM 402
R387 113K 1% 1/16W MF 402
C528 180PF 5% 50V CERM 402
R386 21.5K 1% 1/16W MF 402
D7 SM MBR0540
R360 1M 5% 1/16W MF 402
5V_BOOST_ESR
C512 0.22UF 20% 25V CERM 805
R380 2.2 5% 1/16W MF 603
R379 0 5% 1/16W MF 402
NO STUFF
R395 0 5% 1/16W MF 402
C529 4.7UF 20% 10V CERM 1206
38 3707_INTVCC
3V_TG
R427 1M 5% 1/16W MF 402
D14 SM MBR0540
3V_BOOST_ESR
R401 2.2 5% 1/16W MF 603
C547 0.22UF 20% 25V CERM 805
+5V_MAIN
U27 LTC3707 SSOP
EXT VCC INT VCC VIN 3.3 VOUT NC
TG1 BOOST1 SW1 BG1 SNS1+ SNS1- VOSNS1 ITH1 RUN/SS1 FCB FREQSET STBYMD SGND PGND
TG2 BOOST2 SW2 BG2 SNS2+ SNS2- VOSNS2 ITH2 RUN/SS2 PGOOD
5V_TG 5V_BOOST 38 5V_SW 5V_BG 37 5V_SNSP 37 5V_SNSM 5V_VOSNS 5V_ITH 5V_RUNSS
3V_BOOST 38 3V_SW 3V_BG 37 3V_SNSP 37 3V_SNSM 3V_VOSNS 3V_ITH 3V_RUNSS
3707_FSET 3707_FCB 3707_STBY 38 3707_SGND
C539 0.001UF 20% 50V CERM 402 5V_ITH_RC
C500 0.047UF 10% 16V CERM 402
R400 4.99K 1% 1/16W MF 402
C533 270PF 5% 25V CERM 402
C521 0.01UF 20% 16V CERM 402
R389 0 5% 1/16W MF 402
C560 0.001UF 20% 50V CERM 402
C561 0.1UF 20% 10V CERM 402
3V_ITH_RC
C559 270PF 5% 25V CERM 402
R426 4.99K 1% 1/16W MF 402
Q15 2N7002DW SOT-363
R431 1M 5% 1/16W MF 402
35 33 20 DCDC_EN_L
LTC3707_START_RC
XW11 SM
3V_5V_OK 35
C501 220PF 5% 25V CERM 402
THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED
D16 1N914 SOT23
C558 0.01UF 20% 16V CERM 402
5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

CRITICAL Q61 SI4888DY SOI
CRITICAL Q62 SI4888DY SOI
C771 2.2UF 20% 50V CERM 1812
C766 2.2UF 20% 50V CERM 1812
C743 2.2UF 20% 50V CERM 1812
C750 2.2UF 20% 50V CERM 1812
3V_RSNS 38
CRITICAL L35 4.8UH SM1
CRITICAL R424 0.005 1% 1/4W FF 1206
38 +3V_MAIN_JUMPER
XW12 JUMPER OPEN
+3V_MAIN
D33 MBRS140T3 1SM
C780 22UF 20% 6.3V CERM 1210
C793 22UF 20% 10V CERM 1210
C790 330UF 20% 6.3V TANT SMD
R439 10 5% 1/16W MF 402
R453 10 5% 1/16W MF 402
C573 0.001UF 20% 50V CERM 402
C545 180PF 5% 50V CERM 402
R417 63.4K 1% 1/16W MF 402
R423 20K 1% 1/16W MF 402

THERE'S NO 10UF INPUT CAP
BECAUSE Q21 IS PLACED AT
OUTPUT OF +3V_MAIN SWITCHER

+3V_MAIN
+3V_SLEEP
35 33 30 23 SLEEP
R452 100K 5% 1/16W MF 402
TSOP SI3443DV Q21
C585 2200pF 5% 50V CERM 603
3V_SLEEP_PWREN_L

+3V_SLEEP LOADS
1) CPU PLL Config Control
2) INTREPID - IIC PULL-UPS & OSCILLATOR
3) MAP17 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
7) AMBIENT LIGHT SENSOR
8) BOOT BANGER
9) HARD DRIVE (IF USING 3V LOGIC)
10) WIRELESS (IF POWERING OFF IN SLEEP)
11) PMU - IIC Pull-ups
12) FAN

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

+4_6V_BU 32 38
R416 470K 5% 1/16W MF 402
DCDC_EN 20 29 32 34 39
30 29 PMU_POWER_UP_L
R437 100K 5% 1/16W MF 402
35 33 20 DCDC_EN_L
Q17 2N7002DW SOT-363
35 33 30 23 SLEEP
Q15 2N7002DW SOT-363
C571 0.01UF 20% 16V CERM 402

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_MAIN
R302 100K 5% 1/16W MF 402
R274 100K 5% 1/16W MF 402
SLEEP_L_LS5 20 27 34 35
SLEEP_LS5 25 33
SLEEP_L_LS5_EN_L
35 33 30 23 SLEEP
R295 100K 5% 1/16W MF 402
Q3 2N7002DW SOT-363
R294 100K 5% 1/16W MF 402
SLEEP_LS5_EN_L
Q3 2N7002DW SOT-363
C437 0.01UF 20% 16V CERM 402

+5V_MAIN
33 25 SLEEP_LS5
R494 100K 5% 1/16W MF 402
5V_HD_PWREN
C596 10UF 20% 6.3V CERM 805
TSOP SI3443DV Q24
+5V_HD_SLEEP 24 38
C792 100UF 20% 10V TANT SMD-3
C599 0.01UF 20% 16V CERM 402
C628 0.1UF 20% 16V CERM 402
R612 100K 5% 1/16W MF 402
5V_SLEEP_PWREN
C626 10UF 20% 6.3V CERM 805
TSOP SI3443DV Q35
+5V_SLEEP
C623 100UF 20% 10V TANT SMD-3

+5V_SLEEP LOADS
1) HEADPHONE AMPLIFIER
2) OPTICAL DRIVE
3) DVI
4) TRACKPAD

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 401228	REV. 0A
	SCALE NONE	SHT 33 OF 44	

3.3V/5V REGULATOR

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

NEW 1.35V->1.30V 1GHZ@1.4V->667MHZ@1.15V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

+30MV OFFSET

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

Connect MAX1717 GND pin 13
to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1000	1	RES	0402	RES,MTL FILM,1/16W,0 OHM,5%,0402,SMD	0		1/16W	5%	R306	VCORE_NO_OFFSET

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

Fmax Test Connections

J6 M-ST-SM-52465-1217

VCORE SUPPLY

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D	401228	0A

SCALE: NONE SHT 34 OF 44

CR-35

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) L3 I/O
1) MCP I/O - IF USING D3COLD
1) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN
R1606 0 5% 1/16W MF 603
+1_5V_SLEEP_VIN
+1_5V_SLEEP
Q37 SI3446DV TSOP
38 19 16 +1_5V_LDO
NO STUFF
R1607 0 5% 1/16W MF 603
C683 10UF 20% 6.3V CERM 805
C689 2200pF 5% 50V CERM 603
THERE'S 100K PULL-UP ON PG 31 ALREADY
SLEEP_L_LSS 20 27 33 34

+1_5V_MAIN LOADS

1) INTREPID CORE

R385 100K 5% 1/16W MF 402
DP2 BAS16TW SOT-363
R399 20 5% 1/16W MF 402
38 MAX1715_VCC
C544 2.2UF 20% 10V CERM 805
NO STUFF
R351 0 5% 1/16W MF 2402
33 3V_5V_OK
C554 2.2UF 20% 10V CERM 805
NO STUFF
R349 0 5% 1/16W MF 2402
DP2 BAS16TW SOT-363
R373 1330K 5% 1/16W MF 402
33 20 DCDC_EN_L
MAX1715_ON_RC
Q13 2N7002 SM
C499 0.01UF 20% 25V CERM 402
38 MAX1715_TON
DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS
38 2_5V_ILIM
38 1_5V_ILIM
R348 158K 1% 1/16W MF 402
R353 158K 1% 1/16W MF 2402
MAX1715_GND 35 38
+PBUS
MAX1715_SKIP 38
+PBUS
CRITICAL C520 4.7UF 20% 25V CERM 1210
CRITICAL C538 4.7UF 20% 25V CERM 1210
+PBUS
CRITICAL C511 4.7UF 20% 25V CERM 1210
CRITICAL C491 4.7UF 20% 25V CERM 1210
R408 4.7 5% 1/16W MF 603
38 1_5V_BOOST
38 1_5V_BST
38 2_5V_BST
R398 4.7 5% 1/16W MF 603
38 2_5V_BOOST
C536 0.1UF 20% 25V CERM 603
CRITICAL C537 0.1UF 20% 25V CERM 603
38 1_5V_DH
CRITICAL Q48 IRF7805 SM
CRITICAL Q59 IRF7805 SM
38 2_5V_DH
38 2_5V_LX
38 2_5V_DL
38 35 1_5V_LX_F
38 29 1_5V_2_5V_OK
38 MAX1715_REF
35 38 1_5V_FB
NO STUFF R352 0 5% 1/16W MF 402
C476 1UF 20% 10V CERM 603
R350 0 5% 1/16W MF 402
38 1_5V_LX
38 1_5V_DL
OMIT XW8 SM
238 35 MAX1715_GND
CRITICAL Q47 IRF7811W SO-8
CRITICAL Q58 IRF7811W SO-8
D23 SM MBRS130LT3
D32 SM MBRS130LT3
CRITICAL L30 4.7UH SM4
CRITICAL L38 4.7UH SM4
OMIT XW3 JUMPER OPEN
OMIT XW19 JUMPER OPEN
R355 5.11K 1% 1/16W MF 2402
R354 10K 1% 1/16W MF 2402
1_5V_FB 35 38
POSCAPS C704 10UF 20% 6.3V CERM 805
POSCAPS C715 150UF 20% 6.3V TANT SMD-1
POSCAPS C708 150UF 20% 6.3V TANT SMD-1
POSCAPS C776 10UF 20% 6.3V CERM 805
POSCAPS C747 150UF 20% 6.3V TANT SMD-1
POSCAPS C744 150UF 20% 6.3V TANT SMD-1
POSCAPS C753 150UF 20% 6.3V TANT SMD-1
CHANGE R354 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

+2_5V_MAIN LOADS

1) MAP17 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

+2_5V_SLEEP LOADS

1) L3 CORE
2) FBCORE/FBIO IF USING D3COLD
3) L3 I/O IF L3_OVDD EXCEEDS 1.5V

+2_5V_MAIN
+2_5V_SLEEP
35 33 30 23 SLEEP
R231 100K 5% 1/16W MF 402
C401 10UF 20% 6.3V CERM 805
Q U9 TSOP SI3447DV
C396 2200pF 5% 50V CERM 603
2_5V_SLEEP_PWREN_L

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS
2) +1_5V_LDO

+3V_MAIN
C86 10UF 20% 6.3V CERM 805
R40 10 5% 1/16W MF 402
38 LTC3411_VCC
NO STUFF R67 10K 5% 1/16W MF 402
R552 1M 5% 1/16W MF 402
BURST MODE
SVIN PVIN U4 LTC3411 MSOP
38 LTC3411_SHDN
SHDN/RT SW
38 LTC3411_SYNC
CRITICAL SYNC/MODE VFB
PGOOD ITH
PGND SGND
CRITICAL L14 2.2UH SM1
38 1_8V_SW
38 1_8V_SW_F
+1_8V_MAIN
OMIT XW13 JUMPER OPEN
C613 10PF 5% 50V CERM 402
R546 887K 1% 1/16W MF 402
38 1_8V_VFB
C610 22UF 20% 10V CERM 1210
NO STUFF R75 10K 5% 1/16W MF 402
R553 1M 5% 1/16W MF 402
PULSE MODE
CONTINOUS MODE
C15 1UF 20% 10V CERM 603
R57 324K 1% 1/16W MF 402
38 LTC3411_ITH
R545 16.2K 1% 1/16W MF 402
LTC3411_ITH_RC 38
C619 1000PF 5% 25V CERM 603
R551 698K 1% 1/16W MF 402
OMIT XW1 SM
38 LTC3411_GND

+1_8V_MAIN
+1_8V_SLEEP
35 33 30 23 SLEEP
R143 100K 5% 1/16W MF 402
C256 10UF 20% 6.3V CERM 805
Q U5 TSOP SI3447DV
C214 2200pF 5% 50V CERM 603
1_8V_SLEEP_PWREN_L

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) L3_OVDD (IF NOT USING 1.5V)

1.5V/1.8V/2.5V SUPPLIES

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 35 OF 44	

CR-36

DIGITAL SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_ADDR<0..31>	:::1500:3100	5		250			83 MHZ	5 9
	CPU_ARTRY_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_BG_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_BR_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_CI_L	:::1500:2700	5		250				5 9
	CPU_DATA<0..31>	:::1100:2500	5		250			83 MHZ	6 9
	CPU_DATA<32..63>	:::1100:2500	5		250			83 MHZ	6 9
	CPU_DBG_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_DTI<0..2>	:::1500:2950	5		250				5 9
	CPU_DRDY_L_UF	:::500			250	10 MIL SPACING			5
	CPU_DRDY_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_GBL_L	:::1500:2500	5		250				5 9
	CPU_HIT_L	:::1500:2800	5		250	10 MIL SPACING			5 9
	CPU_QACK_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_QREQ_L	:::1500:2600	5		250	10 MIL SPACING			5 9
	CPU_TA_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_TBST_L	:::1500:2600	5		250	10 MIL SPACING			5 9
	CPU_TEA_L	:::1500:3000	5		250				5 9
	CPU_TS_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_TSIZ<0..2>	:::1500:3500	5		250				5 9
	CPU_TT<0..4>	:::1500:3400	5		250				5 9
	CPU_WT_L	:::1500:3100	5		250				5 9
L3 CACHE	L3_DATA<31..0>	::750:1250	4		200				6 8
	L3_DATA<63..32>	::750:1250	4		200				6 8
	L3_CNTL<1..0>	:::1200:1800	4		200				6 8
	L3_ADDR<17..0>	:::1200:1800	4		200				6 8
GROUP 0	MEM_DATA<7..0>	:::1600	4		200			167 MHZ	10 11
	RAM_DATA_A<7..0>	:::1550	4	RAM_GROUP0_A:::450	200			167 MHZ	11 12
	RAM_DATA_B<7..0>	:::2150	4	RAM_GROUP0_B:::600	200			167 MHZ	11 12
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET :::1600	4		200			167 MHZ	10 11
	RAM_DQS_A<0>	:::1550	4	RAM_GROUP0_A:::450	200			167 MHZ	11 12
	RAM_DQS_B<0>	:::2150	4	RAM_GROUP0_B:::600	200			167 MHZ	11 12
	MEM_DQM<0>	:::1600	4		200			167 MHZ	10 11
	RAM_DQM_A<0>	:::1550	4	RAM_GROUP0_A:::450	200			167 MHZ	11 12
	RAM_DQM_B<0>	:::2150	4	RAM_GROUP0_B:::600	200			167 MHZ	11 12
GROUP 1	MEM_DATA<15..8>	:::1500	4		200			167 MHZ	10 11
	RAM_DATA_A<15..8>	:::1550	4	RAM_GROUP1_A:::700	200			167 MHZ	11 12
	RAM_DATA_B<15..8>	:::2100	4	RAM_GROUP1_B:::700	200			167 MHZ	11 12
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET :::1500	4		200			167 MHZ	10 11
	RAM_DQS_A<1>	:::1550	4	RAM_GROUP1_A:::700	200			167 MHZ	11 12
	RAM_DQS_B<1>	:::2100	4	RAM_GROUP1_B:::700	200			167 MHZ	11 12
	MEM_DQM<1>	:::1500	4		200			167 MHZ	10 11
	RAM_DQM_A<1>	:::1550	4	RAM_GROUP1_A:::700	200			167 MHZ	11 12
	RAM_DQM_B<1>	:::2100	4	RAM_GROUP1_B:::700	200			167 MHZ	11 12
GROUP 2/3	MEM_DATA<31..16>	:::1650	4		200			167 MHZ	10 11
	RAM_DATA_A<31..16>	:::1700	4	RAM_GROUP23_A:::850	200			167 MHZ	11 12
	RAM_DATA_B<31..16>	:::2200	4	RAM_GROUP23_B:::850	200			167 MHZ	11 12
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET :::1650	4		200			167 MHZ	10 11
	RAM_DQS_A<3..2>	:::1700	4	RAM_GROUP23_A:::850	200			167 MHZ	11 12
	RAM_DQS_B<3..2>	:::2200	4	RAM_GROUP23_B:::850	200			167 MHZ	11 12
	MEM_DQM<3..2>	:::1650	4		200			167 MHZ	10 11
	RAM_DQM_A<3..2>	:::1700	4	RAM_GROUP23_A:::850	200			167 MHZ	11 12
	RAM_DQM_B<3..2>	:::2200	4	RAM_GROUP23_B:::850	200			167 MHZ	11 12
GROUP 4/5	MEM_DATA<47..32>	:::1500	4		200			167 MHZ	10 11
	RAM_DATA_A<47..32>	:::1850	4	RAM_GROUP45_A:::900	200			167 MHZ	11 12
	RAM_DATA_B<47..32>	:::2350	4	RAM_GROUP45_B:::950	200			167 MHZ	11 12
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET :::1500	4		200			167 MHZ	10 11
	RAM_DQS_A<5..4>	:::1850	4	RAM_GROUP45_A:::900	200			167 MHZ	11 12
	RAM_DQS_B<5..4>	:::2350	4	RAM_GROUP45_B:::950	200			167 MHZ	11 12
	MEM_DQM<5..4>	:::1500	4		200			167 MHZ	10 11
	RAM_DQM_A<5..4>	:::1850	4	RAM_GROUP45_A:::900	200			167 MHZ	11 12
	RAM_DQM_B<5..4>	:::2350	4	RAM_GROUP45_B:::950	200			167 MHZ	11 12
GROUP 6	MEM_DATA<55..48>	:::1650	4		200			167 MHZ	10 11
	RAM_DATA_A<55..48>	:::1800	4	RAM_GROUP6_A:::800	200			167 MHZ	11 12
	RAM_DATA_B<55..48>	:::2400	4	RAM_GROUP6_B:::800	200			167 MHZ	11 12
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET :::1650	4		200			167 MHZ	10 11
	RAM_DQS_A<6>	:::1800	4	RAM_GROUP6_A:::800	200			167 MHZ	11 12
	RAM_DQS_B<6>	:::2400	4	RAM_GROUP6_B:::800	200			167 MHZ	11 12
	MEM_DQM<6>	:::1650	4		200			167 MHZ	10 11
	RAM_DQM_A<6>	:::1800	4	RAM_GROUP6_A:::800	200			167 MHZ	11 12
	RAM_DQM_B<6>	:::2400	4	RAM_GROUP6_B:::800	200			167 MHZ	11 12
GROUP 7	MEM_DATA<63..56>	:::1600	4		200			167 MHZ	10 11
	RAM_DATA_A<63..56>	:::1600	4	RAM_GROUP7_A:::500	200			167 MHZ	11 12
	RAM_DATA_B<63..56>	:::2200	4	RAM_GROUP7_B:::500	200			167 MHZ	11 12
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET :::1600	4		200			167 MHZ	10 11
	RAM_DQS_A<7>	:::1600	4	RAM_GROUP7_A:::500	200			167 MHZ	11 12
	RAM_DQS_B<7>	:::2200	4	RAM_GROUP7_B:::500	200			167 MHZ	11 12
	MEM_DQM<7>	:::1600	4		200			167 MHZ	10 11
	RAM_DQM_A<7>	:::1600	4	RAM_GROUP7_A:::500	200			167 MHZ	11 12
	RAM_DQM_B<7>	:::2200	4	RAM_GROUP7_B:::500	200			167 MHZ	11 12
ADDR	MEM_ADDR<12..0>	:::500	4					83 MHZ	10
	RAM_ADDR<12..0>	::2000:3000	6		200				10 12
	MEM_BA<1..0>	:::500	4						10
	RAM_BA<1..0>	::2000:3300	6		200				10 12
CONTROL	MEM_CS_L<3..0>	:::500	4						10
	RAM_CS_L<3..0>	::1800:2500	6		200				10 12
	MEM_CKE<3..0>	:::500	4						10
	RAM_CKE<3..0>	::1800:2500	6		200				10 12
	MEM_RAS_L	:::500	4						10
	RAM_RAS_L	::2000:4100	6		200				10 12
	MEM_CAS_L	:::500	4						10
	RAM_CAS_L	::2000:4100	6		200				10 12
	MEM_WE_L	:::500	4						10
	RAM_WE_L	::2000:3100	6		200				10 12
	MEM_MUXSEL_H<1..0>	:::500	3						10 11
	MEM_MUXSEL_L<1..0>	:::500	3						10 11
	RAM_MUXSEL_H	::1800:2600	5						11
	RAM_MUXSEL_L	::1800:2600	5						11

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	DELAY_RULE	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF	:::150					10 MIL SPACING	167 MHZ	9
	SYSCLK_CPU	::2650:2750		3	250	200	10 MIL SPACING	167 MHZ	5 9
	TNT_CPUFB_OUT	:::150		3	250		10 MIL SPACING	167 MHZ	9
	TNT_CPUFB_OUT_SHORT	::700:850		3	250		10 MIL SPACING	167 MHZ	9
	TNT_CPUFB_OUT_NORM	::500:600		3	250		10 MIL SPACING	167 MHZ	9
	TNT_CPUFB_IN_NORM	::500:600		3	250		10 MIL SPACING	167 MHZ	9
	TNT_CPUFB_LONG	::1050:1150		3	250		10 MIL SPACING	167 MHZ	9
	TNT_CPUFB_IN	::700:800		3	250	200	10 MIL SPACING	167 MHZ	9
	SYSCLK_DDRCLK_A0_UF	:475:575		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A0_L_UF	:475:575		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A1_UF	:300:400		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A1_L_UF	:300:400		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B0_UF	:430:530		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B0_L_UF	:430:530		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B1_UF	:400:510		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B1_L_UF	:400:510		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A0	::1850:1950 DDRCLK_A0	SYSCLK_DDRCLK_A0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_A0_L	::1850:1950 DDRCLK_A0	SYSCLK_DDRCLK_A0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_A1	::1925:2025 DDRCLK_A1	SYSCLK_DDRCLK_A1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_A1_L	::1925:2025 DDRCLK_A1	SYSCLK_DDRCLK_A1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B0	::2375:2475 DDRCLK_B0	SYSCLK_DDRCLK_B0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B0_L	::2375:2475 DDRCLK_B0	SYSCLK_DDRCLK_B0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B1	::2450:2550 DDRCLK_B1	SYSCLK_DDRCLK_B1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B1_L	::2450:2550 DDRCLK_B1	SYSCLK_DDRCLK_B1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	TNT_REF_CLK_OUT	::1250:1400		3	250	200	10 MIL SPACING	49.92 MHZ	15
	TNT_REF_CLK_IN	:::1900:2000		4	250	200	10 MIL SPACING	167 MHZ	15
	CLK66M_GPU_AGP_UF	:::150				200	10 MIL SPACING	66 MHZ	13
	CLK66M_GPU_AGP	::1400:1500		4	400	200	10 MIL SPACING	66 MHZ	13 19
	TNT_AGP_FB_OUT	:::150				200	10 MIL SPACING	66 MHZ	13
	TNT_AGP_FB_IN	::1400:1500		4	500	200	10 MIL SPACING	66 MHZ	13
	CLK33M_CBUS_UF	:::250				200	10 MIL SPACING	33 MHZ	13
	CLK33M_CBUS	::5000:6000	SHOULD BE AT MOST 4 VIAS FOR CLK	6	500	200	10 MIL SPACING	33 MHZ	13 18
	CLK33M_AIRPORT_UF	:::250				200	10 MIL SPACING	33 MHZ	13
	CLK33M_AIRPORT	::11000:12000	SHOULD BE AT MOST 4 VIAS FOR CLK	6	500	200	10 MIL SPACING	33 MHZ	13 24 39
	CLK33M_USB2_UF	:::250				200	10 MIL SPACING	33 MHZ	13
	CLK33M_USB2	::4000:6000	SHOULD BE AT MOST 4 VIAS FOR CLK	6	500	200	10 MIL SPACING	33 MHZ	13 26
	TNT_PCI_FB_OUT	:::300				200	10 MIL SPACING	33 MHZ	13
	TNT_PCI_FB_IN	::6500:7500		3	500	200	10 MIL SPACING	33 MHZ	13
L3 CACHE	L3_CLK<0>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
	L3_ECHO_CLK<0..1>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
	L3_CLK<1>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
	L3_ECHO_CLK<2..3>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
MAP17	GPU_CLK27M_OUT	:::400		3		200	10 MIL SPACING		21
	GPU_CLK27M_UF	:::250		3		200	10 MIL SPACING		21
	GPU_SSCLK_UF	:::200				200	10 MIL SPACING		21
	GPU_SSCLK_IN	:::920		3	500	200	10 MIL SPACING		21
	GPU_FBCLK0	:::250		3		200	10 MIL SPACING		19
	GPU_FBCLK0_L	:::250		3		200	10 MIL SPACING		19
	GPU_FBCLK1	:::250		3		200	10 MIL SPACING		19
	GPU_FBCLK1_L	:::250		3		200	10 MIL SPACING		19
	GPU_DVO_CLKP	::600:1300		3	250	200	10 MIL SPACING		21
CRYSTALS	CLK27M_GPU_XOUT	:::150					10 MIL SPACING		21
	CLK27M_XTAL_IN	:::250					10 MIL SPACING		21
	CLK27M_GPU_XIN	::300:400					10 MIL SPACING		21
	CLK18M_INT_XIN	::1400:1500					10 MIL SPACING		15
	CLK18M_INT_XOUT	::1300:1400					10 MIL SPACING		15
	CLK18M_XTAL_IN	:::300					10 MIL SPACING		15
	CLK18M_INT_EXT	:::400					10 MIL SPACING		15
	CLK25M_ENET_XIN	:::650					10 MIL SPACING		27
	CLK25M_ENET_XOUT	:::400					10 MIL SPACING		27
	NEC_XT1	::600:700					10 MIL SPACING		26
	NEC_XT2	::300:400	THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		26
SOUND	SND_SCLK			5	500	200	10 MIL SPACING		15 25 39
	SND_CLKOUT			5	500	200	10 MIL SPACING		15 25 39
ETHERNET MARVELL	CKENET_PHY_RX	:::300				200		125 MHZ	27
	CKENET_LINK_RX	::8000:9000		3	500	200	10 MIL SPACING	125 MHZ	14 27
	CKENET_PHY_GBE_REF	:::300				200		125 MHZ	27
	CKENET_LINK_GBE_REF	::8000:9000		3	500	200	10 MIL SPACING	125 MHZ	14 27
	CKENET_PHY_TX	:::300				200		25 MHZ	27
	CKENET_LINK_TX	::8000:9000		4	500	200	10 MIL SPACING	25 MHZ	14 27
	CKENET_LINK_GTX	:::300				200		125 MHZ	14
	CKENET_PHY_GTX	::8000:9000		3	500	200	10 MIL SPACING	125 MHZ	14 27
FIREWIRE	CLKFW_PHY_PCLK	:::300				200		49.152 MHZ	28
	CLKFW_LINK_PCLK	::7500:8000		3	500	200	10 MIL SPACING	49.152 MHZ	14 28
	CLKFW_PHY_LCLK	::7500:8000		3	500	200	10 MIL SPACING	49.152 MHZ	14 28
	CLKFW_LINK_LCLK	:::300				200		49.152 MHZ	14
	FW_XI	:::520				200	10 MIL SPACING	98.034 MHZ	28
	FW_OSC	:::300				200	10 MIL SPACING	98.034 MHZ	28

SIGNAL CONSTRAINTS - PAGE 1

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A

SCALE	SHT	OF
NONE	36	44

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>	::1350:1650	5	100				66 MHz	13 19
AGP BYTES 0-1	AGP_CBE<1..0>	::1350:1650	5	100				66 MHz	13 19
	AGP_AD_STB<0>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
AGP BYTES 2-3	AGP_AD_STB_L<0>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
	AGP_AD<31..16>	::1350:1650	5	100				66 MHz	13 19
	AGP_CBE<3..2>	::1350:1680	5	100				66 MHz	13 19
	AGP_AD_STB<1>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
	AGP_AD_STB_L<1>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
AGP SIDEBAND	AGP_SBA<7..0>	::1100:1700	5	100				66 MHz	13 19
	AGP_SB_STB	::1500:1700	4	100	350	8 MIL SPACING		66 MHz	13 19
	AGP_SB_STB_L	::1500:1700	4	100	350	8 MIL SPACING		66 MHz	13 19
AGP CONTROL	AGP_FRAME_L	::1200:1900	6	250				66 MHz	13 19
	AGP_IRDY_L	::1200:1900	6	250				66 MHz	13 19
	AGP_TRDY_L	::1200:1900	6	250				66 MHz	13 19
	AGP_DEVSEL_L	::1200:1900	6	250				66 MHz	13 19
	AGP_STOP_L	::1200:1900	6	250				66 MHz	13 19
	AGP_PAR	::1200:1900	6	250				66 MHz	13 19
	AGP_REQ_L	::1200:1900	6	250				66 MHz	13 19
	AGP_GNT_L	::1200:1900	6	250				66 MHz	13 19
	AGP_RBF_L	::1200:1900	6	250				66 MHz	13 19
DVO	GPU_DVOD<0..11>	::600:1300	5	250					21
	GPU_DVO_HSYNC	::600:1300	5	250					21
	GPU_DVO_VSYNC	::600:1300	5	250					21
PCI	PCI_AD<31..0>	::8000:13500				MIN_DAISY_CHAIN		33 MHz	10 13 18 24 26 39
	PCI_CBE<3..0>	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
	PCI_FRAME_L	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
	PCI_IRDY_L	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
	PCI_TRDY_L	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
	PCI_DEVSEL_L	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
	PCI_STOP_L	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
	PCI_PAR	::8000:13500				MIN_DAISY_CHAIN		33 MHz	13 18 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>	:::710		NEED TO MATCH DELAY TO 250	200			100 MHZ	14 24
	UIDE_DATA<7>	U44.V1:RP9.4::600			200			100 MHZ	14 24
	UIDE_DATA<6..0>	:::600			200			100 MHZ	14 24
	UIDE_ADDR<2..0>	:::650			200			100 MHZ	14 24
	UIDE_RST_L	:::400			200			100 MHZ	14 24
	UIDE_DIOW_L	:::400			200			100 MHZ	14 24
	UIDE_DIOR_L	:::600		10 MIL SPACING	200			100 MHZ	14 24
	UIDE_DMACK_L	:::400			200			100 MHZ	14 24
	UIDE_CS0_L	:::500			200			100 MHZ	14 24
	UIDE_CS1_L	:::500			200			100 MHZ	14 24
	UIDE_DMARQ	:::400			200			100 MHZ	14
	UIDE_IOCHRDY	:::600		10 MIL SPACING	200			100 MHZ	14 24
	UIDE_INTRQ	:::400			200			100 MHZ	14
	HD_DATA<15..0>	::8000:9500	5	TOTAL UIDE+HD SKEW <500MIL	200	MATCHED_DELAY=HD_DATA:::1000		100 MHZ	24
	HD_ADDR<2..0>	::8000:9500	5		200			100 MHZ	24
	HD_RESET_L	::5000:7000	5		200			100 MHZ	24
	HD_DIOW_L	::6000:8000	5		200			100 MHZ	24
	HD_DIOR_L	::8000:9500	5	10 MIL SPACING	200	MATCHED_DELAY=HD_DATA:::1000		100 MHZ	24
	HD_DMACK_L	::7500:9000	5		200			100 MHZ	24
	HD_CS0_L	::6000:9000	5		200			100 MHZ	24
	HD_CS1_L	::6000:9000	5		200			100 MHZ	24
	HD_DMARQ	::7500:9000	5		200			100 MHZ	14 24
	HD_IOCHRDY	::8000:9500	5	10 MIL SPACING	200	MATCHED_DELAY=HD_DATA:::1000		100 MHZ	24
	HD_INTRQ	::6000:8000	5					100 MHZ	14 24
EIDE INTREPID	EIDE_DATA<15..0>	:::855						33 MHZ	14 24
	EIDE_ADDR<2..0>	:::900						33 MHZ	14 24
	EIDE_CS0_L	:::850						33 MHZ	14 24
	EIDE_CS1_L	:::850						33 MHZ	14 24
	EIDE_RD_L	:::500						33 MHZ	14 24
	EIDE_WR_L	:::500						33 MHZ	14 24
	EIDE_IOCHRDY	:::500						33 MHZ	14 24
	EIDE_INT	:::500						33 MHZ	14 24
	EIDE_RST_L	:::500						33 MHZ	14 24
	EIDE_DMACK_L	:::500						33 MHZ	14 24
	EIDE_DMARQ	:::500						33 MHZ	14 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>	::4500:6500						33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>	::4500:6500						33 MHZ	24 39
	EIDE_OPTICAL_CS0_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_CS1_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_RD_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_WR_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_IOCHRDY	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_INT	::5500:7500						33 MHZ	24 39
	EIDE_OPTICAL_RST_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_DMAACK_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_DMA_RQ	::5000:7000						33 MHZ	24 39
ETHERNET MII	ENET_LINK_RXD<7..0>	::8000:9000	5						14 27
	ENET_RX_DV	::8000:9000							14 27
	ENET_RX_ER	::8000:9000							14 27
	ENET_PHY_TXD<7..0>	::8300:9300	5						14 27
	ENET_LINK_TXD<7..0>	:::600							14
	ENET_PHY_TX_ER	::8000:9200	5						14 27
	ENET_LINK_TX_ER	:::400							14
	ENET_PHY_TX_EN	::8000:9200	5						14 27
	ENET_LINK_TX_EN	:::400							14
	ENET_MDIO	::8000:9000							14 27
	ENET_MDC	::8000:9000							14 27
	ENET_COL	::7500:9000							14 27
	ENET_CRS	::7500:9000							14 27
FIREWIRE MII	FW_LINK_DATA<7..0>	::2700:3500	5						14 28
	FW_PHY_DATA<7..0>	::4700:5500	5						28
	FW_LINK_CNTL<1..0>	::9000:10000							14 28
	FW_PHY_CNTL<1..0>	:::300							28
	FW_LINK_LREQ	:::300							14
	FW_PHY_LREQ	::8500:9500							14 28
	FW_PINT	::8500:9500							14 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0	ENET_MDI0:U49.31:T1.11:100				27
	MDI_P<0>	ENET_MDI0	ENET_MDI0:U49.29:T1.12:100				27
	MDI_M<1>	ENET_MDI1	ENET_MDI1:U49.34:T1.8:100	SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1	ENET_MDI1:U49.33:T1.9:100	OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2	ENET_MDI2:U49.41:T1.5:100	AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2	ENET_MDI2:U49.39:T1.6:100				27
	MDI_M<3>	ENET_MDI3	ENET_MDI3:U49.43:T1.2:100				27
	MDI_P<3>	ENET_MDI3	ENET_MDI3:U49.42:T1.3:100				27
	RJ45_DN<0>	RJ45_DP0	RJ45_DP0:T1.14:J18.2:100		10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0	RJ45_DP0:T1.13:J18.1:100		10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1	RJ45_DP1:T1.17:J18.6:100		10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1	RJ45_DP1:T1.16:J18.3:100		10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2	RJ45_DP2:T1.20:J18.5:100		10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2	RJ45_DP2:T1.19:J18.4:100		10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3	RJ45_DP3:T1.23:J18.8:100		10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3	RJ45_DP3:T1.22:J18.7:100		10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0	FW_TPA0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0	FW_TPA0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0	FW_TPB0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0	FW_TPB0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0	FW_TPI0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0	FW_TPI0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0	FW_TPO0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0	FW_TPO0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1	FW_TPA1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1	FW_TPA1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1	FW_TPB1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1	FW_TPB1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1	FW_TPI1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1	FW_TPI1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1	FW_TPO1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1	FW_TPO1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	CLKLVDS_LP	CLKLVDS_L	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	LVDS_L0N	LVDS_L0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L0P	LVDS_L0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L1N	LVDS_L1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L1P	LVDS_L1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L2N	LVDS_L2	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L2P	LVDS_L2	LVDS:::110		10 MIL SPACING		20 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	CLKLVDS_UP	CLKLVDS_U	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	LVDS_U0N	LVDS_U0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U0P	LVDS_U0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U1N	LVDS_U1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U1P	LVDS_U1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U2N	LVDS_U2	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U2P	LVDS_U2	LVDS:::110		10 MIL SPACING		20 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:::50	500	10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:::50	500	10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS	TMDS:::50	500	10 MIL SPACING	4	20 21 22
	TMDS_CLKP	CLKTMDS	TMDS:::50	500	10 MIL SPACING	4	20 21 22
	TMDS_DN<0>	TMDS_D0	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DP<0>	TMDS_D0	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DN<1>	TMDS_D1	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DP<1>	TMDS_D1	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DN<2>	TMDS_D2	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DP<2>	TMDS_D2	TMDS:::50		10 MIL SPACING		20 21 22 39
USB	NEC_USB_DAM	NEC_USB_DA	NEC_USB_DA:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA	NEC_USB_DA:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE	USB_DE:::200		5 MIL SPACING		15
	USB_DEP	USB_DE	USB_DE:::200		5 MIL SPACING		15
	NEC_USB_DBM	NEC_USB_DB	NEC_USB_DB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB	NEC_USB_DB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF	USB_DF:::200		5 MIL SPACING		15
	USB_DFP	USB_DF	USB_DF:::200		5 MIL SPACING		15
	BT_USB_DM	BT_USB_D	BT_USB_D:::200		5 MIL SPACING		15 24 39
	BT_USB_DP	BT_USB_D	BT_USB_D:::200		5 MIL SPACING		15 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1	NEC_USB_RSD1:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1	NEC_USB_RSD1:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2	NEC_USB_RSD2:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2	NEC_USB_RSD2:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:::200		5 MIL SPACING		15 25 39
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:::200		5 MIL SPACING		15 25 39
	LEFT_USB_DM	LEFT_USB	LEFT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB	LEFT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB	RIGHT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB	RIGHT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1V2_CSSN	1V2_CSS	1V2_CSS:::100				31
	1V2_CSSP	1V2_CSS	1V2_CSS:::100				31
	1V2_CSIN	1V2_CSI	1V2_CSI:::100				31
	1V2_CSIP	1V2_CSI	1V2_CSI:::100				31
	3V_SNSM	3V_SNS	3V_SNS:::100				33
	3V_SNSP	3V_SNS	3V_SNS:::100				33
	5V_SNSM	5V_SNS	5V_SNS:::100				33
	5V_SNSP	5V_SNS	5V_SNS:::100				33
THERMOSTAT	THERM1_DM	THERM1	THERM1:::100				25
	THERM1_DP	THERM1	THERM1:::100				25
	THERM2_DM	THERM2	THERM2:::100				25
	THERM2_DP	THERM2	THERM2:::100				25
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:::100				25
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:::100				25
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:::100				25
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:::100				25
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:::100				25
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:::100				25
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:::100				25
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:::100				25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16 19 35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 23 39
FAN GND	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 25 39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND	
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4	
	CHGND4				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5	
	CHGND5				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6	
	CHGND6				
ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12		27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 9 16 17 23 34
L3 CACHE	L3_VREF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		8
	L3_CLK_REF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		8
	L3_OVDD	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6 8
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	10 11 16 17
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	15
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	9 13 15
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	15
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	13
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	13
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	9
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
			MIN_NECK_WIDTH REDUCED FOR TESTPOINTS		
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		10
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		13
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		10
	HIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		14
CARDBUS	VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
NVIDIA NV17MAP	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20 39
	+2_5V_GPU_FB	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	13 15 19 20 21
	+3V_GPU_DVO	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	13 16 17 19 20
	+3V_DAC1VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_DAC2VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_GPU_AVDD1	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_GPU_AVDD0	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_GPU_PLLVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_GPU_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+2_8V_IFP_PLLVDD	VOLTAGE=2.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	20
	GPU_AGP_VREF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		19
	GPU_FB_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		19
SILICON IMAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	15
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	15

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+12_8V_PBUS_JUMPER	VOLTAGE=12.8V	MIN_LINE_WIDTH=10		32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.65V SWITCHER	5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	5V_ILIM		MIN_LINE_WIDTH=8		35
	5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		15 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	5V_2_5V_OK		MIN_LINE_WIDTH=8		20 35
	1778_VFB		MIN_LINE_WIDTH=8		20
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	3V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	3V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	3V_VFB		MIN_LINE_WIDTH=8		35
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		35
	LTC3411_ITH		MIN_LINE_WIDTH=8		35
	LTC3411_SYNC		MIN_LINE_WIDTH=8		35
	LTC3411_SHDN		MIN_LINE_WIDTH=8		35
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	15
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	16
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	16

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 14 27
FUNC_TEST=YES JTAG_ASIC_TDI 14
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 14 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 14 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23
FUNC_TEST=YES JTAG_L3_TMS 8
FUNC_TEST=YES JTAG_L3_TDI_TP 8
FUNC_TEST=YES JTAG_L3_TDO_TP 8
FUNC_TEST=YES JTAG_L3_TCK 8
FUNC_TEST=YES INT_I2C_CLK0 12 14 23
FUNC_TEST=YES INT_I2C_DATA0 12 14 23
FUNC_TEST=YES INT_I2C_CLK1 14 15 25
FUNC_TEST=YES INT_I2C_DATA1 14 15 25
FUNC_TEST=YES CBUS_DET_1_L 18
FUNC_TEST=YES CBUS_DET_2_L 18
FUNC_TEST=TRUE TMDS_DN<0> 20 21 22 37
FUNC_TEST=TRUE TMDS_DP<0> 20 21 22 37
FUNC_TEST=TRUE TMDS_DN<1> 20 21 22 37
FUNC_TEST=TRUE TMDS_DP<1> 20 21 22 37
FUNC_TEST=TRUE TMDS_DN<2> 20 21 22 37
FUNC_TEST=TRUE TMDS_DP<2> 20 21 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 21 22
FUNC_TEST=YES VGA_HSYNC 21 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 20 22 37
FUNC_TEST=YES LVDS_L0P 20 22 37
FUNC_TEST=YES LVDS_L1N 20 22 37
FUNC_TEST=YES LVDS_L1P 20 22 37
FUNC_TEST=YES LVDS_L2N 20 22 37
FUNC_TEST=YES LVDS_L2P 20 22 37
FUNC_TEST=YES CLKLVDS_LN 20 22 37
FUNC_TEST=YES CLKLVDS_LP 20 22 37
FUNC_TEST=YES LVDS_U0N 20 22 37
FUNC_TEST=YES LVDS_U0P 20 22 37
FUNC_TEST=YES LVDS_U1N 20 22 37
FUNC_TEST=YES LVDS_U1P 20 22 37
FUNC_TEST=YES LVDS_U2N 20 22 37
FUNC_TEST=YES LVDS_U2P 20 22 37
FUNC_TEST=YES CLKLVDS_UN 20 22 37
FUNC_TEST=YES CLKLVDS_UP 20 22 37
FUNC_TEST=YES LVDS_DDC_CLK 20 22
FUNC_TEST=YES LVDS_DDC_DATA 20 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 15 25
FUNC_TEST=YES SND_SYNC 15 25
FUNC_TEST=YES SND_CLKOUT 15 25 36
FUNC_TEST=YES SND_HP_MUTE_L 15 25
FUNC_TEST=YES SND_AMP_MUTE_L 15 25
FUNC_TEST=YES INT_AUDIO_TO_SND 15 25
FUNC_TEST=YES SND_SCLK 15 25 36
FUNC_TEST=YES SND_HW_RESET_L 15 25
FUNC_TEST=YES SND_HP_SENSE_L 15 25
FUNC_TEST=YES SND_LIN_SENSE_L 15 25
FUNC_TEST=YES INT_I2C_DATA2 15 25
FUNC_TEST=YES INT_I2C_CLK2 15 25
FUNC_TEST=YES USB_D1M 15 26
FUNC_TEST=YES USB_D1P 15 26

NO FUNCTIONS DEFINED BY TEST GROUP

FUNC_TEST=YES USB_D2M 15 26
FUNC_TEST=YES USB_D2P 15 26
FUNC_TEST=YES BT_USB_DM 15 24 37
FUNC_TEST=YES BT_USB_DP 15 24 37
FUNC_TEST=YES MODEM_USB_DM 15 25 37
FUNC_TEST=YES MODEM_USB_DP 15 25 37
FUNC_TEST=TRUE PCI_AD<0> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<1> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<2> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<3> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<4> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<5> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<6> 10 13 18 24 26 37

FUNC_TEST=TRUE PCI_AD<7> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<8> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<9> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<10> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<11> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<12> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<13> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<14> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<15> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<16> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<17> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<18> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<19> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<20> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<21> 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<22> 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<23> 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<24> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<25> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<26> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<27> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<28> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<29> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<30> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<31> 10 13 18 24 26 37
FUNC_TEST=YES PCI_FRAME_L 13 18 24 26 37
FUNC_TEST=YES PCI_TRDY_L 13 18 24 26 37
FUNC_TEST=YES PCI_IRDY_L 13 18 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 13 18 24 26 37
FUNC_TEST=YES PCI_STOP_L 13 18 24 26 37

FUNC_TEST=YES PCI_PAR 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<0> 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<1> 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<2> 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<3> 13 18 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 13 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 13 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 15 24
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 36 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 36 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 36 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_ADDR<2> 24 37

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 15 25
FUNC_TEST=YES COMM_SHUTDOWN 15 25
FUNC_TEST=YES COMM_RING_DET_L 15 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=TRUE KBD_X<0> 23 30
FUNC_TEST=TRUE KBD_X<1> 23 30
FUNC_TEST=TRUE KBD_X<2> 23 30
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FUNC_TEST=TRUE KBD_X<4> 23 30
FUNC_TEST=TRUE KBD_X<5> 23 30
FUNC_TEST=TRUE KBD_X<6> 23 30
FUNC_TEST=TRUE KBD_X<7> 23 30
FUNC_TEST=TRUE KBD_X<8> 23 30

FUNC_TEST=TRUE KBD_X<9> 23 30
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FUNC_TEST=TRUE KBD_Y<5> 23 30
FUNC_TEST=TRUE KBD_Y<6> 23 30
FUNC_TEST=TRUE KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FAN1_GND 25 38
FUNC_TEST=YES FAN1_TACH 25
FUNC_TEST=YES FAN2_GND 25 38
FUNC_TEST=YES FAN2_TACH 25
FUNC_TEST=TRUE RJ45_DP<0> 27 37
FUNC_TEST=TRUE RJ45_DN<0> 27 37
FUNC_TEST=TRUE RJ45_DP<1> 27 37
FUNC_TEST=TRUE RJ45_DN<1> 27 37
FUNC_TEST=TRUE RJ45_DP<2> 27 37
FUNC_TEST=TRUE RJ45_DN<2> 27 37
FUNC_TEST=TRUE RJ45_DP<3> 27 37
FUNC_TEST=TRUE RJ45_DN<3> 27 37

FUNC_TEST=YES FW_TPO0R 29 38

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 15 25
FUNC_TEST=YES COMM_TRXC 15 25
FUNC_TEST=YES COMM_GPIO_L 15 25
FUNC_TEST=YES COMM_DTR_L 15 25
FUNC_TEST=YES COMM_RTS_L 15 25
FUNC_TEST=YES COMM_RXD 15 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=TRUE +PBUS 38
FUNC_TEST=TRUE +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 20 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=TRUE +1_8V_MAIN 38
FUNC_TEST=TRUE +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 20 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES LT1962_L3_ADJ 6
FUNC_TEST=YES MAIN_RESET_L 18 19 21 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 10 13 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 10 24
FUNC_TEST=YES ROM_CS_L 10 13 24
FUNC_TEST=YES CLK33M_AIRPORT 13 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 10 13 24

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A
SCALE: NONE	SHT 39 OF 44	

C8-40

REVISION HISTORY

RELEASED FOR PROTO 1 RELEASED FOR PROTO 1

REV 1.1 - 08/14/02

149/ UPDATED SOME NETS FOR CONCEPT 14.2 COMPLIANCE (PG 30,36)
150/ CORRECTED PMU PART NUMBER (PG 28)
151/ DELETED 4 0805 BULK CAPS AND ADDED 20 0402 BYPASS CAPS ON DDR SODIMM CONNECTOR (PG 12)
152/ REPINNED OUT J13 (HARD DRIVE) CONNECTOR FOR BETTER FLEX ROUTING (PG 24)
153/ ADDED A FEW MORE COMPONENTS TO ALS CIRCUIT BASED ON THAI'S RECOMMENDATIONS (PG 23)
154/ REMOVED PROTO1 CONNECTOR OPTIONS (PG 1, 22, 26, 27)
155/ ADDED USB 2.0 CONTROLLER (PG 26)
156/ CHANGED TO SPIDEY 39PIN ZIF CONNECTOR AND PINOUT (PG 23)
157/ ADDED INTREPID SSCG CHIP SUPPORT (PG 15)
158/ CONSOLIDATED BOMS
159/ UPDATED USB 2.0 SIGNAL CONSTRAINTS (PG 26)
160/ CHANGED CPU CORE VOLTAGE TO 1.45V FAST/1.40V SLOW (PG 33)
161/ ADDED +3V_SLEEP TO TUBA CONNECTOR (PG 25)
162/ MERGED MAXBUS_MAIN WITH MAXBUS_SLEEP BECAUSE INTREPID MAXBUS I/O CAN BE POWERED DOWN IN SLEEP (PG 16,17)
163/ DELETED ZT17 AND ZT2 BECAUSE THEY ARE NO LONGER NEEDED (PG 4)
164/ CHANGED FL1 TO NEW COMMON MODE CHOKES FOR FIREWIRE A (PG 28)
165/ CHANGED CRYSTAL VOLTAGE DIVIDER FOR FIREWIRE PHY TO 50/100 (BILL'S RECOMMENDATION) (PG 28)
166/ ADDED 2N7002 TO PREVENT PMU_SLEEP_LED_L FROM PUMPING UP +3V_MAIN DURING SHUTDOWN (PG 23)

REV 2.0 - 08/26/02

167/ DELETED USB POWER FET (PG 23)
168/ CHANGED 14PIN ZIF CONNECTORS AND PINOUT (PG 24,31)
169/ CONNECTED VGATE TO EXTINT10 BECAUSE NEED INTERRUPT CONTROL (PG 15)
170/ UPDATED A FEW CONSTRAINTS
171/ ADDED NEW QUAD-VCORE CONTROL CIRCUITRY (PG 33)
172/ CHANGED OPTICAL CONNECTOR PINOUT (PG 24)
173/ ADDED PMU_LID_CLOSED_L SIGNAL TO LMU (PG 23)
174/ ADDED Q11 ADAPTER DETECTION SCHEME (PG 29)
175/ ADDED DEDICATED RC FILTERING FOR PORT0 TX 0 (PG 28)
176/ ADDED STUFFING OPTION FOR DS1 PIN ON FIREWIRE PHY (PG 28)
177/ CHANGED STUFFING OPTION TO RAISE PLL VOLTAGE TO 1.95V FOR FW (PG 28)
178/ DELETED C741 (100UF INPUT CAP TO +3V_SLEEP) (PG 32)
179/ DELETED C757 (0.22UF BYPASS CAP FOR PCI1510) TO EASE TESTPOINT CONSTRAINTS (PG 18)
180/ SEPERATED PULL-UP FOR PCI_SERR_L AND PCI_PERR_L (PG 18,26)
181/ CHANGED SYSCLK_CPU, INT_PCI_FB_OUT, AND INT_AGP_FB_OUT SERIES RESISTOR VALUE (PG 9, 13)
182/ CHANGED C533, C539 TO 270PF AND CHANGED CONNECTIONS (PG 32)
183/ ADDED 4.7NF CAP ON Q51 GATE (PG 31)
184/ ADDED EMI SHIELD FOR INVERTER CHGND (PG 4)
185/ UPDATED MORE CONSTRAINTS
186/ CHANGED STUFFING OPTION TO FORCE 3V/5V INTO FORCE CONTINUOUS MODE TO REDUCE INDUCTOR SINGING (PG 32)
187/ CHANGED FW DVDD LDO TO 1.95V PER BILL'S RECOMMENDATION (PG 28)
189/ REMOVED C195 - 1.5V AGP(DOUBLED BYPASS), C24,C20 - 3VMAIN (DOUBLED BYPASS) FOR TESTPOINTS (PG 17)
190/ REMOVED C91 - 1.5V AGP BULK CAP BECAUSE THERE ARE 4 ON INTREPID SIDE ALREADY! (PG 20)
191/ CHANGED STUFFING OPTION TO FORCE 14V INTO FORCE CONTINUOUS MODE TO REDUCE INDUCTOR SINGING (PG 31)
192/ CHANGED STUFFING OPTION TO RAISE MARVELL CORE VOLTAGE TO 1.32V (PG 27)
193/ REMOVED COMMON MODE CHOKE FOR FIREWIRE B SIGNALS (PG 28)
194/ CHANGED LINE_WIDTH FOR FIREWIRE SIGNALS TO MAKE THEM 55OHM SINGLE AND 110OHM DIFFERENTIAL (PG 36)
195/ CHANGED STUFFING OPTION TO ENABLE 1.5V_LDO AND MAKE 1.5V_MAIN INTO 1.8V (PG 16, 19, 34)
196/ ADDED BACK IN COMMON MODE CHOKE FOR FIREWIRE B TO ENSURE TESTABILITY (PG 28)

RELEASED FOR PROTO 2 RELEASED FOR PROTO 2

LAST MINUTE BOM CHANGES FOR PROTO2 (9/5/02)

197/ STUFFED 20K FEEDBACK RESISTOR FOR MARVELL 88E1111 CRYSTAL (PG 27)
198/ NO STUFFED 4700PF FOR 14V PBUS GATE - C741 (PG 31)
199/ NO STUFFED L4 AND L5, FIREWIRE COMMON MODE CHOKES (PG 28)
200/ CHANGED BOOTROM APN FOR SHARP DIE-SHRINK PACAKGE (PG 10)
201/ CHANGED VCORE STUFFING OPTION FOR 1GHZ PROCESSOR (PG 33)

REV 3.0 - 09/20/02

202/ COMBINED FIREWIRE FUSE INTO ONE TO LIMIT PORT POWER TO 22W@24V OR 13.5W@15V (PG 28)
203/ UPDATED L3 SYMBOLS TO REFLECT MISSING SA17 SIGNAL ON 4MBIT PARTS VS. 8MBIT PARTS (PG 8)
204/ CHANGED TO NEW SPIDEY CONNECTOR AND PINOUT (PG 23)
205/ REMOVED P93 SUPPORT CIRCUIT (PG 25)
206/ ADDED 0 OHM RESISTOR FOR 2.5V_MARVELL TO MEASURE CURRENT (PG 27)
207/ ADDED 0 OHM RESISTOR FOR POWER BUTTON - DEBUG (PG 25)
208/ ADDED 2 JUMPERS FOR PMU_RESET_BUTTON_L AND PMU_NMI_BUTTON_L (PG 25)
209/ CHANGED TO PROTO2 BOM OPTION - INTREPID REV 2.0, AND MARVELL 2.0 CHANGES

RELEASED FOR PROTO 2-ENCLOSURE RELEASED FOR PROTO 2-ENCLOSURE

LAST MINUTE BOM CHANGES FOR PROTO2-ENCLOSURE (9/25/02)

210/ CHANGED R474 TO 49.9K, 1%, R475 TO 1.0K, 1%, AND R683 TO 10.7K, 1% (PG 30)
211/ CHANGED INTRPEID PART NUMBER TO REV 2.0 (PG 9-16)

REV 4.0 - 10/24/02

212/ ADDED 10K PULL-UP STUFFING OPTION TO CG_ADDRSEL AND 10K PULL-DOWN STUFFING OPTION TO CG_FSEL (PG 15)
213/ REMOVED ZEBRA 15/16 SUPPORT (PG 28)
214/ REMOVED NO_TEST=TRUE PROPERTY ON MAXBUS/L3 BUS (PG 35)
215/ ADDED FUNCTIONAL TEST POINT DEFINITION (PG 38)
216/ REPLACED IRF7822 IN THE BATTERY CHARGER AND 14V SWITCHER SECTION WITH IRF7811W (PG 30, 31)
217/ DELETED CAPACITOR OPTION ON INT_CPUFB_IN - MAKE RISE/FALL TIME WORSE (PG 9)
218/ CHANGED POWER SUPPLY TO FAN TO +3V_SLEEP (PG 25)
219/ UPDATED TO NEW EMI SHIELD PART NUMBER, AND NEW 300MHZ SRAM PART NUMBER (PG 4, 8)
220/ SWITCHED TO NEW 16PIN MODEM CONNECTOR (PG 25)
221/ FIXED AGP CLOCK CONSTRAINTS (PG 13,35)
222/ DELETED PULL-UP RESISTOR TO VCORE_VCC ON VGATE SINCE THERE'S A 10K PULL-UP RESISTOR ON INTREPID SIDE (PG 33)
223/ ADDED BACK INDIVIDUAL FUSE FOR FIREWIRE PORT (PG 28)
224/ SEPARATED FW PORTS TO ANOTHER PAGE; UPDATED PIN DEFINITIONS (PG 28, 29)
225/ ADDED 2 10K PULL-UP TO USB NC PINS (M6 AND P6) - PER NEC (PG 26)
226/ CHANGED SMBUS PULL-UP RESISTOR TO 7.15K (DON'T HAVE ANOTHER 5% ~7K RESISTOR IN BOM) - PER IBOOK (PG 30)
227/ DELETED ALL INTREPID_REV1 STUFFING OPTION (PG 9-16)
228/ CHANGED TO NEW MOUNTING HOLE SIZES - ALL INCREASED BY 0.2MM IN DIAMETER EXCEPT FOR THREE CPU MTG HOLES (PG 4)
229/ CHANGED BOM OPTION TO 167MHZ BUS WITH PLL SET TO 1GHZ/833MHZ (PG 7,9)
230/ CHANGED TO 10K PULL-DOWN FOR MOD_DTI, MOD_SYNC, AND MOD_BITCLK - PER INTREPID PADS SPREADSHEET (PG 14)
231/ CHANGED JUMPER PADS FOR PMU_RESET_L AND PMU_NMI_L TO 0603 RESISTOR PADS (PG 25)
232/ ADDED DAMPING RESISTOR FOR 8MHZ CRYSTAL (PG 23)
233/ CHANGED INT_PLL_EN_PD TO PULL-DOWN AND CHANGED JTAG_ENET_TDI TO PULL-UP (PG 14)
234/ DISCONNECTED FW_LKON FROM INT_EXTINT3_PU BECAUSE FW_LKON OUTPUT NOW WORKS FINE (PG 15)
235/ CHANGED R21 TO +3V_SLEEP TO PREVENT LEAKAGE TO MAXBUS_SLEEP BEFORE LMU SETS OUTPUT AS OPEN-DRAIN (PG 23)
236/ CHANGED FW_PD AND FW_PU TO 5% RESISTORS (PG 28)
237/ ADDED FIREWIRE PORT CURRENT LIMITER (PG 29)
238/ CHANGED +14V_PBUS TO +PBUS SINCE THE VOLTAGE MAY CHANGE BACK AND FORTH (PG ALL)
239/ ADDED A29 ADAPTER DETECT (PG 30)
240/ ADDED NEW SYSTEM CURRENT MONITOR FOR +PBUS (PG 31)
241/ DELETED OLD BATTERY CURRENT LIMITER CIRCUIT (PG 31)
242/ ADDED C843 TO SPEED UP Q10 TURN ON AND CHANGED Q14 TURN ON TO AC_IN (PG 31)
243/ REMOVED C650 (2MILLOHM) SENSE RESISTOR FROM CPU_VCORE SWITCHER BECAUSE IT CAUSES TOO MUCH DROOP ON VOLTAGE (PG 34)
244/ REPLACED LMC6462 WITH LMC7111 BECAUSE ONLY NEED 1 OP-AMP (PG 31)
245/ CHANGED LTC4210 TIMER CAPACITOR TO ONE 0805 INSTEAD OF TWO 0402 (PG 29)
246/ FINALIZED ALL POWER SUPPLY CHANGES (PG 29-32)
247/ CHANGED TO NEW CALIFORNIA MICRO DEVICES LOW-CAPACITANCE ESD DIODES FOR FIREWIRE (PG 29)
248/ ADDED 1K PULL-DOWN TO FW_DS1, FW_SE, AND FW_SM INPUTS PER TI'S RECOMMENDATION (PG 28)
249/ CHANGED DS1 (PIN 32) TO PULL-UP FOR A-ONLY OPERATION (PG 28)
250/ ADDED MORE FUNCTIONAL TEST POINTS PER WAYNE'S INPUT (PG 39)
251/ CHANGED BACK TO OLD BAV99DW DIODES BECAUSE CMD1210 CAN ONLY HANDLE 8MA FORWARD CURRENT (PG 29)
252/ REMOVED COMMON MODE CHOKE PADS FOR FIREWIRE B (PG 29)
253/ ADDED PULL-UP TO PMU_SLEEP_LED_L AND CHANGED R451 TO PULL-DOWN SLEEP_LED_H TO ENSURE STATES WHEN CHIPS TRISTATE OUTPUTS (PG 23)
254/ ADDED SILICON IMAGE SI1162 - FIRST PASS (PG 21)
255/ UPDATED DVI_HPD CIRCUIT PER HYDRA IMPLEMENTATION (PG 22)
256/ REPINNED OUT TUBA CONNECTOR (PG 25)
257/ SWAPPED JTAG_CPU_TRST_L AND JTAG_CPU_TDI WITH SENSORS_I2C*_PD BECAUSE 200OHM PULL-DOWN PREVENTS IN-CIRCUIT PROGRAMMING ON PA0
258/ REMOVED XW17 - CPU_VCORE_JUMPER - FOR HUGE COPPER POUR (PG 34)
259/ ADDED PART NUMBER TABLE FOR SPEAKER CLIP (PG 4)
260/ MIRRORED AIRPORT CONNECTOR BECAUSE CONNECTIONS ARE MIRRORED ON THE FLEX (PG 24)
261/ FINALIZED ALL CHANGES FOR SI1162 PART - RUNNING HIGH SWING MODE (PG 21)
262/ CHANGED TO SI3446DV FOR FAN FETS (PG 25)
263/ PULLED DS2 HIGH TO SHUT-OFF PORT 3 ON FIREWIRE PHY COMPLETELY (PG 28)
264/ ADDED ONE MORE 1000UF POSCAP ON CPU_VCORE_SLEEP TO REDUCE RIPPLE BY ANOTHER 10MV, AND CHANGED OFFSET TO +30MV (PG 34)
265/ FINE TUNED PCI SERIES RESISTOR R VALUES FOR EMI AND DIVDED CY28512 OUTPUT FROM 2.5V TO 1.5V (PG 13,15)
266/ CY28512 NOW RUNS ON 3V_MAIN AND 2.5V_MAIN... UPDATED THE STRAPS TOO (PG 15)
267/ ALS SENSOR IS NOW RUNNING DURING SLEEP PER THAI'S REQUEST (PG 23, 24)
268/ CHGND1 NOW SPLITS INTO CHGND1 AND CHGND6 BECAUSE OF FIREWIRE B ROUTING ON THE SURFACE (PG 29)
269/ SEPARATED 0 OHM RESISTORS FOR EACH FIREWIRE GROUND PINS (PG 29)
270/ CY28512 RESET PIN NOW GOES TO +3V_MAIN - INT_RESET_L WILL NOT WORK (PG 15)
271/ CHANGED PULL-UPS FOR FAN CONTROL SIGNALS TO +3V_SLEEP - LEAKAGE PROBLEM THROUGH THE FAN (PG 25)
272/ NO STUFFED PULL-UP RESISTORS FOR EIDE_RESET AND EIDE_DMAACK_L - PER MKE DRIVE SPEC (PG 24)

RELEASED FOR EVT RELEASED FOR EVT

LAST MINUTE BOM CHANGES FOR PROTO2 (10/29/02)

273/ UPDATED BOMOPTION "NO SSCG" TO "NO_SSCG" (PG 9)
274/ FIXED SYSTEM BUS TO 167MHZ OPERATION BECAUSE WE ARE USING INTREPID 2.0 (PG 15)

REV 5.0 - 12/03/02

275/ P50 IS ONLY POWERED BY +3V_SLEEP NOW (PG 24)
276/ CHANGED TO ONE 1.5A FIREWIRE FUSE (PG 29)
277/ ADDED PULL-DOWN TO P50'S CLKRUN_L SIGNAL AND NO CONNECTED P50'S PME SIGNAL (PG 24)
278/ CHANGED PCI PULL-UP RESISTORS TO +3V_SLEEP TO SUPPORT P50 D3COLD (PG 13)
279/ ADDED TWO 4.7UF BULK CAPS NEAR THE FAN CONNECTORS (PG 25)
280/ FAN POWER GOES BACK TO +5V_SLEEP (PG 25)
281/ NEW PART NUMBERS FOR INTREPID 2.1, ZEBRA-17, BS520, 50&80PIN CONNECTORS, NEW CPU DESC.
282/ NEW BOOTROM AND LMU PART NUMBERS (PG 11, 23)
283/ FIXED DRCS AROUND SIL1162 BY CHANGING CONSTRAINTS (PG 21)
284/ ADDED SLEEP FET FOR +5V_SOUND (PG 25)
285/ ADDED 5A FUSE FOR FIREWIRE PORT POWER - FOR SAFETY COMPLIANCE (PG 29)
286/ ADDED ESD AND LATE VG PROTECTION FOR FIREWIRE (PG 29)
287/ CHANGED NOMINAL CORE VOLTAGE TO 1.36V BECAUSE OF +/-50 MV REQUIREMENT ON GPU_VCORE (PG 20)
288/ CHANGED SIL1162 TO RISING CLOCK EDGE - STUFFING CHANGE (PG 21)
289/ ADDED DUAL SCHOTTKY FOR FIREWIRE PHY POWER (PG 28)
290/ ADDED STUFFING OPTION TO FEED MAIN_RESET_L TO PCI1510 (PG 18)
291/ LOADED IN NEW MECHANICAL SYMBOLS FOR WIRELESS CARDBUS, AND HARD/OPTICAL DRIVES
292/ STUFFED R880 BECAUSE THERE'S A WEAK INTERNAL PULL-UP ALREADY (PG 15)
293/ ADDED TWO 0805 ZERO OHM RESISTORS TO FEED IN EITHER +2.5V_SLEEP OR +2.5V_MAIN TO INTREPID (PG 16)
294/ CHANGED GPU_VCORE SWITCHER BOM OPTIONS TO REDUCE JITTER ON SUPPLY (PG 20)
295/ CONNECTED MAX4172 POWER TO +ADAPTER_SW TO SAVE 1MA WHEN RUNNING ON BATTERY ONLY (PG 31)
296/ CHANGED Q47 AND Q58 TO 7811W FOR BOM CONSOLIDATION - ALSO CHANGED R348 AND R353 TO 113K TO ADJUST CURRENT LIMIT (PG 35)
297/ UPDATED BOM OPTION FOR SSCG (PG 9, 15)
298/ CHANGED RESET CAP TO 0.22UF ON TI PHY PER TI'S RECOMMENDATION (PG 28)
299/ UPDATED TO NEW TUBA CONNECTOR PINOUT (PG 25)
300/ CHANGED BOOTROM RESET TO INT_RESET_L FOR ICT (PG 10)
301/ ADDED 4 ZERO OHM RESISTORS TO NO STUFF THE QUAD_VCORE OPTION (PG 34)
302/ CHANGED ALL 132S1061 (0805 PACKAGE) TO 132S0046 (0603 PACKAGE) - (PG ALL)
303/ CHANGED TO TOP CONTACT SPIDEY CONNECTOR (PG 23)
304/ ADDED BOM OPTION TO PCI_CLOCK_OUT FROM INTREPID TO USB CONTROLLER (PG 13)
305/ CHANGED TO NEW 30PIN TUBA CONNECTOR WITH SOLDER TAPS (PG 25)
306/ UPDATED ETHERNET SERIES R VALUES (PG 14, 27)
307/ CONSOLIDATED 1UF, 10% CAPS TO 1UF, 20% CAPS (PG 28,31)
308/ CHANGED CURRENT LIMIT SETTINGS FOR 1.5V AND 2.5V SWITCHER (PG 35)
309/ ADDED FOUR PULL-DOWN RESISTORS ON CKE FOR DDR MEMORY (PG 10)
310/ ADDED THREE 0402 CAP PADS ON SND_SCLK, SND_CLKOUT, AND LVDS_DDC_CLK FOR EMI (PG 22, 25)
311/ ADDED 5 SPEAKER CLIPS SYMBOLS (PG 4)
312/ CHANGED VCORE OFFSET TO 10MV -> EVT BOARD MEASURED: IDLE 1.407V, SMOKE 1.387V, TRANSIENT 1.37V (PG 34)
313/ ADDED RESISTOR TO TPS2211 SHUTDOWN# PIN TO SUPPORT PSUEDO-D3COLD (PG 18)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 401228 | REV. 0A

SCALE NONE | SHT 40 OF 44

8 7 6 5 4 3 2 1

D C B A

*** Signal Cross-Reference ***
--- for the entire design ---

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+1_0V_MARVELL   27D2 38B3
+1_5V_AGP       13C5 13D1 13D4 16D5 17C8 19A2 19A8
                19C6 19D5 20D8 38C3
+1_5V_INTREPID_PLL 9D6 13D4 13D8 15D6 38D3
+1_5V_INTREPID_PLL1 15C3 38D3
+1_5V_INTREPID_PLL2 15D3 38D3
+1_5V_INTREPID_PLL3 15D3 38D3
+1_5V_INTREPID_PLL4 15D3 38D3
+1_5V_INTREPID_PLL5 13D3 38D3
+1_5V_INTREPID_PLL6 13D6 38D3
+1_5V_INTREPID_PLL7 9D5 38D3
+1_5V_INTREPID_PLL8 15D3 38C3
+1_5V_LDO       16B1 19A3 35D8 38D6
+1_5V_MAIN      38D6
+1_5V_SLEEP     38D6
+1_5V_SLEEP_VIN 35D8 38D6
+1_8V_MAIN      38D6 39A2
+1_8V_SLEEP     38D6
+1_95V_FW_DVDD  28C4 28C7 28D5 38A3
+1_95V_FW_DVDD_PORT1 28D6 38A3
+1_95V_FW_DVDD_RX0 28C5 38A3
+1_95V_FW_DVDD_TX0 28C5 38A3
+1_95V_FW_PLL400VDD 28D5 38A3
+1_95V_FW_PLL500VDD 28D5 38A3
+1_95V_FW_PLLVDD 28D5 28D7 38A3
+2_5V_CG_MAIN   15C6 38A3
+2_5V_GPU_FB    19A4 19A5 19B4 19B5 19C2 19D2 19D5
                38C3
+2_5V_INTREPID  10A8 11D3 11D5 11D6 11D8 16D7 17B8
                38D3
+2_5V_MAIN      38D6
+2_5V_MARVELL   27B8 27C4 38B3
+2_5V_MARVELL_AVDD 27C4 38B3
+2_5V_SLEEP     16D7 38D6
+2_8V_IFP_PLLVDD 20A2 20A4 20A5 38C3
+3V_CG_PLL_MAIN 15C6 38A3
+3V_DAC1VDD     21D4 38C3
+3V_DAC2VDD     21D7 38C3
+3V_FW          28A3 28D7 29D5 38B3
+3V_FW_AVDD     28C6 38A3
+3V_FW_AVDD_PORT0 28C6 38B3
+3V_FW_AVDD_PORT1 28C6 38B3
+3V_FW_AVDD_PORT2 28D6 38B3
+3V_FW_ESD      29B3 29D2 38B3
+3V_FW_ESD_ILIM 29D4 38B3
+3V_FW_UF       28D7 38B3
+3V_GPU         13D1 15C5 19A4 20A8 20B2 20B4 20C4
                20D2 21B8 21C7 21C8 21D1 21D3 21D6
                21D7 38C3
+3V_GPU_AVDD0   20B4 38C3
+3V_GPU_AVDD1   20B2 38C3
+3V_GPU_DVD0    21B6 38C3
+3V_GPU_PLLVDD  21D6 38C3
+3V_GPU_SS      21A4 38C3
+3V_HALL_EFFECT 23C6 38B6 39C4
+3V_INTREPID_USB 15C3 38D3
+3V_LCD         22B4 38B6
+3V_LCD_SW      22A4 38B6
+3V_MAIN        38D6
+3V_MAIN_JUMPER 33D2 38D1
+3V_NEC_VDD     26D7 38A3
+3V_PMU         38D6 39A2
+3V_PMU_AVCC    30B1 30B6 30D5 38C6
+3V_PMU_ESR     32A2 38C6
+3V_SI_AVCC     21D2 38B3
+3V_SI_PLLVCC   21D2 38B3
+3V_SI_VCC      21D2 38B3
+3V_SLEEP       38D6
+4_6V_BU        32A3 33B5 38C6
+4_85V_ESR      32A4 38C6
+4_85V_RAW      30B4 32A4 38C6
+5V_DDC_SLEEP   22D3 22D5 38B6 39A2
+5V_DDC_SLEEP_UF 22D6 38B6
+5V_HD_SLEEP    24D1 33A7 38C6
+5V_INV_SW      22B1 38B6 39D1
+5V_INV_UF_SW   22B2 38B6
+5V_MAIN        38D6
+5V_MAIN_JUMPER 33D8 38D1
+5V_SLEEP       38D6
+5V_SOUND_SLEEP 25D6 38B6
+5V_TPAD_SLEEP  23C7 38B6 39C4
+12_8V_INV      22B1 38B6 39A2
+12_8V_PBUS_JUMPER 32C3 38D1
+24V_PBUS       38D6 39B2
+ADAPTER        31D8 32D7 38D6
+ADAPTER_ILIM   32B6 38C6
+ADAPTER_OR_BATT 32A5 38C6
+ADAPTER_SENSE  31D5 38C6
+ADAPTER_SW     31D6 38C6
+BATT           38D6
+BATT_14V_FUSE  31D1 38C6
+BATT_24V_FUSE  31B1 31D2 38C6
+BATT_POS       31A4 38C6 39C3
+BATT_RSNS      31B2 38C6
+BATT_VSNS      31A4 38C6
+FW_AMP_SENSE   29D6 38B3
+FW_FUSE        29D7 38B3
+FW_PWR_OR      28B8 28D8 29D5 38B3
+FW_PWR_PORTA   29C5 38B3
+FW_SW          29D5 38B3
+FW_VP0         29C2 38B3
+FW_VP1         29A3 38B3
+HD_LOGIC_SLEEP 24C2 38C6
+PBUS           38D6 39B2
+VCC_CBUS_SW    18B1 18B2 18D2 38C3
+VPP_CBUS_SW    18B1 18B2 18D2 38C3
1V20_REF        31C7 32C8 38D1
1V65_REF        31A5
1_5V_2_5V_OK    20C8 35C5 38B1
1_5V_BOOST      35C6 38C1
1_5V_BST        35C5 38C1
1_5V_DH         35C5 38C1
1_5V_DL         35B5 38C1
1_5V_FB         35B5 35B7 38C1
1_5V_ILIM       35C5 38C1
1_5V_LX         35B5 38C1
1_5V_LX_F       35B7 35C5 38C1
1_8V_SLEEP_PWREN_L 35A3
1_8V_SW         35A5 38A1
1_8V_SW_F       35A4 38A1
1_8V_VFB        35A5 38A1
2_5V_BOOST      35C4 38D1
2_5V_BST        35C4 38D1
2_5V_DH         35C4 38D1
2_5V_DL         35B4 38C1
2_5V_FB         35B4 38C1
2_5V_ILIM       35C5 38D1
2_5V_LX         35B4 38D1
2_5V_LX_F       35B2 35C4 38D1
2_5V_SLEEP_PWREN_L 35C2
2_8V_ADJ1       20A7
2_8V_BYP        20A8
2_34V_REF       30A4
3V_5V_OK        33B4 35D6
3V_BG           33C4
3V_BOOST        33C4
3V_BOOST_ESR    33D3
3V_ITH          33C4
3V_ITH_RC       33C3
3V_PMU_VTAP     32B3
3V_RSNS         33D2 38D1
3V_RUNSS        33C4
3V_SLEEP_PWREN_L 33A3
3V_SNSM         33C4 37A2
3V_SNSP         33C4 37A2
3V_SW           33C4 38D1
3V_TG           33D4
3V_VOSNS        33C4
5V_BG           33C5
5V_BOOST        33C5
5V_BOOST_ESR    33D6
5V_HD_PWREN     33A8
5V_ITH          33C5
5V_ITH_RC       33C6
5V_RSNS         33D7 38D1
5V_RUNSS        33C5
5V_SLEEP_PWREN  33A8
5V_SND_PWREN    25D8
5V_SNSM         33C5 37A2
5V_SNSP         33C5 37A2
5V_SW           33C5 38D1
5V_TG           33C5
5V_VOSNS        33C5
1625_BG         32C5
1625_BST_ESR    32C5
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1625_COMP       31D2 32C6
1625_DIV        32C8
1625_ENABLE     32D7
1625_ENABLE_L   32D6
1625_EXTVCC     32D5 38D1
1625_FCB        32C6
1625_INTVCC     32C5 38D1
1625_RUNSS      32C6
1625_SGND       32B7 38D1
1625_TG         32C5
1625_VFB        32B5
1625_VIN        32C6 38D1
1625_VSW        32C4 38D1
1772_ACIN       31B5
1772_ACOK_L     31B5 31C4
1772_BST        31B4
1772_BST_ESR    31C3
1772_CCI        31B5
1772_CCS        31B5
1772_CCV        31B5
1772_CCV_RC     31B5
1772_CELLS      31B4
1772_CLS        31A4
1772_CSIN       31B4 37A2
1772_CSIP       31B4 37A2
1772_CSSN       31C5 37A2
1772_CSSP       31C5 37A2
1772_DCIN       31B5 38C6
1772_DHI        31B4
1772_DLO        31B4
1772_DLOV       31B4 38C6
1772_GND        31A5 38C6
1772_ICHG       31B5
1772_ICTL       31B5
1772_IINP       31B5
1772_LDO        31C4 38C6
1772_LX         31B4 38C6
1772_REF        31B5
1772_VCTL       31B5
1778_BG         20B7 38B1
1778_BST        20C8 38B1
1778_BST_RC     20C6 38B1
1778_FCB        20B7 38B1
1778_GND        20B6 20B8 38B1
1778_ION        20B7 38B1
1778_ITH        20C7 38B1
1778_ITH_RC     20B8 38B1
1778_SHDN_L     20B7
1778_SHDN_L_D3COLD 20D7
1778_TG         20C7 38B1
1778_VCC        20C7 38B1
1778_VFB        20B7 38B1
1778_VIN        20C7 38B1
1778_VRNG       20B7 38B1
3405_MODE       27D5
3405_VFB        27D4
3707_FCB        33C5
3707_FSET       33C5
3707_INTVCC     33D4 38D1
3707_SGND       33B5 38D1
3707_STBY       33C5
A29_CLS_ADJ     31A5
A29_CURRENT_ADJ 31C4
A29_DETECT      30A2 31A5 31C4
A29_DET_L       30A3
AC_DIV          31C8
AC_ENABLE_GATE  31D6
AC_ENABLE_L     31C6
AC_GTR_18V      31C4
AC_IN           27B8 29C8 30B3 31C5 31C7
AC_IN_FW_CNTL   29C8
AC_IN_L         31C2 31C6
AC_IN_L_RC      31C2
ADAPTER_DET     30A4 31D8 39C2
ADAPTER_I_REG   31D3
AGP_AD<31..0>   13B2 13C2 13D2 19C7 19D7 37D5
AGP_AD_STB<1..0> 13A2 13B2 19A7 19B7 37D5
AGP_AD_STB_L<1..0> 13A2 13B2 19A7 37D5
AGP_BUSY_L      13C4 13D2 19A7
AGP_CAL_PD      19A7
AGP_CAL_PU      19A7
AGP_CBE<3..0>   13B2 19B7 19C7 37D5
AGP_DEVSEL_L    13B2 13C2 19B7 37D5
AGP_FRAME_L     13B2 13C2 19B7 37D5
AGP_GNT_L       13C2 13D2 19B7 37D5
AGP_GPU_RESET_L 19B7
AGP_IRDY_L      13B2 13C2 19B7 37D5
AGP_NV_INT_L    15B5 19B7
AGP_NV_PIPE_L   19B7
AGP_NV_WBF_L    19B7
AGP_PAR         13B2 19B7 37D5
AGP_PIPE_L      13A2 13B2 19B8
AGP_RBF_L       13A2 13C2 19B7 37D5
AGP_REQ_L       13C2 13D2 19B7 37D5
AGP_SBA<7..0>   13B2 19A7 37D5
AGP_SB_STB      13B2 19A7 37D5
AGP_SB_STB_L    13A2 19A7 37D5
AGP_ST<2..0>    13C2 19B7
AGP_STOP_L      13B2 13C2 19B7 37D5
AGP_TRDY_L      13B2 13C2 19B7 37D5
AGP_WBF_L       13A4 13B2 19B8
AIRPORT_CLKRUN_L 24C6 39C1
AIRPORT_IDSEL   24C5 39B1
AIRPORT_PCI_GNT_L 13D7 24D5 39C4
AIRPORT_PCI_INT_L 15B5 15D7 24D5 39C4
AIRPORT_PCI_REQ_L 13A7 13D7 24D6 39D4
AIRPORT_PME_L_TP 24D5
BATTV_HIGH      31B7
BATTV_LOW       31B8
BATT_14PBUS_EN  31C1
BATT_14V_GATE   31C1
BATT_24PBUS_EN  31C2
BATT_24V_GATE   31C2
BATT_CLK        31A4 39C3
BATT_DATA       31A4 39C3
BATT_DIV        31A5
BATT_LOW        31A5 38C6
BATT_LOW_L      31B6
BATT_NEG        31A4 38C6 39C3
BBANG_HRESET_L  23A4 23C4 39C1
BBANG_JTAG_TCK  23B3 23C4
BBANG_TCK_EN    23B3
BCKFD_PROT_EN_L 31C6
BCKFD_PROT_GATE 31D6
BRIGHT_PWM      22A1 39A7
BRIGHT_PWM_UF   22A2
BT_USB_DM       15C1 24B2 37B2 39B6
BT_USB_DP       15C1 24B2 37B2 39B6
CAPSLOCK_LED    23A8
CAPSLOCK_LED_L  23B8 30C7
CBUS_ADDR<25..0> 18A4 18B1 18B2 18B4 18C1
CBUS_ADDR_16_UF 18B5
CBUS_BVD1_L     18B2 18C4
CBUS_BVD2_L     18B2 18C4
CBUS_CE1_L      18C1 18C4
CBUS_CE2_L      18B4 18C2
CBUS_DATA<15..0> 18A3 18A2 18A4 18C1 18C2
CBUS_DET_1_L    18C2 18C4 39B8
CBUS_DET_2_L    18C2 18C4 39B8
CBUS_INPACK_L   18B2 18B4
CBUS_INT_L      15B5 15B7 18A7
CBUS_IORD_L     18B2 18C4
CBUS_IOWR_L     18B2 18C4
CBUS_MFUNC1_PD  18A7
CBUS_MFUNC2_PD  18A7
CBUS_MFUNC3_PD  18A7
CBUS_MFUNC4_PD  18A7
CBUS_MFUNC5_PD  18A7
CBUS_MFUNC6_PD  18A7
CBUS_OE_L       18C1 18C4
CBUS_PCI_GNT_L  13D7 18A7
CBUS_PCI_IDSEL  18B7
CBUS_PCI_PERR_L 18B7 18D7
CBUS_PCI_REQ_L  13A7 13D7 18A7
CBUS_PCI_RESET_L 18A7
CBUS_READY      18B1 18C4
CBUS_REG_L      18B2 18C4
CBUS_RESET_L    18B2 18C4
CBUS_SUSPEND_PU 18A7 18D7
CBUS_VCCD0_L    18C4
CBUS_VCCD1_L    18C4
CBUS_VPPD0      18C4
CBUS_VPPD1      18C5
CBUS_VS1        18B2 18C4
CBUS_VS2        18B2 18C4
CBUS_WAIT_L     18B2 18B4
CBUS_WE_L       18B1 18C4
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CBUS_WP_L       18A1 18B4
CG_ADDRSEL      15B7
CG_CLKOUT       15B6
CG_FSEL         15B7 15C5
CG_LOCK         15B7
CG_RESET_L      15B7
CHARGE_DISABLE  31A7
CHARGE_LED_L    30C6 30D7 31D8 39D2
CHGND1          38A6
CHGND2          38A6
CHGND3          38A6
CHGND4          38A6
CHGND5          38A6
CHGND6          38A6
CLK10M_PMU_XIN  30B6
CLK10M_PMU_XOUT 30B6
CLK10M_PMU_XOUT_UF 30B7
CLK18M_INT_EXT  15A6 36B1
CLK18M_INT_XIN  15A5 36B1
CLK18M_INT_XOUT 15A5 36B1
CLK18M_XTAL_IN  15A6 36B1
CLK25M_ENET_XIN 27A7 36B1
CLK25M_ENET_XOUT 27A7 36B1
CLK25M_XTAL_IN  27A7
CLK27M_GPU_XIN  21B4 36B1
CLK27M_GPU_XOUT 21B4 36B1
CLK27M_XTAL_IN  21B4 36B1
CLK32K_PMU_XIN  30B3
CLK32K_PMU_XOUT 30B3
CLK32K_PMU_XOUT_UF 30B2
CLK33M_AIRPORT  13D8 24D5 36C1 39B1
CLK33M_AIRPORT_UF 13C7 36C1
CLK33M_CBUS     13D8 18A7 36C1
CLK33M_CBUS_UF  13C7 36C1
CLK33M_USB2     13C8 26B7 36C1
CLK33M_USB2_UF  13C7 36C1
CLK66M_AGP_15V_TP 13C4
CLK66M_GPU_AGP  13C8 19B7 36C1
CLK66M_GPU_AGP_UF 13C7 36C1
CLKENET_LINK_GBE_REF 14C5 27C8 36B1
CLKENET_LINK_GTX 14C5 36A1
CLKENET_LINK_RX 14D5 27C8 36B1
CLKENET_LINK_TX 14D5 27D8 36A1
CLKENET_PHY_GBE_REF 27C7 36B1
CLKENET_PHY_GTX 14C6 27C7 36A1
CLKENET_PHY_RX  27C7 36B1
CLKENET_PHY_TX  27D7 36B1
CLKFW_LINK_LCLK 14C3 36A1
CLKFW_LINK_PCLK 14C3 28C3 36A1
CLKFW_PHY_LCLK  14C2 28B7 36A1
CLKFW_PHY_PCLK  28B5 28C4 36A1
CLKLVDS_LN      20C2 22A4 37C2 39B7
CLKLVDS_LP      20C2 22A4 37C2 39B7
CLKLVDS_UN      20B2 22A4 37C2 39B7
CLKLVDS_UP      20B2 22A4 37C2 39A7
COMM_DTR_L      15C2 25D2 39B2
COMM_GPIO_L     15C2 25D3 39C2
COMM_RESET_L    15C5 25C4 39C4
COMM_RING_DET_L 15B5 15C7 25C5 30C6 39C4
COMM_RTS_L      15C2 25D2 39B2
COMM_RXD        15C2 25D2 39B2
COMM_SHUTDOWN   15C5 25C4 39C4
COMM_TRXC       15C2 25D3 39C2
COMM_TXD_L      15C2 25D3 39C2
COMP_DISABLE    22C2
COMP_ENABLE     22C1
COMP_RC         32C6
CPU_AACK_L      5A7 9B6 9C2 36D5
CPU_ADDR<31..0> 5B7 5C7 9B6 9C6 9D6 36D5
CPU_ARTRY_L     5A7 9B6 9D2 36D5
CPU_AVDD        5D4 38D3
CPU_BG_L        5C7 9C2 9D6 36D5
CPU_BR_L        5C7 9D2 9D6 36D5
CPU_BUS_VSEL    5C3 7B7
CPU_CHKSTP_OUT_L 5B3 5C2 39D8
CPU_CHKS_L      5B3 5D2
CPU_CI_L        5A7 9B6 36D5
CPU_CLKOUT_SPN  5C3
CPU_CLK_EN      9A6 30C4
CPU_DATA<63..0> 6A8 6B8 6C8 6D8 9A8 9B3 9B4 9B8 9C4
                9C8 9D4 9D8 36D5
CPU_DBG_L       5C3 9A4 9C2 36D5
CPU_DRDY_L      5C2 9A4 9C2 36D5
CPU_DRDY_L_UF   5C4 36D5
CPU_DTI<2..0>   5C3 9A4 36D5
CPU_EDTI        5B2 5C3
CPU_EMODE0_L    5A3 7B5
CPU_EMODE1_L    5A3 5C2
CPU_GBL_L       5A7 9B6 36D5
CPU_HIT_L       5A7 9B6 9D2 36D5
CPU_HRESET_INV  7A5 7A7 7B5
CPU_HRESET_L    5B3 5C2 7A5 7A8 7B4 23A2 39C8
CPU_L1TSTCLK    5B2 5B3
CPU_L2TSTCLK    5B3 5C2
CPU_L3_VSEL     6C3 7A7
CPU_LSSD_MODE   5B3 5C2
CPU_MCP_L       5B3 5D2
CPU_PLL_CFG<3..0> 5C3 7D3
CPU_PLL_CFGEXT  5C3 7D3
CPU_PLL_FS00    7C3
CPU_PLL_FS01    7C3
CPU_PLL_FS10    7C3
CPU_PLL_STOP_BASE 7C7
CPU_PLL_STOP_OC 7C8 30B6
CPU_PMONIN_L    5B3 5C2
CPU_PULLDOWN    5A2 5A3 5C7
CPU_PULLUP      5A3 5C2
CPU_QACK_L      5B3 9B6 36D5
CPU_QREQ_L      5B3 9B6 9C2 36D5
CPU_RSRV_D      5A7 5D2
CPU_SHD0_L      5A7 5D2
CPU_SHD1_L      5A7 5D2
CPU_SMI_L       5B3 5C2 30C4
CPU_SRESET_L    5B2 5B3 39C8
CPU_SRWX_L      5A3 5C2
CPU_TA_L        5B3 9A4 9D2 36D5
CPU_TBEN        5B3 5D2 9A6
CPU_TBST_L      5A7 9B6 36D5
CPU_TEA_L       5B3 9A4 9C2 36D5
CPU_TSIZ<2..0>  5A7 9B6 36D5
CPU_TS_L        5C7 9D2 9D6 36D5
CPU_TT<4..0>    5A7 9B6 36C5
CPU_VCORE_HI_OC 7B8 30D4 34C8 34D7
CPU_VCORE_PWR_SEQ 34D8
CPU_VCORE_SEQ   34D8
CPU_VCORE_SEQ_L 34D8
CPU_VCORE_SLEEP 5D3 5D8 34C1 34D2 38D3 39B2
CPU_VCORE_SNUB  34B3
CPU_VCORE_SW    34C1
CPU_WT_L        5A7 9B6 36C5
CSLOT_ADDR3_SPN 14B7
CSLOT_ADDR4_SPN 14B7
CSLOT_ADDR5_SPN 14B7
CSLOT_ADDR6_SPN 14B7
CSLOT_ADDR7_SPN 14B7
CSLOT_ADDR8_SPN 14B7
CSLOT_ADDR9_SPN 14B7
CSLOT_CE1_L_SPN 14C7
CSLOT_CE2_L_SPN 14C7
CSLOT_IORD_L_SPN 14C7
CSLOT_IOWAIT_L_PU 14C7
CSLOT_IOWR_L_SPN 14C7
CSLOT_OE_L_SPN  14C7
CSLOT_WE_L_SPN  14C7
CURRENT_THRESHOLD 31C4
CY25811_S0      21A4
CY25811_S1      21A4
DCDC_EN         20D6 29C8 32B7 33B5 34C8 39C1
DCDC_EN_L       20C8 33B6 35C7
DOC_CLK_ISO     22D4
DDR_VREF        12D1 12D3 12D5 12D6 12D8 38D3
DVI_DDC_CLK     22D4
DVI_DDC_CLK_UF  22C5 22D3 39C7
DVI_DDC_DATA    22C4
DVI_DDC_DATA_UF 22C5 39C7
DVI_HPD         22C4
DVI_HPD_DIV     22C3
DVI_HPD_UF      22C3 22C5 39C7
DVI_TRUN_ON_ILIM 22D2
DVI_TURN_ON     22D3
DVI_TURN_ON_BASE 22D2
EEPROM_ADDR     23D4
EEPROM_WP_PD    23D3
EIDE_ADDR<2..0> 14B7 24B8 37B5
EIDE_CS0_L      14B7 24B8 37B5
EIDE_CS1_L      14B7 24A8 37B5
EIDE_DATA<15..0> 14B7 14C7 24B8 24C8 24D8 37B5
EIDE_DMACK_L    14A7 24A8 37B5
EIDE_DMARQ      14A7 24A8 37B5
EIDE_INT        14A7 24A8 37B5
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EIDE_IORDY      14B7 24A8 37B5
EIDE_OPTICAL_ADDR<2..0> 24A5 24A6 24B7 37B5 39A4
EIDE_OPTICAL_CS0_L 24A5 24B7 37B5 39D4
EIDE_OPTICAL_CS1_L 24A6 24A7 37B5 39D4
EIDE_OPTICAL_DATA<15..0> 24A5 24A6 24B7 24C7 24D7
                37B5 39B4 39C4
EIDE_OPTICAL_DMACK_L 24A6 24A7 37A5 39A4
EIDE_OPTICAL_DMA_RQ 24A6 24A7 37A5 39A4
EIDE_OPTICAL_INT 24A5 24A7 37A5 39D4
EIDE_OPTICAL_IOCHRDY 24A5 24A7 37A5 39D4
EIDE_OPTICAL_RD_L 24A6 24A7 37B5 39A4
EIDE_OPTICAL_RST_L 24A7 24B5 37A5 39D4
EIDE_OPTICAL_WR_L 24A5 24A7 37A5 39D4
EIDE_RD_L       14A7 24A8 37B5
EIDE_RST_L      14B7 24A8 37B5
EIDE_WR_L       14A7 24B8 37B5
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ENET_COMA       27B7
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INT_GPIO1_PU    15C5 15C7 34C8
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INT_GPIO12_PU   15B5 15B7
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INT_I2C_CLK1    14C2 14C3 15B7 25B4 39B8
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INT_I2C_DATA0   12A3 12A8 14C2 14C3 23D2 23D4 39B8
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INT_PU_RESET_L  14D3 30A2 30C4
INT_REF_CLK_IN  15A5 15B5 36C1
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JTAG_ASIC_TDI   14C5 14D2 39D8
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JTAG_CPU_TDI    5B2 5C3 23D4 39C8
JTAG_CPU_TDO_TP 5C3 39C8
JTAG_CPU_TMS    5B2 5C3 23C4 39C8
JTAG_CPU_TRST_L 5A3 5B3 23D4 39C8
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KBD_LED_SET     23A5
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KBD_PWR         23A5
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L3_CLK<1..0>    6C3 8D1 8D4 36C1
L3_CLK_REF      8B7 8D1 8D4 38D3
L3_CNTL<1..0>   6C3 8C3 8C6 36C5
L3_DATA<63..0>  6A6 6B6 6C6 8C1 8C4 8D1 8D4 36C5
L3_DQP<A<1..0>  8C1 8C4 8D7
L3_DQPB<1..0>   8C1 8C4 8D7
L3_DQPC<1..0>   8C1 8C4 8D7
L3_DQPD<1..0>   8C1 8C4 8D7
L3_ECHO_CLK<3..0> 6B3 8C3 8C6 36C1
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L3_PULLDOWN<1..0> 8C3 8C6 8C7
L3_VREF         8B7 8C3 8C6 38D3
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LVDS_L0P        20C2 22B4 37C2 39C7
LVDS_L1N        20C2 22B4 37C2 39C7
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LVDS_U0N        20C2 22A4 37C2 39B7
LVDS_U0P        20C2 22A4 37C2 39B7
LVDS_U1N        20C2 22A4 37C2 39C7
LVDS_U1P        20B2 22A4 37C2 39B7
LVDS_U2N        20B2 22A4 37B2 39B7
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MEM_CKE<3..0>   10B6 10C5 36A5
MEM_CS_L<3..0>  10C5 10C6 36A5
MEM_DATA<63..0> 10B8 10C8 10D8 11B1 11B3 11B5 11B7
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MEM_DQM<7..0>   10C6 11B1 11B3 11B5 11B7 11C1 11C3
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NEC_USB_DAP     26A4 26C4 37B2
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NEC_USB_RSDP1   26C5 37B2
NEC_USB_RSDP2   26C5 37B2
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PMU_AC_DET      30A4 30B4
PMU_AC_IN       30A4 30B4
PMU_BATT0_DET_L 30B4
PMU_BATT1_DET_L_PU 30B4 30D2
PMU_BATT_DET_L  30B3 30D2 31A4 39C3
PMU_BYTE        30B6 30C7
PMU_CAPSLOCK_LED_L 30C6
PMU_CHARGE_V    30C4 31B8
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PMU_CPU_HRESET_L 23A4 23C4 30C4
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PMU_I2C_DATA    30B4 30C2
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PMU_NMI_L       30C2 30C4
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PMU_PME_L       15B5 26B8 30B2 30C4
PMU_POWERUP_OK  30B4 30D2
PMU_POWER_UP_L  29C8 30C6 30D7 33B6
PMU_REQ_L       15B7 15C2 30C4
PMU_RESET_BUTTON_L 25C2 30C4 30D2
PMU_RESET_L     30B6
PMU_RESET_L_SW  30B7 34A4
PMU_SLEEP_LED   23C4
```

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PMU_SLEEP_LED_L 23C2 30C4
PMU_SMB_CLK     30B4 30C2 31A3
PMU_SMB_DATA    30B4 30C2 31A2
PMU_TO_INT      15C2 30C4
POWER_UP        29C8
POWER_VALID     30B2 30C4
PWR_BUTTON_L    23A7 25D2 39B2
RAM_ADDR<12..0> 10A4 10B4 12B3 12B5 12B6 12B8 36A5
RAM_BA<1..0>    10A4 12B3 12B5 12B6 12B8 36A5
RAM_CAS_L       10A4 12B5 12B6 36A5
RAM_CKE<3..0>   10A3 10C4 12B6 12B8 12C3 12C5 36A5
RAM_CS_L<3..0>  10C4 12B3 12B5 12B6 12B8 36A5
RAM_DATA_A<63..0> 11B2 11B4 11B6 11B8 11C1 11C2
                11C3 11C4 11C5 11C6 11C7 11C8 11D1
                11D3 12A6 12A8 12B6 12B8 12C6 12C8
                12D6 12D8 36A5 36B5 36C5
RAM_DATA_B<63..0> 11C2 11C4 11C6 11C8 11D2 11D4
                12A3 12A5 12B3 12B5 12C3 12C5 12D3
                12D5 36A5 36B5 36C5
RAM_DQM_A<7..0> 11B2 11B4 11B6 11B8 11C1 11C3 11C5
                11C7 12A6 12B6 12C6 12D6 36A5 36B5
                36C5
RAM_DQM_B<7..0> 11C2 11C4 11C6 11C8 12A5 12B5 12C5
                12D5 36A5 36B5 36C5
RAM_DQS_A<7..0> 11B2 11B4 11B6 11B8 11C1 11C3 11C5
                11C7 12A8 12B8 12C8 12D8 36A5 36B5
                36C5
RAM_DQS_B<7..0> 11C2 11C4 11C6 11C8 12A3 12B3 12C3
                12D3 36A5 36B5 36C5
RAM_MUXSEL_H    11A3 11A5 11B1 11B3 36A5
RAM_MUXSEL_L    11A3 11A5 11B5 11B7 36A5
RAM_RAS_L       10A4 12B5 12B6 36A5
RAM_WE_L        10A4 12B3 12B8 36A5
RF_DISABLE_L_SPN 24D6 39C1
RIGHT_USB_DM    26A3 32A7 37A2 39D1
RIGHT_USB_DP    26A3 32A7 37A2 39D1
RJ45_C0_PD      27B2
RJ45_C1_PD      27B2
RJ45_C2_PD      27B2
RJ45_C3_PD      27B2
RJ45_DN<3..0>   27B2 37D2 39A3 39B3
RJ45_DP<3..0>   27B2 37D2 39A3 39B3
ROM_CS_L        10B3 13A5 24B6 39B1
ROM_OE_L        10B3 13A5 24C5 39B1
ROM_ONBOARD_CS_L 10B3 24C6 39B1
ROM_RW_L        10B3 13A5 24C6 39B1
ROM_WP_L        10B3
SI_DK<1..0>     21C3
SI_EDGE         21C3
SI_EXT_SWING_SET 21C1
SI_I2C_OFF      21C3
SI_TMDS_CLKN    21A2 21B3 21C1
SI_TMDS_CLKP    21A2 21B3 21C1
SI_TMDS_DN<2..0> 21A2 21B3 21C1
SI_TMDS_DP<2..0> 21A2 21B3 21C1
SLEEP           23C4 30B6 30D7 33A5 33A6 33B3 35B3
                35D2
SLEEP_LED       23C1 25C7
SLEEP_LED_I     23D1
SLEEP_LED_L     23D1
SLEEP_LED_SW_L  23C2
SLEEP_LED_UF    23C1
SLEEP_LSS       25B8 33A3 33A8
SLEEP_LSS_EN_L  33A4
SLEEP_L_LSS     20D6 27A8 33A4 34C8 35D7
SLEEP_L_LSS_EN_L 33A5
SND_AGND        25C7 38B6
SND_AMP_MUTE_L  15C5 25C6 39C6
SND_CLKOUT      15A1 25C6 36B1 39D6
SND_HP_MUTE_L   15C5 25C6 39C6
SND_HP_SENSE_L  15B5 25C6 39C6
SND_LIN_SENSE   15A7 15B5 25C7 39C6
SND_LIN_SENSE_L 15B5 25C7 39C6
SND_SCLK        15B1 25C6 36B1 39C6
SND_SYNC        15B1 25C6 39D6
SND_TO_AUDIO    15B1 25C6 39D6
SOFT_PWR_ON_L   22D1 23A8 30A8 30C6 30D7 34A4
ST7_ICP_SEL_PD  23A2 23D6
ST7_KBD_LED_OUT 23A4 23C4
ST7_OSC1        23D5
ST7_OSC2        23D5
ST7_PB6_PD      23B2 23C4
ST7_RESET_L     23D5
ST7_SENSOR4_SCK_PD 23B2 23D4
ST7_SENSOR4_SDA_PD 23B2 23D4
ST7_SENSOR5_SCK_PU 23B2 23D4
ST7_SENSOR5_SDA_PU 23B2 23D4
ST7_SLEEP_LED_H 23C2 23C4
ST7_XTAL_IN     23C5
STOP_AGP_L      13D2 13D4 19A7
SUTRO_ALS_GAIN_SW 23C4 24B2 39C2
SUTRO_ALS_OUT   23C4 24B2 39C2
SYSCLK_CPU      5C3 9A6 36D1
SYSCLK_CPU_UF   9A6 36D1
SYSCLK_DDRCLK_A0 10D4 12D8 36D1
SYSCLK_DDRCLK_A0_L 10D4 12D8 36D1
SYSCLK_DDRCLK_A0_L_UF 10B6 10D5 36D1
SYSCLK_DDRCLK_A0_UF 10B6 10D5 36D1
SYSCLK_DDRCLK_A1 10D4 12A6 36D1
SYSCLK_DDRCLK_A1_L 10D4 12A6 36D1
SYSCLK_DDRCLK_A1_L_UF 10B6 10D5 36D1
SYSCLK_DDRCLK_A1_UF 10B6 10D5 36D1
SYSCLK_DDRCLK_B0 10D4 12D3 36D1
SYSCLK_DDRCLK_B0_L 10C4 12D3 36C1
SYSCLK_DDRCLK_B0_L_UF 10B6 10C5 36D1
SYSCLK_DDRCLK_B0_UF 10B6 10D5 36D1
SYSCLK_DDRCLK_B1 10C4 12A5 36C1
SYSCLK_DDRCLK_B1_L 10D4 12A5 36C1
SYSCLK_DDRCLK_B1_L_UF 10B6 10D5 36D1
SYSCLK_DDRCLK_B1_UF 10B6 10D5 36D1
SYSCLK_LA_TP    9A6
SYSTEM_CLK_EN   15A5 15B7 15C7 30C4
THERM1_A_DM     25A6 25A7 37A2
THERM1_A_DP     25A6 25A7 37A2
THERM1_DM       25A5 25B4 25B5 37A2
THERM1_DP       25A5 25B4 25B5 37A2
THERM1_M_DM     25B6 25B7 37A2
THERM1_M_DP     25B6 25B7 37A2
THERM2_A_DM     25A6 25A7 37A2
THERM2_A_DP     25A6 25A7 37A2
THERM2_DM       25A5 25B4 25B5 37A2
THERM2_DP       25A5 25B4 25B5 37A2
THERM2_M_DM     25B6 25B7 37A2
THERM2_M_DP     25B6 25B7 37A2
THERM_L_OC      25B3 30B2 30B4
TMDS_CLKN       20A1 21B1 21B2 22C8 37B2
TMDS_CLKP       20A1 21B1 21B2 22C8 37B2
TMDS_CLK_CMF    20B1
TMDS_CONN_CLKN  22C7 37B2 39A8
TMDS_CONN_CLKP  22C7 37B2 39B7
TMDS_D0_CMF     20B1
TMDS_D1_CMF     20C1
TMDS_D2_CMF     20C1
TMDS_DN<2..0>   20B1 20C1 20D1 21B1 21B2 22D5 22D6
                37B2 39A8 39B8
TMDS_DP<2..0>   20B2 20C2 20D2 21B1 21B2 22D5 22D6
                37B2 39A8
TPAD_F_RXD      23A7 39C4
TPAD_F_TXD      23A7 39C4
TPAD_RXD        23A8 30C2 30C4
TPAD_TXD        23A8 30B2 30C4
TPS2211_SHDN_L_PU 18C4
TV_C            22B6 39D6
TV_COMP         22B6 39D6
TV_GND1         22B6 38B6 39A7
TV_GND2         22A6 38B6 39A7
TV_Y            22B6 39D6
UIDE_ADDR<2..0> 14D7 24B4 24C4 37C5
UIDE_CS0_L      14C7 24C4 37C5
UIDE_CS1_L      14C7 24B4 37C5
UIDE_DATA<15..0> 14D7 24B4 24C4 24D4 37C5
UIDE_DIOR_L     14C7 24A4 37C5
UIDE_DIOW_L     14C7 24A4 37C5
UIDE_DMACK_L    14C7 24A4 37C5
UIDE_DMARQ      14C7 37C5
UIDE_INTRQ      14C7 37C5
UIDE_IOCHRDY    14C7 24A4 37C5
UIDE_REF        14C7 38C3
UIDE_RST_L      14C7 24A4 37C5
USB2_PCI_INT_L  15B5 15C7 26A8
USB2_PCI_REQ_L  13A7 13D7 26B7
USB_D1M         15C1 26A4 26A5 39B6
USB_D1P         15C1 26A4 26A5 39B6
USB_D2M         15D1 26A4 26A5 39B6
USB_D2P         15D1 26A4 26A5 39B6
USB_DAM         15B2 15D2 26A5
USB_DAP         15B2 15D2 26A5
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USB_DBM	15B2 15D2
USB_DBP	15B2 15D2
USB_DCM	15B2 15C2 26A5
USB_DCP	15B2 15C2 26A5
USB_DDM	15B2 15C2
USB_DDP	15B2 15C2
USB_DEM	15B2 15C2 37B2
USB_DEP	15B2 15C2 37B2
USB_DFM	15B2 37B2
USB_DFP	15B2 37B2
USB_OC_AB_L	15B2 15C7
USB_OC_CD_L	15B2 15C7
USB_OC_EF_L	15B2 15C7
USB_PWREN_AB_L	15B2 15C7
USB_PWREN_CD_L	15B2 15C7
USB_PWREN_EF_L	15B2 15D7
VCORE_BOOST	34C4 38C1
VCORE_BST	34C5 38C1
VCORE_CC	34B6 38B1
VCORE_DH	34B5 38C1
VCORE_DL	34B5 38C1
VCORE_FAST<4..1>	34D2 34D3 34D5
VCORE_FB	34B5 38B1 39A2
VCORE_GND	34B5 38B1
VCORE_GNDA	34B6
VCORE_GNDDIV	34A5 34B5 38B1
VCORE_GNDDIV_TEST	34A4
VCORE_GNDSNS	34A1 34A5 38B1
VCORE_GNDSNS_TEST	34A4
VCORE_ILIM	34C6 38C1
VCORE_LX	34B5 38C1
VCORE_MUX_EN	34D5
VCORE_MUX_SEL	34D5
VCORE_REF	34B6 38C1
VCORE_SHDN_L	34C6
VCORE_SLOW<4..1>	34D6
VCORE_SNS	34A1 38B1
VCORE_TIME	34B4 38B1
VCORE_TON	34B6 38C1
VCORE_VCC	34C6 38C1
VCORE_VGATE	15B5 15B7 34B4 38B1
VCORE_VID<4..0>	34A3 34B8 34D4
VGA_B	22C6 22D7 39D7
VGA_G	22C5 22D7 39D7
VGA_HSYNC	21D4 22C6 39D7
VGA_R	22C5 22D7 39D7
VGA_VSYNC	21D4 22C5 39D7
VIPPCLK_PD	19C2

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*** Unit Cross-Reference ***
--- for the entire design --

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C2	CAP	34D1
C3	CAP	34D2
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C410	CAP	20B1
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C414	CAP	34C3
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C574	CAP	32A5
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C576	CAP	28D5
C577	CAP	28C6
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C687	CAP	8A2
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C690	CAP	22B8
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C693	CAP_P	34B1
C694	CAP_P	34B2
C695	CAP_P	34B1
C696	CAP_P	34B1
C697	CAP_P	34B2
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C779	CAP	28D8
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C785	CAP_P	32C2
C786	CAP_P	32C2
C787	CAP_P	32C2
C788	CAP	23D4
C789	CAP	23D5
C790	CAP_P	33C1
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C792	CAP_P	33A7
C793	CAP	33C2
C794	CAP	30B2
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C836	CAP	26C2
C837	CAP	34D4
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C856	CAP	25B2
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C862	CAP	29B3
C863	CAP	29D3
C864	CAP	29D2
C865	CAP	22B4
C866	CAP	25C6
C867	CAP	25C6
C1000	CAP	28C5
C1600	CAP	16B3
C1601	CAP	16B2
C1602	CAP	16B1
D1	DIODE	27B7
D2	DIODE_SCHOT	34C4
D3	DIODE_SCHOT	32C5
D4	DIODE	32C7
D5	DIODE	20C6
D6	DIODE_DUAL_6P	29D3
D7	DIODE_SCHOT	33D5
D8	DIODE_DUAL_6P	29D2
D9	DIODE_SCHOT	32B4
D10	DIODE	31C5
D11	DIODE	31C3
D12	DIODE_SCHOT	32A4
D13	DIODE_DUAL_6P	29B4
D14	DIODE_SCHOT	33D4
D15	DIODE_DUAL_6P	29B4
D16	DIODE	33B6
D17	DIODE_SCHOT	32B6
D18	DIODE_SCHOT	32A6
D19	DIODE_SCHOT	32A6
D20	DIODE_SCHOT	28D7
D21	DIODE_SCHOT	22D5
D22	DIODE	33C7
D23	DIODE_SCHOT	35B6
D24	DIODE_SCHOT	20C5
D25	DIODE	34B2
D26	DIODE	32C4
D27	DIODE_SCHOT_3P2	28D8
D28	DIODE	31D1
D29	DIODE	31B2
D30	DIODE	31D2
D31	DIODE	29D5
D32	DIODE_SCHOT	35B2
D33	DIODE	33C3
DP1	DPAK3P	34C7 34D7
DP2	DPAK3P	35C3 35D6 35D7
DP3	DPAK3P	31C1 31C2 31D3
DP4	DPAK3P	29C8 29D7
DP20	DPAK3P	20D7
DZ1	ZENER	29D6
DZ2	ZENER	29D3
F1	FUSE	22D6
F2	FUSE	29D7
F3	FUSE	29D5
F4	FUSE	31D1
F5	FUSE	31D1
G1	OSC	28A4
J1	CON_F1ST_S2MT_SM	15A6
J2	CON_3RTSM_125	25B2
J3	CON_F14RT_S2MT_SM	24B1
J4	CON_3RTSM_125	25A3
J5	CON_10STSM_5087	25D3
J6	CON_12	34A4
J7	CON_F30RT_S2MT_SM	22B3
J8	CON_4RT_WRIB	22B1
J9	CON_F16ST_D_SMA	25D4
J10	CON_M80ST_D4MT_SM	18C2
J11	CON_M50SM_5MM	24B5
J12	CON_F14RT_S2MT_SM	32B8
J13	CON_M50SM_5MM	24D1
J14	CON_F30ST_D_SM	25D6
J15	CON_F40RT_S2MT_SM	23C6
J16	CON_F30RT_T6MT_TH1	22D6
J17	CON_F5RT_MINIDIN_TH	22B6
J18	CON_RJ45_SHORT_4MT_TH	27C1
J19	CON_M8RT_S_SM	31D8
J20	CON_F200RT_DDRDIMM_SM1	12D7
J21	CON_F80ST_D4MT_SM	24D5
J22	CON_F9RT_S2MT_SMA	29C1
J23	CON_F200RT_DDRDIMM_SM2	12D4
J24	CON_F6RT_S4MT_TH1	29A2
J25	CON_M8RT_S_SM	31A4
L1	IND	15D3
L2	IND	22A4
L3	IND	28D6
L4	IND	21D3
L5	IND	21D3
L6	IND	31A3
L7	IND	31A3
L8	IND	31A3
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L12	IND	22D7
L13	IND	22D8
L14	IND	35A4
L15	IND	22D7
L16	IND	22D8
L17	FILTER_4P	22C7
L18	IND	22D5
L19	IND	21A4
L20	IND	22B7
L21	IND	22B7
L22	IND	22A7
L23	IND	22A7
L24	IND	22B7
L25	IND	20C5
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L27	IND	27C4
L28	IND	22B2
L29	IND	22B2
L30	IND	35B7
L31	IND_3P	34C2
L32	IND_3P	32C4
L33	IND_3P	33D7
L34	IND	29C4
L35	IND_3P	33D2
L36	IND	31B2
L37	IND	29C5
L38	IND	35B2
L39	IND	23C1
L40	IND	31A3
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L42	IND	23A7
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L44	IND	23A7
L45	IND	23C7
L46	IND	23A7
L47	IND	27D3
L48	IND	26D7
L49	IND	15C6
L50	IND	15C5
L51	FILTER_4P	29B3
L52	FILTER_4P	29A3
L53	IND	21D1
L54	IND	29D4
PD1	PHOTODIODE_2P	23D8
Q1	TRA_FDG6324L	22B2
Q2	TRA_2N7002	22A6
Q3	TRA_2N7002DW	33A3 33A4
Q4	TRA_2N7002DW	31C6 31C7
Q5	TRA_SI3443DV	22A5
Q6	TRA_2N3904	34D7
Q7	TRA_FDS3670	29D6
Q8	TRA_SI4435DY	31D6
Q9	TRA_FDG6324L	32D6
Q10	TRA_SI4435DY	31D5
Q11	TRA_2N3904	34D7
Q12	TRA_2N7002DW	20B5 20C7
Q13	TRA_2N7002	35C6
Q14	TRA_2N7002DW	31C2 31C5
Q15	TRA_2N7002DW	33B5
Q16	TRA_SI4435DY	31D2
Q17	TRA_2N7002DW	29C8 33A6
Q18	TRA_2N3906	23C1
Q19	TRA_2N7002DW	31B7 31B8
Q20	TRA_2N7002DW	23C2 23C3
Q21	TRA_SI3443DV	33B2
Q22	TRA_2N7002DW	31B6
Q23	TRA_2N7002DW	31A7
Q24	TRA_SI3443DV	33A7
Q25	TRA_2N3904	7C6
Q26	TRA_2N7002	7C7
Q27	TRA_SI3446DV	25B3
Q28	TRA_2N7002DW	7C7
Q29	TRA_2N7002DW	22C4 22D4
Q30	TRA_SI3446DV	25A3
Q31	TRA_2N3904	25B6
Q32	TRA_TP0610	22D3
Q33	TRA_2N7002DW	22C2
Q34	TRA_2N3904	22D1
Q35	TRA_SI3443DV	33A7
Q36	TRA_2N3904	22C1
Q37	TRA_SI3446DV	35D7
Q38	TRA_2N3904	25A6
Q39	TRA_IRF7811W	20C6
Q40	TRA_IRF7805	34C3
Q41	TRA_IRF7805	34C4
Q42	TRA_IRF7805	20C6
Q43	TRA_SI4888DY	33C6
Q44	TRA_IRF7822	34B3
Q45	TRA_IRF7822	34B4
Q46	TRA_IRF7822	34B3
Q47	TRA_IRF7811W	35B6
Q48	TRA_IRF7805	35C6
Q49	TRA_SI3443DV	25D7
Q50	TRA_IRF7805	32C4
Q51	TRA_IRF7811W	32C4
Q52	TRA_SI4888DY	33D6
Q53	TRA_2N3904	25A6
Q54	TRA_IRF7805	31B3
Q55	TRA_IRF7811W	31B3
Q56	TRA_2N3904	25B6
Q57	TRA_2N7002	30A3
Q58	TRA_IRF7811W	35B3
Q59	TRA_IRF7805	35C3
Q60	TRA_SI4435DY	31D1
Q61	TRA_SI4888DY	33D3
Q62	TRA_SI4888DY	33C3
Q63	TRA_2N3906	23B8
Q64	TRA_2N3906	23B8
Q65	TRA_2N7002DW	27A7 27B7
Q66	TRA_2N7002DW	31A4 31C3
Q68	TRA_2N7002DW	22C4 23C7
Q70	TRA_TP0610	22C2
Q2000	TRA_2N3904	20D7
Q2001	TRA_2N3904	20D7
Q3100	TRA_2N7002DW	31C3 31C4
R1	RES	23B3
R2	RES	15D8
R3	RES	24C4
R4	RES	15C1
R5	RES	5D4
R6	RES	7B6
R7	RES	15A6
R8	RES	15A3
R9	RES	24A7
R10	RES	24A8
R11	RES	24A8
R12	RES	5B1
R13	RES	5B1
R14	RES	7A6
R15	RES	14C3
R16	RES	24A3
R17	RES	24C2
R18	RES	24B8
R19	RES	5A2
R20	RES	23B3
R21	RES	23B3
R22	RES	19C6
R23	RES	5A2
R24	RES	5C1
R25	RES	15A6
R26	RES	14C7
R27	RES	14C7
R28	RES	19C6
R29	RES	19B2
R30	RES	19B2
R31	RES	19C2
R32	RES	5B1
R33	RES	23B3
R34	RES	24A4
R35	RES	19B4
R36	RES	24A1
R37	RES	5C1
R38	RES	5C1
R39	RES	5D1
R40	RES	35A6
R41	RES	24A3
R42	RES	24A7
R43	RES	24A2
R44	RES	5C1
R45	RES	15C2
R46	RES	24A3
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R86	RES	9C8
R87	RES	9D7
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R93	RES	9B2
R94	RES	9B8
R95	RES	9C7
R96	RES	9D8
R97	RES	9C8
R98	RES	9A6
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R100	RES	9B2
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R102	RES	9C8
R103	RES	9C7
R104	RES	9A6
R105	RES	14C3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401228	0A

SCALE	SHT	OF
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D C B A

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RP27  RPAK4P  10A4 10A5 10A5
RP28  RPAK4P  15A8 15B8 15C8 15D8
RP29  RPAK4P  10A4 10B4 10B5
RP30  RPAK4P  10A4 10A5 10B4 10B5
RP31  RPAK4P  10D4 10D4 10D5 10D5
RP32  RPAK4P  10D4 10D4 10D5 10D5
RP33  RPAK4P  10C4 10C4 10C5 10C5
RP34  RPAK4P  10C4 10C4 10C5 10C5
RP35  RPAK4P  28A8
RP36  RPAK4P  28B8
RP37  RPAK4P  26B8
RP38  RPAK10P2C 18A8
RP39  RPAK4P  26A7
RP40  RPAK4P  15B8 15C1 15C2
RP41  RPAK4P  15C8
RP42  RPAK4P  15B8 15C8 15D1
RP43  RPAK4P  24B7 24B8 24C8
RP44  RPAK4P  24C7 24C8 24D7
RP45  RPAK4P  8D8
RP46  RPAK4P  8D8
RP47  RPAK4P  15B8 15C8
RP48  RPAK4P  23B1
RP49  RPAK4P  30C1 30C1 30D1
RP50  RPAK10P2C 23B5
RP51  RPAK4P  23B1 23C3 26C8
RP52  RPAK4P  30C8 30D8
RP53  RPAK10P2C 23B5
RP54  RPAK4P  26B3 26B4 26D2
RP55  RPAK4P  21B3
RP56  RPAK4P  21B3
RP57  RPAK4P  21B1
RP58  RPAK4P  21B1
SH1   SHLD_3P_EMI 4D2
SP1   SPKR_CLIP_P84 4C3
SP2   SPKR_CLIP_P84 4C3
SP3   SPKR_CLIP_P84 4C2
SP4   SPKR_CLIP_P84 4C2
SP5   SPKR_CLIP_P84 4C2
T1    XFR_ENET_1000BT 27B3
U1    SN74AUC1G04 7A7
U2    SN74AUC1G08 23A3
U3    SN74AUC1G08 23B3
U4    LTC3411   35A5
U5    TRA_SI3447DV 35A2
U6    SRAM_DDR_128KX36 8D2
U7    SRAM_DDR_128KX36 8D5
U8    LTC1761   20A7
U9    TRA_SI3447DV 35C1
U10   VREG_LT1962 15D6
U11   CBTV4020  11C2
U12   CBTV4020  11C4
U13   CBTV4020  11C5
U14   CBTV4020  11C7
U15   LTC4210   29D6
U16   COMPARATOR_LMC7211 31C7
U17   FEPR_1MX8 10C2
U18   LTC1625   32C5
U19   LTC1778   20B7
U20   PWR_CNTRL_TPS2211 18D3
U21   MAX1717   34C5
U22   COMPARATOR_LMC7211 32C7
U23   MAX1715   35C4
U24   AMP_MAX4172 31D5
U25   VREG_LP2951 32B3
U26   PCI1510GGU 18C5
U27   LTC3707   33C4
U28   TSB81BA3  28B6
U29   VREG_LP2951 32B5
U30   MAX1772   31B5
U31   VREG_LM2594 28D7
U32   7432      22A2 30A7 30A8
U33   LTC1761   28B8
U34   VREG_LT1962 28C8
U35   COMPARATOR_LMC7211 31A6
U36   FEPR_256KX8_ST72264_BGA 23D5
U37   EEPROM_16KX8_M24128B 23D3
U38   MAX6804   30B7
U39   M16C62    30D5
U40   OPAMP_MAX4236EUTT 23D7
U41   PI3B3257  34D4
U42   APOLLO483 5C5 6D5 6D7
U43   MAP31_612P 19D1 19D3 19D6 20C3 21D5
U44   INTREPID  9D4 10D7 13D3 13D7 14D4 14D8 15C4
                16D4 16D7
U45   COMPARATOR_LMC7211 22C2
U46   CLK_GEN_CY25811 21A4
U47   VREG_LT1962 6B3
U48   ADM1031   25B4
U49   TRANSCEIVER_88E1111 27C6
U50   MAX1916   23A5
U51   LTC3405   27D4
U52   UPD720101_FBGA 26C6
U53   COMPARATOR_LMC7211 30A3
U54   OPAMP_LMC7111 31D3
U55   SIL1162   21C2
U56   CLK_GEN_CY28512 15B6
U1600 VREG_LT1962 16B2
XW1   SHORT     35A4
XW2   SHORT     34B1
XW3   JUMPER    35B8
XW4   SHORT     20B7
XW5   JUMPER    33D8
XW6   SHORT     32B5
XW7   SHORT     34B4
XW8   SHORT     35B6
XW9   SHORT     34B4
XW10  JUMPER    32C2
XW11  SHORT     33B4
XW12  JUMPER    33D1
XW13  JUMPER    35A4
XW14  SHORT     22B8
XW15  SHORT     22A8
XW16  JUMPER    20C5
XW17  SHORT     25C7
XW18  SHORT     34C2
XW19  JUMPER    35B1
XW20  SHORT     31B3
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Y1    CRYSTAL   15A5
Y2    CRYSTAL_4PIN 21B4
Y3    CRYSTAL   27A7
Y4    CRYSTAL   23C6
Y5    CRYSTAL   30B7
Y6    CRYSTAL_4PIN 30B3
Y7    CRYSTAL   26D4
ZT1   MTGHOLE   4D3
ZT3   MTGHOLE   4D4
ZT4   MTGHOLE   4C4
ZT5   MTGHOLE   4D4
ZT6   MTGHOLE   4D4
ZT7   MTGHOLE   4D4
ZT8   MTGHOLE   4C4
ZT10  MTGHOLE   4D3
ZT14  MTGHOLE   4D3
ZT18  HOLE_VIA  4B4
ZT19  HOLE_VIA  4B4
ZT20  HOLE_VIA  4B4
ZT21  HOLE_VIA  4B4
ZT22  HOLE_VIA  4B4
ZT23  HOLE_VIA  4B4
ZT24  HOLE_VIA  4B4
ZT25  HOLE_VIA  4B4
ZT26  HOLE_VIA  4B4
ZT27  HOLE_VIA  4A4
ZT28  HOLE_VIA  4A4
ZT29  HOLE_VIA  4A4
ZT30  HOLE_VIA  4A4
ZT31  HOLE_VIA  4A4
ZT32  HOLE_VIA  4A4
ZT33  HOLE_VIA  4B4
ZT34  HOLE_VIA  4B4
ZT35  HOLE_VIA  4B4
ZT36  HOLE_VIA  4B4
ZT37  HOLE_VIA  4B4
ZT38  HOLE_VIA  4B4
ZT39  HOLE_VIA  4B4
ZT40  HOLE_VIA  4B4
ZT41  HOLE_VIA  4B4
ZT42  HOLE_VIA  4A4
ZT43  HOLE_VIA  4A4
ZT44  HOLE_VIA  4A4
ZT45  HOLE_VIA  4A4
ZT46  HOLE_VIA  4A4
ZT47  HOLE_VIA  4A4
ZT48  HOLE_VIA  4B3
ZT49  HOLE_VIA  4B3
ZT50  HOLE_VIA  4B3
ZT51  HOLE_VIA  4B3
ZT52  HOLE_VIA  4B3
ZT53  HOLE_VIA  4B3
ZT54  HOLE_VIA  4B3
ZT55  HOLE_VIA  4B3
ZT56  HOLE_VIA  4B3
ZT57  HOLE_VIA  4A3
ZT58  HOLE_VIA  4A3
ZT59  HOLE_VIA  4A3
ZT60  HOLE_VIA  4A3
ZT61  HOLE_VIA  4A3
ZT62  HOLE_VIA  4A3
ZT63  HOLE_VIA  4B3
ZT64  HOLE_VIA  4B3
ZT65  HOLE_VIA  4B3
ZT66  HOLE_VIA  4B3
ZT67  HOLE_VIA  4B3
ZT68  HOLE_VIA  4B3
ZT69  HOLE_VIA  4B3
ZT70  HOLE_VIA  4B3
ZT71  HOLE_VIA  4B3
ZT72  HOLE_VIA  4A3
ZT73  HOLE_VIA  4A3
ZT74  HOLE_VIA  4A3
ZT75  HOLE_VIA  4A3
ZT76  HOLE_VIA  4A3
ZT100 HOLE_VIA  4A3
ZT101 HOLE_VIA  4B2
ZT102 HOLE_VIA  4B2
ZT103 HOLE_VIA  4B2
ZT104 HOLE_VIA  4B2
ZT105 HOLE_VIA  4B2
ZT106 HOLE_VIA  4B2
ZT107 HOLE_VIA  4B2
ZT108 HOLE_VIA  4B2
ZT109 HOLE_VIA  4B2
ZT110 HOLE_VIA  4A2
ZT111 HOLE_VIA  4A2
ZT112 HOLE_VIA  4A2
ZT114 HOLE_VIA  4A2
ZT115 HOLE_VIA  4A2
ZT116 HOLE_VIA  4A2
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