1. All resistance values are in Ohms, 0.1 Watt +/- 5%.

2. All capacitance values are in microfarads.

3. All crystals & oscillator values are in Hertz.
<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ALTERNATE FOR PART NUMBER</th>
<th>BOM OPTION</th>
<th>REF DES</th>
<th>COMMENTS</th>
</tr>
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<tbody>
<tr>
<td>PCB, SCHEM, MLB, M23 1051-6790</td>
<td>SCH1</td>
<td>CRITICAL</td>
<td>17_INCH_LCD</td>
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<tr>
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<td>CRITICAL</td>
<td>17_INCH_LCD</td>
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<td>SCH1</td>
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### PROCESSORS

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### MISC PARTS

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<th>COMMENTS</th>
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<td>LED700, LED702</td>
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<td>126S0068</td>
<td>EL CAP</td>
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### ASICS

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<tr>
<td>820-1783</td>
<td>MLB1, 17_INCH_LCD</td>
<td>CRITICAL</td>
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KODIAK CORE VOLTAGE REGULATOR

NOTE:

LOAD FROM POWER SUPPLY
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW

1.35V R1205=3.65K
1.30V R1205=3.24K
1.25V R1205=3.65K

VOUT=VREF*(R1203+R1205)/R1205=1.25VDC

MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.45MM
MIN_LINE_WIDTH=0.6MM

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NOTE:

1.25V   R1205=3.65K
1.30V R1205=3.24K
1.25V R1205=3.65K

VOUT=VREF*(R1203+R1205)/R1205=1.25VDC
NOTE:

- Set output to 2.5V
- VRD500SC VREG=1.24VDC
- VO(0)=VREG*(R1581+R1582)+1=5.005VDC

Power budget current of total rails
- 0.2A peak
- 0.1A continuous

NOSTUFF option to delay 2.5V PWRON to come up with 3.3V PWRON

**PEAK CURRENT 0.1A**

**PP2V5_RUN FET SWITCH**
- Peak current 0.1A

**PP2V5_PWRON FET SWITCH**
- Peak current 0.1A
SHASTA ALIASES

PCI_RESET_L is an "alias" of NB_PCI_RESET_L (36)
and NB_PCI_RESET_L (36)

SHASTA JTAG

These pins have internal pullups or pulldowns

MAKE_BASE=TRUE

DIFFERENTIAL_PAIR=TSENSE_NB
MIN_NECK_WIDTH=0.25MM

NET_PHYSICAL_TYPE=10MIL_WIDTH

PCI_AIRPORT_RESET_L

JTAG_SB_TCK

RAI_EXP_INTR_L<0>

RAI_EXP_INTR_L<1>

(56) SOME OF THESE ARE NOT STUFF SHASTA ALIASES

SHASTA GPIO TERMINATIONS
(SOME OF THESE ARE NOT STUFF ON PAGE 24)

JTAG_NB_TRST_L

JTAG_NB_TDO

NOTE: LOW = DISABLE PMR_CLK

PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK

PLACE R2012 IN AN ACCESSIBLE LOCATION

WITHDRAWN
other Shasta supplies.

Must power Shasta VCore rail before any PCI, otherwise 3.3V.

VIO1 TO SAME IF 64-BIT appropriate PCI bus voltage and CONNECT VIO2 TO

NOTE: PCI pads use the VIO supply to meet -PP2V5_PWRON_SB

Power aliases required by this page:

[Diagram with components and connections]

Shasta Core Power

APPLE COMPUTER INC. 051-6790 19

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PLACE NEAR PULSAR2

PP1V5_PWRON_PULSAR

PP2506

PLACE NEAR PULSAR2

PP2505

PP3V3_PSL_XTAL

PP3V3_PLSR_I

NOSTUFF

VDD_33_XTAL

VDD_OVDD_4 VSS_OVDD_4

VDD_15_12_3

VDD_15_12_1

VDD_33_I VSS_33_I

VDD_15_C2

VDD_OVDD_5 VSS_OVDD_5

VDD_12_3 VSS_12_3

VDD_12_5

VDD_12_2

VDD_OVDD_2

VDD_15_C4

VDD_12_4 VSS_12_4

VSS_OVDD_3

VSS_OVDD_1VDD_OVDD_1

VSS_33_BC

VSS_15_C4

VSS_12_6

VDD_12_4

VDD_OVDD_1

VDD_33_BC

VSS_33_BC

VDD_15_C4

VSS_OVDD_3

VSS_OVDD_1VDD_OVDD_1

VDD_33_XTAL

VDD_OVDD_2

VDD_15_C4

VDD_12_4 VSS_12_4
N/C ALIASES

N/C RAINIER CLOCKS

N/C CPUB CLOCKS

N/C QUASAR CLOCKS

CLOCK CONSTRAINTS

NOTE:
ALL OTHER CLOCK CONSTRAINTS ON THEIR RESPECTIVE BUS PAGES
Review the latest SMU specification provided on this page. Please.

NOTE: All analog inputs to SMU should have

<table>
<thead>
<tr>
<th>BOM options provided by this page:</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NONE)</td>
</tr>
</tbody>
</table>

**System Management Unit**

**Alternate Functions**

**Tower & Server**
Q63 USE PWM FAN

Aliases are only necessary where use differs from Q63.

M23/M33 only connects I2C to Kodiak now; CPU has pullups on its PG.

M23/M33 uses Fan_RPM0 (P7.3), Fan_RPM1 (P7.5), Fan_RPM2 (P7.7) only.

Q63 uses SMU_SER_SEL for SPDIF-SMU-DEBUG. Not M23/M33 feature.

M23/M33 uses Tach0 (P2.2), Tach1 (P2.3), Tach2 (P2.4) only.

Q63 uses SMU_REN_SEL for VID control. Not M23/M33 feature.

M23/M33 doesn’t need to make VDNAP0 do triple-duty.

CPU_VID_LE0 for Q82. Not M23/M33 feature.

M23/M33 doesn’t have those fans.

Q63 use of P9.1 is Tach 8.

M23/M33 has no slots.

Comments (Only if use differs from Q63)

Select between CPU or NB TMS and TDO from/to SMU

M23/M33 doesn’t need to make VDNAP0 do triple-duty.

SMU_CPU_NB_SEL

SMU_JTAG_TCK

I2C_SMU_A_SCL

NC_SMU_FAN_TACH4

NC_SMU_FAN_TACH3

NC_SYS_DOOR_AJAR_L

NC_SMU_CPU_VID_LE0

NC_SMU_SER_SEL

NC_SMU_FAN_RPM4

NC_SMU_FAN_RPM3

CPU_VID_LE1

IIC_A_DAT

FAN_TACH2_7

FAN_CNTL0_6

CPU_BYPASS

CPU_TEMP0

CPU_SENSE_V0

POWERFAIL*

PS1_3

CPU_SENSE_I1

FAN_CNTL0_5

CPU_TEMP1

POWERFAIL*

PS1_4

CPU_BYPASS

CPU_SENSE_V1

FAN_CNTL0_4

CPU_TEMP2

POWERFAIL*

PS1_5

CPU_BYPASS

CPU_SENSE_V2

FAN_CNTL0_3

CPU_TEMP3

POWERFAIL*

PS1_6

CPU_BYPASS

CPU_SENSE_V3

FAN_CNTL0_2

CPU_TEMP4

POWERFAIL*

PS1_7

CPU_BYPASS

CPU_SENSE_V4

FAN_CNTL0_1

CPU_TEMP5

POWERFAIL*

PS1_8

CPU_BYPASS

CPU_SENSE_V5

FAN_CNTL0_0

CPU_TEMP6

POWERFAIL*

PS1_9
EI BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

WE HAVE USED A DIFFERENT ELECTRICAL_SUBCIRCUIT_NET FOR CPU_A AND CPU_B.
Q63: See P.20 for more decoupling caps for these pins.
DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS
GPU Vcore VREG

GPU 1.7V VDDC_CT

GPU 1.20V PCIE PVDD

GPU 1.80V TPVDD

GPU 2.5V A2VDD

GPU 1.8V VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR 8970S XT

SECTION VDDC 3.3V OC
VDDC=VDDR-P8550/P8505
MODEL:STU

PEAK CURRENT OF PVCORE_GPU
7.2A WITH 8970S XT
8.3A WITH RV380 XT

VOUT = 1.802V
VOUT = 0.59V * [1 + R8560 / R8561]

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

MIN_LINE_WIDTH=0.45MM
MIN_NECK_WIDTH=0.25MM

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### KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

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<thead>
<tr>
<th>COL_NAME</th>
<th>ELECTRICAL_CONSTRAINT</th>
<th>DIFFERENTIAL_PAIR</th>
<th>NET_PHYSICAL_TYPE</th>
<th>NET_IMPLEMENT_TYPE</th>
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<tbody>
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### KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

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<th>COL_VALUE</th>
<th>COL.Warn</th>
<th>COL.VALUE_1</th>
<th>COL.VALUE_2</th>
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ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

<table>
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<tr>
<th>Name</th>
<th>Value</th>
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PLACE CLOSE TO SHASTA

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PCI SERIES TERMINATION

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NOTE: This AirPort implementation does not support PME#.
USB 2.0 PCI Interface

DRAWING NUMBER

REV.

A

B

C

D

SCALE

NONE

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4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PPI2V_SATA_VDD AND THEN HECK DOWN TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127 ARE SET BY G63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TAIWAN AMERICA PN: H20122401.

4-11-05.
PPI2V_ALL REG. IS SET TO BE 1.2V TO 1.23V AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL HELP MITIGATE THE LOSS ACROSS THE Q1306 PET (13323REV).

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA J900.
ADDED DECOUPLING CAPS FOR J901 PPS,VATA NET.
PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

ENET SERIES TERM

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EXTRA CONSTRAINTS TO SUPPLEMENT THE MISSING NET PHYSICAL FROM EARLIER PAGE

<table>
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<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
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</table>

Spare gnd vias for layer traversals during routing

Put development leads on top side of board.
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
AUDI2S0OUT = PP3V3_AUDIO

AUDI2S0_RESET_L

AUDI2S0_SYNC

AUDI2S0_BITCLK

AUDI2S0_SB_TO_DEV_DTI

AUDI2S0_DEV_TO_SB_DTI

AUDI2S0_BCK

AUDI2S0_SCKI

AUDI2S0_ADR

AUDI2S0_SCL

AUDI2S0_I2CEN

AUDI2S0_DOUTS

AUDI2S0_DIN

AUDI2S0_AGC

AUDI2S0_AGND

AUDI2S0_VOL2

AUDI2S0_VOL1

AUDI2S0_VCS

AUDI2S0_VCOM2

AUDI2S0_VCOM1

AUDI2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO_CODEC

MIN_LINE_WIDTH = 0.6MM

MIN_NECK_WIDTH = 0.25MM

NET_SPACING_TYPE = AUDIO

AUDI_CODEC_MCLK

AUDI_PCM_VCOM

AUDI_PCM_REF1

AUDI_PCM_REF2

AUDI_CODEC_IN_R

AUDI_CODEC_IN_L

AUDI_CODEC_OUT_L

AUDI_CODEC_OUT_R

AUDI_CODEC_OUT

AUDI_MICIN_P

AUDI_MICIN_N

AUDI_PCM_MBIAS

AUDI_PCM_MCLK

AUDI_PCM_VCS

AUDI_PCM_REF1

AUDI_PCM_REF2

VOLTAGE = 4.5V

PP4V5_AUDIO_ANALOG

GND_AUDIO_CODEC

MIN_LINE_WIDTH = 0.6MM

MIN_NECK_WIDTH = 0.25MM

NET_SPACING_TYPE = AUDIO

I2C_AUDIO_SCL

I2C_AUDIO_SDA

I2S0_RESET_L

I2S0_BCK

I2S0_SCKI

I2S0_ADR

I2S0_SCL

I2S0_I2CEN

I2S0_DOUTS

I2S0_DIN

I2S0_AGC

I2S0_AGND

I2S0_VOL2

I2S0_VOL1

I2S0_VCS

I2S0_VCOM2

I2S0_VCOM1

I2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO

MIN_LINE_WIDTH = 0.30MM

NET_SPACING_TYPE = AUDIO

I2S0_BCK

I2S0_SCKI

I2S0_ADR

I2S0_SCL

I2S0_I2CEN

I2S0_DOUTS

I2S0_DIN

I2S0_AGC

I2S0_AGND

I2S0_VOL2

I2S0_VOL1

I2S0_VCS

I2S0_VCOM2

I2S0_VCOM1

I2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO

MIN_LINE_WIDTH = 0.10MM

NET_SPACING_TYPE = AUDIO

I2S0_BCK

I2S0_SCKI

I2S0_ADR

I2S0_SCL

I2S0_I2CEN

I2S0_DOUTS

I2S0_DIN

I2S0_AGC

I2S0_AGND

I2S0_VOL2

I2S0_VOL1

I2S0_VCS

I2S0_VCOM2

I2S0_VCOM1

I2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO

MIN_LINE_WIDTH = 0.10MM

NET_SPACING_TYPE = AUDIO

I2S0_BCK

I2S0_SCKI

I2S0_ADR

I2S0_SCL

I2S0_I2CEN

I2S0_DOUTS

I2S0_DIN

I2S0_AGC

I2S0_AGND

I2S0_VOL2

I2S0_VOL1

I2S0_VCS

I2S0_VCOM2

I2S0_VCOM1

I2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO

MIN_LINE_WIDTH = 0.10MM

NET_SPACING_TYPE = AUDIO

I2S0_BCK

I2S0_SCKI

I2S0_ADR

I2S0_SCL

I2S0_I2CEN

I2S0_DOUTS

I2S0_DIN

I2S0_AGC

I2S0_AGND

I2S0_VOL2

I2S0_VOL1

I2S0_VCS

I2S0_VCOM2

I2S0_VCOM1

I2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO

MIN_LINE_WIDTH = 0.10MM

NET_SPACING_TYPE = AUDIO

I2S0_BCK

I2S0_SCKI

I2S0_ADR

I2S0_SCL

I2S0_I2CEN

I2S0_DOUTS

I2S0_DIN

I2S0_AGC

I2S0_AGND

I2S0_VOL2

I2S0_VOL1

I2S0_VCS

I2S0_VCOM2

I2S0_VCOM1

I2S0_VCOM

VOLTAGE = 3.3V

PPV_3V3_AUDIO