2. All capacitance values are in microfarads.

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</tr>
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<tr>
<td>Signal Alias</td>
<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>FUNC TEST 2 OF 2</td>
<td>FINO-M23 08/26/2005</td>
</tr>
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<td>1.8V VREG</td>
<td>M33-PF 06/20/2005</td>
</tr>
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<td>1.5V Vreg</td>
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<td>1.2V Vreg</td>
<td>FINO-M23 08/26/2005</td>
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<tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>Vestas Core / Misc</td>
<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
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<tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
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<td>q63 08/26/2005</td>
</tr>
<tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>PULSAR2 POWER</td>
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</tr>
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</tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>System Management Unit</td>
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</tr>
<tr>
<td>SMU SUPPLEMENTAL (1)</td>
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</tr>
<tr>
<td>SMU SUPPLEMENTAL (2)</td>
<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>SMU SUPPLEMENTAL (3)</td>
<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>SMU SUPPLEMENTAL (4)</td>
<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>Fan 0, 1 &amp; System Temp</td>
<td>FINO-M23 08/26/2005</td>
</tr>
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<td>M33-HS 08/04/2005</td>
</tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>KODIAK E1 PWR &amp; CAPS</td>
<td>q63 08/26/2005</td>
</tr>
<tr>
<td>KODIAK E1 A</td>
<td>q63 08/26/2005</td>
</tr>
<tr>
<td>CPU E1 AND IO</td>
<td>FINO-M23 08/26/2005</td>
</tr>
<tr>
<td>KODIAK E1 B</td>
<td>q63 08/26/2005</td>
</tr>
<tr>
<td>CPU STRAPS</td>
<td>FINO-M23 08/26/2005</td>
</tr>
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<td>FINO-M23 08/26/2005</td>
</tr>
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</tr>
<tr>
<td>CPU VCORE VREG</td>
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</tr>
<tr>
<td>CPU VCORE MORE BYPASS</td>
<td>FINO-M23 08/26/2005</td>
</tr>
</tbody>
</table>
### Table Items

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Part #</th>
<th>Package</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>343S0356</td>
<td>Vesta A4</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1343S0319</td>
<td>Pulsar2</td>
<td>100P</td>
<td>P8MM</td>
<td>BGA</td>
</tr>
<tr>
<td>343S0377</td>
<td>Flash, 1MX8</td>
<td>3.3V</td>
<td>90NS</td>
<td></td>
</tr>
</tbody>
</table>

### Processors

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Part #</th>
<th>Package</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3224</td>
<td>17 Inch LCD</td>
<td>50MV</td>
<td></td>
<td>U43001</td>
</tr>
<tr>
<td>337S3223</td>
<td>20 Inch LCD</td>
<td></td>
<td></td>
<td>U43003</td>
</tr>
</tbody>
</table>

### Asics

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Part #</th>
<th>Package</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3224</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>IC,DD3.1,1.9G,1.20V</td>
</tr>
<tr>
<td>337S3225</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>IC,DD3.1,1.9G,1.25V</td>
</tr>
<tr>
<td>337S3226</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>IC,DD3.0X,1.9G,1.25V</td>
</tr>
</tbody>
</table>

### Misc Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Part #</th>
<th>Package</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3220</td>
<td>20 Inch LCD</td>
<td>CBGA-576-1MM</td>
<td>1.9GHZ</td>
<td>U43002</td>
</tr>
<tr>
<td>337S3221</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>U43004</td>
</tr>
<tr>
<td>337S3229</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>U43005</td>
</tr>
</tbody>
</table>

### Alternates

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Part #</th>
<th>Package</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3228</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>IC,DD3.0X,1.9G,1.30V</td>
</tr>
<tr>
<td>337S3227</td>
<td>17 Inch LCD</td>
<td></td>
<td></td>
<td>IC,DD3.1,1.9G,1.15V</td>
</tr>
</tbody>
</table>

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The following nets are used only when the development run option is enabled.

The following nets are not used:

Test points because of routing density and signal integrity.

Test coverage will be by FCT. Notes for marking: do not include this list until for layout. Also, test points. This list is a result of PCB design.

An extra difficulty placing test points on these nets.

TO AVOID STUBS, ADDING NO_TEST TO ALL PCIE NETS.

TEST POINT BECAUSE OF ROUTING DENSITY.

THE FOLLOWING NETS ARE USED ONLY.

THE FOLLOWING NETS DO NOT EXIST:

JTAG test points here to be on the bottom of the board.

ADDER FUNK=test-true to these nets.
PP1V2_ALL VOLTAGE REGULATOR

PP1V2_PWRON FET SWITCH
PEAK CURRENT 1.3A
1.0A CONTINUOUS
PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH
PEAK CURRENT 1.3A
IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.2A/M23 IF NOT

NOTE:

SET OUTPUT=1.22-1.23V
VOD=VREF*(R1003+R1005)/R1005=1.22-1.23VDC
POWER BUDGET CURRENT OF TOTAL RAILS
PEAK CURRENT OF TOTAL RAILS

VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC
SET OUTPUT=1.22-1.23V

1.2V Vreg
PLACE LED NEAR VREG
NOTE:

- PEAK CURRENT 0.1A
- POWER BUDGET CURRENT OF TOTAL RAILS

- SET OUTPUT=2.5V
- VDIODE=0.5VDC
- VCC=VREF+(R1581+R1582)=1.5V

- NOSTUFF OPTION TO DELAY 2.5V PWRON TO COME UP WITH 3.3V PWRON

- RDSON=0.04 OHM
- RDSON=0.04 OHM@ VGS=2.5 V

- DSO-2V5_ALL VOLTAGE REGULATOR
- PP2V5_ALL VOLTAGE REGULATOR

- CRITICAL 6.3V CERM 1206 20% 10UF C1580
- CRITICAL 6.3V CERM 1206 20% 10UF C1580

- 0.01UF 20% 402 C1580
- 0.01UF 20% 402 C1580

- 5% MF-LF 1/16W 2 1 R1508
- 5% MF-LF 1/16W 2 1 R1508

- 5% MF-LF 1/16W 2 1 R1512
- 5% MF-LF 1/16W 2 1 R1512

- CRITICAL SI3446DV TSOP-LF
- CRITICAL SI3446DV TSOP-LF

- Q1503_G Q1504 Q1505_G Q1506

- 2.5V Vreg

- SYNCE_DATE=08/26/2005
- SYNCE_MASTER=FINO-M23
5V & 3.3V Fets

Q1601G

SYS_POWERUP_L_BUF

PP3V3_RUN

PP5V_PWRON

PP3V3_PWRON

PP12V_ALL

PP5V_ALL

PP3V3_ALL

SYNC_MASTER=FINO-M23

SYNC_DATE=08/26/2005

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other Shasta supplies. Must power Shasta VCore rail before any
BOM options provided by this page:
(NONE)

Signal aliases required by this page:
VIO1 TO SAME IF 64-BIT
CONNECT VIO2 TO

different drive timing

NOTE: PCI pads use the VIO supply to meet
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)

Power aliases required by this page:
7 =PP1V2_PWRON_SB_VCORE
119 =PP3V3_PWRON_SB

Page Notes

NO TEST=YES

PP_2V5_PWRON_SB

PP_3V3_PWRON_SB_PCI32

SEE_TABLE

I/O 2.5  -  2.5V -  20 mA (  60 mW)
I/O 3.3  -  3.3V - 220 mA ( 770 mW)
VDDPs    - 2.5V - 100 mA ( 250 mW)
DIGITAL  - 1.2V - 950 mA (1175 mW)
Shasta max (est 06/30/03) current:
NOTE: XGC required for Shasta GPIOs.

PLACE R2432 CLOSE TO SHASTA.
N/C ALIASES

N/C RAINIER CLOCKS

N/C CPUB CLOCKS

N/C QUASAR CLOCKS

CLOCK CONSTRAINTS

NOTE:
ALL OTHER CLOCK CONSTRAINTS ON THEIR RESPECTIVE BUS PAGES
To ensure missing pull-ups are reviewed, the latest SMU specification should be consulted. A 100pF capacitor should be connected to the SMU AVSS (CPU_SENSE_I/CPU_SENSE_V) to avoid any interference. The BOM options provided by this page include:

- **I474**: 100pF capacitor
- **I473**: 0.38MM spacing
- **PP2806**: 680K 3.3V H.T.
- **PP2804**: 2.2uf 16V SM
- **SM**: 31
- **PP3V3_ALL_SMU**: 0.38MM spacing
- **10UF**: 6.3V
- **Y2800**: 1 uf 50V S SN
- **AN21**: 0.38MM spacing
- **AN22**: 0.38MM spacing
- **AN23 TA1 in**: Y
- **AN24**: 0.38MM spacing
- **AN05**: 0.38MM spacing
- **R2825**: 402 W 40% 20% 1% Y
- **I2C_SMU_A_SCL**: 0.38MM spacing
- **I2C_SMU_A_SDA_OUT_L**: 0.38MM spacing
- **CPU_VID<1>/CPU_VID<2>:**
  - **P0[7]**
  - **P1[0]**
  - **P2[5]**
  - **P2[6]**
  - **P3[3]**
  - **P3[5]**
  - **P0[0]**
  - **P8[0]**
  - **P7[4]**
  - **P10[0]**
  - **VOLTAGE=0V**
- **SMU_FAN_RPM9**: 0.38MM spacing
- **SMU_FAN_PWM9**: 0.38MM spacing
- **SMU_FAN_TACH6**: 0.38MM spacing
- **SMU_POWERUP_L**: 0.38MM spacing
- **SMU_PWRSEQ_P9_6**: 0.38MM spacing
- **SMU_PWRSEQ_P9_5**: 0.38MM spacing
- **SYS_RESET_BUTTON_L**: 0.38MM spacing
- **SYS_POWERUP_L**: 0.38MM spacing
- **SYS_DOOR_AJAR_L**: 0.38MM spacing
- **SMU_FAN_RPM3**: 0.38MM spacing
- **SMU_FAN_RPM5**: 0.38MM spacing
- **PP3V3_RUN_SMU**: 0.38MM spacing
- **PP3V3_ALL_SMU**: 0.38MM spacing
- **PP3V3_ALL_SMU_AVCC**: 0.38MM spacing
- **Fuses**: 0.38MM spacing
- **SMU_PWRSEQ_P9_6**: 0.38MM spacing
- **SMU_PWRSEQ_P9_5**: 0.38MM spacing
- **Sout3**: 0.38MM spacing
- **CS1**: 0.38MM spacing
- **CS2**: 0.38MM spacing
- **SCLmm**: 0.38MM spacing
- **DIFFERENTIAL_PAIRNET_SPACING_TYPE**: 0.38MM spacing
- **Y2801**: 0.38MM spacing
- **SYNC_DATE=08/26/2005**: 0.38MM spacing
- **SYNC_MASTER=Q63**: 0.38MM spacing

The system management unit features:

- **System Management Unit**
  - **CPU_PWR**: 0.38MM spacing
  - **CPU_VDNAP2**: 0.38MM spacing
  - **CPU_VID<1>/CPU_VID<2>:**
    - **P0[7]**
    - **P1[0]**
    - **P2[5]**
    - **P2[6]**
    - **P3[3]**
    - **P3[5]**
    - **P0[0]**
    - **P8[0]**
    - **P7[4]**
    - **P10[0]**
    - **VOLTAGE=0V**
  - **SMU_PWRSEQ_P9_6**: 0.38MM spacing
  - **SMU_PWRSEQ_P9_5**: 0.38MM spacing
  - **SYS_RESET_BUTTON_L**: 0.38MM spacing
  - **SYS_POWERUP_L**: 0.38MM spacing
  - **SYS_DOOR_AJAR_L**: 0.38MM spacing
  - **SMU_FAN_RPM9**: 0.38MM spacing
  - **SMU_FAN_PWM9**: 0.38MM spacing
  - **SMU_FAN_TACH6**: 0.38MM spacing

The system management unit also includes:

- **Alternate Functions**
- **Tower & Server**

The diagram includes various components and connections, such as:

- **I474**
- **I473**
- **PP2806**
- **PP2804**
- **SM**
- **PP3V3_ALL_SMU**
- **10UF**
- **Y2800**
- **AN21**
- **AN22**
- **AN23 TA1 in**
- **AN24**
- **AN05**
- **R2825**
- **I2C_SMU_A_SCL**
- **I2C_SMU_A_SDA_OUT_L**
- **CPU_VID<1>/CPU_VID<2>**
- **Fuses**
- **Sout3**
- **CS1**
- **CS2**
- **SCLmm**
- **DIFFERENTIAL_PAIRNET_SPACING_TYPE**
- **Y2801**
- **SYNC_DATE=08/26/2005**
- **SYNC_MASTER=Q63**

The page also includes page notes and various annotations to guide the reader through the diagram.
REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CONNECT KODIAK EI A TO/FROM CPU
EI_CPU_TBEN_CLK
EI_CPU_SYSCLK_P
TP_CPU_APSYNCOUT
TP_NB_B_TRIGGER_OUT
NOTUSED_CPU_B1_SRESET_L
NOTUSED_CPU_B0_SRESET_L
NOTUSED_CPU_A1_SRESET_L
NC_NB_CPU_B1_INT_L
NC_NB_CPU_B0_INT_L
EI_NB_TO_CPU_SR_N<0..1>
EI_NB_TO_CPU_SR_P<0..1>
EI_NB_TO_CPU_CLK_P
EI_CPU_TO_NB_CLK_N
EI_CPU_TO_NB_CLK_P

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE
MAKE_BASE=TRUE

EI_CPU_A_TO_NB_AD<0..43>
EI_NB_TO_CPU_A_CLK_N
EI_NB_TO_CPU_A_CLK_P
EI_CPU_A_TO_NB_CLK_P
CPU_A0_TO_NB_QREQ_L
CPU_TO_NB_QREQ_L
NB_STOP_IS_CHKSTOP
NB_STOP_IS_MCP
1/16W
R5600
MF-LF
402
1K
4.7K
MF-LF
1/16W
R5612
NOSTUFF

CPU CHKSTOP OR MCP TO NB
CPU_AFN
CPU_PSRONC_PSRO
CPU_TRIGGER_IN
CPU_APSYNCOUT
NB_A_TRIGGER_OUT
SB_CPU_B0_SRESET_L
SB_CPU_B1_SRESET_L
SB_CPU_A1_SRESET_L

PULLUPS FOR SRESET'S FROM SHASTA
NC_EI_CPU_B_TO_NB_SR_N<0..1>
NC_EI_CPU_B_TO_NB_AD<0..43>
NC_EI_NB_TO_CPU_B_SR_P<0..1>
NC_EI_NB_TO_CPU_B_AD<0..43>
NC_EI_NB_TO_CPU_B_CLK_P
R5643
NOSTUFF

SYNC_MASTER=FINO-M23
CPU_ALIASES & MISC
www.vinafix.vn

SMOOTH OUTPUT
R5641
5K
1/16W
R5640
IS OPTIONAL

SOURCE LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT
SOURCE LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT
SRCOM_VCORE_R
VCC
VSSOP
1/16W
MF-LF
1/16W
MF-LF

TURN-OFF VCORE < 0.77 V
Q63: SEE P.28 FOR MORE DECOUPLING CAPS FOR THESE PINS.
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MEMORY ADDR BRANCHING
ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A
### KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

<table>
<thead>
<tr>
<th>COL_NAME</th>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>DIFFERENTIAL_PAIR</th>
<th>NET_PHYSICAL_TYPE</th>
<th>NET_PARTITION_TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

<table>
<thead>
<tr>
<th>COL_NAME</th>
<th>COL_LINE_WIDTH</th>
<th>COL_WIDTH_MUL</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

PLACE CLOSE TO SHASTA
PCI Devices implemented on this page:

- PCI_CLK33M_USB2 (33MHz PCI clock)

Power aliases required by this page:

CLOCKS = PCI_CLK33M_USB2

DIFFERENTIAL_PAIR
ELECTRICAL_CONSTRAINT_SET NET_SPACING_TYPE = PCI_USB2_RESET_L

SYS_PME_L

RC250, RC251 & RPC203 REQUIRED TO

1/16W

47
5%

SM-LF

RC216

MF-LF

402

1/16W

47
21
5%

SM-LF

7
1/16W

47
5%

PPVIO_PCI_USB2

Preliminary

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PPV3_RUN

4.7K

1%
SATA data pairs is 100 ohms.

NOTE: Target differential impedance for Primary Max Sep: 0.23mm inner,
Length Tolerance: 1.27mm

BOM options provided by this page:

- PP1V2_PWRON_DISK

PLACE DATA TERMINATION RESISTORS NEAR JC901 CONNECTOR

AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
SATA PINS WERE REMAPPED FOR BETTER ROUTING AROUND SATA CONNECTOR.
DATA FROM JCAPS TO JC901

DATA FROM SHASTA U2300 TO JCAPS

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A NICE SHAPE
FOR PP1V2, SATA_VDD AND THEN HECK DOWN TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127 ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC2000 CHANGED TO 15500240 (600 Ohm, 0.2 Ohm DCR, 1A)
PREVIOUS WAS 15500231 (600 Ohm, 0.6 Ohm DCR, 0.2A)
PER TDK TURIN AMERICA PN: MT2122601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.2V TO 1.3V AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL HELP MITIGATE THE LOSS ACROSS THE Q1306 FET.

S1322601.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901_PP5V_PATA NET.

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SCALE

D

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EXTRA CONSTRAINTS TO SUPPLEMENT THE MISSING NET PHYSICAL FROM EARLIER PAGE

<table>
<thead>
<tr>
<th>NET_PHYSICAL_TYPE</th>
<th>ENET_MDI_N&lt;3&gt;</th>
<th>ENET_MDI_P&lt;3&gt;</th>
<th>ENET_MDI_N&lt;2&gt;</th>
<th>ENET_MDI_P&lt;2&gt;</th>
<th>ENET_MDI_N&lt;1&gt;</th>
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PLACE THESE PARTS NEAR VESTA

ENET TERMINATION

Spare GND vias for layer traversals during routing
NOTE: Target differential impedance for Line To Line: 0.50mm

Signal aliases required by this page:

- USB2 data pairs is 90 ohms.