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*Pages where master page is in a different schematic*
DATE | DESCRIPTION
---|---
11/20/03 | DSU1 RELEASE (REV 09)
10/19/03 | CHECKIN 12005
10/18/03 | CHECKIN 12004
10/17/03 | NO_TEST, FUNC_TEST UPDATES
10/16/03 | 11/17/03
10/15/03 | RELEASE REV 12
10/14/03 | RELEASE REV 11
10/13/03 | NO_TEST UPDATES
10/12/03 | UPDATED POWER SEQUENCING TO MATCH SMU PINOUT 1.4
10/11/03 | ADDED SERIAL SIGNALS TO AIRPORT CARD FOR NEW MARTY CARD
10/10/03 | CHANGED SHASTA P/N TO V1.1
10/09/03 | NEW CONNECTORS FOR MODEM AND PATA
10/08/03 | POWER BUTTON CONNECTOR SYMBOL UPDATED
10/07/03 | CHANGED XW3302 TO LAYER 6 SHORT
10/06/03 | STUFFING CHANGES FOR ETHERNET RESET
10/05/03 | UPDATED CRITICAL LIST
10/04/03 | CHANGE Y5700 TO 4 PIN CRYSTAL
11/20/03 | CHANGED R2700 TO 22OHM AND NOSTUFFED
11/19/03 | CHANGED HALF OF DIMM AND VTT DECOUPLING TO 1UF
11/18/03 | CPU VID SET TO 1.475V
11/17/03 | J1400 CHANGED TO NOSTUFF
11/16/03 | CPU VDD SUPPLY VIACCESS_0-NR_TO_VIACCESS_0-NR SHORTS ADDED
11/15/03 | CPU VDD SUPPLY VIACCESS_0-NR_TO_VIACCESS_0-NR SHORTS ADDED
11/14/03 | CPU VDD SUPPLY VIACCESS_0-NR_TO_VIACCESS_0-NR SHORTS ADDED
11/13/03 | CPU VDD SUPPLY VIACCESS_0-NR_TO_VIACCESS_0-NR SHORTS ADDED
11/12/03 | CPU VDD SUPPLY VIACCESS_0-NR_TO_VIACCESS_0-NR SHORTS ADDED
11/11/03 | CPU VDD SUPPLY VIACCESS_0-NR_TO_VIACCESS_0-NR SHORTS ADDED
11/10/03 | MASTER PAGE SYNC
11/09/03 | MASTER PAGE SYNC
11/08/03 | MASTER PAGE SYNC
11/07/03 | MASTER PAGE SYNC
11/06/03 | MASTER PAGE SYNC
11/05/03 | MASTER PAGE SYNC
11/04/03 | MASTER PAGE SYNC
11/03/03 | MAIN PROTO RELEASE (REV 10)
11/02/03 | CHECKIN 09002
11/01/03 | TERMINATION FOR CPU CLOCK NOW TRACKS PP1V2_EI_CPU RAIL
10/31/03 | TERMINATION FOR CPU CLOCK NOW TRACKS PP1V2_EI_CPU RAIL
10/30/03 | TERMINATION FOR VSP CLOCK NOW TRACKS PP1V2_HT RAIL
10/29/03 | CHANGED ALL 4 NB AVDDS TO PP1V5_PWRON_NB_AVDD RAIL
10/28/03 | EMI-SPRING ADDED AND TIED TO GND
10/27/03 | NEW LARGER CAP FOR VTT VREG. C4609 CHANGED TO 128S0022. C4608 NOSTUFFED
10/26/03 | ADDED 4 SMT NUTS
10/25/03 | REPINNED J9240 BLUETOOTH CONNECTOR
10/24/03 | BOM OPTIONS AND SCHEMATIC CLEANUP TO AGP (BUSY, STOP, TYPEDET, GCDET)
10/23/03 | ADDED MORE POWER AND GROUND SHORTS FOR AUDIO
10/22/03 | MASTER PAGE SYNC
10/21/03 | ALIASED PP5V_AUDIO TO PP5V_RUN RAIL
10/20/03 | CPU POWER SUPPLY FETS - VISHAY USED ON SAMSUNG BOMS AND ON SEMI ON HYNIX BOMS
10/19/03 | INPUT AND OUTPUT CERM CAPS MARKED AS CRITICAL
10/18/03 | CHANGED INPUT CAPS TO 124-0323
10/17/03 | NEW LARGER CAP FOR VTT VREG. C4609 CHANGED TO 128S0022. C4608 NOSTUFFED
10/16/03 | CPU VID SET TO 1.475V
10/15/03 | MASTER PAGE SYNC
10/14/03 | MASTER PAGE SYNC
10/13/03 | MASTER PAGE SYNC
10/12/03 | MASTER PAGE SYNC
10/11/03 | MASTER PAGE SYNC
10/10/03 | MASTER PAGE SYNC
10/09/03 | MASTER PAGE SYNC
2.5V VOLTAGE REGULATOR

NOTE:
- Set output+2.62V EVB FRAME BUFFER
- Use Jumper (J901) or J902 2.62VDC
- Peak current of total rails
  - 12.68A with DIMM termination
  - 9.24A without DIMM termination

VOUT=VREF*(R903+R905)/R905=2.62VDC

IRU3037CS VREF=1.25VDC

12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

NOTE:
- Min line width=25MIL
- Voltage=2.5V
- Min neck width=10MIL

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FAN 2 - Q37 STYLE SYSTEM FAN CONTROL CIRCUIT
NOTE:
SET OUTPUT=1.5VDC FOR U3LITE CORE
VOUT=VREF*(R2203+R2205)/R2205=1.5VDC
7.73A of PEAK CURRENT DRAW ON PCORE_NB
VOUT=VREF*(R2203+R2205)/R2205=1.5VDC
7.73A of PEAK CURRENT DRAW ON PCORE_NB
VOUT=VREF*(R2203+R2205)/R2205=1.5VDC
7.73A of PEAK CURRENT DRAW ON PCORE_NB
Power aliases required by this page:
- _PP2V5_PWRON_SB (2.5V)
- _PP3V3_PWRON_SB (3.3V)
- _PPPCI32_PWRON_SB (5V)
- _PPPCI64_PWRON_SB (5V)

Signal aliases required by this page:
- _CCVRAD_PGOOD
- _CCVRAD_RUN
- _CCVRAD_PAON
- _CCVRAD_PAMB

Power Sequencing:
- (NONE)
- _PPPCI32_PWRON_SB to _PPPCI64_PWRON_SB (5V)
- _PP2V5_PWRON_SB
- _PP3V3_PWRON_SB
- _PPPCI32_PWRON_SB (5V or 3.3V)
- _PPPCI64_PWRON_SB (5V or 3.3V)

Power aliases required by this page:
- _CCVRAD_PGOOD
- _CCVRAD_RUN

Signal aliases required by this page:
- _CCVRAD_PAON
- _CCVRAD_PAMB
- _CCVRAD_PAMB

neoBorg Implementation
Master power enable signal (from PMU)
connects directly to SBVCORE supply
when ready, which acts as the power enable signal for the rest of the neoBorg components.
PROCESSOR PULL-UPS AND -DOWNS
NOTE: U4700 PIN 4 IS LOW ACTIVE.

RAM_VTT

SPAK-5

NE57811

603

10K0.1UF

603

16V10%

1/16W

MF

402

NOSTUFF

1206

6.3V

20%

10UF

CERM

7343

VOLTAGE=1.25V

PP1V25_RAM_VTT

MIN_LINE_WIDTH=25MIL

MIN_NECK_WIDTH=10MIL

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LEVEL SHIFTER FOR U3LITE & NVIDIA AGP BUS.
AGP BUSY AND STOP NOT USED IN THIS DESIGN
NOTE: CONNECT VR5001 PIN 9 TO GND PLANE.

SC4215 VREF=0.8VDC
VOUT=VREF*(R5004+R5005)/R5007=1.60(OR 1.40) VDC

PEAK CURRENT OF TOTAL RAILS
1.40VDC
SET OUTPUT=1.40V FOR NV34
1.60VDC
SET OUTPUT=1.60V FOR NV18B

IRU3037CS VREF=1.25VDC
VOUT=VREF*(R5004+R5005)/R5007=1.60(OR 1.40) VDC

PEAK CURRENT OF TOTAL RAILS
0.95A
<table>
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<th>DESCRIPTION</th>
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<td>RES, 1.5K OHM, 1%, 1/16W, 0402</td>
<td>R5807</td>
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<tr>
<td></td>
<td>IFP0AVCC</td>
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<td>MIN_NECK_WIDTH = 10MIL</td>
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SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2
NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.

Signal aliases required by this page:

- PCI_AD<0> to intercept ROM chip select
- Allows ROM override module

Power aliases required by this page:

- _PP3V3_PCI

Page Notes

BOM options provided by this page:

- (NONE)
NOTE: This USB2 implementation supports AD27 (Slot "G") - USB2 (0x1033/0x0035)

_PCI_CLK33M_USB2 (33MHz PCI clock) D3cold.

PCI Devices implemented on this page:
(NONE)

Signal aliases required by this page:

ELECTRICAL_CONSTRAINT_SET

Page Notes

Power aliases required by this page:

信号 aliases required by this page:

Non-aliases provided by these pages:

-PCI_CLK33M_USB2

Items placed on this page:

-Note that "F" = 0x682 (e.g. 0x682/0x7876)

Note: Here this representation supports

0.1uF

1/16W

10V20%

VDD_PCI

CRITICAL

FBGA

VDD_PCI

C8

H3

CRITICAL

M4

FBGA

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NOTE: Target differential impedance for:

- Secondary Length: 500 mils
- Primary Max Sep: 10 mils outer
- Length Tolerance: 50 mils
- Line To Line: 15 mils

BOM options provided by this page:

- (NONE)
- SATA_VDD x 5

Signal aliases required by this page:

- UATA_DEV_R
- UATA_INTRQ
- UATA_DEV_R_C
- UATA_DSTROBE
- UATA_HOST_R
- UATA_RESET_L
- UATA_DD7
- UATA_DD<7>
- UATA_DD
- UATA_DD<15..8>
- UATA_HOST
- UATA_HSTROBE
- UATA_HOST
- UATA_CS1_L
- SATA_RXD1
- SATA_RXD1_CSATA
- SATA_RXD_P1_C
- SATASATA_TXD2
- SATA_TXD_P2
- SATASATA_RXD2
- SATA_RXD_P2_CSATA_RXD2_C
- SATASATA_RXD2
- SATA_RXD_P2_C
- SATASATA_RXD2
- SATA_RXD_P1_C
- SATASATA_RXD2
- SATA_RXD1_CSATA
- SATASATA_RXD2
- SATA_RXD_P2_C
- SATASATA_TXD2
- SATA_TXD_N2SATA_TXD2
- SATASATA_TXD2
- SATA_TXD_N2_CSATA_RXD2_C
- SATASATA_RXD2
- SATA_RXD_N2_C
- SATA_RXD_P2_C

Page Notes

- NET_SPACING_TYPE: SATA
- Length Tolerance: 50 mils
- Primary Max Sep: 10 mils outer
- Secondary Max Sep: 50 mils
- Secondary Length: 50 mils

All coupling required for any SATA pair used.

- Recommended 0.1uF cap placed 0cm to 1cm away.

CAPS provided by device page

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ADD DUAL LAYOUT SUPPORT

NOTE: PLACE R3128, R3100, RP 3101 CLOSE TO PHY

NET_SPACING_TYPE DIFFERENTIALPAIR

NET_SPACING_TYPE=10 MIL

TRANSC_BCM5221

REGAVDD

REGDVDD

DVDD2

AVDD1

OVDD1

TRANSC_BCM5221

SD-

FDX

SPDLED/JTAG_TMS*

LNKLED/JTAG_TDI*

ANEN/JTAG_TRST

REGAVDD REGDVDD

MIN_NECK_WIDTH=10MIL

CLEAR OUT ALL PLANES BETWEEN MIDDLE

VIA COUNT, AND SHORT IF POSSIBLE

ROUTE RD OVER GROUND PLANE (TOP LAYER) ONLY

ROUTE TD OVER 2.5V PLANE (BOTTOM LAYER) ONLY

OF TRANSFORMER AND CONNECTOR

PD NCH

3. RX TERMINATION - LOCATE NEAR PHY

2. TX TERMINATION - LOCATE NEAR PHY

1. TRANSMIT - LOCATE NEAR PHY

THEORY
development
USB2 data pairs is 90 ohms.

Secondary Length: 500 mils
Secondary Max Sep: 100 mils
Length Tolerance: 50 mils

BOM options provided by this page:

Power aliases required by this page:

Signal aliases required by this page:

- _PP3V3_PWRON_USB

Net Spacing Type: USB2

15 MIL SPACING
USB2_NEC_XTAL NEC_CLK30M_XT1
USB2_USB2_4 USB2_4 USB2_N<4>
USB2_USB2_3 USB2_USB2_3 USB2_N<3>
USB2_USB2_1 USB2_USB2_1 USB2_N<1>
USB2_USB2_0 USB2_USB2_0 USB2_P<0>

NEC_CLK30M_XT2 15 MIL SPACING

1. C9120 CERM 6.3V 20%
2. C9121 0.1uF MF 1/16W 10K
3. C9127 1
4. C9122 0.1uF MF 0.1uF CERM 20%10V
5. C9128 1
6. R9110 CERM 30.0000M
7. Y9145 1 2 1.5K MF 1.5K 402
8. R9140 30.0000M
9. R9135 2 1/16W 4.7 MF 5%
10. C9130 1
11. C9135 1
12. C9136 1
13. P2 10uF MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil
14. R9145 5%
15. RSDM5 RSDM4 RSDM2 RSDM1 RSDD5 RSDD4 RSDD2 RSDD1
16. RSDP5 RSDP4 RSDP2 RSDP1 RSDP0
17. RSDM5 RSDM4 RSDM2 RSDM1 RSDD5 RSDD4 RSDD2 RSDD1
18. RSDP5 RSDP4 RSDP2 RSDP1 RSDP0
19. Tie to GND at ball N11
20. P12 1
22. N8 A3E2
23. N13 B13 M11
24. N14 H14B14
25. N10 M12 A13A12
26. N14 H14B14
27. N14 H14B14
28. B9 G4 J11F11 A9
29. P12 1
USB controller outputs to indicate control on USB ports 2-4. Rename NOTE: This design does not provide power provide the appropriate constraints USB Host Controller page will this page. It is assumed that the USB pairs are NOT constrained on USB2_PWREN<1> USB2_PWREN<2> USB2_PWREN<3> USB2_PWREN<4>. BOM options provided by this page: terminate unused signals. USB pairs to their appropriate destinations and/or to properly terminate unused signals. USB2_OC<1> USB2_OC<2> USB2_OC<3> USB2_OC<4>.

neoBorg Implementation NOTE: This design does not provide power control on USB ports 2-4. Wires indicated single-pin connections.

External USB Ports

Q37 BlueTooth Connector

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NEED TO PICK A MODEM TO STUFF FOR EVT
AND THE CORRESPONDING STANDOFF
GAIN SETTINGS: +16dB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS