

IM4, 2 - REV B

09/11/06

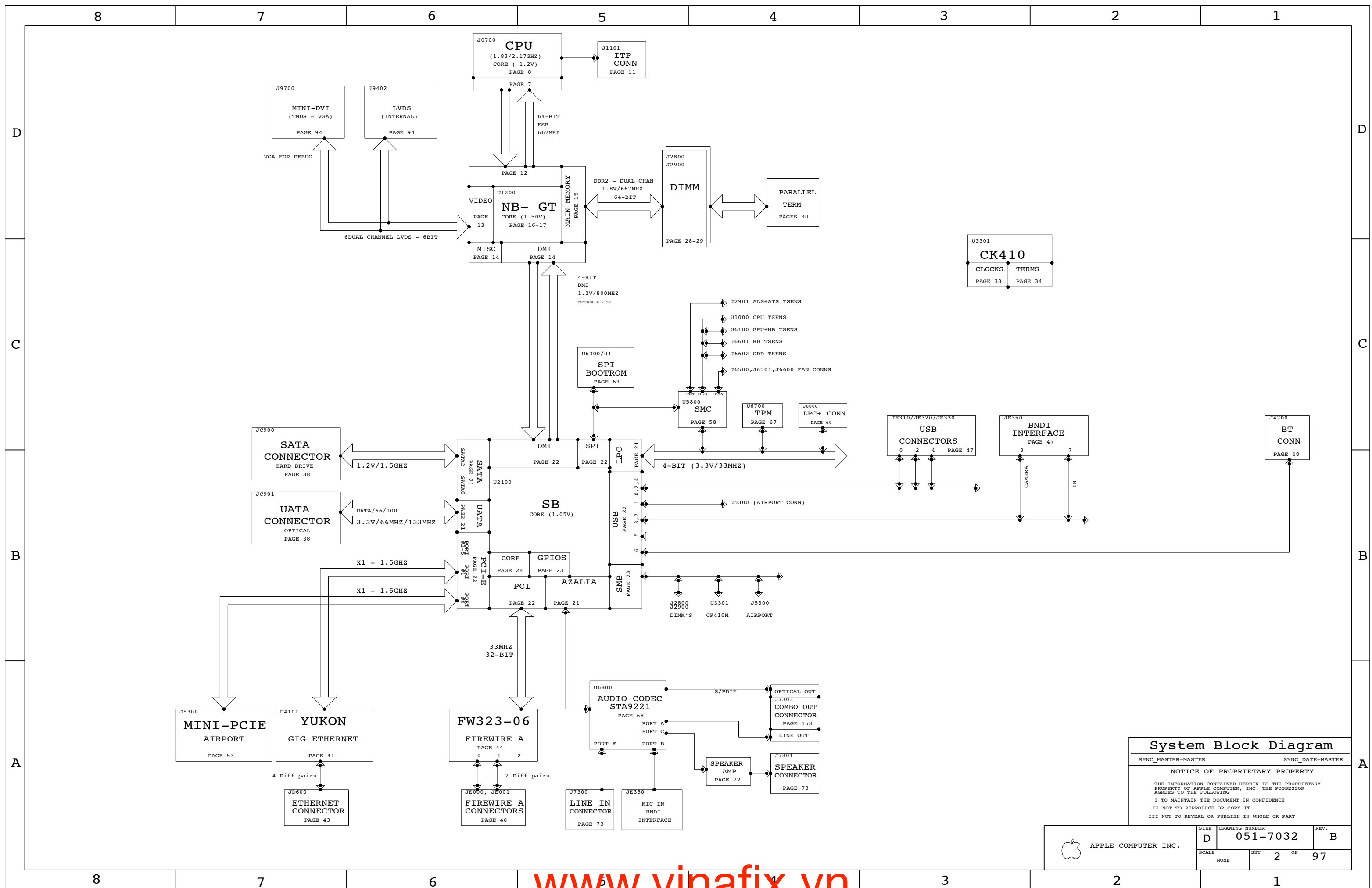
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
B		461143	PRODUCTION RELEASED	09/12/06	06/22/04

PDF	CSA	CONTENTS	SYNC MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER
3	3	Power Block Diagram	MASTER	MASTER
4	4	Table Items	MASTER	MASTER
5	5	FUNC TEST 1 OF 2	MASTER	MASTER
6	6	Power Conn / Alias	MASTER	MASTER
7	7	CPU 1 OF 2-FSB	MASTER	MASTER
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER
9	9	CPU DECAPS & VID<>	MASTER	MASTER
10	10	CPU TEMP SENSOR	MASTER	MASTER
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006
12	12	NB CPU Interface	M1	01/05/2006
13	13	NB PEG / Video Interfaces	M1	01/05/2006
14	14	NB Misc Interfaces	MASTER	MASTER
15	15	NB DDR2 Interfaces	M1	01/05/2006
16	16	NB Power 1	MASTER	MASTER
17	17	NB Power 2	M40	01/05/2006
18	18	NB Grounds	M1	01/05/2006
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)
20	20	NB Config Straps	M1	01/05/2006
21	21	SB: 1 OF 4	M38	01/05/2006
22	22	SB: 2 OF 4	MASTER	MASTER
23	23	SB: 3 OF 4	MASTER	MASTER
24	24	SB: 4 OF 4	M38	01/05/2006
25	25	SB: DECOUPLING	MASTER	MASTER
26	26	SB: MISC	MASTER	MASTER
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER
30	30	Memory Active Termination	MASTER	MASTER
31	31	Memory Vtt Supply	MASTER	MASTER
32	33	CLOCKS	MASTER	MASTER
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER
34	38	Disk Connectors	MASTER	MASTER
35	41	ETHERNET CONTROLLER	MASTER	MASTER
36	42	ETHERNET MISC	MASTER	MASTER
37	43	ETHERNET CONNECTOR	MASTER	MASTER

PDF	CSA	CONTENTS	SYNC MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER
39	45	FW: DECAPS	MASTER	MASTER
40	46	FIREWIRE CONNECTORS	MASTER	MASTER
41	47	USB Device Interfaces	MASTER	MASTER
42	53	AIRPORT CONN	MASTER	MASTER
43	54	PCIE PORT ALIASES	MASTER	MASTER
44	58	SMC	M1	01/05/2006
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)
46	60	LPC+ CONN	M38	12/09/2005
47	61	NB THERMAL	MASTER	MASTER
48	63	SPI BOOTROM	M38	01/05/2006
49	65	Fan 0, 1 & System Temp	MASTER	MASTER
50	66	Fan 2 & HD Temp	MASTER	MASTER
51	67	TPM	M38	01/05/2006
52	68	AUDIO: CODEC	AUDIO	05/12/2006
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER
57	76	CPU & SYSTEM SENSE CIRCUITS	(MASTER)	(MASTER)
58	77	PWR GOOD	(MASTER)	(MASTER)
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)
60	79	1.8V & 1.2V VREG	MASTER	MASTER
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER
62	82	5V DC/DC	MASTER	MASTER
63	83	S0 AND S3 FETS	MASTER	MASTER
64	94	Internal Display Conns	MASTER	MASTER
65	95	EXTERNAL TMDS	MASTER	MASTER
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER
67	97	External Display Conns	MASTER	MASTER

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <p style="text-align: center;"> THIRD ANGLE PROJECTION </p>	<p>METRIC</p>	<p style="text-align: right; font-weight: bold;">Apple Computer Inc.</p> <p style="font-size: x-small;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="text-align: center; font-weight: bold; font-size: large;">SCHEM VALLCO</p> <p style="text-align: right;">DRAWING NUMBER 051-7032 REV. B</p> <p style="text-align: right; font-size: x-small;">SHT 1 OF 97</p>
<p>DRAPFR</p> <p>ENG APPD</p> <p>QA APPD</p> <p>RELEASE</p> <p>MATERIAL/FINISH NOTED AS APPLICABLE</p>	<p>DESIGN CK</p> <p>MFG APPD</p> <p>DESIGNER</p> <p>SCALE</p> <p>SIZE D</p>	



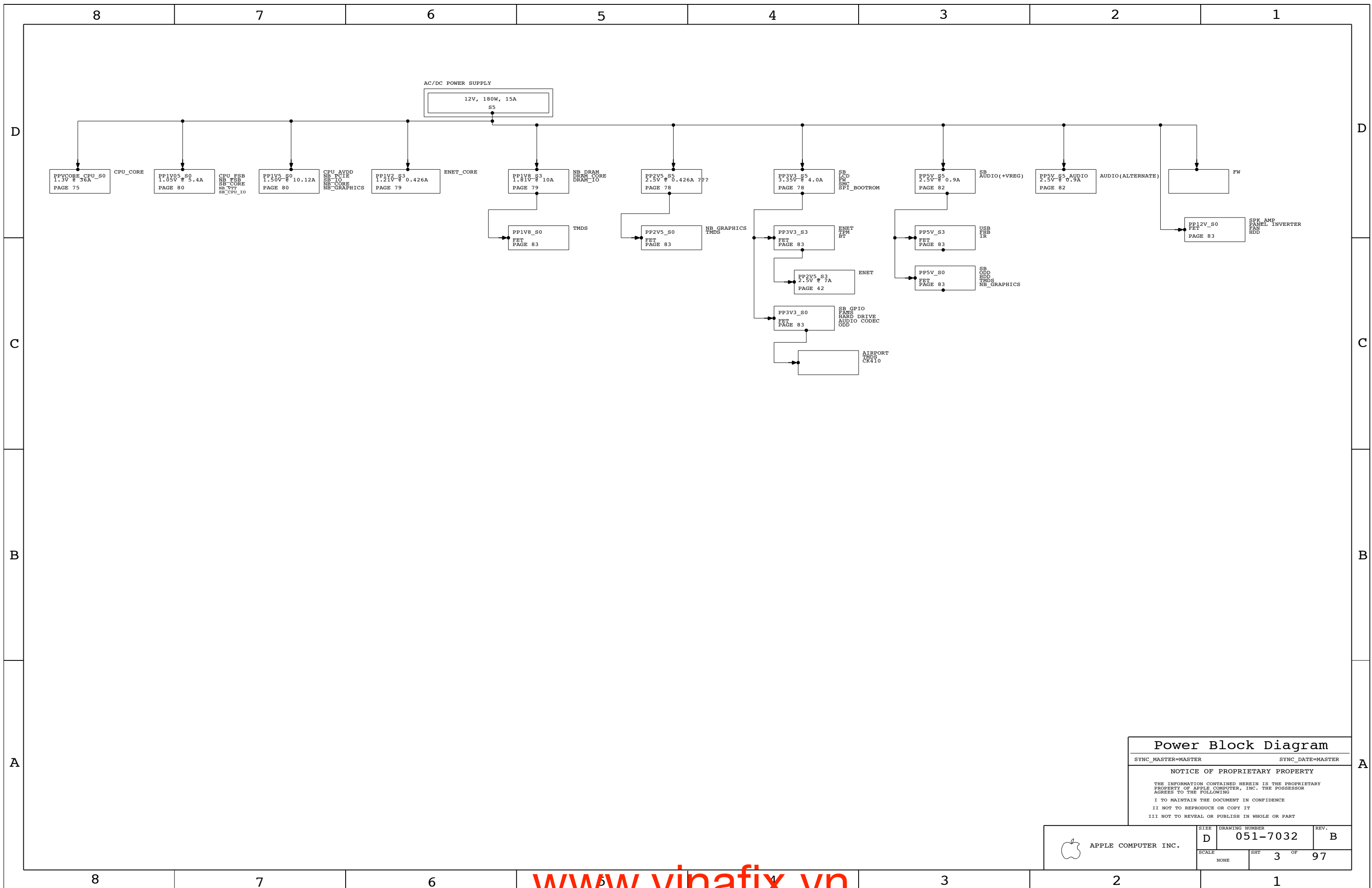
System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	OF	REV.
NONE	2	97	



Power Block Diagram

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	D	051-7032	B
SCALE	SHT	OF	REV.
NONE	3	97	

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3

2

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51180025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
33880298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
338S0270	1	IC,888053,1GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TOFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0021	1	EFI ROM,M50	U6301	CRITICAL	
337S3242	1	M38 CPU (C0)	CPU	CRITICAL	YONAH_1_83

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		L2D601,L2D602,L2D603	
353S1235	353S1465		U7500	CPU VREG, NON-SCREENED PART

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:XOM]	CRITICAL	YONAH_1_83

Table Items

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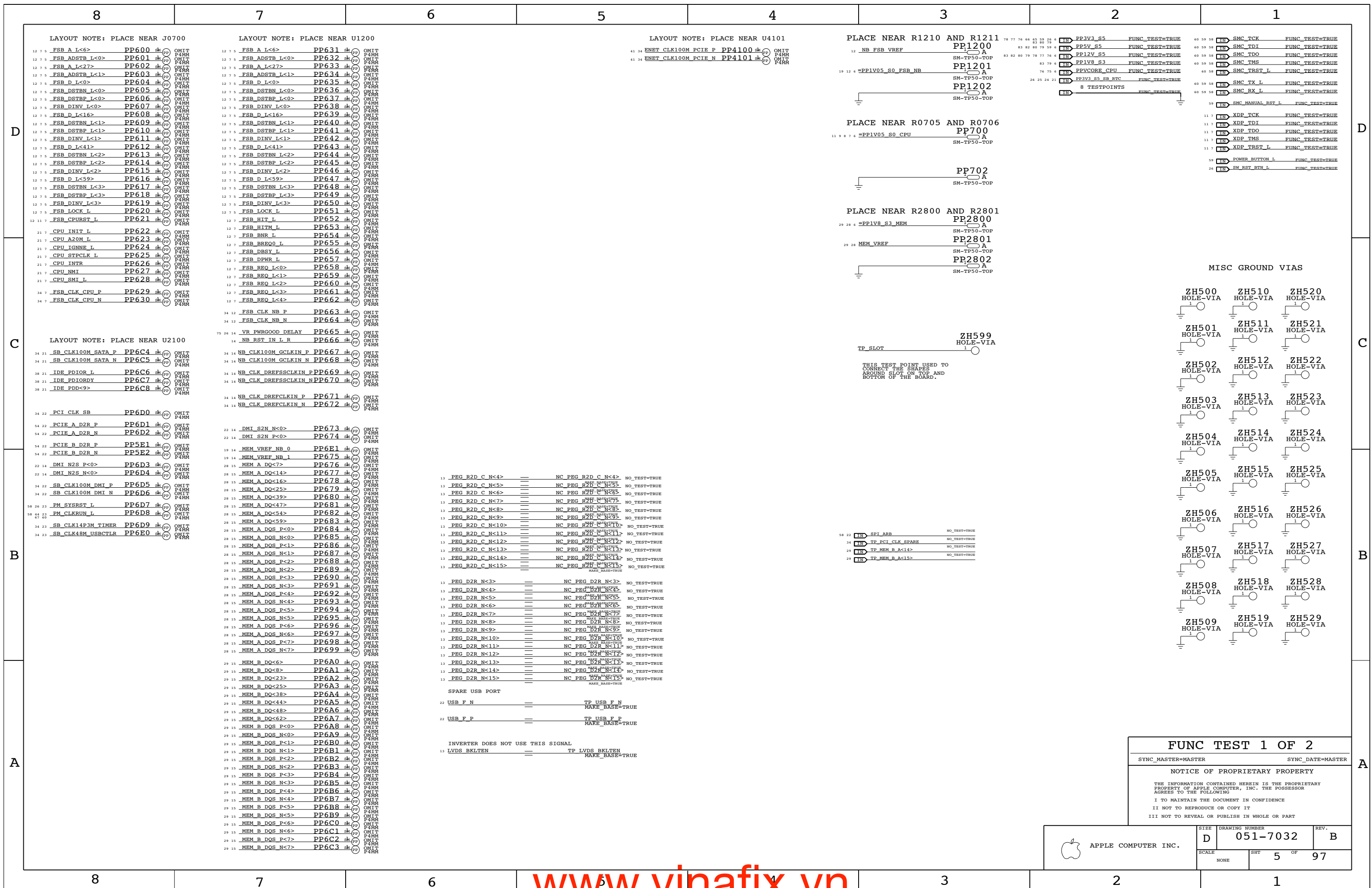
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SCALE	SHT	OF
NONE	4	97



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

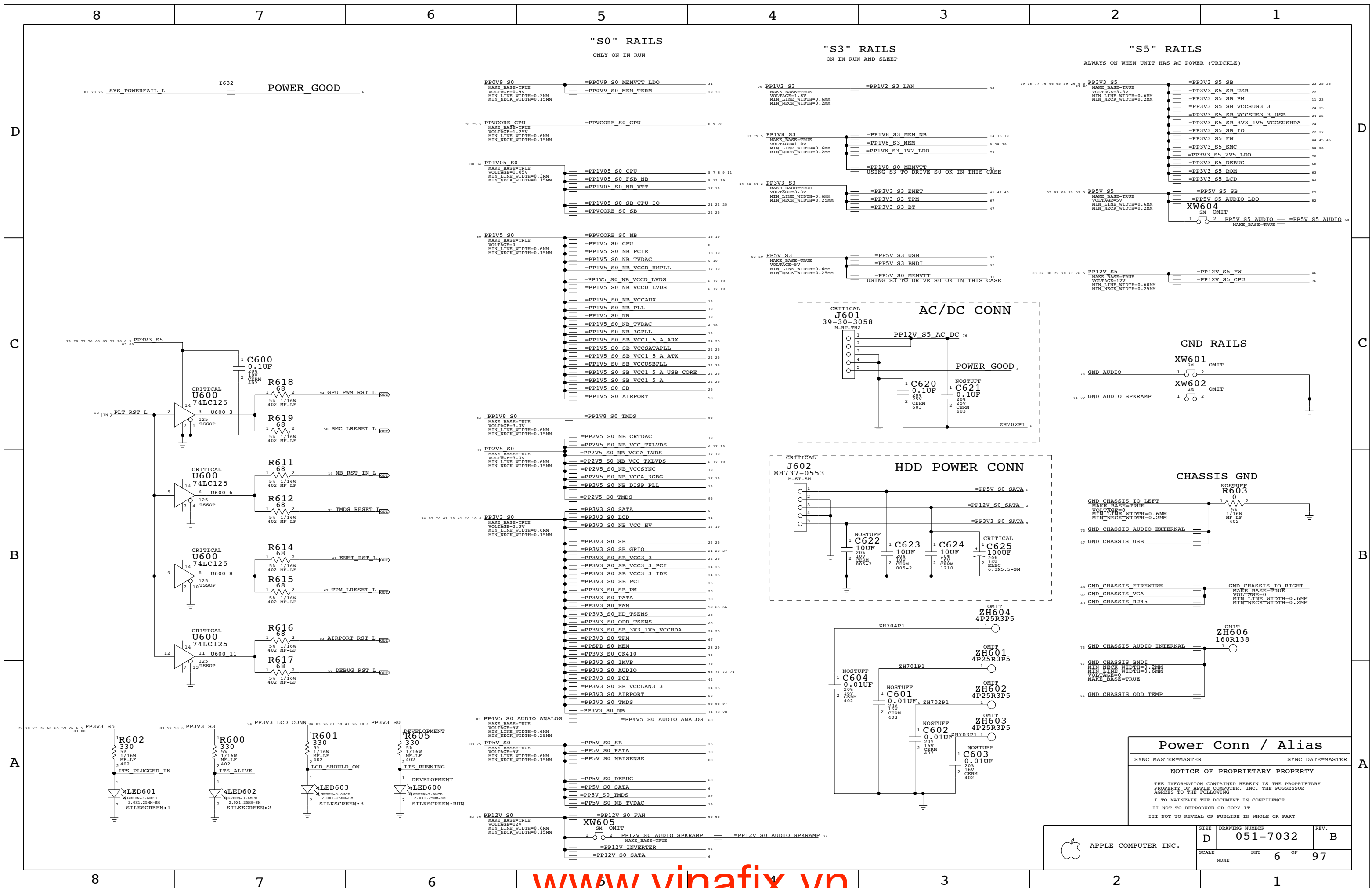
PLACE NEAR R2800 AND R2801

MISC GROUND VIAS

THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

FUNC TEST 1 OF 2
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	SCALE NONE	SHEET 5 OF 97	



"S0" RAILS

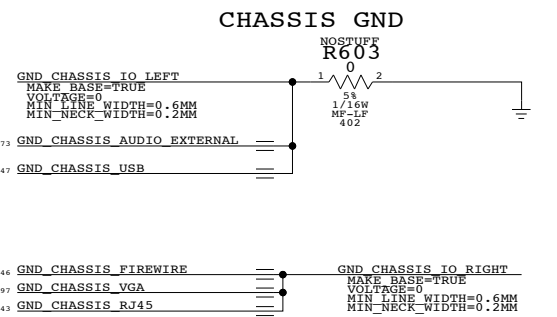
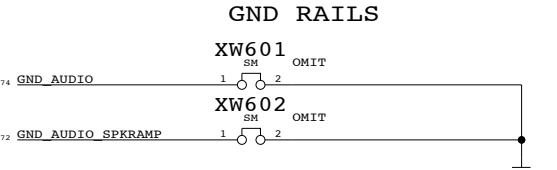
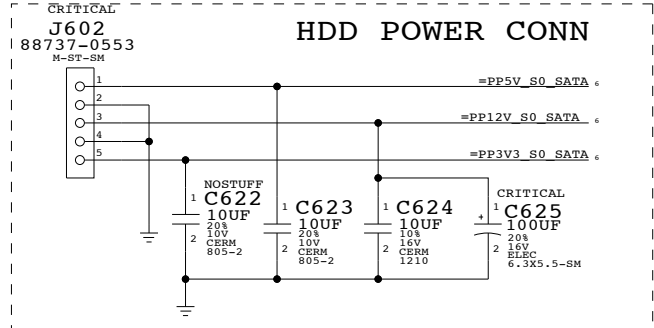
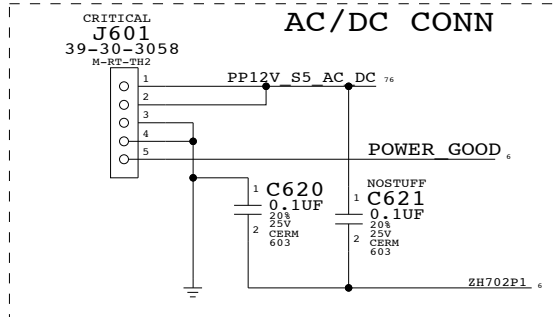
ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

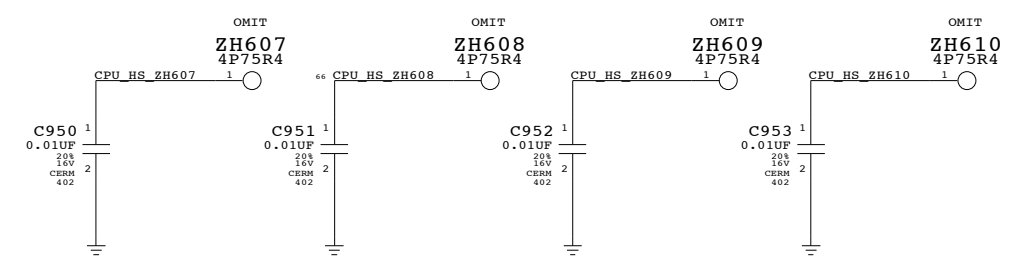
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



Power Conn / Alias	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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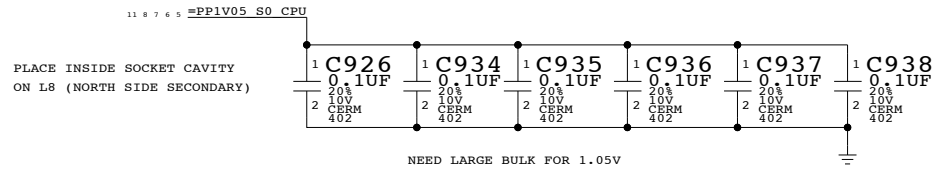
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHT 6 OF 97	

CPU HEATSINK MOUNTING HOLES



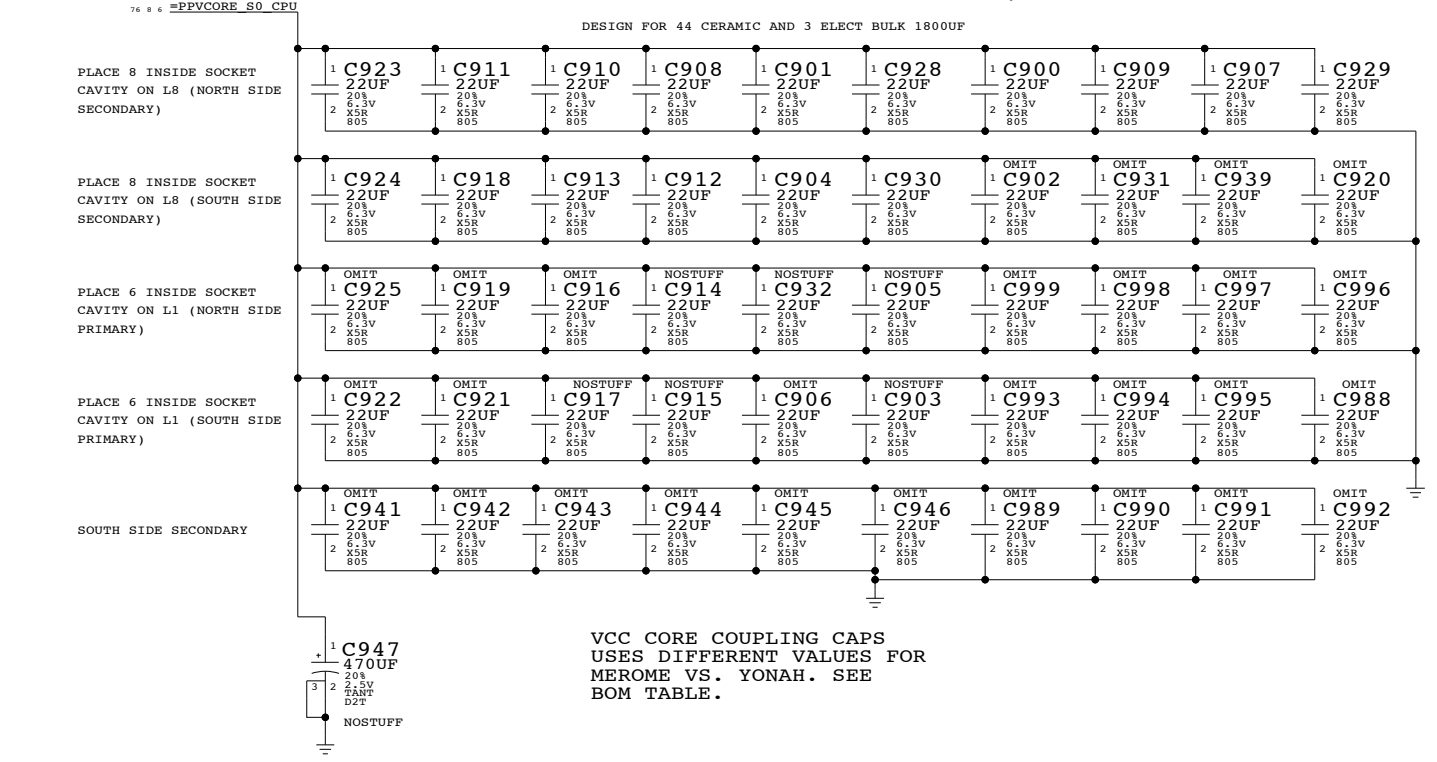
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH

CPU DECAPS & VID<>

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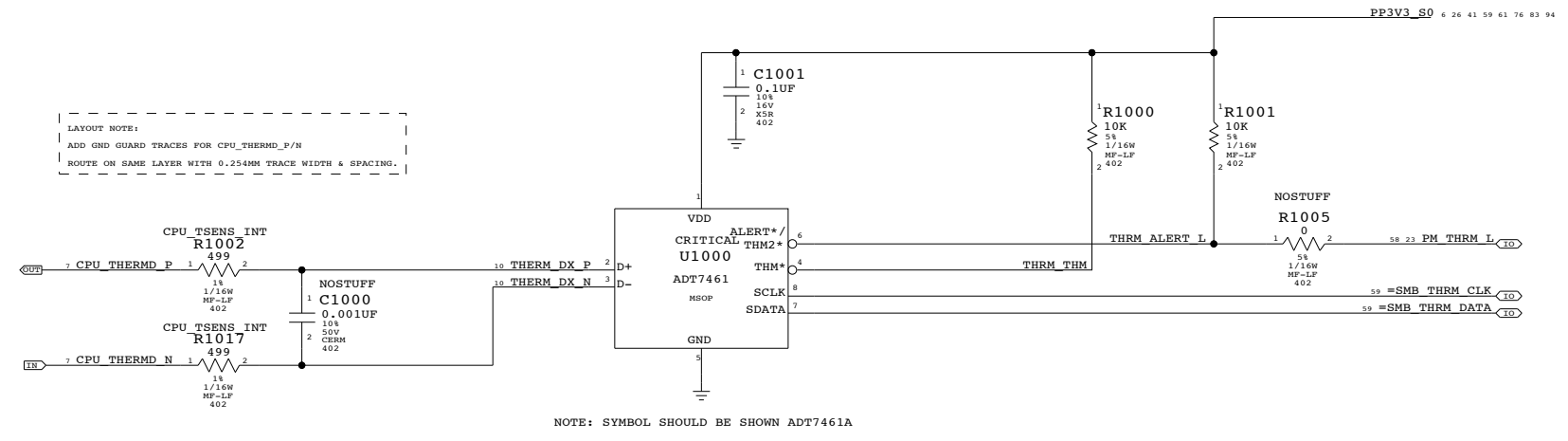
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	D	051-7032	B
SCALE	SHT	9 OF	97
NONE			

CPU THERMAL SENSOR

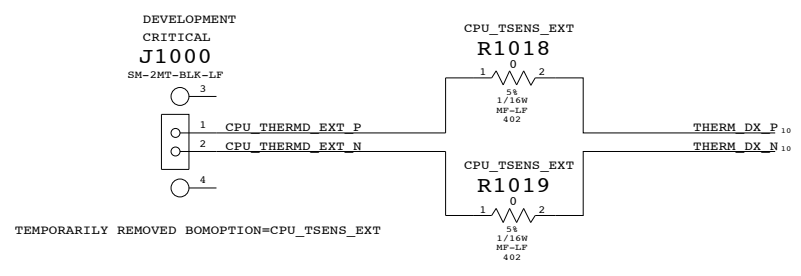
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.

NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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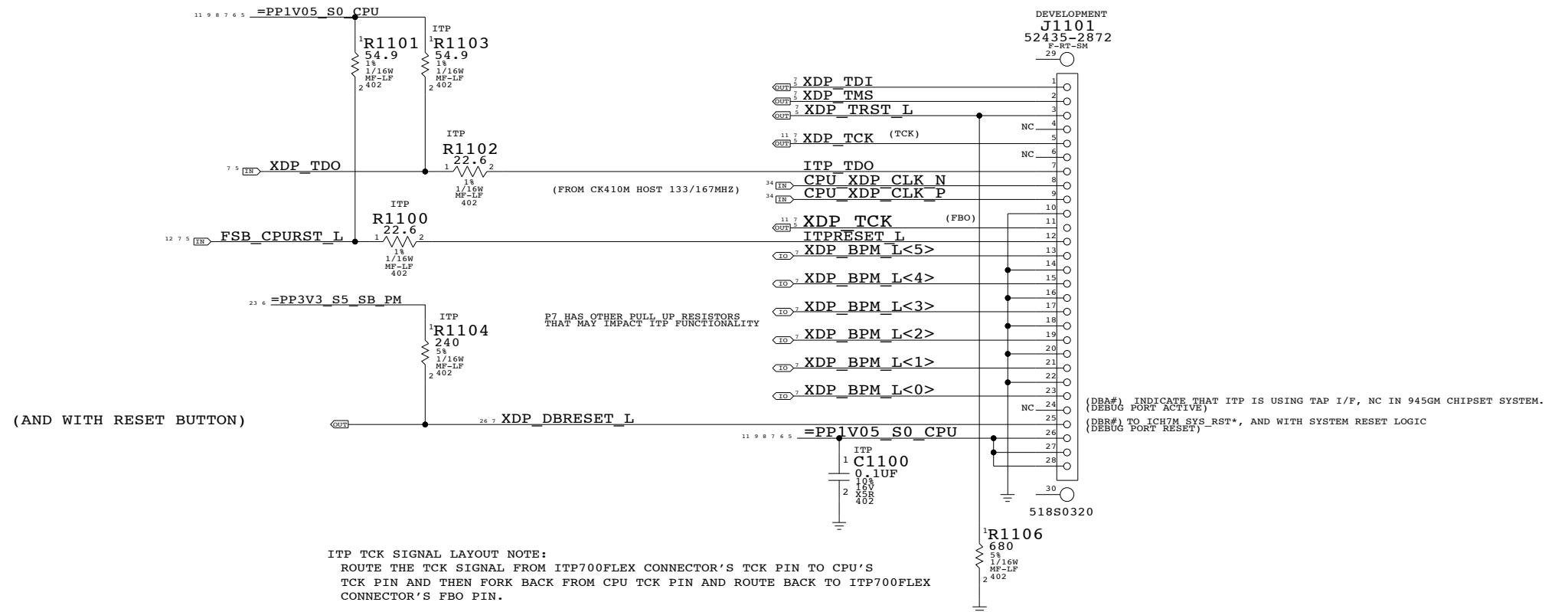
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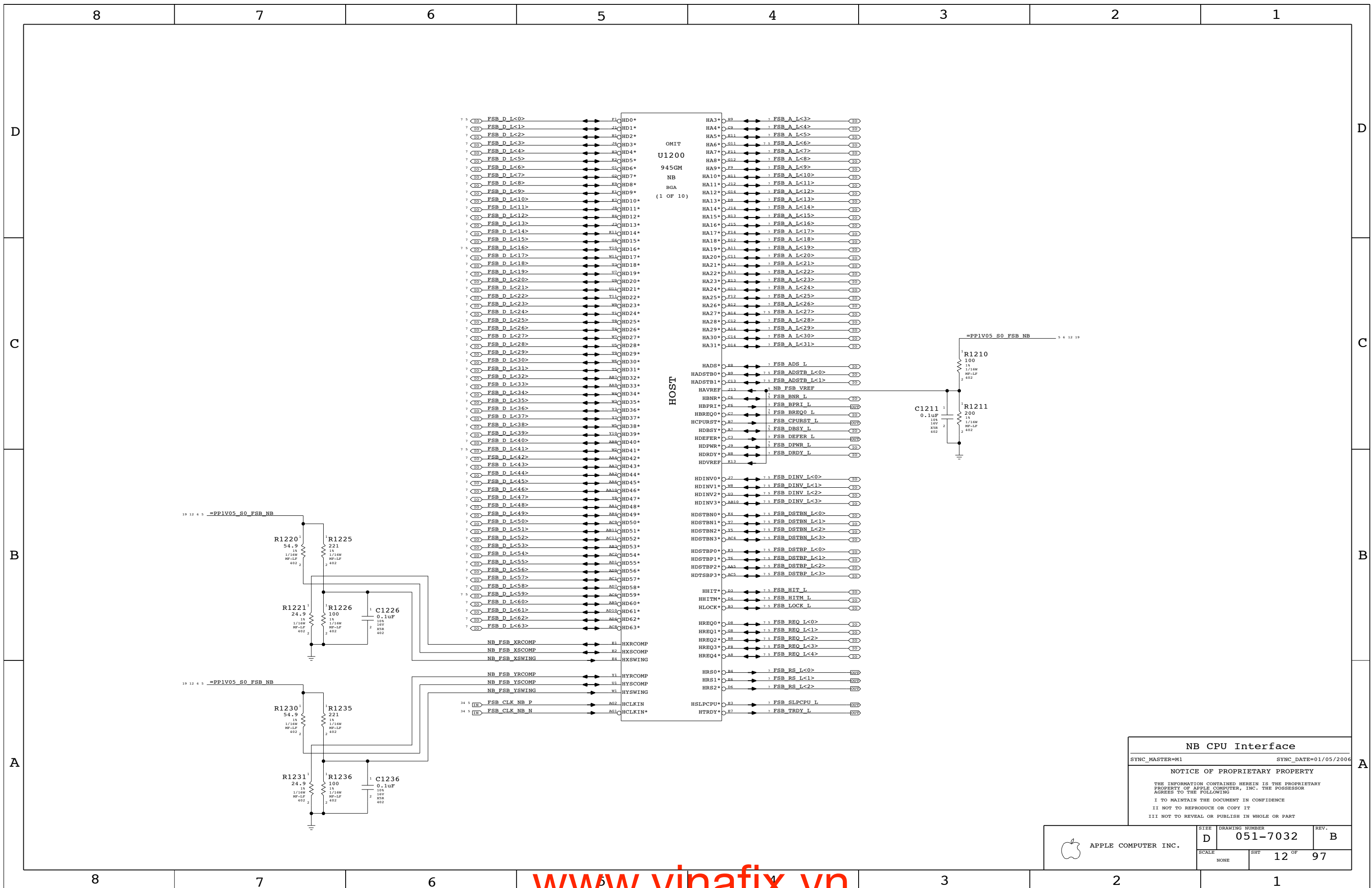
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

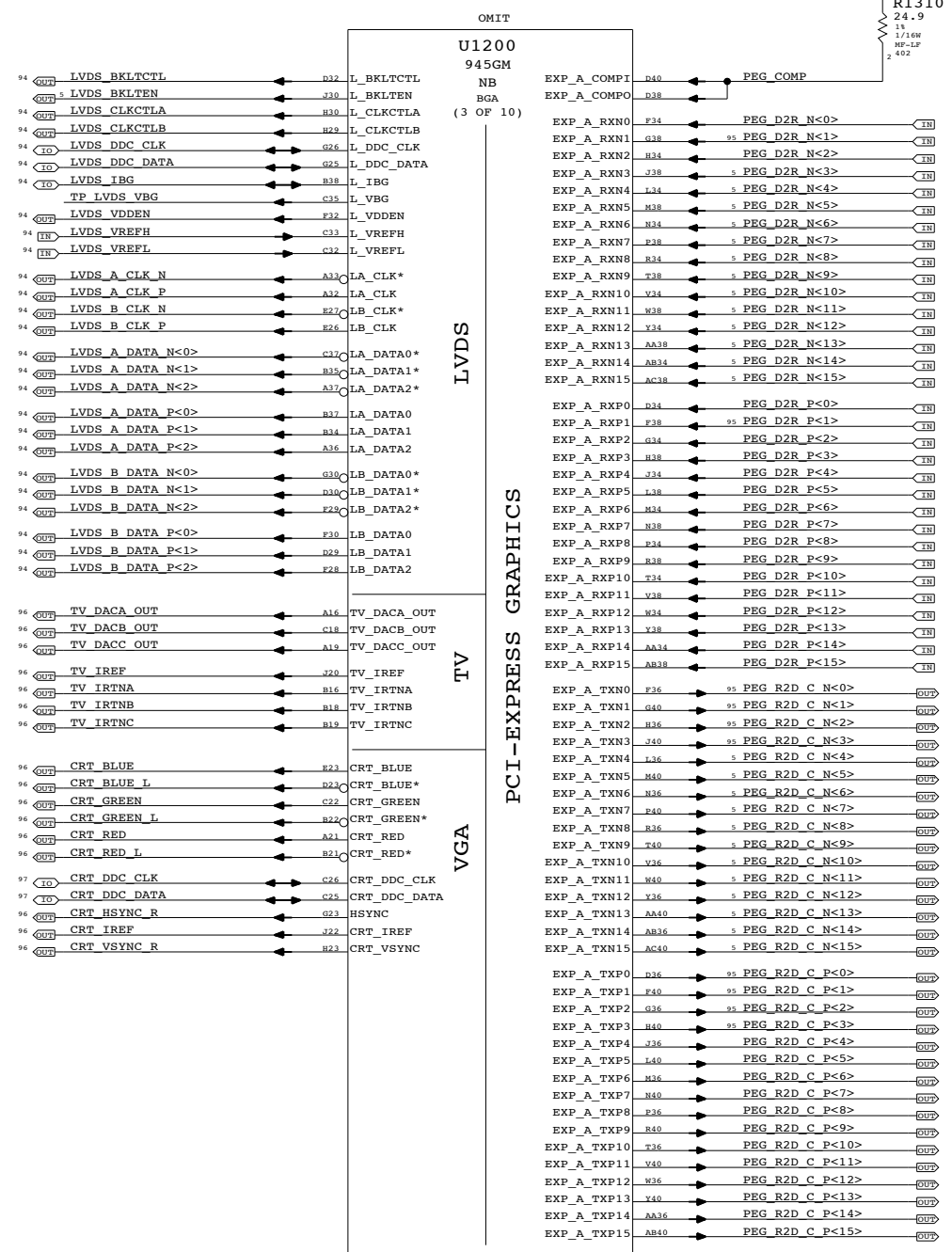
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

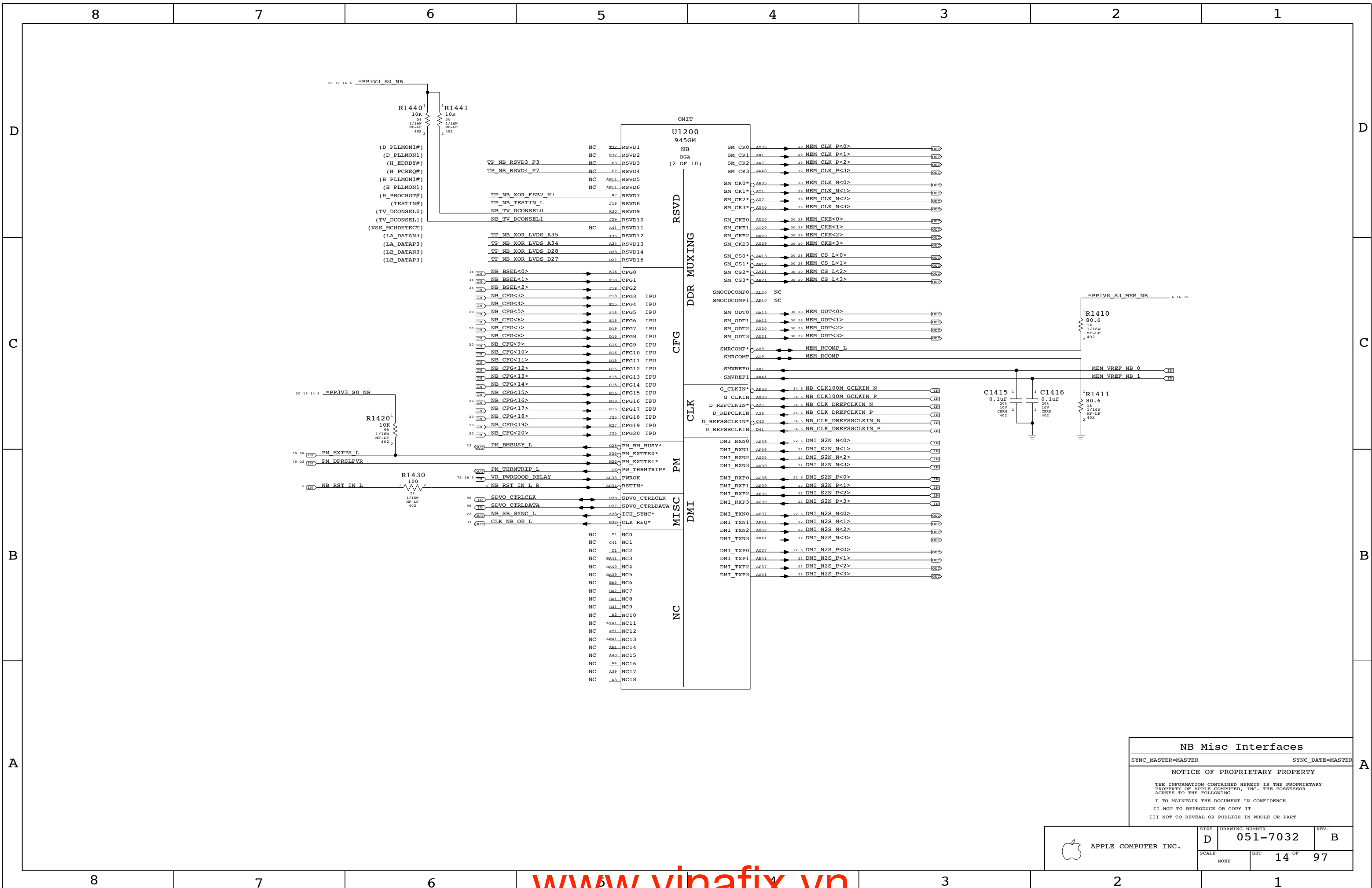
SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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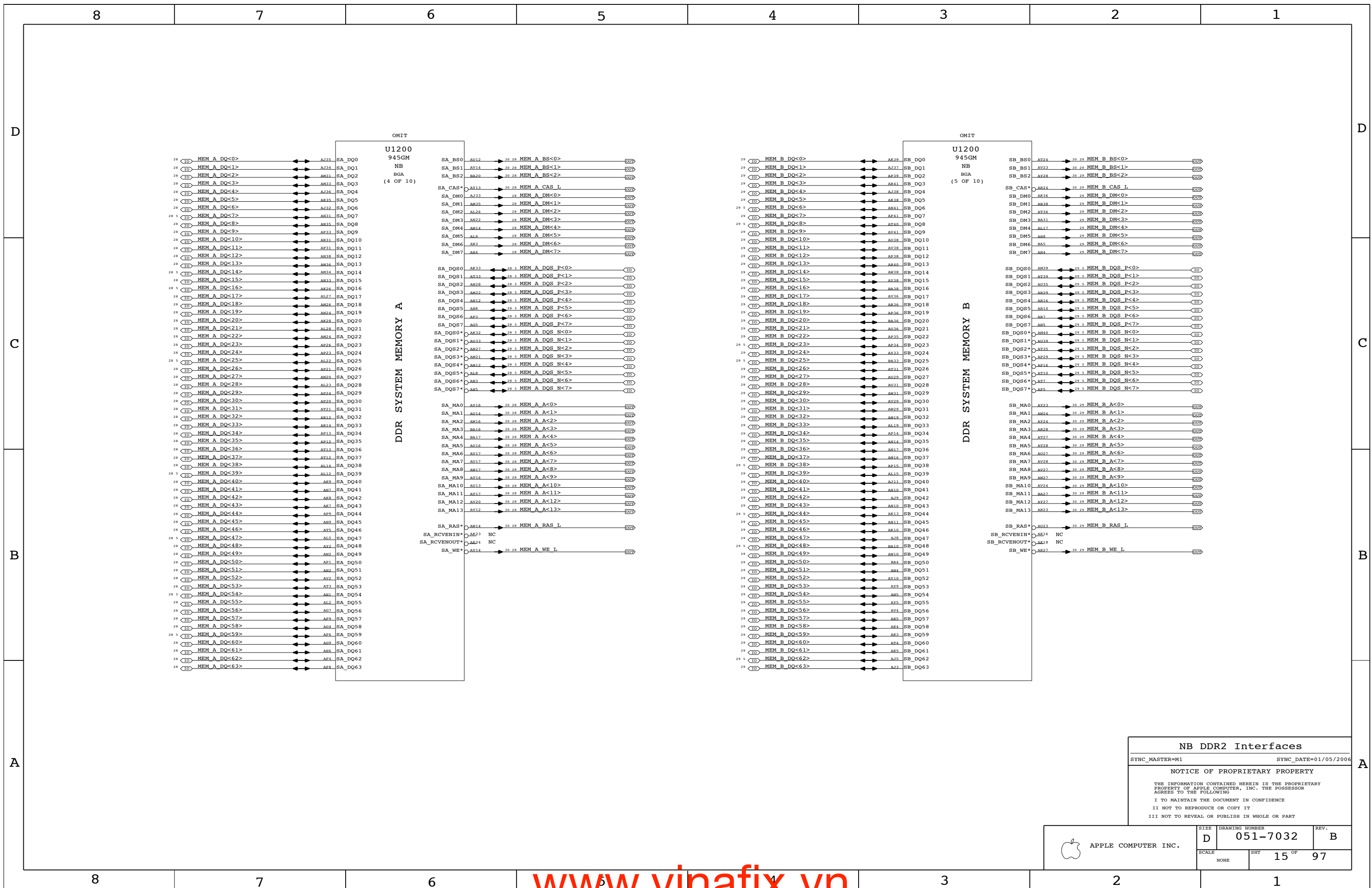
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SCALE	SHT	OF	REV.
NONE	14	97	



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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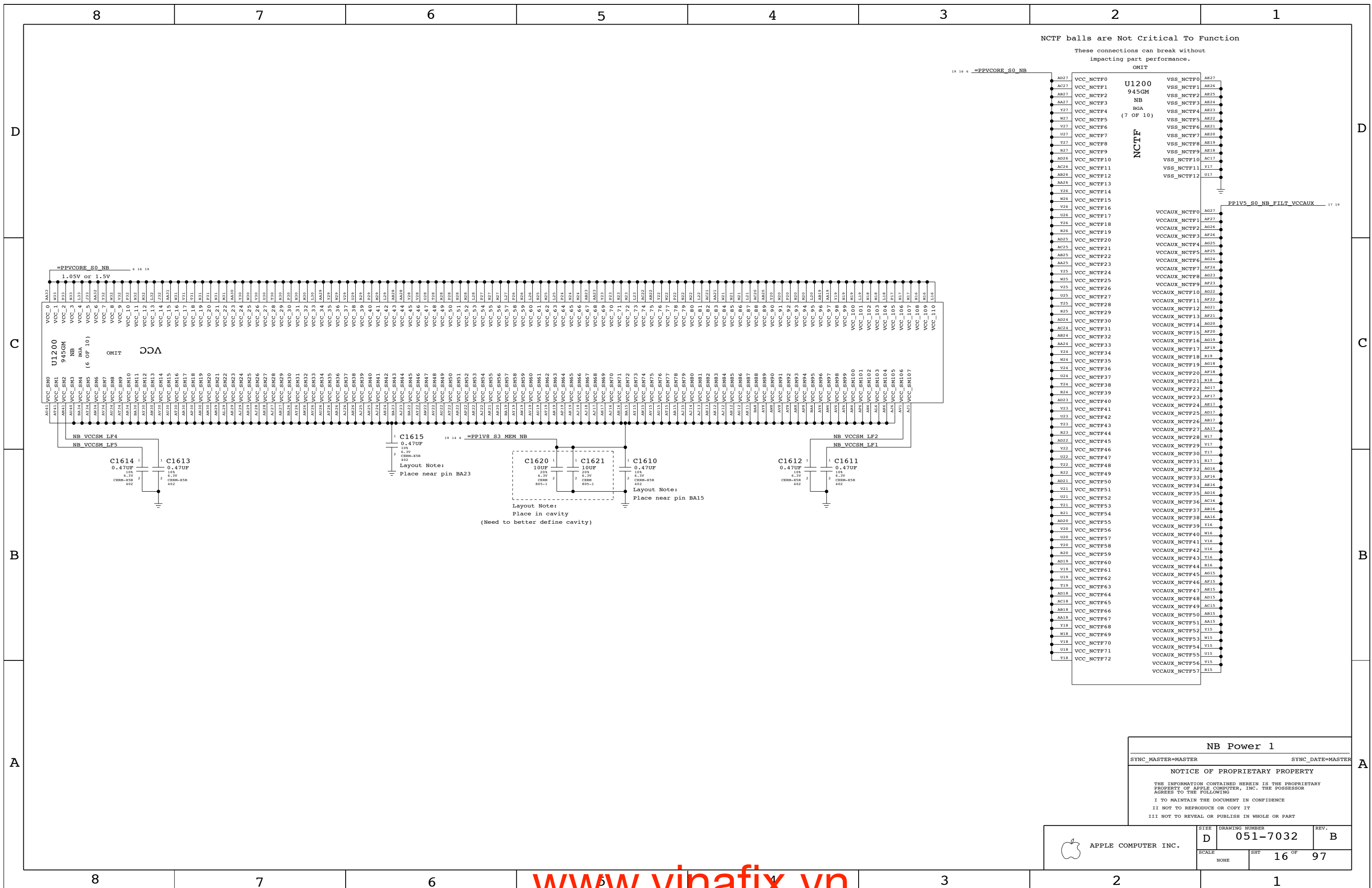
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	D	051-7032	B
SCALE	SHT	15 OF 97	
NONE			



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)

NCTF

VCC

VSS

VCCAUX

VCCSM

MEM

LP

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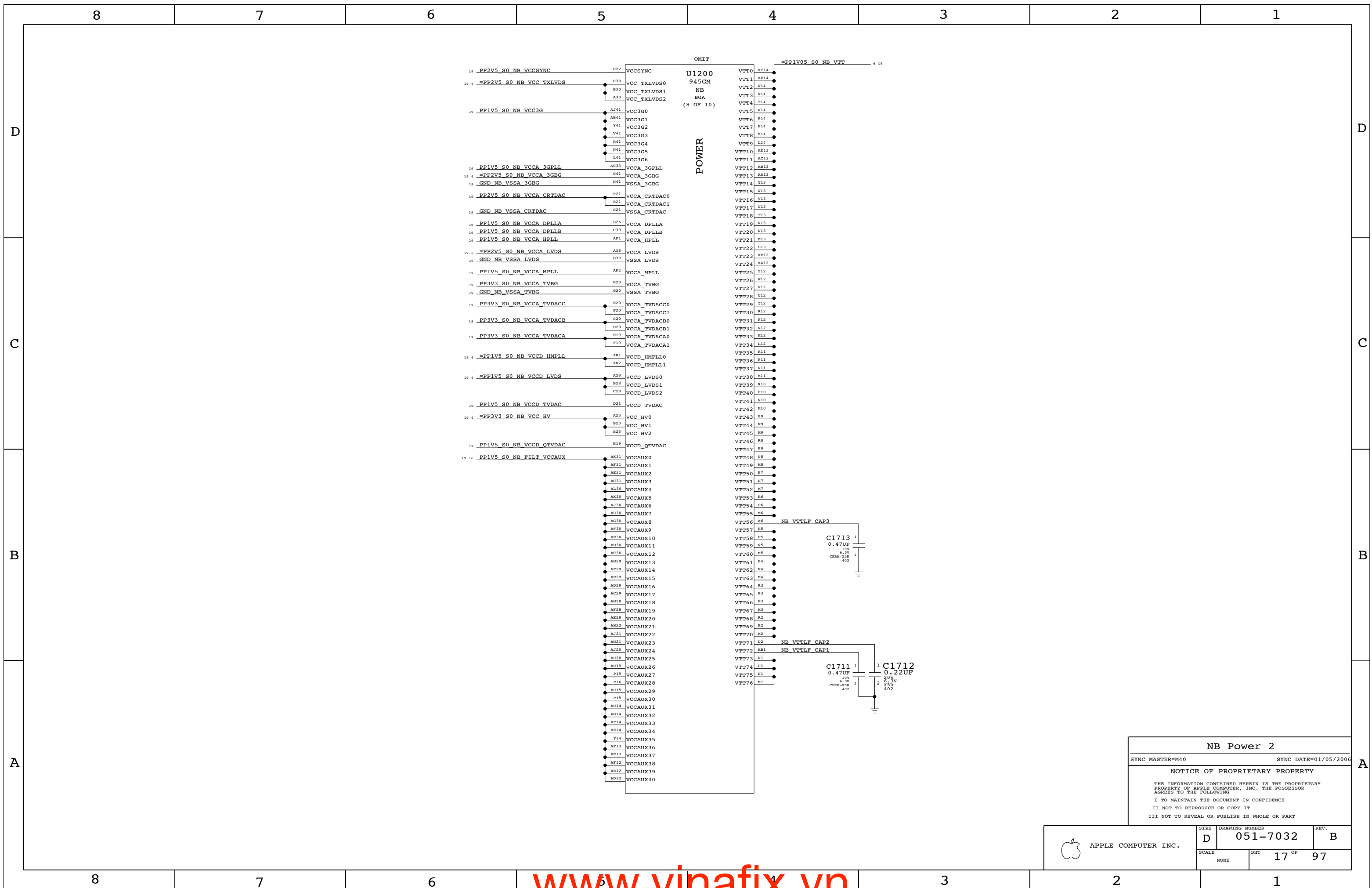
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NB Power 2

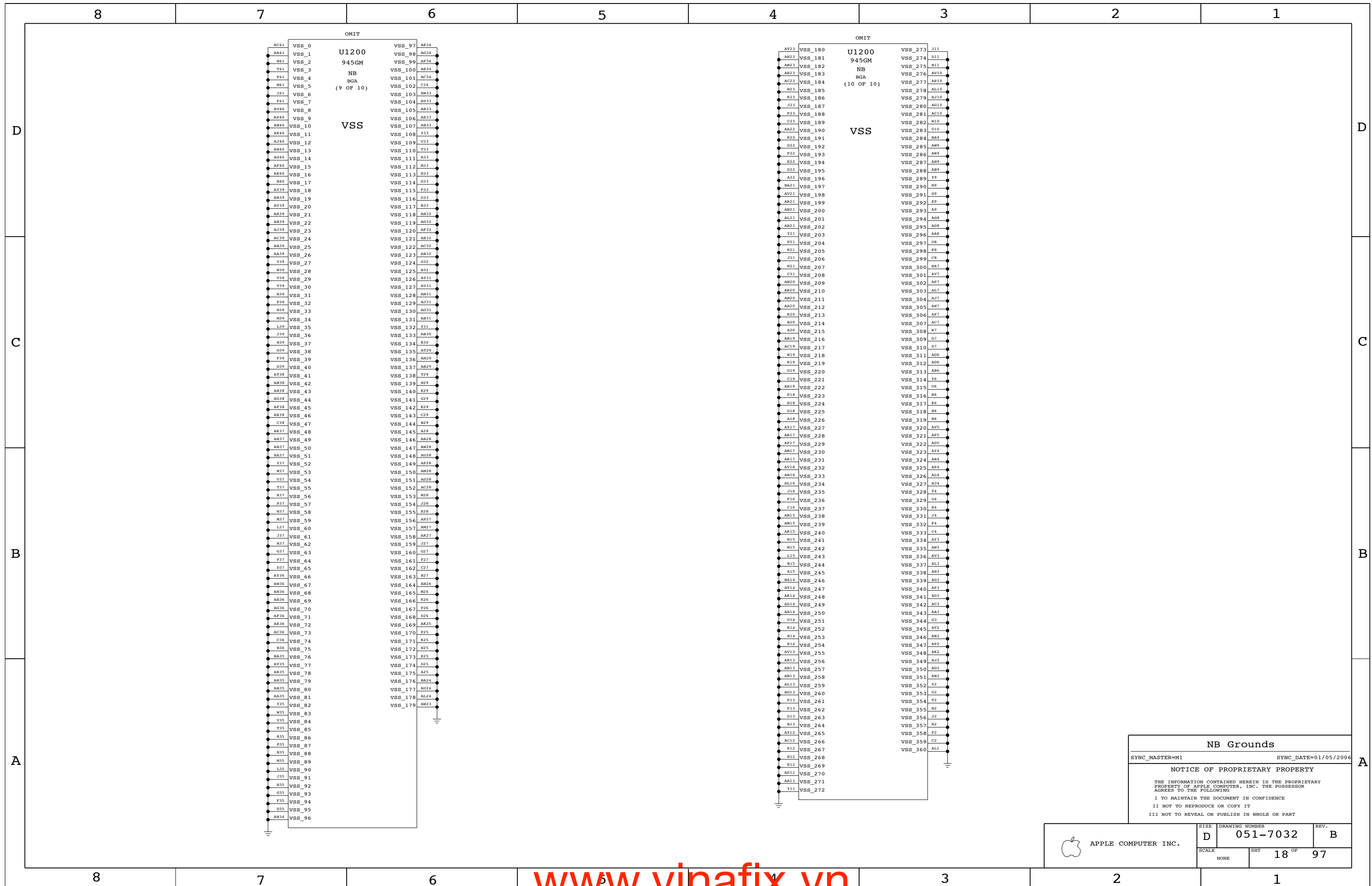
SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHT 17 OF 97	



NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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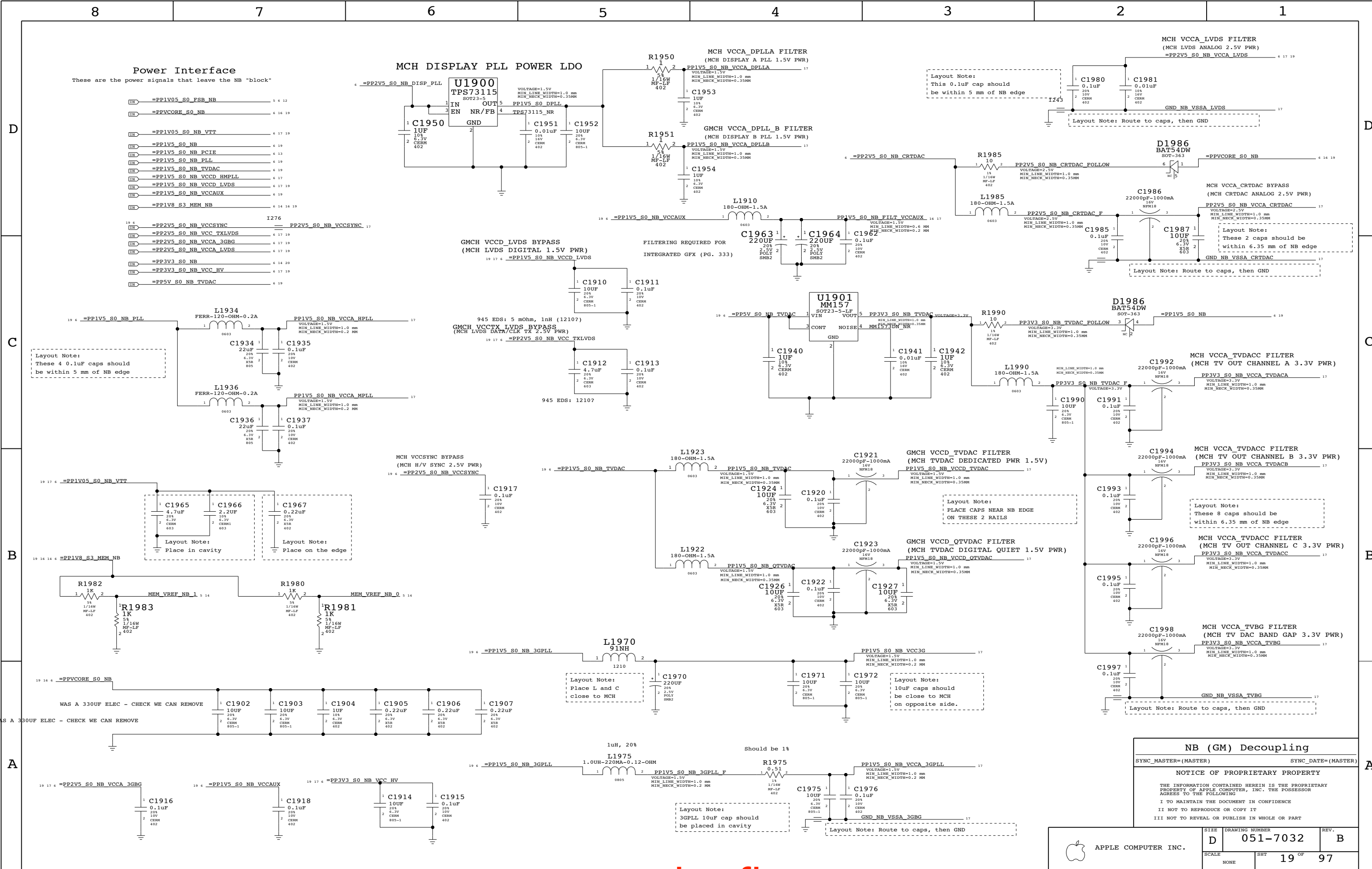
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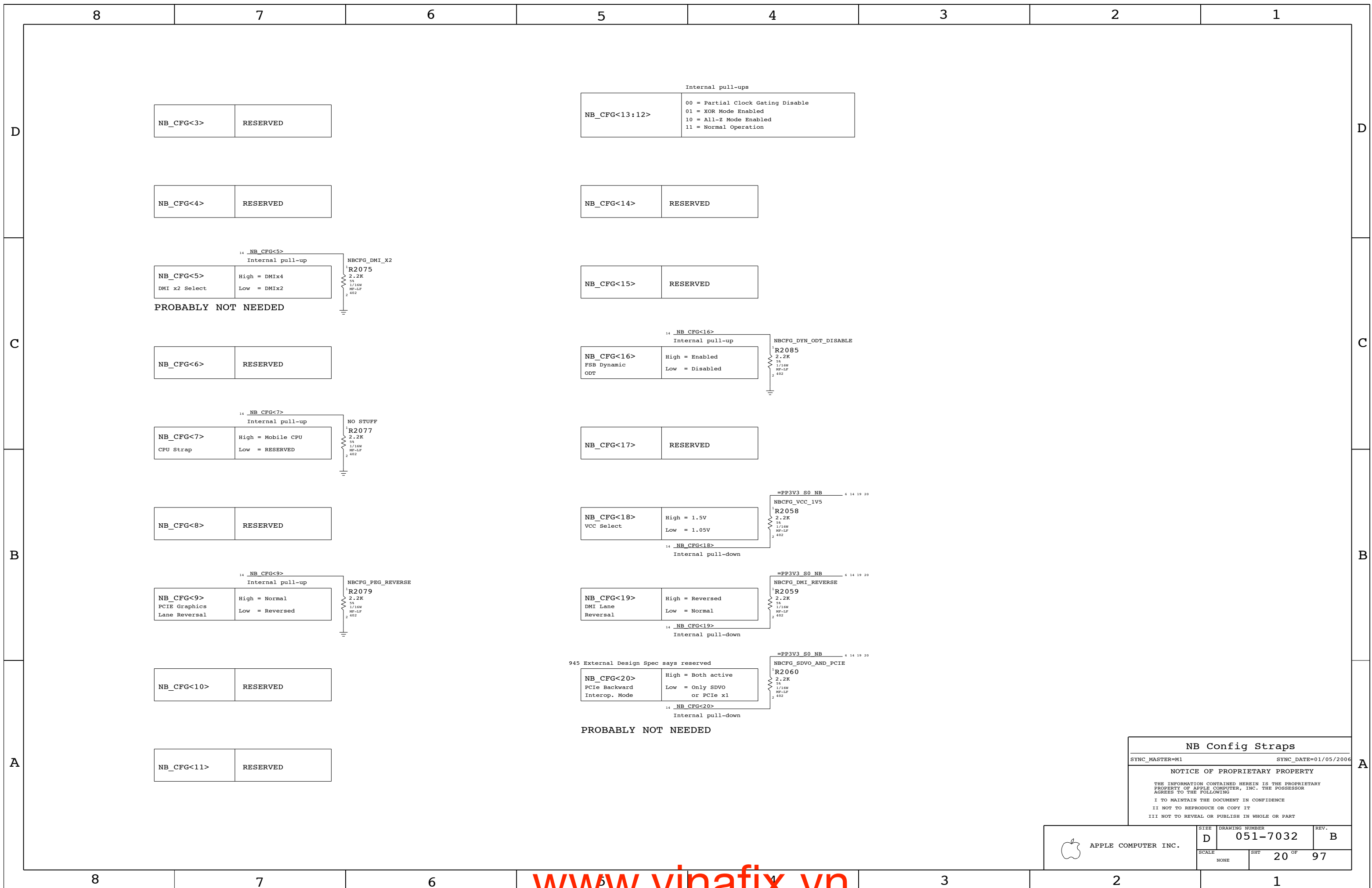
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	18 OF 97	
NONE			



NB (GM) Decoupling		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE: D SCALE: NONE	DRAWING NUMBER: 051-7032 SHEET: 19 OF 97	REV.: B
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NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED

NB_CFG<8>	RESERVED
-----------	----------

14 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

NB_CFG<10>	RESERVED
------------	----------

NB_CFG<11>	RESERVED
------------	----------

Internal pull-ups	
NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<15>	RESERVED
------------	----------

14 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled

NB_CFG<17>	RESERVED
------------	----------

14 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V

14 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal

945 External Design Spec says reserved	
14 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

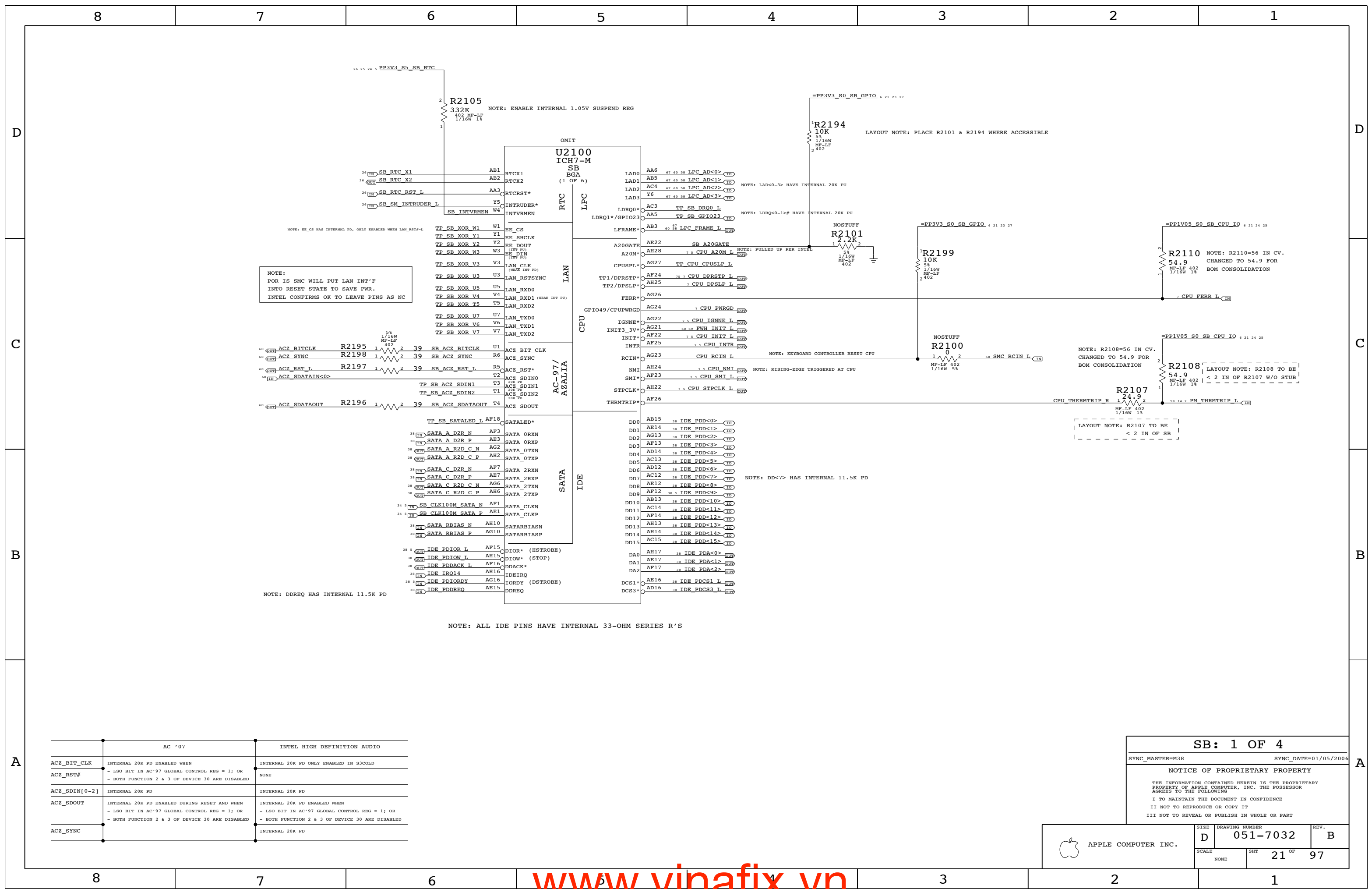
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	D	051-7032	B
SCALE	SHT	20 OF 97	
NONE			



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

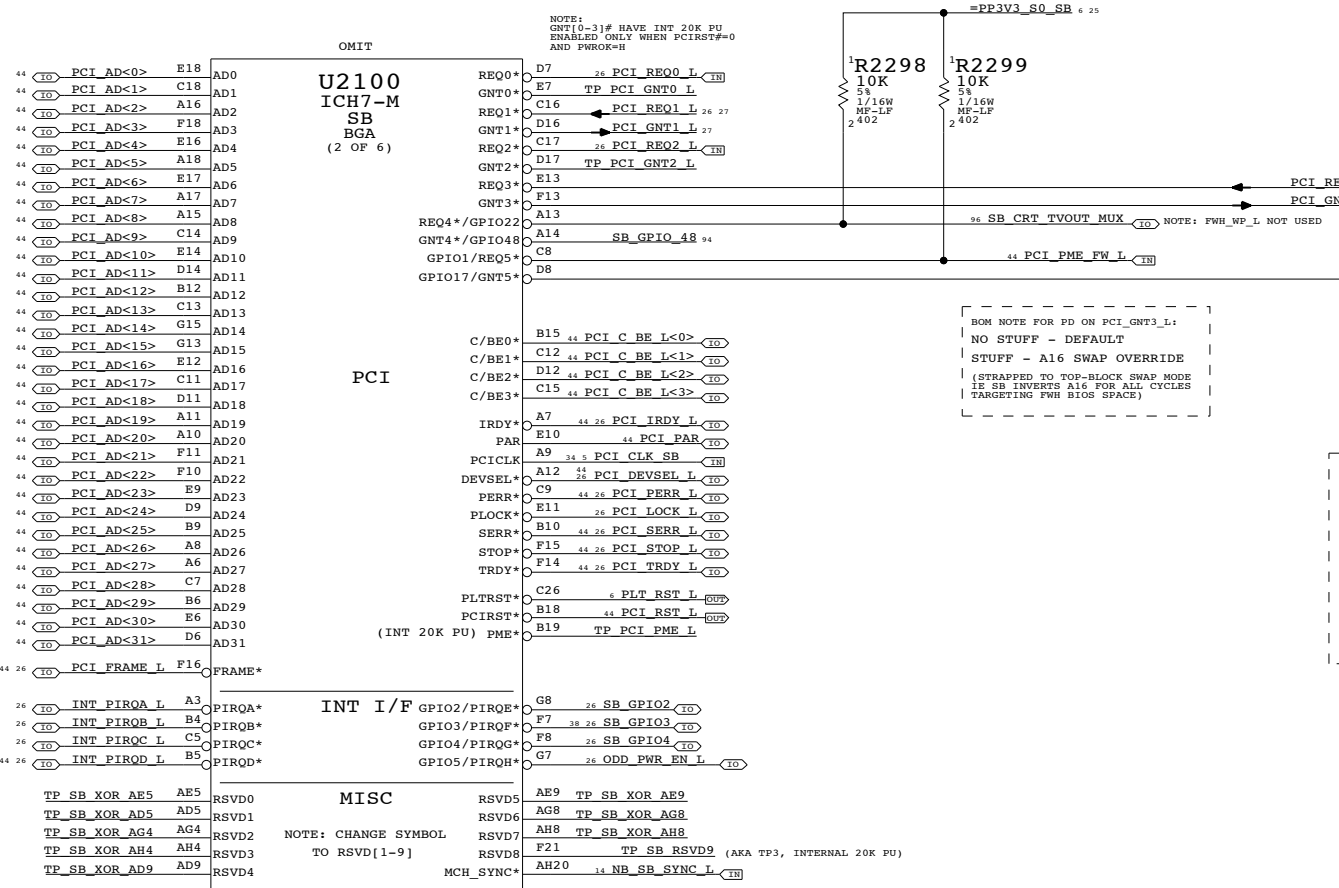
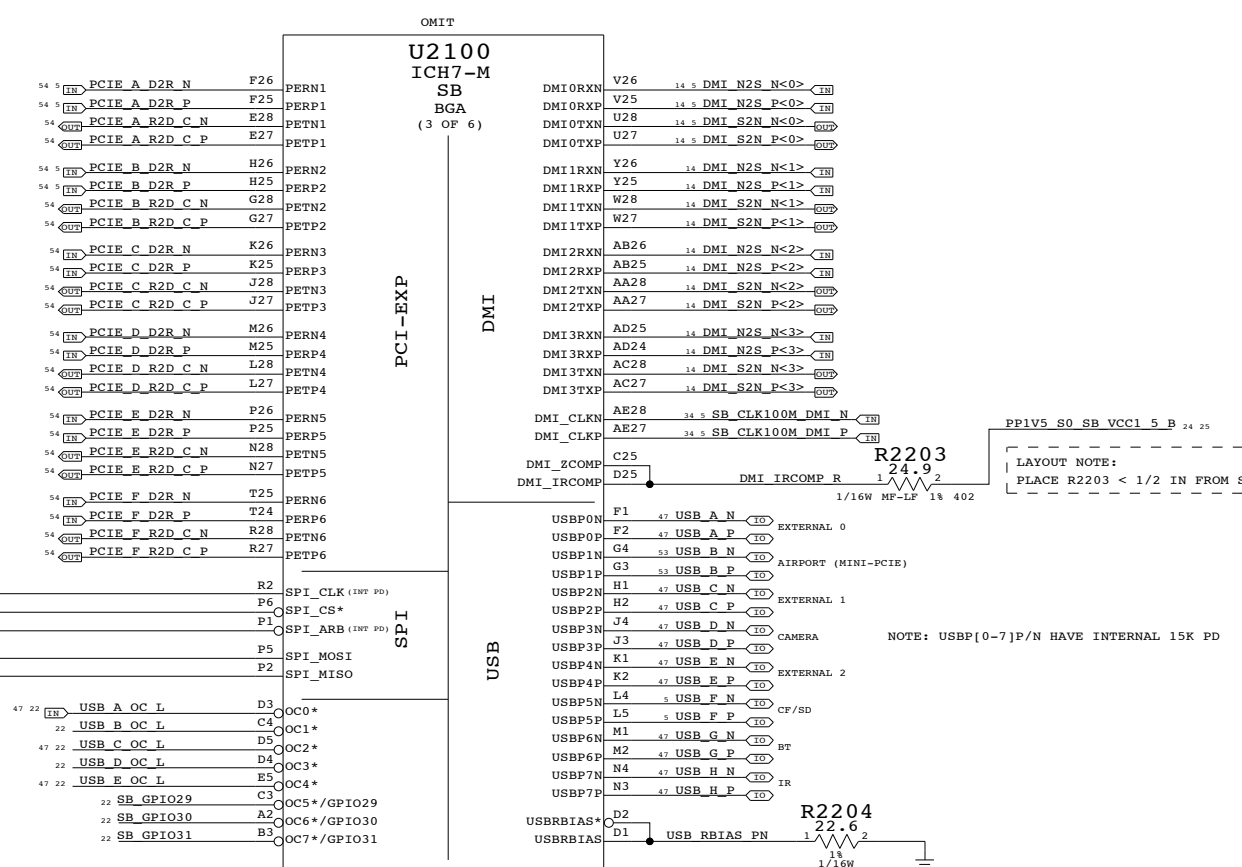
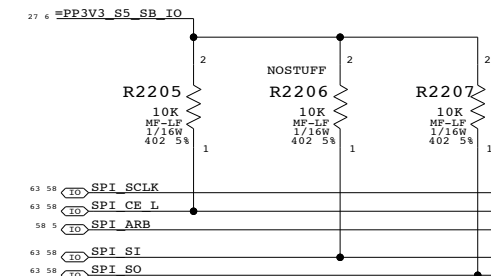
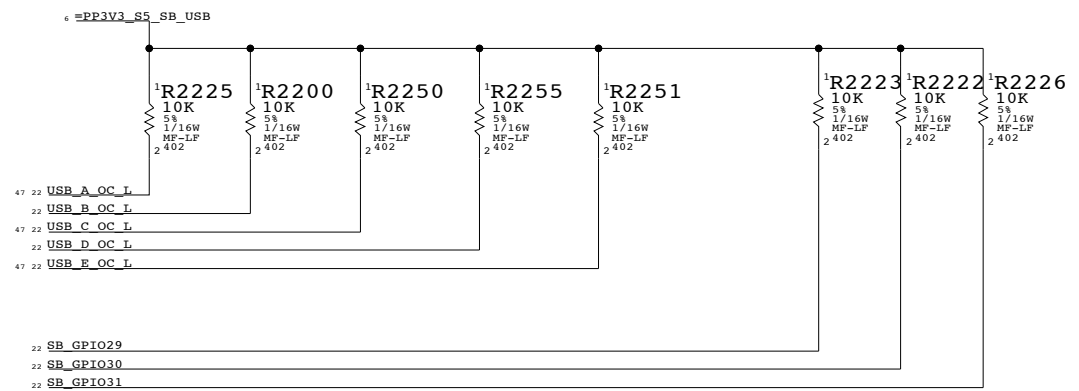
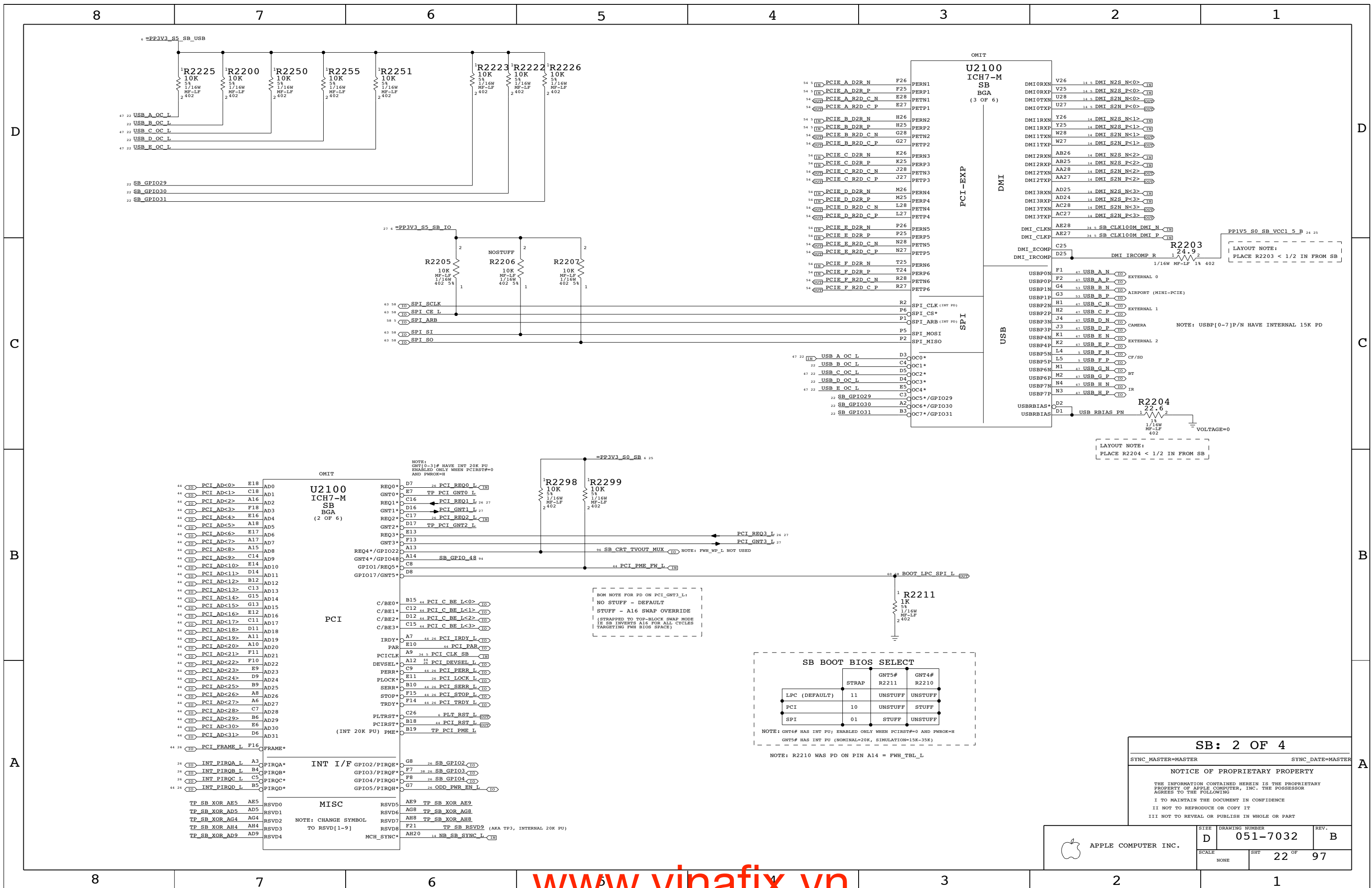
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT		REV.
NONE	21 OF 97		



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#0 AND FWOR#H

NOTE: GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FW_H_TBL_L

SB: 2 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

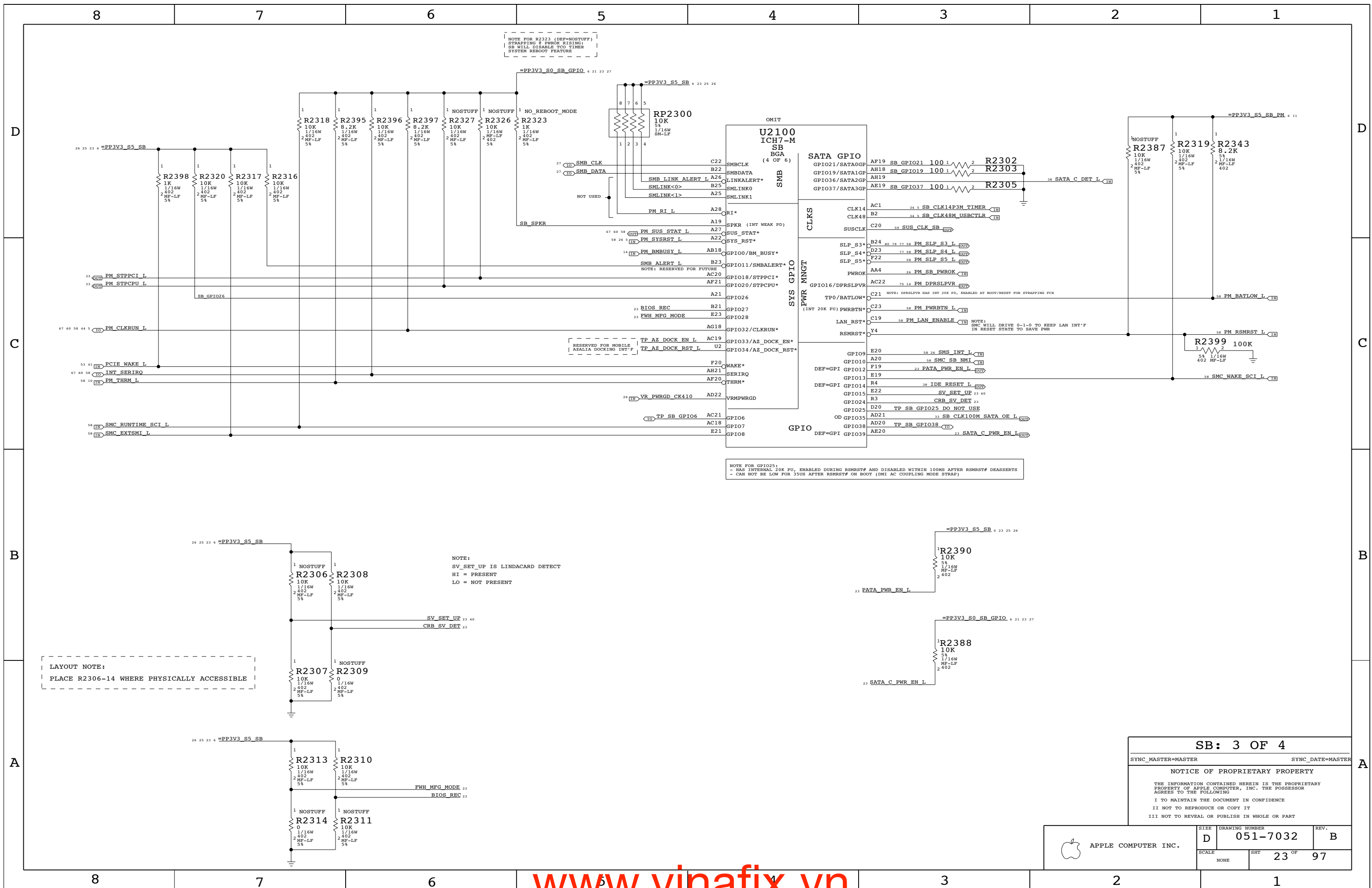
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	D	051-7032	B
SCALE	SHT	22 OF 97	
NONE			



NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING & PWROK RISING:
SB WILL DISABLE TOO TIMER
SYSTEM REBOOT FEATURE

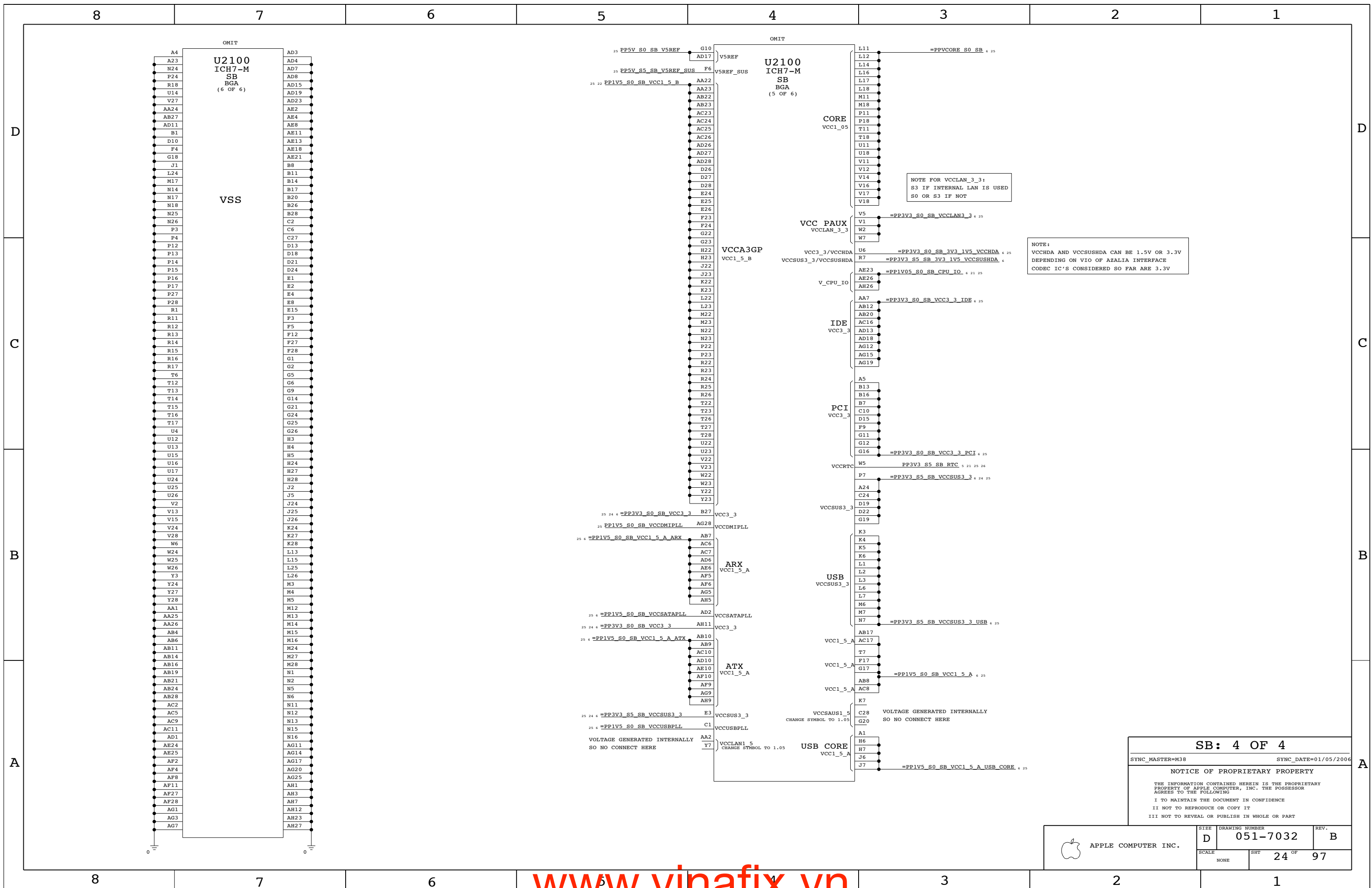
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SB: 3 OF 4
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	B
SCALE	NONE	SHT	23 OF 97



SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

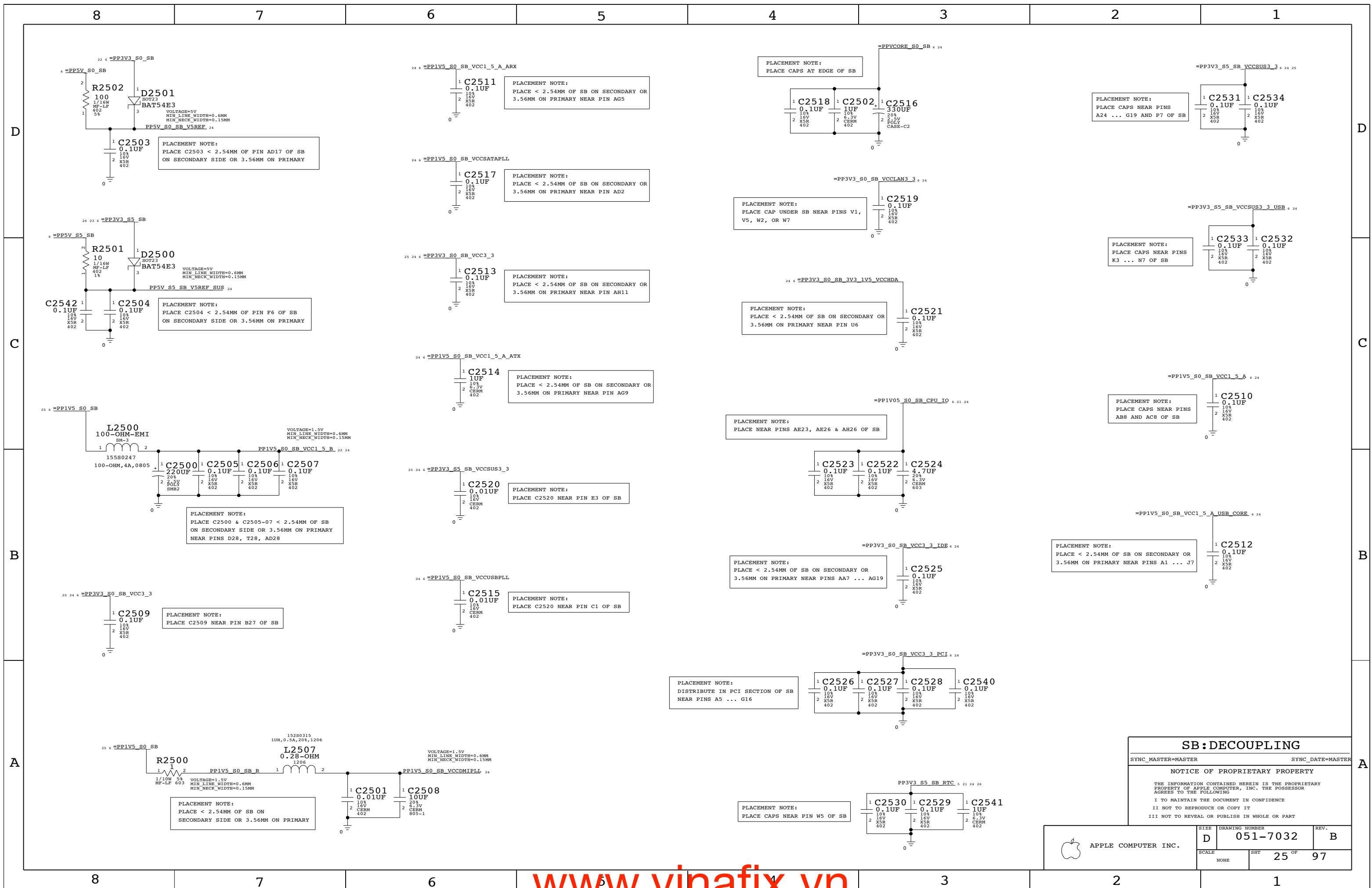
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 24 OF 97	



SB: DECOUPLING

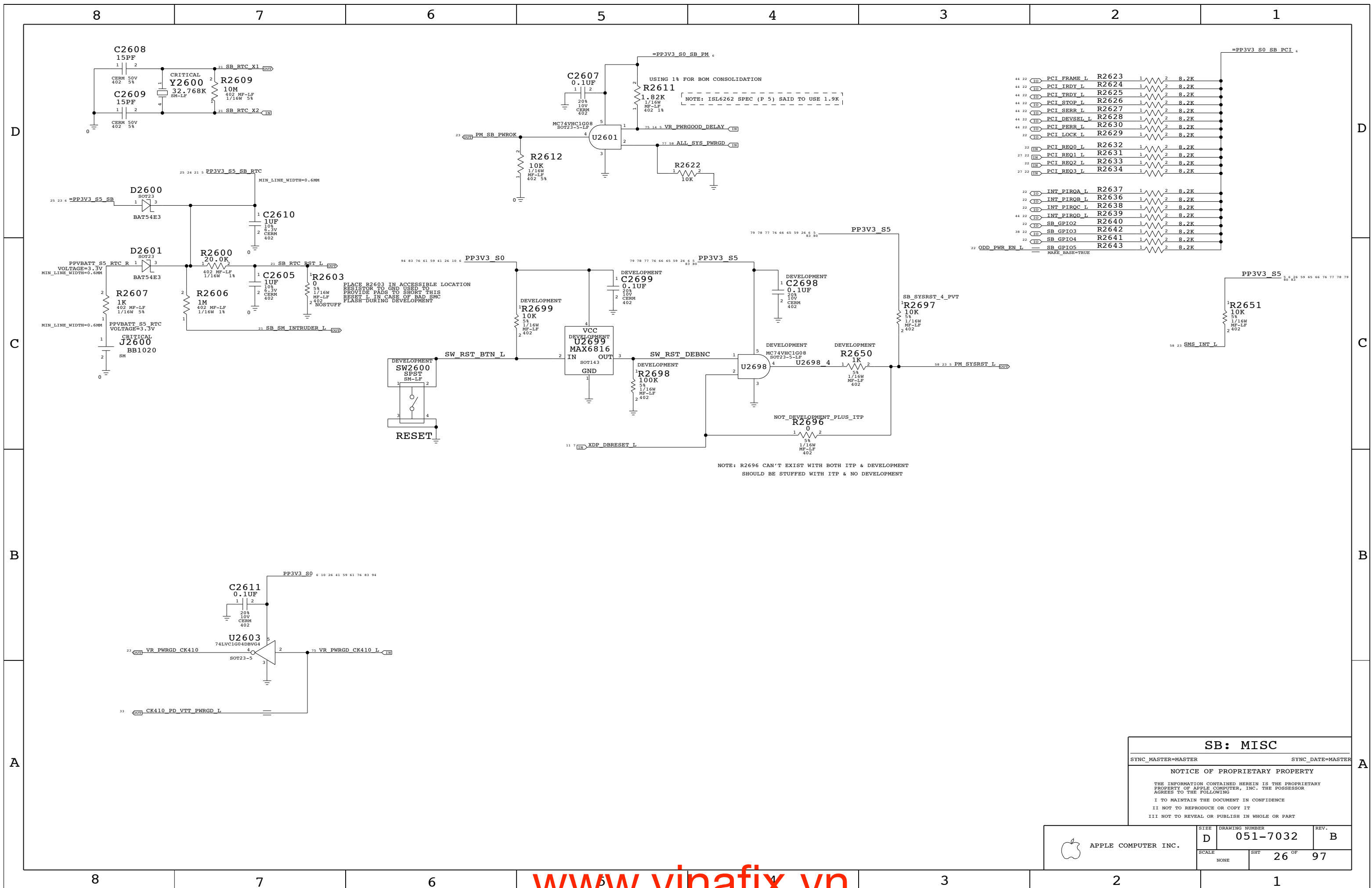
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	25 OF 97	
NONE			



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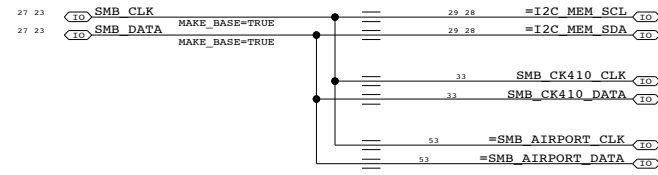
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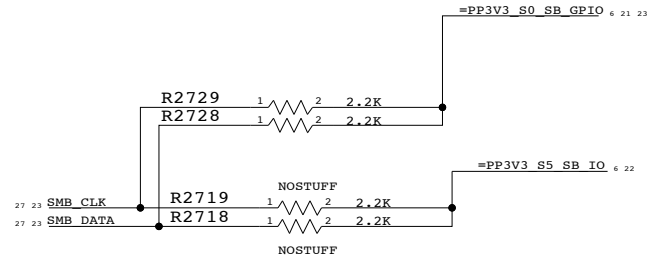
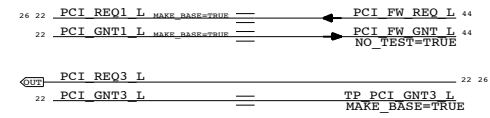
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SB I2C BUSSES



PCI CONTROL



SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT		OF
NONE	27		97

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Page Notes

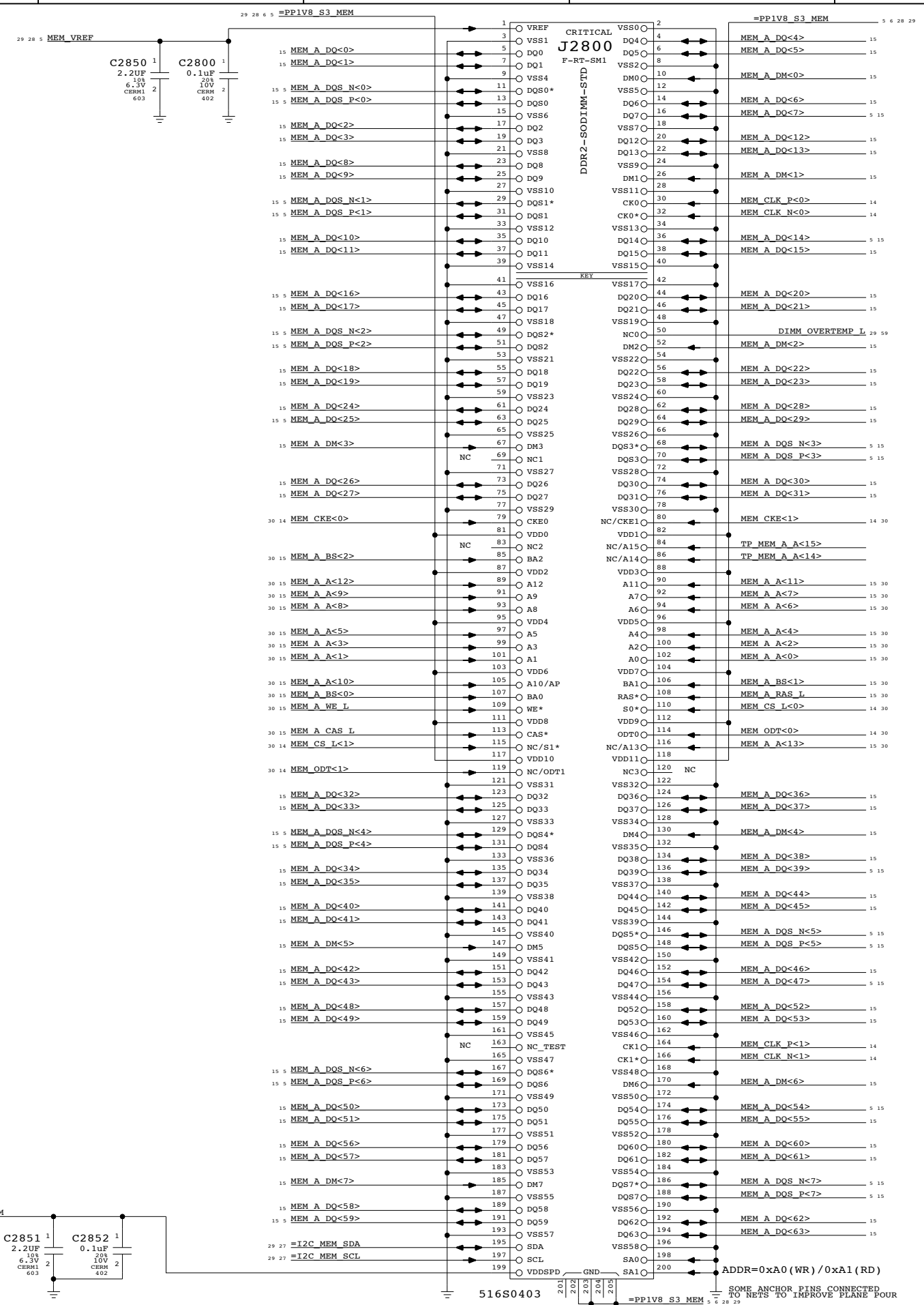
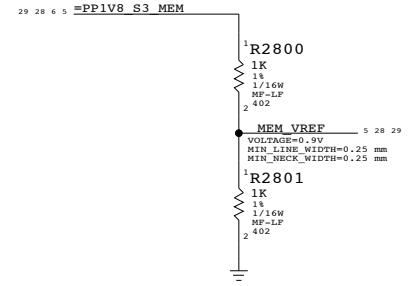
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

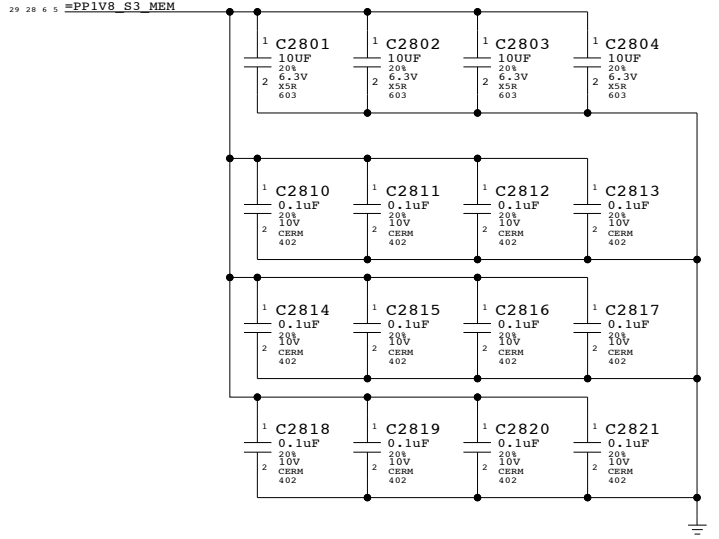
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	28 OF 97	
NONE			

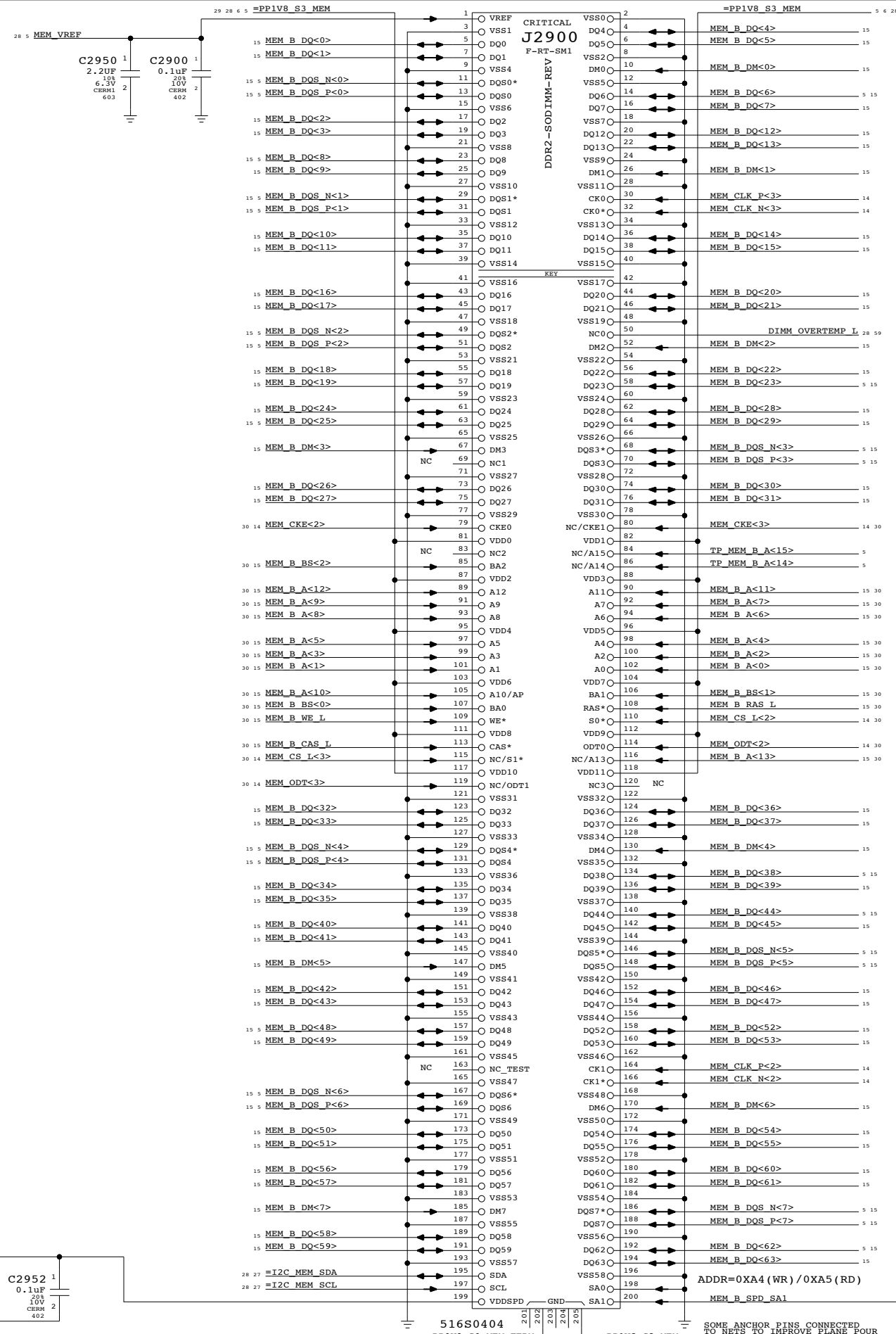
Page Notes

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 - =PPSPD_S0_MEM (2.5V - 3.3V)

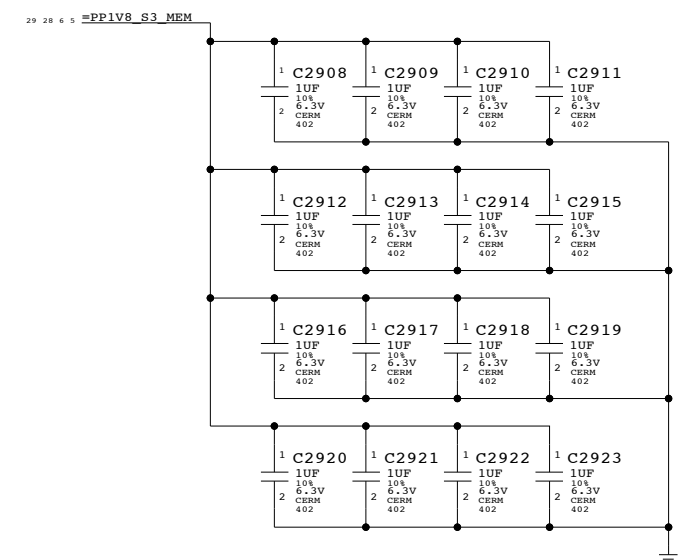
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	29 OF	97
NONE			

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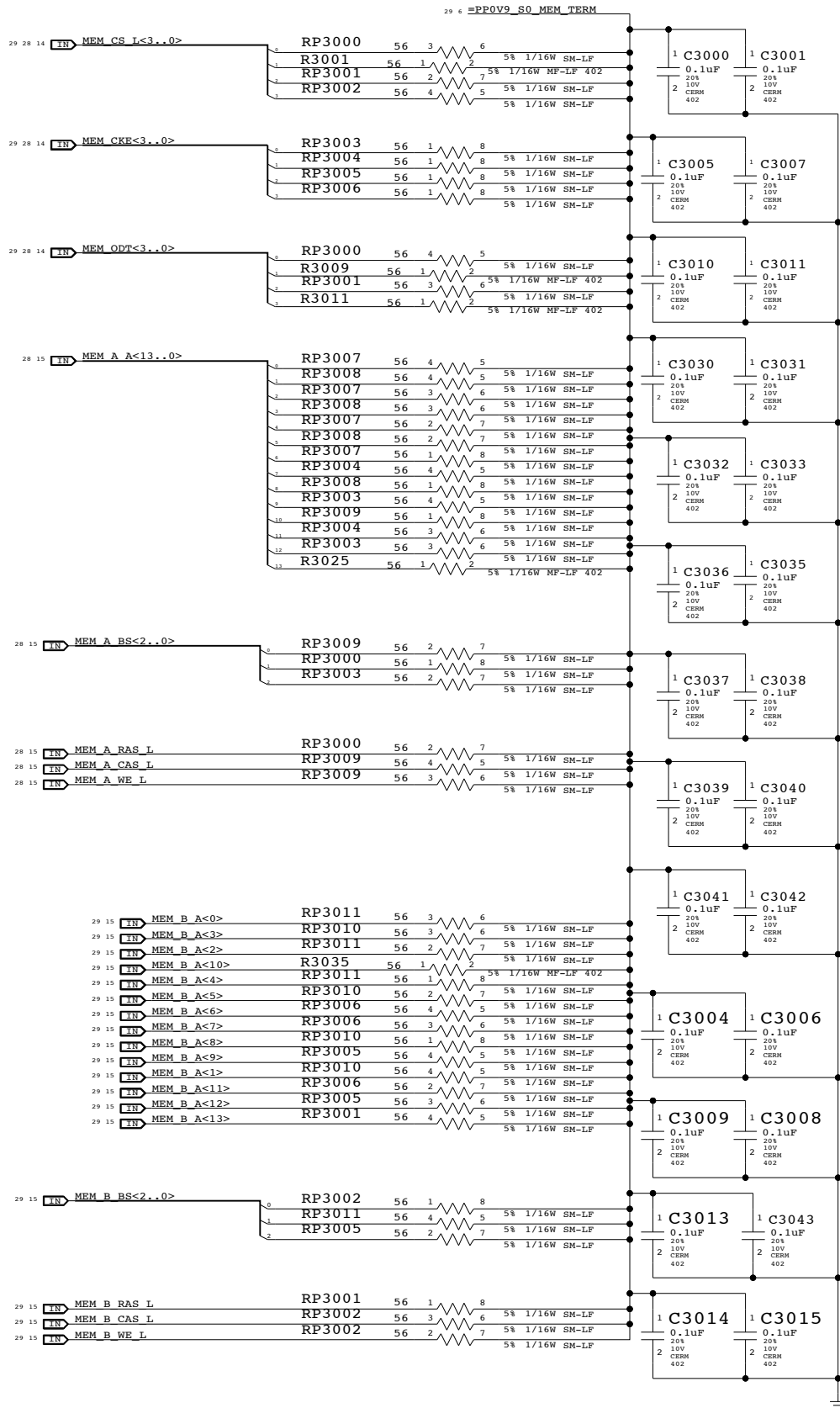
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One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7032	B
SCALE	SHT	30 OF	97
NONE			

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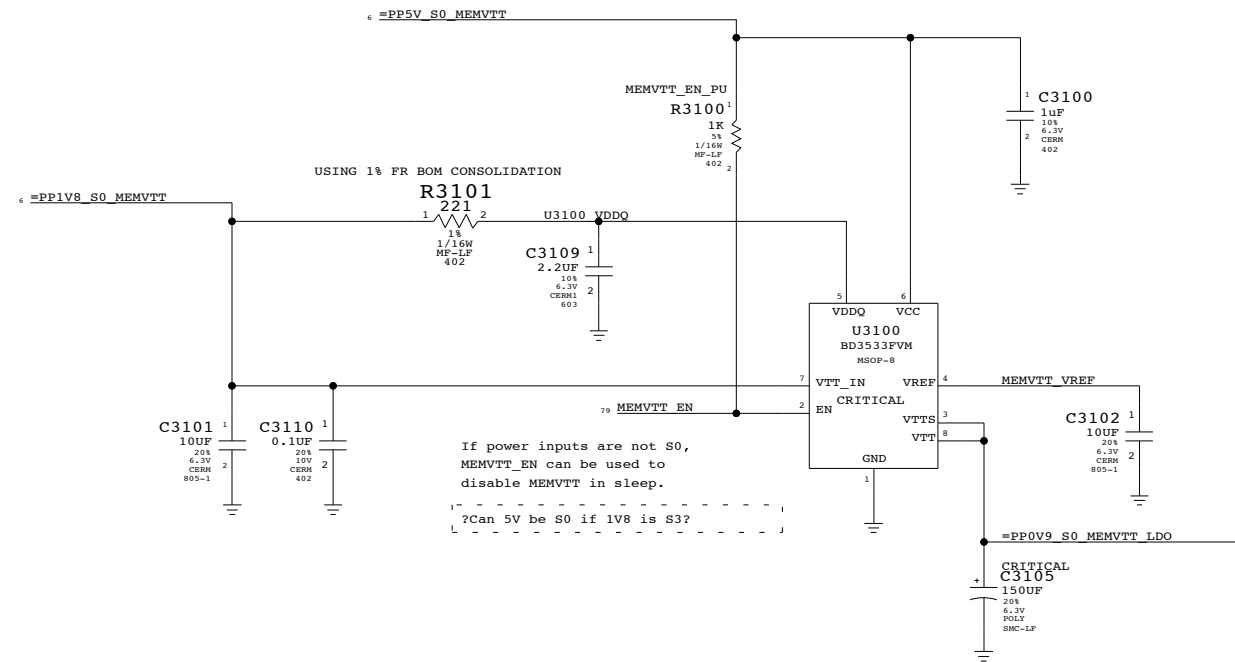
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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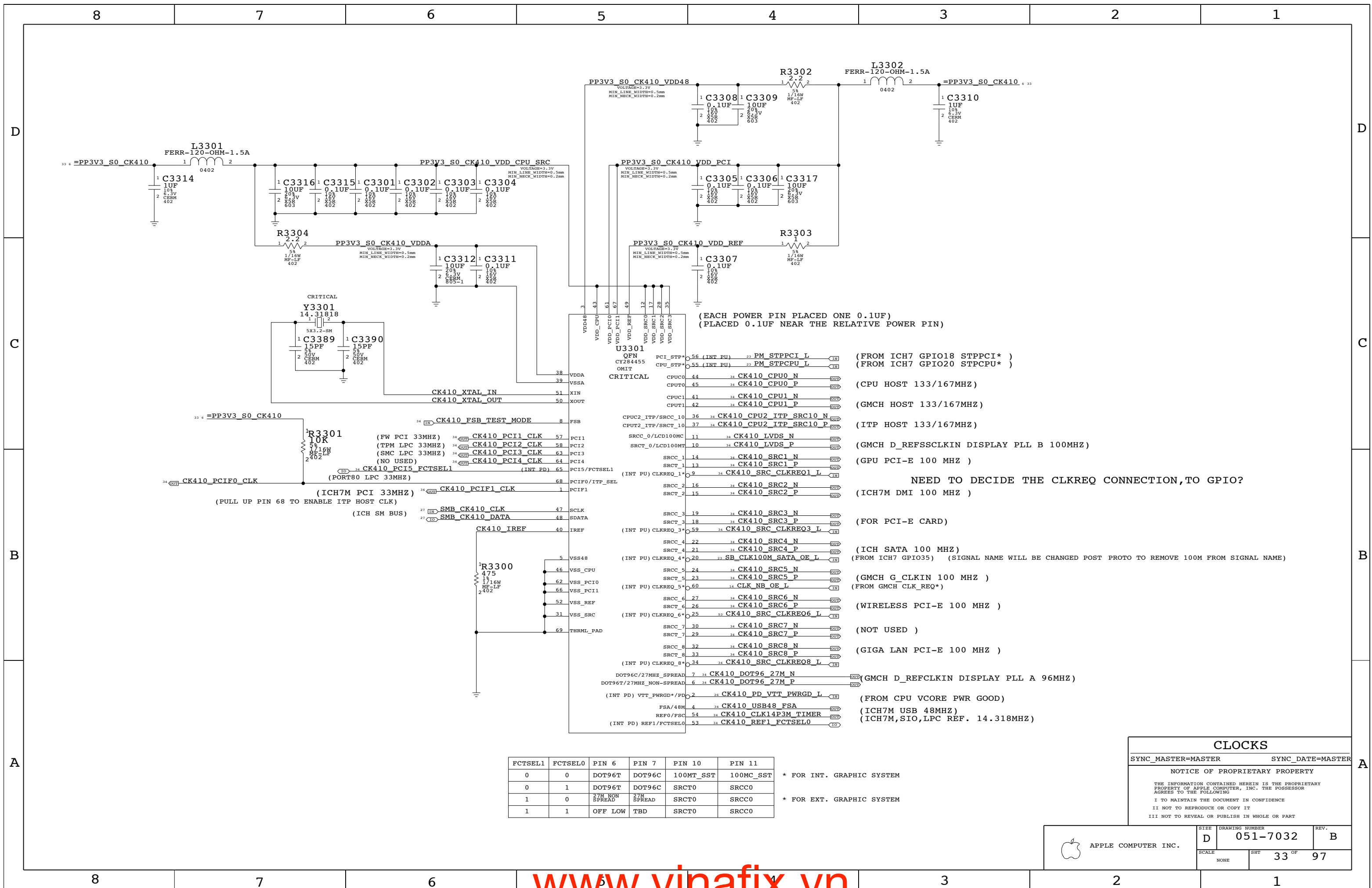
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	D	051-7032	B
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) PM STPPCI L (FROM ICH7 GPIO18 STPPCI*)
- 55 (INT PU) PM STPCPU L (FROM ICH7 GPIO20 STPCPU*)
- 34 CK410_CPU0_N (CPU HOST 133/167MHZ)
- 34 CK410_CPU0_P
- 34 CK410_CPU1_N (GMCH HOST 133/167MHZ)
- 34 CK410_CPU1_P
- 34 CK410_CPU2_ITP_SRC10_N (ITP HOST 133/167MHZ)
- 34 CK410_CPU2_ITP_SRC10_P
- 34 CK410_LVDS_N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 34 CK410_LVDS_P
- 34 CK410_SRC1_N (GPU PCI-E 100 MHZ)
- 34 CK410_SRC1_P
- 34 CK410_SRC_CLKREQ1_L (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 34 CK410_SRC2_N (ICH7M DMI 100 MHZ)
- 34 CK410_SRC2_P
- 34 CK410_SRC3_N (FOR PCI-E CARD)
- 34 CK410_SRC3_P
- 34 CK410_SRC_CLKREQ3_L
- 34 CK410_SRC4_N (ICH SATA 100 MHZ)
- 34 CK410_SRC4_P (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 34 CK410_SRC5_N (GMCH G_CLKIN 100 MHZ)
- 34 CK410_SRC5_P (FROM GMCH CLK_REQ*)
- 34 CK410_SRC6_N (WIRELESS PCI-E 100 MHZ)
- 34 CK410_SRC6_P
- 34 CK410_SRC_CLKREQ6_L
- 34 CK410_SRC7_N (NOT USED)
- 34 CK410_SRC7_P
- 34 CK410_SRC8_N (GIGA LAN PCI-E 100 MHZ)
- 34 CK410_SRC8_P
- 34 CK410_SRC_CLKREQ8_L
- 34 CK410_DOT96_27M_N (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 34 CK410_DOT96_27M_P
- 34 CK410_PD_VTT_PWRGD_L (FROM CPU VCORE PWR GOOD)
- 34 CK410_USB48_FSA (ICH7M USB 48MHZ)
- 34 CK410_CLK14P3M_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 34 CK410_REF1_FCTSELO

FCTSEL1	FCTSELO	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0
1	1	OFF_LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

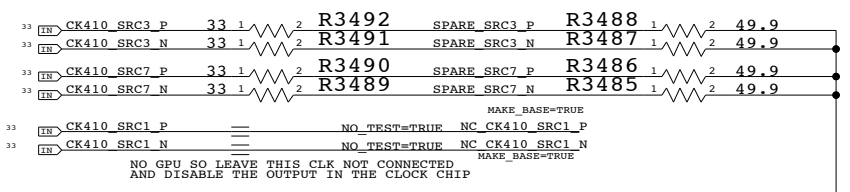
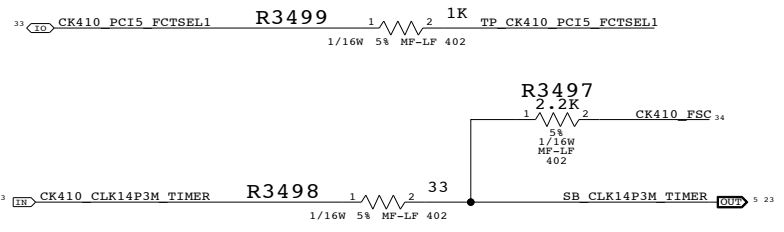
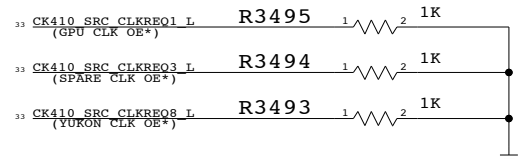
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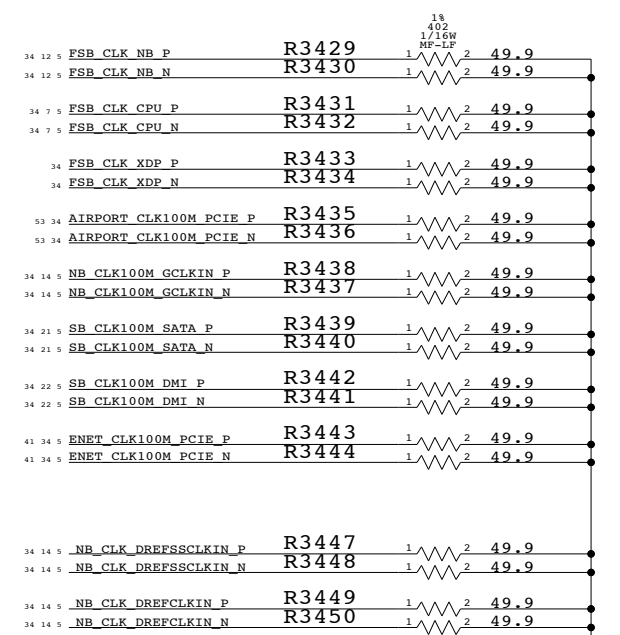
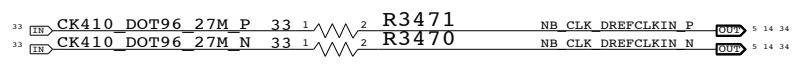
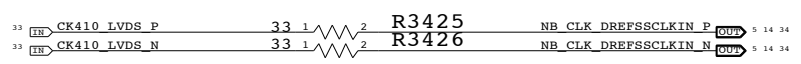
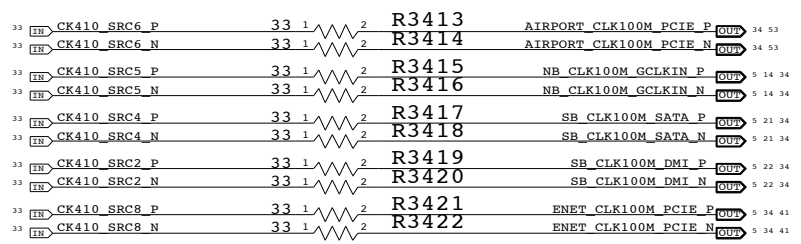
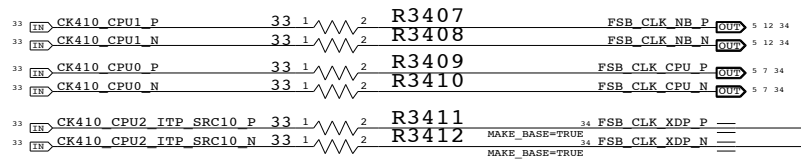
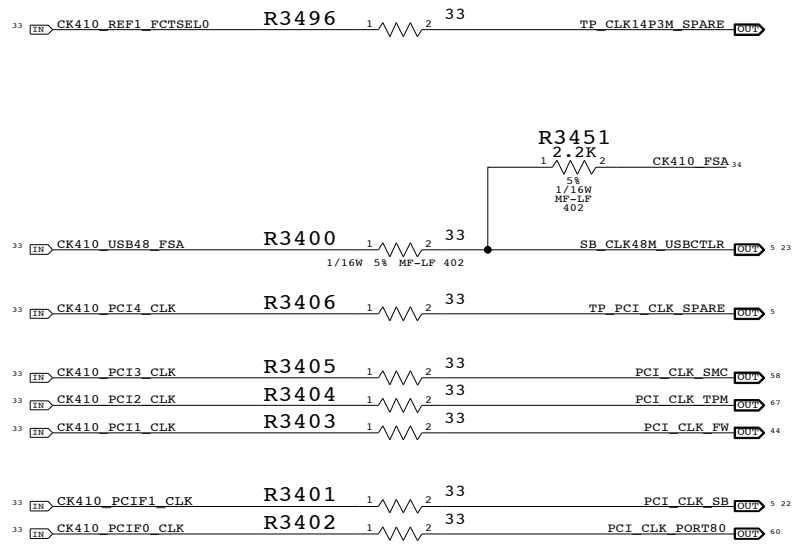
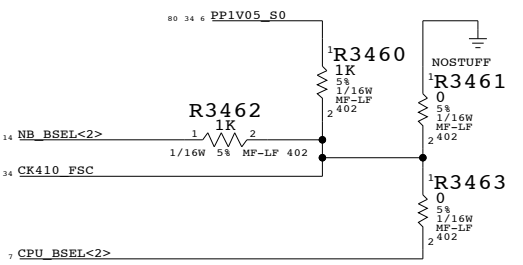
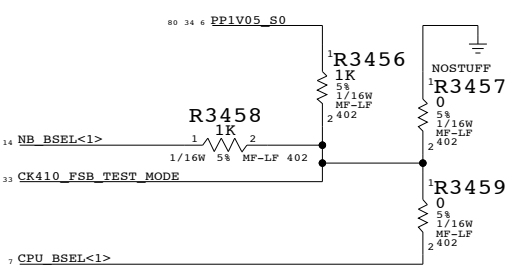
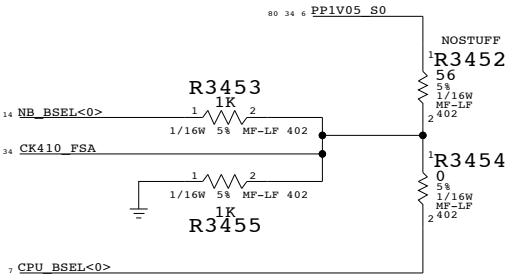
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	33 OF 97	
NONE			

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3455 R3461	R3452 R3453 R3463
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3461	R3454 R3455 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3461	R3454 R3455 R3463



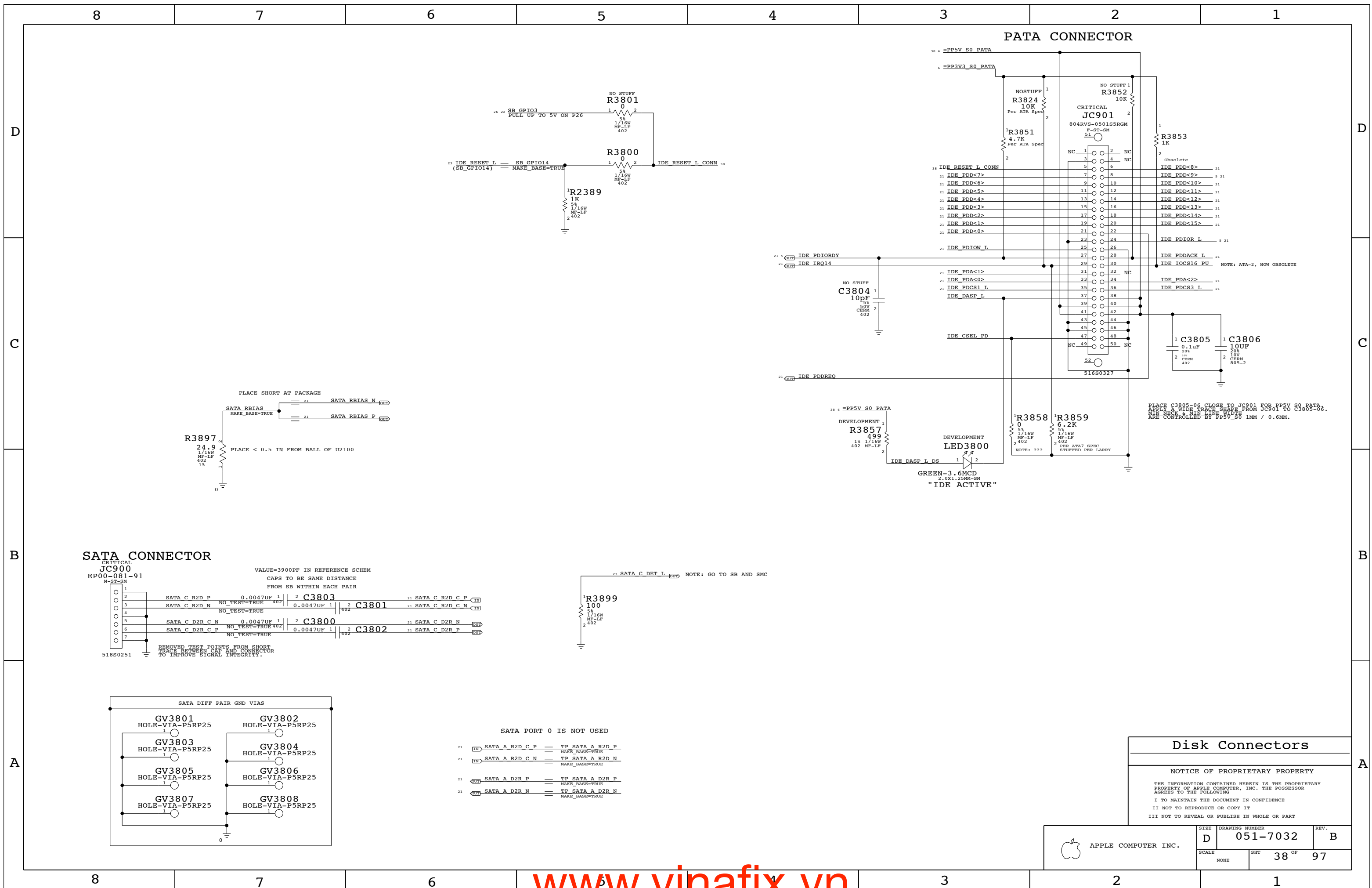
CLOCKS: TERMINATIONS

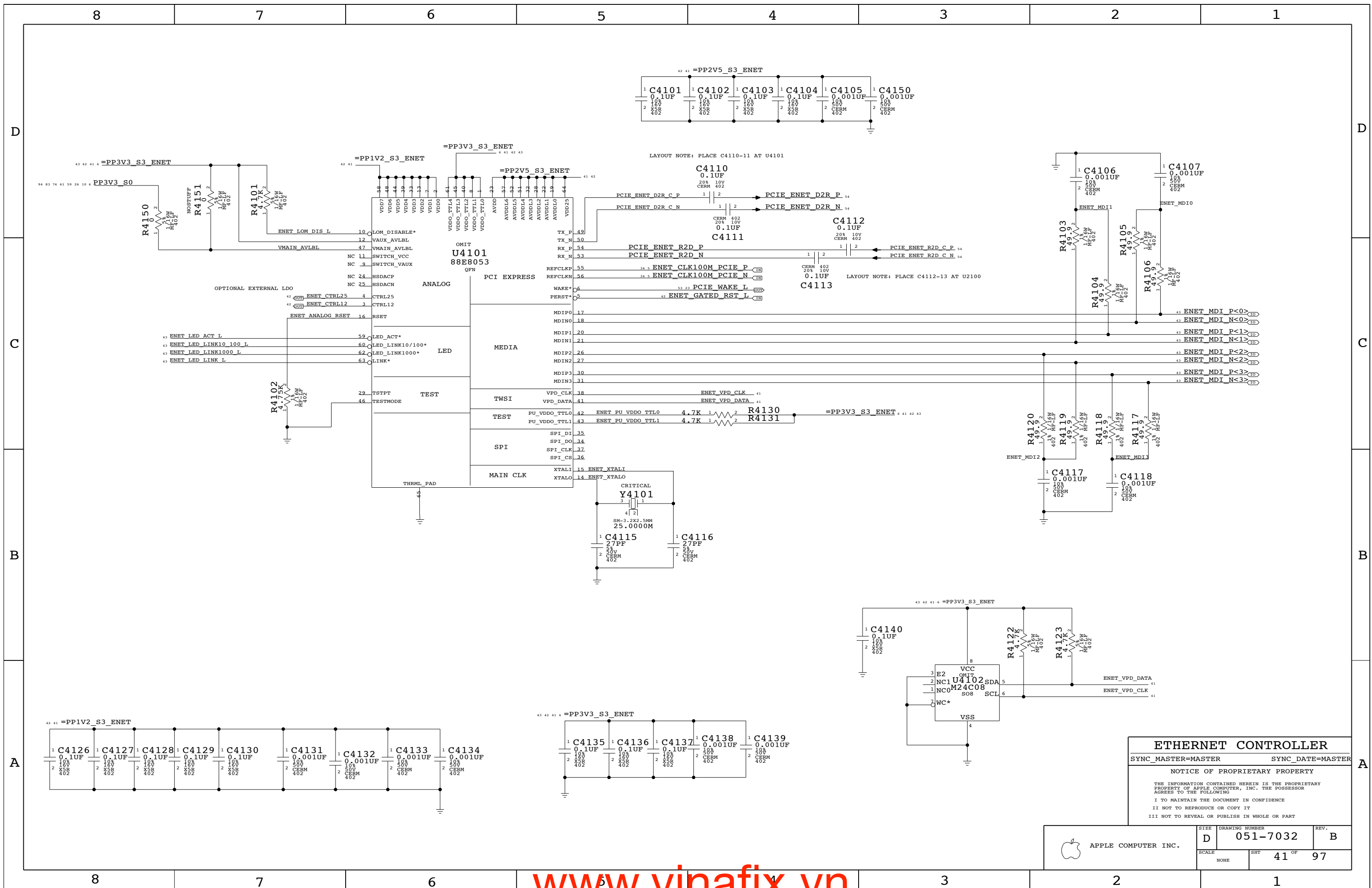
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	34 OF	97
NONE			





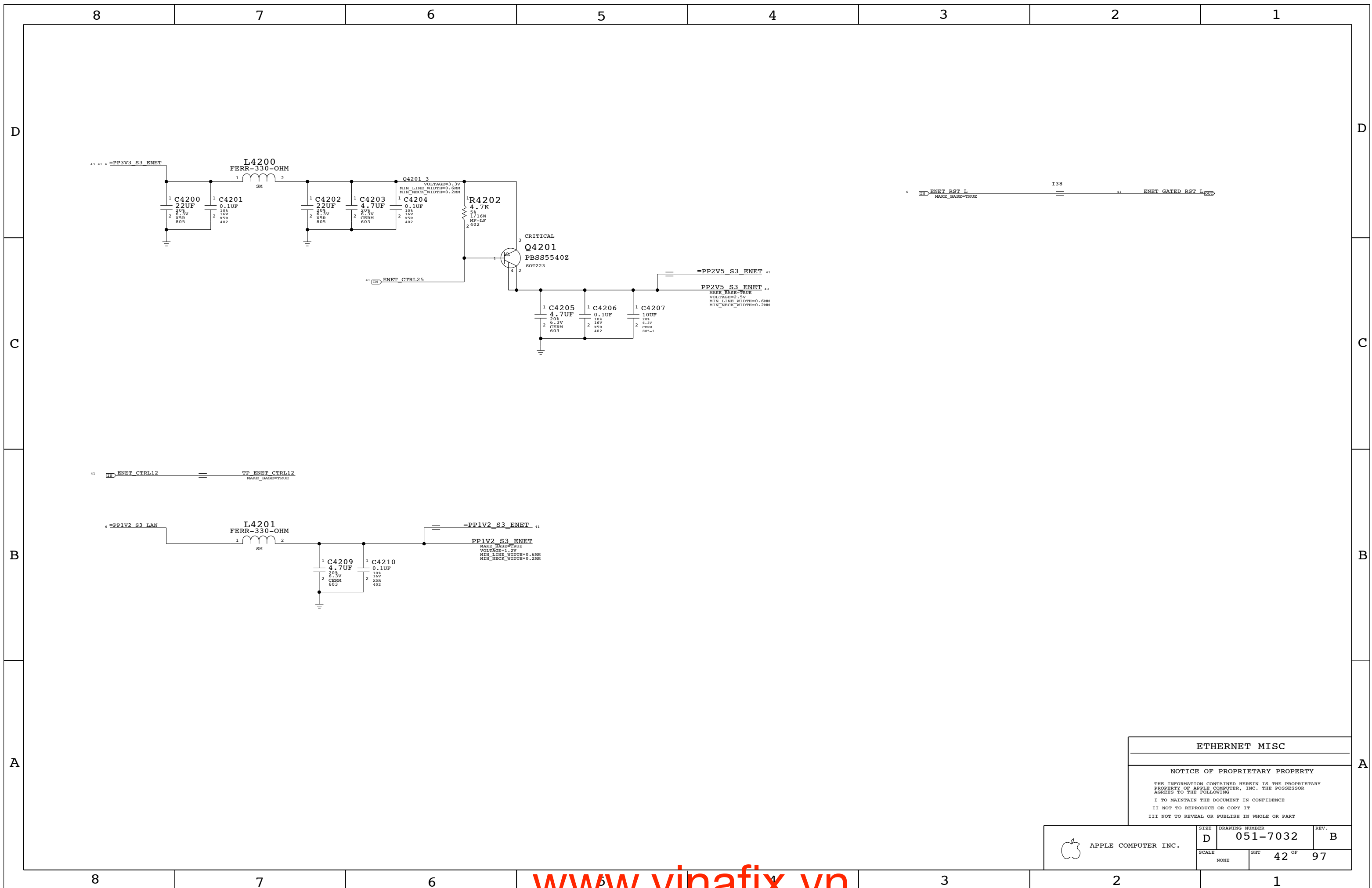
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

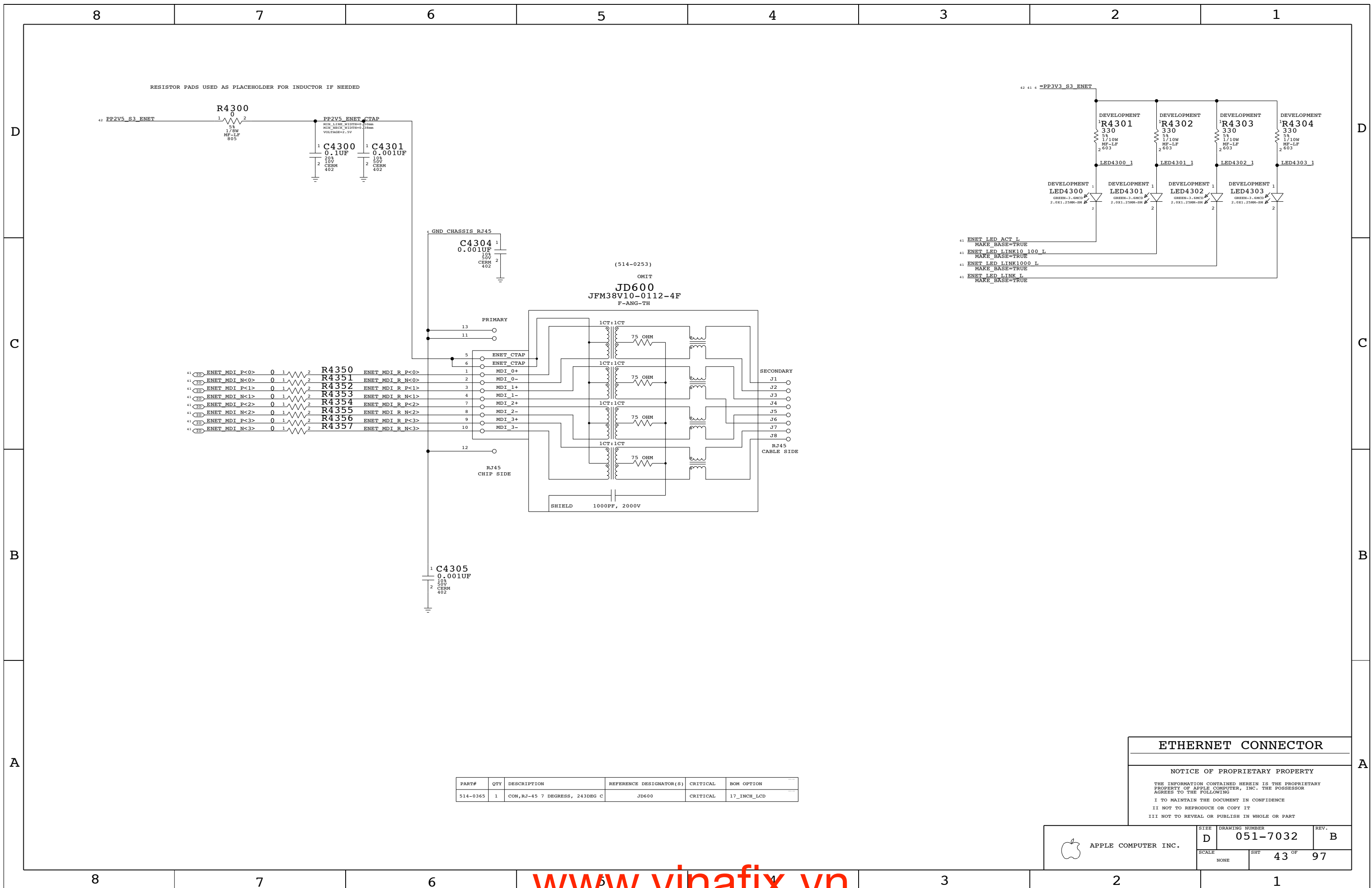
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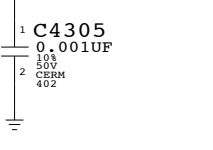
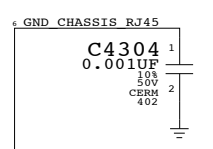
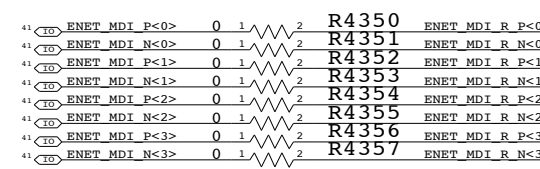
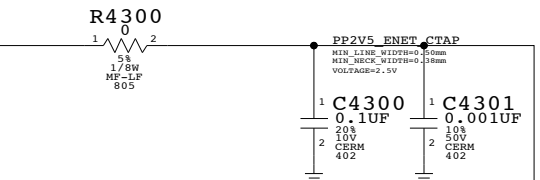
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

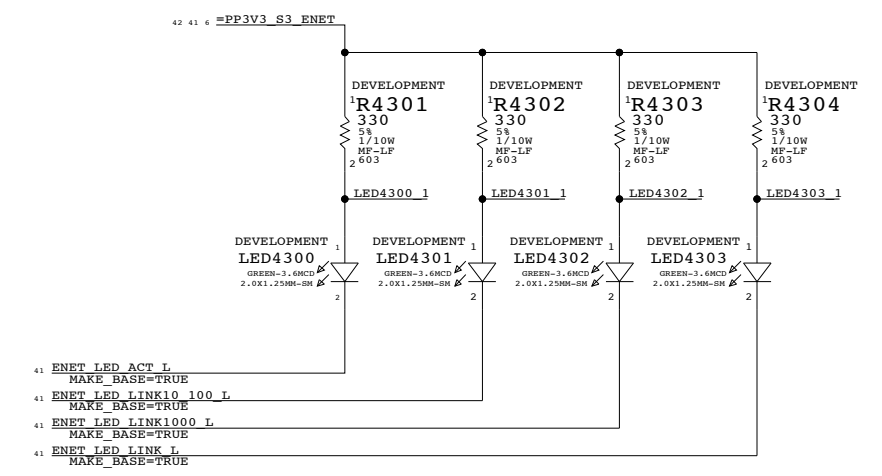
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 42 OF 97	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



(514-0253)
 OMIT
JD600
 JFM38V10-0112-4F
 P-ANG-TH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

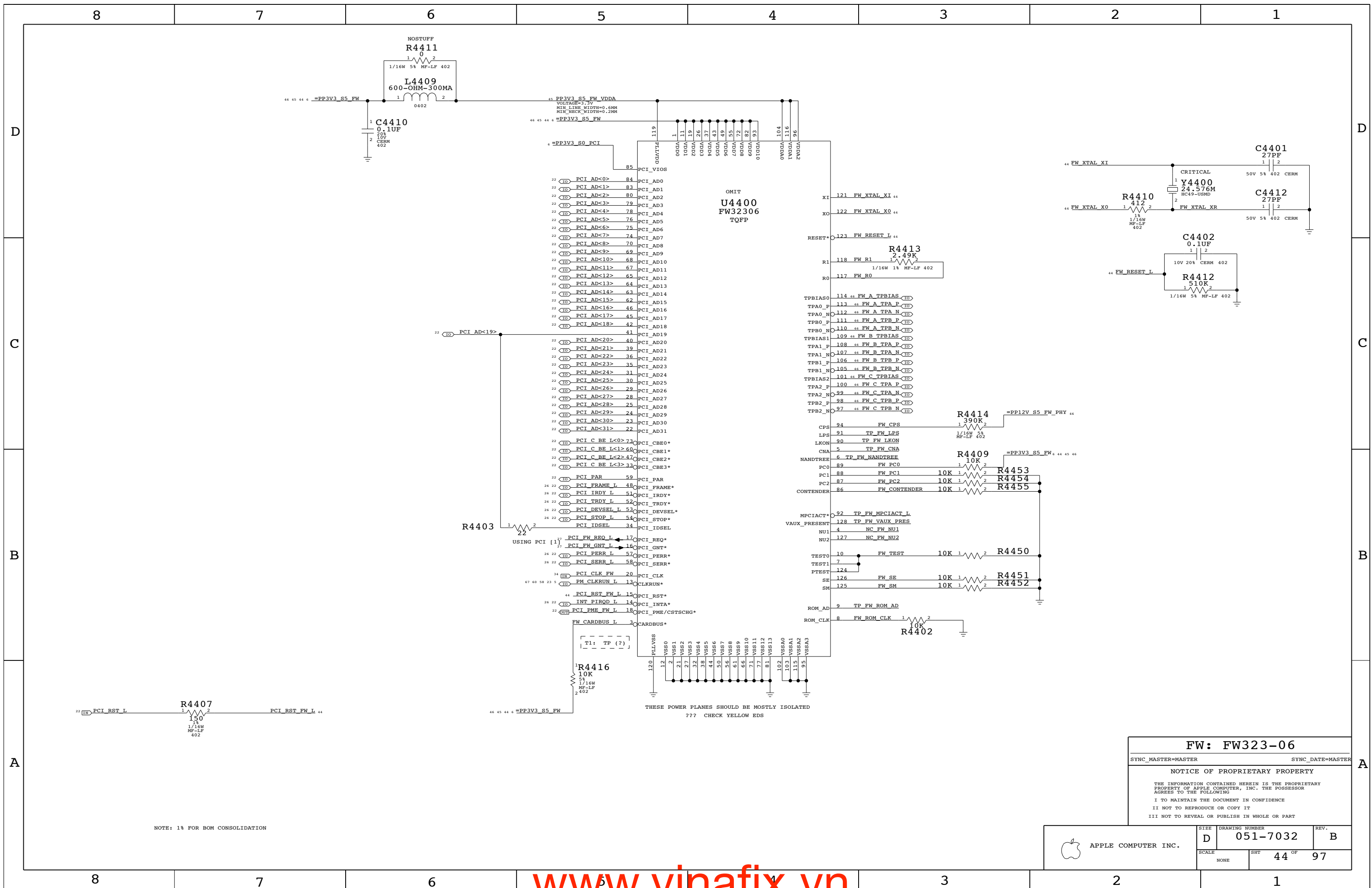
ETHERNET CONNECTOR

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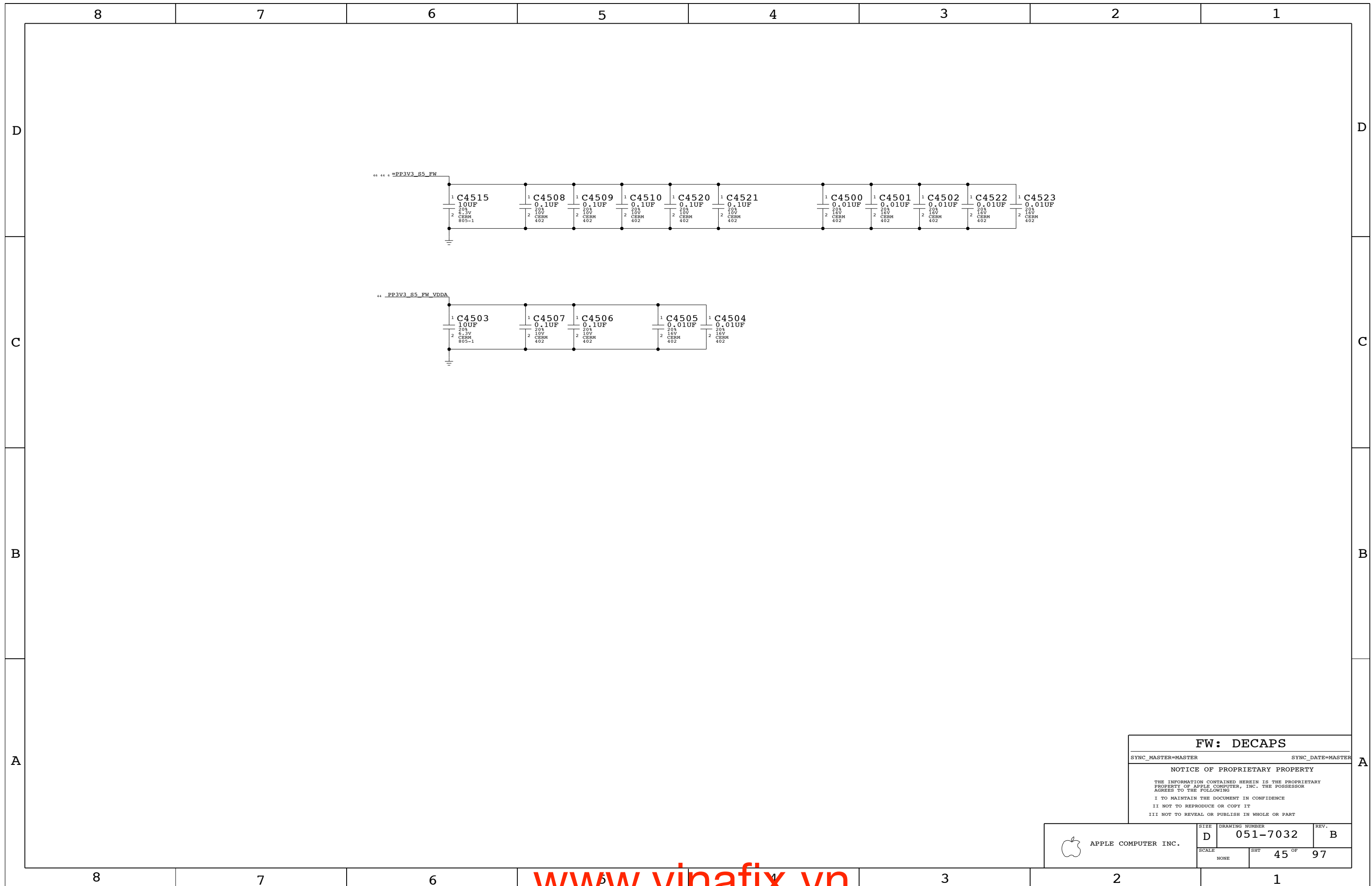
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	43 OF 97	
NONE			



NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	44 OF 97	
NONE			



FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

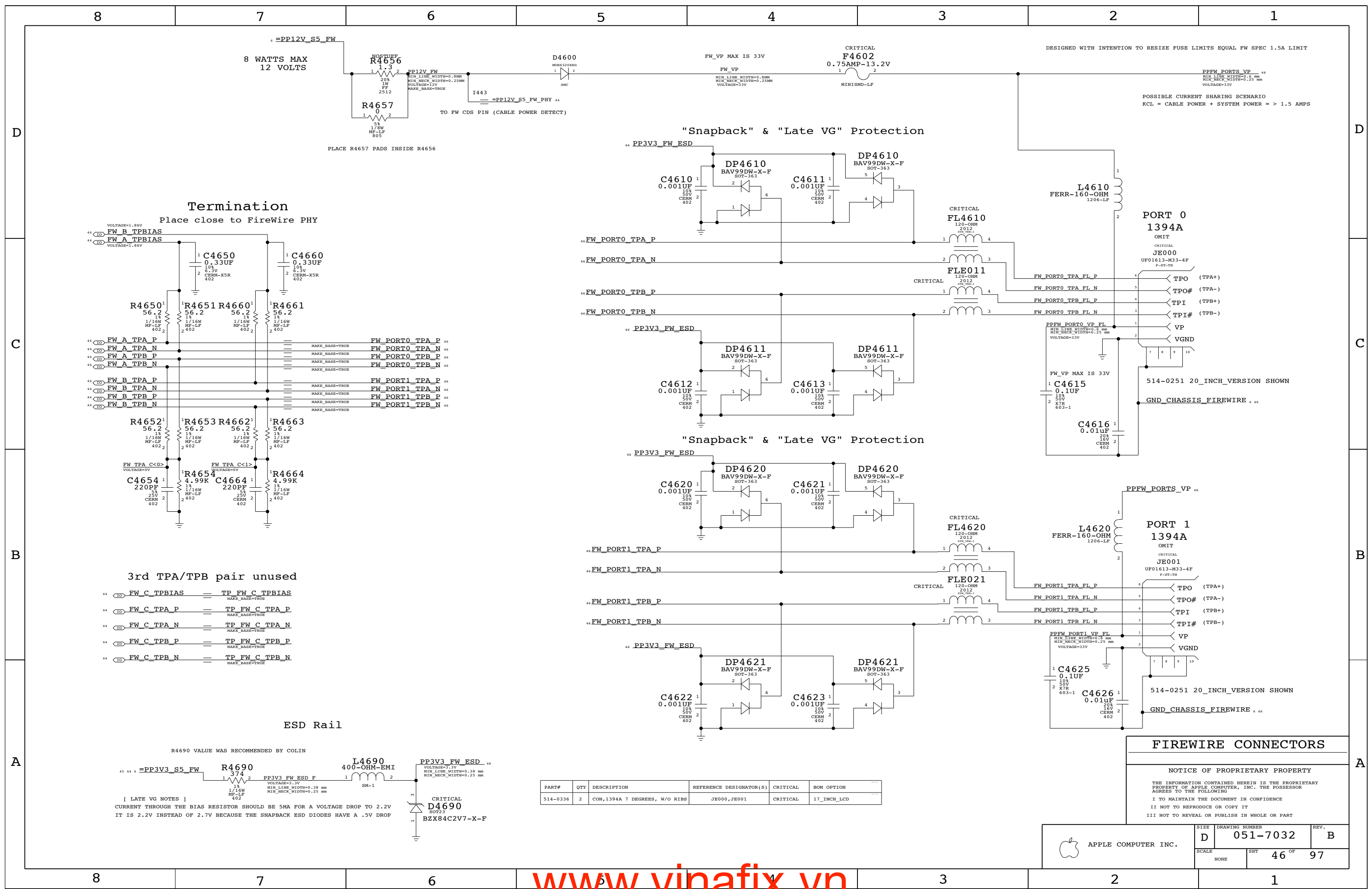
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 45 OF 97	



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

ESD Rail

FIREWIRE CONNECTORS

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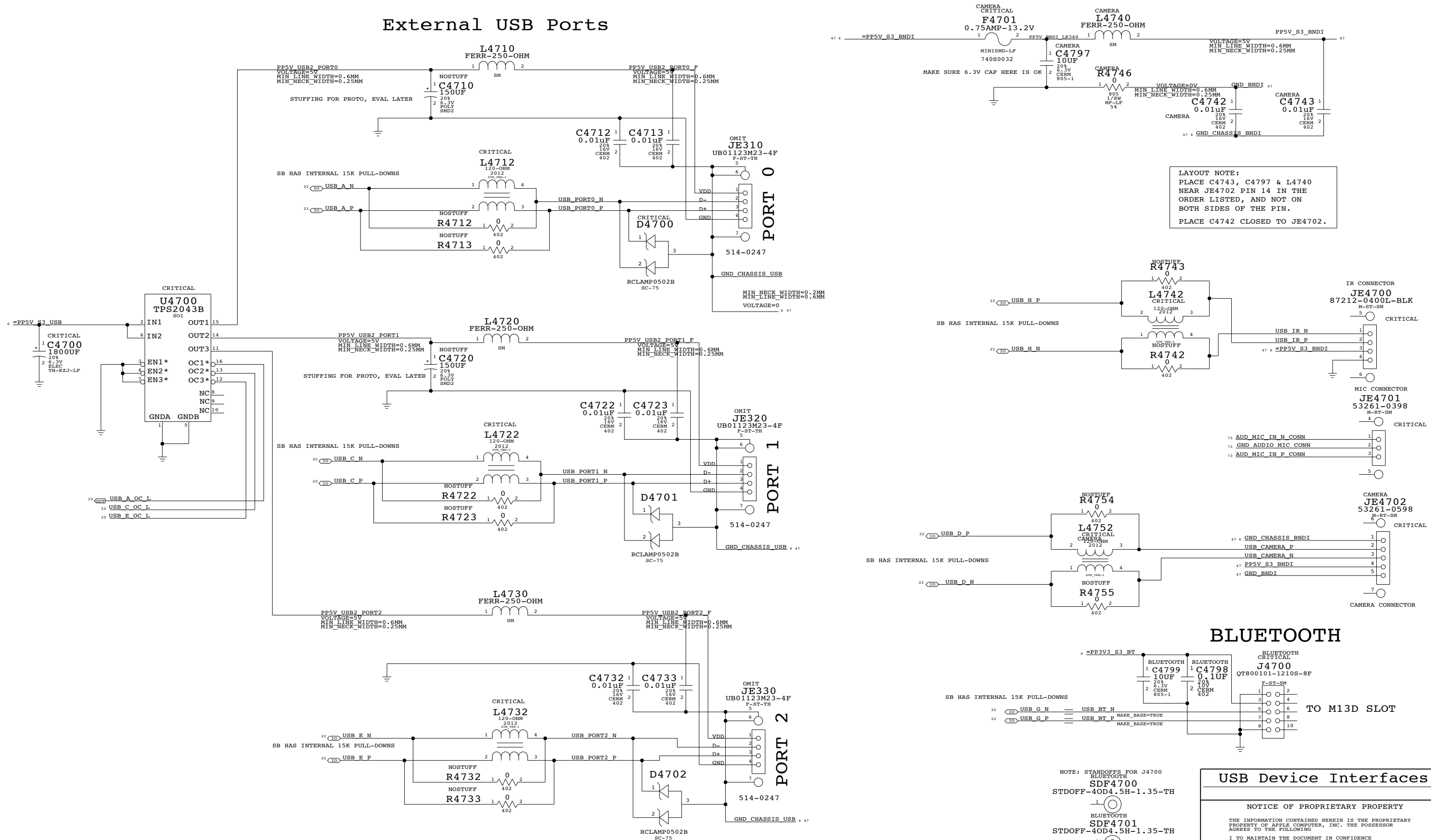
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON, 1394A 7 DEGREES, W/O RIBS	JE000, JE001	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.

SIZE: D DRAWING NUMBER: 051-7032 REV. B

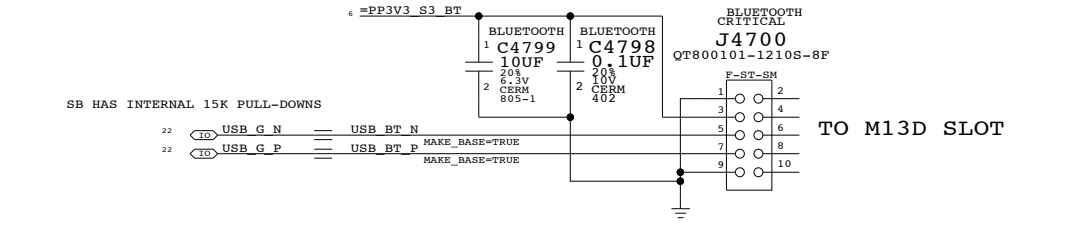
SCALE: NONE SHT: 46 OF 97

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE4702 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE4702.

BLUETOOTH



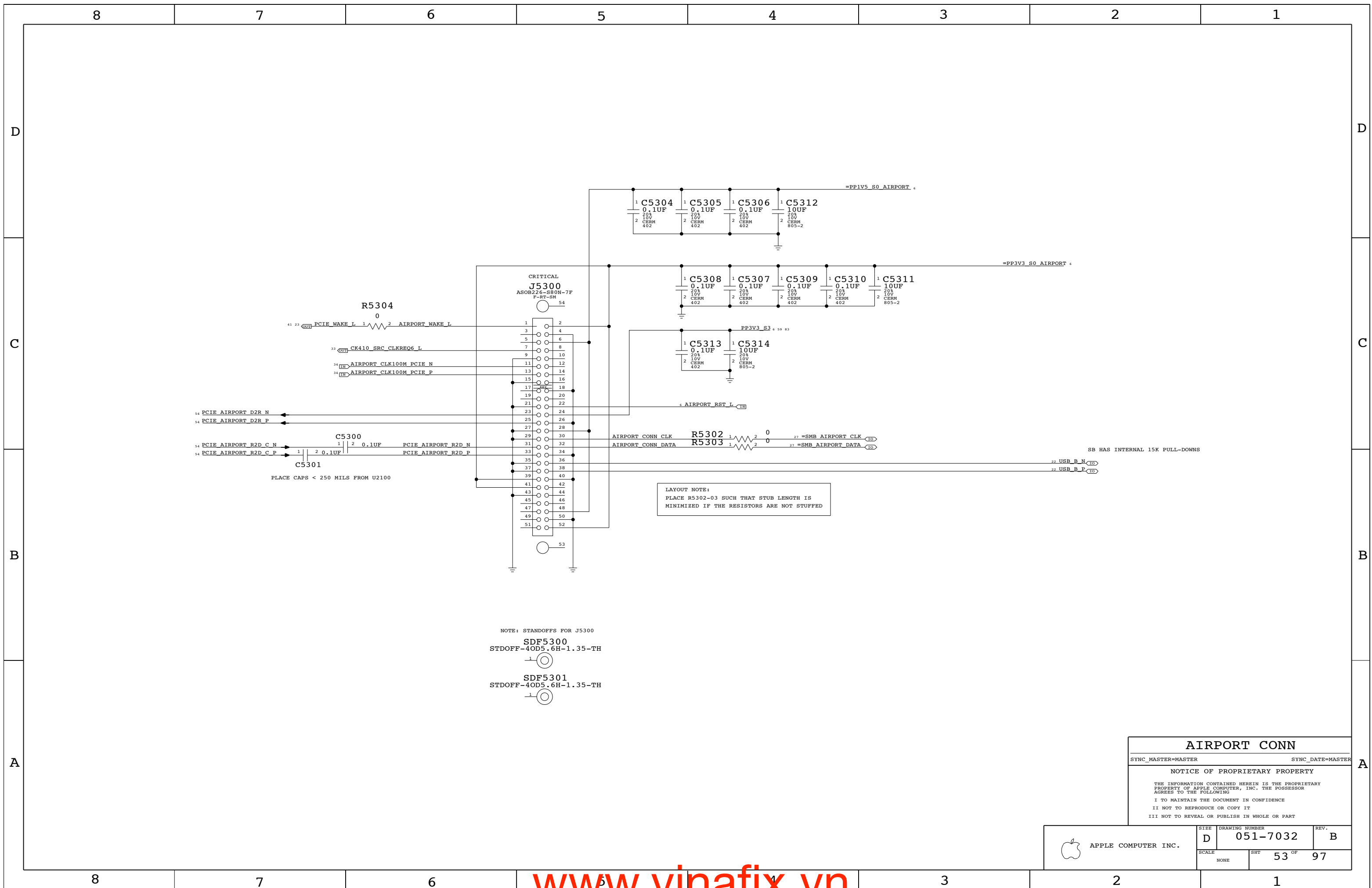
NOTE: STANDOFFS FOR J4700
 BLUETOOTH
SDF4700
 STDOFF-40D4.5H-1.35-TH
 BLUETOOTH
SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	47 OF	97
NONE			



R5304
0

41 23 PCIE_WAKE L 1 2 AIRPORT_WAKE L

32 CK410_SRC_CLKREQ6 L

34 AIRPORT_CLK100M_PCIE N

34 AIRPORT_CLK100M_PCIE P

54 PCIE_AIRPORT_D2R_N

54 PCIE_AIRPORT_D2R_P

54 PCIE_AIRPORT_R2D_C_N

54 PCIE_AIRPORT_R2D_C_P

C5300 1 2 0.1UF PCIE_AIRPORT_R2D_N PCIE_AIRPORT_R2D_P

C5301

PLACE CAPS < 250 MILS FROM U2100

LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300

SDF5300
STDOFF-40D5.6H-1.35-TH



SDF5301
STDOFF-40D5.6H-1.35-TH



SB HAS INTERNAL 15K PULL-DOWNS

22 USB_B_N
22 USB_B_P

AIRPORT CONN
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT		OF
NONE	53		97

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 IN PCIE_C_R2D_C_N == TP PCIE_C_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_C_R2D_C_P == TP PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N == TP PCIE_C_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_P == TP PCIE_C_D2R_P
MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N == TP PCIE_D_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_P == TP PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N == TP PCIE_D_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_P == TP PCIE_D_D2R_P
MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N == TP PCIE_E_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_P == TP PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N == TP PCIE_E_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_P == TP PCIE_E_D2R_P
MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N == TP PCIE_F_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_P == TP PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N == TP PCIE_F_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_P == TP PCIE_F_D2R_P
MAKE_BASE=TRUE

USED PCIE PORTS

22 IN PCIE_A_R2D_C_N == PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE

22 IN PCIE_A_R2D_C_P == PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 OUT PCIE_A_D2R_N == PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE

22 5 OUT PCIE_A_D2R_P == PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE


22 IN PCIE_B_R2D_C_N == PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE

22 IN PCIE_B_R2D_C_P == PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 5 OUT PCIE_B_D2R_N == PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE

22 5 OUT PCIE_B_D2R_P == PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES			
SYNC_MASTER=MASTER		SYNC_DATE=MASTER	
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHT 54 OF 97	

8

7

6

5

4

3

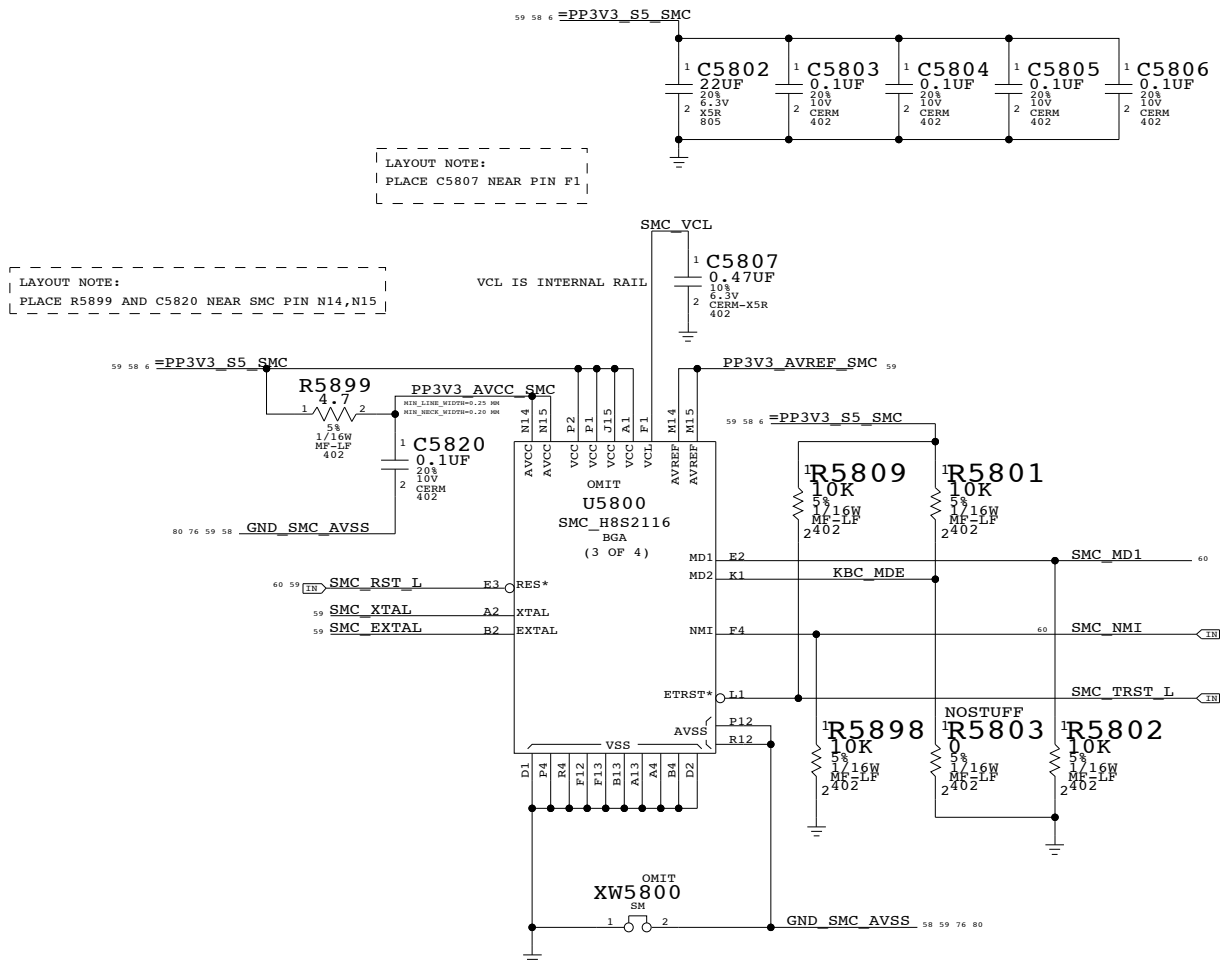
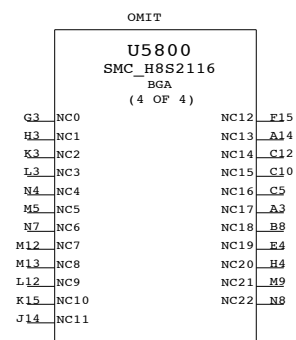
2

1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

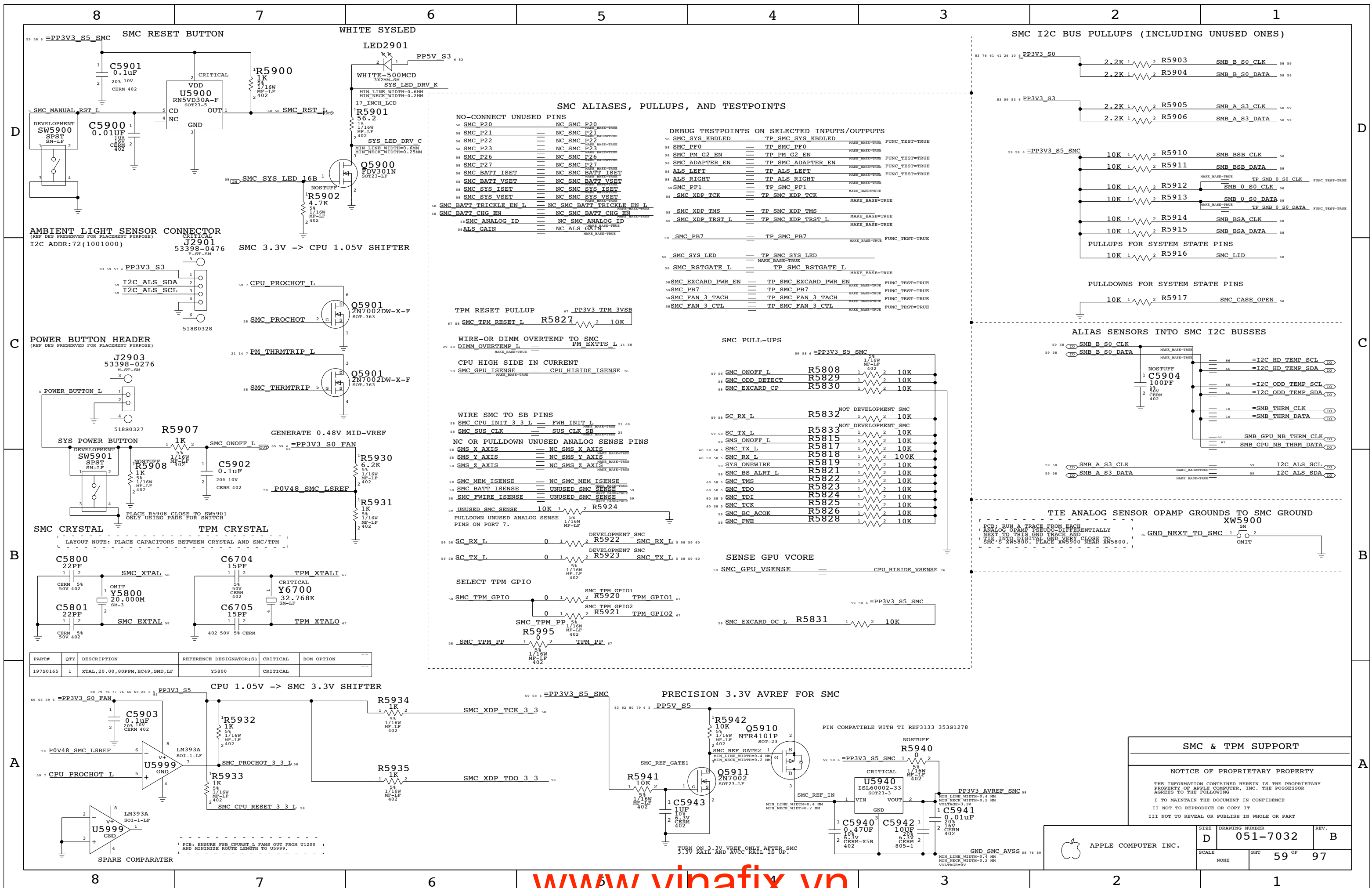
OMIT U5800 SMC_H8S2116 (1 OF 4)			OMIT U5800 SMC_H8S2116 (2 OF 4)		
P10	B12	PM LAN_ENABLE	P10	B12	PM LAN_ENABLE
P11	C13	SMC_RSTGATE_L	P11	C13	SMC_RSTGATE_L
P12	A15	ALL_SYS_PWRGD	P12	A15	ALL_SYS_PWRGD
P13	B14	RSMRST_PWRGD	P13	B14	RSMRST_PWRGD
P14	B15	SMC_SB_NMI	P14	B15	SMC_SB_NMI
P15	C14	PM_RSMRST_L	P15	C14	PM_RSMRST_L
P16	D12	IMVP_VR_ON	P16	D12	IMVP_VR_ON
P17	C15	PM_PWRBTN_L	P17	C15	PM_PWRBTN_L
P20	D13	SMC_P20	P20	D13	SMC_P20
P21	D14	SMC_P21	P21	D14	SMC_P21
P22	D15	SMC_P22	P22	D15	SMC_P22
P23	E12	SMC_P23	P23	E12	SMC_P23
P24	E14	SMC_BATT_TRICKLE_EN_L	P24	E14	SMC_BATT_TRICKLE_EN_L
P25	E15	SMC_BATT_CHG_EN	P25	E15	SMC_BATT_CHG_EN
P26	E13	SMC_P26	P26	E13	SMC_P26
P27	F14	SMC_P27	P27	F14	SMC_P27
P30	D9	LPC_AD<0>	P30	D9	LPC_AD<0>
P31	C9	LPC_AD<1>	P31	C9	LPC_AD<1>
P32	A9	LPC_AD<2>	P32	A9	LPC_AD<2>
P33	B9	LPC_AD<3>	P33	B9	LPC_AD<3>
P34	D8	LPC_FRAME_L	P34	D8	LPC_FRAME_L
P35	C8	SMC_LRESET_L	P35	C8	SMC_LRESET_L
P36	A8	PCI_CLK_SMC	P36	A8	PCI_CLK_SMC
P37	D7	INT_SERIRQ	P37	D7	INT_SERIRQ
P40	A5	SMC_XDP_TMS	P40	A5	SMC_XDP_TMS
P41	B5	SMC_SYS_LED_16B	P41	B5	SMC_SYS_LED_16B
P42	D5	SMB_BSB_DATA	P42	D5	SMB_BSB_DATA
P43	C3	SMC_TPM_PP	P43	C3	SMC_TPM_PP
P44	B1	SMC_XDP_TRST_L	P44	B1	SMC_XDP_TRST_L
P45	C2	SMC_XDP_TCK	P45	C2	SMC_XDP_TCK
P46	D3	SMC_SYS_LED	P46	D3	SMC_SYS_LED
P47	C1	SMC_SYS_KBDLED	P47	C1	SMC_SYS_KBDLED
P50	G1	SMC_TX_L	P50	G1	SMC_TX_L
P51	G4	SMC_RX_L	P51	G4	SMC_RX_L
P52	F2	SMB_0_S0_CLK	P52	F2	SMB_0_S0_CLK
P60	L13	SMC_PM_G2_EN	P60	L13	SMC_PM_G2_EN
P61	L14	SMC_ADAPTER_EN	P61	L14	SMC_ADAPTER_EN
P62	L15	SPI_ARB	P62	L15	SPI_ARB
P63	K12	SPI_SCLK	P63	K12	SPI_SCLK
P64	K13	SPI_SI	P64	K13	SPI_SI
P65	K14	SPI_SO	P65	K14	SPI_SO
P66	J12	SMC_PROCHOT_3_3_L	P66	J12	SMC_PROCHOT_3_3_L
P67	J13	SMC_CPU_INIT_3_3_L	P67	J13	SMC_CPU_INIT_3_3_L
P70	N12	SMC_CPU_ISENSE	P70	N12	SMC_CPU_ISENSE
P71	R13	SMC_CPU_VSENSE	P71	R13	SMC_CPU_VSENSE
P72	P13	SMC_GPU_ISENSE	P72	P13	SMC_GPU_ISENSE
P73	R14	SMC_GPU_VSENSE	P73	R14	SMC_GPU_VSENSE
P74	P14	SMC_DCIN_ISENSE	P74	P14	SMC_DCIN_ISENSE
P75	R15	SMC_PBUS_VSENSE	P75	R15	SMC_PBUS_VSENSE
P76	N13	SMC_BATT_ISENSE	P76	N13	SMC_BATT_ISENSE
P77	P15	SMC_FWIRE_ISENSE	P77	P15	SMC_FWIRE_ISENSE
P80	C7	SMC_SMC_SCI_L	P80	C7	SMC_SMC_SCI_L
P81	A7	SMC_TPM_GPIO	P81	A7	SMC_TPM_GPIO
P82	B7	PM_CLKRUN_L	P82	B7	PM_CLKRUN_L
P83	D6	PM_SUS_STAT_L	P83	D6	PM_SUS_STAT_L
P84	C6	SC_TX_L	P84	C6	SC_TX_L
P85	A6	SMC_RX_L	P85	A6	SMC_RX_L
P86	B6	SMB_BSB_CLK	P86	B6	SMB_BSB_CLK
P90	K4	SMC_ONOFF_L	P90	K4	SMC_ONOFF_L
P91	J2	SMC_BC_ACOK	P91	J2	SMC_BC_ACOK
P92	J1	SMC_BS_ALARM_L	P92	J1	SMC_BS_ALARM_L
P93	J3	PM_SLP_S3_L	P93	J3	PM_SLP_S3_L
P94	J4	PM_SLP_S4_L	P94	J4	PM_SLP_S4_L
P95	H2	PM_SLP_S5_L	P95	H2	PM_SLP_S5_L
P96	H1	SMC_SUS_CLK	P96	H1	SMC_SUS_CLK
P97	G2	SMB_0_S0_DATA	P97	G2	SMB_0_S0_DATA

OMIT U5800 SMC_H8S2116 (3 OF 4)			OMIT U5800 SMC_H8S2116 (4 OF 4)		
P21	R3	SMC_RCIN_L	P21	R3	SMC_RCIN_L
P22	P3	BOOT_LPC_SPI_L	P22	P3	BOOT_LPC_SPI_L
P23	R2	PM_SYSRST_L	P23	R2	PM_SYSRST_L
P24	N3	SMC_TPM_RESET_L	P24	N3	SMC_TPM_RESET_L
P25	R1	PM_EXTTTS_L	P25	R1	PM_EXTTTS_L
P26	N2	PM_THRM_L	P26	N2	PM_THRM_L
P27	M4	SYS_ONEWIRE	P27	M4	SYS_ONEWIRE
P28	N1	PM_BATLOW_L	P28	N1	PM_BATLOW_L
P30	B10	SMC_EXTSMI_L	P30	B10	SMC_EXTSMI_L
P31	A10	SMC_RUNTIME_SCI_L	P31	A10	SMC_RUNTIME_SCI_L
P32	D10	SMC_ODD_DETECT	P32	D10	SMC_ODD_DETECT
P33	A11	ISENSE_CAL_EN	P33	A11	ISENSE_CAL_EN
P34	B11	SMC_EXCARD_CP	P34	B11	SMC_EXCARD_CP
P35	C11	SMC_EXCARD_PWR_EN	P35	C11	SMC_EXCARD_PWR_EN
P36	B6	SMC_EXCARD_OC_L	P36	B6	SMC_EXCARD_OC_L
P37	D11	SMC_XDP_TDO_3_3	P37	D11	SMC_XDP_TDO_3_3
P40	G14	SMC_FAN_0_CTL	P40	G14	SMC_FAN_0_CTL
P41	G15	SMC_FAN_1_CTL	P41	G15	SMC_FAN_1_CTL
P42	G13	SMC_FAN_2_CTL	P42	G13	SMC_FAN_2_CTL
P43	G12	SMC_FAN_3_CTL	P43	G12	SMC_FAN_3_CTL
P44	H14	SMC_FAN_0_TACH	P44	H14	SMC_FAN_0_TACH
P45	H15	SMC_FAN_1_TACH	P45	H15	SMC_FAN_1_TACH
P46	H13	SMC_FAN_2_TACH	P46	H13	SMC_FAN_2_TACH
P47	H12	SMC_FAN_3_TACH	P47	H12	SMC_FAN_3_TACH
P50	M11	SMS_X_AXIS	P50	M11	SMS_X_AXIS
P51	P11	SMS_Y_AXIS	P51	P11	SMS_Y_AXIS
P52	R11	SMS_Z_AXIS	P52	R11	SMS_Z_AXIS
P53	N11	SMC_ANALOG_ID	P53	N11	SMC_ANALOG_ID
P54	P10	SMC_NB_ISENSE	P54	P10	SMC_NB_ISENSE
P55	R10	SMC_MEM_ISENSE	P55	R10	SMC_MEM_ISENSE
P56	N10	ALS_LEFT	P56	N10	ALS_LEFT
P57	M10	ALS_RIGHT	P57	M10	ALS_RIGHT
P60	M3	SMC_CASE_OPEN	P60	M3	SMC_CASE_OPEN
P61	M2	SMC_TCK	P61	M2	SMC_TCK
P62	M1	SMC_TDI	P62	M1	SMC_TDI
P63	L4	SMC_TDO	P63	L4	SMC_TDO
P64	L2	SMC_TMS	P64	L2	SMC_TMS
P66	M7	SMC_PF0	P66	M7	SMC_PF0
P67	P6	SMC_PF1	P67	P6	SMC_PF1
P68	R6	SMC_LID	P68	R6	SMC_LID
P69	N6	SMC_CPU_RESET_3_3_L	P69	N6	SMC_CPU_RESET_3_3_L
P70	M6	SMC_BATT_ISET	P70	M6	SMC_BATT_ISET
P71	R5	SMC_BATT_VSET	P71	R5	SMC_BATT_VSET
P72	P5	SMC_SYS_ISET	P72	P5	SMC_SYS_ISET
P73	N5	SMC_SYS_VSET	P73	N5	SMC_SYS_VSET
P74	R9	SPI_CE_L	P74	R9	SPI_CE_L
P75	R9	SMC_XDP_TCK_3_3	P75	R9	SMC_XDP_TCK_3_3
P76	N9	SMB_BSA_DATA	P76	N9	SMB_BSA_DATA
P77	P8	SMB_BSA_CLK	P77	P8	SMB_BSA_CLK
P78	H8	SMB_A_S3_DATA	P78	H8	SMB_A_S3_DATA
P79	P7	SMB_A_S3_CLK	P79	P7	SMB_A_S3_CLK
P80	R7	SMB_B_S0_DATA	P80	R7	SMB_B_S0_DATA
P81	R7	SMB_B_S0_CLK	P81	R7	SMB_B_S0_CLK
P82	R1	SMC_PROCHOT	P82	R1	SMC_PROCHOT
P83	E3	SMC_THRMTRIP	P83	E3	SMC_THRMTRIP
P84	K2	SMC_FWE	P84	K2	SMC_FWE
P85	C4	ALS_GAIN	P85	C4	ALS_GAIN
P86	D4	SMS_INT_L	P86	D4	SMS_INT_L
P87	B3	SMC_ONOFF_L	P87	B3	SMC_ONOFF_L



SMC
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	D	051-7032	B
SCALE	SHT	58 OF	97
NONE			



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC_P22 == TP_SMC_P22 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC_P23 == TP_SMC_P23 MAKE_BASE=TRUE
58 SMC P23 == NC SMC P23	58 SMC_P26 == TP_SMC_P26 MAKE_BASE=TRUE
58 SMC P26 == NC SMC P26	58 SMC_P27 == TP_SMC_P27 MAKE_BASE=TRUE
58 SMC P27 == NC SMC P27	58 SMC_BATT_ISET == NC_SMC_BATT_ISET MAKE_BASE=TRUE
58 SMC_BATT_ISET == NC_SMC_BATT_ISET	58 SMC_BATT_VSET == NC_SMC_BATT_VSET MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC_SMC_BATT_VSET	58 SMC_SYS_ISET == NC_SMC_SYS_ISET MAKE_BASE=TRUE
58 SMC_SYS_ISET == NC_SMC_SYS_ISET	58 SMC_SYS_VSET == NC_SMC_SYS_VSET MAKE_BASE=TRUE
58 SMC_SYS_VSET == NC_SMC_SYS_VSET	58 SMC_XDP_TCK == TP_SMC_XDP_TCK MAKE_BASE=TRUE
58 SMC_BATT_TRICKLE_EN_L == NC_SMC_BATT_TRICKLE_EN_L	58 SMC_XDP_TMS == TP_SMC_XDP_TMS MAKE_BASE=TRUE
58 SMC_BATT_CHG_EN == NC_SMC_BATT_CHG_EN	58 SMC_XDP_TRST_L == TP_SMC_XDP_TRST_L MAKE_BASE=TRUE
58 SMC_ANALOG_ID == NC_SMC_ANALOG_ID	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 ALS_GAIN == NC_ALS_GAIN MAKE_BASE=TRUE	58 SMC_SYS_LED == TP_SMC_SYS_LED MAKE_BASE=TRUE
	58 SMC_RSTGATE_L == TP_SMC_RSTGATE_L MAKE_BASE=TRUE
	58 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL MAKE_BASE=TRUE FUNC_TEST=TRUE

SMC PULL-UPS

58 SMC_ONOFF_L	R5808	10K
58 SMC_ODD_DETECT	R5829	10K
58 SMC_EXCARD_CP	R5830	10K
58 SC_RX_L	R5832	10K
58 SC_TX_L	R5833	10K
58 SMS_ONOFF_L	R5815	10K
58 SMC_TX_L	R5817	10K
58 SMC_RX_L	R5818	100K
58 SYS_ONEWIRE	R5819	10K
58 SMC_BS_ALRT_L	R5821	10K
58 SMC_TMS	R5822	10K
58 SMC_TDO	R5823	10K
58 SMC_TDI	R5824	10K
58 SMC_TCK	R5825	10K
58 SMC_BC_ACOK	R5826	10K
58 SMC_FWE	R5828	10K

WIRE SMC TO SB PINS

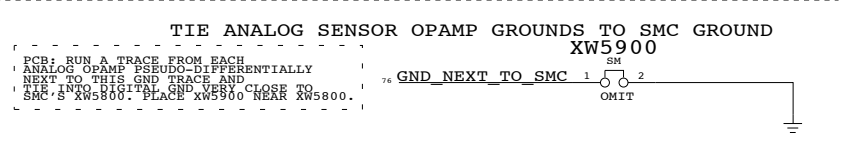
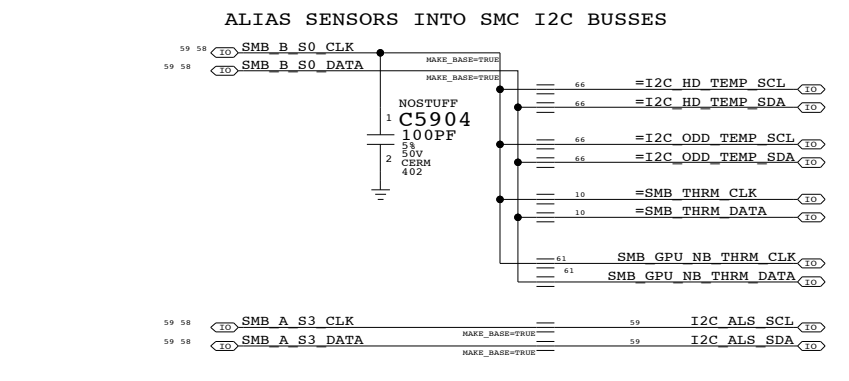
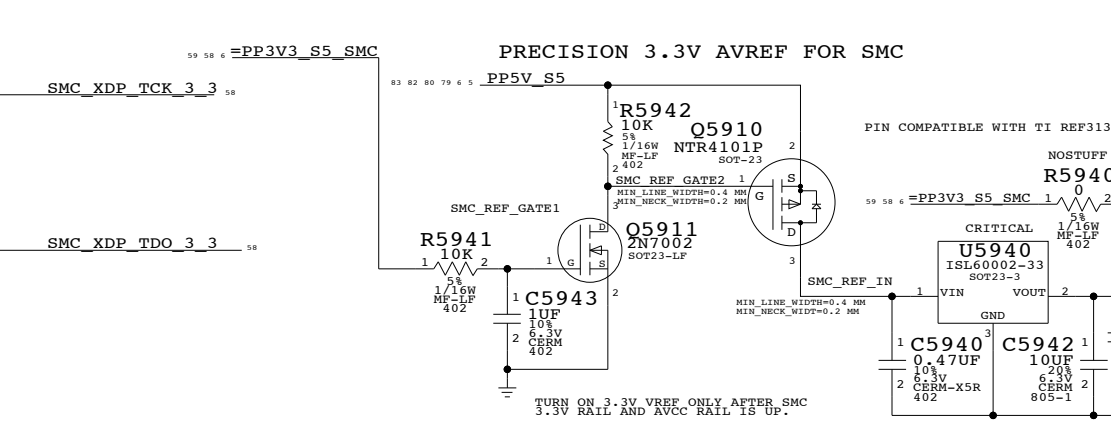
58 SMC_CPU_INIT_3_3_L	FWH_INIT_L	21
58 SMC_SUS_CLK	SUS_CLK_SB	23
58 SMS_X_AXIS	NC_SMS_X_AXIS	
58 SMS_Y_AXIS	NC_SMS_Y_AXIS	
58 SMS_Z_AXIS	NC_SMS_Z_AXIS	

SELECT TPM GPIO

58 SMC_TPM_GPIO	SMC_TPM_GPIO1	TPM_GPIO1
	SMC_TPM_GPIO2	TPM_GPIO2
58 SMC_TPM_PP	R5995	TPM_PP

SMC CRystal

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19780165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	



SMC & TPM SUPPORT

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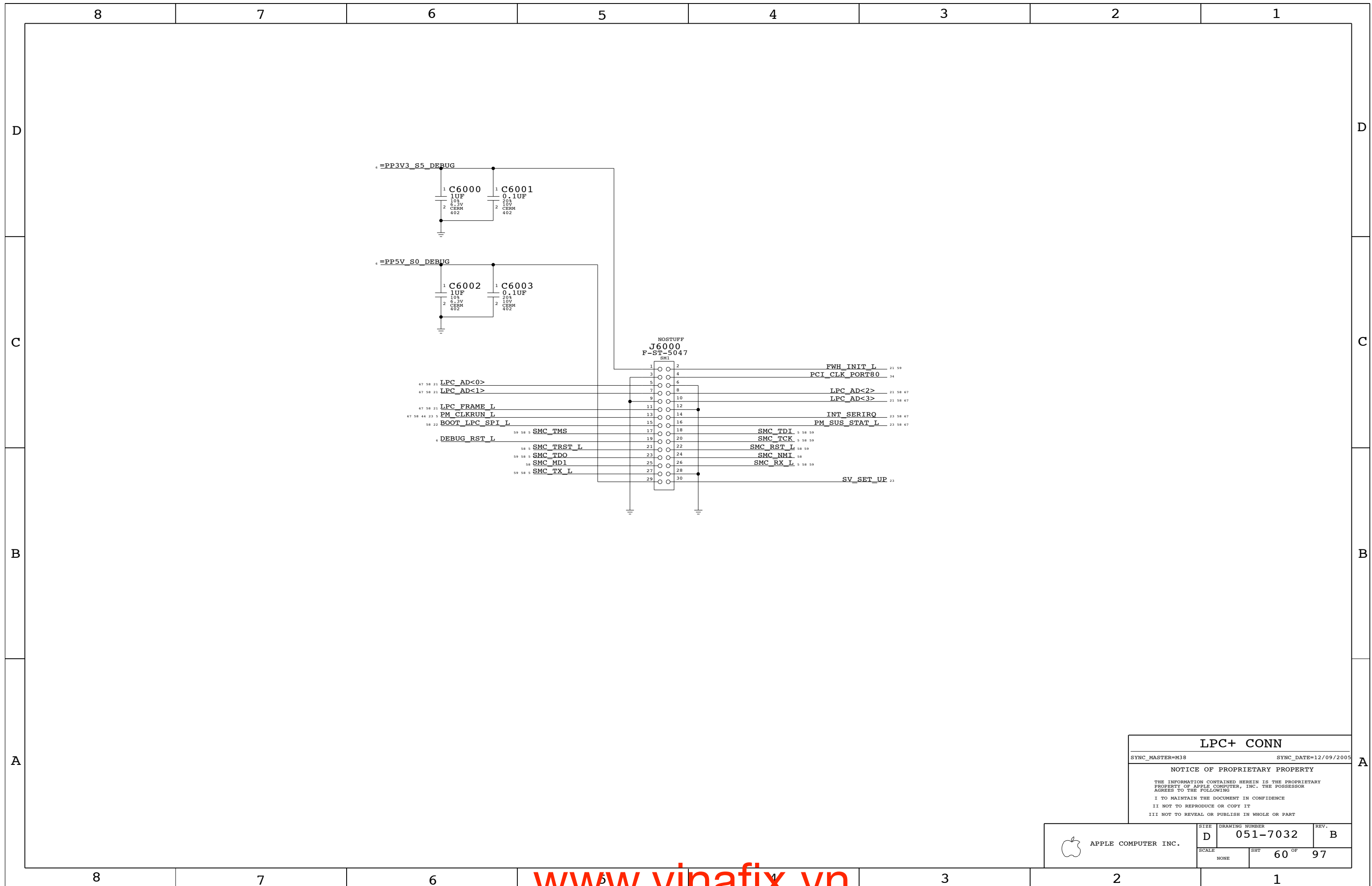
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SIZE	DRAWING NUMBER	REV.
D	051-7032	B
SCALE	SHT	59 OF 97
NONE		

APPLE COMPUTER INC.



LPC+ CONN

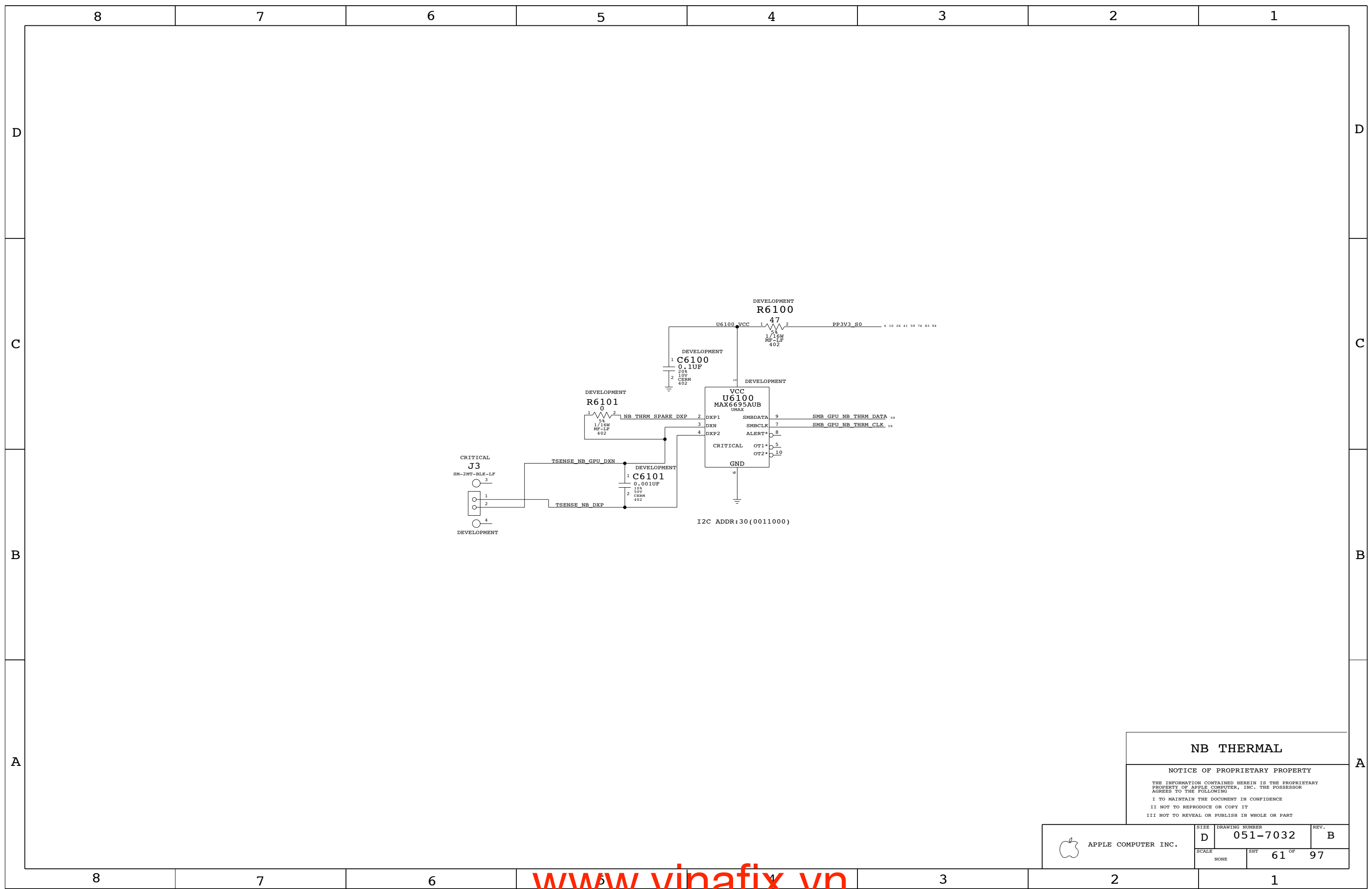
SYNC_MASTER=M38 SYNC_DATE=12/09/2005

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	SCALE NONE	SHEET 60 OF 97	



NB THERMAL

NOTICE OF PROPRIETARY PROPERTY

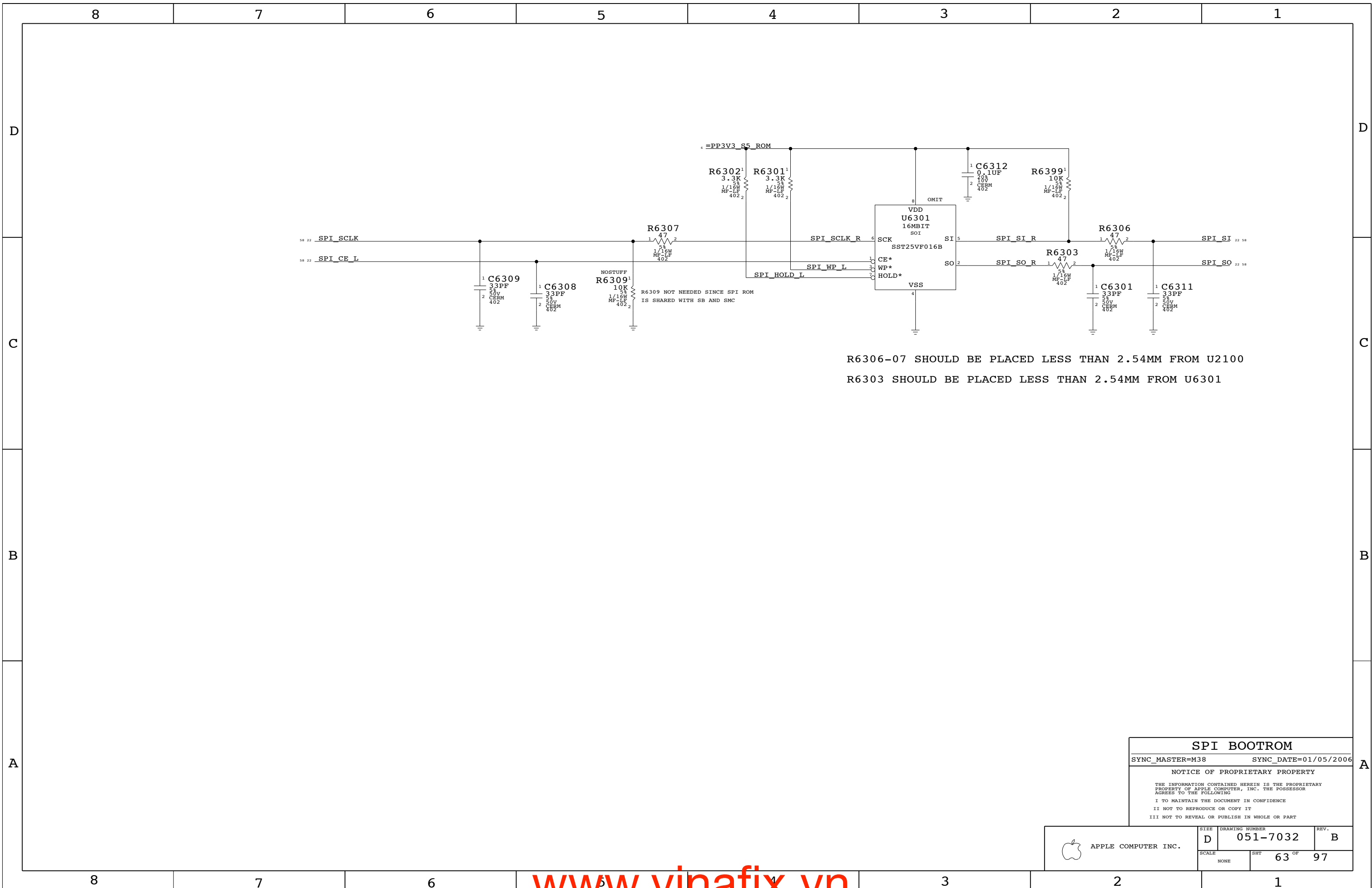
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 61 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

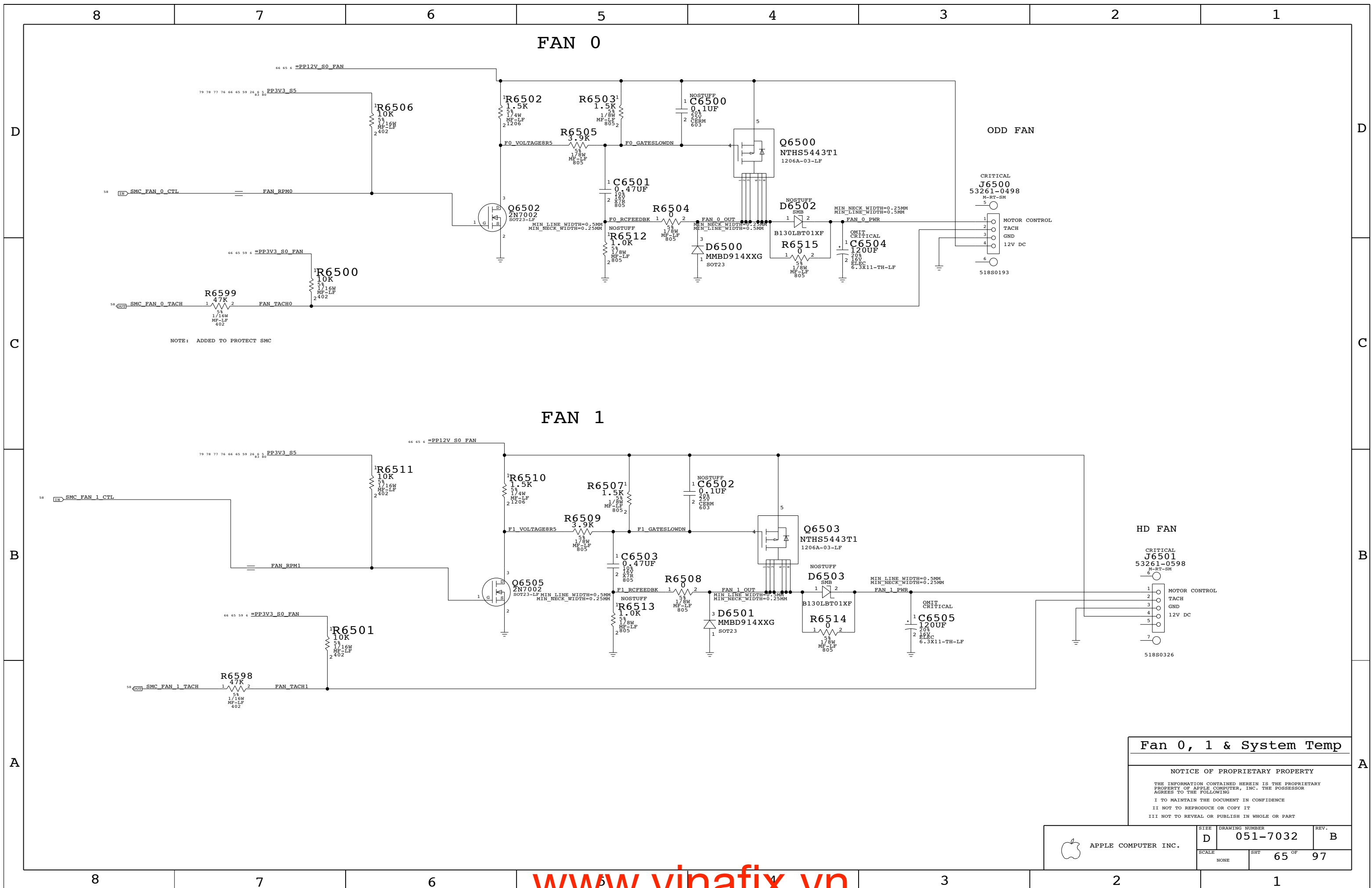
SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 63 OF 97	

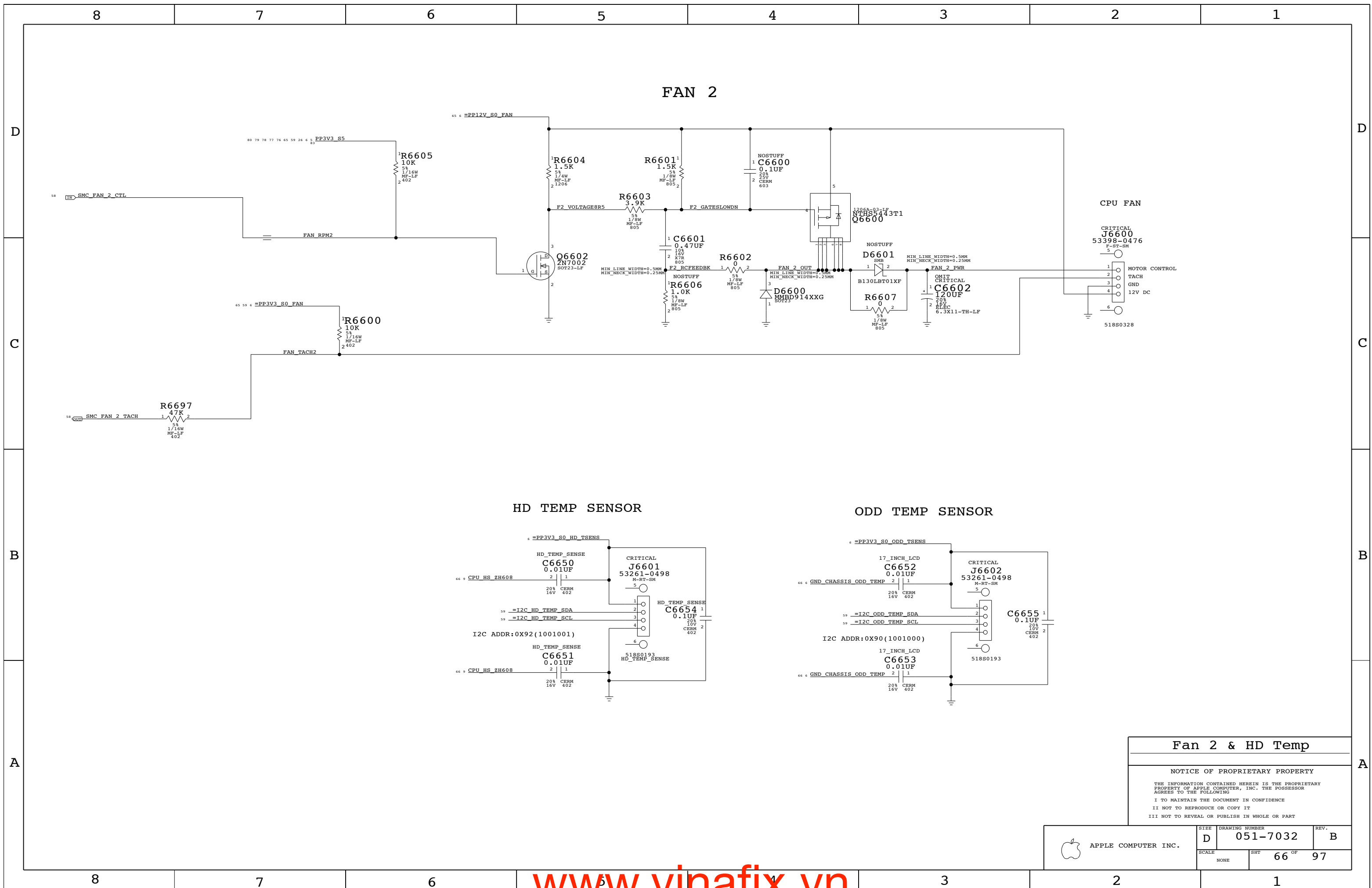


NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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	D	051-7032	B
SCALE	SHT	65 OF 97	
NONE			



FAN 2

HD TEMP SENSOR

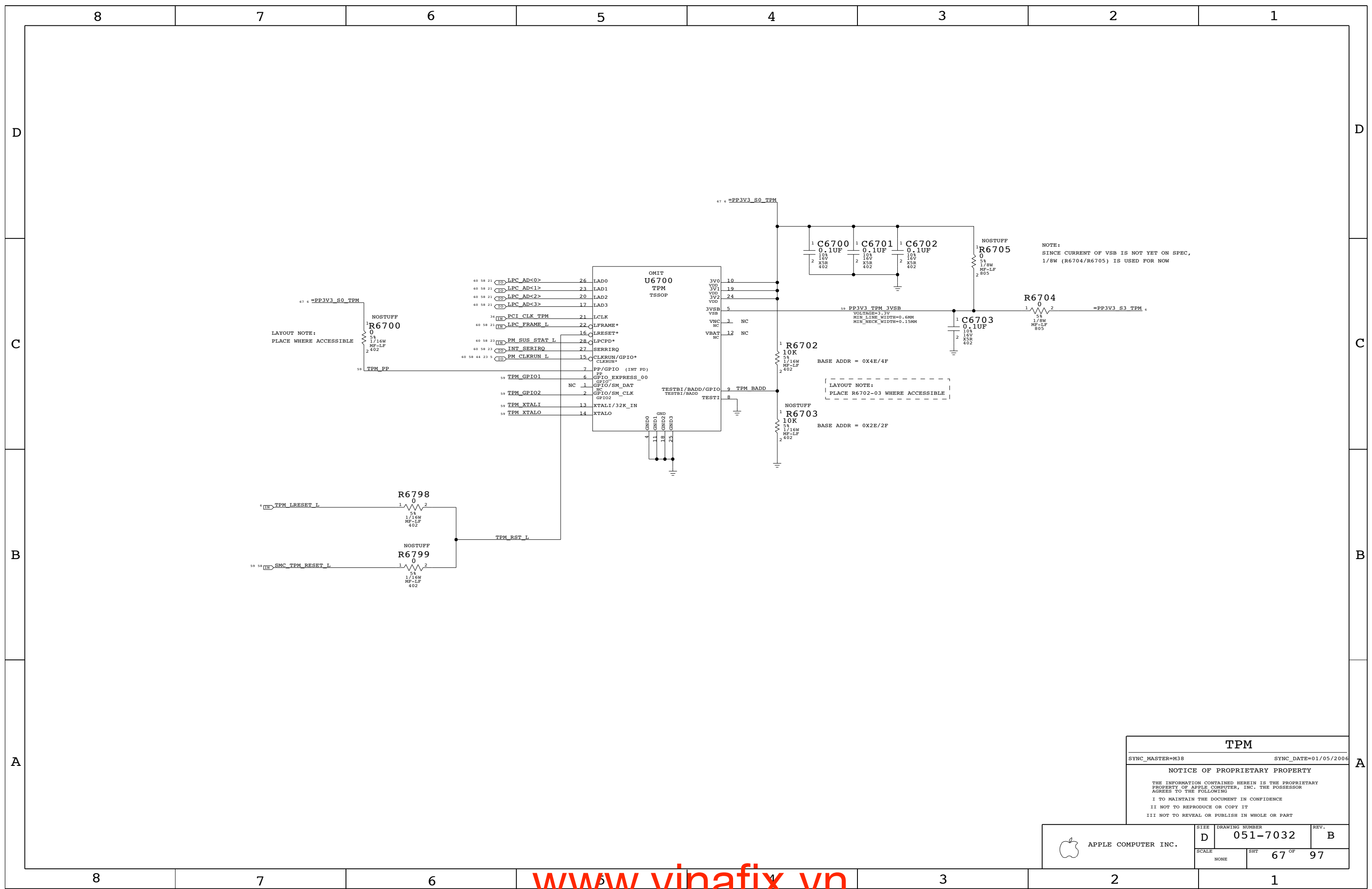
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
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LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

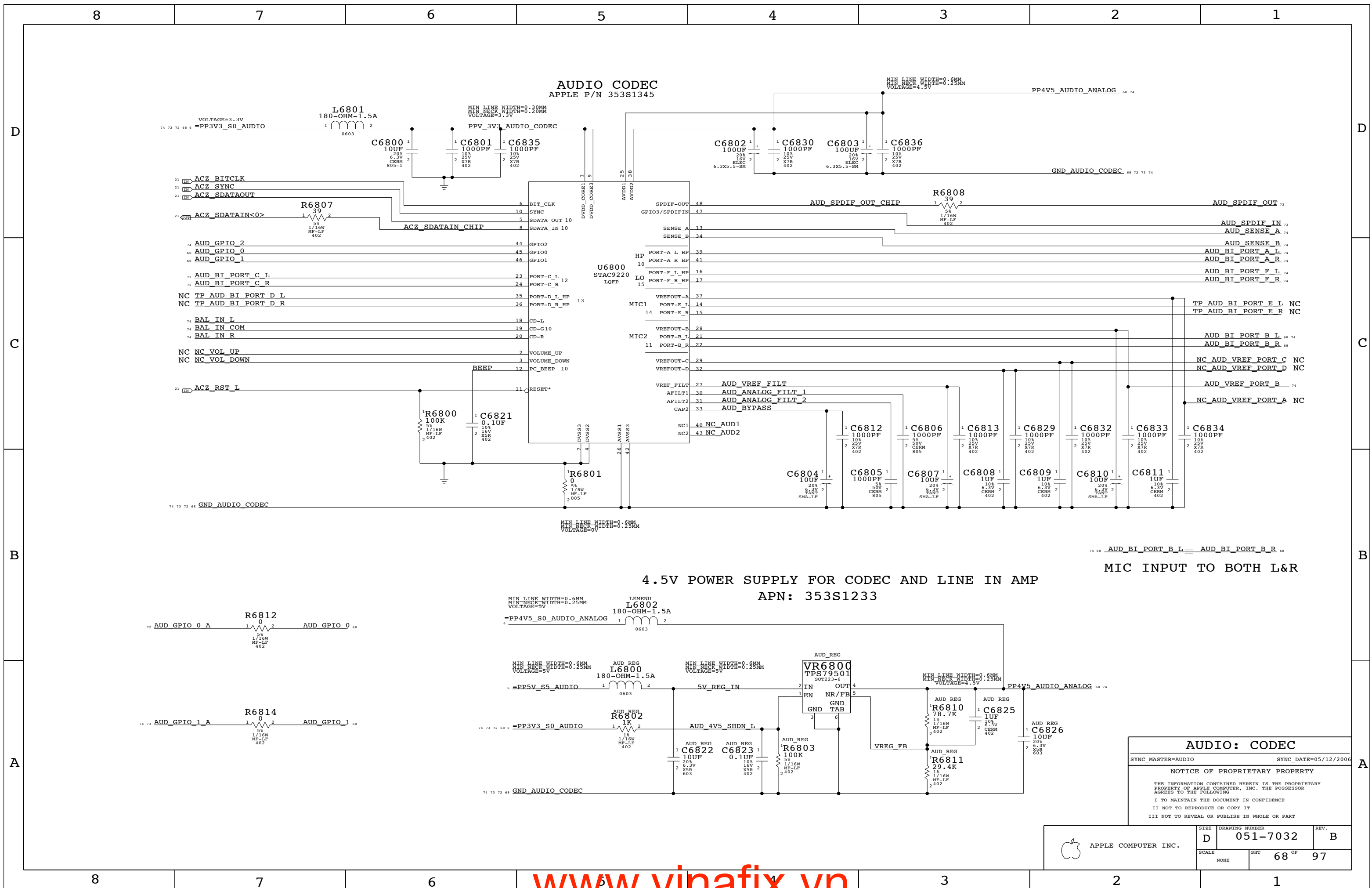
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	SCALE NONE	SHT 67 OF 97	

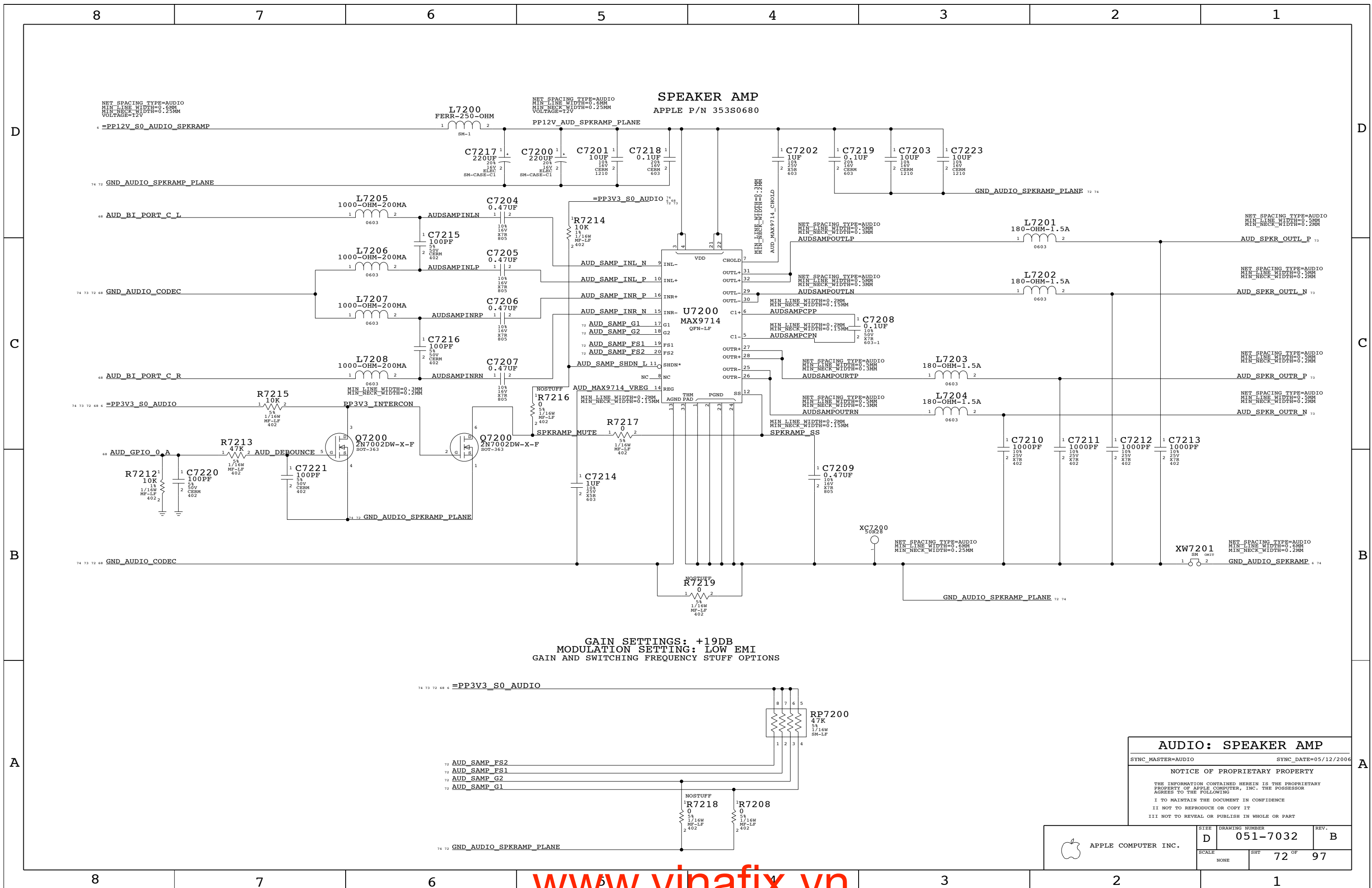


AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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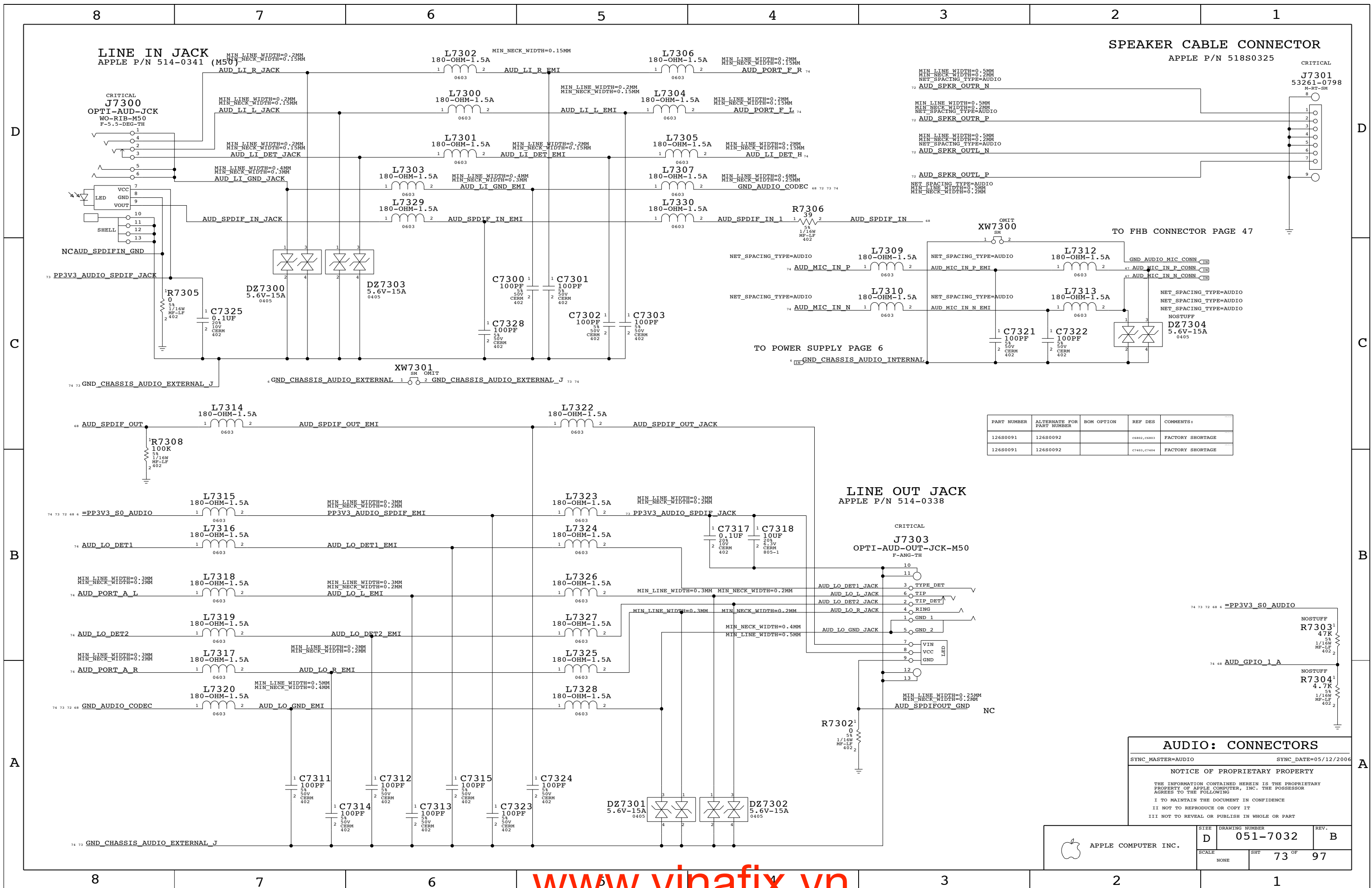
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 68 OF 97	



GAIN SETTINGS: +19DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	72 OF	97
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7483, C7484	FACTORY SHORTAGE

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

NOTICE OF PROPRIETARY PROPERTY

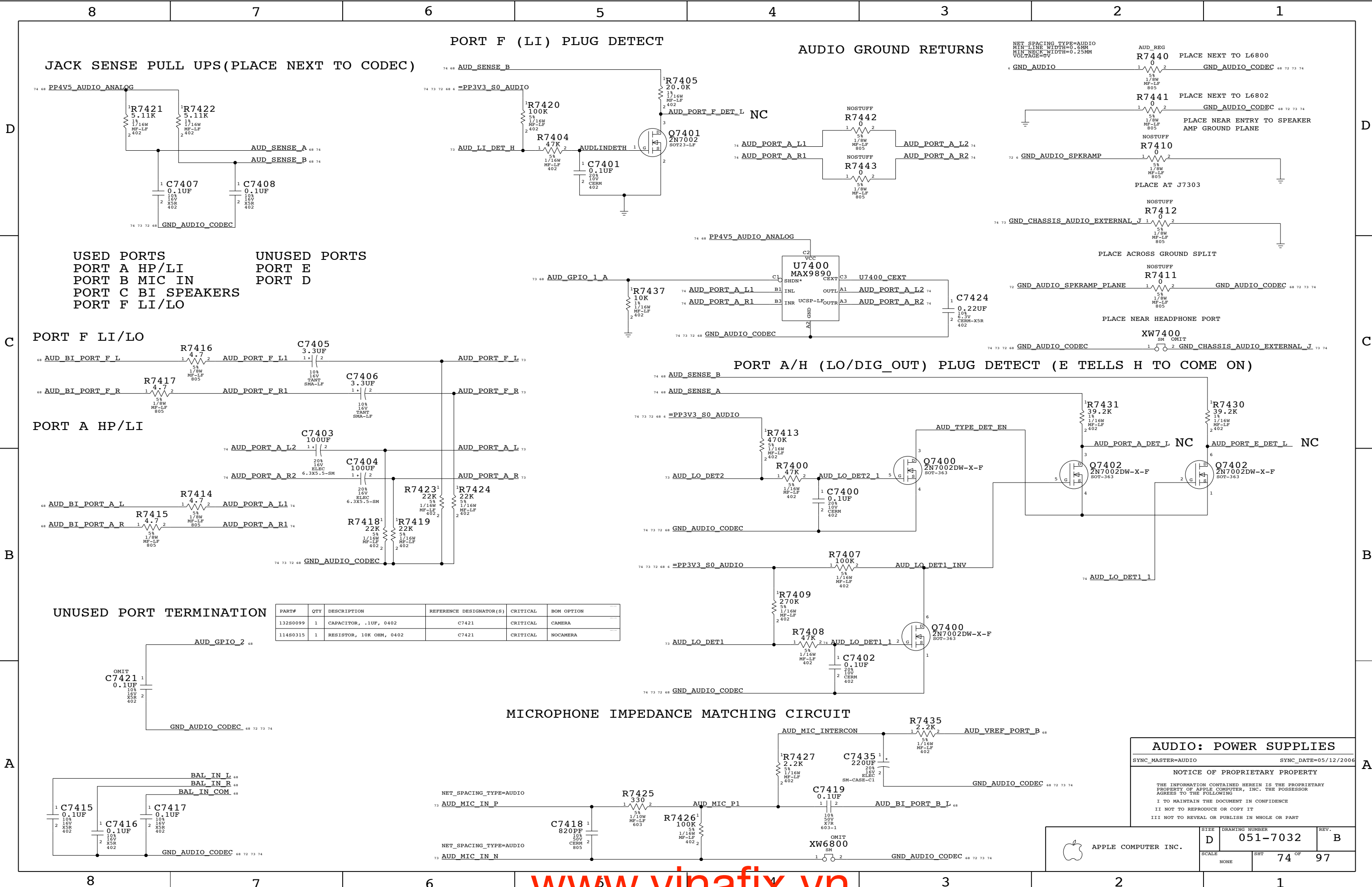
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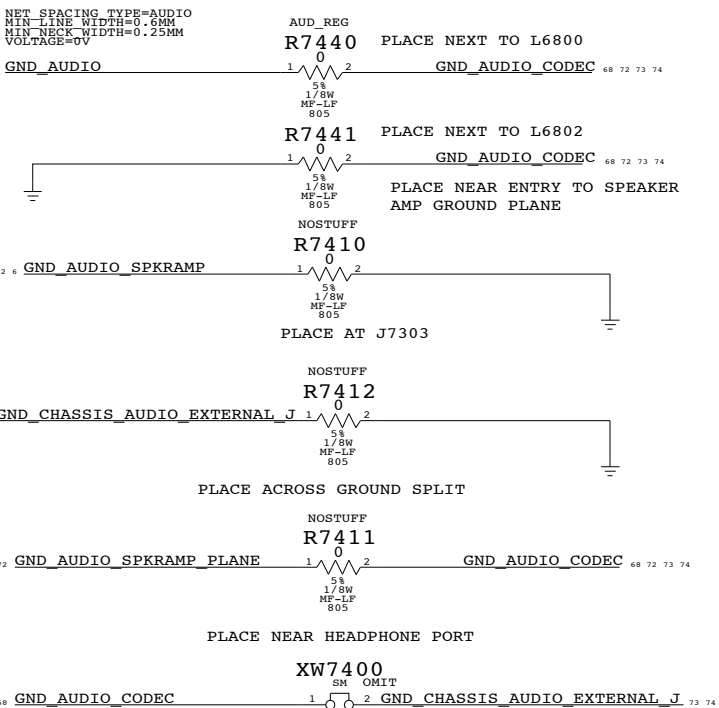
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	73 OF	97
NONE			



JACK SENSE PULL UPS (PLACE NEXT TO CODEC)

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS



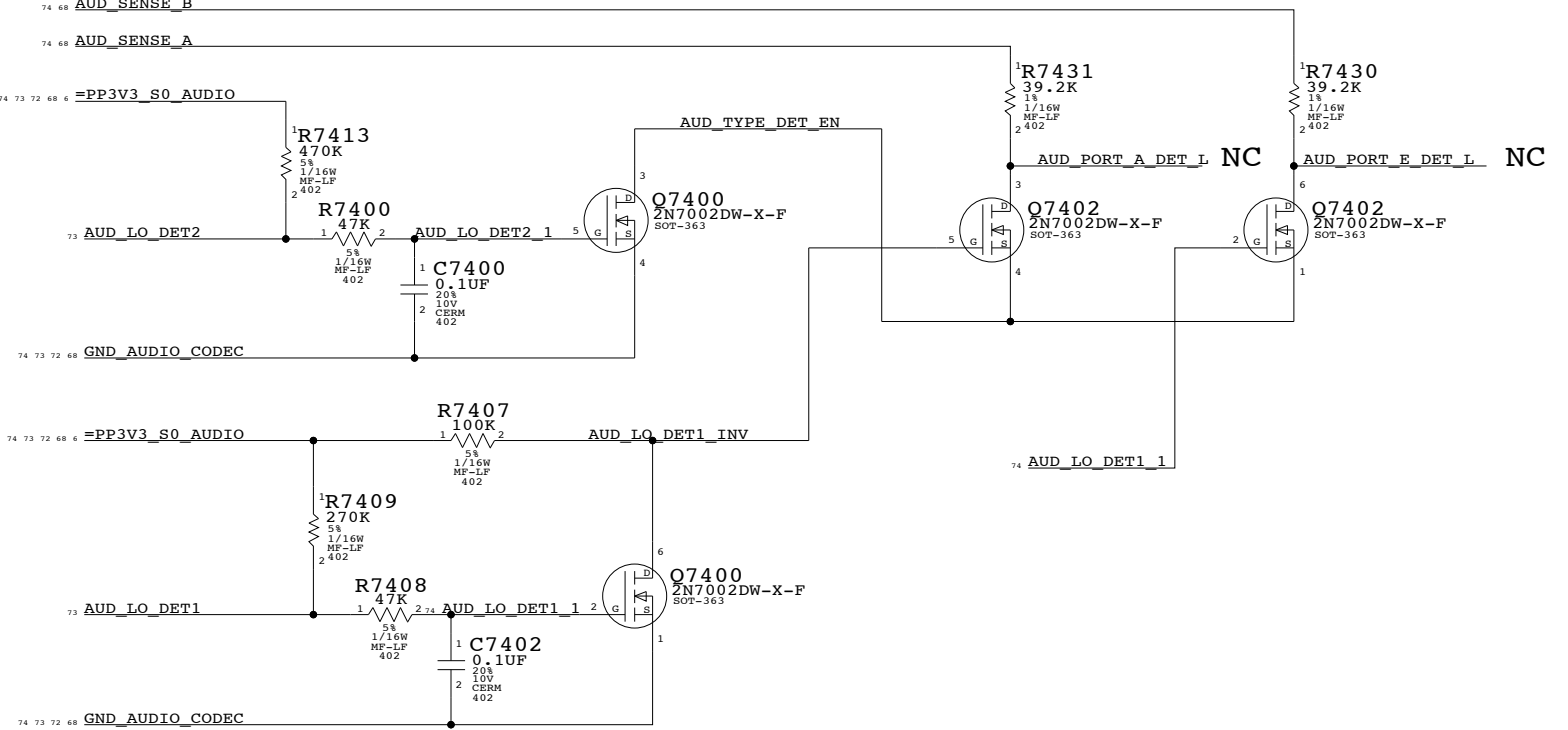
USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

PORT F LI/LO

PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

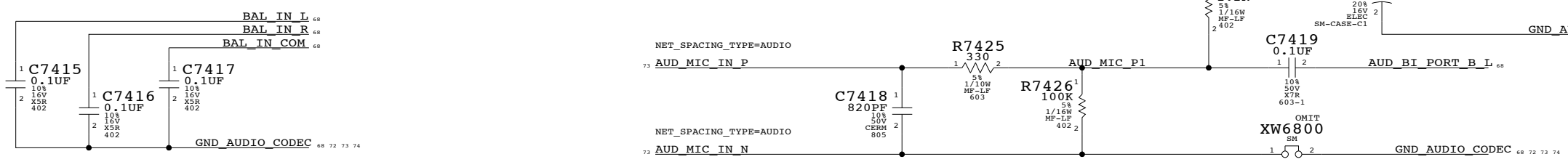
PORT A HP/LI



UNUSED PORT TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

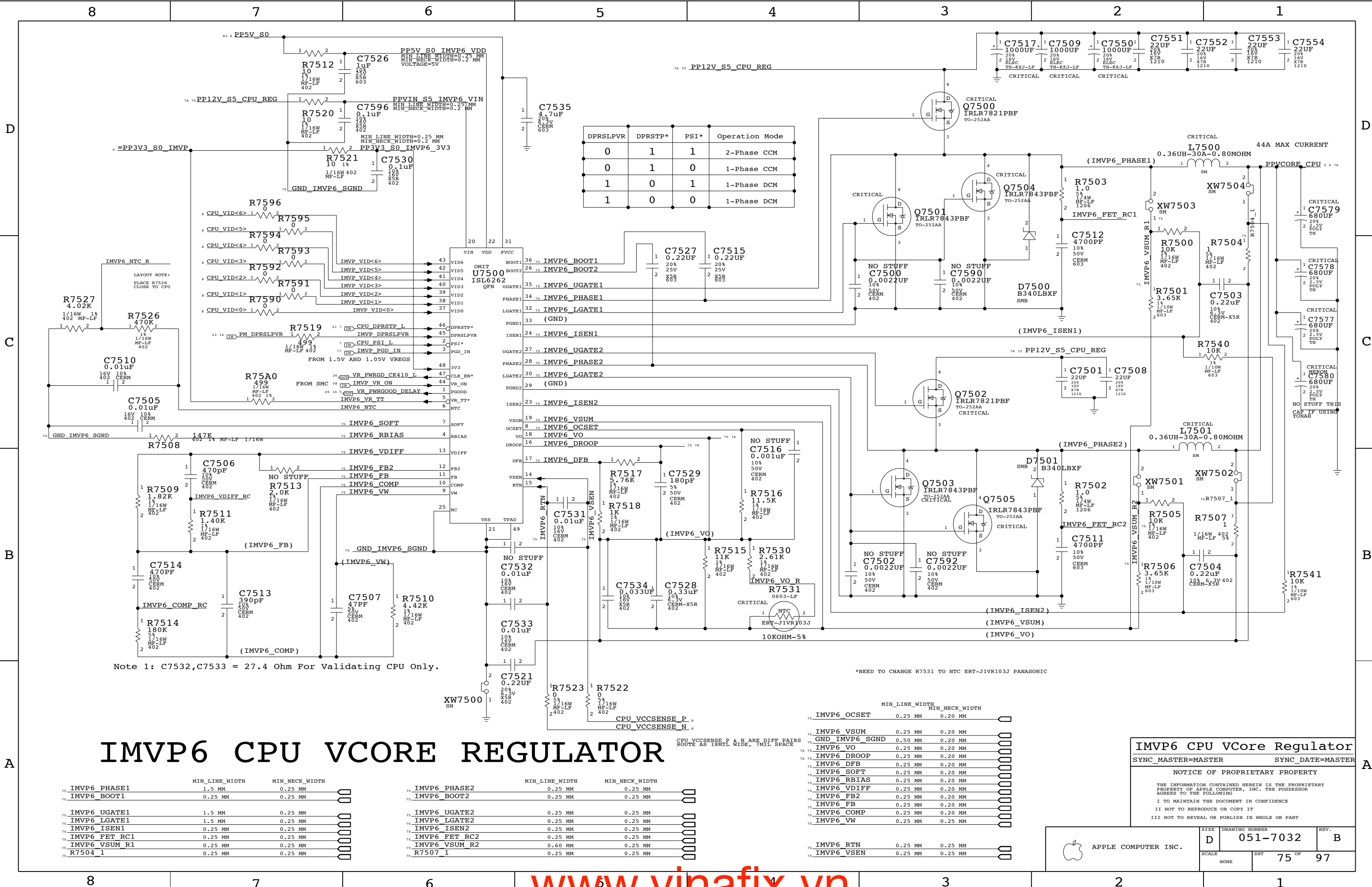
MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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	D	051-7032	B
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Pin	Signal	Pin	Signal
36	IMVP6_BOOT1	21	IMVP6_VSEN
26	IMVP6_BOOT2	22	IMVP6_VSEN
35	IMVP6_UGATE1	23	IMVP6_ISEN2
34	IMVP6_PHASE1	24	IMVP6_ISEN1
32	IMVP6_LGATE1	25	IMVP6_VO
33	(GND)	26	IMVP6_DROOP
27	IMVP6_UGATE2	27	IMVP6_DFB
28	IMVP6_PHASE2	28	IMVP6_VSEN
30	IMVP6_LGATE2	29	IMVP6_VO
29	(GND)	30	IMVP6_VSEN
19	IMVP6_VSUM	31	IMVP6_VSEN
8	IMVP6_OCSET	32	IMVP6_VSEN
18	IMVP6_VO	33	IMVP6_VSEN
16	IMVP6_DROOP	34	IMVP6_VSEN
17	IMVP6_DFB	35	IMVP6_VSEN
14	IMVP6_VSEN	36	IMVP6_VSEN
15	IMVP6_VSEN	37	IMVP6_VSEN
21	IMVP6_VSEN	38	IMVP6_VSEN
49	IMVP6_VSEN	39	IMVP6_VSEN
75	IMVP6_VSEN	40	IMVP6_VSEN
75	IMVP6_VSEN	41	IMVP6_VSEN
75	IMVP6_VSEN	42	IMVP6_VSEN
75	IMVP6_VSEN	43	IMVP6_VSEN
75	IMVP6_VSEN	44	IMVP6_VSEN
75	IMVP6_VSEN	45	IMVP6_VSEN
75	IMVP6_VSEN	46	IMVP6_VSEN
75	IMVP6_VSEN	47	IMVP6_VSEN
75	IMVP6_VSEN	48	IMVP6_VSEN
75	IMVP6_VSEN	49	IMVP6_VSEN
75	IMVP6_VSEN	50	IMVP6_VSEN

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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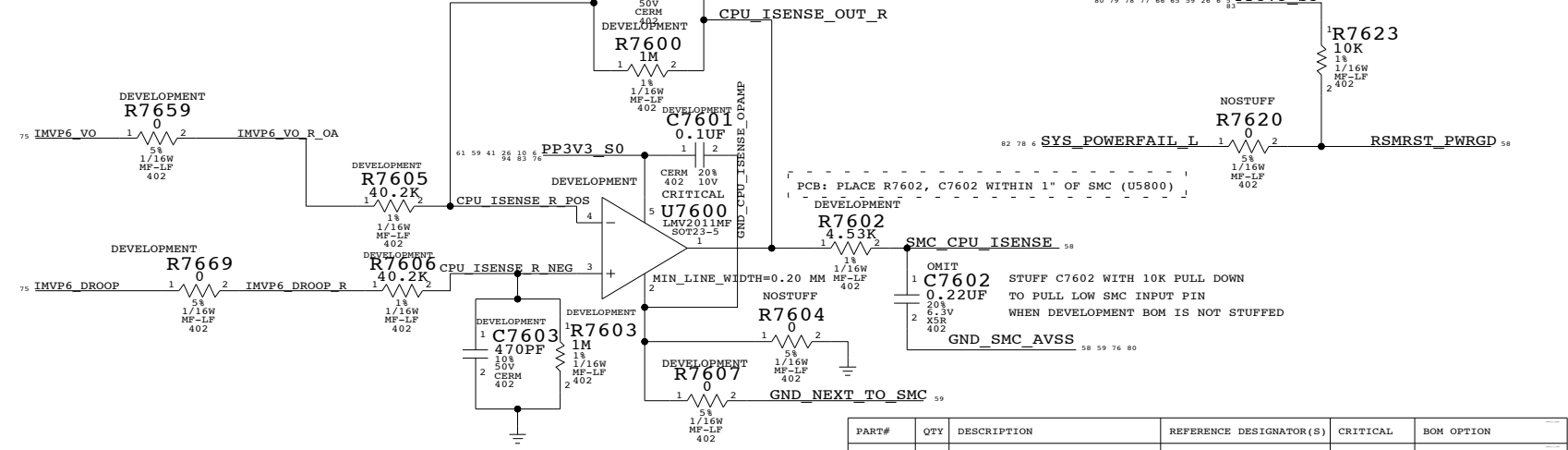
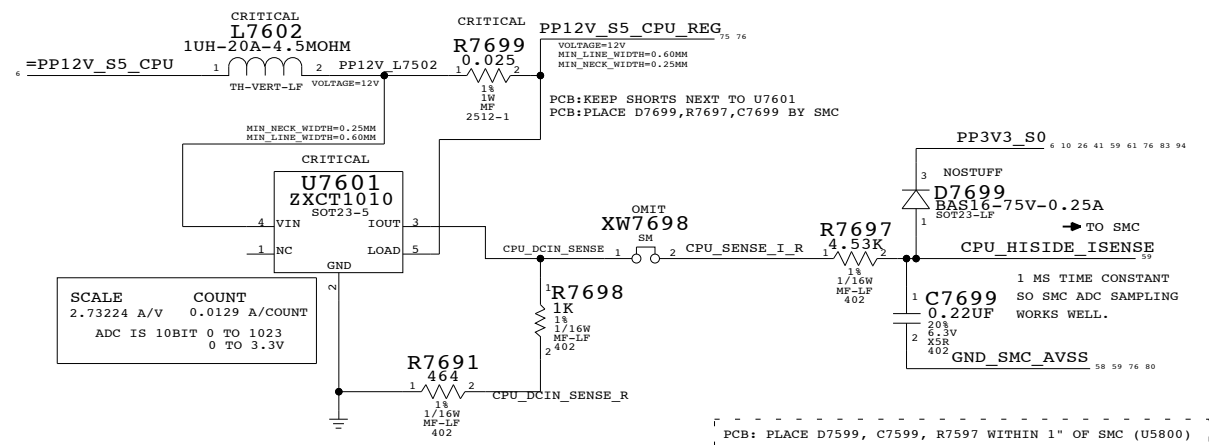
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	SCALE: NONE	SHEET: 75 OF 97	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

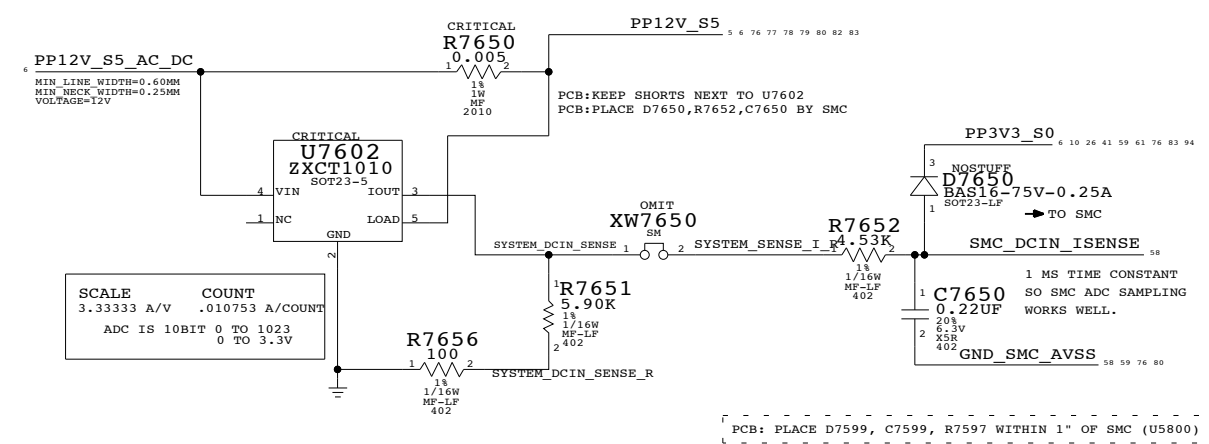
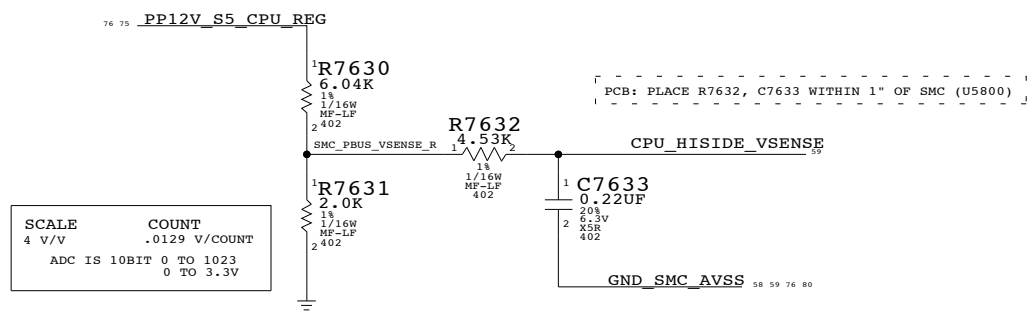
SMC PWRGD PULLUP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 6.3V, 20%, 0402	C7602		DEVELOPMENT
116S0090	1	RES, 10K, 5%, 0402	C7602		NOT_DEVELOPMENT

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

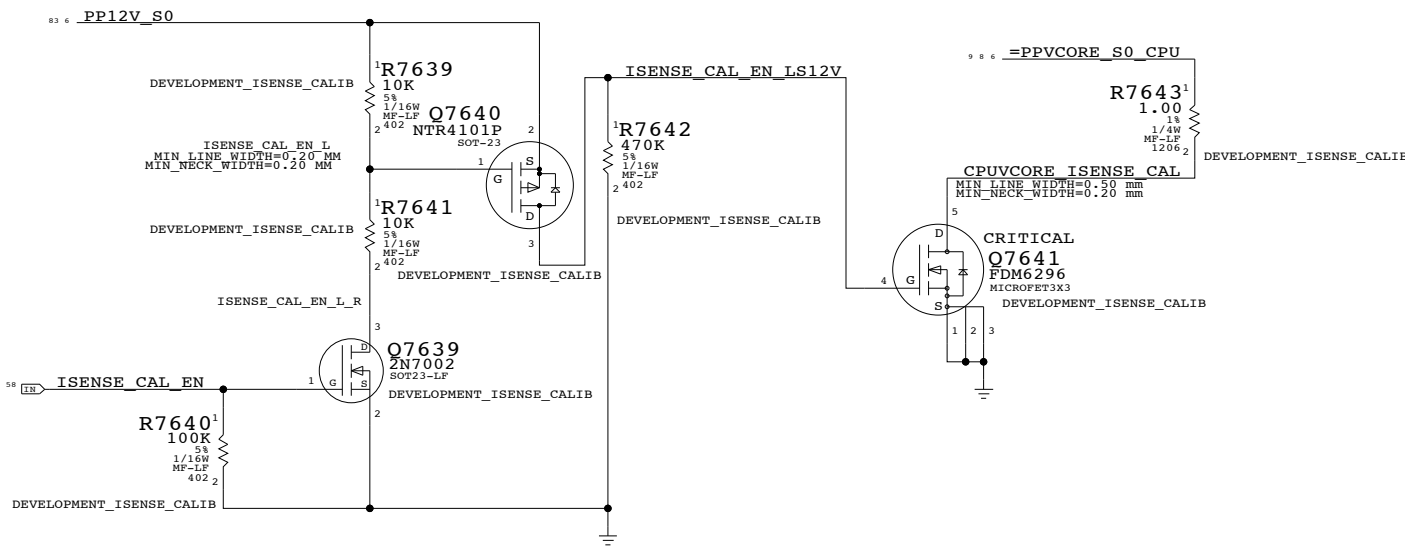
SYSTEM CURRENT SENSE



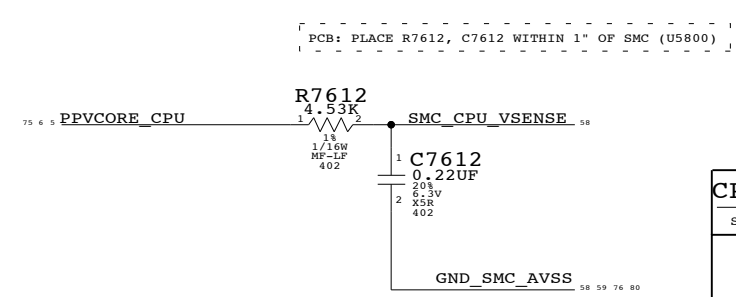
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



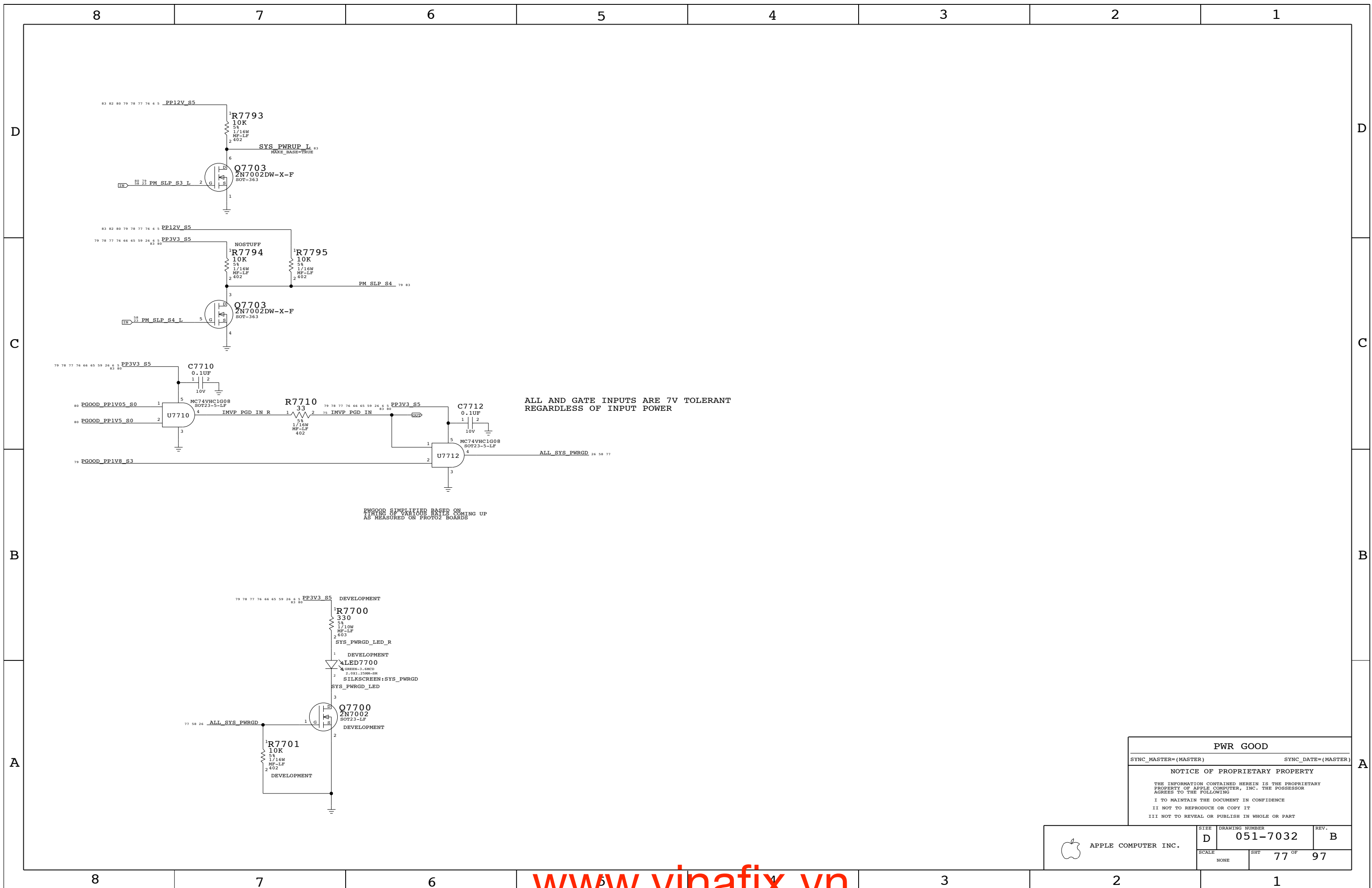
PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	76 OF 97	
NONE			



PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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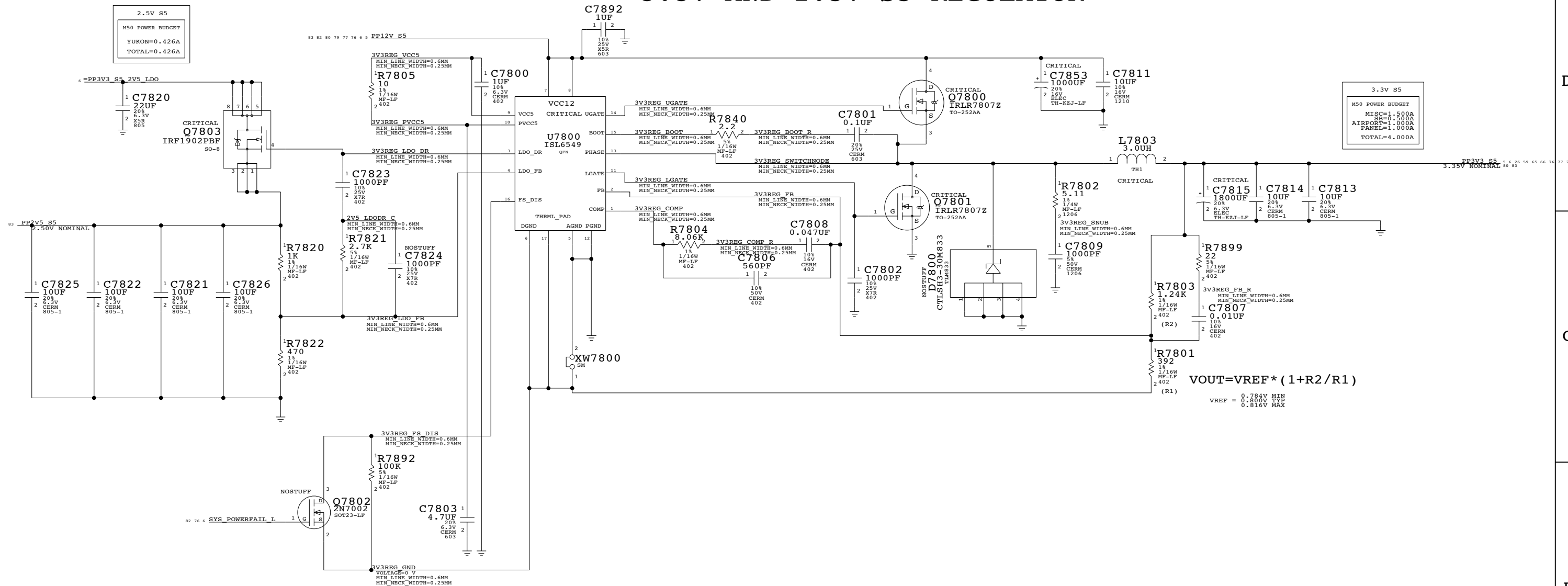
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	D	051-7032	B
SCALE	SHT		REV.
NONE	77 OF 97		

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

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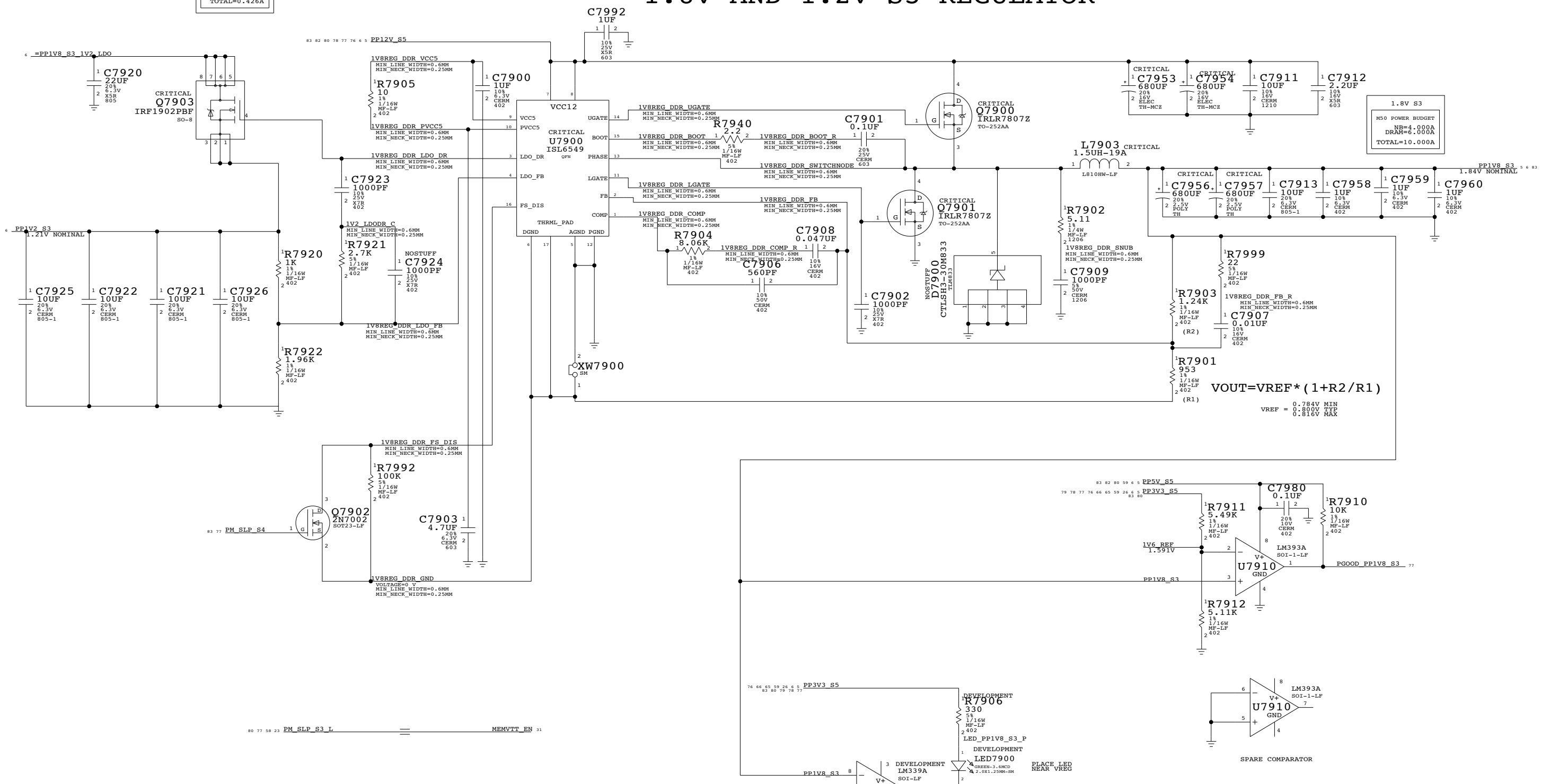
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	D	051-7032	B
SCALE	SHT	78 OF 97	
NONE		TRUE	

1.8V AND 1.2V S3 REGULATOR

1.2V S3
M50 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
M50 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A



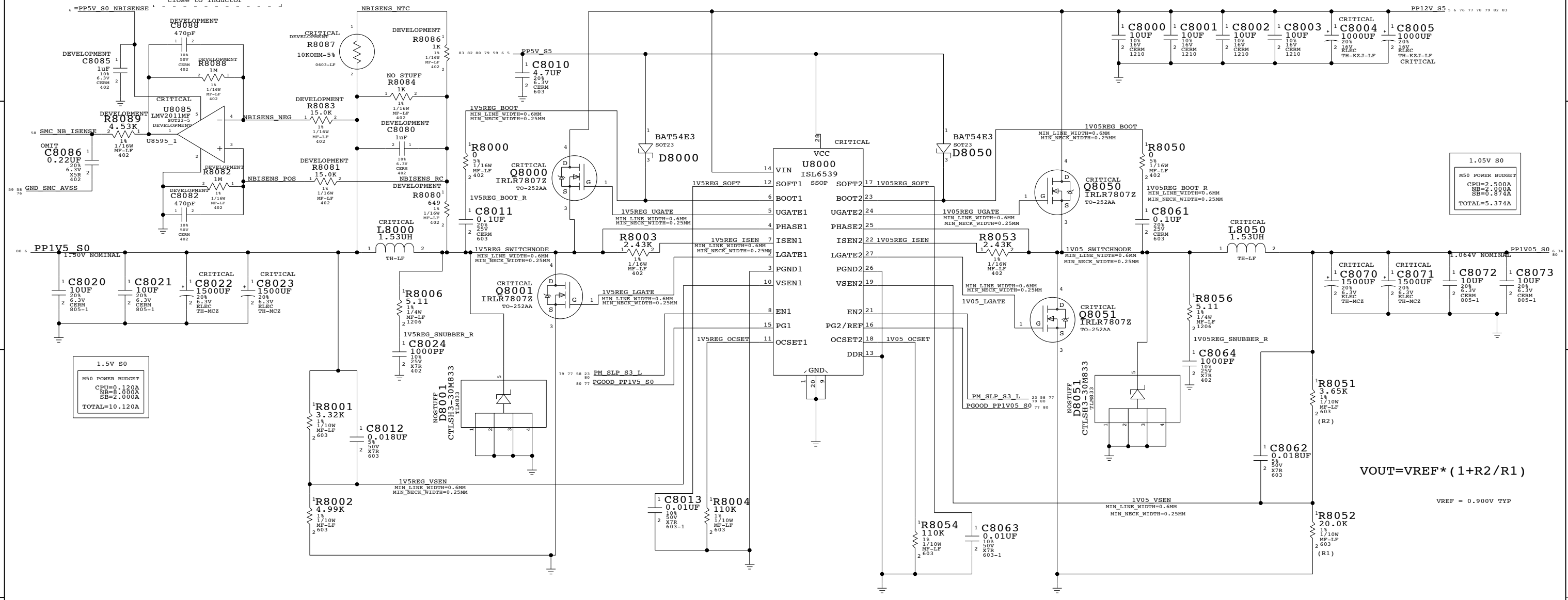
1.8V & 1.2V VREG
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	B
SCALE	SHT	79 OF	97
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor

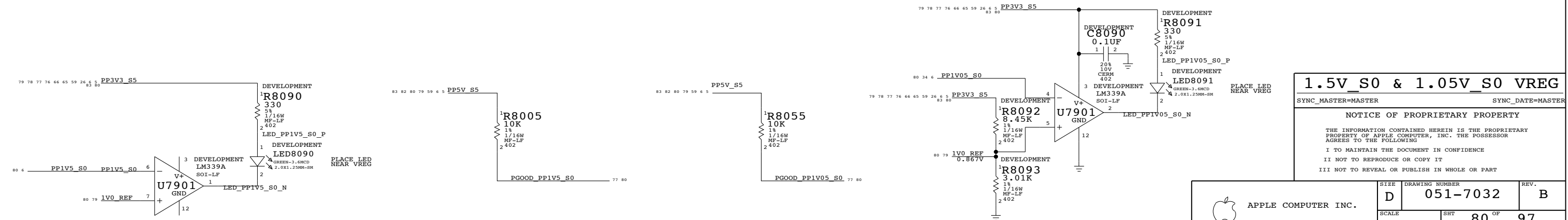


1.5V S0
M50 POWER BUDGET
CPU=0.120A
NB=8.0000A
SB=2.0000A
TOTAL=10.120A

1.05V S0
M50 POWER BUDGET
CPU=2.500A
NB=2.000A
SB=0.874A
TOTAL=5.374A

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.900V TYP



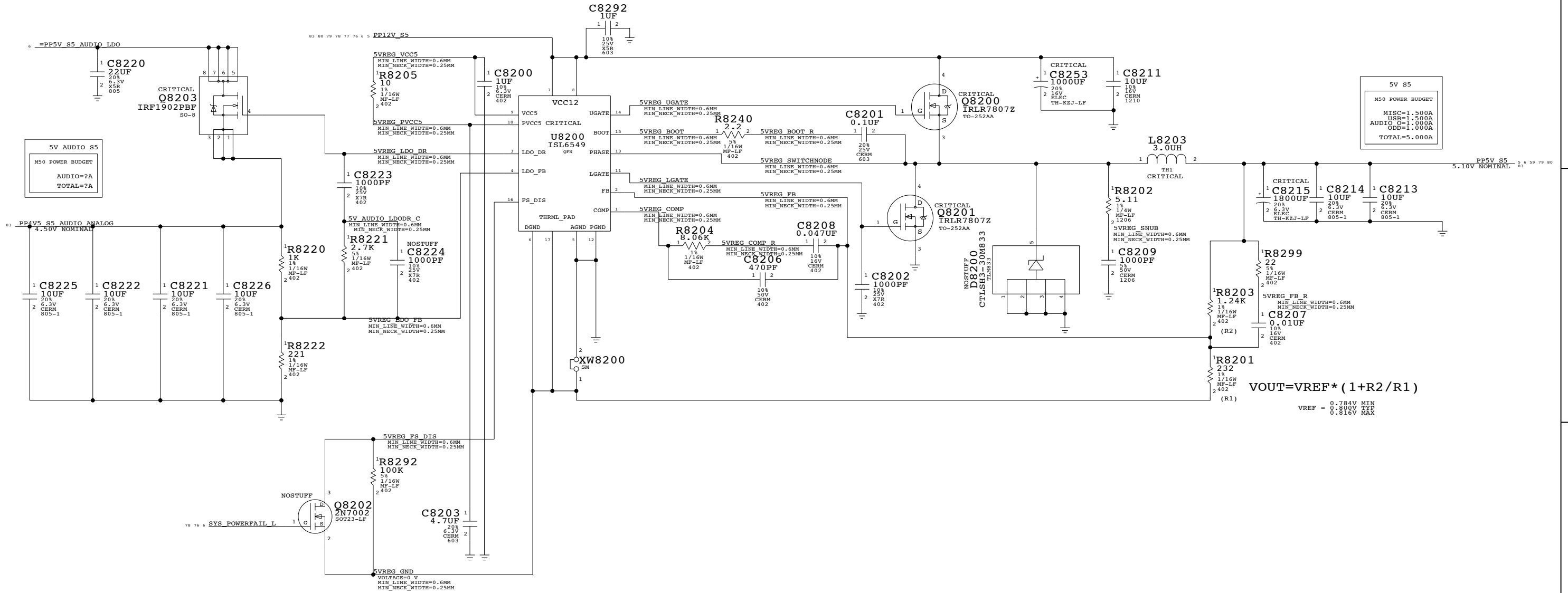
1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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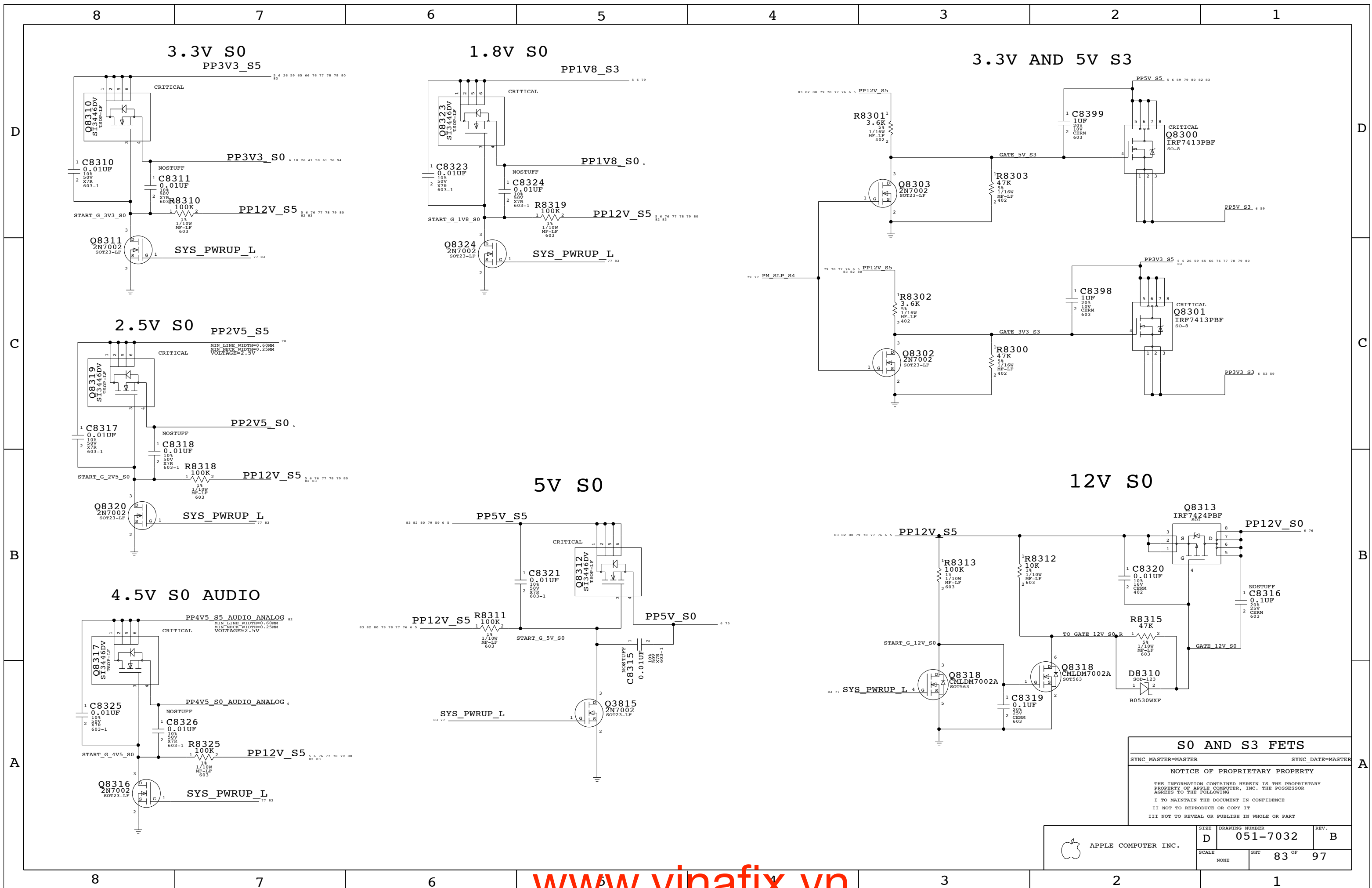
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	D	051-7032	B
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NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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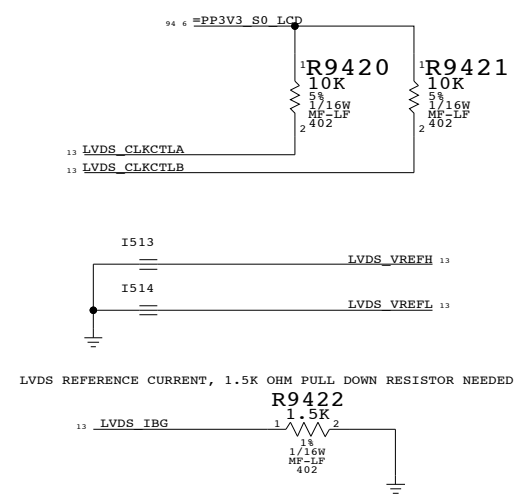
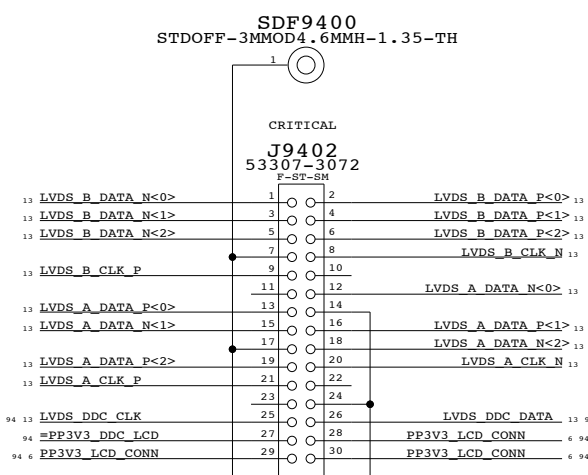
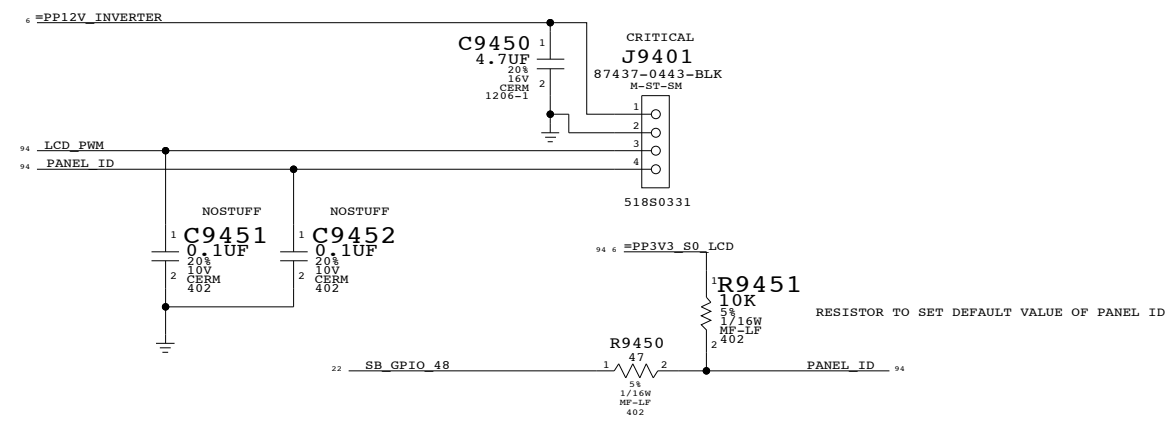
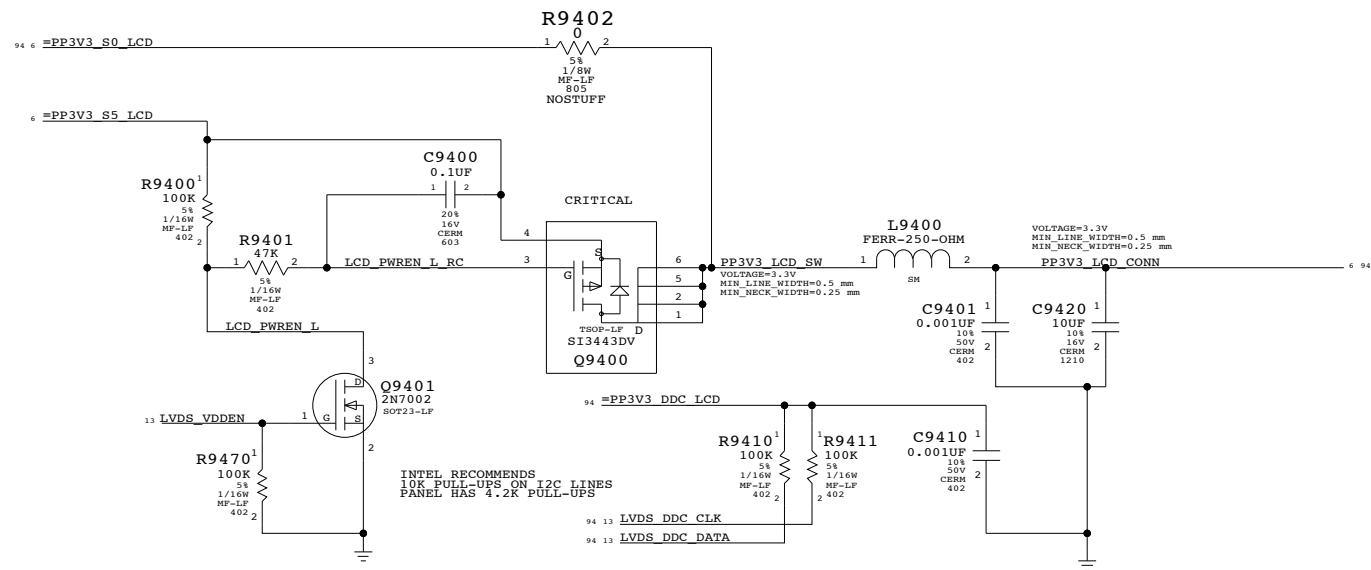
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	D	051-7032	B
SCALE	SHT	83 OF	97
NONE			

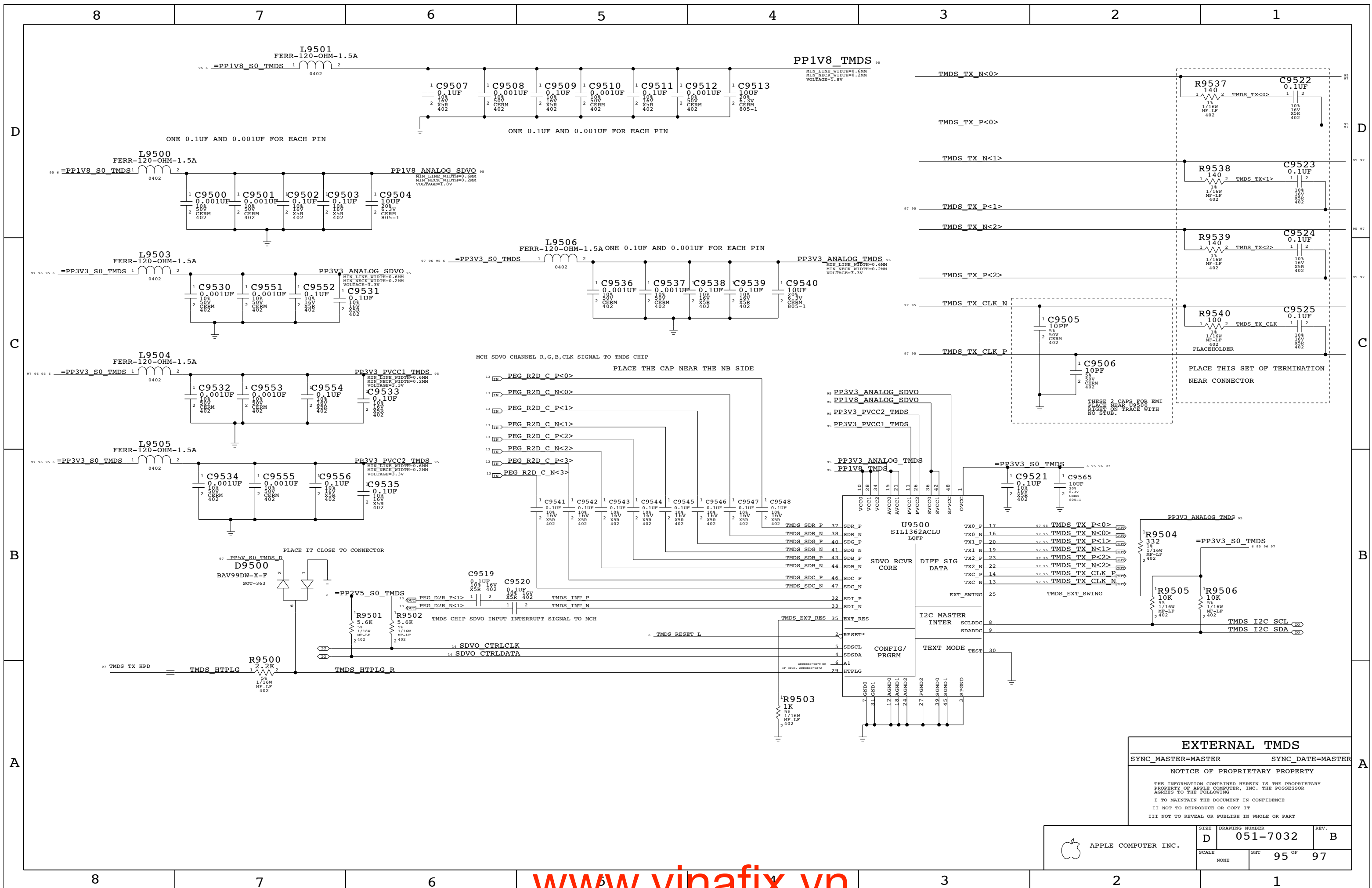
LCD (LVDS) INTERFACE

INVERTER INTERFACE



Internal Display Conns	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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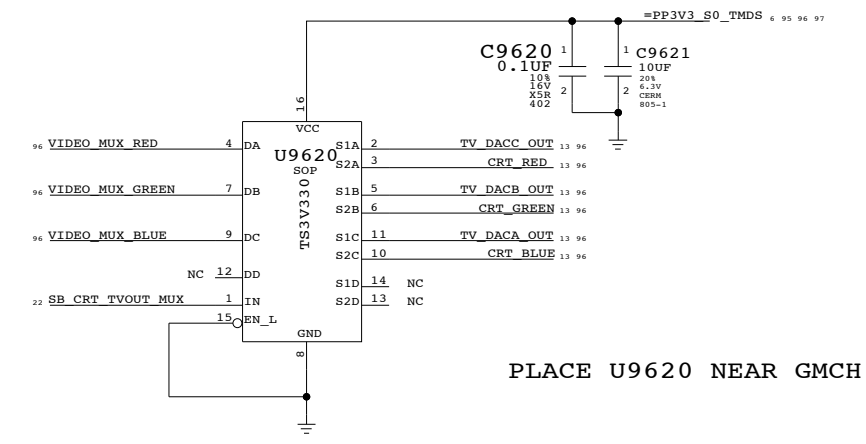
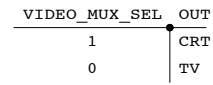
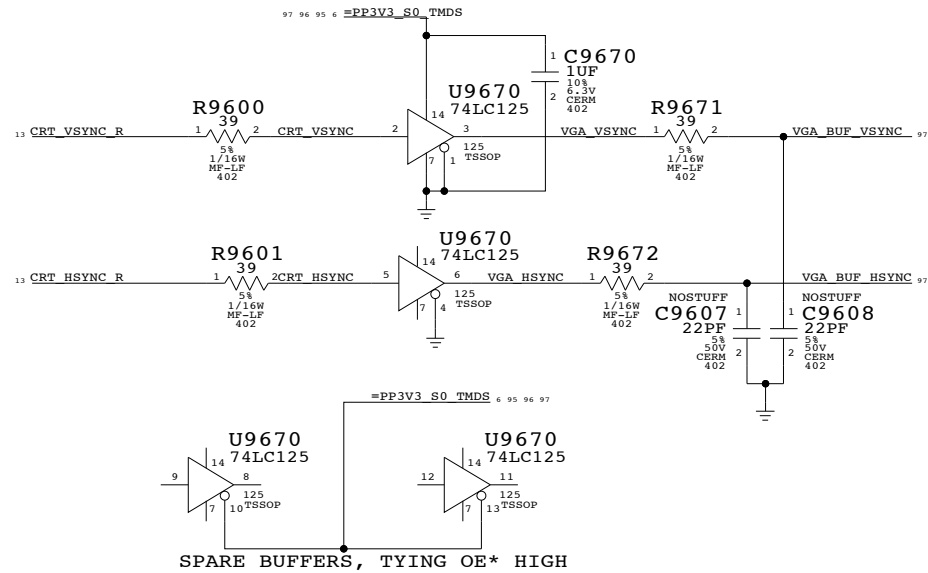
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	94 OF	97
NONE			



EXTERNAL TMSD
 SYNC_MASTER=MASTER SYNC_DATA=MASTER
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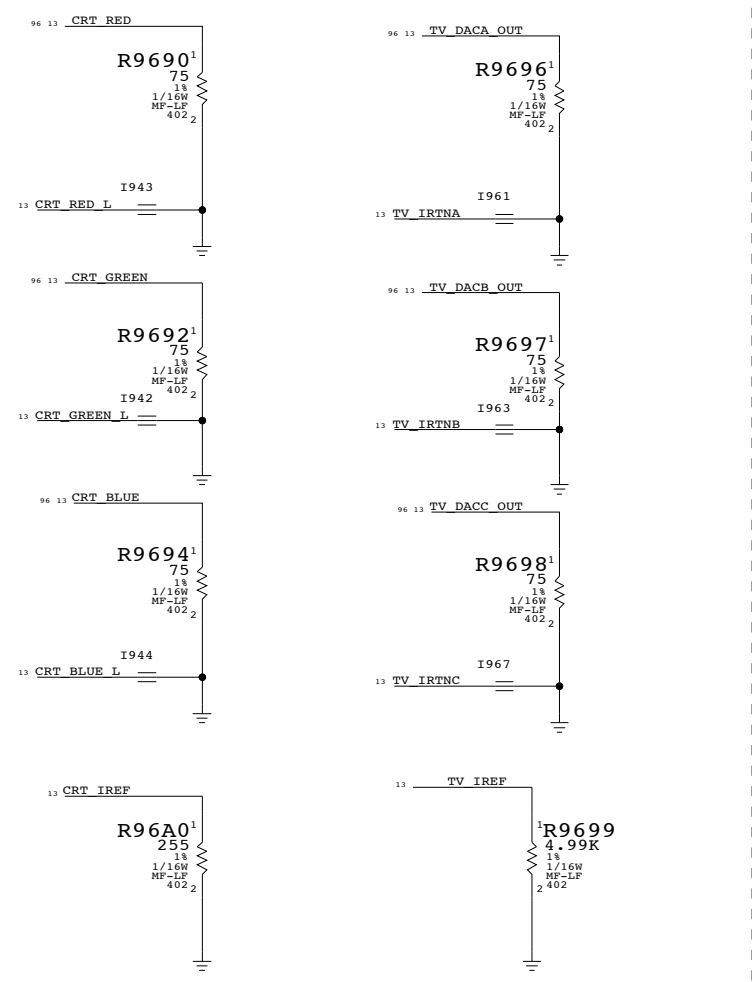
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 95 OF 97	

VGA SYNC BUFFERS

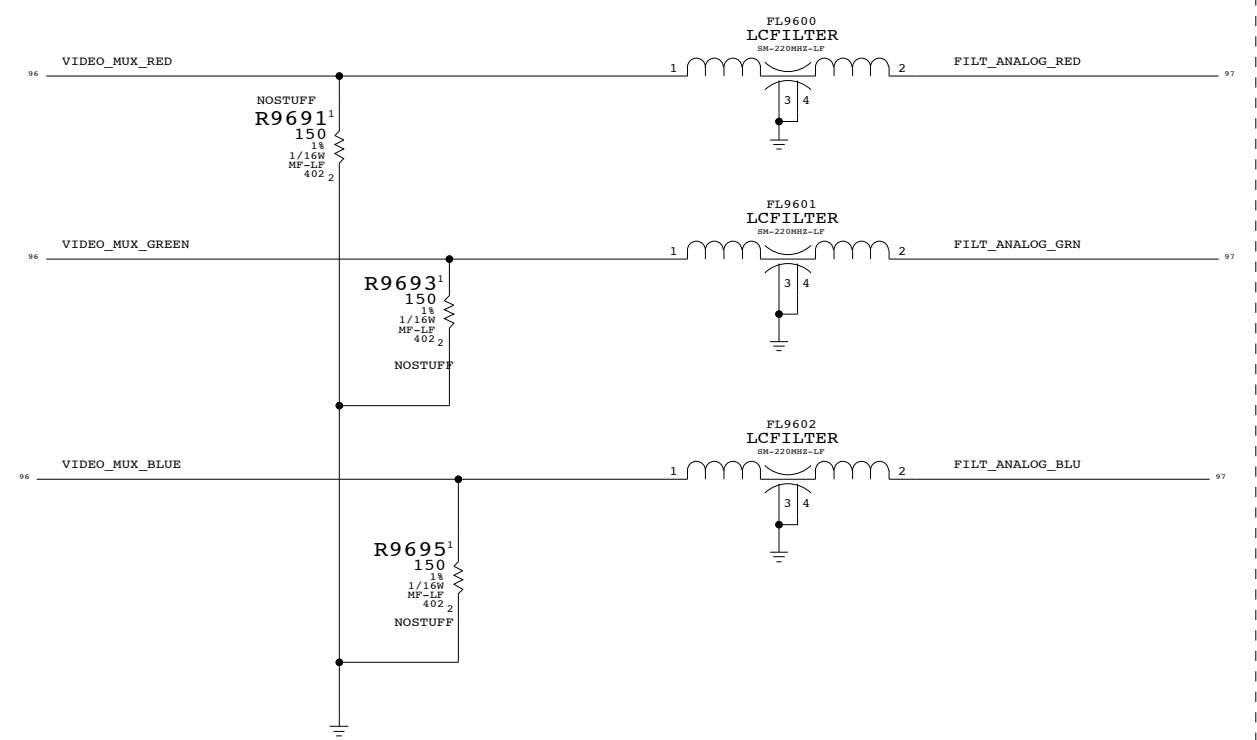


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE

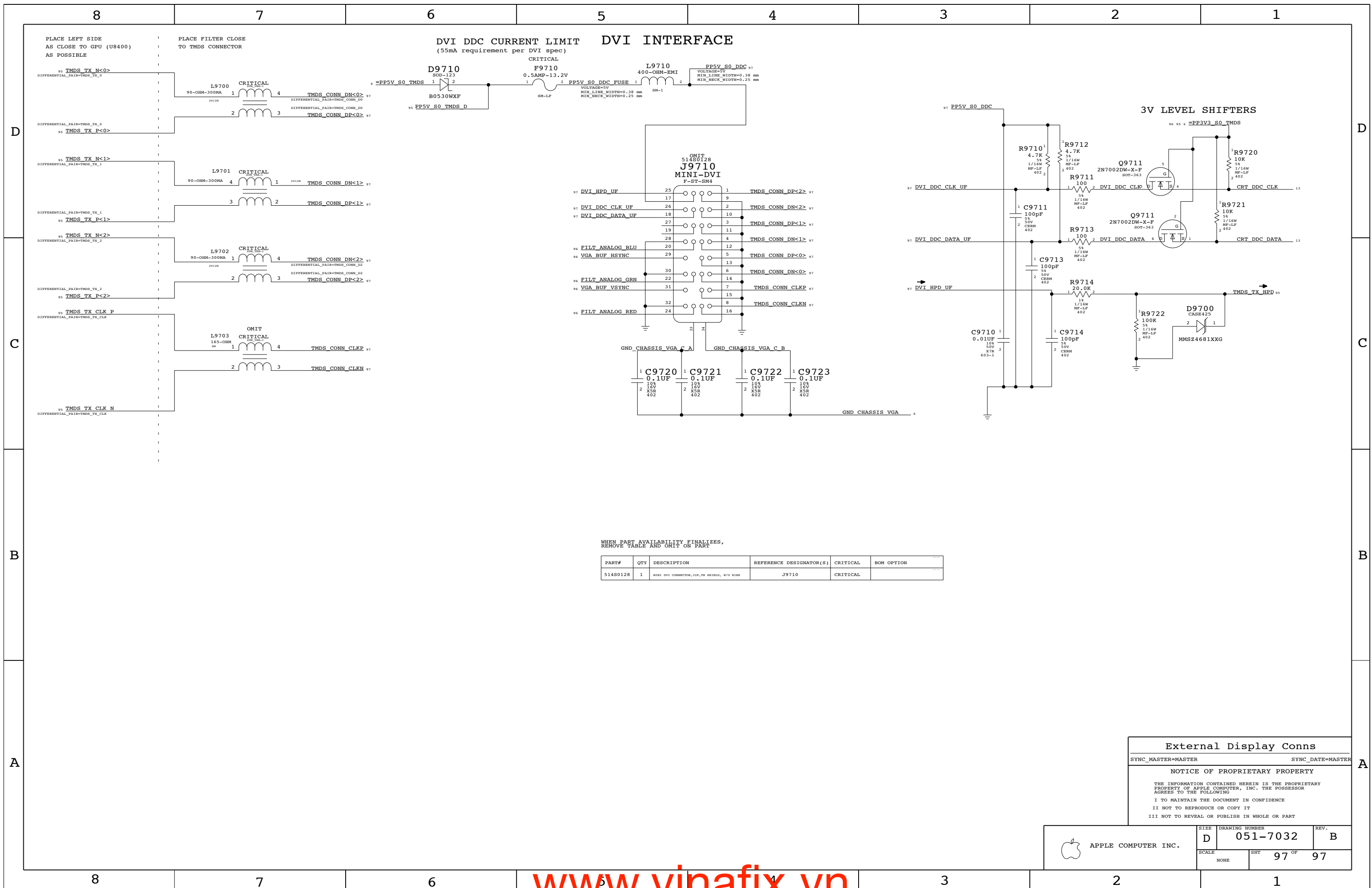


ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
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	D	051-7032	B
SCALE	SHT	96 OF	97
NONE			



WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51480128	1	MINI DVI CONNECTOR, 32P, TB SHIELD, W/O RING	J9710	CRITICAL	

External Display Conns
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	97 OF 97	
NONE			