1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-15

SCHEM,MLB_KEPLER_2PHASE,J31

FRB & RISK RAMP 02/15/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9585	1	SCHEM,MLB_KEPLER_2PHASE,J31	SCH	CRITICAL	
820-3330	1	PCBF,MLB_KEPLER_2PHASE,J31	PCB	CRITICAL	

DRAWING ABBREV=DRAWING TITLE=MLB

LAST_MODIFIED=Wed Feb 15 20:30:03 2012

DRAWING TITLE: SCHEM,MLB_KEPLER,J31

Apple Inc.

DRAWING NUMBER: 051-9585 | SIZE: D

REVISION: 3.0.0

BRANCH:

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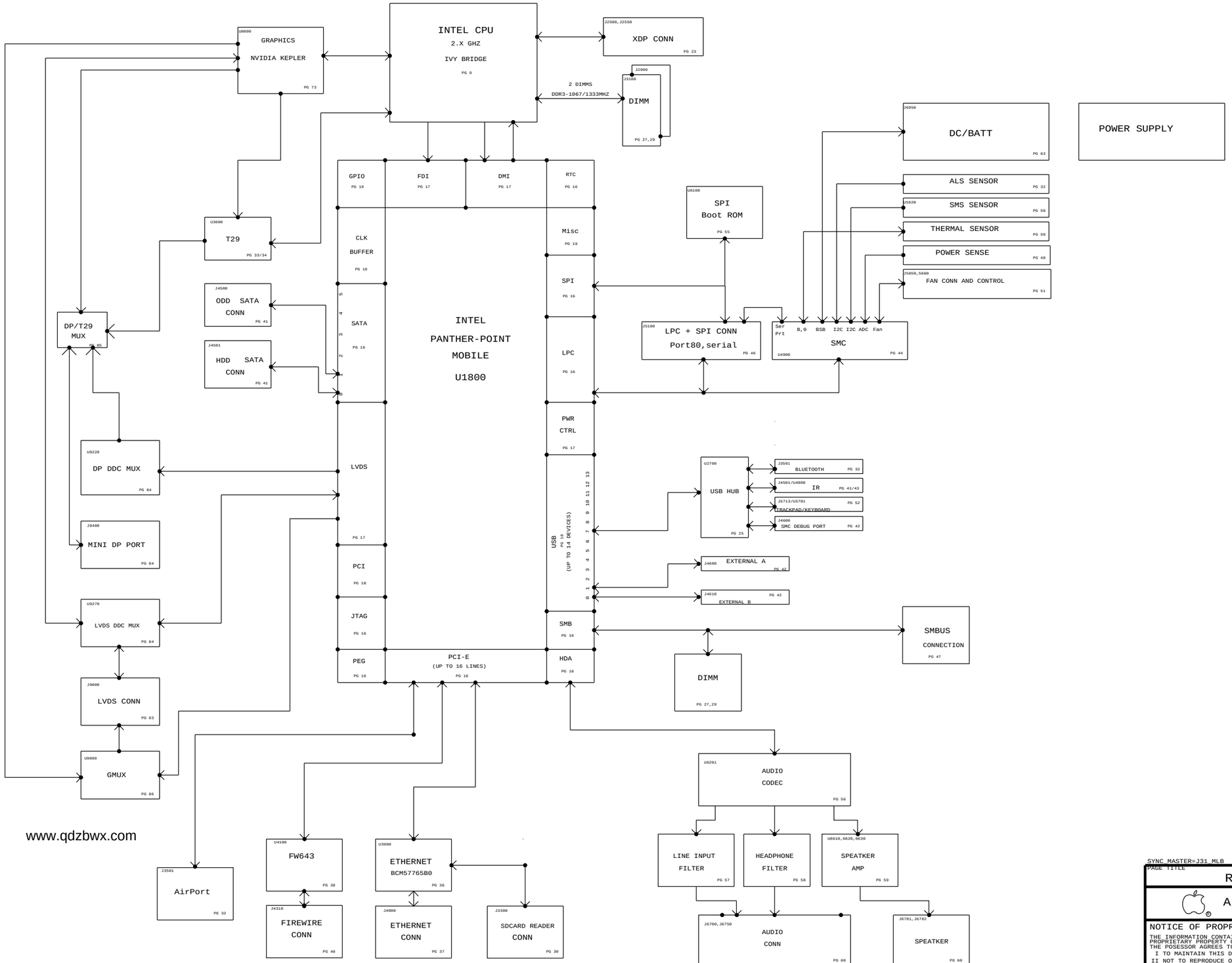

SYNC_MASTER=J31_MLB SYNC_DATE=04/19/2011

PAGE TITLE

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J31 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN — DCIN(18.5V) — F6905 6A FUSE — PP18V5_DCIN_CONN — R6990 — D6990 — PPBUS_G3H

R7020 — SMC_DCIN_ISENSE — U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64) — SMC_RESET_L — SMB_RST_N — PPVBUS_G3H — Q5310 SMC_DCIN_VSENSE — F7040 8A FUSE — PPBUS_G3H — Q5300 SMC_PBUS_VSENSE

R7050 — SMC_BMON_ISENSE — PPBUS_G3H — U5400 SMC_CPU_HI_ISENSE

J6950 — PPVBAT_G3H_CONN — 3S2P (9 TO 12.6V) — Q7055 CHGR_BGATE — PPVBAT_G3H_CHGR_R

PPBUS_G3H — U5410 SMC_GPU_HI_ISENSE

Q7840 — PP5V_SUS_FET — P5VSUS_EN — PP5V_S5_P5VSUSFET

PP5V_S5_LDO — PPDDR_S3_REG — Q7801 — PP1V5_S3RS0_FET — P1V5S3RS0FET_GATE

P5VS3_EN — P3V3S5_EN — TPS51980 U7201 (PAGE 66) — VREG5 — VOUT1 5V (L/H) — VOUT2 3.3V (R/H) — PP5V_S3_REG — PP3V3_S5_REG — PGOOD1 — PGOOD2 — P3V3S5_PGOOD — P5VS3_PGOOD

P1V5CPU_EN — SLG5AP020 U7801 (PAGE 72) — PP5V_S5_LDO

VIN — VOUT — TPS61045 U5805 (PAGE 54) — PP18V5_S4

USB PORT POWER SWITCH 5V — U4600 (PAGE 42) — VIN — VOUT1 — VOUT2 — EN1 — EN2 — USB_PWR_EN — PP5V_S3_RTUSB_A_ILIM — PP5V_S3_RTUSB_B_ILIM

SMC U4900 (PAGE 45) — H10 SMC_BATLOW_L — M2 SMC_PM_G2_EN — RC DELAY — P3V3S5_EN

COUGAR-POINT MOBILE U1800 — RC DELAY P3V3S3_EN — RC DELAY DDRREG_EN — P5VS3_EN — PM_SLP_S4_L — PM_SLP_SUS_L — R7916 — R2526 — SCDS_IMAGE|R.jpg|272|166 — U2150 (PAGE 24) — FW_PWR_EN_PCH — FW_PWR_EN — U2152 (PAGE 24) — AUD_IPHS_SWITCH_EN_PCH — TBT_PWR_EN — PM_SLP_S3_L — (PAGE 16~21)

SLP_S4#(H4) — SLP_SUS — SLP_S5*(D10) — (D14) — (V13) — (U2) — SLP_S3#(F4)

GMUX U9600(N8) (PAGE 88) — LCD_PWR_EN — T29_A_HV_EN_R — PORT A MCU U9330 (PAGE 86) — R9334 — SCDS_IMAGE|R.jpg|272|166 — T29_A_HV_EN

SMC_BATLOW_L — 3.3V/5.0V (A) — SUS ENABLE (C) U7940 (PAGE 73) — (Y) — PM_SLP_SUS_L — P5VSUS_EN — P3V3SUS_EN

GMUX U9600 — PB7A LCD_BKLT_EN — PB16B EG_RAIL1_EN — P3V3GPU_EN — PB17A EG_RAIL2_EN — GPUVCORE_EN — PB17B EG_RAIL3_EN — P1V0GPU_EN — PB18A EG_RAIL4_EN — P1V5FB_EN — P1V8GPU_EN — ALL_EG_PGOOD — PM_ALL_GPU_PGOOD — XP25-5 (PAGE 88) PL25A

ISOLATE_CPU_MEM_L — SCDS_IMAGE|O.jpg|416|272 — PM_SLP_S3_L — PM_SLP_S4_L — P1V5CPU_EN — PLT_RST_L — SCDS_IMAGE|O_0.jpg|416|272 — MEMVTT_EN — CPU_MEM_RESET — SCDS_IMAGE|O_1.jpg|416|272 — MEM_RESET_L — P5VS0_EN — P3V3S0_EN — PBUSVSENS_EN

Q7870 — PP3V3_S0GPU_FET — P3V3GPU_EN — PP3V3_S5

Q7810 — PP3V3_S3_FET — Q7922 — PP3V3_ENET_FET — P3V3S3_EN — PM_SLP_S3_L & WOL_EN & SMC_ADAPTER_EN

Q7830 — PP3V3_S0_FET — P3V3S0_EN — T29 SWITCH 3.3V TPS22924 U3810 (PAGE 35) — VIN — VOUT — PP3V3_T29_FET — TBT_PWR_EN — EN

Q7860 — PP5V_S0_FET — P5VS0_EN — SMC_SYS_KBDLED — VIN CTRL KB_BL LT3491 U5850 (PAGE 54) — LED

PP3V3_S0_AUDIO — 4.5V AUDIO MAX8840 U6200 (PAGE 57) — VIN — VOUT — SHND — PP4V5_AUDIO_ANALOG

T29 15V BOOST — VIN LT3957 U3800 (PAGE 35) — VOUT — PP15V_T29_REG — T29_A_HV_EN — EN — FIREWIRE PORT — POWER SWITCH U4260 (PAGE 39) — VIN — VOUT — PPBUS_FW_FET — FWPORT_PWR_EN — EN

Q7800 — PP3V3_S4_FET — P3V3S4_EN

TPS22924 U4201 (PAGE 39) — VIN — VOUT — PP3V3_FW_FET — EN — FW_PWR_EN

FPF1009 U9000 (PAGE 84) — VIN — VOUT — PP3V3_SW_LCD_UF — EN — LCD_PWR_EN

P1V5S0_EN — TPS62201 U7710 (PAGE 71) — EN — VIN — VOUT — PP1V5_S0_REG

P1V2S0_EN — 1V2_S0(GMUX) TPS62201 U7760 (PAGE 71) — VIN — EN — VOUT — PP1V2_S0_REG

Q7820 — PP3V3_SUS_FET — P3V3SUS_EN — PP3V3_SUS_P1V05SUSLDO

TPS720105 U7740 (PAGE 71) — VIN — EN — VOUT — PP1V05_SUS_LDO

P1V8S0_EN — ISL8014A U7720 (PAGE 71) — VIN — EN — VOUT — PGOOD — PP1V8_S0_REG — P1V8S0_PGOOD

P1V8GPU_EN — 1V8GPU FET NCP4543IMN5RG-A U7880 (PAGE 72) — VIN — EN — VOUT — PP1V8_GPU_FET — UD180 (RD186) — PP1V8_S0GPU_ISNS — SMC_GPU_1V8_ISENSE

F9700 3A 32V FUSE — Q9706 — LCD_BKLT_EN — && — BKLT_PLT_RST_L — UD120 — PPBUS_SW_BKL — SMC_LCDBKLT_ISENSE

PPBUS_SW_LCDBKLT_PWR — LP8550 U9701 (PAGE 89) — VIN — EN — VOUT — PPVOUT_SW_LCDBKLT — SMC_LCDBKLT_VSENSE

ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 63) — PP3V42_G3H — SMC_TPAD_RST_L — SMC_ONOFF_L — VIN SMC RESET SMC AVREF SUPPLY SN0903048 U5010 (PAGE 46) — MR1 — MR2 — RESET — REFOUT — SMC_RESET_L — PP3V3_S5_AVREF_SMC

U3815 & U3816 — 1V05 T29 SWITCH (PAGE 35) — VIN — VOUT — EN — PP1V05_T29_FET — TBT_PWR_EN

PP5V_S0_CPUVCCIOS0 — CPU VCCIO 1V0 / 1.05V ISL95870 U7600 (PAGE 70) — VIN — VOUT — PGOOD — EN — CPUVCCIOS0_EN — U5310 (R7640) — PPCPUVCCIO_S0_REG — SMC_CPUVCCIO_ISENSE — CPUVCCIOS0_PGOOD — TPS22924 U4202 (PAGE 39) — VIN — VOUT — EN — PP1V0_FW_FET_R — FW_PWR_EN

CPU/AXG VCORE CPU VOUT MAX15119GTM U7400 (PAGE 68) — VIN — EN — PGOKA — PGOKB — CPUIMVP_VR_ON — U5450 — SMC_CPU_ISENSE — SMC_CPU_VSENSE — PPVCORE_S0_CPU — U5460 — SMC_AXG_ISENSE — SMC_AXG_VSENSE — PPVCORE_S0_AXG_REG — CPUIMVP_PGOOD — CPUIMVP_AXG_PGOOD

PP5V_S3_DDRREG — VIN VLDOIN 1.5V — S5 — VOUT1 — PPDDR_S3_REG — U5360 (R7350) — PP1V5_S3 — SMC_DDR3_ISENSE — DDRREG_EN — DDRVTT_EN — S3 — 0.75V — VOUT2 — PPVTT_S0_DDR_LDO — TPS51916 U7300 (PAGE 67) — PGOOD — DDRREG_PGOOD

SYSTEM AGENT — VIN — ISL95870A U7100 (PAGE 65) — VOUT — PGOOD — PVCCSA_EN — U5360 (R7140) — PPVCCSA_S0_REG — SMC_CPUVCCSA_ISENSE — PVCCSA_PGOOD

GPU VDDCI 0V9~1V15 ISL95870A U9800 (PAGE 90) — VIN — VOUT — PGOOD — EN — PVDDCI_EN — PPVDDCI_S0_REG — PVDDCI_PGOOD

PP3V3_S0_VMON — PP5V_S0_VMON — PP1V5_S3RS0_VMON — PP1V05_S0_VMON — VCC — V2MON — V3MON — V4MON — U7960 ISL88042IRTEZ (PAGE 73) — RST* — TRST = 200mS

UD141 (RD145) — PP1V0_S0GPU_REG — P1V0GPU_EN — EN1 — VIN — VOUT — 1V0GPU/1V5 FB 1.003V(L/H) — VOUT2 — SMC_GPU_1V0_ISENSE — P1V5FB_EN — EN2 — 1.503V(R/H) — ISL6236 U8300 (PAGE 77) — POK1 — POK2 — PP1V5_GPU_REG — P1V0GPU_PGOOD — P1V5FB_PGOOD — PP3V3_S0_PWRCTL — R9990 — GPUVCORE_PGOOD — P1V5FB_PGOOD — P1V0GPU_PGOOD — PM_ALL_GPU_PGOOD — ALL_EG_PGOOD

WHISTLER PCI-E — PWRGOOD (AH16) U8000 (PAGE 74)

GRAPHICS MUX — PL25A (N1) U9600 (PAGE 88)

PP5V_S3_GPUVCORE — U5310 — VIN — VDD/PVCC — VOUT — GPU VCORE ISL6263C U8900 (PAGE 83) — VR_ON — PGOOD — GPUVCORE_EN — SMC_GPU_ISENSE — SMC_GPU_VSENSE — PPVCORE_GPU_REG — GPUVCORE_PGOOD — R5388/U5388

U9950 — PM_S0_PGOOD — PM_PCH_SYS_PWROK — PM_PCH_PWROK — U9950 — CPUIMVP_VR_ON

COUGAR_POINT — PWRBTN# (E20) — PM_PWRBTN_L — SYS_RERST# (K3) — PM_SYSRST_L — DPWROK (E22) — PM_DSW_PWRGD — ACPRESENT/GPIO31 (H20) — SMC_ADAPTER_EN — PLTRST# (C6) — PLT RESET L — SYS_PWROK — CPU_PWRGD — PROCPWRGD (AY11) — PM_MEM_PWRGD — DRAMPWROK — RSMRST# (C21) — PM_RSMRST_L — U1800 (PAGE 16~21)

P1V5S0_PGOOD — P1V8S0_PGOOD — P5VS3_PGOOD — CPUVCCIOS0_PGOOD — PCHVCCIOS0_PGOOD — PVCCSA_PGOOD — ALL_SYS_PWRGD_R

3V3 SUS DETECT — U7930 (PAGE 73) — RESET

CPU — SM_DRAMPWROK (AY25) — PM_MEM_PWRGD — UNCOREPWRGOOD (C60) — CPU_PWRGD — U1000 (PAGE 9~13) — RESET* (K51) — CPU_RESET_L

SMC — T1CCP1/PJ1 — SMC_ADAPTER_EN (B9) — WT2CCP0/PH0(K3) — ALL_SYS_PWRGD — SSIOFSS/PA3 (M3) — PM_DSW_PWRGD — S5_PWRGD(L9) — S5_PWRGD — SMC_ONOFF_L — PQ7/IRQ131(L6) — WT3CCP1/PH5 (H4) — PM_SYSRST_L — WT3CCP0/PH4 (J3) — PM_PWRBTN_L — PM_SLP_S5_L — PQ6/IRQ130(M6) — VREFA* (D2) — PP3V3_S5_AVREF_SMC — PM_SLP_S4_L — PQ5/IRQ129(K5) — PM_SLP_S3_L — PQ4/IRQ128(N6) — RST* (G10) — SMC_RESET_L — LM4FSXAH5BB U4900 (PAGE 44)

SYNC_MASTER=K17_REF — SYNC_DATE=06/30/2009

PAGE TITLE: Power Block Diagram

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

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BOM VARIANTS - FSB

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3860	PCBA,MLB_2P,FSB,2.3,FOX,512_HYN,REN,J31,F327	J31_CMNPTS,SODIMM:FOXCONN,CPU:2_3GHZ,FB_512_HYNIX,FET:REN,DEVEL_BOM,GPUDEC:EXP,EEEE:F327
639-3861	PCBA,MLB_2P,FSB,2.3,MOL,512_SAM,FAIR,J31,F32C	J31_CMNPTS,SODIMM:MOLEX,CPU:2_3GHZ,FB_512_SAMSUNG,FET:FAIR,DEVEL_BOM,GPUDEC:EXP,EEEE:F32C
639-3862	PCBA,MLB_2P,FSB,2.6,MOL,1G_HY,FAIR,J31,F325	J31_CMNPTS,SODIMM:MOLEX,CPU:2_6GHZ,FB_1G_HYNIX_A_DIE,FET:FAIR,DEVEL_BOM,GPUDEC:EXP,EEEE:F325
639-3863	PCBA,MLB_2P,FSB,2.6,FOX,1G_SAM,REN,J31,F324	J31_CMNPTS,SODIMM:FOXCONN,CPU:2_6GHZ,FB_1G_SAMSUNG,FET:REN,DEVEL_BOM,GPUDEC:EXP,EEEE:F324
639-3864	PCBA,MLB_2P,FSB,2.7,FOX,1G_HY,REN,J31,F328	J31_CMNPTS,SODIMM:FOXCONN,CPU:2_7GHZ,FB_1G_HYNIX_A_DIE,FET:REN,DEVEL_BOM,GPUDEC:EXP,EEEE:F328
639-3865	PCBA,MLB_2P,FSB,2.7,MOL,1G_SAM,FAIR,J31,F329	J31_CMNPTS,SODIMM:MOLEX,CPU:2_7GHZ,FB_1G_SAMSUNG,FET:FAIR,DEVEL_BOM,GPUDEC:EXP,EEEE:F329
607-9557	CMN PTS,PCBA,MLB_KEPLER,J31	J31_COMMON
085-4620	J31 MLB_KEP_2P DEVELOPMENT BOM	J31_DEVEL:PVT

SUB BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4620	1	J31 MLB_KEP_2P DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9557	1	CMN PTS,PCBA,MLB_KEP_2P,J31	CMNPTS	CRITICAL	J31_CMNPTS

BOM GROUPS

BOM GROUP	BOM OPTIONS
J31_COMMON	ALTERNATE,COMMON,J31_COMMON1,J31_COMMON2,J31_PROGPARTS,J31_PROGPARTS1,UVGLUE_J31,J31_PVT
J31_COMMON1	CPUMEM_S0,RAMCFG_SLOT,USBHUB2513B,HUB_3NONREM,SMC_PACKAGE:PROD,MOJO:YES,TBTHV:P15V,SKIP_5V3V3:AUDIBLE
J31_COMMON2	BTPWR:S4,TPAD:Z2,T29:YES,TBTBST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR,LPCPLUS_R:YES,MEM_VDD_SEL:GPIO15,GPU:2P
J31_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:FSB,ENETROM_PROG:FSB,T29ROM:PROG,T29MCU:PROG
J31_PROGPARTS1	SMC_PROG:RR,BOOTROM_PROG:FSB
J31_PVT	VREF:PROD,XDP,XDP_CPU:BPM,BKLT:PROD,LOADISNS:NO,XWLOADISNS:NO
J31_DEVEL:ENG	DDRVREF_DAC,VREF:ENG_M3,IVB_PPT_XDP,GMUX_JTAG_CONN,LPCPLUS_CONN:YES,BKLT:ENG,S0PGOOD_ISL,CPURIPPLE_ENG,LOADISNS:YES,XWLOADISNS:YES,DEBUG_ADC
J31_DEVEL:FSB	DDRVREF_DAC,VREF:ENG_M3,IVB_PPT_XDP,LPCPLUS_CONN:YES,BKLT:PROD,S0PGOOD_ISL,LOADISNS:YES,XWLOADISNS:NO
J31_DEVEL:PVT	LPCPLUS_CONN:YES,XDP_CONN_CPU
IVB_PPT_XDP	XDP,XDP_CONN_PCH,XDP_CONN_CPU,XDP_CPU:BPM,XDP_PCH

BOM GROUP	BOM OPTIONS
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4266	1	IC,CPU,IVB,S,RBMP,PRQ,E1,2.3,45W,4+2,1.2,GM,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4267	1	IC,CPU,IVB,S,RBMM,PRQ,E1,2.6,45W,4+2,1.25,GM,BGA	U1000	CRITICAL	CPU:2_6GHZ
337S4268	1	IC,CPU,IVB,S,RBMK,PRQ,E1,2.7,45W,4+2,1.25,GM,BGA	U1000	CRITICAL	CPU:2_7GHZ
337S4269	1	IC,PCH,PPT,C1,SLJ8C,PRQ,BD82HM77	U1800	CRITICAL	
337S4239	1	IC,GPU,NV GK107-GTX-QS-A2	U8000	CRITICAL	
338S1072	1	IC,ASSP,LIGHTRIDGE,PRQ,S LJJY,FCBGA,15X15MM,C1	U3600	CRITICAL	T29:YES
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
353S3055	1	IC,PJ3VCDF212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
333S0619	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,G-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0620	4	IC,SDRAM,GDDR5,32MX32,1.5GHz,VEGA 44NM,B-DIE	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0631	4	IC,SGRAM,GDDR5,64MX32,5GBPS,D-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0630	4	IC,SGRAM,GDDR5,64MX32,5GBPS,A-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX_A_DIE
333S0609	4	IC,SGRAM,GDDR5,64MX32,4.2GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX_M_DIE
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_J31	CRITICAL	UVGLUE_J31
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID
376S0964	2	RJK0225	Q7330,Q8360	CRITICAL	FET:REN
376S0965	2	RJK0225	Q7335,Q8361	CRITICAL	FET:REN
376S0979	2	FDMC8225	Q7330,Q8360	CRITICAL	FET:FAIR
376S0874	2	FDMC8202S	Q7335,Q8361	CRITICAL	FET:FAIR
376S0826	1	FET,N-CH,30V,3.6MOHM,LF,HF,RJK0332DPB	Q7630	CRITICAL	FET:REN
376S0617	1	FET,N-CH,30V,30A,6.7MOHM,RJK0305DPB	Q7635	CRITICAL	FET:REN
376S0917	1	FET,N-CH,30V,3.6MOHM,LF,HF,FDMS8333S	Q7630	CRITICAL	FET:FAIR
376S1018	1	FET,N-CH,30V,14A,13MOHM,FDMS8349	Q7635	CRITICAL	FET:FAIR

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F327]	CRITICAL	EEEE:F327
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F32C]	CRITICAL	EEEE:F32C
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F325]	CRITICAL	EEEE:F325
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F324]	CRITICAL	EEEE:F324
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F328]	CRITICAL	EEEE:F328
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F329]	CRITICAL	EEEE:F329

Alternate Parts

(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	RDHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Delta/Vishay/TDK alt for Cynteс
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	ASSY OPTIONS FOR ALT TO ST MICRO
335S0550	335S0777		ALL	add 4K Byte as alternative to 2K
371S0709	371S0652		ALL	NXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps
514-0788	514-0671		ALL	Acon (with Tolmar) alt to Acon
155S0578	155S0367		ALL	Taps Yuden alt to Murata inductors
138S0681	138S0638		ALL	Taps Yuden alt to Samsung caps.
138S0671	138S0673		ALL	Taps Yuden alt to Murata caps.
155S0625	155S0559		ALL	Murata alt to TDK cm mode filter
376S0777	376S0761		ALL	ABM alternate to Fairchild
157S0084	157S0055		ALL	TDK alternate for ethernet transformer
353S3312	353S3055		ALL	NXP alternate to Percom-ST mux
376S0958	376S0953		ALL	For QT350, Fairchild alt to Ren.
376S1053	376S0604		ALL	Radar 10567726
371S0713	371S0558		ALL	Radar 10562580
128S0311	128S0329		ALL	Radar 10557464
127S0134	127S0111		ALL	Radar 10360888
127S0127	127S0090		ALL	Radar 10382328
197S0431	197S0432		ALL	RADAR 10670230
197S0434	197S0343		ALL	RADAR 10739227
197S0435	197S0343		ALL	RADAR 10739227

PD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
452-1708	2	SCR,M1.6X0.35X6.0,D4,HO.3,BLK,M97	SODIMM_SCREW1,SODIMM_SCREW2	CRITICAL	
452-1708	2	SCR,M1.6X0.35X6.0,D4,HO.3,BLK,M97	SODIMM_SCREW3,SODIMM_SCREW4	CRITICAL	
725-1607	1	INSULATOR,GPU,J31	GPU_INSULATOR	CRITICAL	

Programmables - All Builds

PSOC

341S3099	1	IC,TP PSOC,K0x,DVT,PVT,J31	U5701	CRITICAL	TPAD_PROG:PROTO0
341S3351	1	IC,TP PSOC,PROTO1,J31	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3227	1	IC,TP PSOC,PROTO2,PROTO3-ZZ,J31	U5701	CRITICAL	TPAD_PROG:PROTO3
341S3489	1	IC,TP PSOC,PIB,J31	U5701	CRITICAL	TPAD_PROG:PIB
341S3522	1	IC,TP PSOC,FSB,J31	U5701	CRITICAL	TPAD_PROG:FSB

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F,J31	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CY7C63823-LFXC	U4800	CRITICAL	IR_PROG
341S3430	1	IC,T29 EEPROM,LR,J30/J31	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3365	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25,J31	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
335S0852	1	IC,GPUROM,J31,BLANK	U8701	CRITICAL	GPUROM:BLANK

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K90I/K91x,J31	U3990	CRITICAL	ENETROM_PROG:PROTO3
341S3492	1	IC,PRGRMD,ENET,SPI ROM,FSB,J30/J31	U3990	CRITICAL	ENETROM_PROG:FSB

SMC

338S0895	1	IC,SMC,MSB/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S3258	1	IC,SMC,DEVELOPMENT-PROTO0,J31	U4900	CRITICAL	SMC_PROG:PROTO0
341S3294	1	IC,SMC,DEVELOPMENT-PROTO1,J31	U4900	CRITICAL	SMC_PROG:PROTO1
341S3401	1	IC,EXTERNAL,PROTO2,PROTO3,J31	U4900	CRITICAL	SMC_PROG:PROTO3
341S3481	1	IC,SMC,EXTERNAL,PIB,V2.1A83,A3,J31	U4900	CRITICAL	SMC_PROG:A3_PIB
341S3296	1	IC,SMC,EXTERNAL,FSB,V2.1A143,J31	U4900	CRITICAL	SMC_PROG:FSB
341S3297	1	IC,SMC,EXTERNAL,RISKRAMP,J31	U4900	CRITICAL	SMC_PROG:RR

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S3257	1	IC,EFI,ROM,PROTO0, J31	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3344	1	IC,EFI,ROM,PROTO1, J31	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3419	1	IC,EFI,ROM,PROTO2,J31	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3454	1	IC,EFI,ROM,PROTO3,J31	U6100	CRITICAL	BOOTROM_PROG:PROTO3
341S3510	1	IC,EFI,ROM,POST-PIB,J31	U6100	CRITICAL	BOOTROM_PROG:PIB2
341S3476	1	IC,EFI,ROM,FSB,J31	U6100	CRITICAL	BOOTROM_PROG:FSB

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
PP5V_S0 — FAN_LT_PWM — FAN_LT_TACH — GND

J5660 (RIGHT FAN CONN)

PP5V_S0 — FAN_RT_PWM — FAN_RT_TACH — GND

J6780 (MIC CONN)

BI_MIC_N — BI_MIC_SHIELD — BI_MIC_P — GND — 2 TPs

J5100

GND — 6 TPs
PP5V_S0
PP3V42_G3H

J6781 & J6782 (SPEAKERS CONN)

SPKRCONN_L_OUT_P — SPKRCONN_L_OUT_N — SPKRCONN_R_OUT_P — SPKRCONN_R_OUT_N — SPKRCONN_S_OUT_P — SPKRCONN_S_OUT_N — GND — 4 TPs

J9000 (LVDS CONN)

PP3V3_SW_LCD — 2 TP needed
PP3V3_S0 — 3 TP needed
PPVOUT_S0_LCDBKLT
LVDS_DDC_CLK
LVDS_DDC_DATA
LVDS_CONN_A_DATA_P<0>
LVDS_CONN_A_DATA_N<0>
LVDS_CONN_A_DATA_P<1>
LVDS_CONN_A_DATA_N<1>
LVDS_CONN_A_DATA_P<2>
LVDS_CONN_A_DATA_N<2>
LVDS_CONN_A_CLK_F_P
LVDS_CONN_A_CLK_F_N
LVDS_CONN_B_DATA_P<0>
LVDS_CONN_B_DATA_N<0>
LVDS_CONN_B_DATA_P<1>
LVDS_CONN_B_DATA_N<1>
LVDS_CONN_B_DATA_P<2>
LVDS_CONN_B_DATA_N<2>
LVDS_CONN_B_CLK_F_P
LVDS_CONN_B_CLK_F_N
LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
GND — 8 TPs

J4500 (SATA ODD CONN)

PP5V_SW_ODD — 4 TPs
SMC_ODD_DETECT
SATA_ODD_D2R_C_P
SATA_ODD_D2R_C_N
SATA_ODD_R2D_P
SATA_ODD_R2D_N
GND — 7 TPs

J4501 (SATA HDD CONN)

PP5V_S0_HDD_FLT — 4 TPs
SATA_HDD_R2D_P
SATA_HDD_R2D_N
SATA_HDD_D2R_C_N
SATA_HDD_D2R_C_P
GND — 8 TPs

IR_RX_OUT
PP5V_S3_IR_R
SSD_OOBD2R_L
SSD_OOBR2D_L

J5815 (KBD BACKLIGHT CONN)

KBDLED_ANODE — 2 TPs
SMC_KDBLED_PRESENT_L
GND

J5713 (KEY BOARD CONN)

PP3V3_S4
PP3V42_G3H
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
GND

J3501 & J3502 (AIRPORT/BT/CAMERA CONN)

PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
AP_CLKREQ_O_L
PCIE_WAKE_L
WIFI_EVENT_L
AP_RESET_CONN_L
PP3V3_WLAN — 6 TPs
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_2_S3_SDA
SMBUS_SMC_2_S3_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
GND — 10 TPs

PP3V3_S3R54_BT_F
USB_BT_CONN_P
USB_BT_CONN_N

J6950 (BAT CONN)

SYS_DETECT_L

J5800 (IPD FLEX CONN)

PP18V5_Z2
PP3V3_S4
PP5V_S5_CUMULUS
Z2_HOST_INTN
Z2_MOSI
Z2_CS_L
Z2_DEBUG3
Z2_MISO
Z2_BOOST_EN
Z2_SCLK
Z2_CLKIN
Z2_KEY_ACT_L
Z2_RESET
PSOC_F_CS_L
PICKB_L
PSOC_MISO
PSOC_MOSI
PSOC_SCLK
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
GND — 2 TPs needed

J6900 (DC POWER CONN)

ADAPTER_SENSE
PP18V5_DCIN_FUSE — 2 TPs
GND — 2 TPs

J6950 (MAIN BATT CONN)

PPVBAT_G3H_CONN — 3 TPs
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
SYS_DETECT_L
GND — 7 TPs

J6955 (BAT LED CONN)

PP3V42_G3H — 3 TPs
SMBUS_SMC_5_G3_SDA
SMBUS_SMC_5_G3_SCL
SMC_BIL_BUTTON_L
SMC_LID_R
GND — 7 TPs

FUNC_TEST
BKLT_EN
ISSP_SCLK_P1_1
ISSP_SDATA_P1_0
LCD_BKLT_PWM
LPCPLUS_GPIO
LPCPLUS_RESET_L
LPC_AD<0..3>
LPC_CLK33M_LPCPLUS
LPC_FRAME_L
LPC_PWRDWN_L
LPC_SERIRQ
PM_CLKRUN_L
PM_SYSRST_L
SMC_ONOFF_L
SMC_RESET_L
SMC_RX_L
SMC_TCK
SMC_TDI
SMC_TDO
SMC_TMS
SMC_ROMBOOT
SMC_TX_L
SPIROM_USE_MLB
SPI_ALT_CLK
SPI_ALT_CS_L
SPI_ALT_MISO
SPI_ALT_MOSI
SYS_LED_ANODE_R

J6950 (BIL CABLE CONN)

PP5V_S3_IR_R
SMC_LID_R
IR_RX_OUT
SYS_LED_ANODE
GND

NO_TEST=TRUE

TBT_R2D_C_P<1..0>
TBT_R2D_C_N<1..0>

TBTDPA_ML_P<3..0>
TBTDPA_ML_N<3..0>
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_ML_C_P<3..0>
DP_TBTSNK0_ML_C_N<3..0>
DP_TBTSNK0_ML_P<3..0>
DP_TBTSNK0_ML_N<3..0>
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_ML_C_P<3..0>
DP_TBTSNK1_ML_C_N<3..0>
DP_TBTSNK1_ML_P<3..0>
DP_TBTSNK1_ML_N<3..0>
TP_DP_TBTSRC_AUXCH_CN
TP_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_ML_C_P<3..0>
TP_DP_TBTSRC_ML_C_N<3..0>
DP_SDRVA_ML_C_P<0>
DP_SDRVA_ML_C_N<0>
DP_SDRVA_ML_C_P<2>
DP_SDRVA_ML_C_N<2>
DP_SDRVA_ML_P<0>
DP_SDRVA_ML_N<0>
DP_SDRVA_ML_P<2>
DP_SDRVA_ML_N<2>
TP_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L
PEG_D2R_C_P<7..0>
PEG_D2R_C_N<7..0>
PEG_R2D_P<7..0>
PEG_R2D_N<7..0>

POWER RAILS

FUNC_TEST
PM_SLP_S3_L — PP0V75_S0_DDRVTT — PP1V05_S0 — PP1V05_S0GPU — PP1V0_FW_FWPHY — PP1V2_ENET — PP1V2_S0 — PP1V5_S3
PP1V8_S0
PP3V3_ENET
PP3V3_FW_FWPHY
PP3V3_S0
PP3V3_S3
PP3V3_S5
PP3V3_S5_AVREF_SMC
PP3V42_G3H
PP5V_S0
PP5V_S3
PPBUS_G3H
PPDCIN_G3H
PPVCORE_GPU
PPVCORE_S0_CPU
PPVP_FW
PPVTTDDR_S3

NC NO_TESTS

NO_TEST
TP_FW643_SCIFCLK
TP_FW643_SCIFDAIN
TP_FW643_SCIFDOUT
TP_FW643_SCIFMC
TP_FW643_SDA
TP_FW643_SE
TP_FW643_SM
TP_FW643_CE
TP_FW643_FW620_L
TP_FW643_JASI_EN
DMI_S2N_N<1>
DMI_S2N_P<1>
FDI_DATA_P<1>
FDI_DATA_N<1>
FDI_FSYNC<1..0>
FDI_LSYNC<1..0>
FDI_INT
FDI_DATA_N<7..4>
FDI_DATA_P<7..4>

TP_FW643_VAUX_ENABLE
TP_FW643_VBUF
TP_FW643_TCK
TP_FW643_TMS
TP_SMC_P10
TP_P7_7
TP_PSOC_SCL
TP_PSOC_SDA
TP_SMC_P24
DC_TEST_BH1_8G2
DC_TEST_BH3_8J2
TP_USB_HUB1_OCS1
TP_USB_HUB1_PRTPWR1
TP_USB_HUB2_OCS1
TP_USB_HUB2_PRTPWR1
TP_DC_TEST_A62
TP_DC_TEST_D65

ICT Test Points

CPU NO_TESTs

NO_TEST
TP_CPU_RSVD<65..62> — NC_TP_CPU_RSVD<65..62>
TP_CPU_RSVD<58..45> — NC_TP_CPU_RSVD<58..45>
TP_CPU_RSVD<43..32> — NC_TP_CPU_RSVD<43..32>
TP_CPU_RSVD<27..26> — NC_TP_CPU_RSVD<27..26>
TP_CPU_RSVD<24..15> — NC_TP_CPU_RSVD<24..15>
TP_CPU_RSVD<2..1> — NC_TP_CPU_RSVD<2..1>
TP_CPU_RSVD_NCTF<8..5> — NC_TP_CPU_RSVD_NCTF<8..5>

NC NO_TESTs

NO_TEST
TP_CRT_IG_BLUE — NC_CRT_IG_BLUE
TP_CRT_IG_GREEN — NC_CRT_IG_GREEN
TP_CRT_IG_RED — NC_CRT_IG_RED
TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA
TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC
TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC
TP_LVDS_IG_CTRL_CLK — NC_LVDS_IG_CTRL_CLK
TP_LVDS_IG_CTRL_DATA — NC_LVDS_IG_CTRL_DATA
TP_PCH_LVDS_VBG — NC_PCH_LVDS_VBG

TP_HDA_SDIN1 — NC_HDA_SDIN1
TP_HDA_SDIN2 — NC_HDA_SDIN2
TP_HDA_SDIN3 — NC_HDA_SDIN3

TP_DP_TBTSRC_AUXCH_CP — NC_TP_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN — NC_TP_DP_TBTSRC_AUXCH_CN
TP_TBT_PCIE_RESET0_L — NC_TP_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L — NC_TP_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L — NC_TP_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L — NC_TP_TBT_PCIE_RESET3_L

TP_TBT_MONDC0 — NC_TBT_MONDC0
TP_TBT_MONDC1 — NC_TBT_MONDC1
TP_TBT_MONOBSP — NC_TBT_MONOBSP
TP_TBT_MONOBSN — NC_TBT_MONOBSN
TP_DP_TBTSRC_ML_CP<0..3> — NC_DP_TBTSRC_ML_CP<0..3>
TP_DP_TBTSRC_ML_CN<0..3> — NC_DP_TBTSRC_ML_CN<0..3>

NO_TEST
TP_AUD_GPIO_2
TP_AUD_GPIO_1
TP_AUD_LO1_L_N
TP_AUD_LO1_L_P
TP_BKL_FAULT
TP_SPI_DESCRIPTOR_OVERRIDE_L
TP_XDPPCH_HOOK2
TP_XDPPCH_HOOK3
TP_GMUX_PL68
CPUIMVP_BOOT1
CPUIMVP_BOOT2
TP_LVDS_S0_PCH_VCCAPLLEXP

TP_PCI_PME_L — NC_PCI_PME_L
TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3
TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PE5N — NC_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P — NC_PCIE_CLK100M_PE5P
TP_PCIE_CLK100M_PE6N — NC_PCIE_CLK100M_PE6N
TP_PCIE_CLK100M_PE6P — NC_PCIE_CLK100M_PE6P
TP_PCIE_CLK100M_PE7N — NC_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P — NC_PCIE_CLK100M_PE7P
TP_PSOC_P1_3 — NC_PSOC_P1_3
TP_SATA_B_D2RN — NC_SATA_B_D2RN
TP_SATA_B_D2RP — NC_SATA_B_D2RP
TP_SATA_B_R2D_CN — NC_SATA_B_R2D_CN
TP_SATA_B_R2D_CP — NC_SATA_B_R2D_CP
TP_SATA_D_D2RN — NC_SATA_D_D2RN
TP_SATA_D_D2RP — NC_SATA_D_D2RP
TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP
TP_SATA_E_D2RN — NC_SATA_E_D2RN
TP_SATA_E_D2RP — NC_SATA_E_D2RP
TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP
TP_SATA_F_D2RN — NC_SATA_F_D2RN
TP_SATA_F_D2RP — NC_SATA_F_D2RP
TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP
TP_SMC_P41 — NC_SMC_P41

PCH ALIASES

NC_LPC_DREQ0_L — TP_LPC_DREQ0_L
TP_CLINK_CLK — NC_CLINK_CLK
TP_CLINK_DATA — NC_CLINK_DATA
TP_CLINK_RESET_L — NC_CLINK_RESET_L
TP_PCIE_CLK100M_PEBN — NC_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP — NC_PCIE_CLK100M_PEBP

NC NO_TESTs

NO_TEST
NC_SMC_FAN_3_TACH
NC_SMC_FAN_3_CTL
NC_SMC_FAN_2_TACH
NC_SMC_FAN_2_CTL
NC_FW2_TPBP
NC_FW2_TPBN
NC_FW2_TPBIAS
NC_FW2_TPAP
NC_FW2_TPAN
NC_FW0_TPBP
NC_FW0_TPBN
NC_FW0_TPAP
NC_ESTARLDO_EN
NC_ALS_GAIN

TP_FW643_AVREG — NC_FW643_AVREG
TP_FW643_TDI — NC_FW643_TDI

TP_DP_IG_C_HPD — NC_DP_IG_C_HPD
TP_DP_IG_C_CTRL_CLK — NC_DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA — NC_DP_IG_C_CTRL_DATA
TP_DP_IG_C_MLP<3..0> — NC_DP_IG_C_MLP<3..0>
TP_DP_IG_C_MLN<3..0> — NC_DP_IG_C_MLN<3..0>
TP_DP_IG_C_AUXP — NC_DP_IG_C_AUXP
TP_DP_IG_C_AUXN — NC_DP_IG_C_AUXN
TP_DP_IG_D_HPD — NC_DP_IG_D_HPD
TP_DP_IG_D_CTRL_CLK — NC_DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA — NC_DP_IG_D_CTRL_DATA
TP_DP_IG_D_MLP<3..0> — NC_DP_IG_D_MLP<3..0>
TP_DP_IG_D_MLN<3..0> — NC_DP_IG_D_MLN<3..0>
TP_DP_IG_D_AUXP — NC_DP_IG_D_AUXP
TP_DP_IG_D_AUXN — NC_DP_IG_D_AUXN

TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN
TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP
TP_SDVO_STALLN — NC_SDVO_STALLN
TP_SDVO_STALLP — NC_SDVO_STALLP
TP_SDVO_INTN — NC_SDVO_INTN
TP_SDVO_INTP — NC_SDVO_INTP

TP_GPU_BUFRST_L — NC_GPU_BUFRST_L
TP_GPU_GSTATE<0> — NC_GPU_GSTATE<0>
TP_GPU_GSTATE<1> — NC_GPU_GSTATE<1>
TP_GPU_MIOA_D<9..0> — NC_GPU_MIOA_D<9..0>
TP_GPU_MIOA_DE — NC_GPU_MIOA_DE

TP_LVDS_IG_BKL_PWM — NC_LVDS_EG_BKL_PWM
TP_LVDS_IG_B_CLKN — NC_LVDS_IG_B_CLKN
TP_LVDS_IG_B_CLKP — NC_LVDS_IG_B_CLKP
TP_LVDS_IG_BKL_PWM — NC_LVDS_IG_B_BKL_PWM

MEM_A_BA<2..0>
MEM_A_CKE<1..0>
MEM_A_CLK_N<1..0>
MEM_A_CLK_P<1..0>
MEM_A_CS_L<1..0>
MEM_A_ODT<1..0>
MEM_A_SA<1..0>
MEM_A_DQ<63..0>
MEM_A_DQS_N<7..0>
MEM_A_DQS_P<7..0>
FB_A0_DQ<31..0>
FB_A0_A<8..0>
FB_A0_ABI_L
FB_A0_EDC<3..0>
FB_A0_WCLK_N<1..0>
FB_A0_WCLK_P<1..0>
FB_A0_DBI_L<3..0>
FB_A1_DQ<31..0>
FB_A1_A<8..0>
FB_A1_ABI_L
FB_A1_EDC<3..0>
FB_A1_WCLK_N<1..0>
FB_A1_WCLK_P<1..0>
FB_A1_DBI_L<3..0>
MEM_A_A<15..0>
MEM_A_CAS_L
MEM_A_RAS_L
MEM_A_WE_L
MEM_B_A<15..0>
MEM_B_CAS_L
MEM_B_RAS_L
MEM_B_WE_L

MEM_B_BA<2..0>
MEM_B_CKE<1..0>
MEM_B_CLK_N<1..0>
MEM_B_CLK_P<1..0>
MEM_B_CS_L<1..0>
MEM_B_ODT<1..0>
MEM_B_SA<1..0>
MEM_B_DQ<63..0>
MEM_B_DQS_N<7..0>
MEM_B_DQS_P<7..0>
FB_B0_DQ<31..0>
FB_B0_A<8..0>
FB_B0_ABI_L
FB_B0_EDC<3..0>
FB_B0_WCLK_N<1..0>
FB_B0_WCLK_P<1..0>
FB_B0_DBI_L<3..0>
FB_B1_DQ<31..0>
FB_B1_A<8..0>
FB_B1_ABI_L
FB_B1_EDC<3..0>
FB_B1_WCLK_N<1..0>
FB_B1_WCLK_P<1..0>
FB_B1_DBI_L<3..0>

NO_TEST=TRUE

CHGR_BOOT
CHGR_ICOMP_RC
CHGR_LGATE
CHGR_PHASE
CHGR_UGATE
CHGR_VCOMP
CPU_VCCSASENSE_DIV
CPUIMVP_AXG1_SNUB
CPUIMVP_AXG2_SNUB
CPUIMVP_BOOT1
CPUIMVP_BOOT1_RC
CPUIMVP_BOOT1G
CPUIMVP_BOOT1G_R
CPUIMVP_LGATE1
CPUIMVP_LGATE1G
CPUIMVP_LGATE2
CPUIMVP_LGATE2G
CPUIMVP_LGATE3
CPUIMVP_PH1_SNUB
CPUIMVP_PH2_SNUB
CPUIMVP_PH3_SNUB
CPUIMVP_PHASE1
CPUIMVP_PHASE1G
CPUIMVP_PHASE2
CPUIMVP_PHASE2G
CPUIMVP_PHASE3
CPUIMVP_SKIP
CPUIMVP_SLEW
CPUIMVP_TONA
CPUIMVP_TONB
CPUIMVP_VSW61
CPUIMVP_VSW62
CPUVCCIOS0_BOOT_RC
CPUVCCIOS0_DRVH
CPUVCCIOS0_DRVL
CPUVCCIOS0_FB
CPUVCCIOS0_LL
CPUVCCIOS0_OCSET
CPUVCCIOS0_RTN
CPUVCCIOS0_VBST
PCHVCCIOS0_BOOT_RC
PCHVCCIOS0_DRVH
PCHVCCIOS0_DRVL
PCHVCCIOS0_FB
PCHVCCIOS0_LL
PCHVCCIOS0_OCSET
PCHVCCIOS0_VBST
PPVCORE_S0_CPU_PH1_L
PPVCORE_S0_CPU_PH2_L
PPVCORE_S0_CPU_PH3_L
VCCSASO_BOOT_RC
VCCSASO_DRVL
VCCSASO_LL
VCCSASO_VBST

CPUIMVP_BOOT2
CPUIMVP_BOOT2_RC
CPUIMVP_BOOT2G
CPUIMVP_BOOT2G_RC
CPUIMVP_BOOT3
CPUIMVP_BOOT3_RC

CPUIMVP_UGATE1
CPUIMVP_UGATE1G
CPUIMVP_UGATE2
CPUIMVP_UGATE2G
CPUIMVP_UGATE3

DDRREG_TRIP
GFXIMVP_LGATE
GFXIMVP_LL_RC
GFXIMVP_PHASE
GFXIMVP_PHASE_L
GFXIMVP_UGATE
GFXIMVP_UGATE_R
GFXIMVP_VBST
GFXIMVP_VBST_R
GPUFB_BOOT_RC
GPUFB_DRVH
GPUFB_DRVL
GPUFB_LL
GPUFB_VBST
P1V05_GPU_DRVL
P1V05_GPU_DRVH
P1V05_GPU_LL
P1V05_GPU_VBST
P1V05_GPU_BOOT_RC
P1V8S0_FB
P1V8S0_SW
P3V3S5_CSP2_R
P3V3S5_DRVH
P3V3S5_DRVL
P3V3S5_LL
P3V3S5_SNUBR
P3V3S5_TG
P5V5G3H_BOOST
P5V5G3H_SW

DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_S2N_N<1..0>
DMI_S2N_P<1..0>
DMI_N2S_N<2..1>
DMI_N2S_P<3..1>

USB3_EXTB_RX_N
USB3_EXTB_RX_P
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
USB3_EXTB_TX_N
USB3_EXTB_TX_C_N
USB3_EXTB_TX_F_N
USB3_EXTB_TX_P
USB3_EXTB_TX_C_P
USB3_EXTB_TX_F_P

USB3_EXTA_RX_N
USB3_EXTA_RX_P
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
USB3_EXTA_TX_N
USB3_EXTA_TX_C_N
USB3_EXTA_TX_F_N
USB3_EXTA_TX_P
USB3_EXTA_TX_C_P
USB3_EXTA_TX_F_P

SYNC_MASTER=K18_MLB — SYNC_DATE=04/27/2010

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D C B A

G3H Rails

=PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V
  - =PPBUS_S0_LCDBKLT 90
  - =PPBUS_S5_FWPWRSW 39
  - =PPVIN_S5_HS_OTHER_ISNS_R 50
  - =PPVIN_S5_HS_COMPUTING_ISNS_R 50
  - =PPVIN_S5_HS_GPU_ISNS_R 50
  - =PPBUS_SW_TBTBST 8 35
  - =PPBUS_S0_VSENSE 49

=PPVIN_S5_HS_COMPUTING_ISNS 50
- PPVIN_S5_HS_COMPUTING_ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE
  - =PPVIN_S0_CPUIMVP 69 70
  - =PPVIN_S3_DDRREG 68
  - =PPVIN_S0_CPUVCCIOS0 71
  - =PPVIN_S0_CPUAXG 70
  - =PPVIN_S0_VCCSAS0 66
  - =PPVIN_S0_PCHVCCIOS0

=PPVIN_S5_HS_GPU_ISNS 50
- PPVIN_S5_HS_GPU_ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE
  - =PPVIN_S0GPU_P1V5 78
  - =PPVIN_S0_GFXIMVP 84
  - =PPVIN_S0GPU_P1V05 78

=PPVIN_S5_HS_OTHER_ISNS 50
- PPVIN_S5_HS_OTHER_ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE
  - =PPVIN_S5_P5VP3V3 67

=PP18V5_DCIN_CONN 64
- PPDCIN_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=18.5V, MAKE_BASE=TRUE
  - =PPDCIN_S5_CHGR 65
  - =PPDCIN_S5_VSENSE 49

=PP3V42_G3H_REG 64
- PP3V42_G3H — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
  - =PP3V3_S5_LPCPLUS 47
  - =PP3V3_S5_SMC 45 46 82
  - =PP3V42_G3H_BIL 64
  - =PP3V42_G3H_CHGR 65 74
  - =PP3V42_G3H_ONEWIREPROT 64
  - =PP3V42_G3H_PWRCTL 74
  - =PP3V42_G3H_SMBUS_SMC_5 48
  - =PP3V42_G3H_SMCUSBMUX 42
  - =PP3V42_G3H_TPAD 53
  - =PPVIN_S5_SMCVREF 46
  - =PPVBAT_G3_SYSCLK 24
  - =PP3V42_G3H_AUDIO 59

For PCH RTC Power

=PPVRTC_G3_OUT 24
- PPVRTC_G3H — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
  - =PPVRTC_G3_PCH 16 17 20

5V Rails

=PP5V_S5_LDO 67
- PP5V_S5 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE
  - =PP5V_S5_P1V5S3RS0FET 73
  - =PP5V_S5_P5VSUSFET 73
  - =PP5V_S5_TPAD 54
  - =PP5V_S5_ISNS

=PP5V_SUS_FET 73
- PP5V_SUS — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE
  - =PP5V_SUS_PCH 22

=PP5V_S3_REG 67
- PP5V_S3 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE
  - =PP5V_S3_ALSCAMERA 32
  - =PP5V_S3_DDRREG 68
  - =PP5V_S5_DEBUG_ADC_AVDD 104
  - =PP5V_S5_DEBUG_ADC_DVDD 104
  - =PP5V_S3_AUDIO
  - =PP5V_S3_IR 41 44
  - =PP5V_S3_MEMRESET 26
  - =PP5V_S3_ODD 41
  - =PP5V_S3_P5VS0FET 73
  - =PP5V_S3_USB 42
  - =PP5V_S3_SYSLED 46
  - =PP5V_S3_P5VS0SW
  - =PP5V_S3_P3V3S0SW
  - =PP5V_S3_GFXIMVP 84

=PP5V_S0_FET 73
- PP5V_S0 — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE

=PP5V_S0_ISNS 103
- =PP5V_S0_BKL 90
- =PP5V_S0_CPUIMVP 69 70
- =PP5V_S0_CPUVCCIOS0 71
- =PP5V_S0_FAN_LT 52
- =PP5V_S0_FAN_RT 52
- =PP5V_S0_VCCSAS0 66
- =PP5V_S0_VMON 74
- =PP5V_S0_HDD 41
- =PP5V_S0_KBDLED 54
- =PP5V_S0_LPCPLUS 47
- =PP5V_S0_PCH 22 24
- =PP5V_S0GPU_P1V05 78
- =PP5V_S0_AUDIO_XW 8
- =PP5V_S0_RMC 105
- =PP5V_S0GPU_P1V5 78

3.3V Rails

=PP3V3_S4_FET 73
- PP3V3_S4 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=3.3V

=PP3V3_S4_SD_HPD 30
- =PP3V3_S4_TPAD 53 54

=PP3V3_S4_BT 32
- =PP3V3_S4_SMC 46

=PP3V3_SUS_FET 73
- PP3V3_SUS — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=3.3V
  - =PP3V3_SUS_P1V05SUSLDO 72
  - =PP3V3_SUS_PCH_VCCSUS 20 22
  - =PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
  - =PP3V3_SUS_PCH_GPIO 16 17 18 19
  - =PP3V3_SUS_PCH_VCCSUS_USB 20 22
  - =PP3V3_SUS_CNTRL 74
  - =PP3V3_SUS_SMC 46
  - =PP3V3_SUS_ROM 56
  - =PP3V3_SUS_PCH_VCC_SPI 20 22

=PP3V3_S5_REG 67
- PP3V3_S5 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_GPU_P3V3GPUFET 73
  - =PP3V3_S0_P3V3S0FET 73
  - =PP3V3_S3_P3V3S3FET 73
  - =PP3V3_S4_P3V3S4FET 73
  - =PP3V3_S5_SYSCLK 24
  - =PP3V3_S5_LCD 85
  - =PP3V3_FW_P3V3FWFET 39
  - =PP3V3_S5_P1V2P1V8 72
  - =PP3V3_S5_PCH 17
  - =PP3V3_S5_PCHPWRGD 92
  - =PP3V3_S5_PCH_GPIO 19
  - =PP3V3_S5_CPU_VCCDDR 26
  - =PP3V3_S5_MEMVDDSEL
  - =PP3V3_S5_PCH_VCCDSW 20 22
  - =PP3V3_S5_VMON 74
  - =PP3V3_S5_XDP 23
  - =PP3V3_S5_P3V3SUSFET 73
  - =PP3V3_S5_PWRCTL 74
  - =PP3V3_S5_P1V5S0 72
  - =PP3V3_S5_SMCBATLOW 46
  - =PP3V3_S4_TBTAPWRSW 88

=PP3V3_S3_FET 73
- PP3V3_S3_FET — MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_S3_ISNS_R 104

=PP3V3_S3_ISNS 104 103 49 7
- PP3V3_S3 — MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_S3_BT
  - =PP3V3_S3_GMUX 89
  - =PP3V3_S3_MEMRESET 26
  - =PP3V3_S3_P3V3ENETFET 74
  - =PP3V3_S3_SMBUS_SMC_2_S3 48
  - =PP3V3_S3_SMBUS_SMC_3 48
  - =PP3V3_S3_SMS 55
  - =PP3V3_S3_USB_HUB 25
  - =PP3V3_S3_USB_RESET 25
  - =PP3V3_S3_VREFMRGN 31
  - =PP3V3_S3_WLAN 32
  - =PP3V3_S3_ISNS 7 49 103 104
  - =PP3V3_S3_PCH_GPIO 18 24
  - =PP3V3_S3_USBMUX 25
  - =PP3V3_S3_SDBUF 24

=PP3V3_S0_FET 73
- PP3V3_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.075 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_S0_XDP 23
  - =PP3V3_S0_ENETPHY 36
  - =PP3V3_S0_AUDIO 57 62 63
  - =PP3V3_S0_BKL_VDDIO 90
  - =PP3V3_S0_DPSDRVA 87
  - =PP3V3_S0_HS_ISNS
  - =PP3V3_S0_CPUTHMSNS 51
  - =PP3V3_S0_DDC_LCD 85
  - =PP3V3_S0_ISNS 49 50 103 104
  - =PP3V3_S0_TBTPWRCTL 35
  - =PP3V3_S0_DPMUX 86
  - =PP3V3_S0_FAN_LT 52
  - =PP3V3_S0_FAN_RT 52
  - =PP3V3_S0_FWPWRCTL 39
  - =PP3V3_S0_FWLATEVG 39 40
  - =PP3V3_S0_CPU_VCCIO_SEL 12
  - =PP3V3_S0_GMUX 86 89
  - =PP3V3_S0_P3V3TBTFET 35
  - =PP3V3_S0_GPUTHMSNS 51
  - =PP3V3_S0_LVDSDDCMUX 86
  - =PP3V3_S0_ODD 41
  - =PP3V3_S0_PCH 16 22
  - =PP3V3_S0_PCH_GPIO 16 17 18 19 30
  - =PP3V3_S0_PCH_VCC3_3_CLK 22
  - =PP3V3_S0_PCH_VCC3_3_GPIO 20 22
  - =PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
  - =PP3V3_S0_PCH_VCC3_3_PCI 20 22
  - =PP3V3_S0_PCH_VCC3_3_SATA 20 22
  - =PP3V3_S0_PCH_VCCADAC 22
  - =PP3V3_S0_PCH_VCCA_LVDS 20
  - =PP3V3_S0_PWRCTL 74 92
  - =PP3V3_S0_RSTBUF 24
  - =PP3V3_S0_SB_PM 24 92
  - =PP3V3_S0_SDCARD 30
  - =PP3V3_S0_SMBUS_PCH 48
  - =PP3V3_S0_SMBUS_SMC_0_S0 48
  - =PP3V3_S0_SMBUS_SMC_1_S0 48
  - =PP3V3_S0_SMC 41
  - =PP3V3_S0_TPAD 54
  - =PP3V3_S0_VMON 74
  - =PPSPD_S0_MEM_A 27
  - =PPSPD_S0_MEM_B 29
  - =PP3V3_S0_HDD 41
  - =PP3V3_S0_P1V8GPUFET 73
  - =PP3V3_S0_IMVPISNS 50
  - =PP3V3_S0_T29I2C 48
  - =PP3V3_S0_TBT_HPD_GPU

T29 Rails

=PP3V3_TBT_FET 35
- PP3V3_TBT — MIN_LINE_WIDTH=0.4 MM, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE
  - =PP3V3_T29_PCH_GPIO 16 19
  - =PPVDDIO_T29_CLK 24
  - =PP3V3_TBT_RTR 33 34 35
  - =PP3V3_T29_JTAG 89

=PP1V05_TBT_FET 35
- PP1V05_TBT — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE
  - =PP1V05_TBT_RTR_R 104

=PP15V_TBT_REG 35 8
- PP15V_TBT — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=15V, MAKE_BASE=TRUE
  - =PPHV_SW_TBTAPWRSW 88

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG 72 — 2A max supply
- PP1V8_S0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V8_S0_GMUX 89
  - =PP1V8_S0_GPUFET 73
  - =PP1V8_S0_PCH_VCCTX_LVDS 22
  - =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
  - =PP1V8_S0_CPU_VCCPLL 14
  - =PP1V8R1V5_S0_PCH_VCCVRM 20
  - =PPVDDIO_S0_SBCLK 24

=PP1V8_S0_CPU_VCCPLL_R 14 12
- PP1V8_S0_CPU_VCCPLL_R — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.8V, MAKE_BASE=TRUE

=PPDDR_S3_REG 68
- PP1V5_S3_REG — MIN_LINE_WIDTH=0.8 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V5_S3_ISNS_R 103

=PP1V5_S3_ISNS 103
- PP1V5_S3 — MIN_LINE_WIDTH=0.8 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V5_S3_DDR_ISNS_R 49
  - =PPVIN_S3_P1V5S3RS0_FET 73

=PP1V5_S3RS0_FET 73
- PP1V5_S3RS0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V5_S3_CPU_VCCDDR 10 13 15 26

=PP1V5_S3_DDR_ISNS 49
- PP1V5_S3_DDR — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V5_S3_MEMRESET 26
  - =PP1V5_S3_MEM_A 27
  - =PP1V5_S3_MEM_B 29
  - =PPVIN_S0_DDRREG_LDO 68
  - =PPDDR_S3_MEMVREF 31

=PP1V5_S0_REG 72
- PP1V5_S0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V5_S0_RDRVR 41
  - =PP1V5_S0_AUDIO 57
  - =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 24
  - =PP1V5_S0_VMON 74

=PPVTT_S3_DDR_BUF 68 31
- PPVTTDDR_S3 — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.75V, MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO 68
- PP0V75_S0_DDRVTT — MIN_LINE_WIDTH=2 mm, MIN_NECK_WIDTH=0.17 mm, VOLTAGE=0.75V, MAKE_BASE=TRUE
  - =PP0V75_S0_MEM_VTT_A 27
  - =PP0V75_S0_MEM_VTT_B 29
  - =PPVTT_S0_VTTCLAMP 26

=PP1V2_S0_REG 72
- PP1V2_S0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.2V, MAKE_BASE=TRUE
  - =PP1V2_S0_GMUX 89

=PP1V05_SUS_LDO 72
- PP1V05_SUS — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE
  - =PP1V05_SUS_PCH_JTAG 23

=PPCPUVCCIO_S0_REG 71
- PP1V05_S0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE
  - =PP1V05_S0_CPU_VCCIO 9 10 12 13 14
  - =PPVCCIO_S0_XDP 23
  - =PPVCCIO_S0_CPUIMVP 69
  - =PPVCCIO_S0_SMC 46
  - =PP1V05_S0_RMC 105
  - =PP1V05_S0_FWPWRCTL 39
  - =PP1V05_FW_P1V0FWFET 39
  - =PP1V05_S0_VMON 74
  - =PP1V05_S0_P1V05TBTFET 35
  - =PP1V05_S0_PCH_VCCIO_PLLPCIE 20
  - =PP1V05_S0_PCH_VCCADPLL 22
  - =PP1V05_S0_PCH_VCCIO 20 22
  - =PP1V05_S0_PCH_VCCIO_PCIE 17
  - =PP1V05_S0_PCH_VCCIO_SATA 16 20 22
  - =PP1V05_S0_PCH_VCCIO_CLK 7 20 22
  - =PP1V05_S0_PCH_VCCIO_USB 20 22
  - =PP1V05_S0_PCH_VCC_CORE 20 22
  - =PP1V05_S0_PCH_VCCASW 20 22
  - =PP1V05_S0_PCH_VCCIO_CLK 7 20 22
  - =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
  - =PP1V05_S0_PCH 16 22
  - =PP1V05_S0_PCH_VCCSSC 20 22
  - =PP1V05_S0_PCH_V_PROC_IO 20 22
  - =PP1V05_S0_PCH_VCCIO_PLLUSB 20
  - =PP1V05_S0_PCH_VCC_DMI 20 22
  - =PP1V05_S0_PCH_VCCIO_PLLFDI 20
  - =PP1V05_S0_PCH_VCCDMI_FDI 20
  - =PPPCHVCCIO_S0_REG 91

Backlight Rails

=PPBUS_SW_BKL 104 90
- PPBUS_SW_BKL — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE, VOLTAGE=12.8V

=PP3V3_ENET_FET 74
- PP3V3_ENET — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_ENET_PHY 24 36 72
  - =PPVDDIO_ENET_CLK 24
  - =PP3V3_ENET_SYSCLK 24

ENET Rails

=PP1V2_S3_ENET_PHY 72
- PP1V2_ENET — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.2V, MAKE_BASE=TRUE
  - =PP1V2_ENET_PHY 36

TBT Rails

=PP1V05_TBT_RTR 104 34
- PP1V05_TBT_RTR — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE

PPVIN_SW_TBTBST 35 — VOLTAGE=12.8V

"GPU" Rails

=PP3V3_S0GPU_FET 73
- PP3V3_S0GPU_FET — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.10MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_S0GPU_ISNS_R 104

=PP3V3_S0GPU_ISNS 104
- PP3V3_S0GPU — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.10MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_GPU_IFPX_PLLVDD 81
  - =PP3V3_GPU_LVDS_DDC 86
  - =PP3V3_S0_GFX3V3BIAS 84
  - =PP3V3_GPU_VDD33 75 81 82 83
  - =PP3V3_GPU_OSC

=PP1V8_GPU_FET 73
- PP1V8_S0GPU — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.15 MM, VOLTAGE=1.8V, MAKE_BASE=TRUE
  - =PP1V8_GPU_IFPAB_IOVDD 81

=PP1V5R1V35_GPU_REG 103 78
- PPGPUFB_S0 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE
  - =PP1V35_GPU_FBVDDQ 76 79 80
  - =PP1V35_GPU_S0_FB 77

=PP1V05_S0GPU_REG 78
- PP1V05_S0GPU — MIN_LINE_WIDTH=0.9 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE
  - =PP1V05_GPU_IFPAB_PLLVDD 81
  - =PP1V05_GPU_IFPCD_IOVDD 81
  - =PP1V05_GPU_IFPEF_IOVDD 81
  - =PP1V05_GPU_PEX_IOVDD 77 83
  - =PP1V05_GPU_PEX_PLLVDD 81 83

=PPVCORE_S0_GFX_REG 84
- PPVCORE_GPU — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.0V, MAKE_BASE=TRUE
  - =PPVCORE_GPU 76 83
  - =PPVCORE_GPU_REG 49

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG 70
- PPVCORE_S0_CPU — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, MAKE_BASE=TRUE, VOLTAGE=1.25V
  - =PPVCORE_S0_CPU 12 14 49 105

=PPVCORE_S0_AXG_REG 70 49
- PPVCORE_S0_AXG — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=1.05V
  - =PPVCORE_S0_CPU_VCCAXG 12 13 15

=PP1V5_S3_CPU_VCCDQ 15 12
- PP1V5_S3_CPU_VCCDQ — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE, VOLTAGE=1.5V

=PP1V05_S0_CPU_VCCPQE 14 12 8
- PP1V05_S0_CPU_VCCPQE — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE

=PPVCCSA_S0_REG 66 49
- PPVCCSA_S0_REG — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.9V, MAKE_BASE=TRUE
  - =PPVCCSA_S0_CPU 12 15

FireWire Rails

=PPBUS_FW_FET 39
- PPVP_FW — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=12.8V, MAKE_BASE=TRUE
  - =PPVP_FW_PORT1 40
  - =PPVP_FW_PHY_CPS_FET 40

=PP3V3_FW_FET 39
- PP3V3_FW_FWPHY — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - =PP3V3_FW_FWPHY 38 39 40

=PP1V0_FW_FET_R 39
- PP1V0_FW_FWPHY — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.0V, MAKE_BASE=TRUE
  - =PP1V0_FW_FWPHY 38 39

SYNC_MASTER=J31_MLB SYNC_DATE=08/29/2013

PAGE TITLE: Power Aliases

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Thermal Module Holes

ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0950 TH — GND_CHASSIS_FAN
SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0990 3R2P5 — GND_CHASSIS_BATTCONN

Tall EMI pogo pins

SH0930 POGO-2.00D-3.5H-K86-K87
SH0931 POGO-2.00D-3.5H-K86-K87
SH0902 POGO-2.00D-3.5H-K86-K87
SH0903 POGO-2.00D-3.5H-K86-K87
SH0904 POGO-2.00D-3.5H-K86-K87
SH0936 NOSTUFF POGO-2.00D-3.5H-K86-K87
SH0911 1.4DIA-SHORT-SILVER-K99
SH0910 1.4DIA-SHORT-SILVER-K99
SH0913 1.4DIA-SHORT-SILVER-K99
SH0912 1.4DIA-SHORT-SILVER-K99
SH0917 1.4DIA-SHORT-SILVER-K99
SH0901 1.4DIA-SHORT-SILVER-K99
SH0918 1.4DIA-SHORT-SILVER-K99
SH0914 1.4DIA-SHORT-SILVER-K99
GND_CHASSIS_AUDIO_JACK

NOSTUFF SH0932 POGO-2.00D-3.5H-K86-K87
SH0933 NOSTUFF POGO-2.00D-3.5H-K86-K87
SH0900 POGO-2.00D-3.5H-K86-K87
SH0916 POGO-2.00D-3.5H-K86-K87
SH0937 NOSTUFF POGO-2.00D-3.5H-K86-K87
SH0938 NOSTUFF POGO-2.00D-3.5H-K86-K87

Short (IO Row) EMI pogo pins

Fan Holes

ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

Left Speaker Holes

ZT0934 STDOFF-4.00D3.0H-TH
ZT0935 STDOFF-4.00D3.0H-TH
NOSTUFF SH0934 POGO-2.00D-3.5H-K86-K87
SH0935 NOSTUFF POGO-2.00D-3.5H-K86-K87

Keyboard / IPD Conn Protect

ZT0952 4.00D1.85H-M1.6X0.35
ZT0953 4.00D1.85H-M1.6X0.35

R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS0P — C0901 0.01UF 10% 10V XSR 201
R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS0N — C0902 0.01UF 10% 10V XSR 201
R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS2P — C0903 0.01UF 10% 10V XSR 201
R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS2N — C0904 0.01UF 10% 10V XSR 201

R9490 51 5% 1/20W MF 201 — T29_A_BIAS_R (VOLTAGE=3.3V) — C9490 0.1UF 10% 6.3V XSR 201 — =TBT_A_BIAS
PLACE_NEAR=C9490.1:2 mm

R0941 1K 5% 1/16W MF-LF 402 — DPLL_REF_CLK_P — DPLL_REF_CLK
R0940 1K 5% 1/16W MF-LF 402 — =PP1V05_S0_CPU_VCCPQE — DPLL_REF_CLKN
Unused eDP CLK

R0950 0 5% 1/8W MF-LF 805 — =PPVIN_SW_TBTBST — =PP15V_TBT_REG
TBTBST:N

T29 / GMUX JTAG Signals

JTAG_GMUX_TCK
JTAG_ISP_TCK — JTAG_TBT_TCK
JTAG_ISP_TDI — JTAG_TBT_TDI
JTAG_ISP_TDO — JTAG_TBT_TDO
TBT_LSOE<3> — T29_LSEO_LSOE3 — TBT_LSEO<3>
TBT_LSOE<2> — T29_LSEO_LSOE2 — TBT_LSEO<2>

GMUX ALIASES

GMUX_INT — DPMUX_UC_IRQ
PM_ALL_GPU_PGOOD — ALL_EG_PGOOD
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG
EG_RESET_L — GPU_RESET_L
LVDS_IG_BKL_ON — IG_BKLT_EN
LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN
PPVOUT_S0_LCDBKLT — PPVOUT_SW_LCDBKLT

PEX_CLKREQ_L — EG_CLKREQ_IN_L
PEG_CLKREQ_L — EG_CLKREQ_OUT_L
PM_ENET_EN — =P1V2ENET_EN

Unused eDP signals

DP_INT_IG_ML_P<3..0> — NC_DP_INT_IG_MLP<3..0>
DP_INT_IG_ML_N<3..0> — NC_DP_INT_IG_MLN<3..0>
DP_INT_IG_AUX_P — NC_DP_INT_IG_AUXP
DP_INT_IG_AUX_N — NC_DP_INT_IG_AUXN
DP_INT_IG_HPD — NC_DP_INT_IG_HPD

FW_PLUG_DET_L — FW_PME_L
FW643_WAKE_L — =FW_PME_L
TP_SMC_EXCARD_PWR_EN — SMC_EXCARD_PWR_EN

PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_CP

PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARDP

TP_PEG_B_CLKRQ_L_GPIO56 — NC_PEG_B_CLKRQ_L_GPIO56
TP_PCIECLKRQ4_L_GPIO26 — NC_PCIECLKRQ4_L_GPIO26

TP_ISSP_SCLK_P1_1 — ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — ISSP_SDATA_P1_0

TP_GMUX_PT20A
TP_GMUX_PT20B
TP_GMUX_PT32A
TP_GMUX_PT32B
=PP1V05_S0M_PCH_VCC_LAN

TP_PCH_CLKOUT_DPN — NC_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP — NC_PCH_CLKOUT_DPP
TP_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3

NC_FSB_CLK133M_PCHP — FSB_CLK133M_PCH_P
NC_FSB_CLK133M_PCHN — FSB_CLK133M_PCH_N
NC_LT_GAIN_TP — LT_GAIN_TP
NC_RT_GAIN_TP — RT_GAIN_TP
NC_SW_GAIN_TP — SW_GAIN_TP

LCD_BKLT_EN — R0901 4.7K 5% 1/16W MF-LF 402

XW0901 SM — =PP5V_S0_AUDIO_XW — PP5V_S0_AUDIO — =PP5V_S0_AUDIO
XW0902 SM — PP5V_S0_AUDIO_AMP_L (MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.30MM VOLTAGE=5V)
XW0903 SM — PP5V_S0_AUDIO_AMP_R (MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.30MM VOLTAGE=5V)

USB Signals

NC_USB_EXTD_EHCIN — USB_EXTD_EHCI_N
NC_USB_EXTD_EHCIP — USB_EXTD_EHCI_P
NC_USB3_EXTC_RXN — USB3_EXTC_RX_N
NC_USB3_EXTC_RXP — USB3_EXTC_RX_P
NC_USB3_EXTC_TXN — USB3_EXTC_TX_N
NC_USB3_EXTC_TXP — USB3_EXTC_TX_P

Unused PEG signals

NC_PEG_D2RP<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2RN<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_CP<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_CN<15..12> — =PEG_R2D_C_N<15..12>

T29 Signals Through PEG

PCIE_TBT_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

GPU signals

PEG_D2R_P<7..0> — =PEG_D2R_P<7..0>
PEG_D2R_N<7..0> — =PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0> — =PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0> — =PEG_R2D_C_N<7..0>

Unused T29 Ports

TBT_D2R_P<3..2> — NC_T29_D2RP<3..2>
TBT_D2R_N<3..2> — NC_T29_D2RN<3..2>
TBT_R2D_C_P<3..2> — NC_T29_R2D_CP<3..2>
TBT_R2D_C_N<3..2> — NC_T29_R2D_CN<3..2>

CPU signals

MEMVTT_EN — =DDRVTT_EN

DP_EG_AUXCH_N — DP_EG_AUX_CH_N
DP_EG_AUXCH_P — DP_EG_AUX_CH_P
NC_DPB_EG_AUX_CHN — DPB_EG_AUX_CH_N
NC_DPB_EG_AUX_CHP — DPB_EG_AUX_CH_P
NC_DPB_EG_DDC_CLK — DPB_EG_DDC_CLK
NC_DPB_EG_DDC_DATA — DPB_EG_DDC_DATA
NC_DPB_EG_MLN<3..0> — DPB_EG_ML_N<3..0>
NC_DPB_EG_MLP<3..0> — DPB_EG_ML_P<3..0>

R0926 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS1P — C0906 0.01UF 10% 10V XSR 201
R0927 51 5% 1/20W MF 201 — T29_A_BIAS_R — TBT_A_BIAS1N — C0907 0.01UF 10% 10V XSR 201

PLACE_NEAR=C9361.1:2 mm
R9363 51 5% 1/20W MF 201 — DP_A_BIAS2
DP_A_BIAS — =DP_A_BIAS
R9362 51 5% 1/20W MF 201 — DP_A_BIAS0
PLACE_NEAR=C9361.1:2 mm
C0905 0.01UF 10% 10V XSR 201
C0908 0.01UF 10% 10V XSR 201
GND (MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.095 mm VOLTAGE=0V)

NC_DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0>
NC_DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0>
DP_IG_AUX_CH_P — DPA_IG_AUX_CH_P
DP_IG_AUX_CH_N — DPA_IG_AUX_CH_N
DP_IG_DDC_CLK — DPA_IG_DDC_CLK
DP_IG_DDC_DATA — DPA_IG_DDC_DATA
DP_IG_HPD — DPA_IG_HPD

Digital Ground

USB Signals

USB_BT_N — USBHUB_DN1_N
USB_BT_P — USBHUB_DN1_P
USB_TPAD_N — USBHUB_DN3_N
USB_TPAD_P — USBHUB_DN3_P
USB_IR_N — USBHUB_DN2_N
USB_IR_P — USBHUB_DN2_P
USB_SMC_N — USBHUB_DN4_N
USB_SMC_P — USBHUB_DN4_P

ADC_CH6 — ADC_CH6
ADC_CH7 — ADC_CH7

TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N
TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM
GPU_XTALOUT — GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3>
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3>
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3>

NC_USB_EXTCN — USB_EXTC_N
NC_USB_EXTCP — USB_EXTC_P

NC_USB3_EXTD_RXN — USB3_EXTD_RX_N
NC_USB3_EXTD_RXP — USB3_EXTD_RX_P
NC_USB3_EXTD_TXN — USB3_EXTD_TX_N
NC_USB3_EXTD_TXP — USB3_EXTD_TX_P

TALL POGO PINS for BT NF

SH0939 POGO-2.00D-3.5H-K86-K87
SH0941 POGO-2.00D-3.5H-K86-K87
SH0940 POGO-2.00D-3.5H-K86-K87
SH0942 POGO-2.00D-3.5H-K86-K87

SYNC_MASTER=K18_MLB — SYNC_DATE=04/27/2010
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10K,0402,SMD,LF	R1031		EDP:NO

```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION   0 = LANES REVERSED
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PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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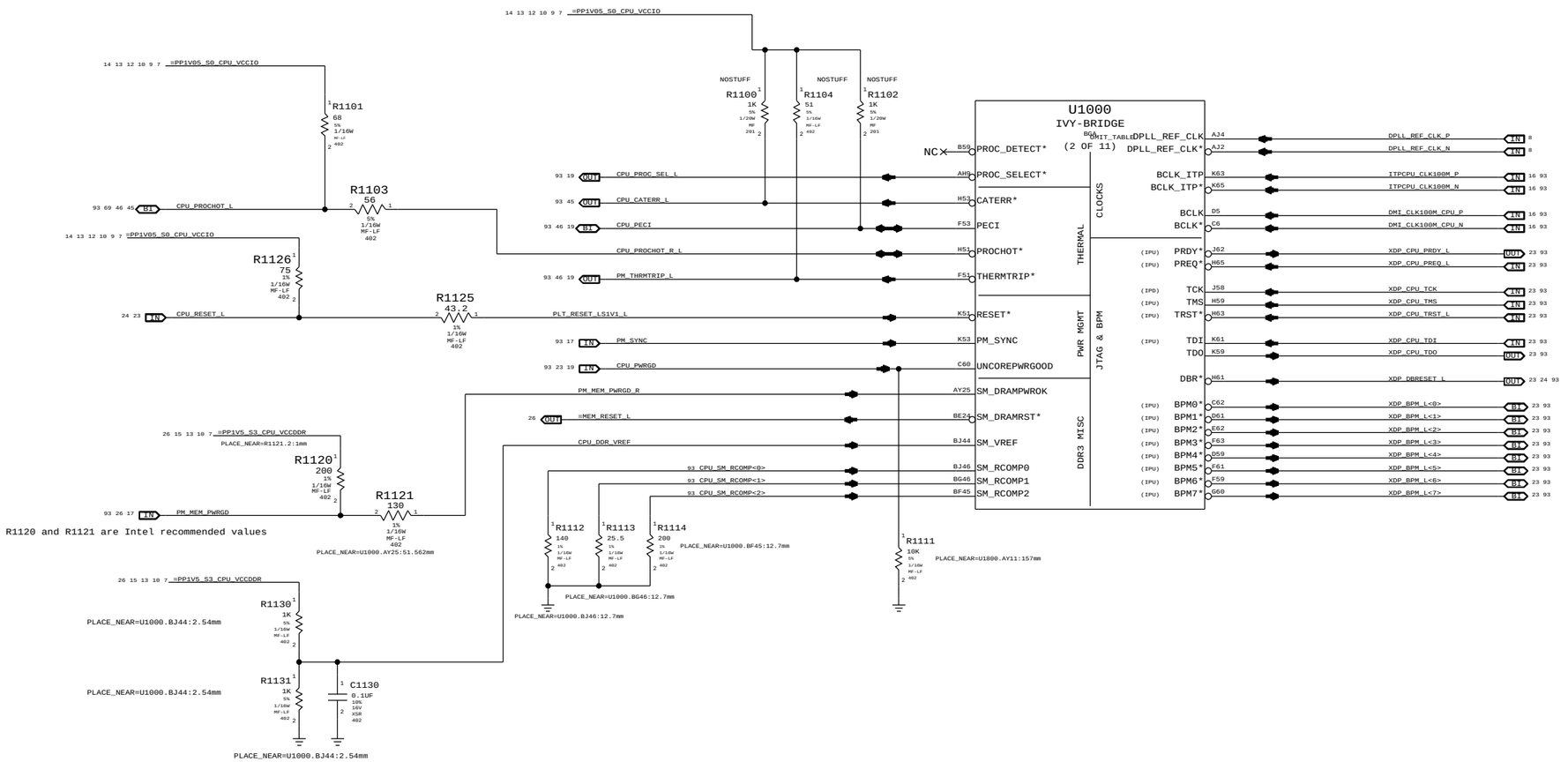

PAGE TITLE	CPU CLOCK/MISC/JTAG
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
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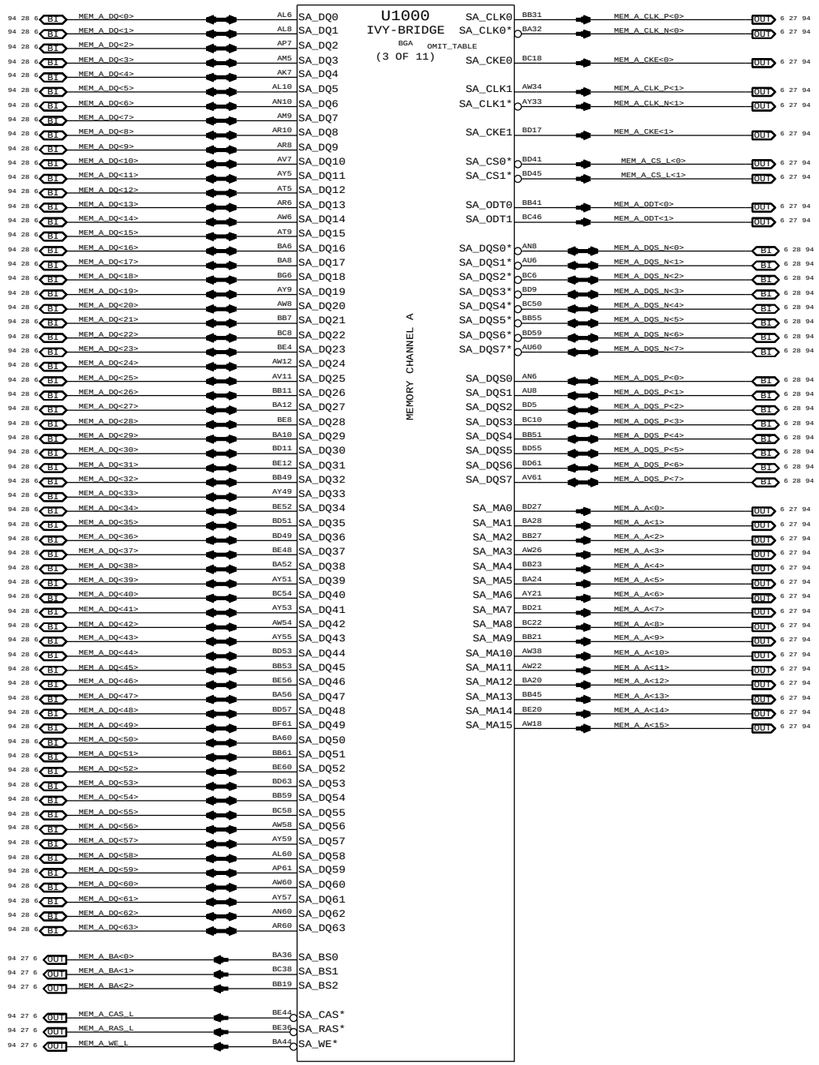

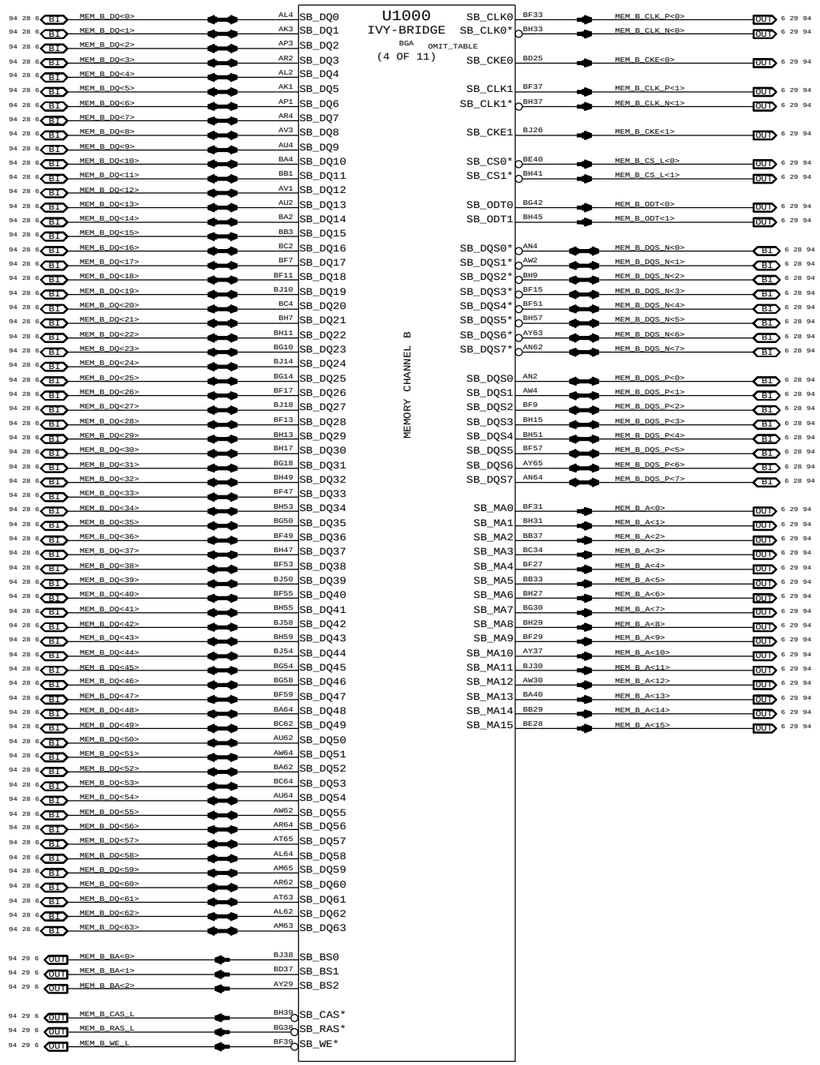

SYNC_DATE=06/15/2016

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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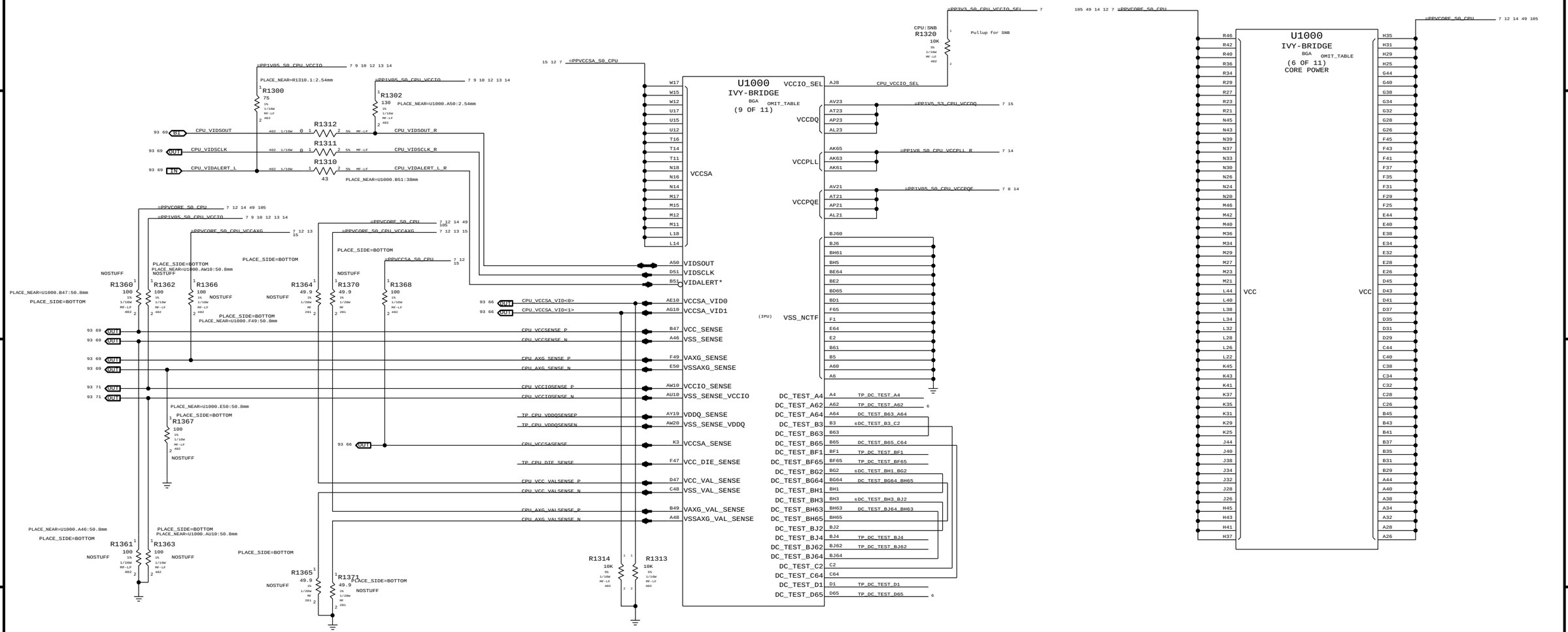

NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2016

PAGE TITLE: CPU POWER

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
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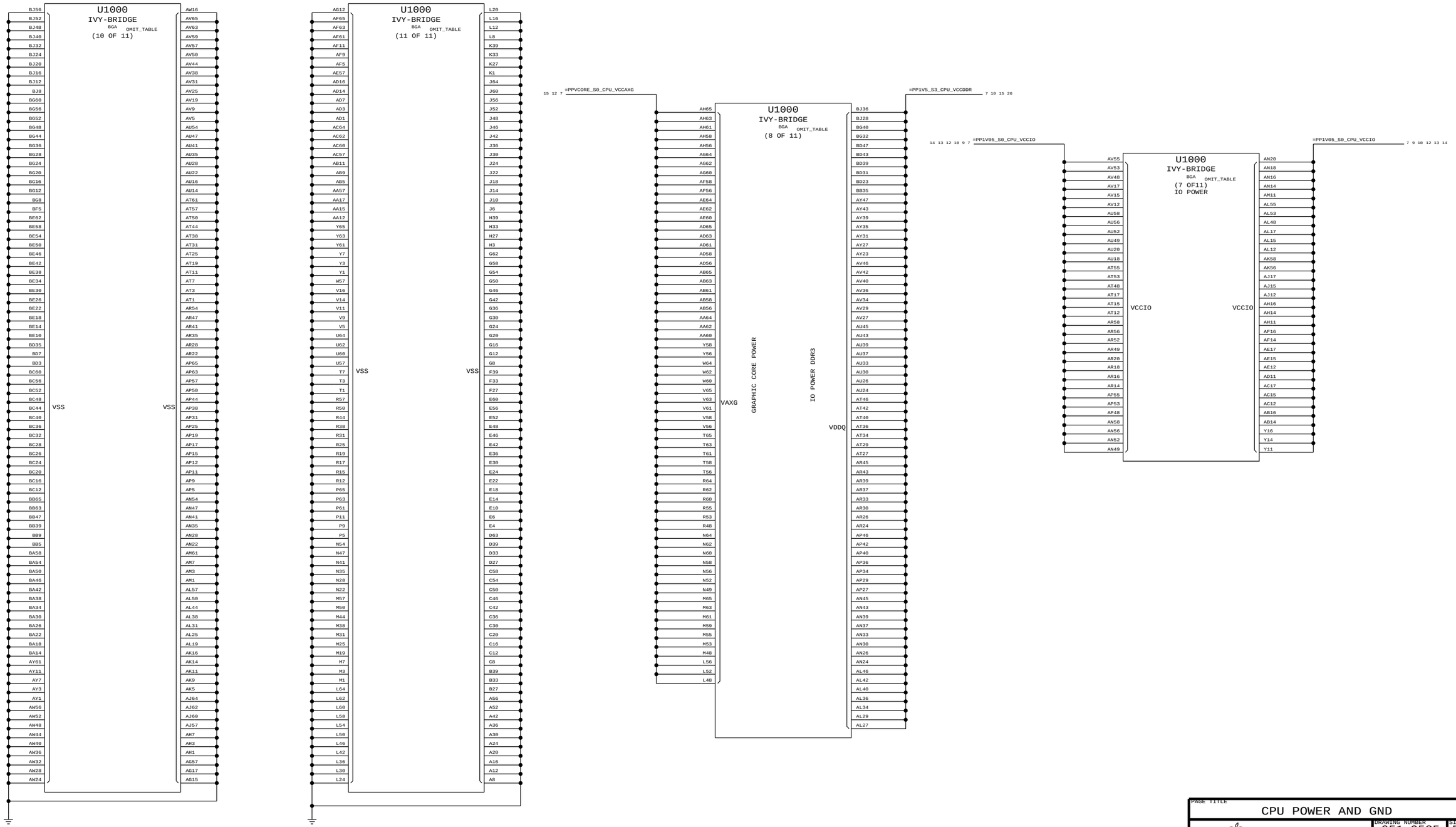

PAGE TITLE
CPU POWER AND GND

Apple Inc.

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 8x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

105 49 12 7 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):

Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):

Place near U1000 on bottom side

CRITICAL C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1624-C16D5):

Place near inductors on bottom side. Decoupling on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R-CERM1 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1640-C1645):

Place near inductors on bottom side.

NOSTUFF C1640
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CRITICAL C1641 C1642 C1643 C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):

13 12 10 9 7 =PP1V05_S0_CPU_VCCIO

Place on bottom side of U1000

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

CRITICAL C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL C1682
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603

=PP1V05_S0_CPU_VCCPQE 7 8 12

C1684
1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

7 =PP1V8_S0_CPU_VCCPLL

R1600
0
5% 1/10W MF-LF 402

=PP1V8_S0_CPU_VCCPLL_R 7 12

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1685 C1686
1UF 10% 10V X5R 402

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2016

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 8x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

13 12 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):

CRITICAL C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
CRITICAL C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
NOSTUFF CRITICAL C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

26 13 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603
=PP1V5_S3_CPU_VCCDQ 7 12
C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 3x 10uF 0603, 3x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

12 7 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2016

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

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OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(1 OF 10)

RTC
LPC
IHDA
SATA
JTAG
SPI

SYSCLK_CLK32K_RTC
NCX
RTCX1
RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTCRST*
SRTCRST*
INTRUDER*
INTVRMEN

LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
(IPU)
FWH4/LFRAME*
LPC_FRAME_R_L
(IPU) LDRQ0*
LDRQ1*/GPIO23 (IPU)
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
SERIRQ
LPC_SERIRQ
=PP3V3_S0_PCH
R1820 10K 5% 1/20W MF 201

HDA_BIT_CLK_R
HDA_SYNC_R
VSel strap not functional (VCCVRM = 1.8V)
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_TBT_TMS
ENET_MEDIA_SENSE_RDIV
HDA_BCLK
HDA_SYNC (IPD-BOOT)
SPKR (IPD-PLTRST#)
HDA_RST*
HDA_SDIN0 (IPD)
HDA_SDIN1 (IPD)
HDA_SDIN2 (IPD)
HDA_SDIN3 (IPD)
HDA_SDO (IPD-BOOT)
HDA_DOCK_EN*/GPIO33
HDA_DOCK_RST*/GPIO13

SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
SATAICOMPO
SATAICOMPI
PCH_SATAICOMPI
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.Y11:2.54mm
R1830 37.4 1% 1/20W MF 201
=PP1V05_S0_PCH
R1831 49.9 1% 1/20W MF 201
PLACE_NEAR=U1800.AB12:2.54mm
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AH1:2.54mm
R1832 750 5% 1/20W MF 201
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
SATA1GP/GPIO19 (IPU)
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN

=PPVRTC_G3_PCH
R1800 330K 5% 1/20W MF 201
R1801 1M 5% 1/20W MF 201
R1802 20K 5% 1/20W MF 201
R1803 20K 5% 1/20W MF 201
C1802 1UF 10% 10V X5R 402
C1803 1UF 10% 10V X5R 402

R1860 33 5% 1/20W MF 201
R1861 33 5% 1/20W MF 201
R1862 33 5% 1/20W MF 201
R1863 33 5% 1/20W MF 201
R1864 33 5% 1/20W MF 201
R1810 33 5% 1/20W MF 201
R1811 33 5% 1/20W MF 201
R1812 33 5% 1/20W MF 201
R1813 33 5% 1/20W MF 201
PLACE_NEAR=U1800.N34:1.27mm
PLACE_NEAR=U1800.L34:1.27mm
PLACE_NEAR=U1800.K34:1.27mm
PLACE_NEAR=U1800.A36:1.27mm

=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
=PP3V3_T29_PCH_GPIO
R1876 10K
R1877 4.7K
R1878 10K
R1834 10K
R1833 10K
R1842 10K
R1869 10K
R1844 10K
R1845 10K
R1847 10K
R1814 10K
R1815 10K
R1843 10K
R1846 10K
R1848 10K
R1853 10K
R1854 10K
R1855 10K
R1879 10K
GPU:1P
R1880 10K
GPU:2P
PEGCLKRQB_L_GPIO56

NO STUFF
R1840 0 5% 1/20W MF 201
R1841 0 5% 1/20W MF 201
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(2 OF 10)

SMBUS
PCI-E*
C-LINK
CLOCKS
FLEX CLOCKS

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
PERN5
PERP5
PETN5
PETP5
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
PERN6
PERP6
PETN6
PETP6
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
PERN7
PERP7
PETN7
PETP7
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PERN8
PERP8
PETN8
PETP8

PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
PCIECLKRQ0_L_GPIO73
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L_GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
Controlled by PCIECLKRQ5#

SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
PCH_GPIO11
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
PEGCLKRQA_L_GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
CLKOUT_DMI_N
CLKOUT_DMI_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CLKOUT_DP_N
CLKOUT_DP_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
CLKIN_DMI_N
CLKIN_DMI_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
CLKIN_GND1_N
CLKIN_GND1_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
CLKIN_DOT_96N
CLKIN_DOT_96P
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
CLKIN_SATA_N
CLKIN_SATA_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
REFCLK14IN
PCH_CLK14P3M_REFCLK
CLKIN_PCILOOPBACK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
XTAL25_IN
XTAL25_OUT
SYSCLK_CLK25M_SB_R
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9 1% 1/20W MF 201
PLACE_NEAR=U1800.Y47:2.54mm
XCLK_RCOMP
PCH_XCLK_RCOMP
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3

SYSCLK_CLK25M_SB
R1872 604 1% 1/16W MF-LF 402
SYSCLK_CLK25M_SB_R
1.8V -> 1.1V
R1873 1K 1% 1/20W MF 201

Unused clock terminations for FCIM Mode
PCH_CLK96M_DOT_P R1891 10K
PCH_CLK96M_DOT_N R1892 10K
PCH_CLK100M_SATA_P R1893 10K
PCH_CLK100M_SATA_N R1894 10K
PCIE_CLK100M_PCH_P R1895 10K
PCIE_CLK100M_PCH_N R1896 10K
PCH_CLK14P3M_REFCLK R1897 10K
PCH_CLKIN_GNDP1 R1870 10K
PCH_CLKIN_GNDN1 R1871 10K

SYNC_MASTER=J31_ANNE SYNC_DATE=06/02/2011
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
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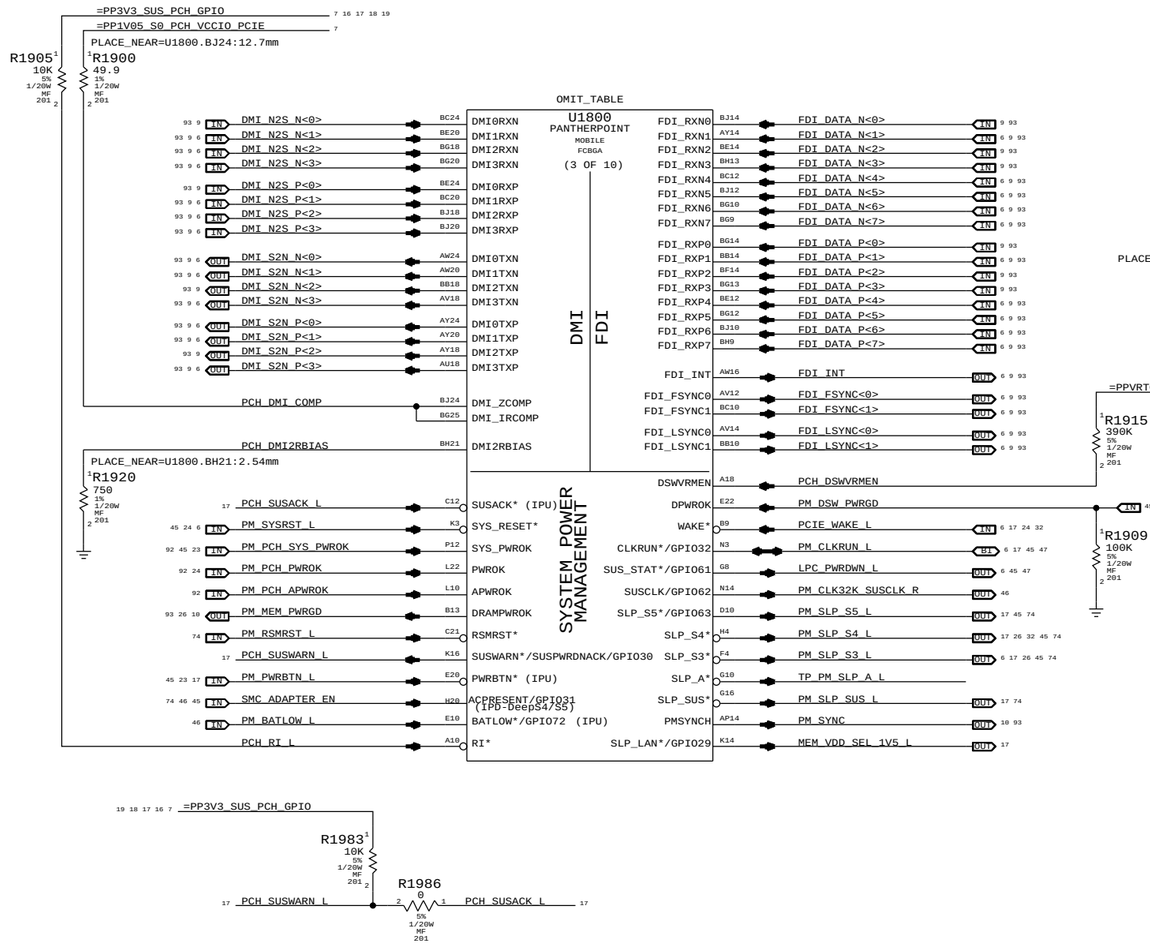
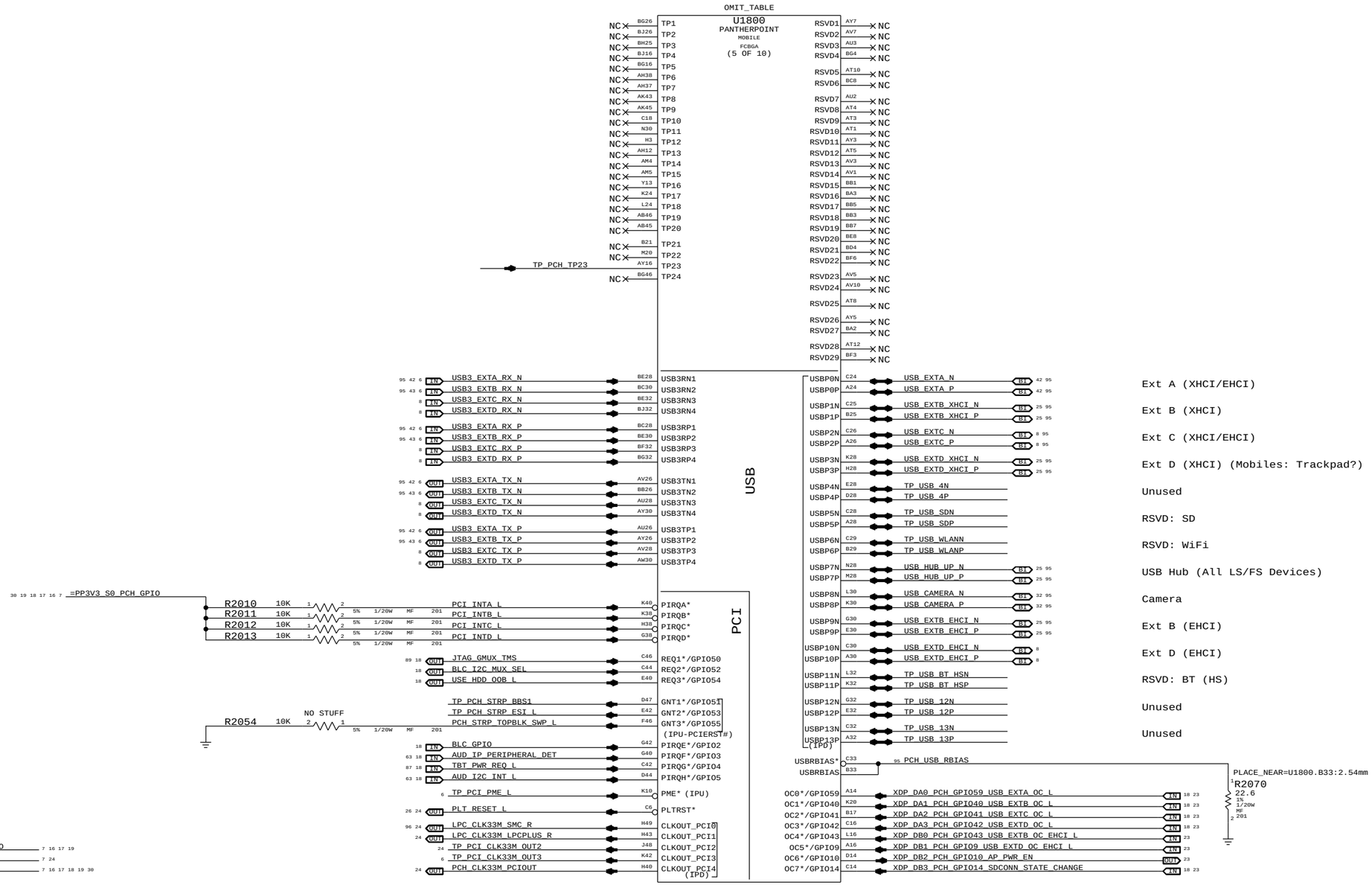


SYNC_MASTER=J5_MLB	SYNC_DATE=05/26/2011
PAGE TITLE	PCH DMI/FDI/PM/Graphics
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D · REVISION 3.0.0 · BRANCH · PAGE 19 OF 132 · SHEET 17 OF 105



SYNC_MASTER=J31_ANNE SYNC_DATE=06/02/2011

PAGE TITLE

PCH PCI/USB/TP/RSVD

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

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BRANCH

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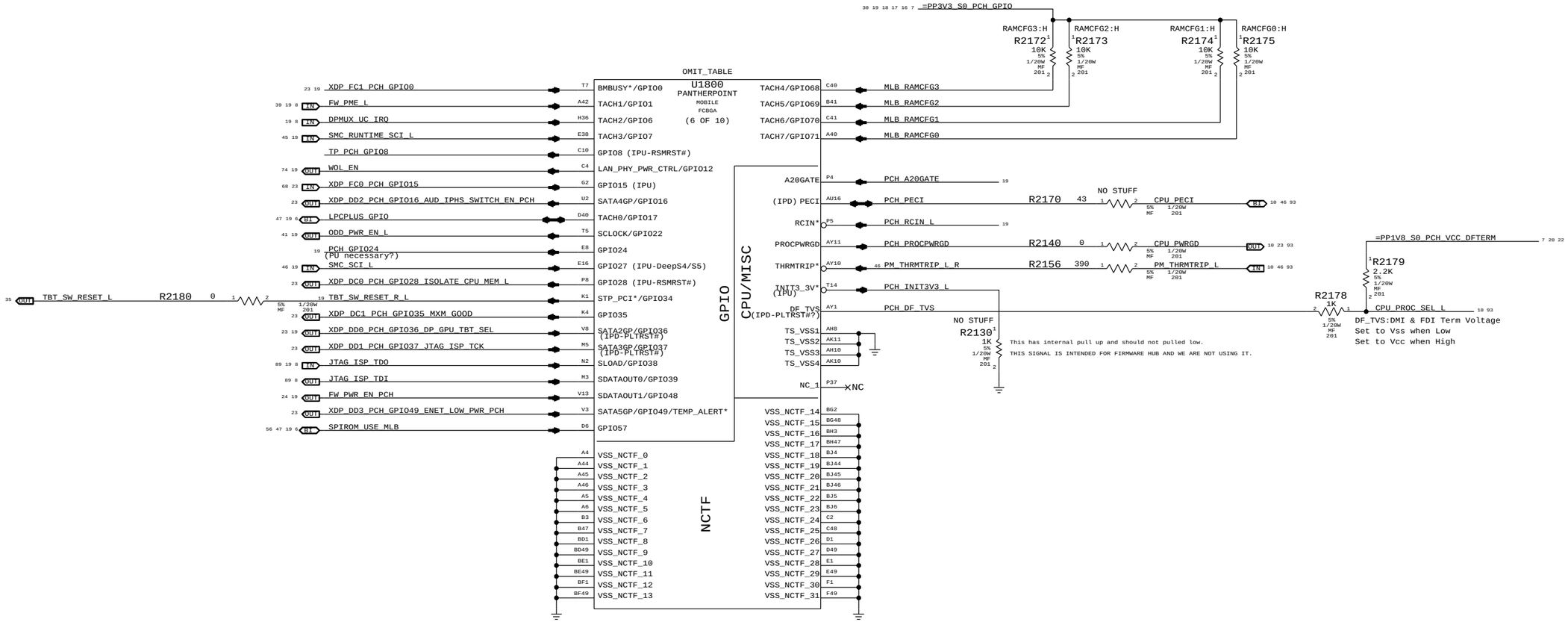
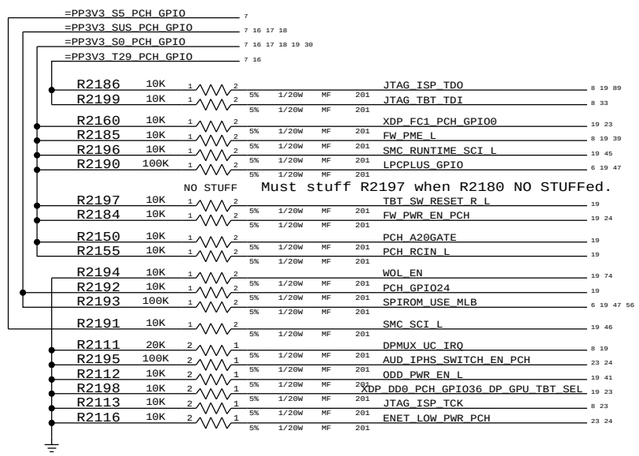
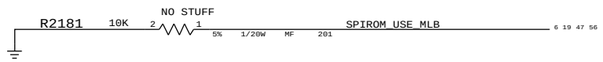
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.







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PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
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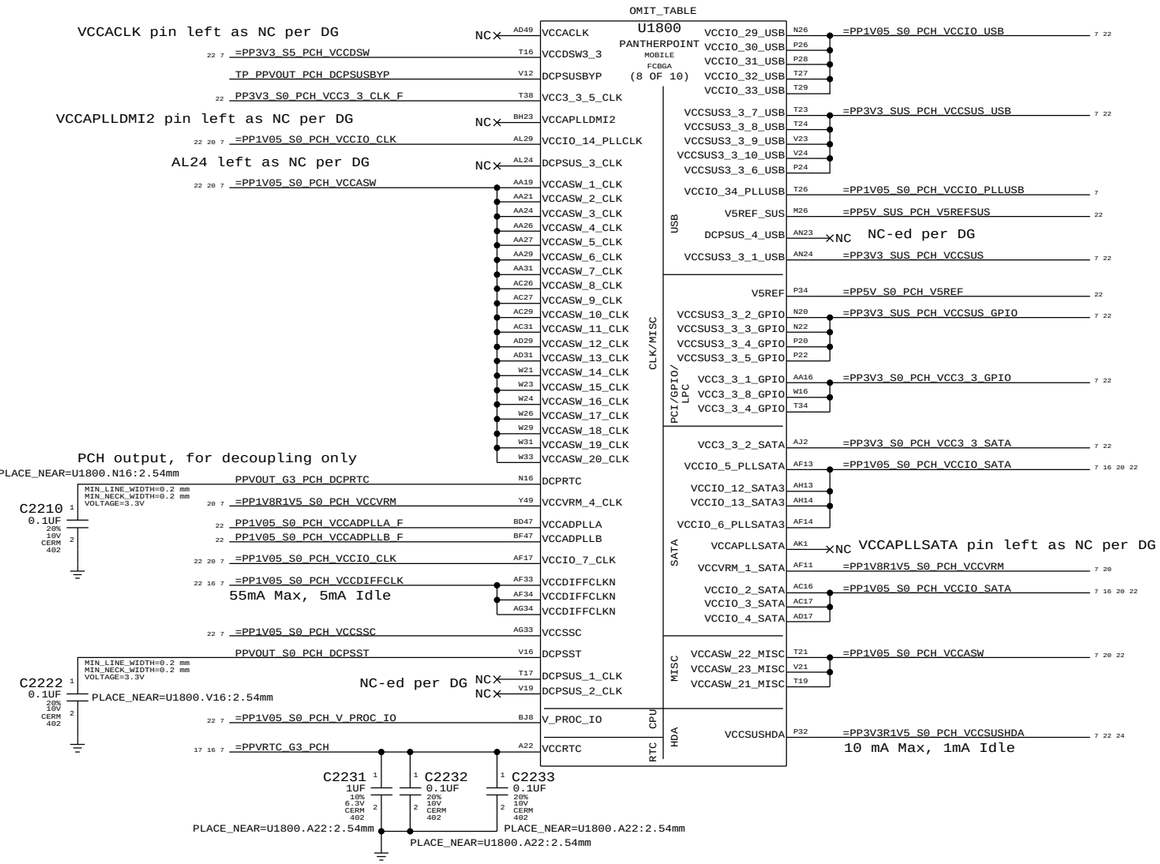

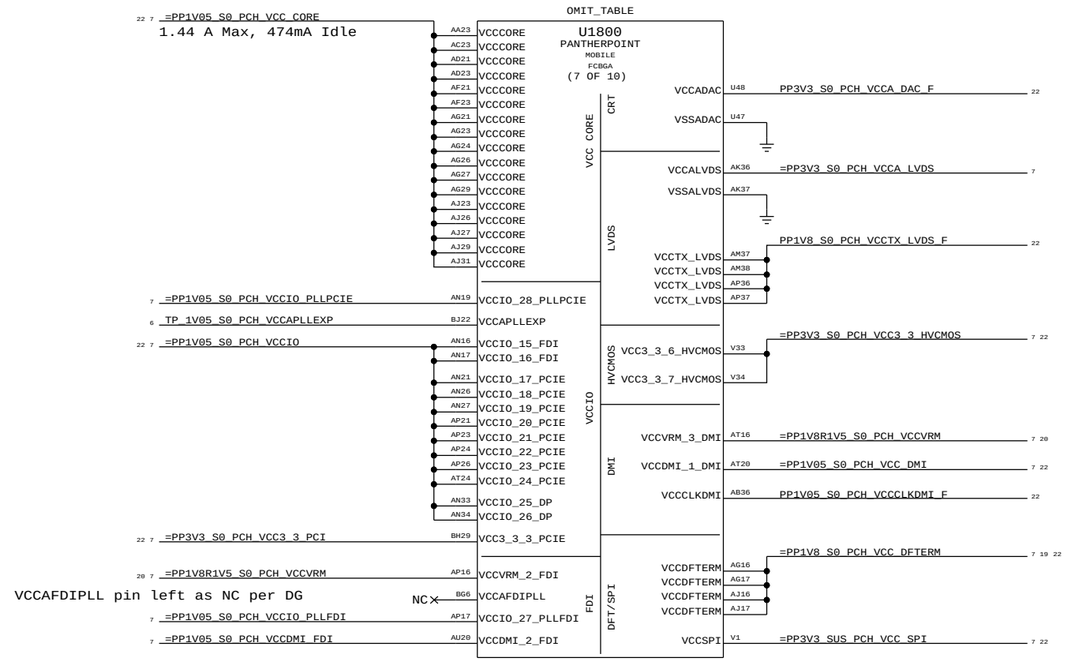

SYNC_MASTER=J5_MLB	SYNC_DATE=03/21/2011
PAGE TITLE	PCH POWER
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
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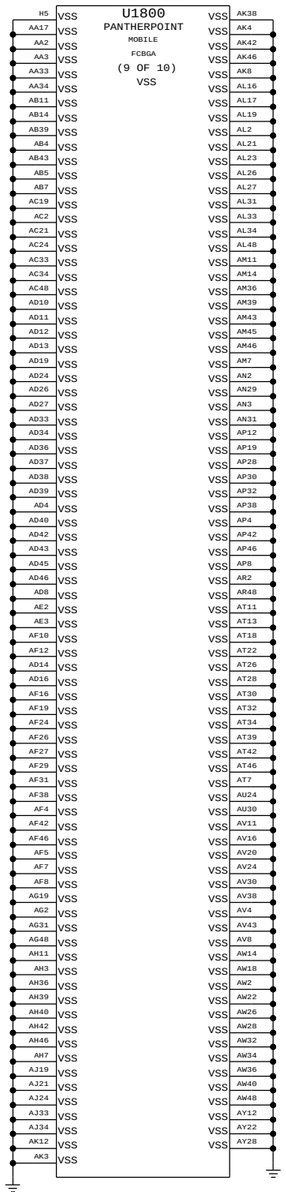

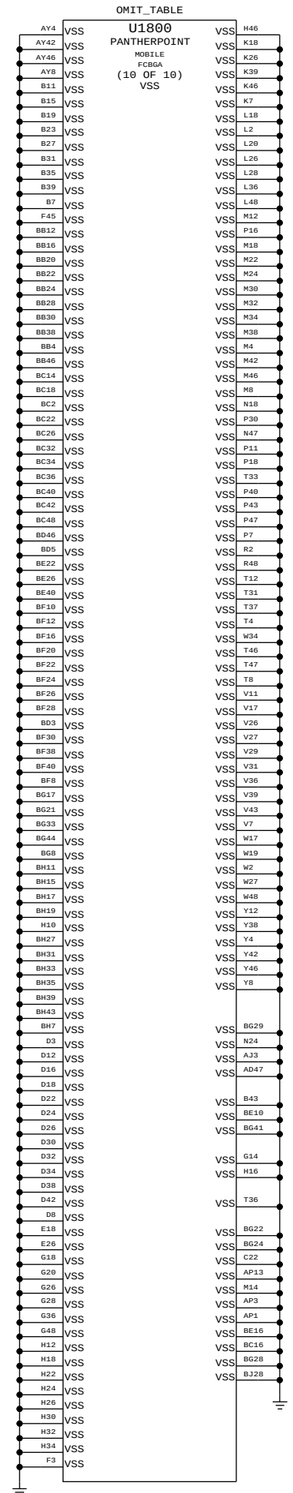

SYNC_MASTER=J5_MLB SYNC_DATE=03/21/2011

PAGE TITLE

PCH GROUNDS

Apple Inc.

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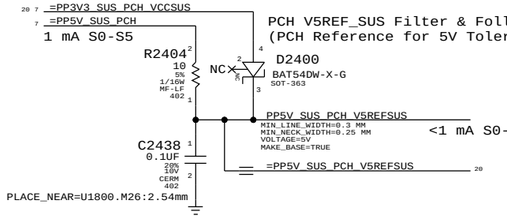

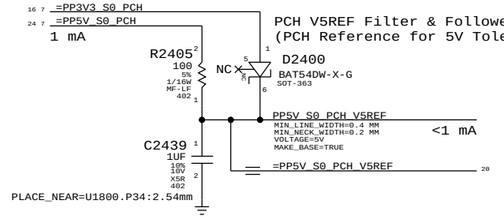

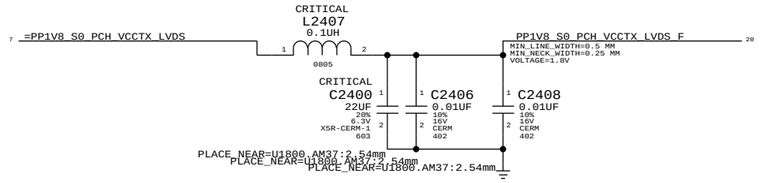

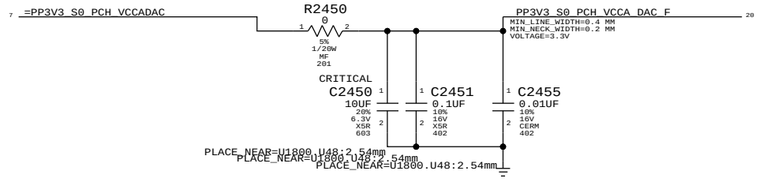

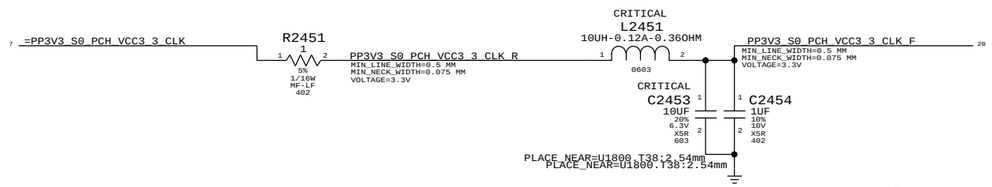

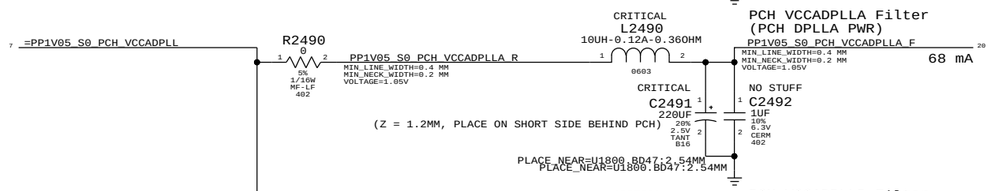

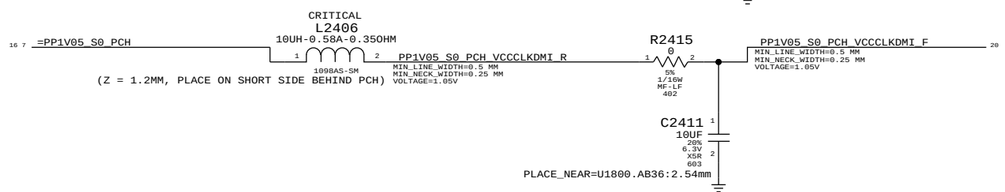

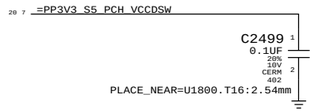

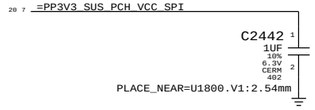

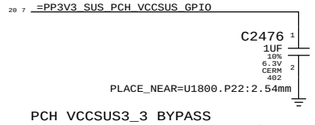

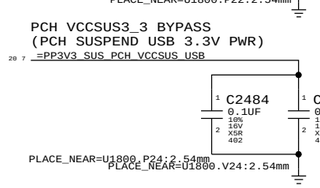

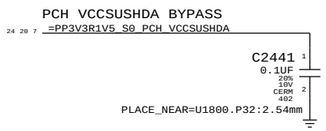

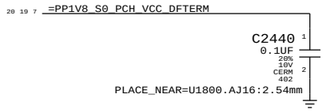

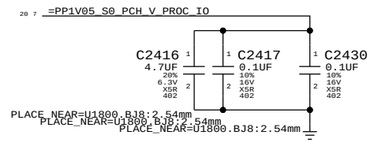

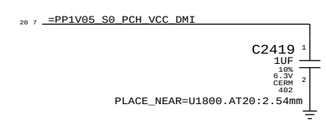

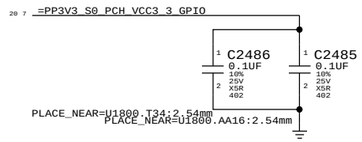

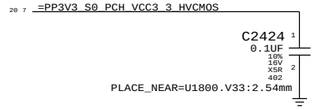

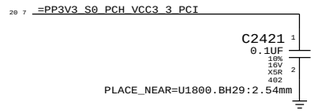

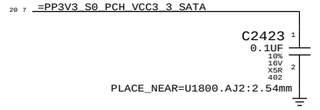

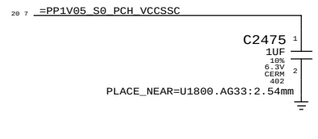

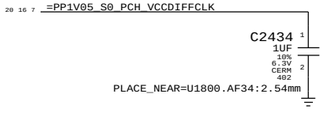

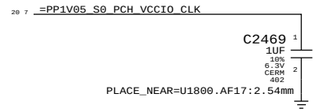

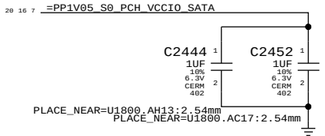

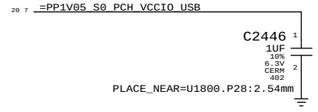

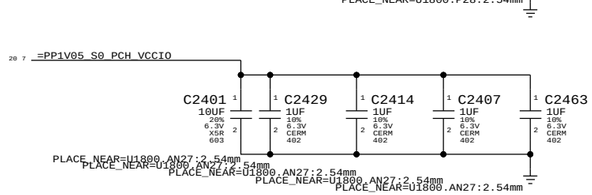

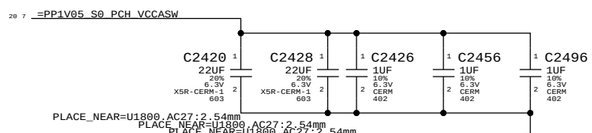

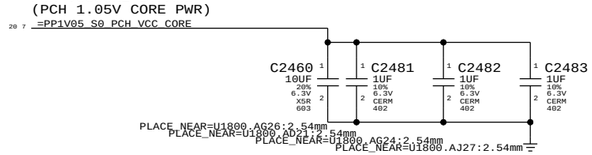

PCH VCCIO BYPASS

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

SYNC_MASTER=J5_MLB	SYNC_DATE=05/26/2011
PAGE TITLE	PCH DECOUPLING
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CPU Micro2-XDP

=PPVCCIO_S0_XDP (23 7)

=PP3V3_S0_XDP (7) — NO STUFF — R2540[1] 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN_CPU
J2500
DF40RC-60DP-0.4V
M-ST-SM

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L (93 10 BI)	OBSEN_A0	OBSEN_C0	CPU_CFG<16> (IN 9 93)	XDP_CPU_TDO (93 23 10)	R2510 51
XDP_CPU_PRDY_L (93 10 IN)	OBSEN_A1	OBSEN_C1	CPU_CFG<17> (IN 9 93)	XDP_CPU_TDI (93 23 10)	R2511 51
XDP_BPM_L<0> (93 10 IN)	OBSDATA_A0	OBSDATA_C0	CPU_CFG<0> (IN 9 23 93)	XDP_CPU_TMS (93 23 10)	R2512 51
XDP_BPM_L<1> (93 10 IN)	OBSDATA_A1	OBSDATA_C1	CPU_CFG<1> (IN 9 93)	XDP_CPU_TCK (93 23 10)	R2513 51
XDP_BPM_L<2> (93 10 IN)	OBSDATA_A2	OBSDATA_C2	CPU_CFG<2> (IN 9 93)	XDP_CPU_TRST_L (93 23 10)	R2514 51
XDP_BPM_L<3> (93 10 IN)	OBSDATA_A3	OBSDATA_C3	CPU_CFG<3> (IN 9 93)		
CPU_CFG<10> (93 9 IN)	OBSEN_B0	OBSEN_D0	CPU_CFG<8> (IN 9 93)		
CPU_CFG<11> (93 9 IN)	OBSEN_B1	OBSEN_D1	CPU_CFG<9> (IN 9 93)		
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<4> (IN 9 93)		
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<5> (IN 9 93)		
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<6> (IN 9 93)		
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<7> (IN 9 93)		
XDP_CPU_PWRGD (93)	PWRGD/HOOK0	ITPCLK/HOOK4	XDP_CPU_CLK100M_P (93)		
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	XDP_CPU_CLK100M_N (93)		
	VCC_OBS_AB	VCC_OBS_CD			
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6	XDP_CPURST_L		
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L (OUT 10 23 24 93)		
=SMBUS_XDP_SDA (48 23 BI)	SDA	TDO	XDP_CPU_TDO (IN 10 23 93)		
=SMBUS_XDP_SCL (48 23 IN)	SCL	TRSTn	XDP_CPU_TRST_L (OUT 10 23 93)		
XDP_CPU_TCK (93 23 10 OUT)	TCK1	TDI	XDP_CPU_TDI (OUT 10 23 93)		
	TCK0	TMS	XDP_CPU_TMS (OUT 10 23 93)		
	NC	XDP_PRESENT#			

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

R2515 0	XDP_CPU_CLK100M_P	ITPXDP_CLK100M_P	(IN 16 93)
R2516 0	XDP_CPU_CLK100M_N	ITPXDP_CLK100M_N	(IN 16 93)
R2505 1K	XDP_DBRESET_L	CPU_RESET_L	(IN 10 24)

XDP C2500 0.1uF 10% 16V X5R 402 (1–2)

998-2516

XDP C2501 0.1uF 10% 16V X5R 402 (1–2)

(R2560-R2563) XDP_CPU:BPM

XDP_BPM_L<4> (93 10 IN)	R2560 0	
XDP_BPM_L<5> (93 10 IN)	R2561 0	
XDP_BPM_L<6> (93 10 IN)	R2562 0	
XDP_BPM_L<7> (93 10 IN)	R2563 0	

(R2564-R2567) XDP_CPU:CFG

CPU_CFG<12> (93 9 IN)	R2564 0	
CPU_CFG<13> (93 9 IN)	R2565 0	
CPU_CFG<14> (93 9 IN)	R2566 0	
CPU_CFG<15> (93 9 IN)	R2567 0	

CPU_PWRGD (93 19 10 IN)	R2500 1K	XDP PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L (45 23 17 OUT)	R2502 0	XDP PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0> (93 23 9 OUT)	R2501 1K	XDP PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK (92 45 17 OUT)	R2504 330	XDP

(R2520-R2537) XDP

XDP SIGNALS

XDP_DA0_USB_EXTA_OC_L (23 OUT)	R2520 33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L (IN 18 23)
XDP_DA1_USB_EXTB_OC_L (23 OUT)	R2521 33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L (IN 18 23)
XDP_DA2_USB_EXTC_OC_L (23 OUT)	R2522 33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L (IN 18)
XDP_DA3_USB_EXTD_OC_L (23 OUT)	R2523 33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L (IN 18 23)
XDP_DB0_USB_EXTB_OC_EHCI_L (23 OUT)	R2524 33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L (IN 18 23)
XDP_DB1_USB_EXTD_OC_EHCI_L (23 OUT)	R2525 33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L (IN 18 23)
XDP_DB2_AP_PWR_EN (23 IN)	R2526 33	XDP_DB2_PCH_GPIO10_AP_PWR_EN (OUT 18 23)
XDP_DB3_SDCONN_STATE_CHANGE (23 OUT)	R2527 33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE (IN 18 23)
XDP_FC0 (23 OUT)	R2528 33	XDP_FC0_PCH_GPIO15 (IN 19 68)
XDP_FC1 (23 OUT)	R2529 33	XDP_FC1_PCH_GPIO0 (IN 19)
XDP_DC0_ISOLATE_CPU_MEM_L (23 IN)	R2530 33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L (OUT 19 23)
XDP_DC1_MXM_GOOD (23 IN)	R2531 33	XDP_DC1_PCH_GPIO35_MXM_GOOD (OUT 19)
XDP_DC2_DP_AUXCH_ISOL (23 IN)	R2532 33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (OUT 16 23)
XDP_DC3_SATARDRVR_EN (23 IN)	R2533 33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN (OUT 16 23)
XDP_DD0_DP_GPU_TBT_SEL (23 IN)	R2534 33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL (OUT 19)
XDP_DD1_JTAG_ISP_TCK (23 IN)	R2535 33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK (OUT 19 23)
XDP_DD2_AUD_IPHS_SWITCH_EN (23 IN)	R2536 33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH (OUT 19 23)
XDP_DD3_ENET_LOW_PWR (23 IN)	R2537 33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH (OUT 19 23)

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L (23 18 OUT)	R2590 0	USB_EXTA_OC_L (IN 42)
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L (23 18 OUT)	R2591 0	USB_EXTB_OC_L (IN 42)
XDP_DB2_PCH_GPIO10_AP_PWR_EN (23 18 IN)	R2596 0	AP_PWR_EN (OUT 18 32 74)
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE (23 18 OUT)	R2597 0	SDCONN_STATE_CHANGE (IN 24)
XDP_DC3_PCH_GPIO19_SATARDRVR_EN (23 16 IN)	R2573 0	SATARDRVR_EN (OUT 16 41)
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L (23 19 OUT)	R2570 0	ISOLATE_CPU_MEM_L (OUT 26)
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (23 16 IN)	R2572 0	DP_AUXCH_ISOL (OUT 16 87)

Non-XDP Signals

XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK (23 19 OUT)	R2575 0	JTAG_ISP_TCK (OUT 8 19)
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH (23 19 OUT)	R2576 0	AUD_IPHS_SWITCH_EN_PCH (OUT 19 24)
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH (23 19 OUT)	R2577 0	ENET_LOW_PWR_PCH (OUT 19 24)

PCH Micro2-XDP

=PP3V3_S5_XDP (7)

CRITICAL
XDP_CONN_PCH
J2550
DF40RC-60DP-0.4V
M-ST-SM

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

TP_XDP_PCH_OBSFN_A<0>	OBSFN_A0	OBSFN_C0	XDP_FC0 (23)	XDP_PCH_TDO (23 16)	R2550 51
TP_XDP_PCH_OBSFN_A<1>	OBSFN_A1	OBSFN_C1	XDP_FC1 (23)	XDP_PCH_TDI (23 16)	R2551 51
XDP_DA0_USB_EXTA_OC_L (23)	OBSDATA_A0	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L (23)	XDP_PCH_TMS (23 16)	R2552 51
XDP_DA1_USB_EXTB_OC_L (23)	OBSDATA_A1	OBSDATA_C1	XDP_DC1_MXM_GOOD (23)	XDP_PCH_TCK (23 16)	R2556 51
XDP_DA2_USB_EXTC_OC_L (23)	OBSDATA_A2	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL (23)		
XDP_DA3_USB_EXTD_OC_L (23)	OBSDATA_A3	OBSDATA_C3	XDP_DC3_SATARDRVR_EN (23)		
TP_XDP_PCH_OBSFN_B<0>	OBSFN_B0	OBSFN_D0	TP_XDP_PCH_OBSFN_D<0>		
TP_XDP_PCH_OBSFN_B<1>	OBSFN_B1	OBSFN_D1	TP_XDP_PCH_OBSFN_D<1>		
XDP_DB0_USB_EXTB_OC_EHCI_L (23)	OBSDATA_B0	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL (23)		
XDP_DB1_USB_EXTD_OC_EHCI_L (23)	OBSDATA_B1	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK (23)		
XDP_DB2_AP_PWR_EN (23)	OBSDATA_B2	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN (23)		
XDP_DB3_SDCONN_STATE_CHANGE (23)	OBSDATA_B3	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR (23)		
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4		
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5		
	VCC_OBS_AB	VCC_OBS_CD			
TP_XDPPCH_HOOK2 (6)	HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L (IN 24)		
TP_XDPPCH_HOOK3 (6)	HOOK3	DBR#/HOOK7	XDP_DBRESET_L (OUT 10 23 24 93)		
=SMBUS_XDP_SDA (48 23 BI)	SDA	TDO	XDP_PCH_TDO (IN 16 23)		
=SMBUS_XDP_SCL (48 23 IN)	SCL	TRSTn	TP_XDP_PCH_TRST_L		
XDP_PCH_TCK (23 16 OUT)	TCK1	TDI	XDP_PCH_TDI (OUT 16 23)		
	TCK0	TMS	XDP_PCH_TMS (OUT 16 23)		
	NC	XDP_PRESENT#			

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

1K series R on PCH Support Page

XDP C2580 0.1uF 10% 16V X5R 402 (1–2)

998-2516

XDP C2581 0.1uF 10% 16V X5R 402 (1–2)

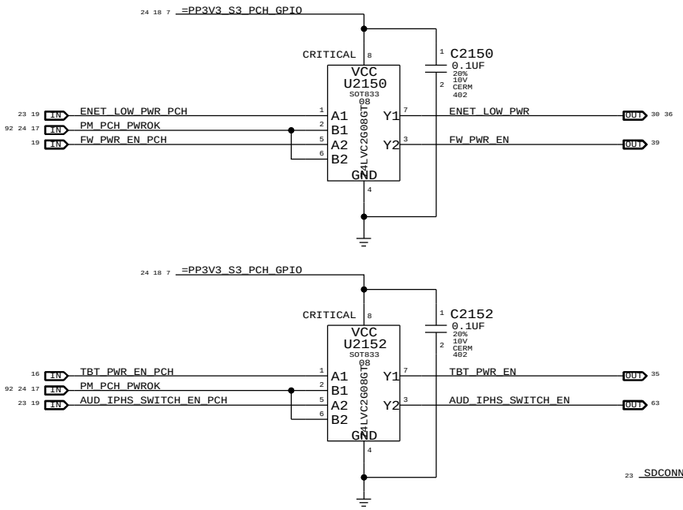
=PP1V05_SUS_PCH_JTAG (7)

ALL_SYS_PWRGD (92 89 74 45 IN)	R2584 1K	XDP PLACE_NEAR=J2550.39:2.54mm
PM_PWRBTN_L (45 23 17 OUT)	R2585 0	XDP PLACE_NEAR=U4900.P17:2.54mm

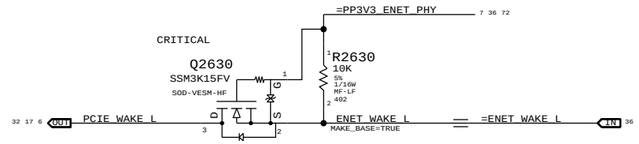
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L (23 18)	R2580 1K	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L (18 23)
XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L (23 18)	R2581 1K	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L (18 23)

SYNC_MASTER=J31_ANNE	SYNC_DATE=06/09/2011
PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D · REVISION 3.0.0 · BRANCH · PAGE 25 OF 132 · SHEET 23 OF 105

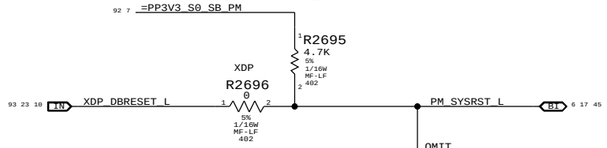
GPIO Glitch Prevention



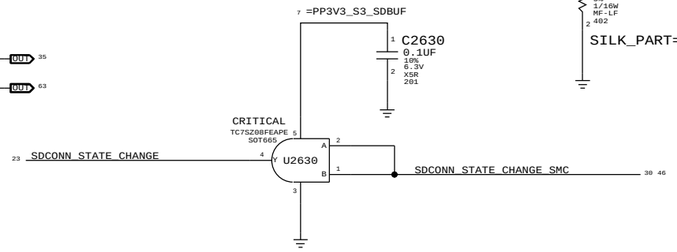
Ethernet WAKE# Isolation



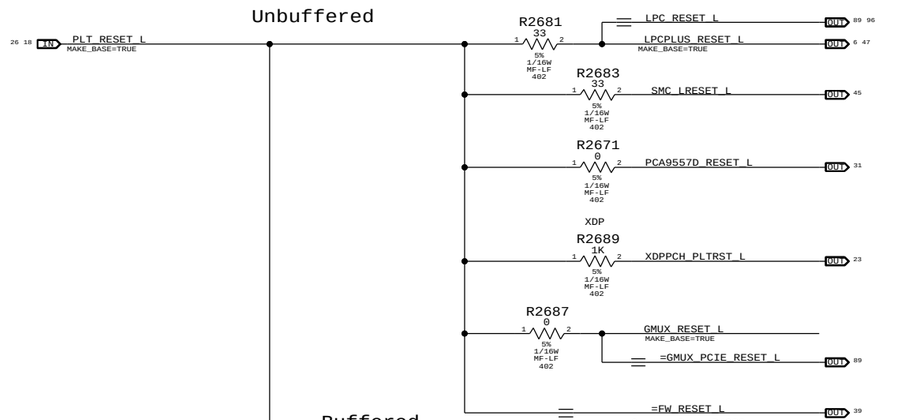
PCH Reset Button

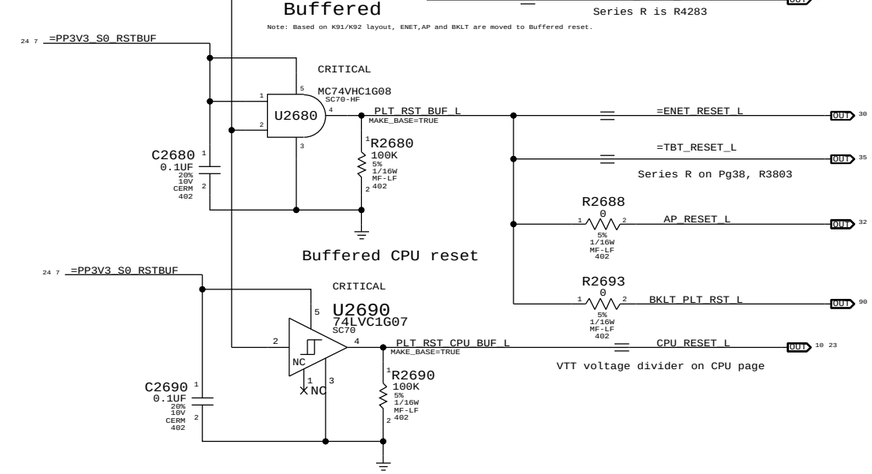


SDCONN_STATE_CHANGE

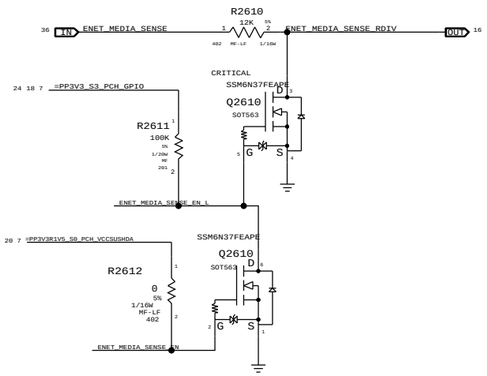


Platform Reset Connections

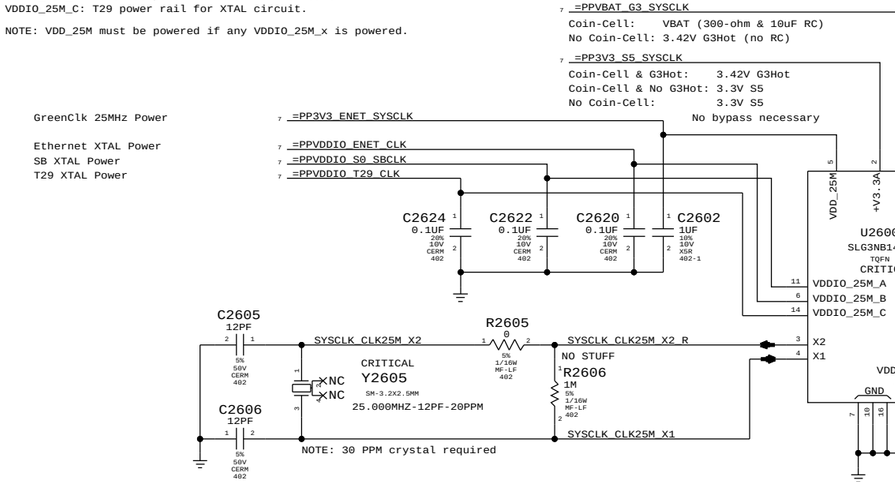




ENET_MEDIA_SENSE ISOLATION CIRCUIT



System RTC Power Source & 32kHz / 25MHz Clock Generator

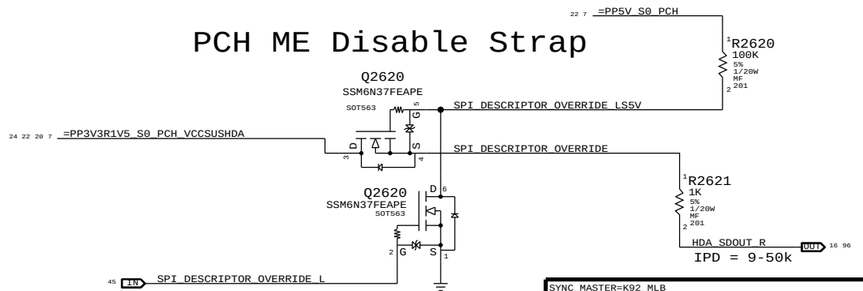


VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH ME Disable Strap



SYNC_MASTER=K92_MLB	SYNC_DATE=07/06/2010
PAGE TITLE: Chipset Support	
Apple Inc.	DRAWING NUMBER: 051-9585 SIZE: D
	REVISION: 3.0.0
	BRANCH
	PAGE: 26 OF 132
	SHEET: 24 OF 105

USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM 1 : NON_REM 0 — STRAP PIN CFG

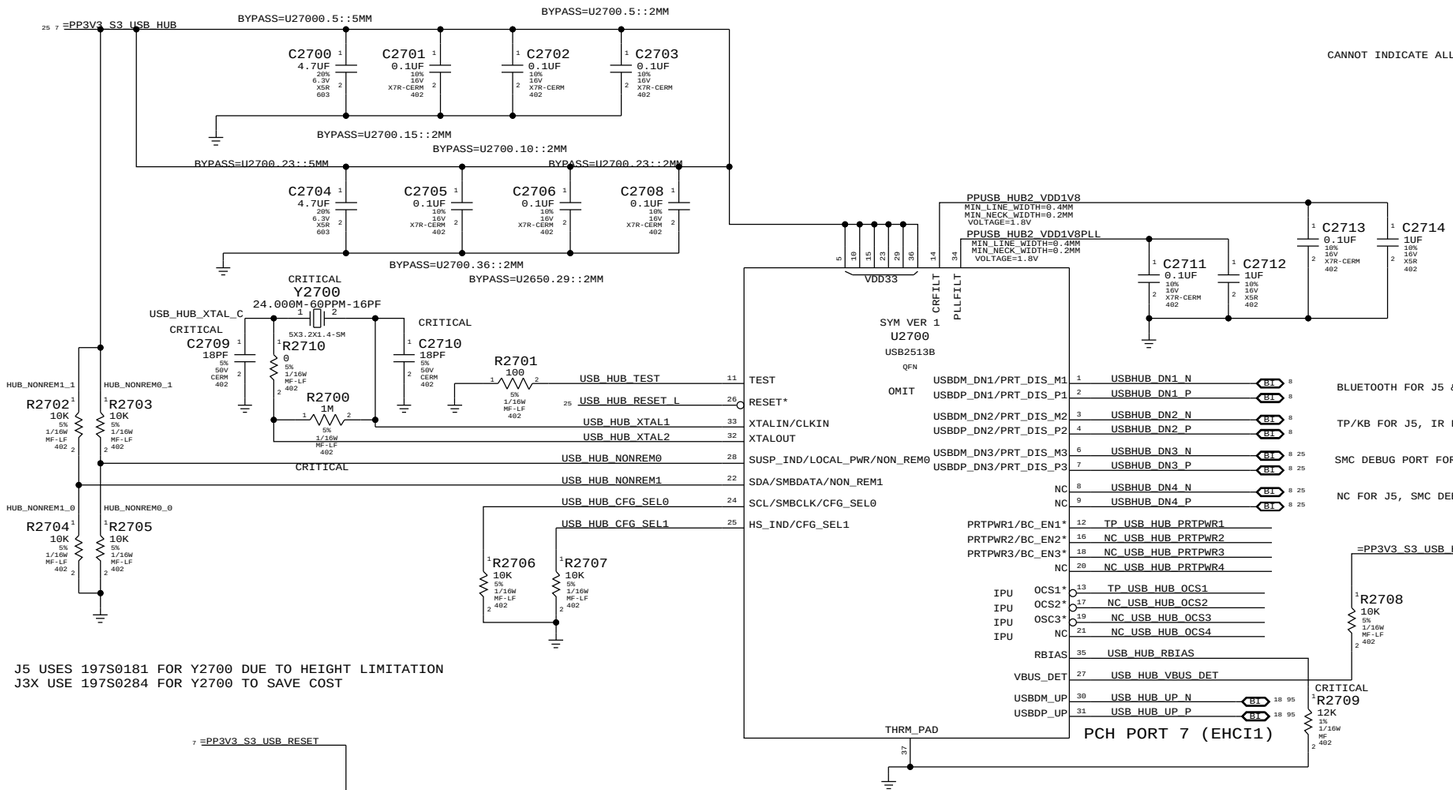
NON_REM 1	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

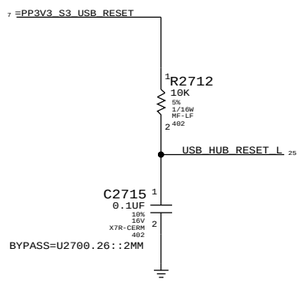
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

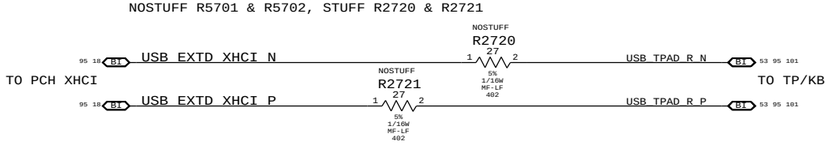
J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



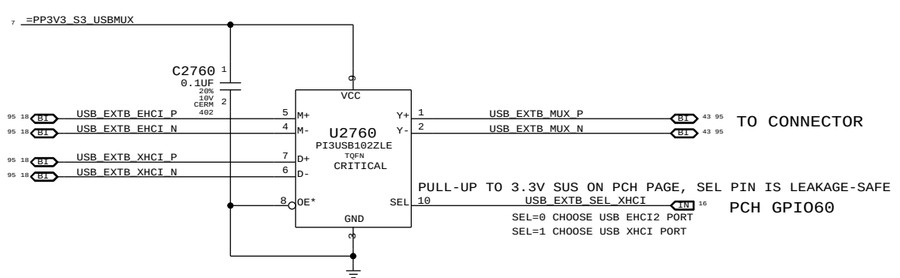
J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
J3X USE 197S0284 FOR Y2700 TO SAVE COST



TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



PCH PORT 9 (EHCI2)

PCH PORT 1 (XHCI)

SYNC_MASTER=J31_LINDA SYNC_DATE=09/16/2011

PAGE TITLE: USB HUB & MUX

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
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BRANCH:
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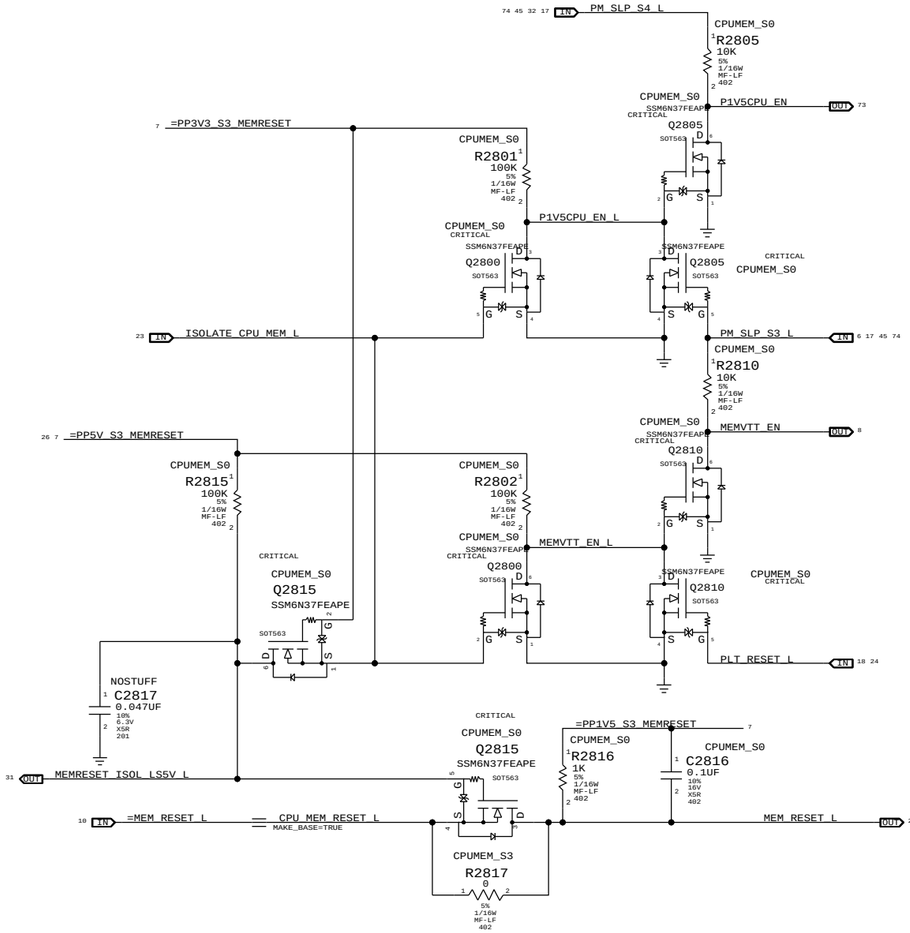
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

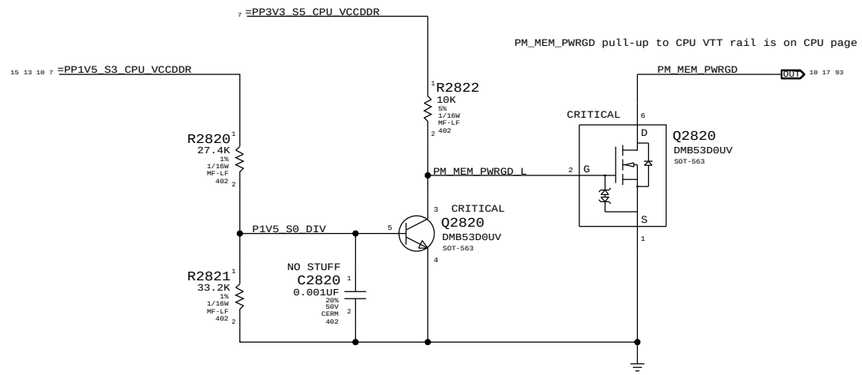


	Step	SOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

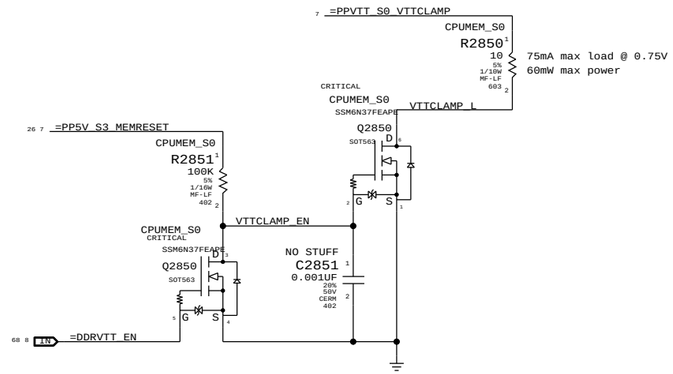
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 28 OF 132
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

7 =PP1V5_S3_MEM_A

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
PLACE_NEAR=J2900.75:2.54mm

C2910 C2911 C2912 C2913 C2914 C2915 C2916 C2917 C2918 C2919 C2920 C2921 C2922 C2923
0.1UF 20% 10V CERM 402
PLACE_NEAR=J2900.75:2.54mm

93 31 PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

OMIT_TABLE

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)
KEY

94 11 6	IN	MEM_A_CKE<0>	73	CKE0	
			75	VDD	
NC			77	NC	
94 11 6	IN	MEM_A_BA<2>	79	BA2	
			81	VDD	
94 11 6	IN	MEM_A_A<12>	83	A12/BC*	
94 11 6	IN	MEM_A_A<9>	85	A9	
			87	VDD	
94 11 6	IN	MEM_A_A<8>	89	A8	
94 11 6	IN	MEM_A_A<5>	91	A5	
			93	VDD	
94 11 6	IN	MEM_A_A<3>	95	A3	
94 11 6	IN	MEM_A_A<1>	97	A1	
			99	VDD	
94 11 6	IN	MEM_A_CLK_P<0>	101	CK0	
94 11 6	IN	MEM_A_CLK_N<0>	103	CK0*	
			105	VDD	
94 11 6	IN	MEM_A_A<10>	107	A10/AP	
94 11 6	IN	MEM_A_BA<0>	109	BA0	
			111	VDD	
94 11 6	IN	MEM_A_WE_L	113	WE*	
94 11 6	IN	MEM_A_CAS_L	115	CAS*	
			117	VDD	
94 11 6	IN	MEM_A_A<13>	119	A13	
94 11 6	IN	MEM_A_CS_L<1>	121	S1*	
			123	VDD	
NC			125	TEST	
			127	VSS	
28	BI	=MEM_A_DQ<32>	129	DQ32	
28	BI	=MEM_A_DQ<33>	131	DQ33	
			133	VSS	
28	BI	=MEM_A_DQS_N<4>	135	DQS4*	
28	BI	=MEM_A_DQS_P<4>	137	DQS4	
			139	VSS	
28	BI	=MEM_A_DQ<34>	141	DQ34	
28	BI	=MEM_A_DQ<35>	143	DQ35	
			145	VSS	
28	BI	=MEM_A_DQ<40>	147	DQ40	
28	BI	=MEM_A_DQ<41>	149	DQ41	
			151	VSS	
			153	DM5	
			155	VSS	
28	BI	=MEM_A_DQ<42>	157	DQ42	
28	BI	=MEM_A_DQ<43>	159	DQ43	
			161	VSS	
28	BI	=MEM_A_DQ<48>	163	DQ48	
28	BI	=MEM_A_DQ<49>	165	DQ49	
			167	VSS	
28	BI	=MEM_A_DQS_N<6>	169	DQS6*	
28	BI	=MEM_A_DQS_P<6>	171	DQS6	
			173	VSS	
28	BI	=MEM_A_DQ<50>	175	DQ50	
28	BI	=MEM_A_DQ<51>	177	DQ51	
			179	VSS	
28	BI	=MEM_A_DQ<56>	181	DQ56	
28	BI	=MEM_A_DQ<57>	183	DQ57	
			185	VSS	
			187	DM7	
			189	VSS	
28	BI	=MEM_A_DQ<58>	191	DQ58	
28	BI	=MEM_A_DQ<59>	193	DQ59	
			195	VSS	
		6 MEM_A_SA<0>	197	SA0	
			199	VDDSPD	
		6 MEM_A_SA<1>	201	SA1	
			203	VTT	

94 11 6	IN	MEM_A_CKE<1>	74	CKE1	
			76	VDD	
94 11 6	IN	MEM_A_A<15>	78	A15	
94 11 6	IN	MEM_A_A<14>	80	A14	
			82	VDD	
94 11 6	IN	MEM_A_A<11>	84	A11	
94 11 6	IN	MEM_A_A<7>	86	A7	
			88	VDD	
94 11 6	IN	MEM_A_A<6>	90	A6	
94 11 6	IN	MEM_A_A<4>	92	A4	
			94	VDD	
94 11 6	IN	MEM_A_A<2>	96	A2	
94 11 6	IN	MEM_A_A<0>	98	A0	
			100	VDD	
94 11 6	IN	MEM_A_CLK_P<1>	102	CK1	
94 11 6	IN	MEM_A_CLK_N<1>	104	CK1*	
			106	VDD	
94 11 6	IN	MEM_A_BA<1>	108	BA1	
94 11 6	IN	MEM_A_RAS_L	110	RAS*	
			112	VDD	
94 11 6	IN	MEM_A_CS_L<0>	114	S0*	
94 11 6	IN	MEM_A_ODT<0>	116	ODT0	
			118	VDD	
94 11 6	IN	MEM_A_ODT<1>	120	ODT1	
NC			122	NC	
			124	VDD	
			126	VREFCA	
			128	VSS	
28	BI	=MEM_A_DQ<36>	130	DQ36	
28	BI	=MEM_A_DQ<37>	132	DQ37	
			134	VSS	
			136	DM4	
			138	VSS	
28	BI	=MEM_A_DQ<38>	140	DQ38	
28	BI	=MEM_A_DQ<39>	142	DQ39	
			144	VSS	
28	BI	=MEM_A_DQ<44>	146	DQ44	
28	BI	=MEM_A_DQ<45>	148	DQ45	
			150	VSS	
28	BI	=MEM_A_DQS_N<5>	152	DQS5*	
28	BI	=MEM_A_DQS_P<5>	154	DQS5	
			156	VSS	
28	BI	=MEM_A_DQ<46>	158	DQ46	
28	BI	=MEM_A_DQ<47>	160	DQ47	
			162	VSS	
28	BI	=MEM_A_DQ<52>	164	DQ52	
28	BI	=MEM_A_DQ<53>	166	DQ53	
			168	VSS	
			170	DM6	
			172	VSS	
28	BI	=MEM_A_DQ<54>	174	DQ54	
28	BI	=MEM_A_DQ<55>	176	DQ55	
			178	VSS	
28	BI	=MEM_A_DQ<60>	180	DQ60	
28	BI	=MEM_A_DQ<61>	182	DQ61	
			184	VSS	
28	BI	=MEM_A_DQS_N<7>	186	DQS7*	
28	BI	=MEM_A_DQS_P<7>	188	DQS7	
			190	VSS	
28	BI	=MEM_A_DQ<62>	192	DQ62	
28	BI	=MEM_A_DQ<63>	194	DQ63	
			196	VSS	
		MEM_EVENT_L	198	EVENT*	
28	BI	=I2C_SODIMMA_SDA	200	SDA	
48	IN	=I2C_SODIMMA_SCL	202	SCL	
			204	VTT	

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

OMIT_TABLE

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2)
CRITICAL
KEY

			1	VREFDQ	
			3	VSS	
28	BI	=MEM_A_DQ<0>	5	DQ0	
28	BI	=MEM_A_DQ<1>	7	DQ1	
			9	VSS	
			11	DM0	
			13	VSS	
28	BI	=MEM_A_DQ<2>	15	DQ2	
28	BI	=MEM_A_DQ<3>	17	DQ3	
			19	VSS	
28	BI	=MEM_A_DQ<8>	21	DQ8	
28	BI	=MEM_A_DQ<9>	23	DQ9	
			25	VSS	
28	BI	=MEM_A_DQS_N<1>	27	DQS1*	
28	BI	=MEM_A_DQS_P<1>	29	DQS1	
			31	VSS	
28	BI	=MEM_A_DQ<10>	33	DQ10	
28	BI	=MEM_A_DQ<11>	35	DQ11	
			37	VSS	
28	BI	=MEM_A_DQ<16>	39	DQ16	
28	BI	=MEM_A_DQ<17>	41	DQ17	
			43	VSS	
28	BI	=MEM_A_DQS_N<2>	45	DQS2*	
28	BI	=MEM_A_DQS_P<2>	47	DQS2	
			49	VSS	
28	BI	=MEM_A_DQ<18>	51	DQ18	
28	BI	=MEM_A_DQ<19>	53	DQ19	
			55	VSS	
28	BI	=MEM_A_DQ<24>	57	DQ24	
28	BI	=MEM_A_DQ<25>	59	DQ25	
			61	VSS	
			63	DM3	
			65	VSS	
28	BI	=MEM_A_DQ<26>	67	DQ26	
28	BI	=MEM_A_DQ<27>	69	DQ27	
			71	VSS	

			2	VSS	
28	BI	=MEM_A_DQ<4>	4	DQ4	
28	BI	=MEM_A_DQ<5>	6	DQ5	
			8	VSS	
28	BI	=MEM_A_DQS_N<0>	10	DQS0*	
28	BI	=MEM_A_DQS_P<0>	12	DQS0	
			14	VSS	
28	BI	=MEM_A_DQ<6>	16	DQ6	
28	BI	=MEM_A_DQ<7>	18	DQ7	
			20	VSS	
28	BI	=MEM_A_DQ<12>	22	DQ12	
28	BI	=MEM_A_DQ<13>	24	DQ13	
			26	VSS	
			28	DM1	
26 29	IN	MEM_RESET_L	30	RESET*	
			32	VSS	
28	BI	=MEM_A_DQ<14>	34	DQ14	
28	BI	=MEM_A_DQ<15>	36	DQ15	
			38	VSS	
28	BI	=MEM_A_DQ<20>	40	DQ20	
28	BI	=MEM_A_DQ<21>	42	DQ21	
			44	VSS	
			46	DM2	
			48	VSS	
28	BI	=MEM_A_DQ<22>	50	DQ22	
28	BI	=MEM_A_DQ<23>	52	DQ23	
			54	VSS	
28	BI	=MEM_A_DQ<28>	56	DQ28	
28	BI	=MEM_A_DQ<29>	58	DQ29	
			60	VSS	
28	BI	=MEM_A_DQS_N<3>	62	DQS3*	
28	BI	=MEM_A_DQS_P<3>	64	DQS3	
			66	VSS	
28	BI	=MEM_A_DQ<30>	68	DQ30	
28	BI	=MEM_A_DQ<31>	70	DQ31	
			72	VSS	

See CSA05 BOM table

PP0V75_S3_MEM_VREFCA_A 31 93

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

7 =PPSPD_S0_MEM_A

=PP0V75_S0_MEM_VTT_A 7

C2950 C2951 C2952 C2953
1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 29 OF 132
SHEET: 27 OF 105

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

94 11 6 MEM_A_DQS_N<0> MAKE_BASE=TRUE =MEM_A_DQS_N<0> 27
94 11 6 MEM_A_DQS_P<0> MAKE_BASE=TRUE =MEM_A_DQS_P<0> 27

94 11 6 MEM_A_DQ<7> MAKE_BASE=TRUE =MEM_A_DQ<3> 27
94 11 6 MEM_A_DQ<6> MAKE_BASE=TRUE =MEM_A_DQ<6> 27
94 11 6 MEM_A_DQ<5> MAKE_BASE=TRUE =MEM_A_DQ<5> 27
94 11 6 MEM_A_DQ<4> MAKE_BASE=TRUE =MEM_A_DQ<4> 27
94 11 6 MEM_A_DQ<3> MAKE_BASE=TRUE =MEM_A_DQ<7> 27
94 11 6 MEM_A_DQ<2> MAKE_BASE=TRUE =MEM_A_DQ<0> 27
94 11 6 MEM_A_DQ<1> MAKE_BASE=TRUE =MEM_A_DQ<1> 27
94 11 6 MEM_A_DQ<0> MAKE_BASE=TRUE =MEM_A_DQ<2> 27

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

94 11 6 MEM_A_DQS_N<1> MAKE_BASE=TRUE =MEM_A_DQS_N<1> 27
94 11 6 MEM_A_DQS_P<1> MAKE_BASE=TRUE =MEM_A_DQS_P<1> 27

94 11 6 MEM_A_DQ<15> MAKE_BASE=TRUE =MEM_A_DQ<15> 27
94 11 6 MEM_A_DQ<14> MAKE_BASE=TRUE =MEM_A_DQ<14> 27
94 11 6 MEM_A_DQ<13> MAKE_BASE=TRUE =MEM_A_DQ<12> 27
94 11 6 MEM_A_DQ<12> MAKE_BASE=TRUE =MEM_A_DQ<13> 27
94 11 6 MEM_A_DQ<11> MAKE_BASE=TRUE =MEM_A_DQ<10> 27
94 11 6 MEM_A_DQ<10> MAKE_BASE=TRUE =MEM_A_DQ<11> 27
94 11 6 MEM_A_DQ<9> MAKE_BASE=TRUE =MEM_A_DQ<9> 27
94 11 6 MEM_A_DQ<8> MAKE_BASE=TRUE =MEM_A_DQ<8> 27

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

94 11 6 MEM_A_DQS_N<2> MAKE_BASE=TRUE =MEM_A_DQS_N<2> 27
94 11 6 MEM_A_DQS_P<2> MAKE_BASE=TRUE =MEM_A_DQS_P<2> 27

94 11 6 MEM_A_DQ<23> MAKE_BASE=TRUE =MEM_A_DQ<23> 27
94 11 6 MEM_A_DQ<22> MAKE_BASE=TRUE =MEM_A_DQ<22> 27
94 11 6 MEM_A_DQ<21> MAKE_BASE=TRUE =MEM_A_DQ<17> 27
94 11 6 MEM_A_DQ<20> MAKE_BASE=TRUE =MEM_A_DQ<20> 27
94 11 6 MEM_A_DQ<19> MAKE_BASE=TRUE =MEM_A_DQ<19> 27
94 11 6 MEM_A_DQ<18> MAKE_BASE=TRUE =MEM_A_DQ<18> 27
94 11 6 MEM_A_DQ<17> MAKE_BASE=TRUE =MEM_A_DQ<16> 27
94 11 6 MEM_A_DQ<16> MAKE_BASE=TRUE =MEM_A_DQ<21> 27

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

94 11 6 MEM_A_DQS_N<3> MAKE_BASE=TRUE =MEM_A_DQS_N<3> 27
94 11 6 MEM_A_DQS_P<3> MAKE_BASE=TRUE =MEM_A_DQS_P<3> 27

94 11 6 MEM_A_DQ<31> MAKE_BASE=TRUE =MEM_A_DQ<31> 27
94 11 6 MEM_A_DQ<30> MAKE_BASE=TRUE =MEM_A_DQ<30> 27
94 11 6 MEM_A_DQ<29> MAKE_BASE=TRUE =MEM_A_DQ<29> 27
94 11 6 MEM_A_DQ<28> MAKE_BASE=TRUE =MEM_A_DQ<28> 27
94 11 6 MEM_A_DQ<27> MAKE_BASE=TRUE =MEM_A_DQ<27> 27
94 11 6 MEM_A_DQ<26> MAKE_BASE=TRUE =MEM_A_DQ<26> 27
94 11 6 MEM_A_DQ<25> MAKE_BASE=TRUE =MEM_A_DQ<25> 27
94 11 6 MEM_A_DQ<24> MAKE_BASE=TRUE =MEM_A_DQ<24> 27

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

94 11 6 MEM_A_DQS_N<4> MAKE_BASE=TRUE =MEM_A_DQS_N<4> 27
94 11 6 MEM_A_DQS_P<4> MAKE_BASE=TRUE =MEM_A_DQS_P<4> 27

94 11 6 MEM_A_DQ<39> MAKE_BASE=TRUE =MEM_A_DQ<38> 27
94 11 6 MEM_A_DQ<38> MAKE_BASE=TRUE =MEM_A_DQ<37> 27
94 11 6 MEM_A_DQ<37> MAKE_BASE=TRUE =MEM_A_DQ<39> 27
94 11 6 MEM_A_DQ<36> MAKE_BASE=TRUE =MEM_A_DQ<33> 27
94 11 6 MEM_A_DQ<35> MAKE_BASE=TRUE =MEM_A_DQ<35> 27
94 11 6 MEM_A_DQ<34> MAKE_BASE=TRUE =MEM_A_DQ<34> 27
94 11 6 MEM_A_DQ<33> MAKE_BASE=TRUE =MEM_A_DQ<32> 27
94 11 6 MEM_A_DQ<32> MAKE_BASE=TRUE =MEM_A_DQ<36> 27

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

94 11 6 MEM_A_DQS_N<5> MAKE_BASE=TRUE =MEM_A_DQS_N<5> 27
94 11 6 MEM_A_DQS_P<5> MAKE_BASE=TRUE =MEM_A_DQS_P<5> 27

94 11 6 MEM_A_DQ<47> MAKE_BASE=TRUE =MEM_A_DQ<47> 27
94 11 6 MEM_A_DQ<46> MAKE_BASE=TRUE =MEM_A_DQ<41> 27
94 11 6 MEM_A_DQ<45> MAKE_BASE=TRUE =MEM_A_DQ<43> 27
94 11 6 MEM_A_DQ<44> MAKE_BASE=TRUE =MEM_A_DQ<44> 27
94 11 6 MEM_A_DQ<43> MAKE_BASE=TRUE =MEM_A_DQ<40> 27
94 11 6 MEM_A_DQ<42> MAKE_BASE=TRUE =MEM_A_DQ<46> 27
94 11 6 MEM_A_DQ<41> MAKE_BASE=TRUE =MEM_A_DQ<42> 27
94 11 6 MEM_A_DQ<40> MAKE_BASE=TRUE =MEM_A_DQ<45> 27

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

94 11 6 MEM_A_DQS_N<6> MAKE_BASE=TRUE =MEM_A_DQS_N<6> 27
94 11 6 MEM_A_DQS_P<6> MAKE_BASE=TRUE =MEM_A_DQS_P<6> 27

94 11 6 MEM_A_DQ<55> MAKE_BASE=TRUE =MEM_A_DQ<49> 27
94 11 6 MEM_A_DQ<54> MAKE_BASE=TRUE =MEM_A_DQ<54> 27
94 11 6 MEM_A_DQ<53> MAKE_BASE=TRUE =MEM_A_DQ<55> 27
94 11 6 MEM_A_DQ<52> MAKE_BASE=TRUE =MEM_A_DQ<52> 27
94 11 6 MEM_A_DQ<51> MAKE_BASE=TRUE =MEM_A_DQ<51> 27
94 11 6 MEM_A_DQ<50> MAKE_BASE=TRUE =MEM_A_DQ<50> 27
94 11 6 MEM_A_DQ<49> MAKE_BASE=TRUE =MEM_A_DQ<53> 27
94 11 6 MEM_A_DQ<48> MAKE_BASE=TRUE =MEM_A_DQ<48> 27

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

94 11 6 MEM_A_DQS_N<7> MAKE_BASE=TRUE =MEM_A_DQS_N<7> 27
94 11 6 MEM_A_DQS_P<7> MAKE_BASE=TRUE =MEM_A_DQS_P<7> 27

94 11 6 MEM_A_DQ<63> MAKE_BASE=TRUE =MEM_A_DQ<59> 27
94 11 6 MEM_A_DQ<62> MAKE_BASE=TRUE =MEM_A_DQ<58> 27
94 11 6 MEM_A_DQ<61> MAKE_BASE=TRUE =MEM_A_DQ<56> 27
94 11 6 MEM_A_DQ<60> MAKE_BASE=TRUE =MEM_A_DQ<61> 27
94 11 6 MEM_A_DQ<59> MAKE_BASE=TRUE =MEM_A_DQ<63> 27
94 11 6 MEM_A_DQ<58> MAKE_BASE=TRUE =MEM_A_DQ<62> 27
94 11 6 MEM_A_DQ<57> MAKE_BASE=TRUE =MEM_A_DQ<57> 27
94 11 6 MEM_A_DQ<56> MAKE_BASE=TRUE =MEM_A_DQ<60> 27

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

94 11 6 MEM_B_DQS_N<0> MAKE_BASE=TRUE =MEM_B_DQS_N<0> 29
94 11 6 MEM_B_DQS_P<0> MAKE_BASE=TRUE =MEM_B_DQS_P<0> 29

94 11 6 MEM_B_DQ<7> MAKE_BASE=TRUE =MEM_B_DQ<6> 29
94 11 6 MEM_B_DQ<6> MAKE_BASE=TRUE =MEM_B_DQ<3> 29
94 11 6 MEM_B_DQ<5> MAKE_BASE=TRUE =MEM_B_DQ<5> 29
94 11 6 MEM_B_DQ<4> MAKE_BASE=TRUE =MEM_B_DQ<4> 29
94 11 6 MEM_B_DQ<3> MAKE_BASE=TRUE =MEM_B_DQ<1> 29
94 11 6 MEM_B_DQ<2> MAKE_BASE=TRUE =MEM_B_DQ<7> 29
94 11 6 MEM_B_DQ<1> MAKE_BASE=TRUE =MEM_B_DQ<2> 29
94 11 6 MEM_B_DQ<0> MAKE_BASE=TRUE =MEM_B_DQ<0> 29

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

94 11 6 MEM_B_DQS_N<1> MAKE_BASE=TRUE =MEM_B_DQS_N<1> 29
94 11 6 MEM_B_DQS_P<1> MAKE_BASE=TRUE =MEM_B_DQS_P<1> 29

94 11 6 MEM_B_DQ<15> MAKE_BASE=TRUE =MEM_B_DQ<15> 29
94 11 6 MEM_B_DQ<14> MAKE_BASE=TRUE =MEM_B_DQ<14> 29
94 11 6 MEM_B_DQ<13> MAKE_BASE=TRUE =MEM_B_DQ<13> 29
94 11 6 MEM_B_DQ<12> MAKE_BASE=TRUE =MEM_B_DQ<12> 29
94 11 6 MEM_B_DQ<11> MAKE_BASE=TRUE =MEM_B_DQ<11> 29
94 11 6 MEM_B_DQ<10> MAKE_BASE=TRUE =MEM_B_DQ<10> 29
94 11 6 MEM_B_DQ<9> MAKE_BASE=TRUE =MEM_B_DQ<9> 29
94 11 6 MEM_B_DQ<8> MAKE_BASE=TRUE =MEM_B_DQ<8> 29

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

94 11 6 MEM_B_DQS_N<2> MAKE_BASE=TRUE =MEM_B_DQS_N<2> 29
94 11 6 MEM_B_DQS_P<2> MAKE_BASE=TRUE =MEM_B_DQS_P<2> 29

94 11 6 MEM_B_DQ<23> MAKE_BASE=TRUE =MEM_B_DQ<23> 29
94 11 6 MEM_B_DQ<22> MAKE_BASE=TRUE =MEM_B_DQ<22> 29
94 11 6 MEM_B_DQ<21> MAKE_BASE=TRUE =MEM_B_DQ<21> 29
94 11 6 MEM_B_DQ<20> MAKE_BASE=TRUE =MEM_B_DQ<20> 29
94 11 6 MEM_B_DQ<19> MAKE_BASE=TRUE =MEM_B_DQ<19> 29
94 11 6 MEM_B_DQ<18> MAKE_BASE=TRUE =MEM_B_DQ<18> 29
94 11 6 MEM_B_DQ<17> MAKE_BASE=TRUE =MEM_B_DQ<17> 29
94 11 6 MEM_B_DQ<16> MAKE_BASE=TRUE =MEM_B_DQ<16> 29

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

94 11 6 MEM_B_DQS_N<3> MAKE_BASE=TRUE =MEM_B_DQS_N<3> 29
94 11 6 MEM_B_DQS_P<3> MAKE_BASE=TRUE =MEM_B_DQS_P<3> 29

94 11 6 MEM_B_DQ<31> MAKE_BASE=TRUE =MEM_B_DQ<31> 29
94 11 6 MEM_B_DQ<30> MAKE_BASE=TRUE =MEM_B_DQ<30> 29
94 11 6 MEM_B_DQ<29> MAKE_BASE=TRUE =MEM_B_DQ<29> 29
94 11 6 MEM_B_DQ<28> MAKE_BASE=TRUE =MEM_B_DQ<28> 29
94 11 6 MEM_B_DQ<27> MAKE_BASE=TRUE =MEM_B_DQ<27> 29
94 11 6 MEM_B_DQ<26> MAKE_BASE=TRUE =MEM_B_DQ<26> 29
94 11 6 MEM_B_DQ<25> MAKE_BASE=TRUE =MEM_B_DQ<25> 29
94 11 6 MEM_B_DQ<24> MAKE_BASE=TRUE =MEM_B_DQ<24> 29

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

94 11 6 MEM_B_DQS_N<4> MAKE_BASE=TRUE =MEM_B_DQS_N<4> 29
94 11 6 MEM_B_DQS_P<4> MAKE_BASE=TRUE =MEM_B_DQS_P<4> 29

94 11 6 MEM_B_DQ<39> MAKE_BASE=TRUE =MEM_B_DQ<39> 29
94 11 6 MEM_B_DQ<38> MAKE_BASE=TRUE =MEM_B_DQ<38> 29
94 11 6 MEM_B_DQ<37> MAKE_BASE=TRUE =MEM_B_DQ<37> 29
94 11 6 MEM_B_DQ<36> MAKE_BASE=TRUE =MEM_B_DQ<36> 29
94 11 6 MEM_B_DQ<35> MAKE_BASE=TRUE =MEM_B_DQ<35> 29
94 11 6 MEM_B_DQ<34> MAKE_BASE=TRUE =MEM_B_DQ<34> 29
94 11 6 MEM_B_DQ<33> MAKE_BASE=TRUE =MEM_B_DQ<33> 29
94 11 6 MEM_B_DQ<32> MAKE_BASE=TRUE =MEM_B_DQ<32> 29

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

94 11 6 MEM_B_DQS_N<5> MAKE_BASE=TRUE =MEM_B_DQS_N<5> 29
94 11 6 MEM_B_DQS_P<5> MAKE_BASE=TRUE =MEM_B_DQS_P<5> 29

94 11 6 MEM_B_DQ<47> MAKE_BASE=TRUE =MEM_B_DQ<47> 29
94 11 6 MEM_B_DQ<46> MAKE_BASE=TRUE =MEM_B_DQ<46> 29
94 11 6 MEM_B_DQ<45> MAKE_BASE=TRUE =MEM_B_DQ<45> 29
94 11 6 MEM_B_DQ<44> MAKE_BASE=TRUE =MEM_B_DQ<44> 29
94 11 6 MEM_B_DQ<43> MAKE_BASE=TRUE =MEM_B_DQ<43> 29
94 11 6 MEM_B_DQ<42> MAKE_BASE=TRUE =MEM_B_DQ<42> 29
94 11 6 MEM_B_DQ<41> MAKE_BASE=TRUE =MEM_B_DQ<41> 29
94 11 6 MEM_B_DQ<40> MAKE_BASE=TRUE =MEM_B_DQ<40> 29

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

94 11 6 MEM_B_DQS_N<6> MAKE_BASE=TRUE =MEM_B_DQS_N<6> 29
94 11 6 MEM_B_DQS_P<6> MAKE_BASE=TRUE =MEM_B_DQS_P<6> 29

94 11 6 MEM_B_DQ<55> MAKE_BASE=TRUE =MEM_B_DQ<55> 29
94 11 6 MEM_B_DQ<54> MAKE_BASE=TRUE =MEM_B_DQ<54> 29
94 11 6 MEM_B_DQ<53> MAKE_BASE=TRUE =MEM_B_DQ<53> 29
94 11 6 MEM_B_DQ<52> MAKE_BASE=TRUE =MEM_B_DQ<52> 29
94 11 6 MEM_B_DQ<51> MAKE_BASE=TRUE =MEM_B_DQ<51> 29
94 11 6 MEM_B_DQ<50> MAKE_BASE=TRUE =MEM_B_DQ<50> 29
94 11 6 MEM_B_DQ<49> MAKE_BASE=TRUE =MEM_B_DQ<49> 29
94 11 6 MEM_B_DQ<48> MAKE_BASE=TRUE =MEM_B_DQ<48> 29

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

94 11 6 MEM_B_DQS_N<7> MAKE_BASE=TRUE =MEM_B_DQS_N<7> 29
94 11 6 MEM_B_DQS_P<7> MAKE_BASE=TRUE =MEM_B_DQS_P<7> 29

94 11 6 MEM_B_DQ<63> MAKE_BASE=TRUE =MEM_B_DQ<63> 29
94 11 6 MEM_B_DQ<62> MAKE_BASE=TRUE =MEM_B_DQ<62> 29
94 11 6 MEM_B_DQ<61> MAKE_BASE=TRUE =MEM_B_DQ<61> 29
94 11 6 MEM_B_DQ<60> MAKE_BASE=TRUE =MEM_B_DQ<60> 29
94 11 6 MEM_B_DQ<59> MAKE_BASE=TRUE =MEM_B_DQ<59> 29
94 11 6 MEM_B_DQ<58> MAKE_BASE=TRUE =MEM_B_DQ<58> 29
94 11 6 MEM_B_DQ<57> MAKE_BASE=TRUE =MEM_B_DQ<57> 29
94 11 6 MEM_B_DQ<56> MAKE_BASE=TRUE =MEM_B_DQ<56> 29

SYNC_MASTER=K92_SUMA SYNC_DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 30 OF 132

SHEET 28 OF 105

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM0_SCL
- =I2C_SODIMM0_SDA

BOM options provided by this page:
(NONE)

7 =PP1V5_S3_MEM_B

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

PLACE_NEAR=J3100.75:2.54mm

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

PLACE_NEAR=J3100.75:2.54mm

93 31 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (2 OF 2)

KEY

94 11 6 IN MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1> IN 6 11 94
	75	VDD	VDD	76	
NC	77	NC	A15	78	MEM_B_A<15> IN 6 11 94
94 11 6 IN MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14> IN 6 11 94
	81	VDD	VDD	82	
94 11 6 IN MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11> IN 6 11 94
94 11 6 IN MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7> IN 6 11 94
	87	VDD	VDD	88	
94 11 6 IN MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6> IN 6 11 94
94 11 6 IN MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4> IN 6 11 94
	93	VDD	VDD	94	
94 11 6 IN MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2> IN 6 11 94
94 11 6 IN MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0> IN 6 11 94
	99	VDD	VDD	100	
94 11 6 IN MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1> IN 6 11 94
94 11 6 IN MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1> IN 6 11 94
	105	VDD	VDD	106	
94 11 6 IN MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1> IN 6 11 94
94 11 6 IN MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L IN 6 11 94
	111	VDD	VDD	112	
94 11 6 IN MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0> IN 6 11 94
94 11 6 IN MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0> IN 6 11 94
	117	VDD	VDD	118	
94 11 6 IN MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1> IN 6 11 94
94 11 6 IN MEM_B_CS_L<1>	121	S1*	NC	122	NC
	123	VDD	VDD	124	
NC	125	TEST	VREFCA	126	
	127	VSS	VSS	128	
28 BI =MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36> BI 28
28 BI =MEM_B_DQ<33>	131	DQ33	DQ37	132	=MEM_B_DQ<37> BI 28
	133	VSS	VSS	134	
28 BI =MEM_B_DQS_N<4>	135	DQS4*	DM4	136	
28 BI =MEM_B_DQS_P<4>	137	DQS4	VSS	138	
	139	VSS	DQ38	140	=MEM_B_DQ<38> BI 28
28 BI =MEM_B_DQ<34>	141	DQ34	DQ39	142	=MEM_B_DQ<39> BI 28
28 BI =MEM_B_DQ<35>	143	DQ35	VSS	144	
	145	VSS	DQ44	146	=MEM_B_DQ<44> BI 28
28 BI =MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45> BI 28
28 BI =MEM_B_DQ<41>	149	DQ41	VSS	150	
	151	VSS	DQS5*	152	=MEM_B_DQS_N<5> BI 28
	153	DM5	DQS5	154	=MEM_B_DQS_P<5> BI 28
	155	VSS	VSS	156	
28 BI =MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46> BI 28
28 BI =MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47> BI 28
	161	VSS	VSS	162	
28 BI =MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52> BI 28
28 BI =MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53> BI 28
	167	VSS	VSS	168	
28 BI =MEM_B_DQS_N<6>	169	DQS6*	DM6	170	
28 BI =MEM_B_DQS_P<6>	171	DQS6	VSS	172	
	173	VSS	DQ54	174	=MEM_B_DQ<54> BI 28
28 BI =MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55> BI 28
28 BI =MEM_B_DQ<51>	177	DQ51	VSS	178	
	179	VSS	DQ60	180	=MEM_B_DQ<60> BI 28
28 BI =MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61> BI 28
28 BI =MEM_B_DQ<57>	183	DQ57	VSS	184	
	185	VSS	DQS7*	186	=MEM_B_DQS_N<7> BI 28
	187	DM7	DQS7	188	=MEM_B_DQS_P<7> BI 28
	189	VSS	VSS	190	
28 BI =MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62> BI 28
28 BI =MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63> BI 28
	195	VSS	VSS	196	
6 MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L OUT 27 45 46
	199	VDDSPD	SDA	200	=I2C_SODIMM0_SDA BI 48
6 MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMM0_SCL IN 48
	203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B 7
	205	MTG PIN	MTG PIN	206	
	207	MTG PIN	MTG PIN	208	
	209	MTG PIN	MTG PIN	210	
	211	MTG PIN	MTG PIN	212	

516S0806

SPD ADDR=0xA4(WR)/0xA5(RD)

7 =PPSPD_S0_MEM_B

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

PP0V75_S3_MEM_VREFCA_B 31 93

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (1 OF 2)

CRITICAL

KEY

	1	VREFDQ	VSS	2	
	3	VSS	DQ4	4	=MEM_B_DQ<4> BI 28
28 BI =MEM_B_DQ<0>	5	DQ0	DQ5	6	=MEM_B_DQ<5> BI 28
28 BI =MEM_B_DQ<1>	7	DQ1	VSS	8	
	9	VSS	DQS0*	10	=MEM_B_DQS_N<0> BI 28
	11	DM0	DQS0	12	=MEM_B_DQS_P<0> BI 28
	13	VSS	VSS	14	
28 BI =MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6> BI 28
28 BI =MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7> BI 28
	19	VSS	VSS	20	
28 BI =MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12> BI 28
28 BI =MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13> BI 28
	25	VSS	VSS	26	
28 BI =MEM_B_DQS_N<1>	27	DQS1*	DM1	28	
28 BI =MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L IN 26 27
	31	VSS	VSS	32	
28 BI =MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14> BI 28
28 BI =MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15> BI 28
	37	VSS	VSS	38	
28 BI =MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20> BI 28
28 BI =MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21> BI 28
	43	VSS	VSS	44	
28 BI =MEM_B_DQS_N<2>	45	DQS2*	DM2	46	
28 BI =MEM_B_DQS_P<2>	47	DQS2	VSS	48	
	49	VSS	DQ22	50	=MEM_B_DQ<22> BI 28
28 BI =MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23> BI 28
28 BI =MEM_B_DQ<19>	53	DQ19	VSS	54	
	55	VSS	DQ28	56	=MEM_B_DQ<28> BI 28
28 BI =MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29> BI 28
28 BI =MEM_B_DQ<25>	59	DQ25	VSS	60	
	61	VSS	DQS3*	62	=MEM_B_DQS_N<3> BI 28
	63	DM3	DQS3	64	=MEM_B_DQS_P<3> BI 28
	65	VSS	VSS	66	
28 BI =MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30> BI 28
28 BI =MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31> BI 28
	71	VSS	VSS	72	

516S0806

"Expansion" (bottom) slot

SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
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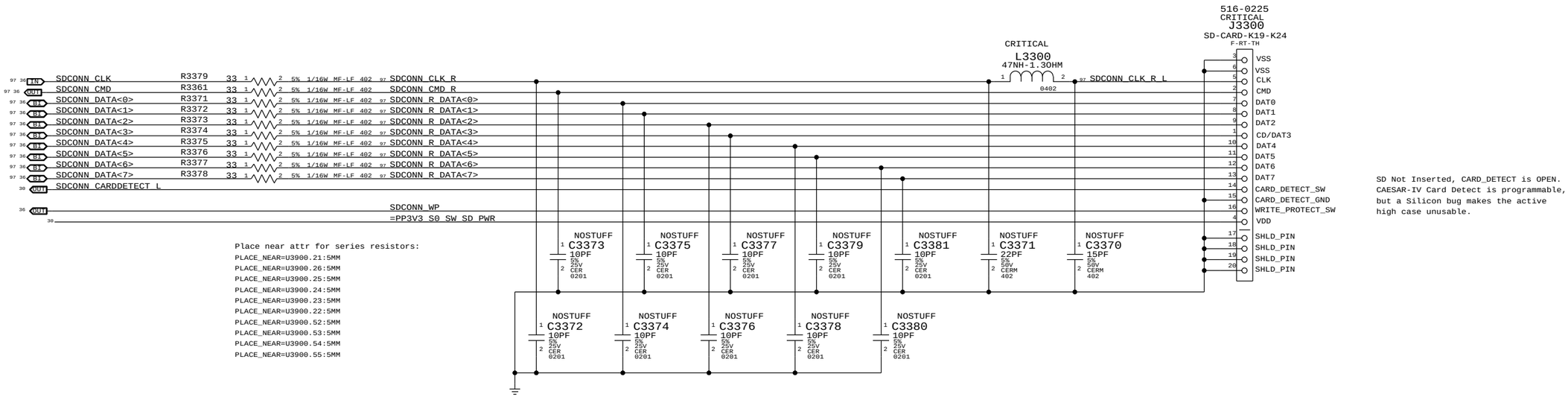
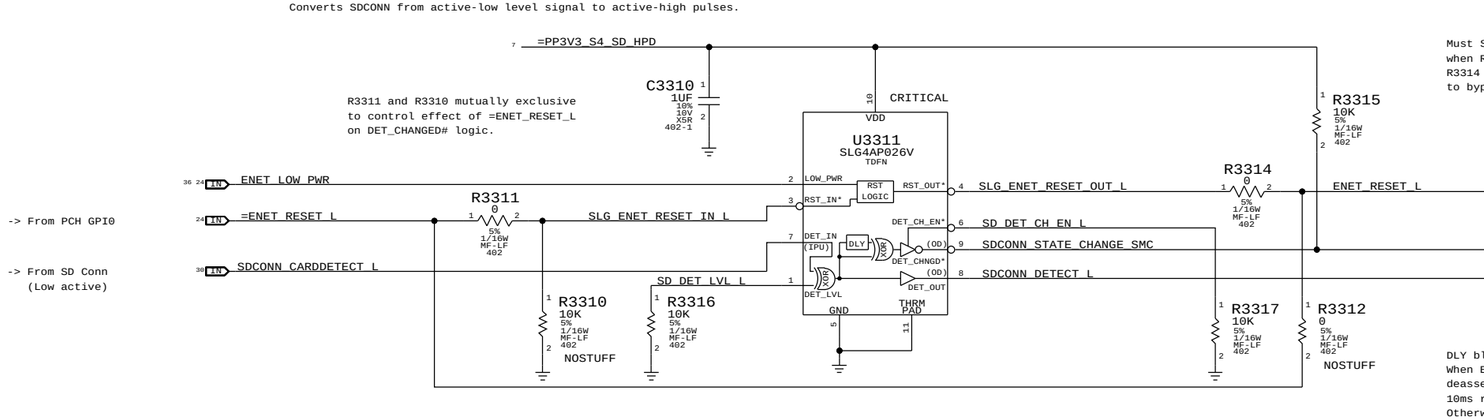
SD Card Connector



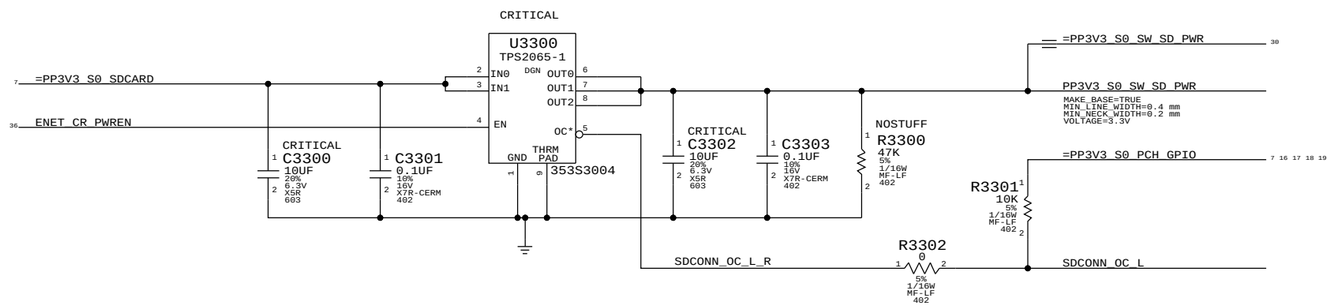
SD Detect & Reset Logic

SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses.



SD Card 3.3V Overcurrent Protection

TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SYNC_MASTER=J31_YONAS SYNC_DATE=10/25/2011

PAGE TITLE: SD Card Connector

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
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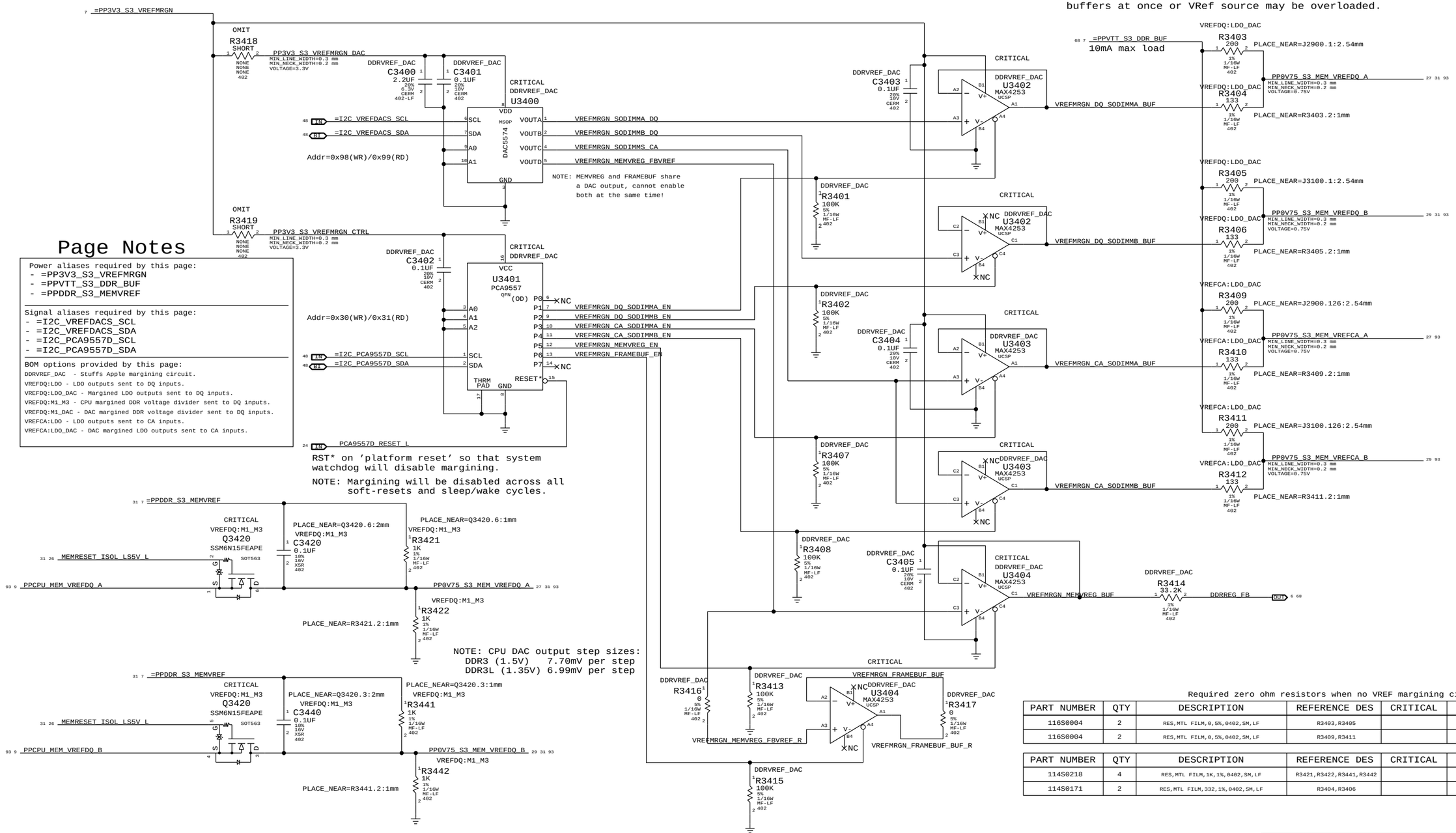

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J31_ANNE SYNC_DATE=06/09/2011

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
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AIRPORT

C3531 0.1UF 10% 16V X5R-CERM 0201 — PLACE_NEAR=J3501.15:2.54mm
C3530 0.1UF 10% 16V X5R-CERM 0201 — PLACE_NEAR=J3501.17:2.54mm

PCIE_AP_R2D_C_P — IN 16 96
PCIE_AP_R2D_C_N — IN 16 96

R3510 0 5% 1/20W MF 201
R3511 0 5% 1/20W MF 201

PCIE_AP_D2R_P — OUT 16 96
PCIE_AP_D2R_N — OUT 16 96

WIFI_EVENT_L — OUT 6 45 46

96 6 PCIE_AP_R2D_P
96 6 PCIE_AP_R2D_N
96 PCIE_AP_D2R_R_P
96 PCIE_AP_D2R_R_N

516S0582
CRITICAL
J3501
500913-0302
F-ST-SM

AP_TEMP_SMB_SCL_PD
AP_TEMP_SMB_SDA_PD

R3520 51 5% 1/16W MF-LF 402
R3521 51 5% 1/16W MF-LF 402

6 PP3V3_S3RS4_BT_F
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm

C3532 0.01UF 10% 16V CERM 402
L3505 BTPWR:S4 FERR-120-OHM-1.5A 0402-LF — PLACE_NEAR=J3501.27:2.54mm
=PP3V3_S4_BT — 7 32

CRITICAL
L3501
330-OHM-80MA
DLP11S SYM_VER-1

PCIE_CLK100M_AP_P — IN 16 96
PCIE_CLK100M_AP_N — IN 16 96
101 6 PCIE_CLK100M_AP_CONN_P
101 6 PCIE_CLK100M_AP_CONN_N
PLACE_NEAR=J3501.11:2.54mm

BLUETOOTH

95 6 USB_BT_CONN_P
95 6 USB_BT_CONN_N

NOSTUFF R3517 15K 1% 1/20W MF 201
BTPWR:S3 R3518 0 5% 1/20W MF 201
NOSTUFF R3515 15K 1% 1/20W MF 201
NOSTUFF R3516 15K 1% 1/20W MF 201

U3510 PI3USB102ZLE TQFN CRITICAL
VCC, Y+, Y-, SEL, OE*, GND, M+, M-, D+, D-

=PP3V3_S4_BT — 7 32
C3510 0.1UF 10% 6.3V X5R 201

USB_BT_WAKEP
USB_BT_WAKEN
USB_BT_N — BI 8 95
USB_BT_P — BI 8 95

BTPWR:S4 R3514 15K 1% 1/20W MF 201
BTPWR:S4 R3512 15K 1% 1/20W MF 201
NOSTUFF R3513 15K 1% 1/20W MF 201

BTPWR:S4
CRITICAL
Q3510
VESM
=BT_WAKE_L — OUT 46
SSM3K15AMFVAPE

BTPWR:S4 R3519 0 5% 1/20W MF 201
74 45 26 17 PM_SLP_S4_L — IN
BTMUX_SEL

NOSTUFF C3511 0.01UF 10% 16V X5R 201

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

Supervisor & CLKFREG # ISolation

Delay = 60 ms +/- 20%

PP3V3_WLAN_F — 32
=PP3V3_S3_WLAN — 7 32

R3553 100K 1% 1/16W MF-LF 402
R3554 232K 1% 1/16W MF-LF 402
P3V3WLAN_VMON
R3555 100K 1% 1/16W MF-LF 402

CRITICAL
U3540
SLG4AP016V
TDFN
VDD, SENSE, 0.7V, RESET*, MR*, EN, IN, OUT (OD), THRM PAD, GND, DLY

C3540 0.1uF 20% 10V CERM 402

AP_RESET_L — IN 24
AP_PWR_EN — IN 18 23 74
AP_CLKREQ_L — OUT 16

PCIE_WAKE_L — OUT 6 17 24

518S0815
CRITICAL
J3502
8190-3506-K281
F-RT-SMT

6 PP5V_S3_ALSCAMERA_F
=I2C_ALS_SCL — IN 48
=I2C_ALS_SDA — BI 48
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
95 6 USB_CAMERA_CONN_P
95 6 USB_CAMERA_CONN_N

ALS CAMERA

275 mA peak
206 mA nominal max

CRITICAL
L3507
90-OHM
DLP0NS SYM_VER-1
USB_CAMERA_P — BI 18 95
USB_CAMERA_N — BI 18 95
PLACE_NEAR=J3502.2:2.54MM

PLACE_NEAR=J3502.6:2.54MM
L3508 FERR-120-OHM-1.5A 0402-LF
=PP5V_S3_ALSCAMERA — 7
C3552 0.1uF 20% 10V CERM 402

15550367
L3504 FERR-120-OHM-3A 0603
MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
46 6 PP3V3_WLAN
MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
32 PP3V3_WLAN_F
C3522 0.1uF 20% 10V CERM 402 — PLACE_NEAR=J3501.29:2.54MM
C3521 0.1uF 20% 10V CERM 402 — PLACE_NEAR=J3501.29:2.54MM

XW3552 SM
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
PP3V3_WLAN_R

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

CRITICAL
Q3550
DMP2018LFK
DFN2563-6
S, G, D, S, S, D

C3550 0.1UF 10% 16V X5R 402-1
C3551 0.033UF 10% 16V X5R 402
R3550 33K 5% 1/16W MF-LF 402
R3551 10K 5% 1/16W MF-LF 402
=PP3V3_S3_WLAN — 7 32
P3V3WLAN_SS
PM_WLAN_EN_L — IN 74

SYNC_MASTER=J30_MLB
SYNC_DATE=11/11/2013
PAGE TITLE
X19/ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
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CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_TBT_R2D_C_P<0>	C3600 0.1UF	PCIE_TBT_R2D_P<0>	PER_0_P
PCIE_TBT_R2D_C_N<0>	C3601 0.1UF	PCIE_TBT_R2D_N<0>	PER_0_N
PCIE_TBT_R2D_C_P<1>	C3602 0.1UF	PCIE_TBT_R2D_P<1>	PER_1_P
PCIE_TBT_R2D_C_N<1>	C3603 0.1UF	PCIE_TBT_R2D_N<1>	PER_1_N
PCIE_TBT_R2D_C_P<2>	C3604 0.1UF	PCIE_TBT_R2D_P<2>	PER_2_P
PCIE_TBT_R2D_C_N<2>	C3605 0.1UF	PCIE_TBT_R2D_N<2>	PER_2_N
PCIE_TBT_R2D_C_P<3>	C3606 0.1UF	PCIE_TBT_R2D_P<3>	PER_3_P
PCIE_TBT_R2D_C_N<3>	C3607 0.1UF	PCIE_TBT_R2D_N<3>	PER_3_N

TRANSMIT

PET_0_P	C3640 0.1UF	PCIE_TBT_D2R_P<0>	PCIE_TBT_D2R_C_P<0>
PET_0_N	C3641 0.1UF	PCIE_TBT_D2R_N<0>	PCIE_TBT_D2R_C_N<0>
PET_1_P	C3642 0.1UF	PCIE_TBT_D2R_P<1>	PCIE_TBT_D2R_C_P<1>
PET_1_N	C3643 0.1UF	PCIE_TBT_D2R_N<1>	PCIE_TBT_D2R_C_N<1>
PET_2_P	C3644 0.1UF	PCIE_TBT_D2R_P<2>	PCIE_TBT_D2R_C_P<2>
PET_2_N	C3645 0.1UF	PCIE_TBT_D2R_N<2>	PCIE_TBT_D2R_C_N<2>
PET_3_P	C3646 0.1UF	PCIE_TBT_D2R_P<3>	PCIE_TBT_D2R_C_P<3>
PET_3_N	C3647 0.1UF	PCIE_TBT_D2R_N<3>	PCIE_TBT_D2R_C_N<3>

TP_TBT_MONDC0	B21	MONDC0
TP_TBT_MONDC1	A20	MONDC1

DEBUG: For monitoring current/voltage

TP_TBT_MONOBSP	K17	MONOBSP
TP_TBT_MONOBSN	M17	MONOBSN

DEBUG: For monitoring clock

WAKE* F1 TBT_PCIE_WAKE_L — R3651 10K 5% 1/16W MF-LF 402 — =PP3V3_TBT_RTR
PERST* E6 TBT_RESET_L
RSENSE E14 TBT_RSENSE — R3655 1K 1% 1/16W MF-LF 402
RBIAS E16 TBT_RBIAS

MISC

=PP3V3_TBT_RTR

R3690 3.3K, R3691 3.3K, C3690 1UF 6.3V CERM 402, R3692 3.3K, R3623 10K, R3622 10K, R3621 10K, R3693 3.3K — 5% 1/16W MF-LF 402

U3690 M95320-RMB6TG MLP (CRITICAL, OMIT_TABLE)

TBT_SPI_MOSI	D	
TBT_SPI_CLK	C	
TBT_SPI_CS_L	S_L	
TBTROM_WP_L	W_L	
TBTROM_HOLD_L	HOLD_L	
	Q	TBT_SPI_MISO
	VCC	
	VSS	THM PAD

=TBT_CLKREQ_L — TBT_GPIO<1> — TBT_GPIO<2> — TBT_RSVD

CLK REQUEST

PCIE_CLKREQ_0*	P3
PCIE_CLKREQ_1*	N4
PCIE_CLKREQ_2*	M3
PCIE_CLKREQ_3*	L4

EEPROM

TBT_SPI_MOSI	P1
TBT_SPI_MISO	M1
TBT_SPI_CS_L	N2
TBT_SPI_CLK	L2

TP_TBT_THERM_DP (Use B1 GND ball for THERM_DN)	A2
THERM_DP	

TEST PORT

TBT_TEST_EN	E4
TP_TBT_TEST_POINT_0	P5
TP_TBT_TEST_POINT_1	N6
TP_TBT_TEST_POINT_2	M5
TBT_TEST_POINT_3	L6

R3625 0 5% 1/16W MF-LF 402

POWER ON RESET

Not used in host mode.

PCIE_RST_0*	K1	TP_TBT_PCIE_RESET0_L
PCIE_RST_1*	J2	TP_TBT_PCIE_RESET1_L
PCIE_RST_2*	K3	TP_TBT_PCIE_RESET2_L
PCIE_RST_3*	J4	TP_TBT_PCIE_RESET3_L

JTAG

TDI	T3	JTAG_TBT_TDI
TMS	R4	JTAG_TBT_TMS
TCK	R2	JTAG_TBT_TCK
TDO	T1	JTAG_TBT_TDO

CLOCKS

REFCLK_100_IN_P	H17	PCIE_CLK100M_TBT_P
REFCLK_100_IN_N	G16	PCIE_CLK100M_TBT_N
XTAL_25_IN	P17	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	R16	TP_TBT_XTAL25OUT
TMU_CLK_OUT	U2	TBT_TMU_CLK_OUT
TMU_CLK_IN	E2	TBT_TMU_CLK_IN

=PP3V3_TBT_RTR — R3698 10K 5% 1/16W MF-LF 402
R3695 806 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_TBT
R3696 1K 5% 1/16W MF-LF 402
NO STUFF R3699 10K 5% 1/16W MF-LF 402

DISPLAY

SINK PORT 0

DP_TBTSNK0_ML_P<3>	AA4	DPSNK0_ML_LANE_3P
DP_TBTSNK0_ML_N<3>	Y3	DPSNK0_ML_LANE_3N
DP_TBTSNK0_ML_P<2>	AA6	DPSNK0_ML_LANE_2P
DP_TBTSNK0_ML_N<2>	Y5	DPSNK0_ML_LANE_2N
DP_TBTSNK0_ML_P<1>	AA8	DPSNK0_ML_LANE_1P
DP_TBTSNK0_ML_N<1>	Y7	DPSNK0_ML_LANE_1N
DP_TBTSNK0_ML_P<0>	AA10	DPSNK0_ML_LANE_0P
DP_TBTSNK0_ML_N<0>	Y9	DPSNK0_ML_LANE_0N
DP_TBTSNK0_AUXCH_P	V1	DPSNK0_AUX_CHP
DP_TBTSNK0_AUXCH_N	W2	DPSNK0_AUX_CHN
DP_TBTSNK0_HPD	V5	DPSNK0_HOT_PLUG_DET

R3630 100K 5% 1/16W MF-LF 402

SINK PORT 1

DP_TBTSNK1_ML_P<3>	V9	DPSNK1_ML_LANE_3P
DP_TBTSNK1_ML_N<3>	U8	DPSNK1_ML_LANE_3N
DP_TBTSNK1_ML_P<2>	V11	DPSNK1_ML_LANE_2P
DP_TBTSNK1_ML_N<2>	U10	DPSNK1_ML_LANE_2N
DP_TBTSNK1_ML_P<1>	V13	DPSNK1_ML_LANE_1P
DP_TBTSNK1_ML_N<1>	U12	DPSNK1_ML_LANE_1N
DP_TBTSNK1_ML_P<0>	V15	DPSNK1_ML_LANE_0P
DP_TBTSNK1_ML_N<0>	U14	DPSNK1_ML_LANE_0N
DP_TBTSNK1_AUXCH_P	V7	DPSNK1_AUX_CHP
DP_TBTSNK1_AUXCH_N	U6	DPSNK1_AUX_CHN
DP_TBTSNK1_HPD	U4	DPSNK1_HOT_PLUG_DET

R3631 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

DPSRC0_ML_LANE_3P	AA18	TP_DP_TBTSRC_ML_CP<3>
DPSRC0_ML_LANE_3N	Y17	TP_DP_TBTSRC_ML_CN<3>
DPSRC0_ML_LANE_2P	AA16	TP_DP_TBTSRC_ML_CP<2>
DPSRC0_ML_LANE_2N	Y15	TP_DP_TBTSRC_ML_CN<2>
DPSRC0_ML_LANE_1P	AA14	TP_DP_TBTSRC_ML_CP<1>
DPSRC0_ML_LANE_1N	Y13	TP_DP_TBTSRC_ML_CN<1>
DPSRC0_ML_LANE_0P	AA12	TP_DP_TBTSRC_ML_CP<0>
DPSRC0_ML_LANE_0N	Y11	TP_DP_TBTSRC_ML_CN<0>
DPSRC0_AUX_CHP	W16	TP_DP_TBTSRC_AUXCH_CP
DPSRC0_AUX_CHN	U16	TP_DP_TBTSRC_AUXCH_CN
DPSRC0_HOT_PLUG_DET	V3	DP_TBTSRC_HPD

DP_ATEST	Y19	TBT_DP_ATEST
DP_RES_0	Y21	
DP_RES_1	AA20	TBT_DP_RES

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm

R3685 14.0K 1% 1/16W MF-LF 402 — R3632 100K 5% 1/10W MF-LF 402 — C3685 100PF 5% 50V CERM 402 — C3686 0.01UF 10% 16V CERM 402

PORTS

PORT0

TBT_R2D_C_P<0>	A6	PRT0_T29T_P
TBT_R2D_C_N<0>	A4	PRT0_T29T_N
TBT_D2R_P<0>	C4	PRT0_T29R_P
TBT_D2R_N<0>	C2	PRT0_T29R_N
TBT_LSEO<0>	J6	T29_0_LSEO
TBT_LSOE<0>	K5	T29_0_LSOE

PORT1

TBT_R2D_C_P<1>	A10	PRT1_T29T_P
TBT_R2D_C_N<1>	A8	PRT1_T29T_N
TBT_D2R_P<1>	C8	PRT1_T29R_P
TBT_D2R_N<1>	C6	PRT1_T29R_N
TBT_LSEO<1>	G6	T29_1_LSEO
TBT_LSOE<1>	H5	T29_1_LSOE

I2C_TBT_SDA	F3	T29_SDA
I2C_TBT_SCL	F5	T29_SCL

PORT2

PRT2_T29T_P	A14	TBT_R2D_C_P<2>
PRT2_T29T_N	A12	TBT_R2D_C_N<2>
PRT2_T29R_P	C12	TBT_D2R_P<2>
PRT2_T29R_N	C10	TBT_D2R_N<2>
T29_2_LSEO	G4	TBT_LSEO<2>
T29_2_LSOE	H3	TBT_LSOE<2>

PORT3

PRT3_T29T_P	A18	TBT_R2D_C_P<3>
PRT3_T29T_N	A16	TBT_R2D_C_N<3>
PRT3_T29R_P	C16	TBT_D2R_P<3>
PRT3_T29R_N	C14	TBT_D2R_N<3>
T29_3_LSEO	G2	TBT_LSEO<3>
T29_3_LSOE	H1	TBT_LSOE<3>

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C3620 0.1uF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C3621 0.1uF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C3622 0.1uF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C3623 0.1uF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C3624 0.1uF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C3625 0.1uF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C3626 0.1uF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C3627 0.1uF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C3628 0.1uF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C3629 0.1uF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C3630 0.1uF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C3631 0.1uF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C3632 0.1uF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C3633 0.1uF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C3634 0.1uF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C3635 0.1uF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C3636 0.1uF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C3637 0.1uF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C3638 0.1uF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C3639 0.1uF	DP_TBTSNK1_AUXCH_N

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2011

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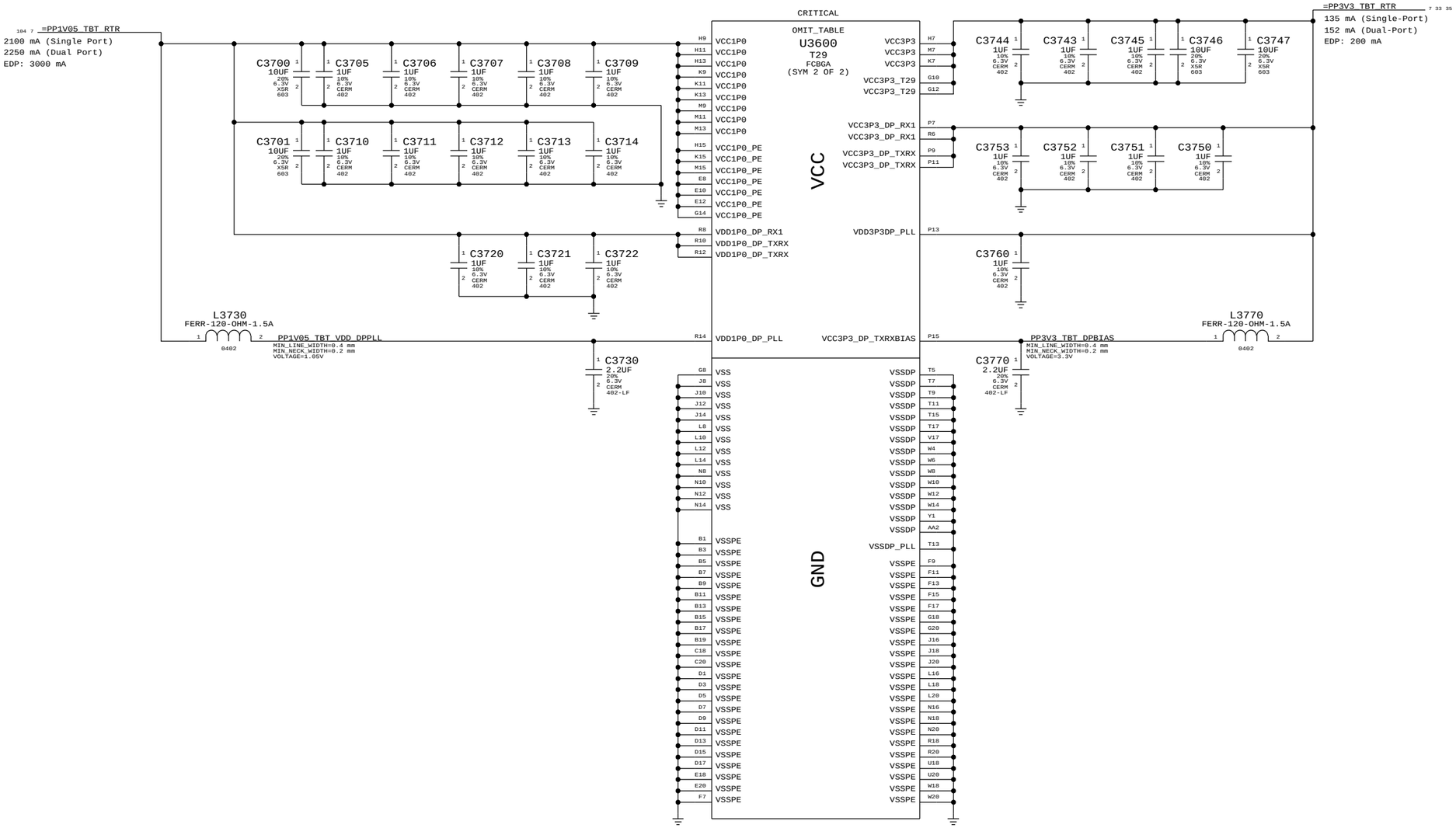

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2011

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_S0_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_S0_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Thunderbolt 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_TBTBST
8-13V Input
Changes required for 2S.

CRITICAL TBTBST:Y Q3880 SI8409DB 8GA

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 25V XSR 402
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L
TBTBST:Y Q3805 SSM3K15FV SOD-VESM-HF
TBT_A_HV_EN

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>
TBTBST:Y C3890 10UF 10% 25V XSR 805
TBTBST:Y C3891 10UF 10% 25V XSR 805

CRITICAL TBTBST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL TBTBST:Y U3890 LT3957 QFN

25	EN/UVLO	
28	INTVCC	
30	VC	
33	RT	
32	SS	
34	SYNC	
27	VIN	
8,9,20,21,30	SW	
6	SNS1	
3	SNS2	
31	FBX	
4,23,24,37	SGND	
12,13,14,15,16,17	GND	

TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS_RC
TBTBST_VSNS
TBTBST_FBX
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

TBTBST:Y R3889 0 5% 1/16W MF-LF 402
TBTBST:Y R3890 49.9K 1% 1/16W MF-LF 402
XW3895 SM
PLACE_NEAR=C3895.1:2 mm

CRITICAL TBTBST:Y D3895 POWERDI-123 DFLS230L

TBTBST:Y C3892 4.7UF 10% 10V XSR 805
TBTBST:Y C3887 47PF 5% 50V CERM 402
TBTBST:Y R3893 10K 1% 1/16W MF-LF 402
TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3893 0.0033UF 10% 50V CERM 402
TBTBST:Y R3894 41.2K 1% 1/16W MF-LF 402
TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

NC
NO STUFF C3889 100PF 5% 50V CERM 402
TBTBST:Y C3888 22PF 5% 50V CERM 402
TBTBST:Y R3895 137K 1% 1/16W MF-LF 402 <Ra>
TBTBST:Y R3896 15.8K 1% 1/16W MF-LF 402 <Rb>

TBTBST:Y C3895 4.7UF 10% 50V X7R-CERM 1206
TBTBST:Y C3897 4.7UF 10% 50V X7R-CERM 1206
TBTBST:Y C3896 4.7UF 10% 50V X7R-CERM 1206
TBTBST:Y C3898 4.7UF 10% 50V X7R-CERM 1206
TBTBST:Y C3899 0.001UF 10% 50V X7R 402

=PP15V_TBT_REG
Vout = 15.47V
Max Current = 1A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Vout = 1.6V * (1 + Ra / Rb)

SGND shorted to GND inside package, no XW necessary.

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K 5% 1/16W MF-LF 402
TBTBST:Y R3888 330K 5% 1/16W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
C3800 0.1UF 10% 25V XSR 402
CRITICAL U3800 SLG4AP016V TDFN
=PP3V3_TBT_RTR
R3807 100K 5% 1/16W MF-LF 402
PP1V05_TBT
SENSE 0.7V
DLY
RESET*
DLY = 60 ms +/- 20%

Platform (PCIe) Reset
=TBT_RESET_L
R3803 10K 5% 1/16W MF-LF 402
Open-Drain GPIO
TBT_SW_RESET_L
TBT_PWR_EN
TBT_CLKREQ_L
Pull-ups provided by SB page.

MR*
EN
OUT (OD)
IN
GND
THRM PAD
TBT_RESET_L
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V Thunderbolt Switch

=PP3V3_S0_P3V3TBTFET
U3810 TPS22924 CSP
VIN VOUT ON GND CRITICAL
=PP3V3_TBT_FET
Max Current = 2A (85C)
C3810 1UF 10% 6.3V CERM 402
R3816 0 5% 1/16W MF-LF 402
TBT_PWR_EN_RC

U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

1.05V Thunderbolt Switch

=PP1V05_S0_P1V05TBTFET
U3815 TPS22920 CSP
VIN VOUT ON GND CRITICAL
=PP1V05_TBT_FET
Max Current = 4A (85C)
C3815 1UF 10% 6.3V CERM 402
NO STUFF C3816 1UF 10% 6.3V CERM 402

U3815	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

72 36 24 7 =PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
36 =PP3V3R1V8_ENET_LR_OUT

CRITICAL L3900 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_XTALVDDH — C3900 0.1UF 10% 16V X7R-CERM 402
CRITICAL L3905 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_BIASVDDH — C3905 0.1UF 10% 16V X7R-CERM 402
CRITICAL L3910 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_AVDDH — R3910 4.7K 5% 1/16W MF-LF 402 — C3910 0.1UF 10% 16V X7R-CERM 402 — C3911 0.1UF 10% 16V X7R-CERM 402

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

7 =PP3V3_S0_ENETPHY
R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402
R3943 0 5% 1/16W MF-LF 402

96 16 OUT PCIE_ENET_D2R_N
96 16 OUT PCIE_ENET_D2R_P
96 16 IN PCIE_ENET_R2D_C_P
96 16 IN PCIE_ENET_R2D_C_N
24 OUT =ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPD)
96 PCIE_ENET_D2R_C_N — 27 PCIE_TXD_N
96 PCIE_ENET_D2R_C_P — 28 PCIE_TXD_P
96 PCIE_ENET_R2D_P — 33 PCIE_RXD_P
96 PCIE_ENET_R2D_N — 34 PCIE_RXD_N
96 16 IN PCIE_CLK100M_ENET_P — 31 PCIE_REFCLK_P
96 16 IN PCIE_CLK100M_ENET_N — 30 PCIE_REFCLK_N
97 30 IN ENET_RESET_L — 11 PERST* (IPD)
16 OUT ENET_CLKREQ_L — 12 CLKREQ* (OD)
ENET_WAKE_R_L — 3 WAKE* (OD)
30 24 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)
BCM57765_SMB_CLK — 6 SMB_CLK
BCM57765_SMB_DATA — 10 SMB_DATA (IPD)
36 BCM57765_SCLK — 66 SCLK_SPD1000LED*
36 BCM57765_MISO — 64 SI/EEDATA
36 BCM57765_MOSI — 65 SO_LINKLED*
36 BCM57765_CS_L — 63 CS*/EECLK
(IPU)
TP_BCM57765_SPD100LED_L — 2 SPD100LED*/SERIAL_DO (OD)
TP_BCM57765_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
24 IN SYSCLK_CLK25M_ENET — 18 XTALI
NC — 19 XTALO
BCM57765_RDAC — 38 RDAC
THRM_PAD — 69

R3965 1.24K 1% 1/16W MF-LF 402

U3900
BCM57765B0
QFN-8X8

AVDDH 42 48 37 — BIASVDDH — XTALVDDH 17 — VDDO 7 20 50 62 — SR_VDD 14 — SR_VDDP 15 — SR_LX 16 — SR_VFB 13 — AVDDL 39 45 51 — PCIE_PLLVDDL 29 32 — GPHY_PLLVDDL 36 — VDDC 35 61

ENET_SR_LX 72
ENET_SR_VFB 72

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 7
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A SM — PP1V2_ENET_PHY_AVDDL — C3921 0.1UF 10% 16V X7R-CERM 402 — C3920 4.7UF 10% 6.3V X5R-CERM 603
CRITICAL L3925 FERR-600-OHM-0.5A SM — PP1V2_ENET_PHY_PCIEPLL — C3926 0.1UF 10% 16V X7R-CERM 402 — C3925 4.7UF 10% 6.3V X5R-CERM 603
CRITICAL L3930 FERR-600-OHM-0.5A SM — PP1V2_ENET_PHY_GPHYPLL — C3931 0.1UF 10% 16V X7R-CERM 402 — C3930 4.7UF 10% 6.3V X5R-CERM 603

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3936 0.1UF 10% 16V X7R-CERM 402
CRITICAL C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT 36
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

TRD0_P 40 — ENET_MDI_P<0> (IO) 37 97
TRD0_N 41 — ENET_MDI_N<0> (IO) 37 97
TRD1_P 44 — ENET_MDI_P<1> (IO) 37 97
TRD1_N 43 — ENET_MDI_N<1> (IO) 37 97
TRD2_P 46 — ENET_MDI_P<2> (IO) 37 97
TRD2_N 47 — ENET_MDI_N<2> (IO) 37 97
TRD3_P 50 — ENET_MDI_P<3> (IO) 37 97
TRD3_N 49 — ENET_MDI_N<3> (IO) 37 97

(IPD) GPIO_0/CR_ACT_LED* 5 — NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 — ENET_MEDIA_SENSE OUT 24

NOTE: "IPx" == Programmable pull-up/down
(IPx) SD_DETECT* 1 — SDCONN_DETECT_L IN 30
SD_DETECT can only be used active low due to errata.
(IPU) CR_CMD 26 — SDCONN_CMD IN 30 97
CR_CLK 21 — SDCONN_CLK OUT 30 97
(IPU) CR_DATA0 25 — SDCONN_DATA<0> IO 30 97
CR_DATA1 24 — SDCONN_DATA<1> IO 30 97
CR_DATA2 23 — SDCONN_DATA<2> IO 30 97
CR_DATA3 22 — SDCONN_DATA<3> IO 30 97
CR_DATA4 52 — SDCONN_DATA<4> IO 30 97
CR_DATA5 53 — SDCONN_DATA<5> IO 30 97
CR_DATA6 54 — SDCONN_DATA<6> IO 30 97
CR_DATA7 55 — SDCONN_DATA<7> IO 30 97

(IPU) MS_INS* 59 — TP_CE_L_MS_INS_L
CR_LED*/CR_BUS_PWR 60 — ENET_CR_PWREN OUT 30
CR_WP* 57 — SDCONN_WP IN 30
SR_DISABLE 68 — BDM57765_SR_DISABLE

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K 5% 1/16W MF-LF 402

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

72 36 24 7 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X7R-CERM 402
U3990 AT45DB011D SOIC-BS1
VCC 8 — SCK 2 — SI 1 — SO 8 — CS* 4 — WP* 5 — RESET* 3 — GND 7 — OMIT
36 BCM57765_SCLK — BCM57765_MOSI 36
36 BCM57765_CS_L — BCM57765_MISO 36
NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

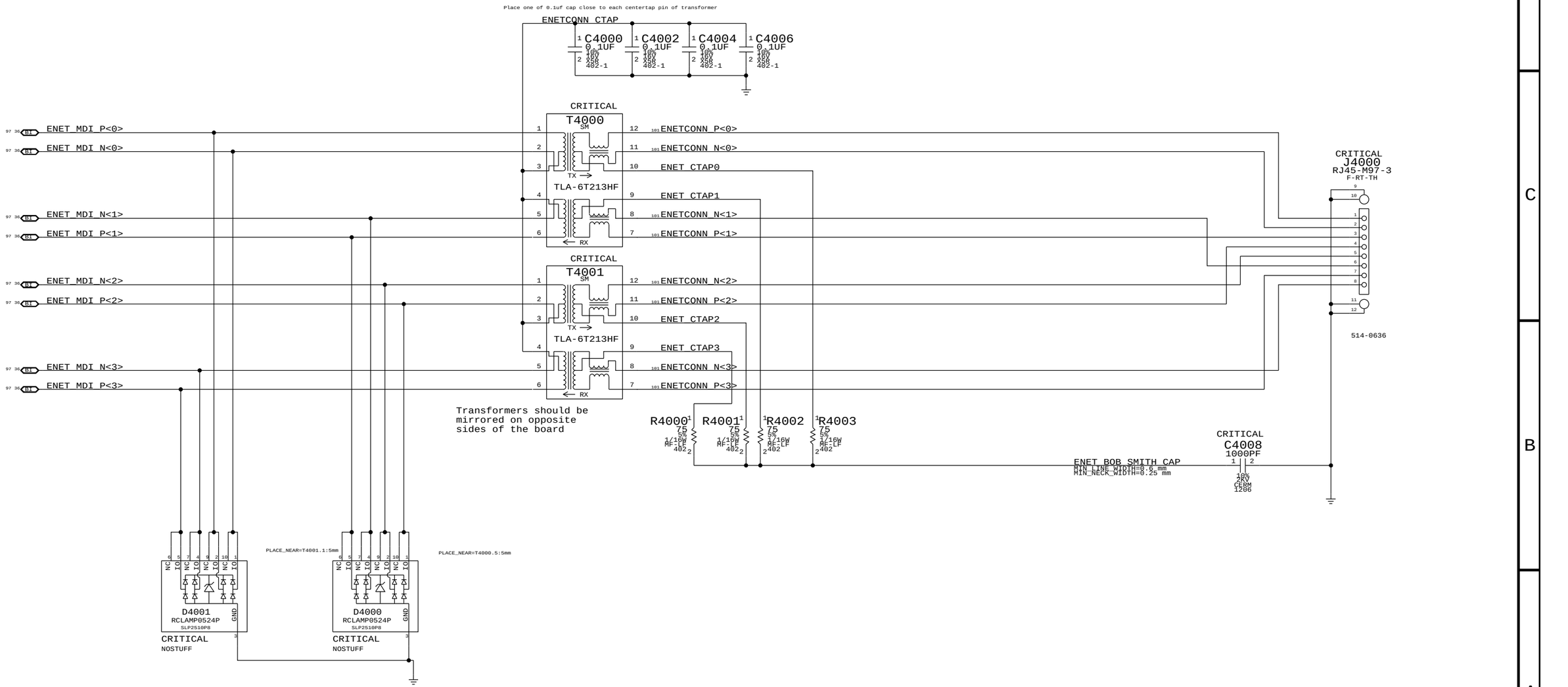
SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 39 OF 132
SHEET 36 OF 105

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
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PAGE 40 OF 132
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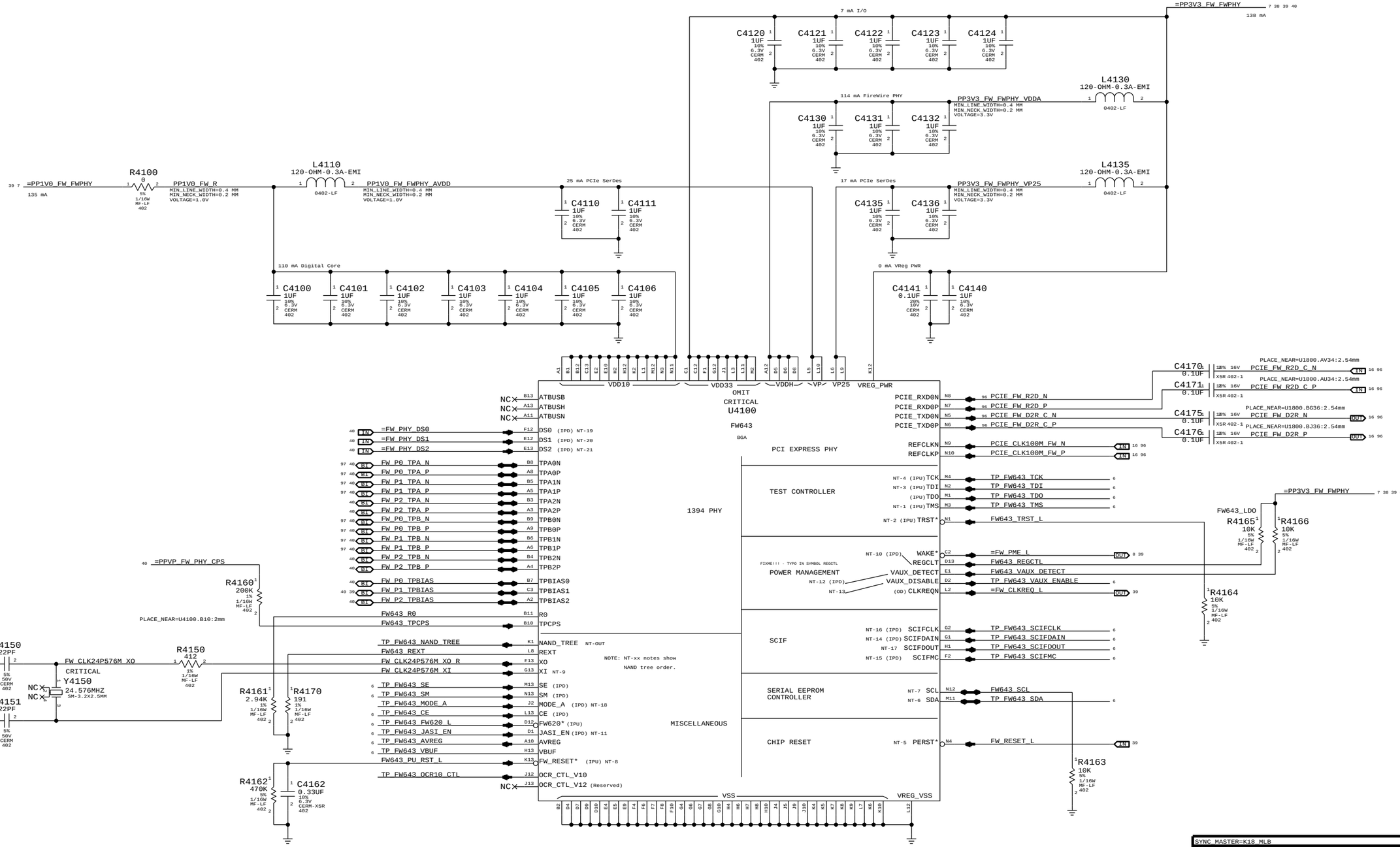

SYNC MASTER=K18_MLB SYNC DATE=04/27/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 41 OF 132

SHEET 38 OF 105

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

=PPBUS_S5_FWPWRSW

Q4262 provides for fast-off of Q4260 in S0 (Late-VG detection)

R4262 10K 5% 1/16W MF-LF 402

R4263 10 5% 1/16W MF-LF 402

FWPORT_FASTOFF_L_DIV

FWPORT_FASTOFF_L

CRITICAL Q4262 BSS8402DW SOT-363 (SYM-VER2)

R4260 300K 5% 1/16W MF-LF 402

FWPORT_PWREN_L_DIV

C4260 0.1UF 10% 25V X5R 402

CRITICAL Q4260 FDC638P_G SM

PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL F4260 1.1A-24V MINISMDC110H24

PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL D4260 SBR3U30P1 PWRDI123

=PPBUS_FW_FET

=PP3V3_S0_FWLATEVG

CRITICAL Q4262 BSS8402DW SOT-363 (SYM-VER1)

R4261 470K 5% 1/16W MF-LF 402

FWPORT_PWREN_L

CRITICAL Q4261 SSM3K15FV SOD-VESM-HF

NO STUFF C4261 0.1UF 10% 25V X5R 402

IN FWPORT_PWR_EN

Supervisor & CLKREQ# Isolation

=PP3V3_S0_FWPWRCTL

=PP3V3_FW_FWPHY

C4290 0.1UF 10% 25V X5R 402

CRITICAL U4290 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
GND
THRM PAD

R4290 100K 5% 1/16W MF-LF 402

=PP1V0_FW_FWPHY

IN =FW_RESET_L

R4283 10K 5% 1/16W MF-LF 402

FW_RESET_R_L

FW_RESET_L

DLY = 60 ms +/- 20%

IN FW_PWR_EN

OUT FW_CLKREQ_L

=FW_CLKREQ_L

FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

Pull-up provided by another page.

FireWire Port 5K Pull-Down Detect

=PP1V05_S0_FWPWRCTL

R4275 1K 5% 1/16W MF-LF 402

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

FW_PWR_EN_L

IN FW_PWR_EN

CRITICAL Q4275 DMB53D0UV SOT-563

R4270 330K 5% 1/16W MF-LF 402

R4271 56K 5% 1/16W MF-LF 402

FW_5KPD_DET_RC

FW_5KPD_DET_L
MAKE_BASE=TRUE

CRITICAL Q4275 DMB53D0UV SOT-563

C4270 0.1UF 10% 16V X5R 402

CRITICAL Q4270 BC847CDXV6TXG SOT563

FWDET_MIRROR

CRITICAL Q4270 BC847CDXV6TXG SOT563

FW_P1_TPBIAS_R

FWDET_EMIT

R4272 1K 5% 1/16W MF-LF 402
PLACE_NEAR=C4360.1:2 mm

R4273 12K 5% 1/16W MF-LF 402

IN FW_P1_TPBIAS

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

=PP3V3_FW_FWPHY

R4277 10K 5% 1/16W MF-LF 402

R4276 100K 5% 1/16W MF-LF 402

FW_WAKE

NO STUFF C4276 0.1UF 10% 16V X5R 402

CRITICAL Q4276 DMB53D0UV SOT-563

IN =FW_PME_L

FW643_WAKE_L
MAKE_BASE=TRUE

CRITICAL Q4276 DMB53D0UV SOT-563

Dual-purpose output:

1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

FW_PME_L OUT

Pull-up provided on another page.

3.3V FW Switch

=PP3V3_FW_P3V3FWFET

U4201 TPS22924 CSP
VIN
VOUT
CRITICAL
ON
GND

C4201 1UF 10% 6.3V CERM 402

=PP3V3_FW_FET

Max Current = 1.7A (85C)

U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch

=PP1V05_FW_P1V0FWFET

U4202 TPS22924 CSP
VIN
VOUT
CRITICAL
ON
GND

C4202 1UF 10% 6.3V CERM 402

PP1V05_FW_FET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

R4202 0.549 1% 1/16W MF 402

LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

=PP1V0_FW_FET_R

SYNC_MASTER=K91_MLB SYNC_DATE=06/17/2011

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 42 OF 132
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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

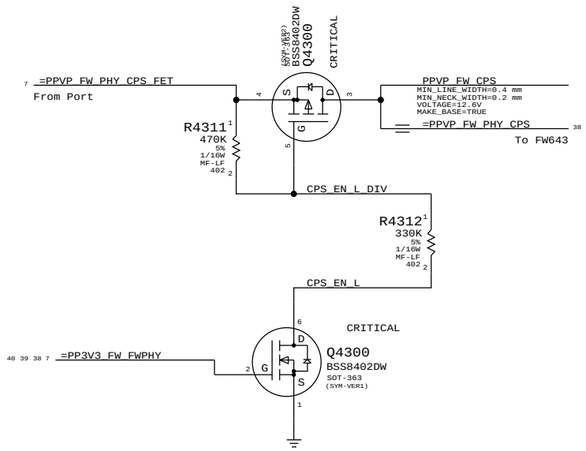
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

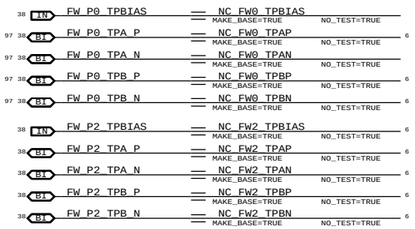
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



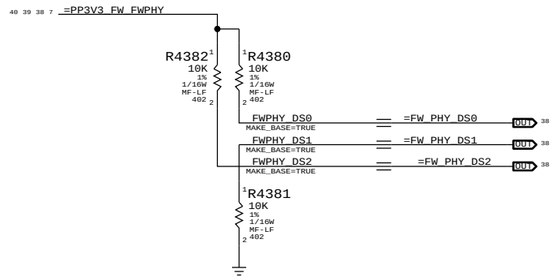
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



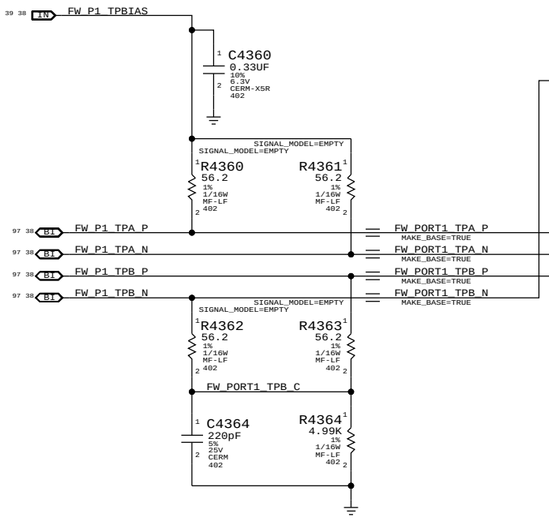
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

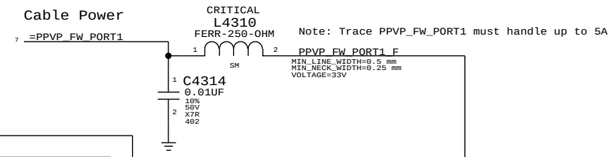


Termination

Place close to FireWire PHY

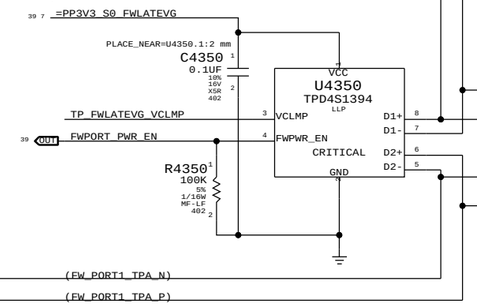


Cable Power



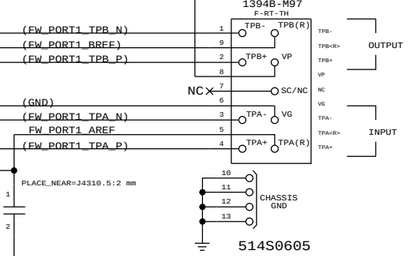
Note: Trace PPVP_FW_PORT1 must handle up to 5A

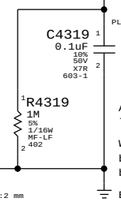
"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL





AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF	SYNC_DATE=06/10/2010
PAGE TITLE	FireWire Connector
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
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ODD Power Control

Note: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

=PP5V_S3_ODD
Q4590 DMP2018LFK DFN2563-6 CRITICAL
PP5V_SW_ODD
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.4MM VOLTAGE=5V
R4596 100K 5% 1/16W MF-LF 402
C4595 0.068UF 10% 10V CERM 402
R4595 100K 5% 1/16W MF-LF 402
C4596 0.01UF 10% 16V CERM 402
ODD_PWR_EN_LS5V_L
ODD_PWR_SS
=PP3V3_S0_ODD
R4597 100K 5% 1/16W MF-LF 402
Q4596 SSM6N37FEAPE SOT563
ODD_PWR_EN
Q4596 SSM6N37FEAPE SOT563
IN ODD_PWR_EN_L

SATA ODD Connector

J4500 54722-0164 F-ST-SM CRITICAL 516S0616

SATA_ODD_R2D_P → C4521 0.01UF → SATA_ODD_R2D_C_P (IN)
SATA_ODD_R2D_N → C4520 0.01UF → SATA_ODD_R2D_C_N (IN)
SATA_ODD_D2R_C_N → C4526 0.01UF → SATA_ODD_D2R_N (OUT)
SATA_ODD_D2R_C_P → C4525 0.01UF → SATA_ODD_D2R_P (OUT)

=PP3V3_S0_ODD
R4590 33K 5% 1/16W MF-LF 402
OUT SMC_ODD_DETECT

Note: Indicates disc presence.

SATA OOB Comparator

Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD

=PP3V3_S0_SMC
=PP1V5_S0_RDRVR
R4581 100K 5% 1/16W MF-LF 402
R4583 49.9K 1% 1/16W MF-LF 402
C4580 0.1UF 20% 10V CERM 402
R4585 1K 5% 1/16W MF-LF 402
SSD_OOB1V0REF
U4580 LMV331 SC70-5
R4586 0 5% 1/16W MF-LF 402 → SMC_SSD_OOBD2R_R_L (OUT)
IN SSD_OOBD2R_FTL_L
R4582 3.3K 5% 1/16W MF-LF 402
SSD_OOBD2R_R_L
R4584 100K 5% 1/16W MF-LF 402
C4584 0.1UF 20% 10V CERM 402

SATA HDD Connector (Gen3)

PP5V_S0_HDD_FLT
L4500 FERR-70-OHM-4A 0603 CRITICAL PLACE_NEAR=J4501.9:3MM
PP5V_S0_HDD_R
CRITICAL R4599 0.001 1% 1W MF-1 0612
=PP5V_S0_HDD
ISNS_HDD_P (OUT 101 103)
ISNS_HDD_N (OUT 101 103)
=PP3V3_S0_HDD
C4501 0.1UF 20% 10V CERM 402 PLACE_NEAR=L4500.1:2MM
C4502 0.1UF 20% 10V CERM 402 PLACE_NEAR=L4500.2:2MM
R4538 100K 5% 1/16W MF-LF 402
C4537 100UF 20% 10V X5R-CERM 1206 PLACE_NEAR=J4501.9:10MM
NOSTUFF C4538 100UF 20% 10V X5R-CERM 1206 PLACE_NEAR=J4501.10:10MM

SSD_OOBR2D_L → R4537 453 1% 1/10W MF-LF 402 → SMC_SSD_OOBR2D_L (IN 46)
SSD_OOBD2R_L → L4539 FERR-220-OHM 0402 → SSD_OOBD2R_FTL_L (OUT 41)
SYS_LED_ANODE_R → R4531 4.7 5% 1/10W MF-LF 402 → SYS_LED_ANODE (IN 46)
C4531 0.001UF 10% 50V CERM 402
IR_RX_OUT (OUT 44)

=PP5V_S3_IR
R4532 0 5% 1/16W MF-LF 402
PP5V_S3_IR_R
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
C4532 0.1UF 10% 10V X7R-CERM 402
J4501 54722-0224 F-ST-SM 516S0687 CRITICAL
GND_VOID

D2R Passive DeEmphasis
VALUE: 4.5 DB

SATA_HDD_D2R_C_P → R4536 68.1 → C4536 5.0PF 0201 → SATA_HDD_D2R_RC_P → C4516 0.01UF → SATA_HDD_D2R_RDRIN_P
SATA_HDD_D2R_C_N → C4535 5.0PF 0201 → SATA_HDD_D2R_RC_N → C4515 0.01UF → SATA_HDD_D2R_RDRIN_N
R4535 68.1

R2D Passive DeEmphasis
VALUE: 3.0 DB

SATA_HDD_R2D_N → R4534 41.2 → C4534 15PF → SATA_HDD_R2D_RC_N → C4511 0.01UF → SATA_HDD_R2D_RDROUT_N
SATA_HDD_R2D_P → C4533 15PF → SATA_HDD_R2D_RC_P → C4510 0.01UF → SATA_HDD_R2D_RDROUT_P
R4533 41.2

SATA Redriver

Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

=PP1V5_S0_RDRVR
R4510 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R4511 0 5% 1/16W MF-LF 402
R4512 3.74K 1% 1/16W MF-LF 402
R4513 4.7K 5% 1/16W MF-LF 402 NO STUFF
R4515 4.7K 5% 1/16W MF-LF 402
SATARDRVR_I2C_ADDR0
SATARDRVR_I2C_ADDR1

C4514 0.1UF 20% 10V CERM 402 PLACE_NEAR=U4510.16:2MM
C4519 0.01UF 20% 16V CERM 402 PLACE_NEAR=U4510.6:2MM

C4518 & C4517 Placement Note:
It is critical that these two should be near to U1800 pin AM1 and AM3.

U4510 PS8521A TQFN 338S0907 CRITICAL

A_INP	A_OUTP	SATA_HDD_D2R_RDROUT_P → C4518 → SATA_HDD_D2R_P (OUT)	PLACE_NEAR=U1800.AM1:5MM GND_VOID=TRUE
A_INN	A_OUTN	SATA_HDD_D2R_RDROUT_N → C4517 → SATA_HDD_D2R_N (OUT)	PLACE_NEAR=U1800.AM3:5MM GND_VOID=TRUE
B_OUTN	B_INN	SATA_HDD_R2D_RDRIN_N → C4513 → SATA_HDD_R2D_C_N (IN)	PLACE_NEAR=U4510.12:5MM GND_VOID=TRUE
B_OUTP	B_INP	SATA_HDD_R2D_RDRIN_P → C4512 → SATA_HDD_R2D_C_P (IN)	PLACE_NEAR=U4510.11:5MM GND_VOID=TRUE
EN	REXT	SATARDRVR_REXT	
B_PRE0/I2C_ADDR0	A_PRE1/SCL_CTL	=SATARDRVR_I2C_SCL (IN 48)	
APRE0/I2C_ADDR1	B_PRE1/SDA_CTL	=SATARDRVR_I2C_SDA (BI 48)	
I2C_EN*		SATARDRVR_I2C_EN_L	
TEST		SATARDRVR_TEST	
GND THRM PAD			

SATARDRVR_EN (IN 23 16)
SATARDRVR_I2C_ADDR0 (IN 41)
SATARDRVR_I2C_ADDR1 (IN 41)

SYNC_MASTER=J31_YONAS SYNC_DATE=11/17/2011
PAGE TITLE: SATA Redriver/Conn, IR, SIL
Apple Inc.
DRAWING NUMBER 051-9585 SIZE D
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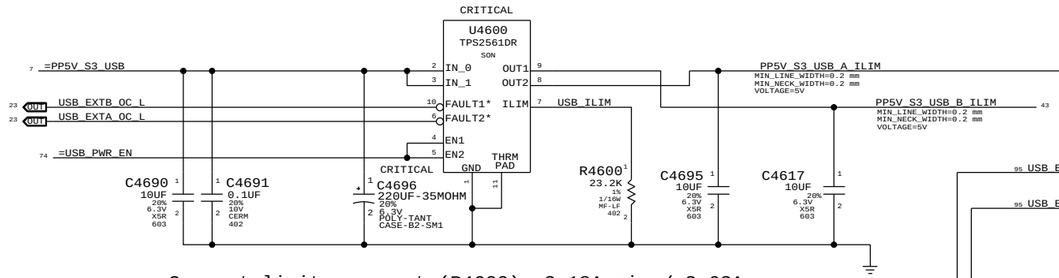
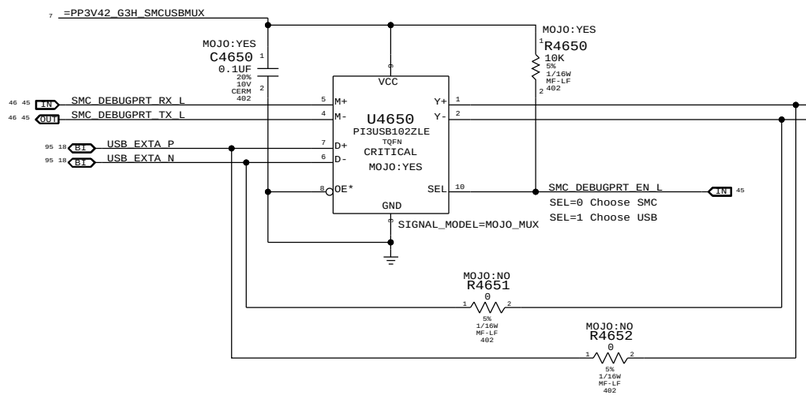
USB Port Power Switch

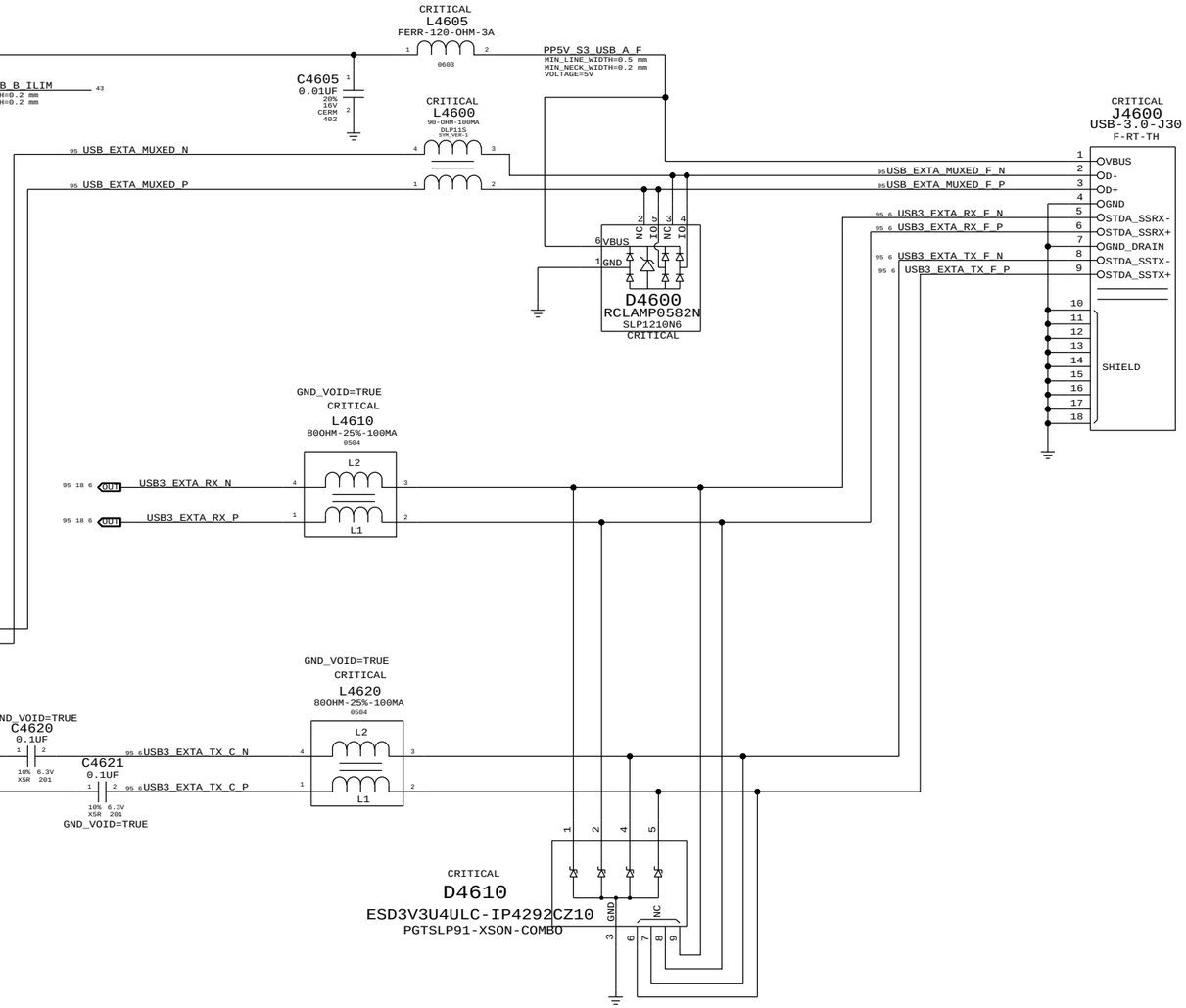


Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux



USB Port A (Front Port)



SYNC_MASTER=J31_LINDA SYNC_DATE=09/21/2011

PAGE TITLE

External A USB3 Connector

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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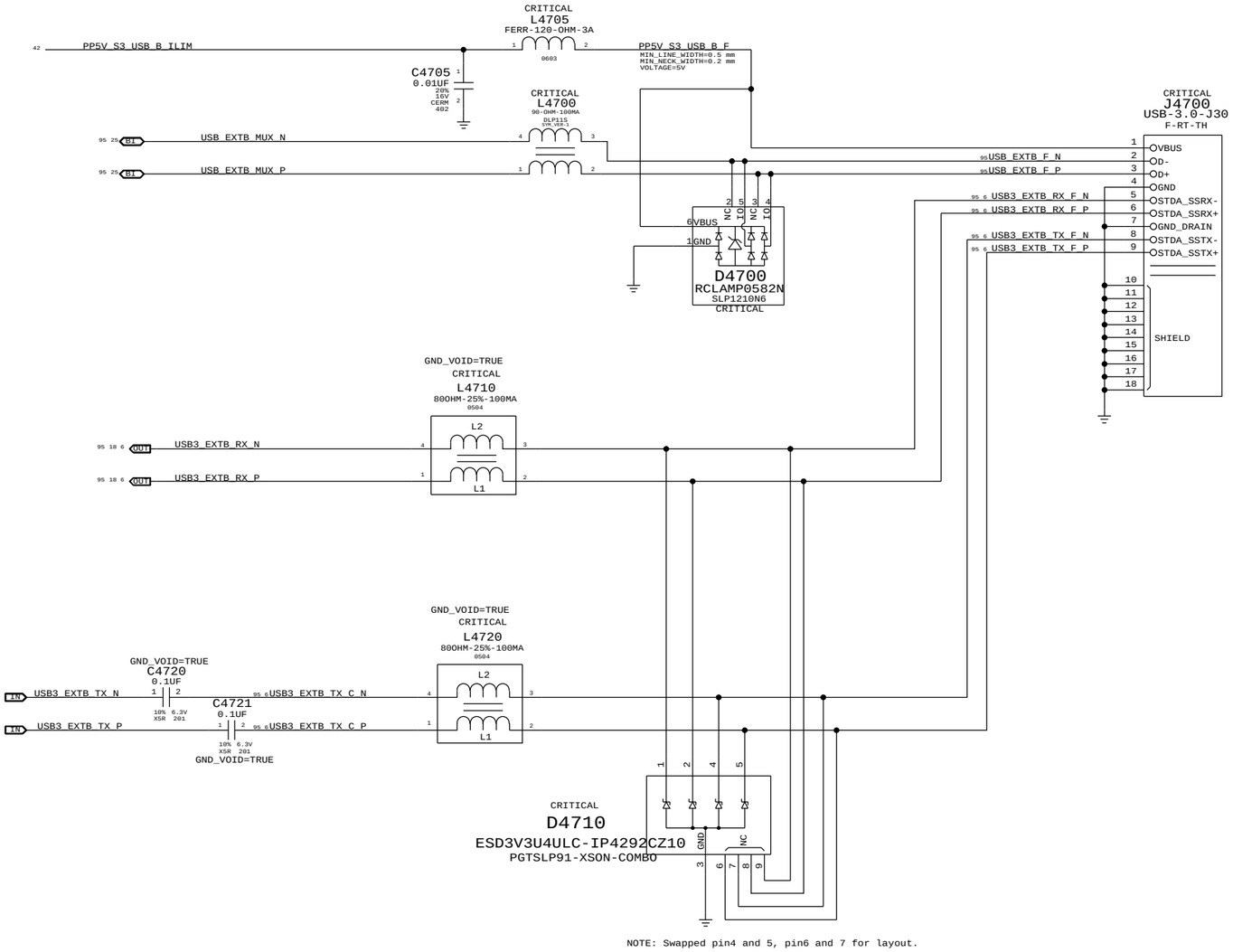
USB Port B (Back Port)



NOTE: Swapped pin4 and 5, pin6 and 7 for layout.

SYNC_MASTER=J30_MLB	SYNC_DATE=08/04/2011
PAGE TITLE: External B USB3 Connector	
Apple Inc.	DRAWING NUMBER: 051-9585 SIZE: D
	REVISION: 3.0.0
	BRANCH:
	PAGE: 47 OF 132
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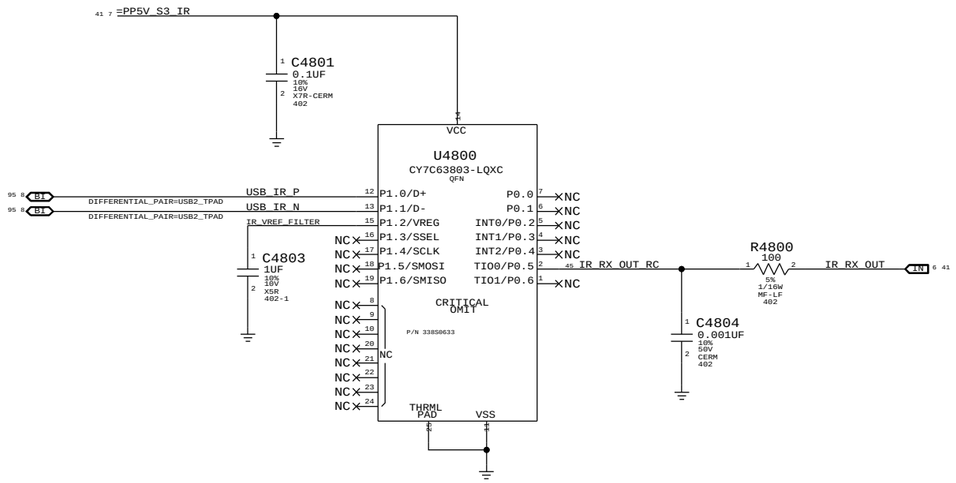
IR SUPPORT



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

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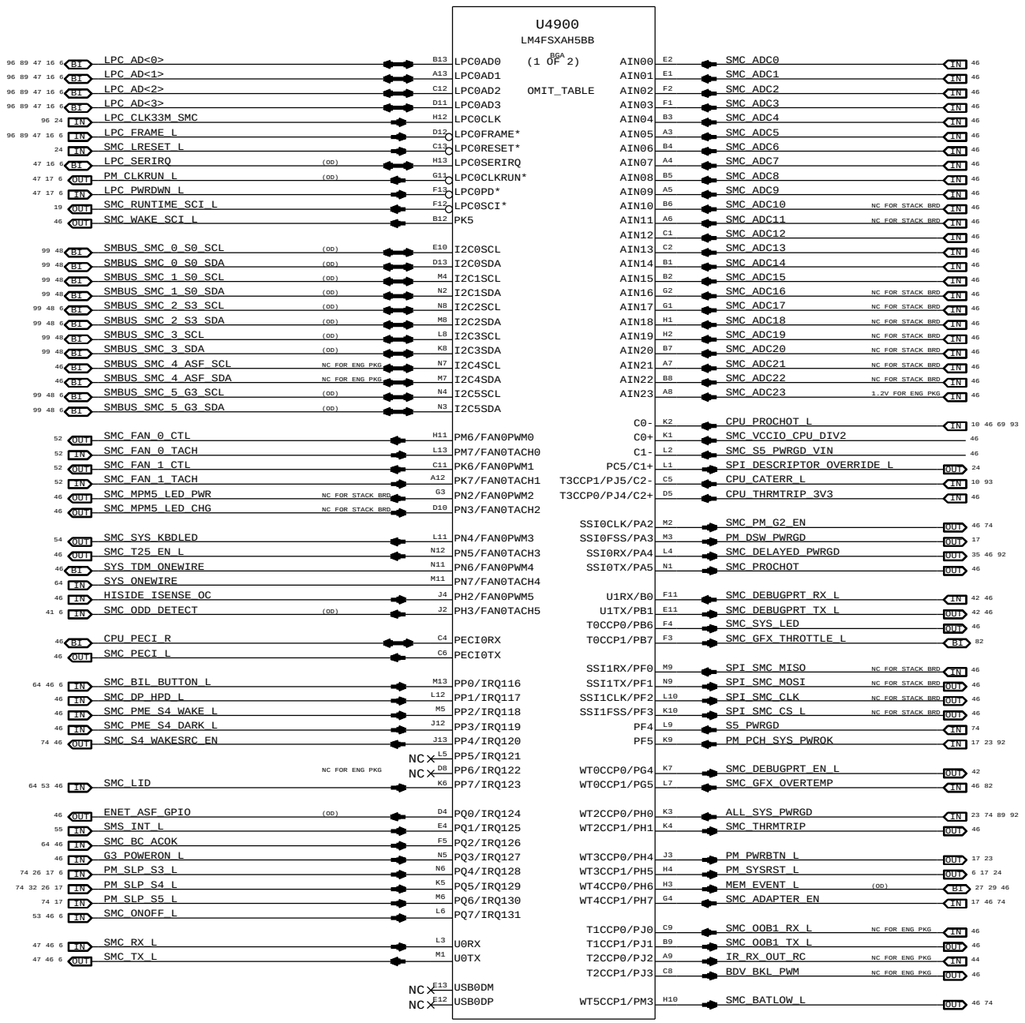
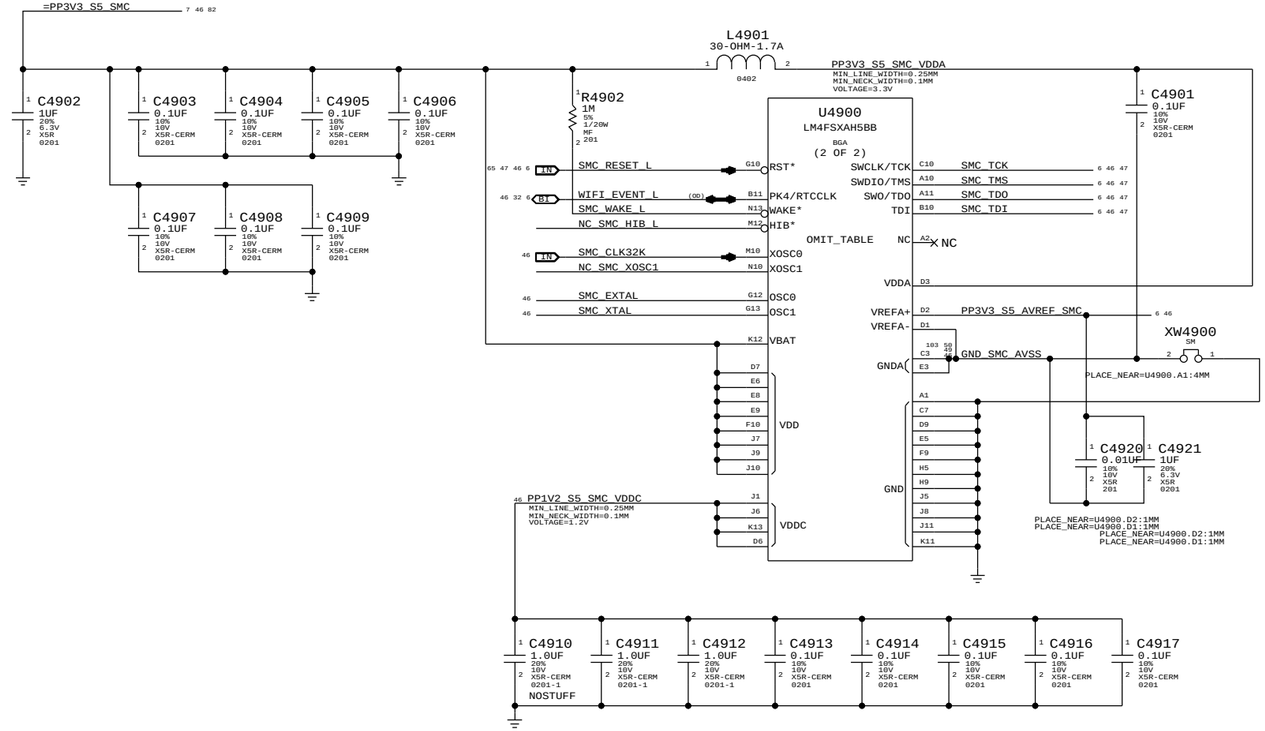


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SYNC_MASTER=J31_YONAS SYNC_DATE=12/19/2013

PAGE TITLE
SMC

Apple Inc.

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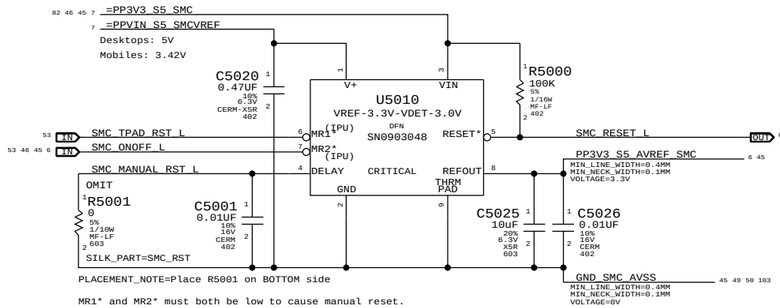
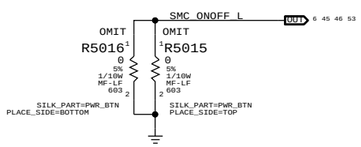
SMC Reset "Button", Supervisor & AVREF Supply



PLACEMENT_NOTE=Place R5001 on BOTTOM side

MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

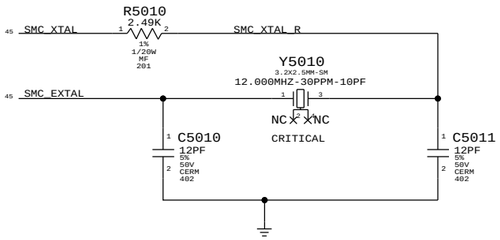
Debug Power "Buttons"



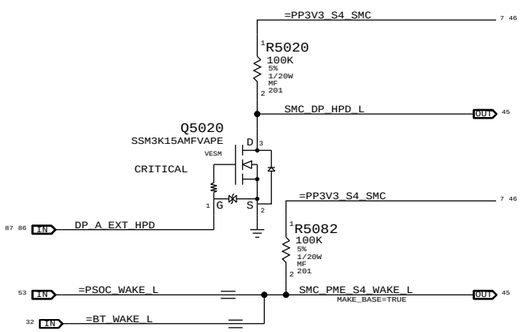
Note:
ADC10 and ADC11 are
share with comparators
on Stack Board.

SMC Crystal Circuit

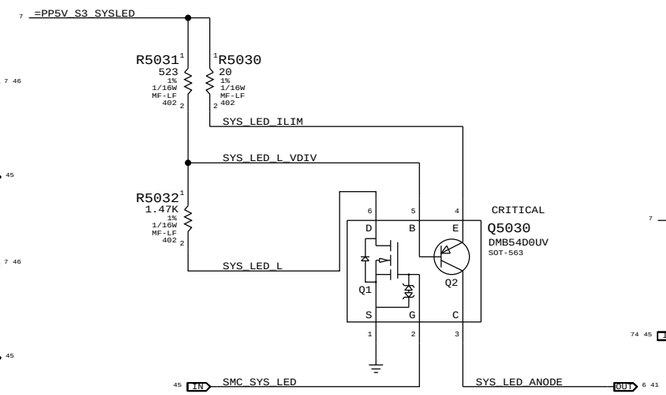
SMC USB Clock require 12 MHz.



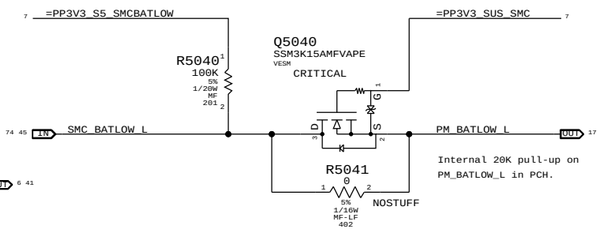
S4 HPD SMC Wake Source



System (Sleep) LED Circuit



BATLOW# Isolation



Internal 20K pull-up on
PM_BATLOW_L in PCH.

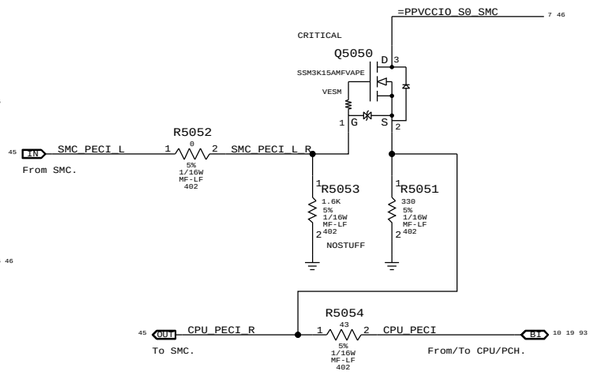
SMC Reset Signals

SMC_ADC0	SMC_CPU_VSENSE	49	
SMC_ADC1	SMC_CPU_ISENSE	50	
SMC_ADC2	SMC_GPU_HI_ISENSE	50	
SMC_ADC3	SMC_DCIN_VSENSE	49	
SMC_ADC4	SMC_DCIN_ISENSE	50	
SMC_ADC5	SMC_PBUS_VSENSE	49	
SMC_ADC6	SMC_HDD_ISENSE	103	
SMC_ADC7	SMC_BMON_ISENSE	50	
SMC_ADC8	SMC_CPU_HI_ISENSE	50	
SMC_ADC9	SMC_OTHER_HI_ISENSE	50	
SMC_ADC10	SMC_MEM_ISENSE	49	
SMC_ADC11	SMC_CPUVCCIO_ISENSE	49	
SMC_ADC12	SMC_AXG_VSENSE	49	
SMC_ADC13	SMC_CPUVCCSA_ISENSE	49	
SMC_ADC14	SMC_GPU_VSENSE	49	
SMC_ADC15	SMC_GPU_ISENSE	49	
SMC_ADC16	SMC_GPU_FB_VSENSE	103	
SMC_ADC17	SMC_CPUVCCSA_VSENSE	49	
SMC_ADC18	SMC_AXG_ISENSE	50	
SMC_ADC19	SMC_GPU_FB_ISENSE	103	
SMC_ADC20	SMC_GPU_1V05_ISENSE	103	
SMC_ADC21	SMC_PCH_ISENSE	103	
SMC_ADC22	SMC_AIRPORT_ISENSE	103	
SMC_ADC23	SMC_CPUMEM_ISENSE_R		
ENET_ASF_GPIO	NC_ENET_ASF_GPIO		
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR		
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG		
SMC_SCI_L	SMC_WAKE_SCI_L	45	
SMC_T25_EN_L	NC_SMC_T25_EN_L		
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE		
SMC_OOB1_RX_L	SMC_SSD_OOBD2R_L	41	
SMC_OOB1_TX_L	SMC_SSD_OOBR2D_L	41	
=CHGR_ACOK	SMC_BC_ACOK	45 46 64	
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC		
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL		
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA		
BDV_BKL_PWM	NC_BDV_BKL_PWM		
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC	24 30	

All: MAKE_BASE=TRUE

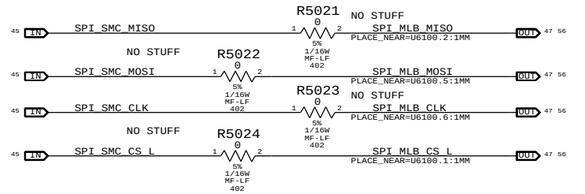
R5012 22 5% 1/20W MF 201
PM_CLK32K_SUSCLK_R (PLACE_NEAR=U1800.N14:5MM) → SMC_CLK32K

SMC12 PECI Support



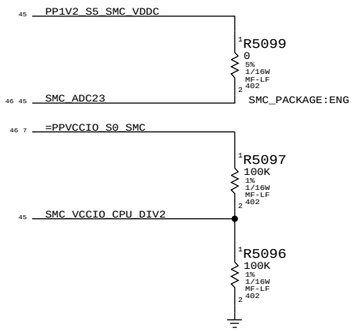
SMC12 SPI Support

Series resistors are no stuffed until the
topology of 2 SPI Masters are verified.



SCM12 Eng Pkg Support

Eng Package requires 1.2V ON SMC_ADC23 pin.



SMC_ONOFF_L	R5070	10K	
G3_POWERON_L	R5072	10K	
SMC_LID	R5071	100K	
SMC_TX_L	R5073	10K	
SMC_RX_L	R5074	100K	
SMC_DEBUGPRT_TX_L	R5075	10K	
SMC_DEBUGPRT_RX_L	R5076	100K	
SMC_TMS	R5077	10K	
SMC_TDO	R5078	10K	
SMC_TDI	R5079	10K	
SMC_TCK	R5080	10K	
SMC_BIL_BUTTON_L	R5081	10K	
SMC_BC_ACOK	R5087	470K	
SMC_S5_PWRGD_VIN	R5092	100K	
MEM_EVENT_L	R5014	10K	
CPU_THRMTRIP_3V3	R5017	100K	

All: 5% 1/20W MF 201

Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD

SMC_ROMBOOT	R5088	1K	
SMC_ADAPTER_EN	R5085	10K	
SMC_THRMTRIP	R5086	10K	
SMC_S4_WAKESRC_EN	R5090	100K	
SMC_DELAYED_PWRGD	R5091	100K	
SMC_PM_G2_EN	R5093	100K	

All: 5% 1/20W MF 201

PP3V3_WLAN
WIFI_EVENT_L — R5089 10K 5% 1/20W MF 201

SYNC_MASTER=J31_YONAS SYNC_DATE=01/19/2012

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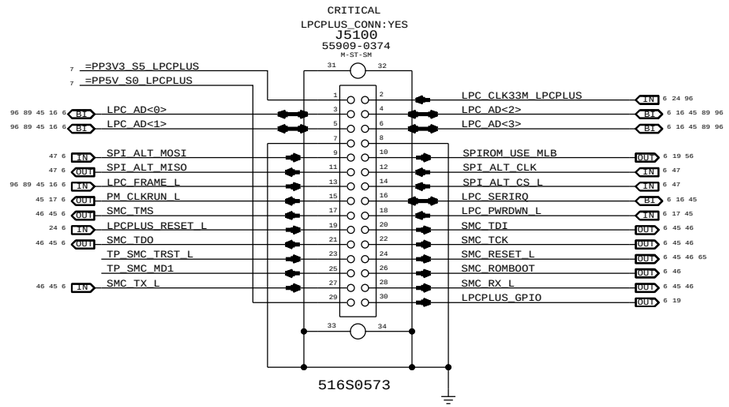
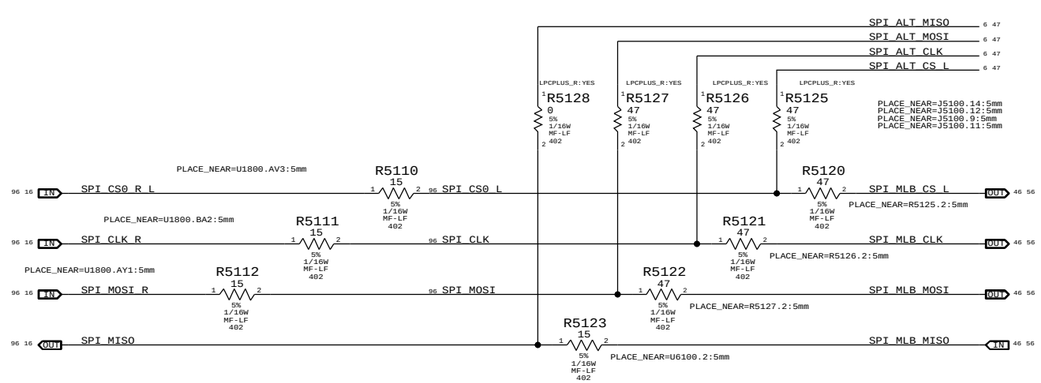
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=J5_MLB SYNC_DATE=05/26/2011

PAGE TITLE

LPC+SPI Debug Connector

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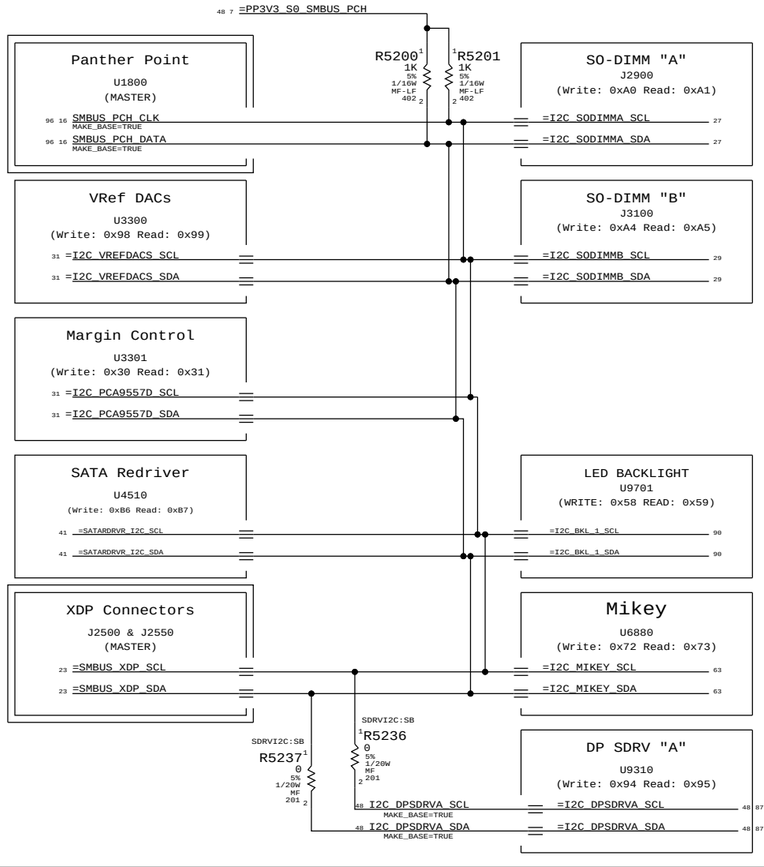
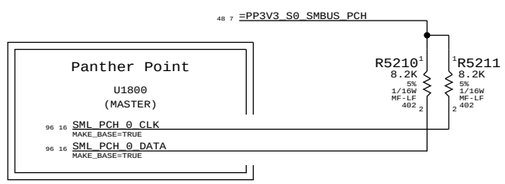
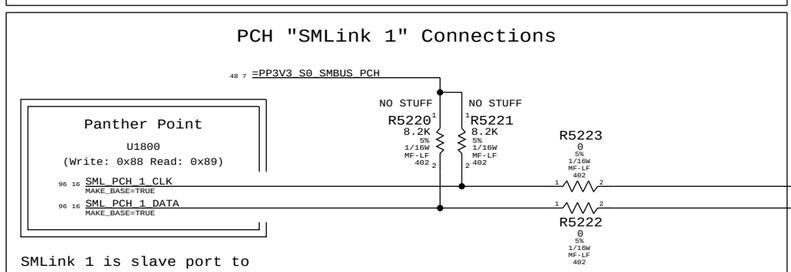
PCH SMBus "0" Connections



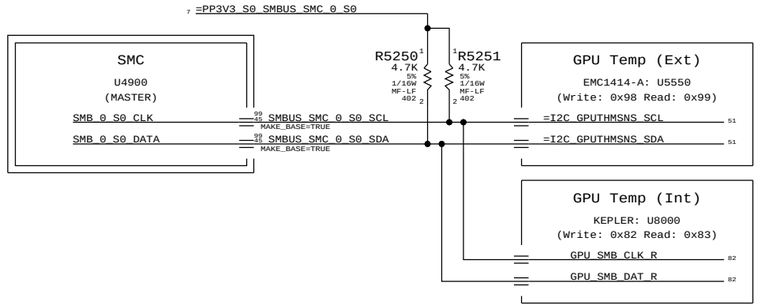
PCH "SMLink 0" Connections



PCH "SMLink 1" Connections

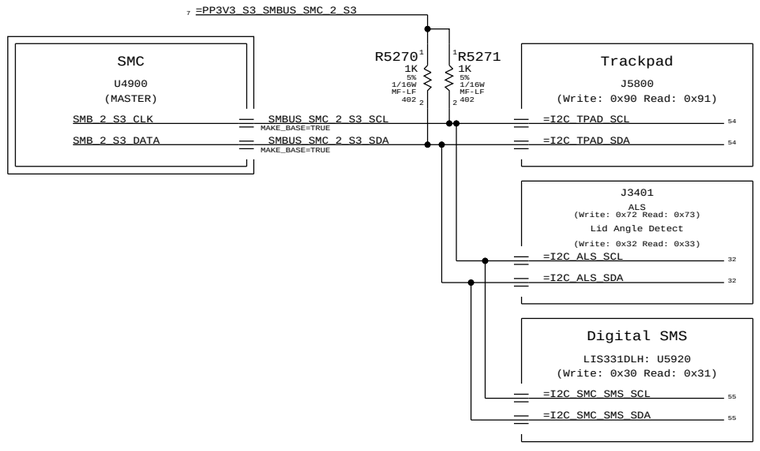


SMC "0" SMBus Connections

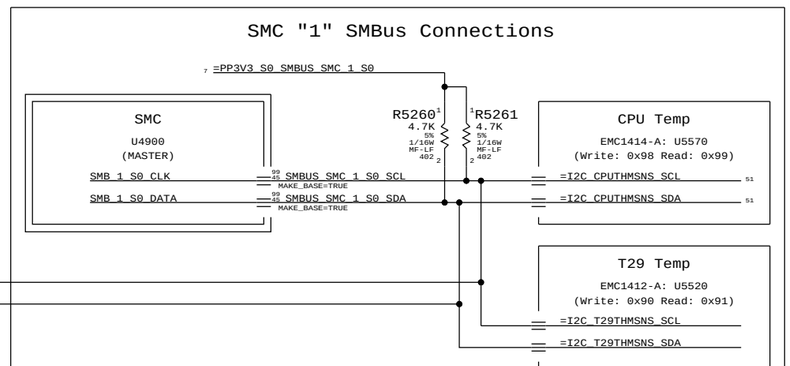


SMC "2" SMBus Connections

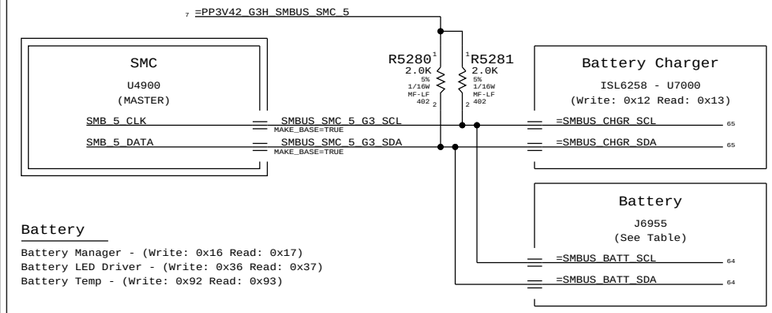
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "1" SMBus Connections



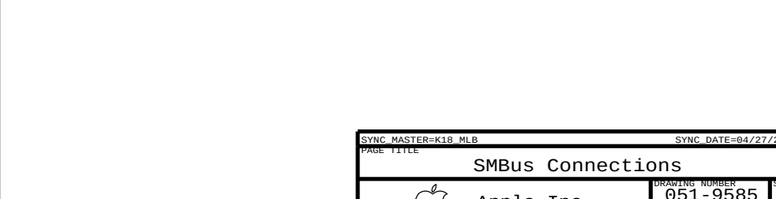
SMC "5" SMBus Connections



Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "3" SMBus Connections



T29 SMBus Connections

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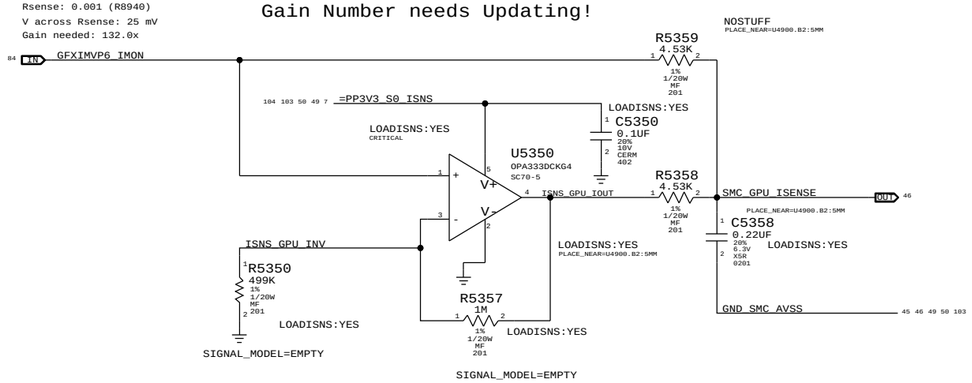
GPU Core Load Side Current Sense (IG0C)

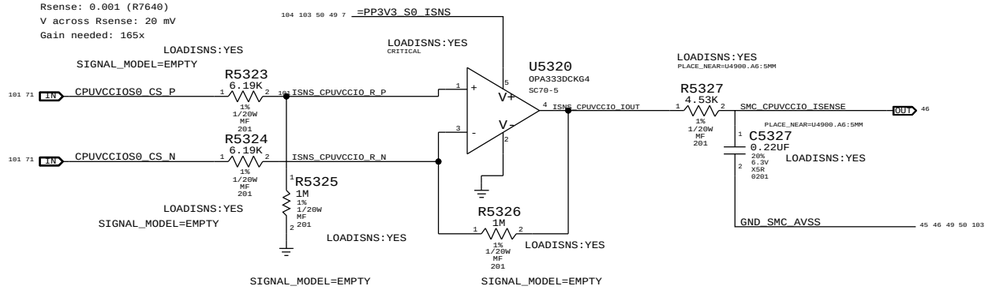
Gain: 130.2x, EDP: 25 A
Rsense: 0.001 (R8940)
V across Rsense: 25 mV
Gain needed: 132.0x

Gain Number needs Updating!



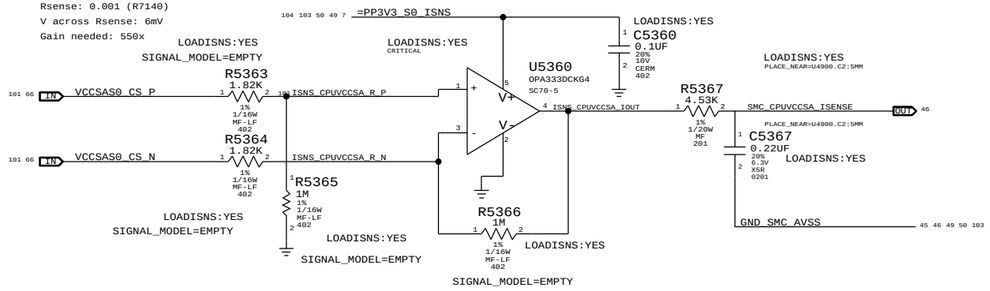
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 161.5x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 20 mV
Gain needed: 165x



CPU VCCSA Load Side Current Sense (IC2C)

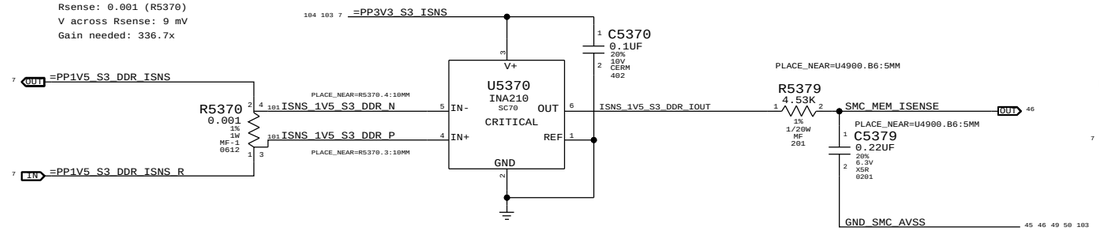
Gain: 549x, EDP: 6A
Rsense: 0.001 (R7140)
V across Rsense: 6mV
Gain needed: 550x



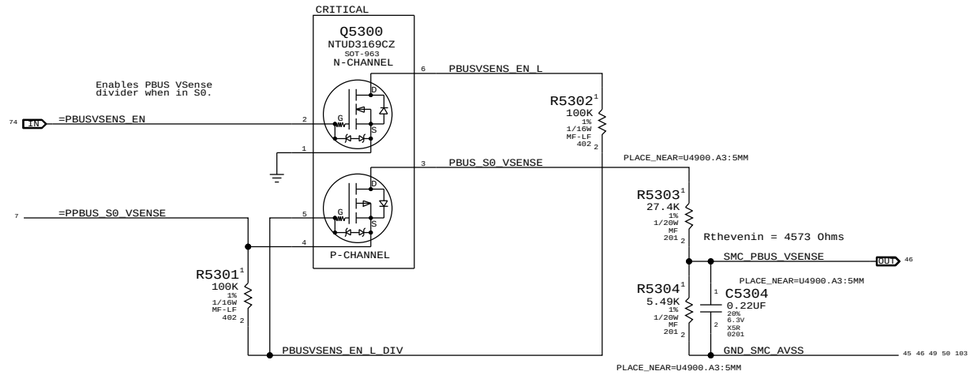
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,100K,201	C5358,C5327,C5367		LOADISNS:NO

DDR 1.5V S3 (Memory) Current Sense (IM0C)

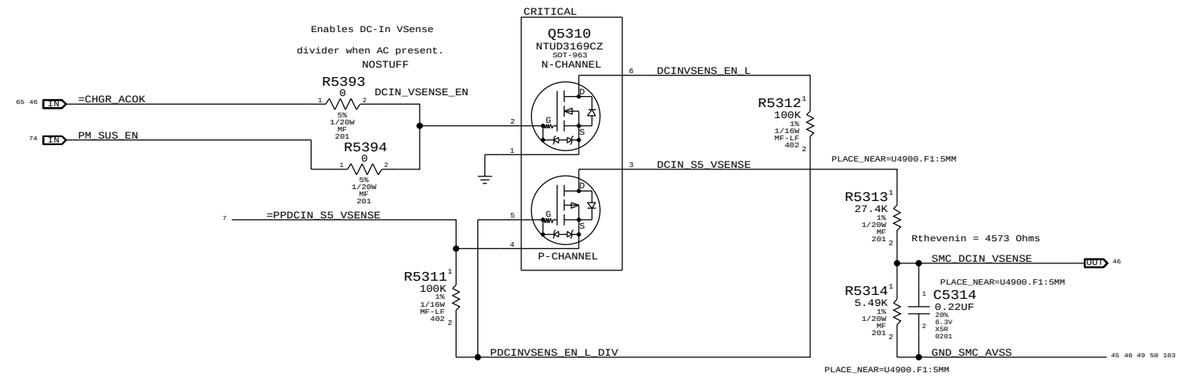
Gain: 200x, EDP: 9A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 336.7x



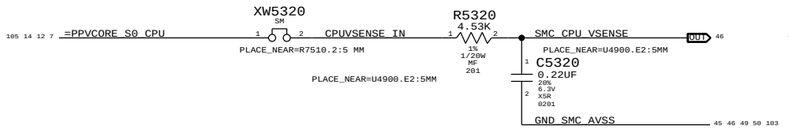
PBUS Voltage Sense & Enable (VP0R)



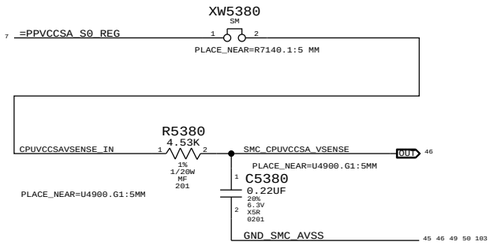
DC-In Voltage Sense & Enable (VD0R)



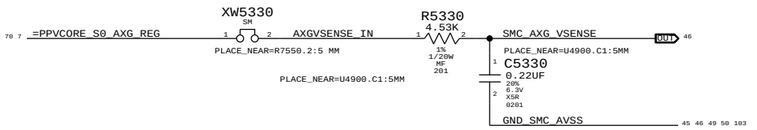
CPU Core Voltage Sense (VC0C)



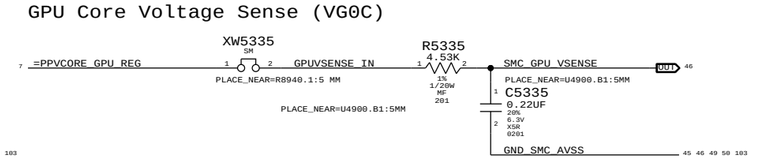
CPU VCCSA Voltage Sense (VC2C)



AXG Core Voltage Sense (VN0C)



GPU Core Voltage Sense (VG0C)



SYNC_MASTER=J31_YONAS SYNC_DATE=01/19/2012

PAGE TITLE

Power Sensors: Load Side

Apple Inc.

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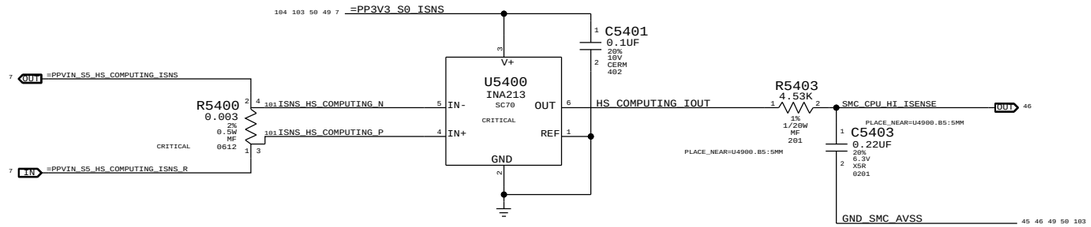
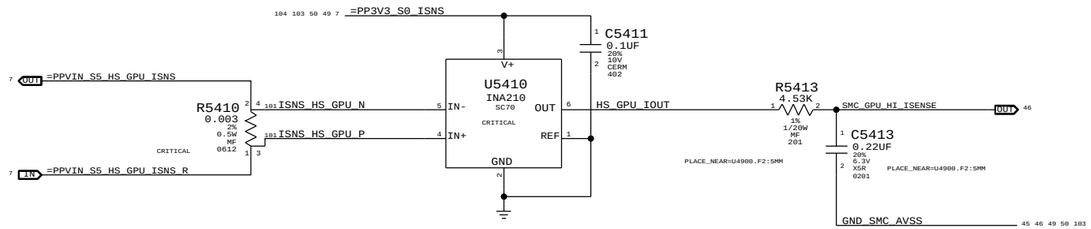
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 22.8 A
Rsense: 0.003 (R5400)
V across Rsense: 68.4 mV
Gain needed: 48.25x



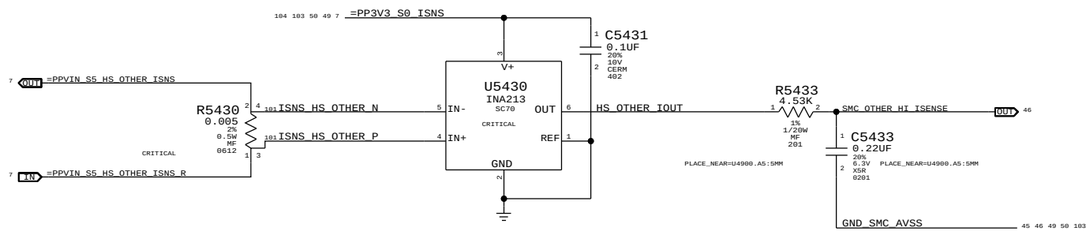
GPU High Side Current Sense (IG0R)

Gain: 200x, EDP: 5.2 A (Kepler)
Rsense: 0.003 (R5410)
V across Rsense: 15.6 mV
Gain needed: 211.54x (Kepler)



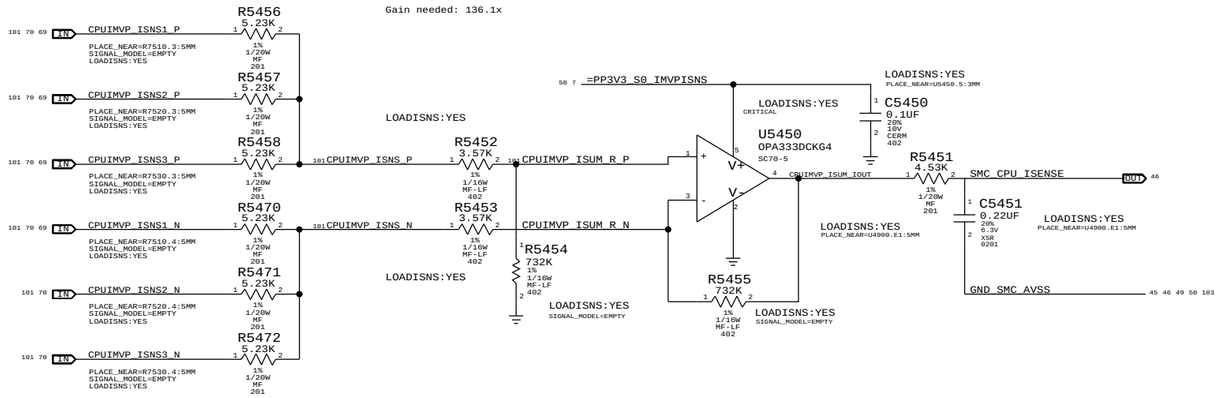
OTHER High Side Current Sense (IO0R)

Gain: 50x, EDP: 10.3 A
Rsense: 0.005 (R5440)
V across Rsense: 51.5 mV
Gain needed: 64.1x



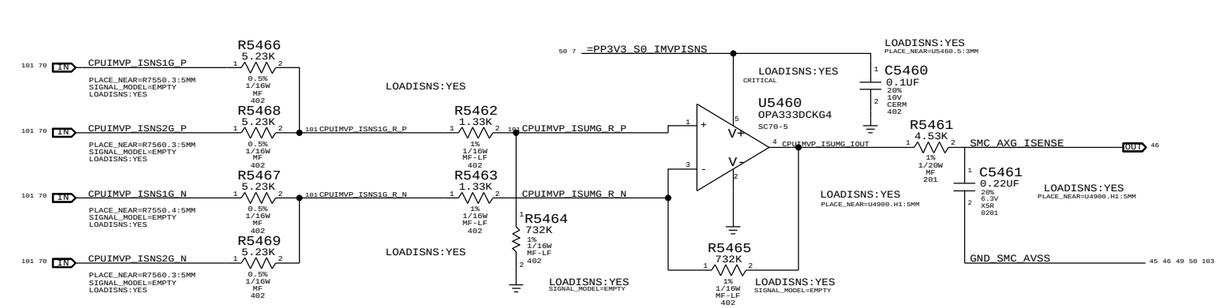
CPU Core Load Side Current Sense (IC0C)

Gain: 136.1x, EDP: 97 A
Rsense: 3x of 0.00075 (R7510, R7520. R7530), Rsum: 0.00025.
V across Rsense: 24.25 mV
Gain needed: 136.1x



AXG Core Load Side Current Sense (IN0C)

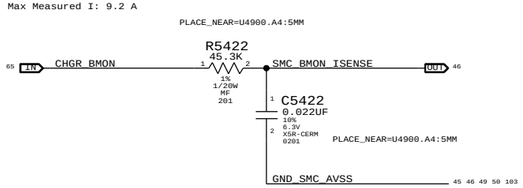
Gain: 185.5x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375.
V across Rsense: 17.25 mV
Gain needed: 191.3x



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,100K,201	C5451,C5461		LOADISNS:NO

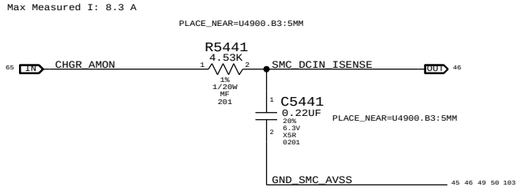
Charger (BMON Prod) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Measured I: 9.2 A



DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Measured I: 8.3 A



SYNC_MASTER=J31_YONAS SYNC_DATE=10/25/2011

PAGE TITLE: Power Sensors: High Side, CPU, AXG

Apple Inc.

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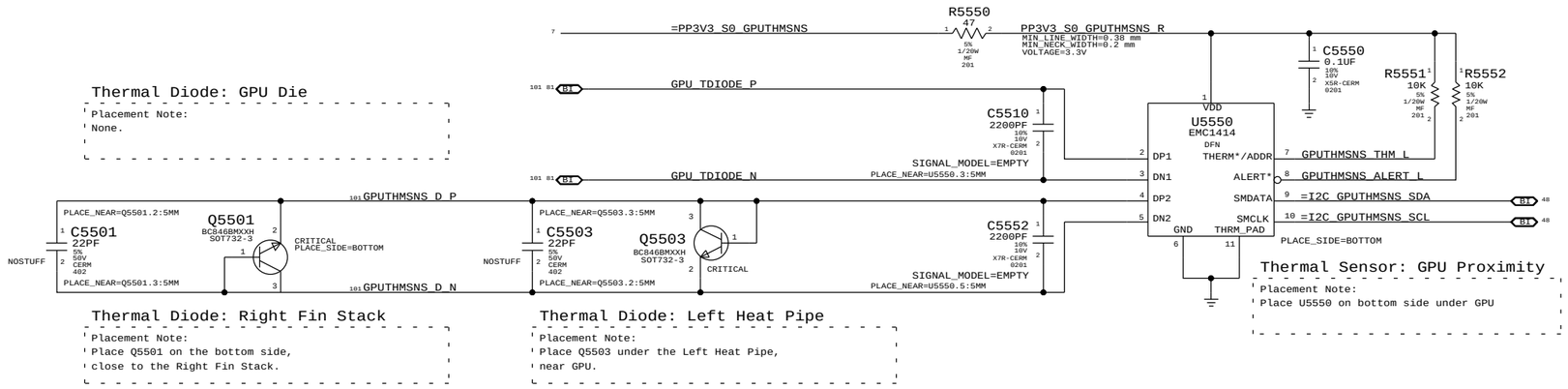
Thermal Sensor A:
GPU Proximity, GPU Die, Left Heat Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: GPU Die

Placement Note:
None.

Thermal Diode: Right Fin Stack

Placement Note:
Place Q5501 on the bottom side,
close to the Right Fin Stack.

Thermal Diode: Left Heat Pipe

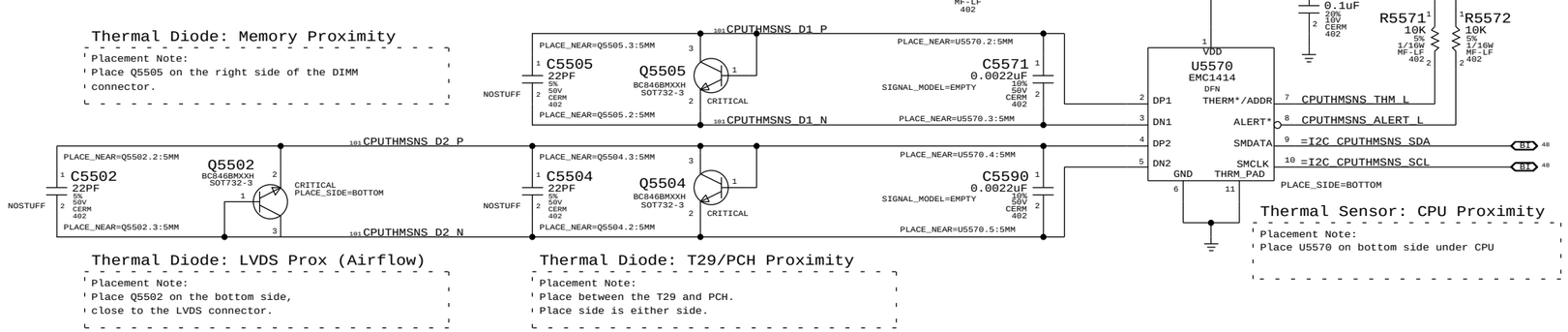
Placement Note:
Place Q5503 under the Left Heat Pipe,
near GPU.

Thermal Sensor: GPU Proximity

Placement Note:
Place U5550 on bottom side under GPU

Thermal Sensor B:
CPU Proximity, Memory Proximity, T29/PCH Proximity, LVDS Proximity (Airflow)

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Memory Proximity

Placement Note:
Place Q5505 on the right side of the DIMM
connector.

Thermal Diode: LVDS Prox (Airflow)

Placement Note:
Place Q5502 on the bottom side,
close to the LVDS connector.

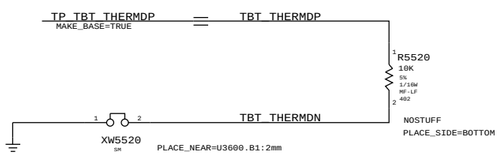
Thermal Diode: T29/PCH Proximity

Placement Note:
Place between the T29 and PCH.
Place side is either side.

Thermal Sensor: CPU Proximity

Placement Note:
Place U5570 on bottom side under CPU

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

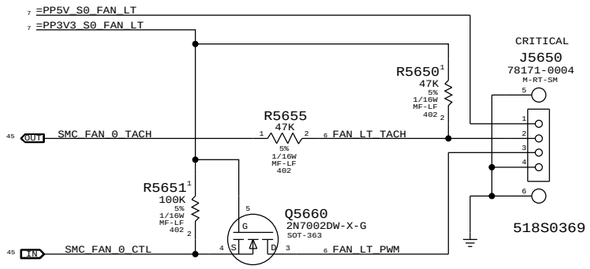
SYNC_MASTER=J31_YONAS SYNC_DATE=09/08/2011

PAGE TITLE: Thermal Sensors

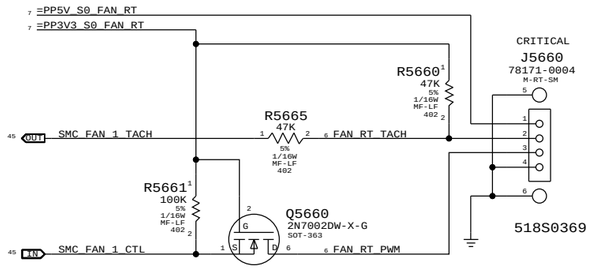
Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 55 OF 132
SHEET: 51 OF 105

Left Fan



Right Fan



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

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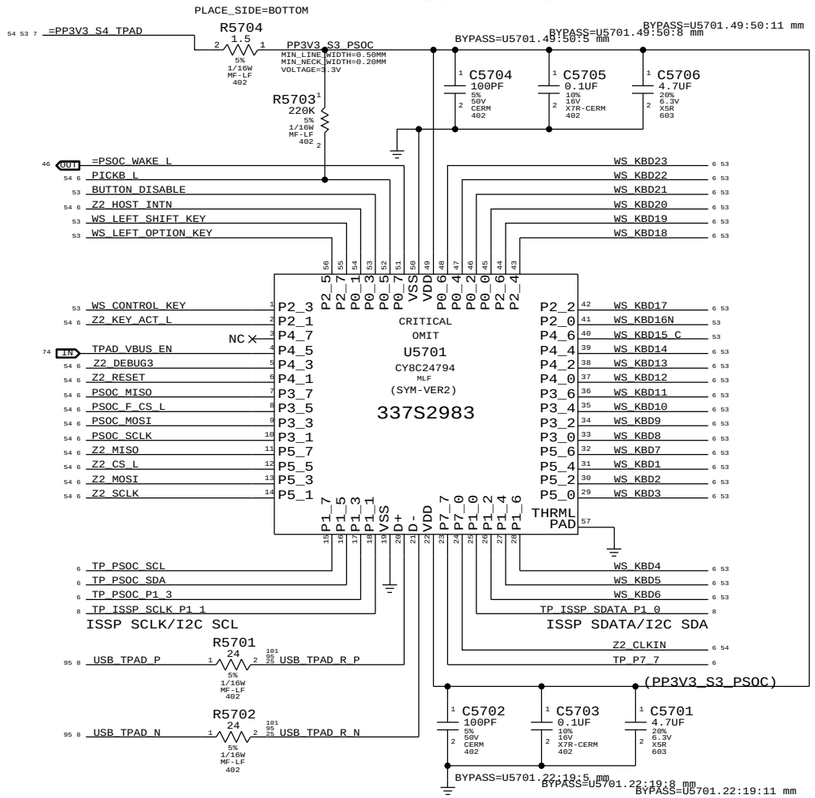
SHEET: 52 OF 105

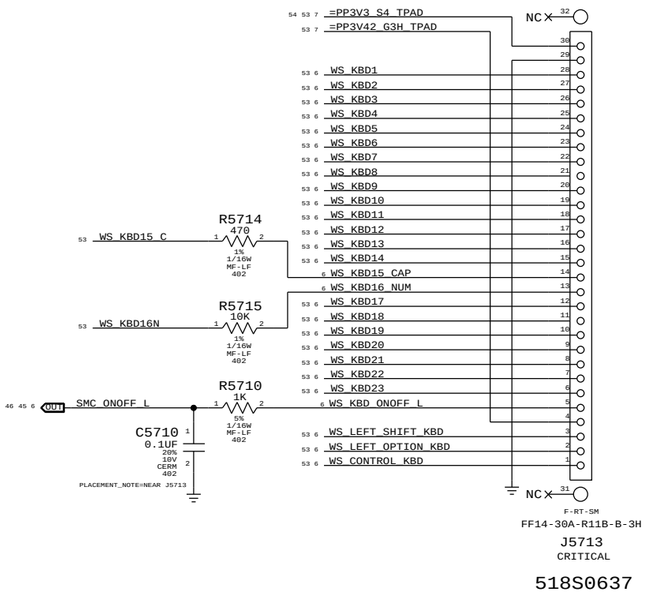
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

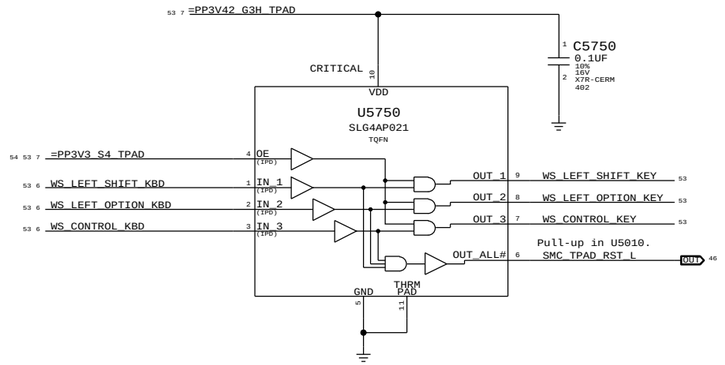
Keyboard Connector



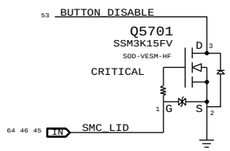
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



TPAD Buttons Disable



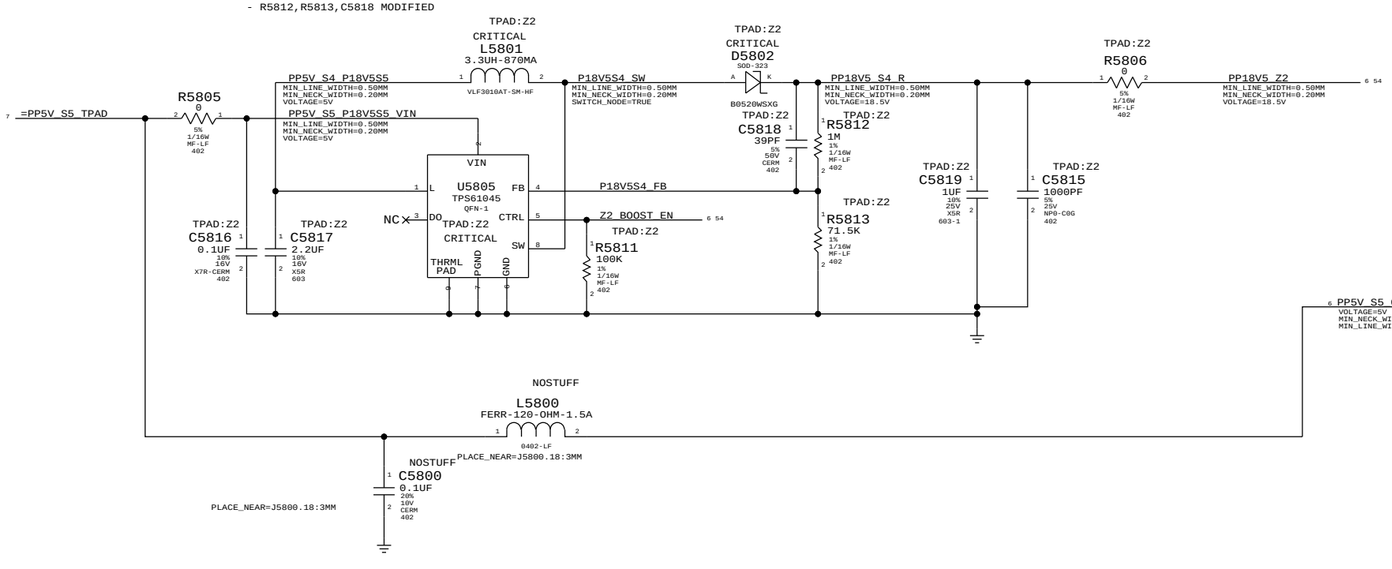
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

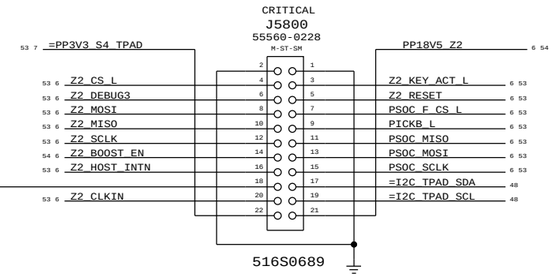
SYNC_MASTER=J30_MLB	SYNC_DATE=06/10/2011
PAGE TITLE: WELLSPRING 1	
Apple Inc.	DRAWING NUMBER: 051-9585 SIZE: D
	REVISION: 3.0.0
	BRANCH:
	PAGE: 57 OF 132
	SHEET: 53 OF 105

BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

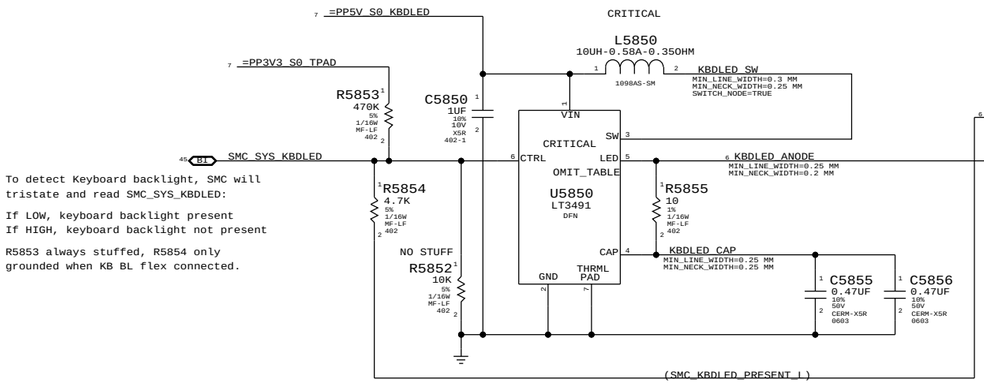


IPD Flex Connector



PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

Keyboard Backlight Driver & Detection

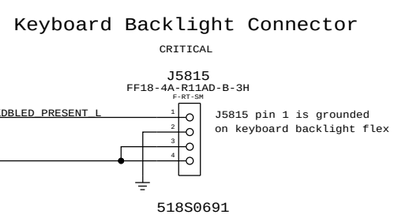


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3085	1	IC,STLA02,1-STRING LED DRIVER,2X2DFN-6	U5850	CRITICAL	

SYNC_MASTER=J31_LINDA SYNC_DATE=07/01/2011

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
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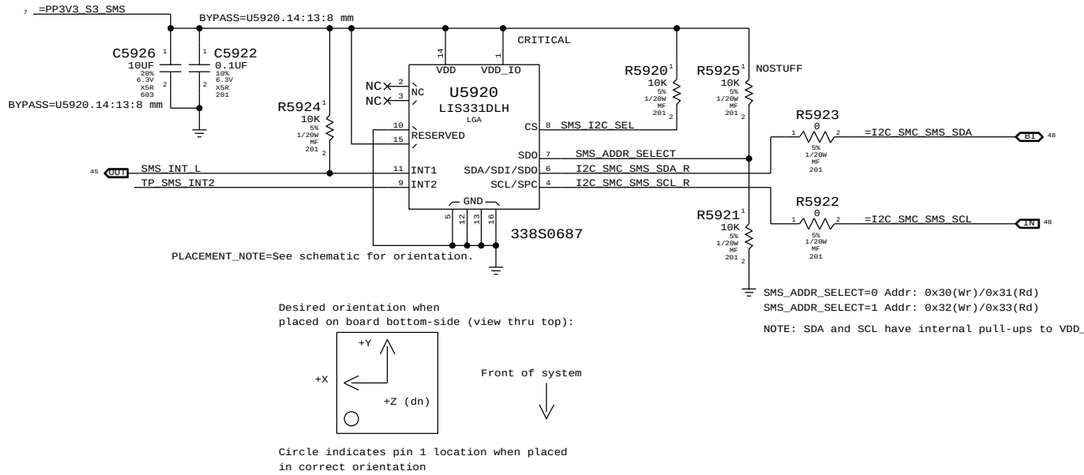

SYNC_MASTER=J31_YONAS SYNC_DATE=08/11/2011

PAGE TITLE: Digital Accelerometer

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

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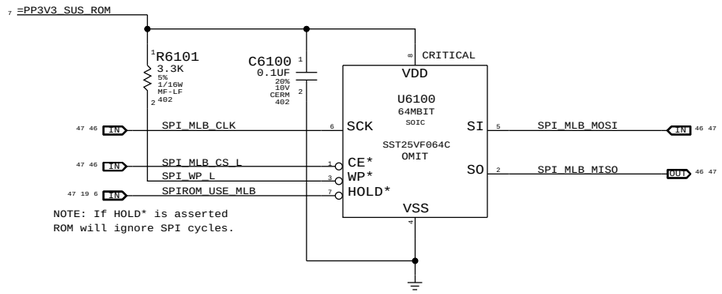

SYNC_MASTER=K91_BEN SYNC_DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

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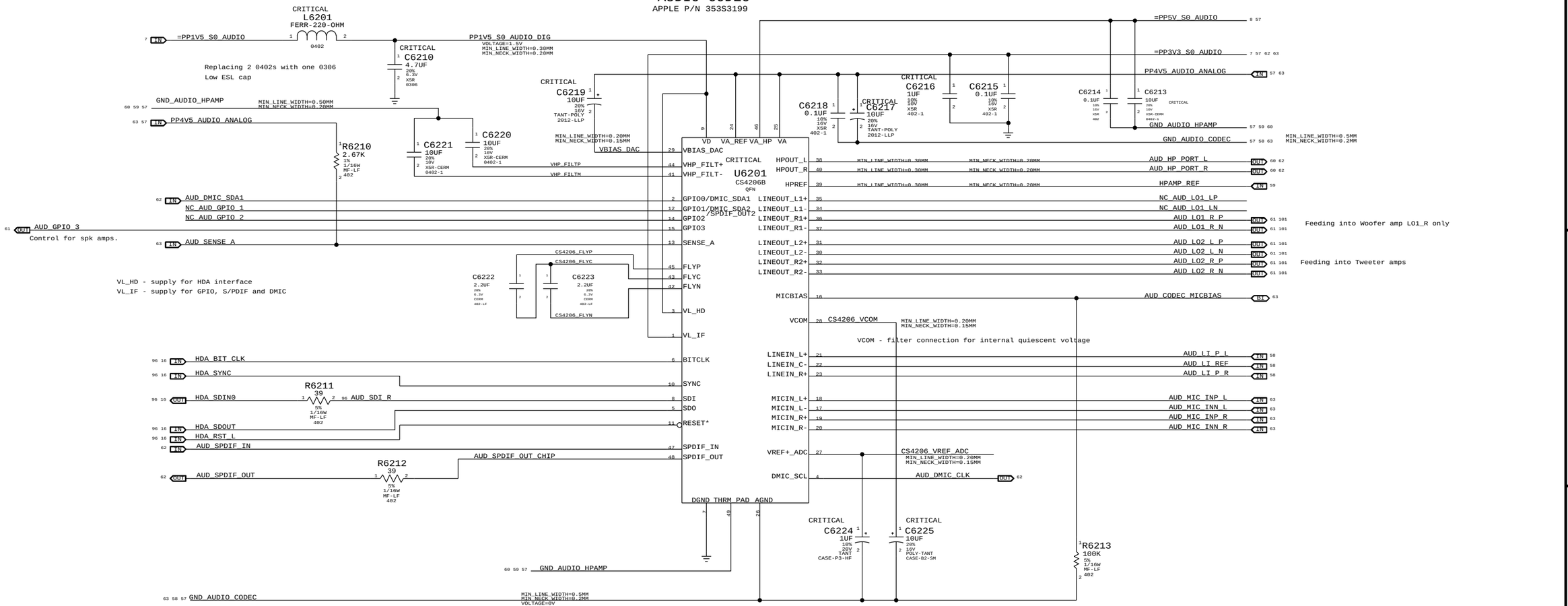
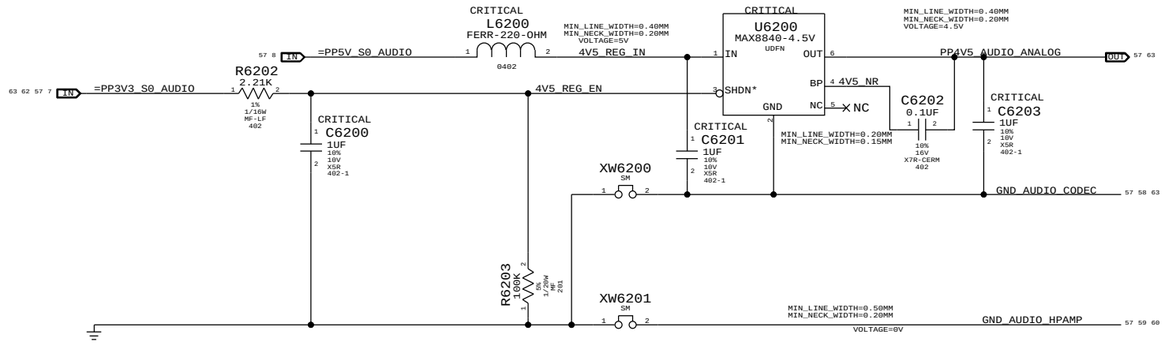
AUDIO CODEC

APPLE P/N 353S3199



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2234



NOTES ON CODEC usage

Hpamp of Codec enabled
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
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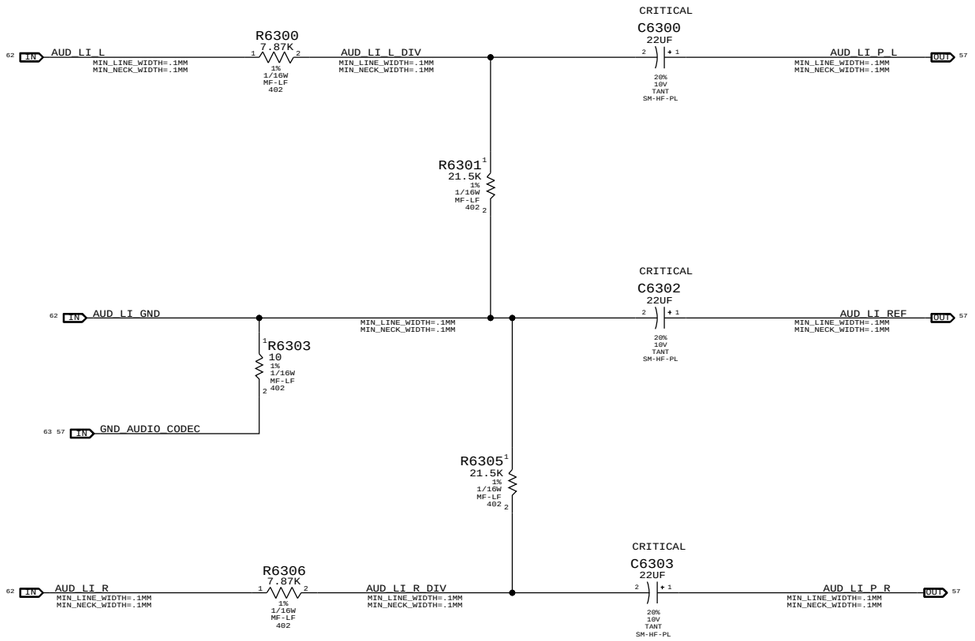
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 0.36 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2013

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D
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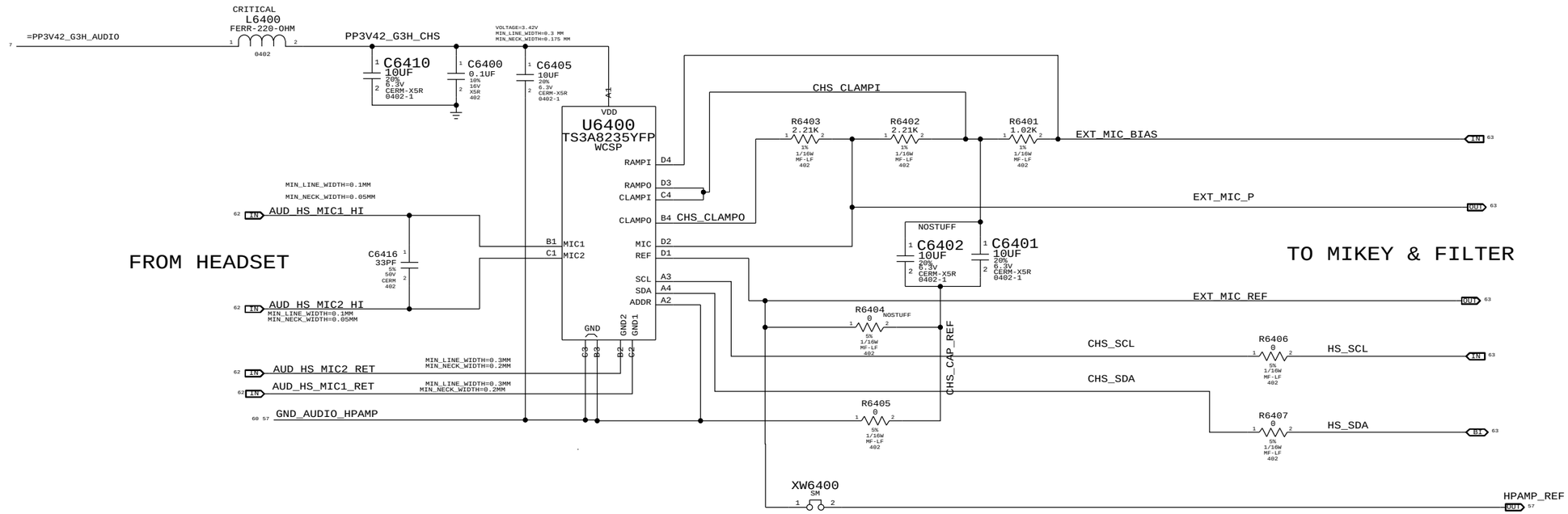
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY

APN: 353S3066 as of JUly 2011

U6400 should get VDD from battery. Should be powered all the time.



I2C ADDRESSES: CHS uses SMBus 0 connections

CHS	U6400	READ	0111	0111	0x77
CHS	U6400	WRITE	0111	0110	0x76

SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE
AUDIO: DETECT/MIC BIAS

Apple Inc.

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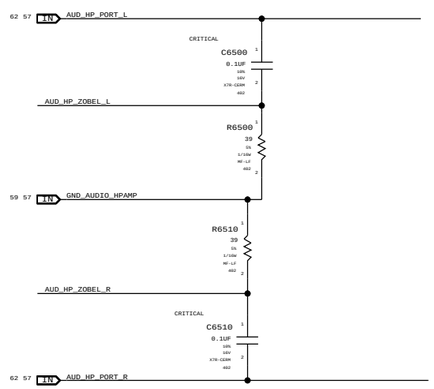
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

3X MONO SPEAKER AMPLIFIERS (SSM2375)

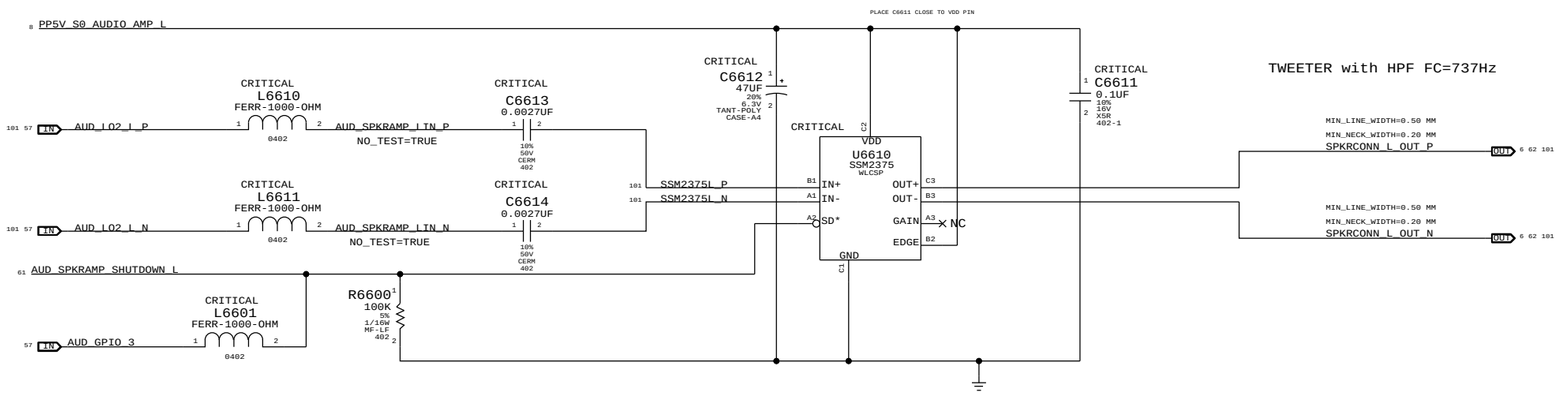
APN: 353S2958 as of July 2011

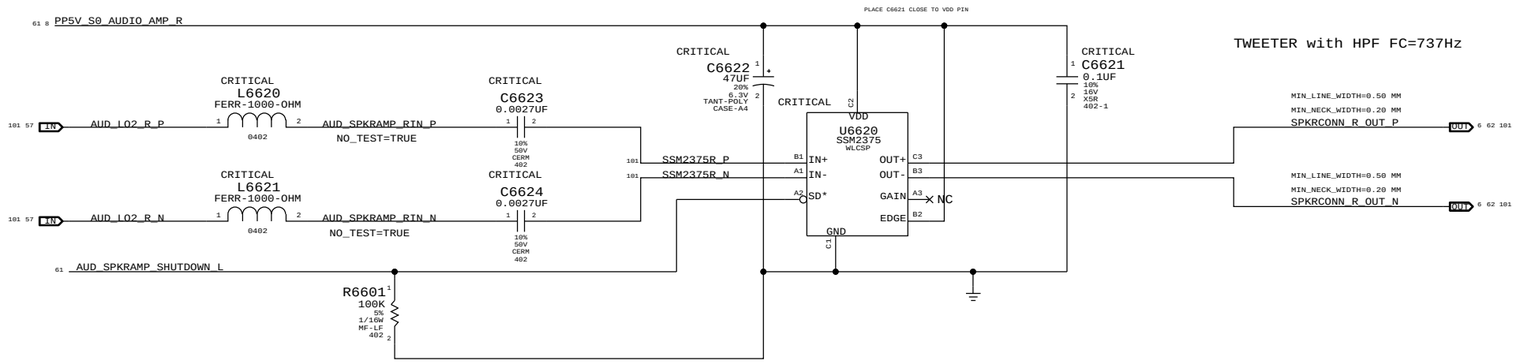
GAIN = +3 DB Rin=80k irrespective of gain

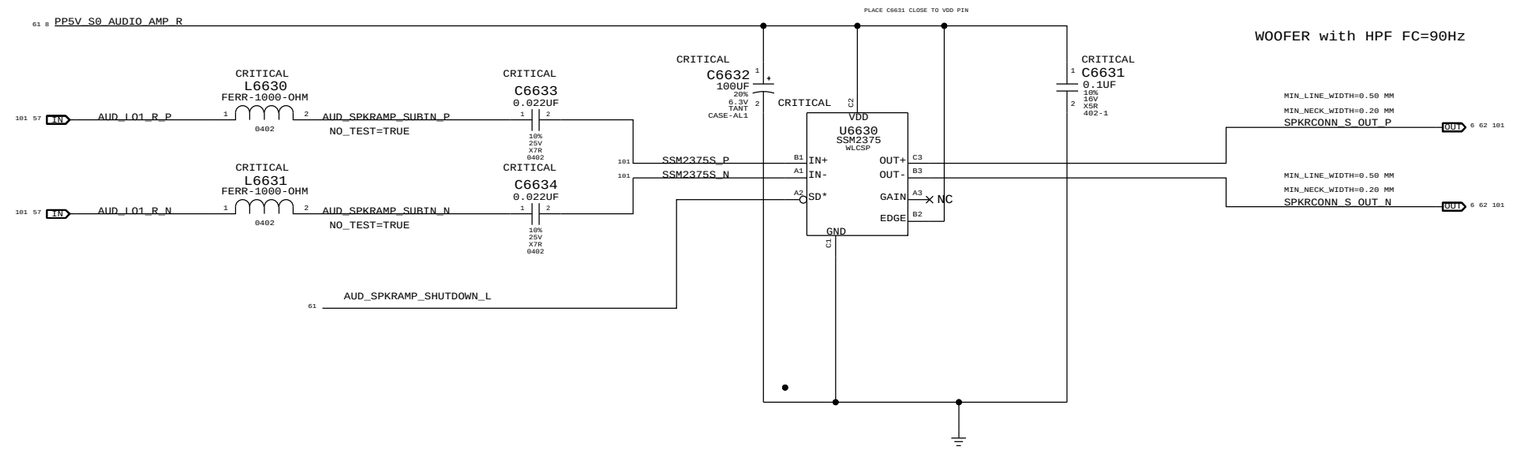
1ST ORDER FC (L&R) = ~737 HZ

1ST ORDER FC (SUB) = ~90 HZ

Gain Pin	Gain dB
Connect to VDD	6
Connect to VDD through 47k	12
Not connected	3
Connect to GND through 47k	9
Connect to GND	0







SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

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REVISION 3.0.0

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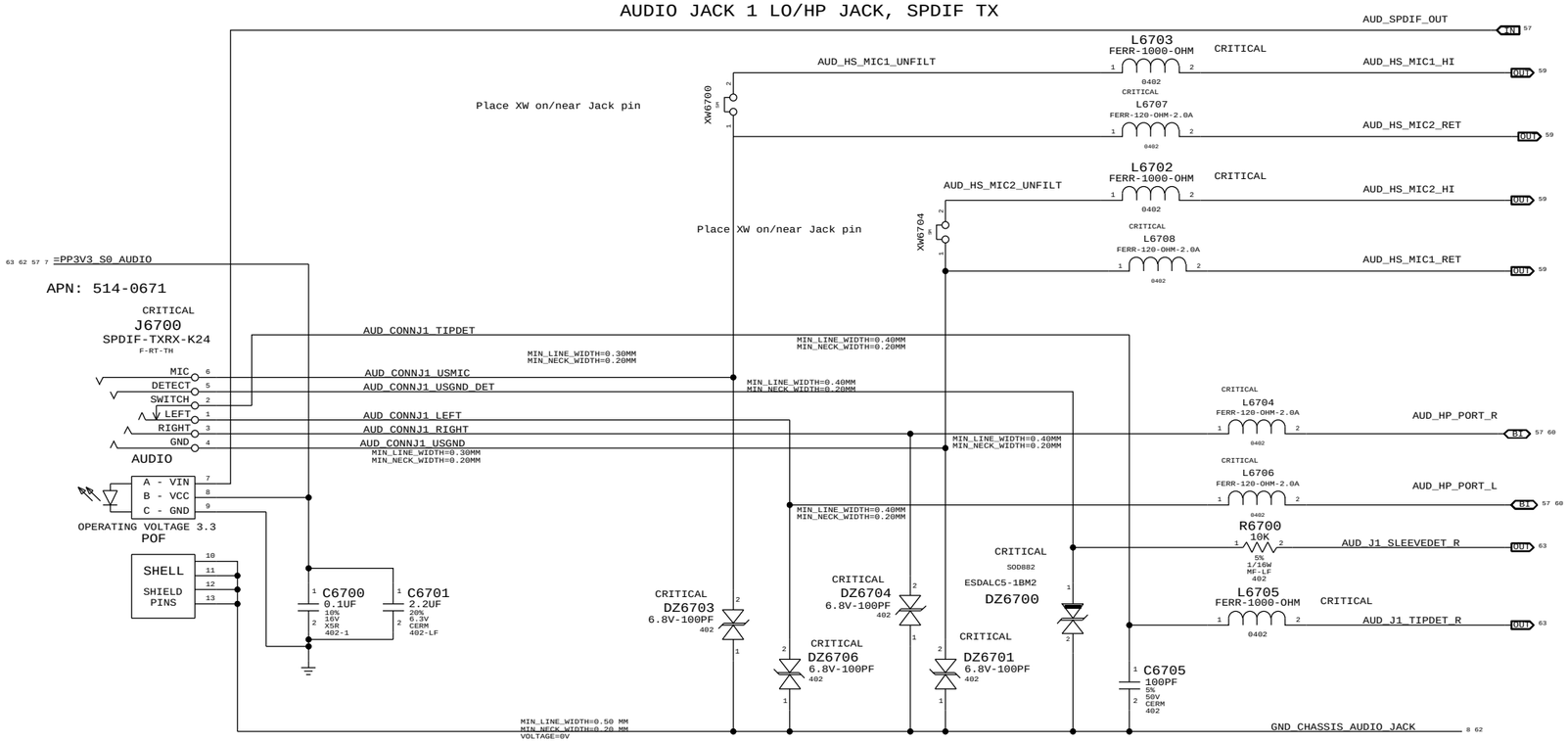
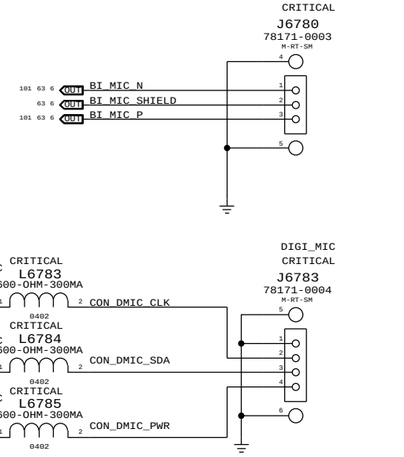
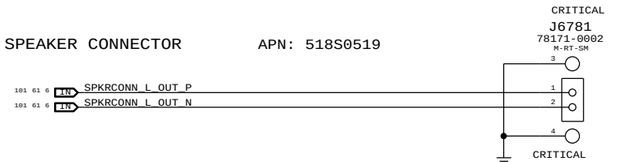
AUDIO JACK 1 LO/HP JACK, SPDIF TX



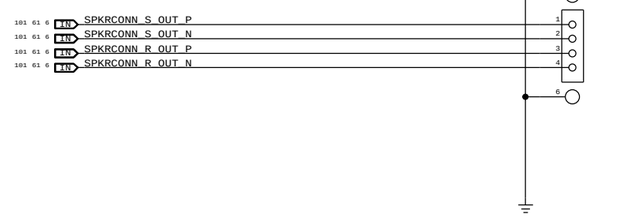
MIC CONNECTOR



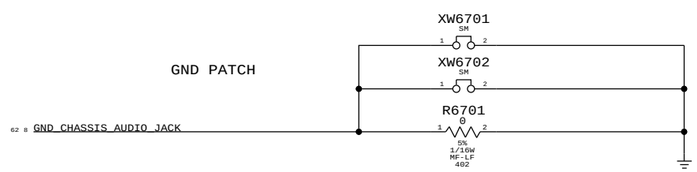
SPEAKER CONNECTOR APN: 518S0519



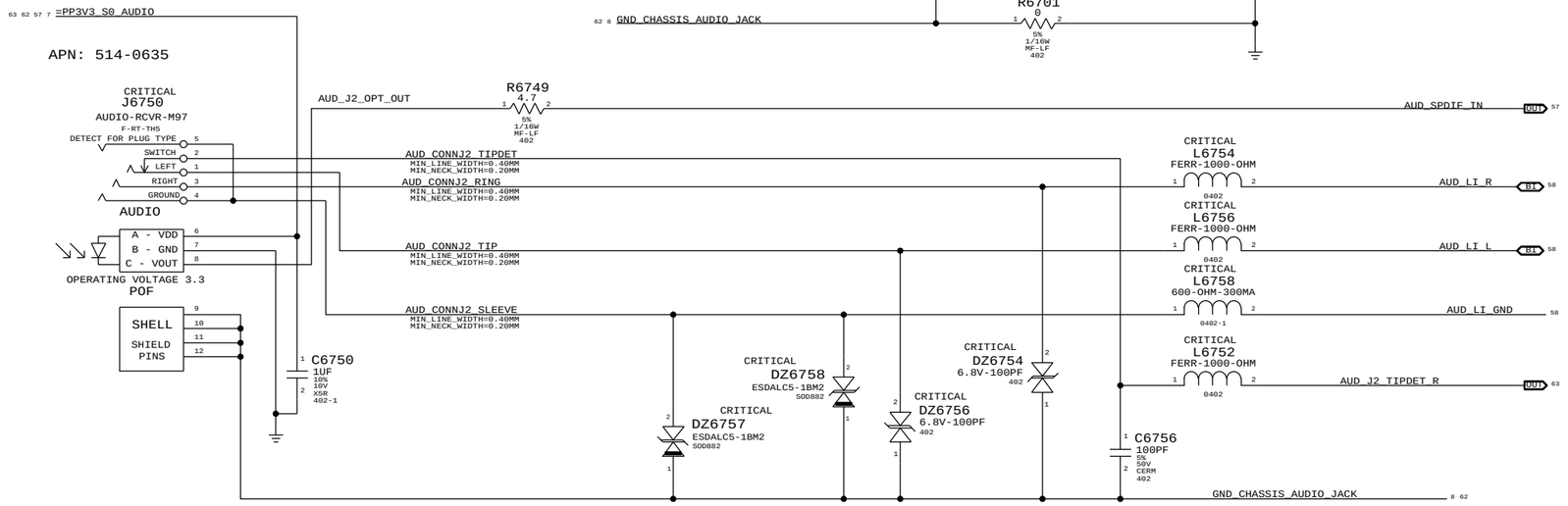
SPEAKER CONNECTOR APN: 518S0521



GND PATCH



AUDIO JACK 2 LINE IN JACK, SPDIF RX



SYNC MASTER=J31_AUDIO	SYNC DATE=10/26/2011
PAGE TITLE	AUDIO: JACKS
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	NA	0X09 (Jack Detect A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (Jack detect B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (Jack detect C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

I2C addresses: Mikey uses SMBus 0

MIKEY U6880 READ 0111 0011 0x73

MIKEY U6880 WRITE 0111 0010 0x72

CRITICAL L6880 FERR-1000-OHM 0402

63 62 57 7 =PP3V3_S0_AUDIO

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V

PP3V3_S0_HS_RX

CSP MIKEY
APN:353S2640

48 IN =I2C_MIKEY_SCL — R6882 0 5% 1/16W MF-LF 402 — PULLUPS ON MCP PAGE — OUT 59

R6886 10K 5% 1/16W MF-LF 402

CRITICAL C6880 10UF 20% 6.3V X5R 603

CRITICAL C6887 0.1UF 10% 25V X5R 402

CRITICAL U6880 AVDD CD3282A1 WCSP

48 B1 =I2C_MIKEY_SDA — R6883 0 5% 1/16W MF-LF 402 — B1 59

HS_SCL C3 SCL — MICBIAS C1 EXT_MIC_BIAS
HS_SDA B3 SDA — DETECT B1 HS_SW_DET
HS_INT_L D3 INT* — BYPASS D1 HS_RX_BP
HS_ENABLE A3 ENABLE
TIPDET_UNFILT 63 — A1 HDET
B2 CS
C2 DGND — D2 AGND

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM

CRITICAL C6882 2.2UF 20% 6.3V TANT 402

GND_AUDIO_CODEC 57 58 63

18 OUT AUD_I2C_INT_L — R6884 0 5% 1/16W MF-LF 402

24 IN AUD_IPHS_SWITCH_EN — R6885 0 5% 1/16W MF-LF 402

R6887 100K 5% 1/16W MF-LF 402

C6881 0.01UF 10% 16V CERM 402

63 58 57 GND_AUDIO_CODEC

R6880 1K 1% 1/16W MF-LF 402 — OUT 59

PORT A DETECT (HEADPHONES)

PORT B DETECT(SPDIF DELEGATE)

63 57 OUT AUD_SENSE_A

PP4V5_AUDIO_ANALOG_FLT 63

R6804 150K 5% 1/16W MF-LF 402

62 IN AUD_J1_SLEEVEDET_R

C6802 0.01UF 10% 16V CERM 402

GND_AUDIO_CODEC 63 58 57

Q6803 DMC2400UV SOT563 P-CH

AUD_J1_SLEEVEDET_R_INV

R6814 220K 5% 1/16W MF-LF 402

AUD_J1_SLEEVEDET_R_BUF 63

AUD_J1_SLEEVEDET_R_INV

APN:376S0975

R6803 100K 5% 1/16W MF-LF 402

GND_AUDIO_CODEC 63 58 57

R6806 39.2K 1% 1/16W MF-LF 402 — AUD_PORTA_DET_L

R6805 20.0K 1% 1/16W MF-LF 402 — AUD_PORTB_DET_L

CRITICAL Q6801 SSM6N37FEAPE SOT563

CRITICAL Q6801 SSM6N37FEAPE SOT563

AUD_J1_SLEEVEDET_R_BUF 63

AUD_J1_DET_NMOS_DRN

CRITICAL L6801 FERR-1000-OHM 0402

57 IN PP4V5_AUDIO_ANALOG

C6804 0.1UF 10% 25% 402 CERM

63 58 57 GND_AUDIO_CODEC

63 PP4V5_AUDIO_ANALOG_FLT
MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=5V

R6801 220K 5% 1/16W MF-LF 402

R6802 100K 5% 1/20W MF 201

62 IN AUD_J1_TIPDET_R

AUD_J1_DET_RC2

AUD_J1_DET_RC

R6807 100K 5% 1/20W MF 201

C6801 0.1UF 20% 10V CERM 402

C6803 0.1UF 20% 10V CERM 402

SOT-563-HF NTZD3152P Q6804

SOT-563-HF NTZD3152P Q6804

AUD_J1_DET_R_GATE

R6808 220K 5% 1/16W MF-LF 402

R6809 220K 5% 1/16W MF-LF 402

AUD_J1_DET_NMOS_GATE

Q6800 SSM3K15AMFVAPE VESM

APN:376S1017

NOSTUFF
R6830 0 5%

TIPDET_UNFILT 63

63 58 57 GND_AUDIO_CODEC

R6840 100K 5% 1/16W MF-LF 402

AUD_IP_PERIPHERAL_DET — OUT 18

EXTRACTION NOTIFICATION
Voltage level shifting from 5V to 3.3V

R6841 200K 5% 1/16W MF-LF 402

63 58 57 GND_AUDIO_CODEC

CRITICAL C6883 0.1UF 10% 25V X5R 402

57 OUT AUD_MIC_INP_L — HS_MIC_HI_RC — R6890 2.2K 5% 1/16W MF-LF 402 — EXT_MIC_P — IN 59

MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.05MM

Place this next to Charleston

R6888 100K 5% 1/16W MF-LF 402

C6884 0.0082UF 10% 25V X7R 402 CRITICAL

C6885 27PF 5% 50V CERM 402 CRITICAL

CRITICAL C6886 0.1UF 10% 25V X5R 402

57 OUT AUD_MIC_INN_L — EXT_MIC_REF — IN 59

MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.05MM

PORT B RIGHT(BUILT-IN MIC)

57 IN AUD_CODEC_MICBIAS — R6850 100 1% 1/16W MF-LF 402 — MIC_BIAS_FILT — R6851 2.4K 1% 1/16W MF 402-1

CRITICAL C6852 2.2UF 20% 6.3V TANT 402

63 58 57 GND_AUDIO_CODEC

CRITICAL C6850 0.1UF 10% 25V X5R 402

57 OUT AUD_MIC_INP_R — BI_MIC_HI_F — L6850 FERR-1000-OHM 0402 — BI_MIC_P — IN 6 62 101

R6852 100K 5% 1/16W MF-LF 402

CRITICAL C6853 0.001UF 50V 10% 402 CERM

CRITICAL C6851 0.1UF 10% 25V X5R 402

57 OUT AUD_MIC_INN_R — BI_MIC_LO_F — L6851 FERR-1000-OHM 0402 — BI_MIC_N — IN 6 62 101

63 58 57 GND_AUDIO_CODEC — R6853 2.4K 1% 1/16W MF 402-1

HP=80HZ

XW6851 SM — BI_MIC_SHIELD — IN 6 62

Place this next to the connector

PORT C DETECT (LINE-IN)

63 57 OUT AUD_SENSE_A — R6813 10K 1% 1/16W MF-LF 402 — AUD_INJACK_INSERT_L — NC

63 62 57 7 =PP3V3_S0_AUDIO

R6811 270K 5% 1/16W MF-LF 402

Q6802 SSM3K15FV SOD-VESM-HF

R6812 47K 5% 1/16W MF-LF 402

62 IN AUD_J2_TIPDET_R — AUD_J2_DET_RC

C6811 0.1UF 20% 10V CERM 402

APN:376S0612

63 58 57 GND_AUDIO_CODEC

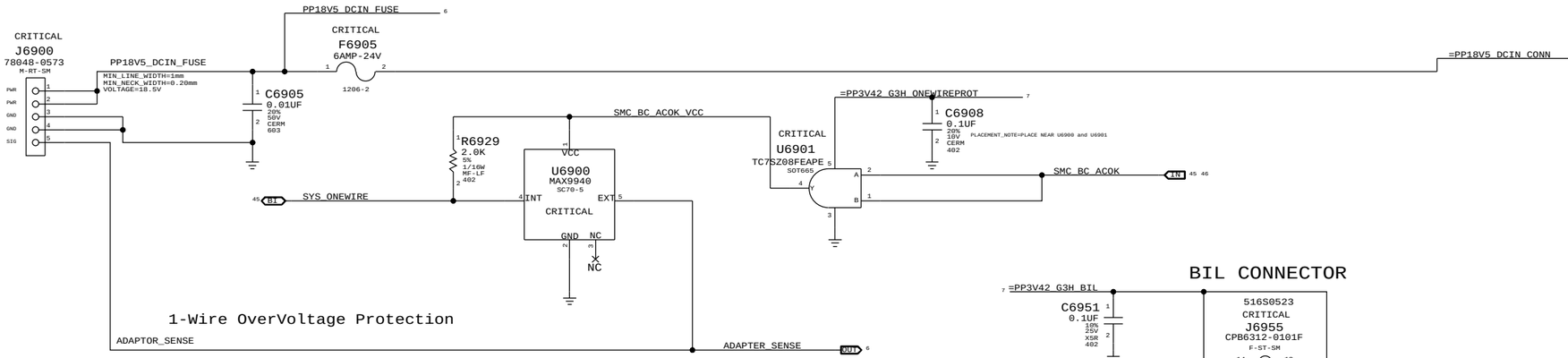
SYNC_MASTER=J31_AUDIO SYNC_DATE=10/26/2011

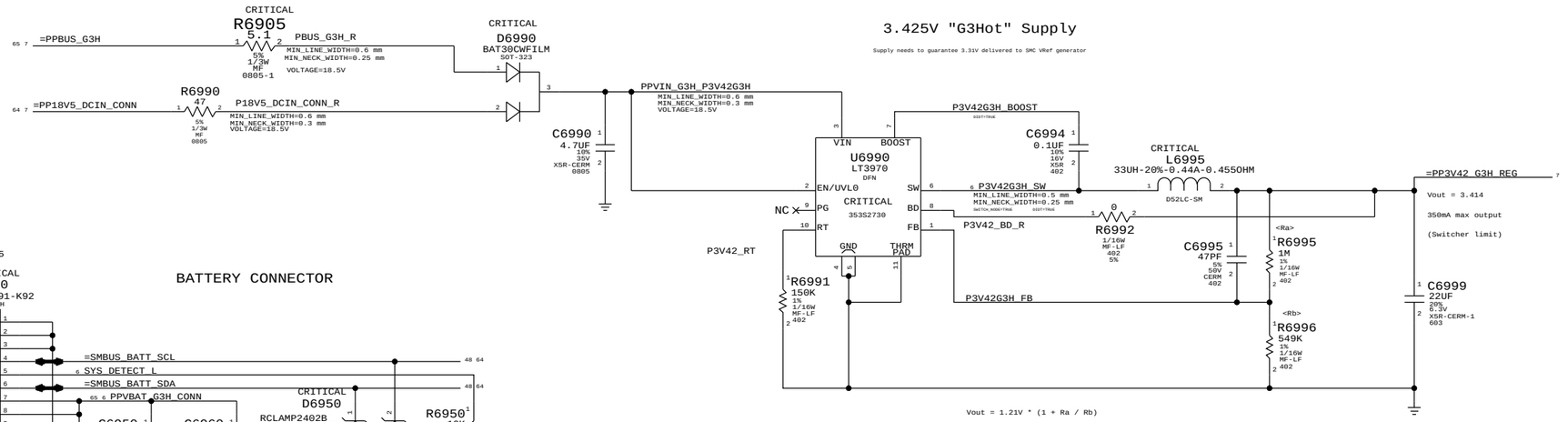
PAGE TITLE: AUDIO: JACK TRANSLATORS

Apple Inc.

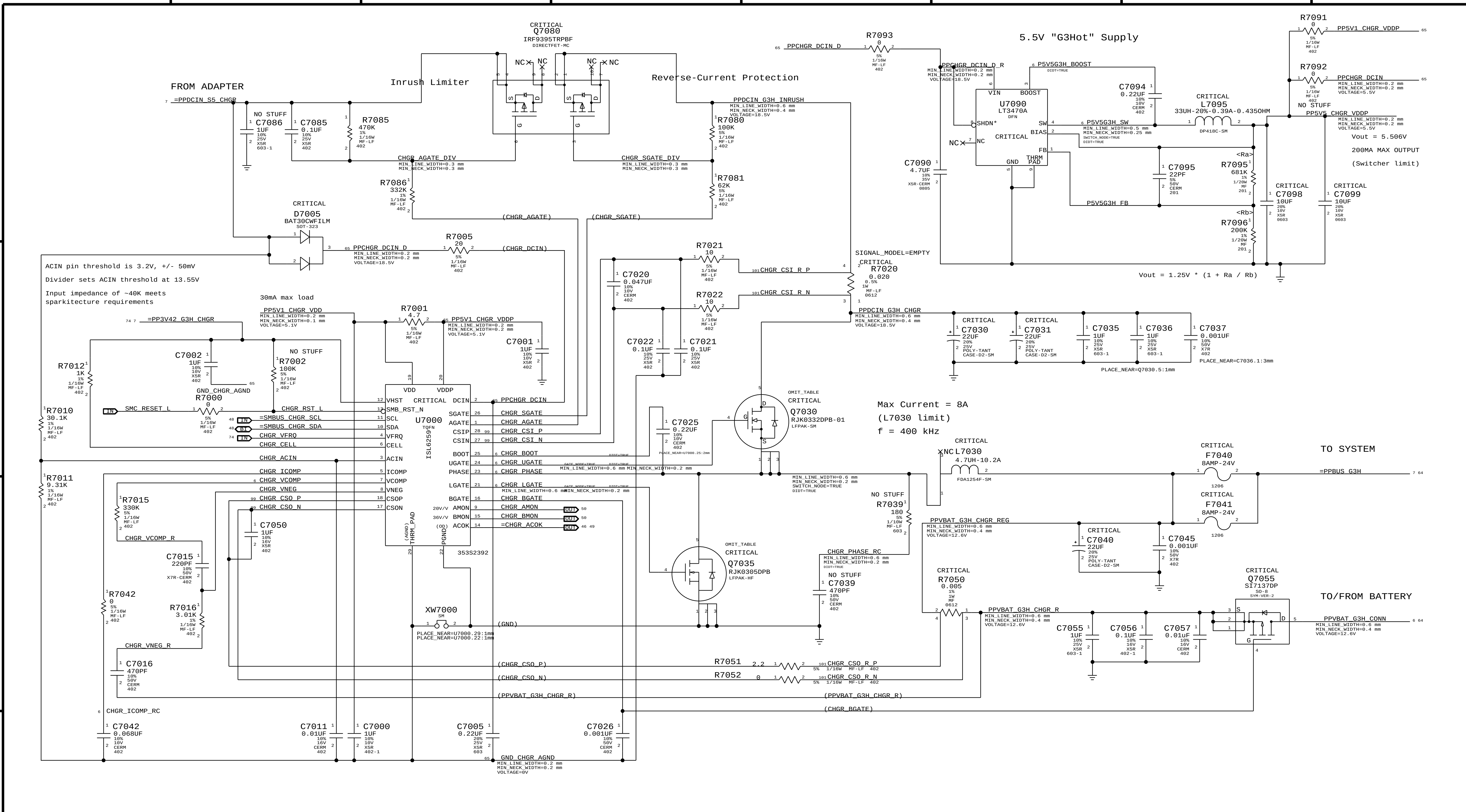
DRAWING NUMBER 051-9585 SIZE D
REVISION 3.0.0
BRANCH
PAGE 68 OF 132
SHEET 63 OF 105

MagSafe DC Power Jack





SYNC_MASTER=J31_JACK	SYNC_DATE=09/02/2011
PAGE TITLE	DC-In & Battery Connectors
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 69 OF 132
	SHEET 64 OF 105



SYNC_MASTER=J31_JACK SYNC_DATE=11/14/2011

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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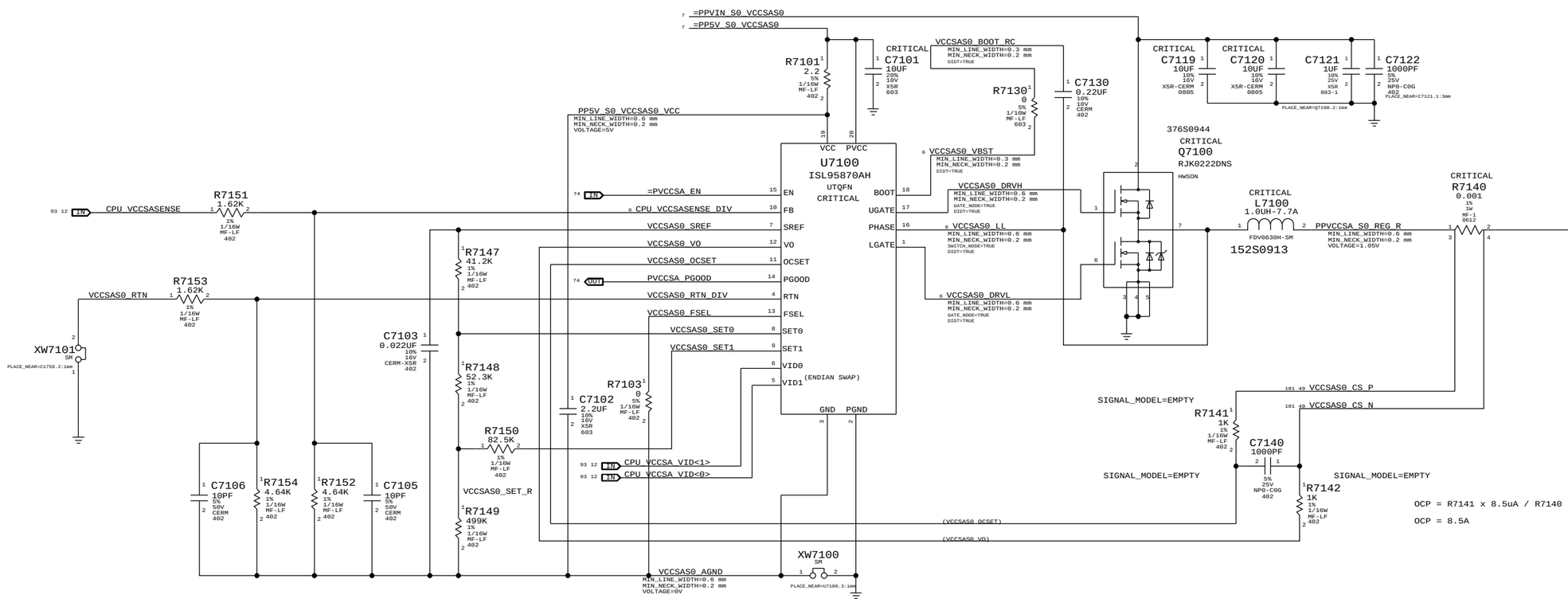


INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=J31_JACK SYNC_DATE=09/14/2011

PAGE TITLE: System Agent Supply

Apple Inc.

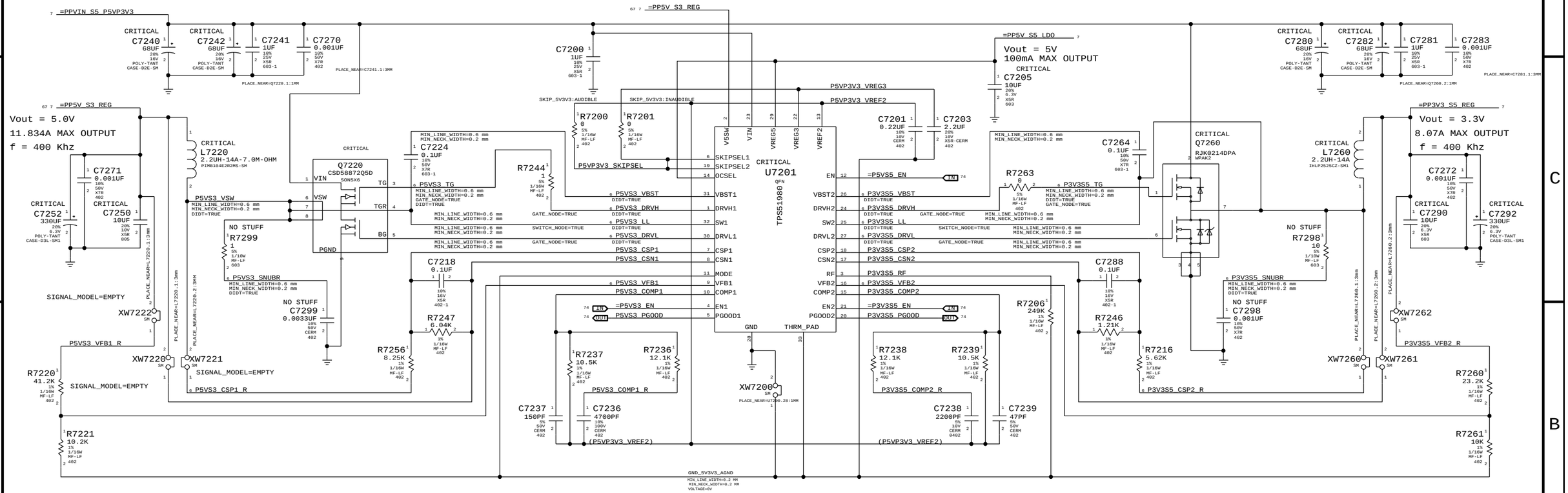
DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 71 OF 132

SHEET: 66 OF 105



SYNC_MASTER=J31_JACK	SYNC_DATE=11/09/2011
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 72 OF 132
	SHEET 67 OF 105

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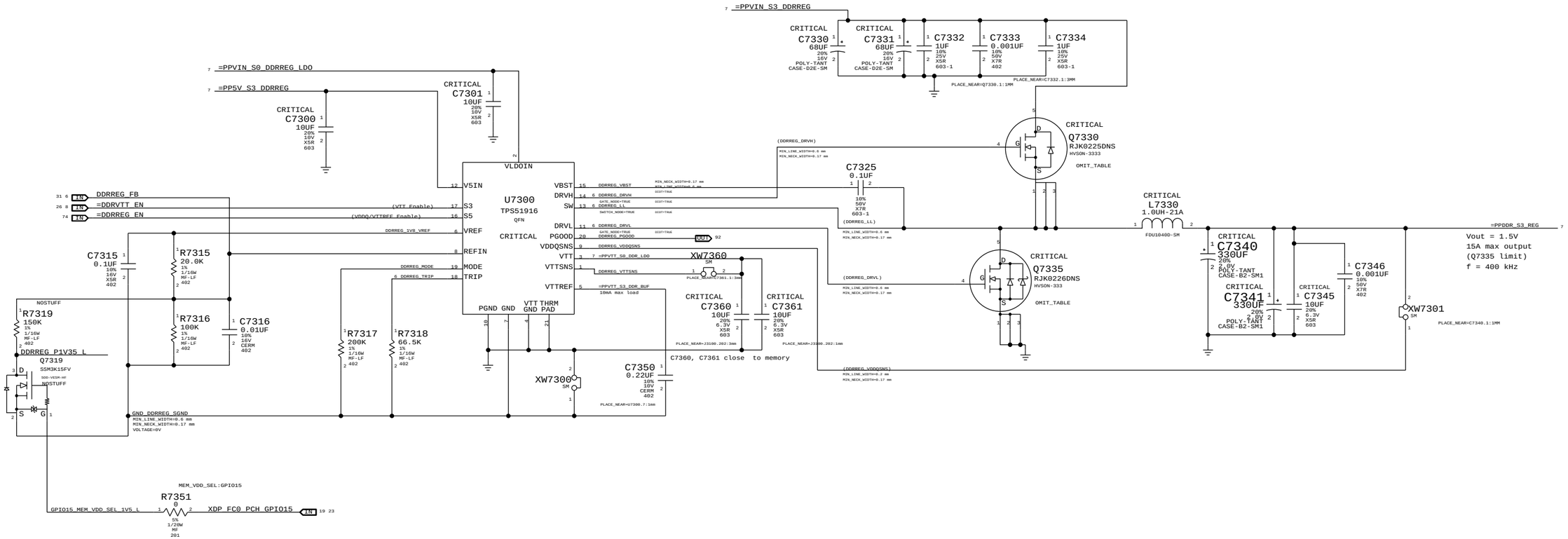


SYNC_MASTER=J31_JACK SYNC_DATE=07/07/2011

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

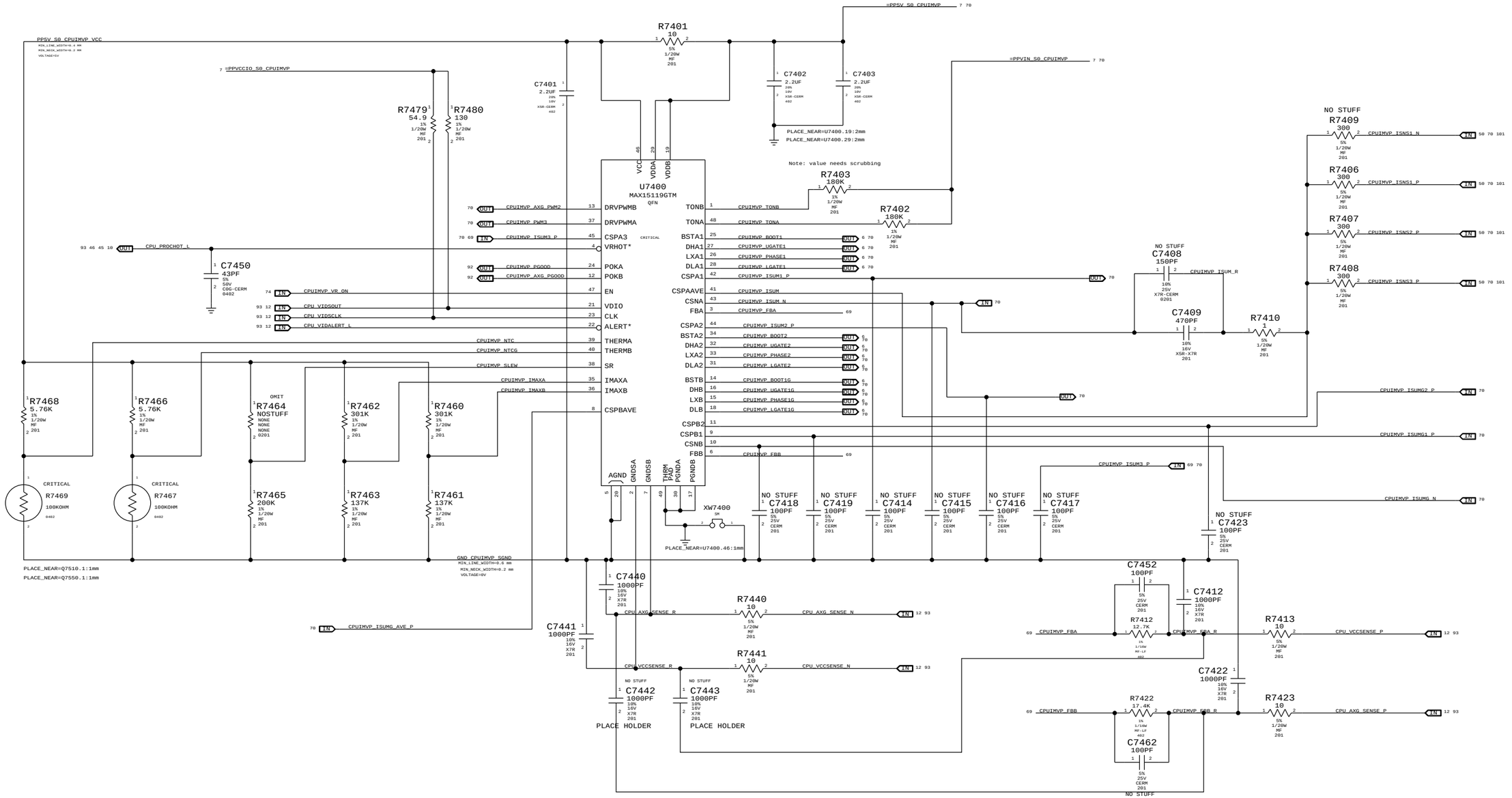
DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

PAGE 73 OF 132

SHEET 68 OF 105



SYNC_MASTER=J31_JACK	SYNC_DATE=11/11/2013
PAGE TITLE	CPU IMVP7 & AXG VCore Regulator
Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 74 OF 132
	SHEET 69 OF 105

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PHASE 1

PHASE 2

PHASE 3

AXG PHASE 1

AXG PHASE 2

Additonal Input Bulk Caps

SYNC_MASTER=J31_JACK	SYNC_DATE=11/11/2013
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 75 OF 132
	SHEET 70 OF 105

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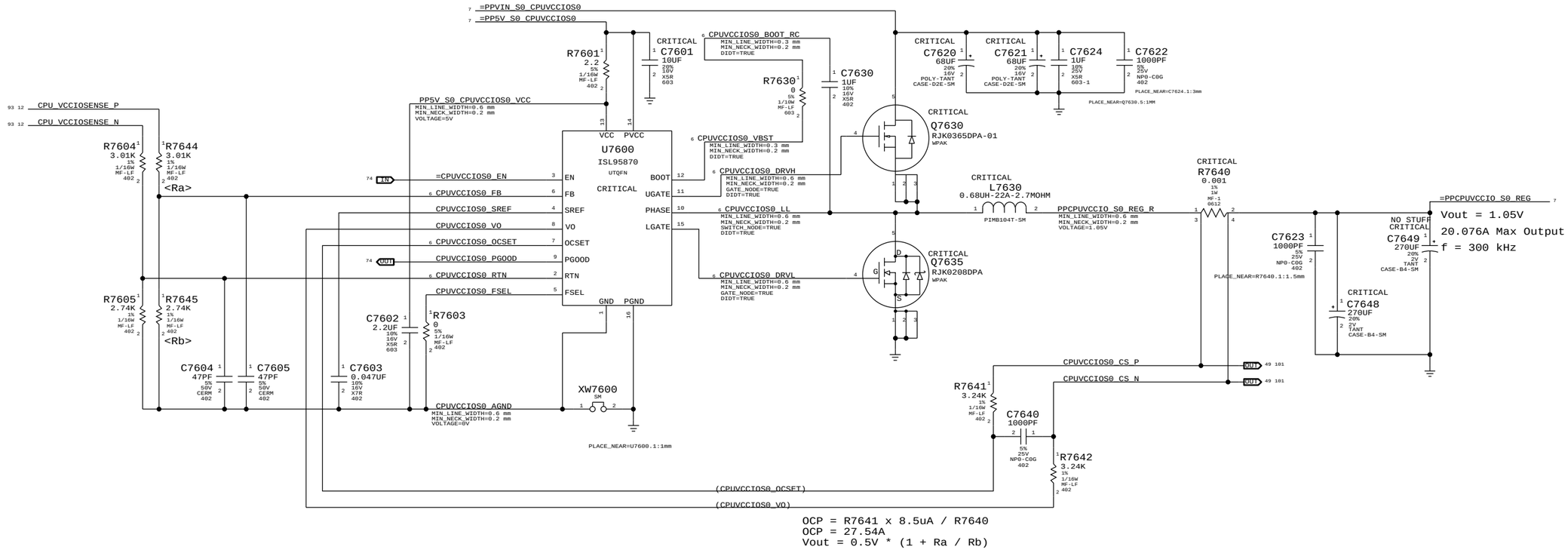
CPU VCCIO REGULATOR



OCP = R7641 x 8.5uA / R7640
OCP = 27.54A
Vout = 0.5V * (1 + Ra / Rb)

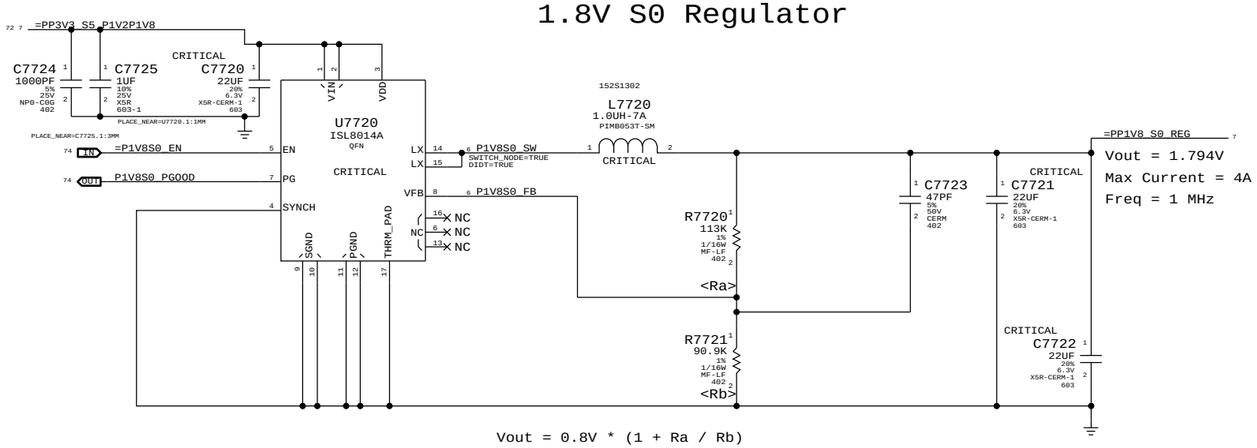
SYNC_MASTER=J31_JACK SYNC_DATE=09/19/2011

PAGE TITLE: CPU VCCIO (1V0R1V05 S0) POWER SUPPLY

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 76 OF 132
SHEET: 71 OF 105

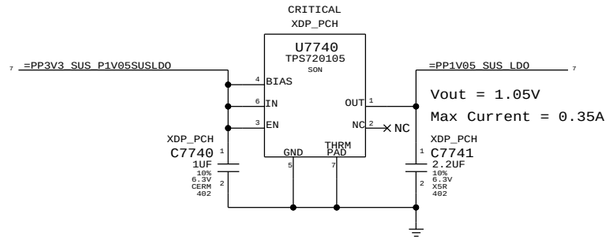
1.8V S0 Regulator



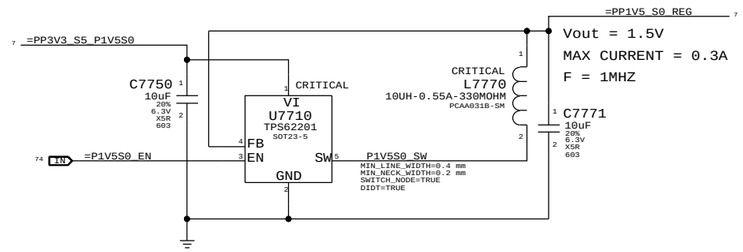
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

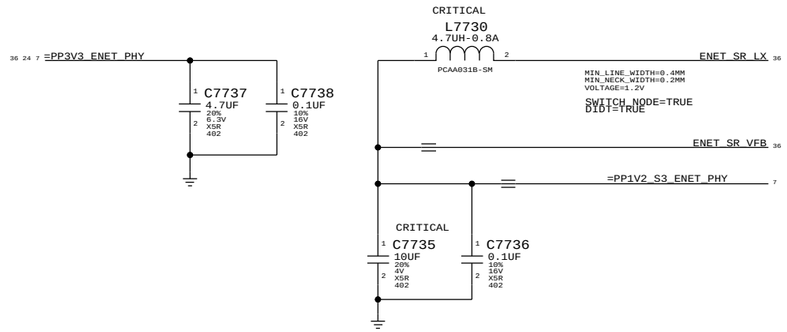
Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



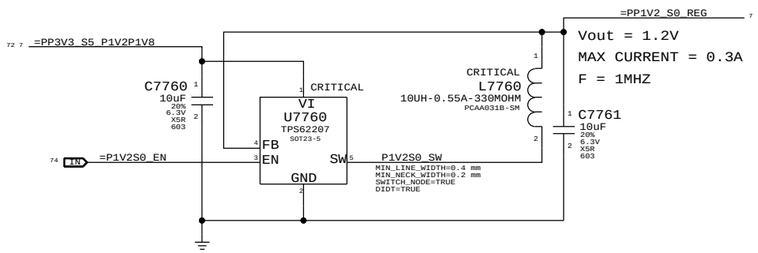
1.5V S0 Regulator



CAESAR IV 1.2V INT.VR CMPTS



1.2V S0 (GMUX) Regulator



SYNC_MASTER=J31_JACK SYNC_DATE=06/10/2011

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

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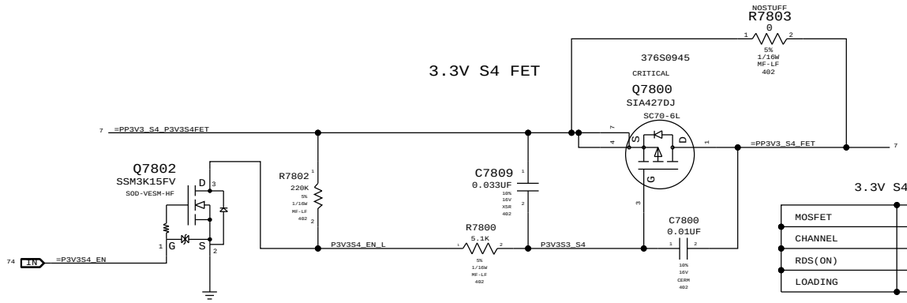
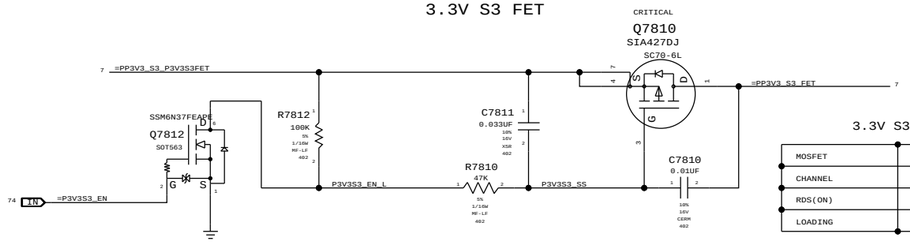
3.3V S4 FET



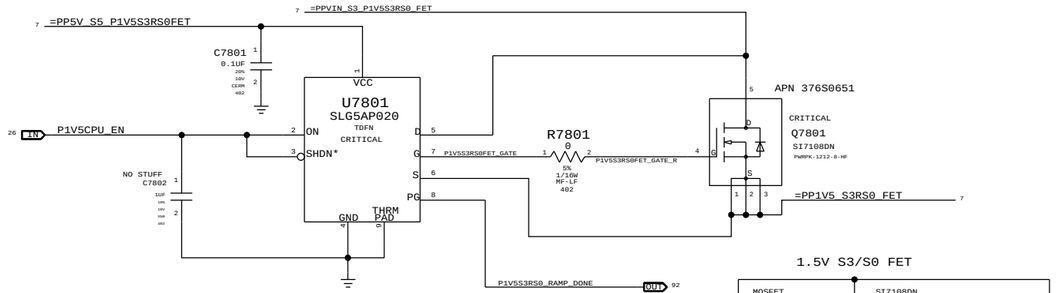
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



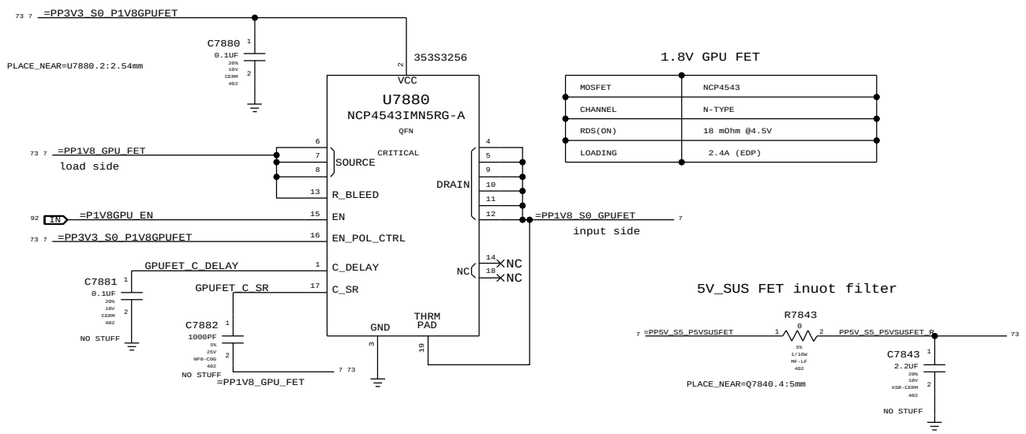
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

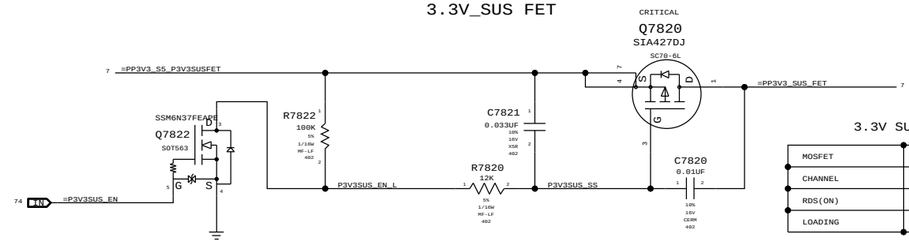


1.8V GPU FET	
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter

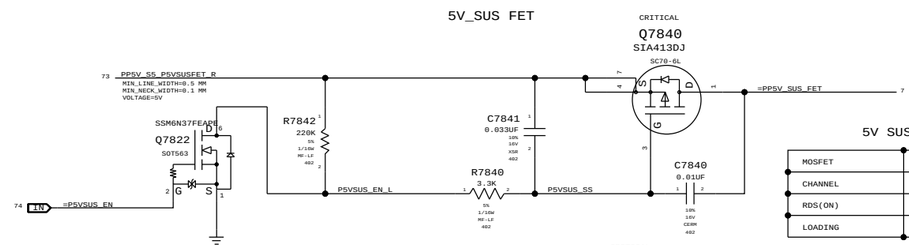
U7880 default Turn on delay EN--> on is 200~650us.

3.3V_SUS FET



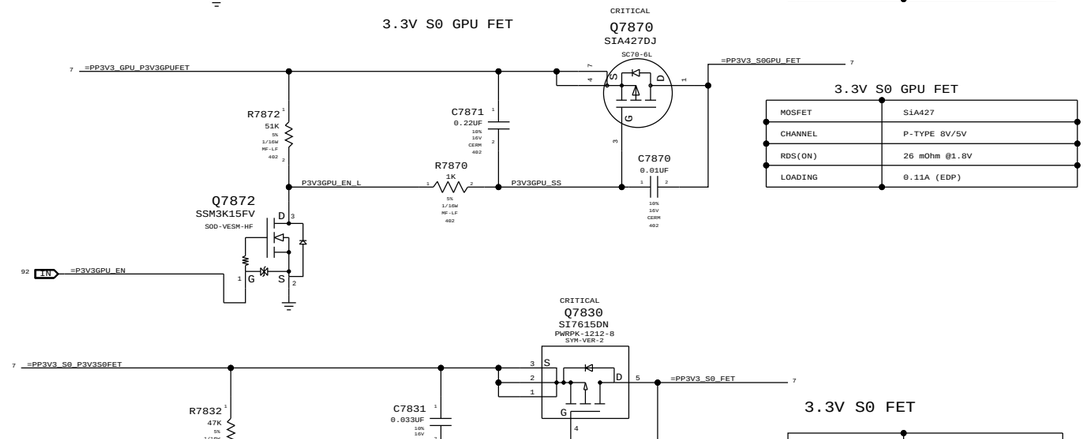
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



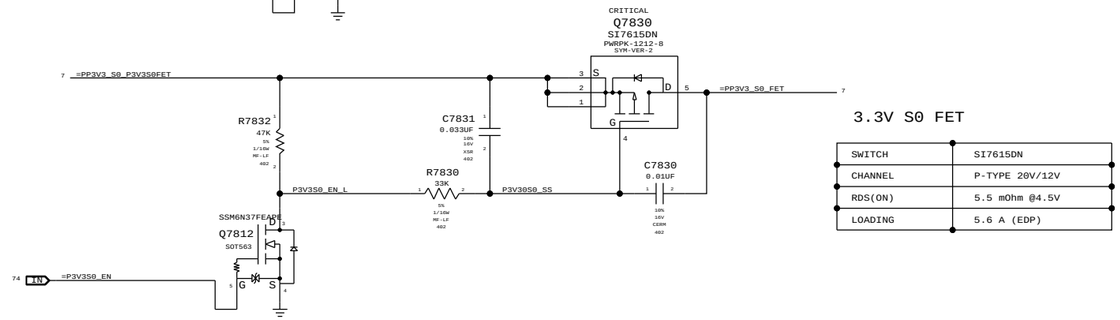
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 GPU FET



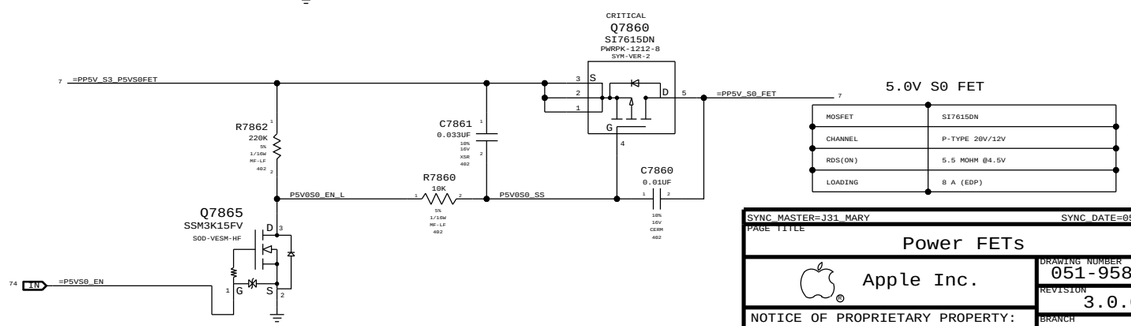
3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

3.3V S0 FET



3.3V S0 FET	
SWITCH	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC MASTER=J31_MARY
SYNC_DATE=05/05/2011
PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
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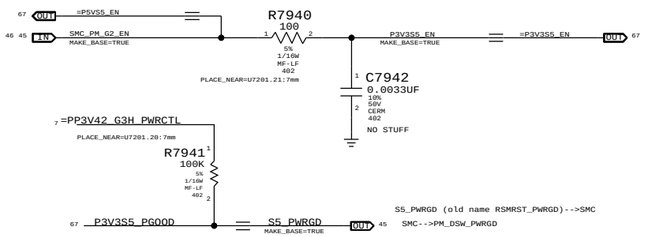
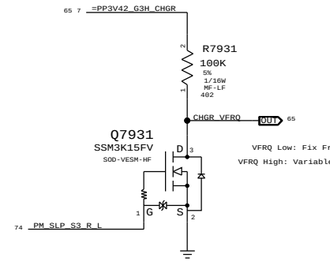
S5 Rail Enables & PGOOD

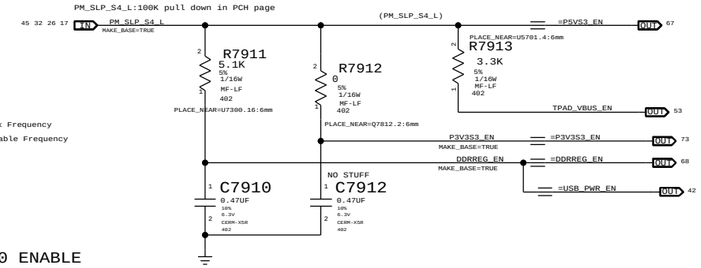


State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

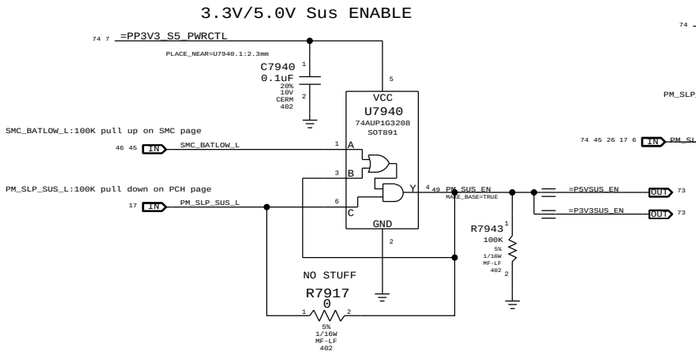
CHGR VFRQ Generation



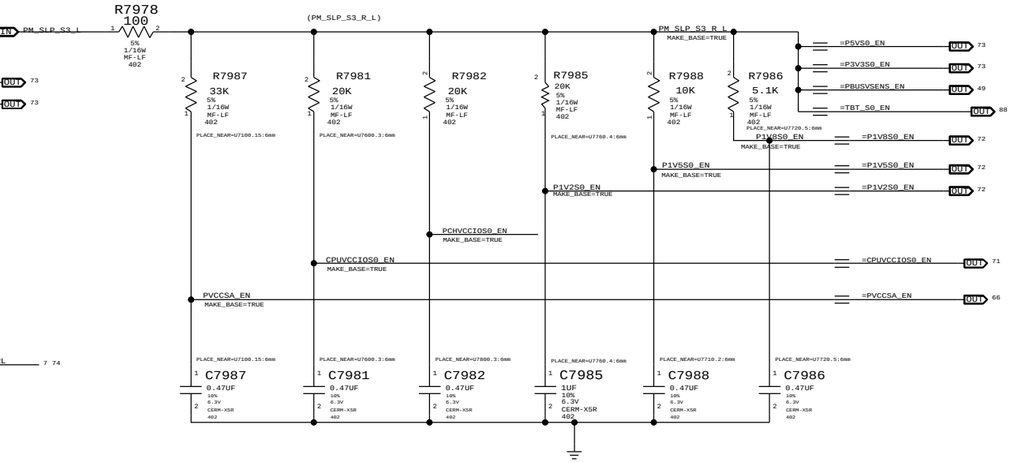
3.3V,5V S3 ENABLE



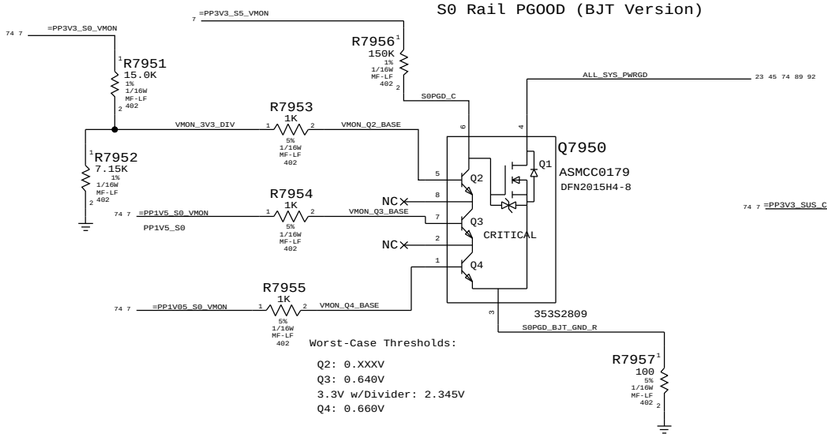
3.3V/5.0V Sus ENABLE



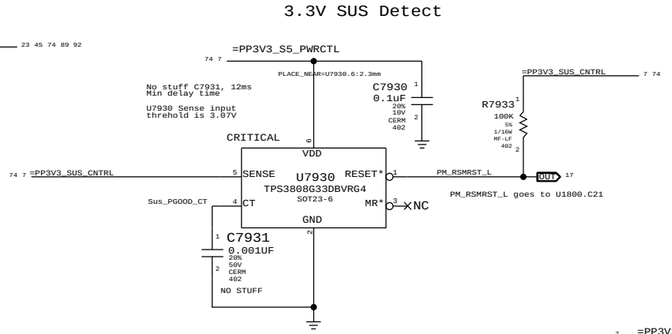
S0 ENABLE



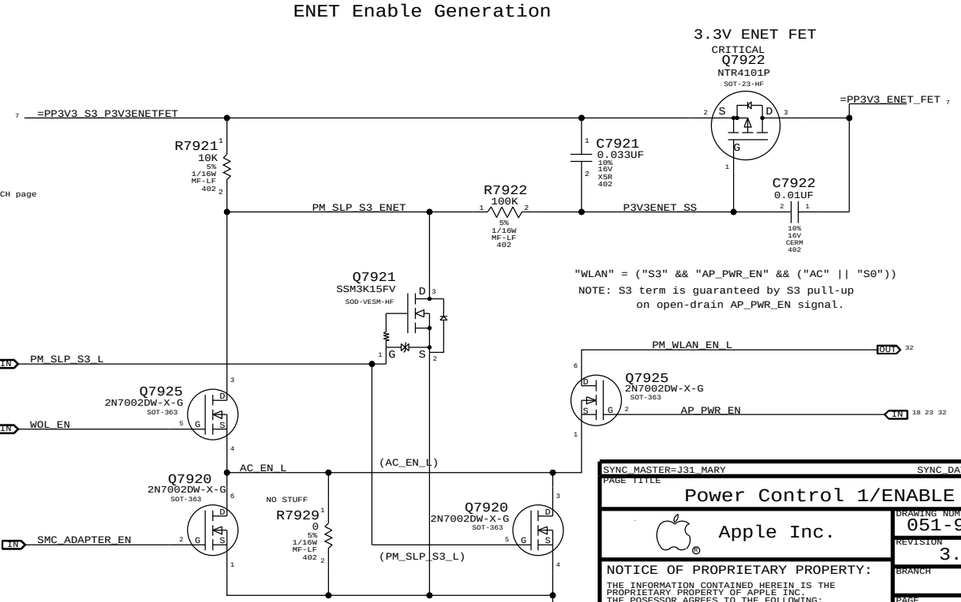
S0 Rail PGOOD (BJT Version)



3.3V SUS Detect

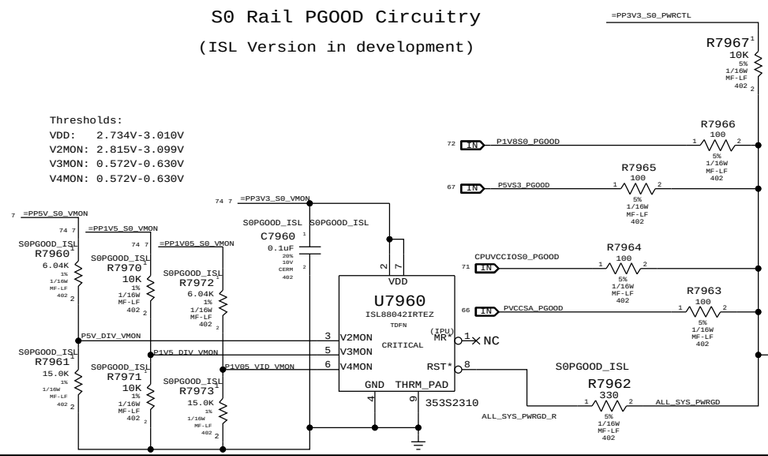


ENET Enable Generation

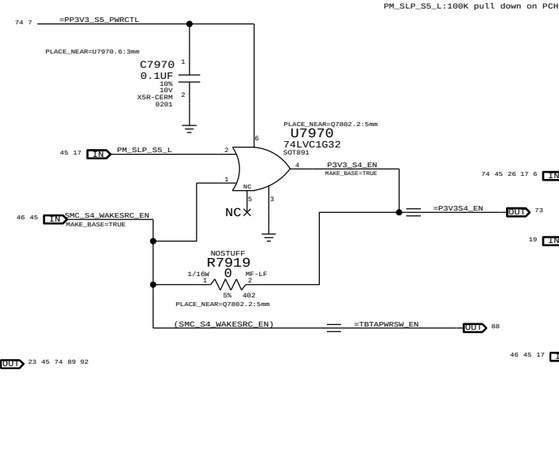


S0 Rail PGOOD Circuitry

(ISL Version in development)



3.3V/5.0V S4 ENABLE



Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Note: Removed GND voids from AC caps for layout (J31).

93 8	IN	PEG_R2D_C_P<0>	C8020	0.22UF	PEG_R2D_P<0>	6 75 92 93
93 8	IN	PEG_R2D_C_N<0>	C8021	0.22UF	PEG_R2D_N<0>	6 75 92 93
93 8	IN	PEG_R2D_C_P<1>	C8022	0.22UF	PEG_R2D_P<1>	6 75 93
93 8	IN	PEG_R2D_C_N<1>	C8023	0.22UF	PEG_R2D_N<1>	6 75 93
93 8	IN	PEG_R2D_C_P<2>	C8024	0.22UF	PEG_R2D_P<2>	6 75 93
93 8	IN	PEG_R2D_C_N<2>	C8025	0.22UF	PEG_R2D_N<2>	6 75 93
93 8	IN	PEG_R2D_C_P<3>	C8026	0.22UF	PEG_R2D_P<3>	6 75 92 93
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93 8	IN	PEG_R2D_C_P<4>	C8028	0.22UF	PEG_R2D_P<4>	6 75 93
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93 8	IN	PEG_R2D_C_P<6>	C8032	0.22UF	PEG_R2D_P<6>	6 75 93
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93 75 6		PEG_D2R_C_N<1>	C8058	0.22UF	PEG_D2R_N<1>	OUT 8 93
93 75 6		PEG_D2R_C_P<2>	C8059	0.22UF	PEG_D2R_P<2>	OUT 8 93
93 75 6		PEG_D2R_C_N<2>	C8060	0.22UF	PEG_D2R_N<2>	OUT 8 93
93 75 6		PEG_D2R_C_P<3>	C8061	0.22UF	PEG_D2R_P<3>	OUT 8 93
93 75 6		PEG_D2R_C_N<3>	C8062	0.22UF	PEG_D2R_N<3>	OUT 8 93
93 75 6		PEG_D2R_C_P<4>	C8063	0.22UF	PEG_D2R_P<4>	OUT 8 93
93 75 6		PEG_D2R_C_N<4>	C8064	0.22UF	PEG_D2R_N<4>	OUT 8 93
93 75 6		PEG_D2R_C_P<5>	C8065	0.22UF	PEG_D2R_P<5>	OUT 8 93
93 75 6		PEG_D2R_C_N<5>	C8066	0.22UF	PEG_D2R_N<5>	OUT 8 93
93 75 6		PEG_D2R_C_P<6>	C8067	0.22UF	PEG_D2R_P<6>	OUT 8 93
93 75 6		PEG_D2R_C_N<6>	C8068	0.22UF	PEG_D2R_N<6>	OUT 8 93
93 75 6		PEG_D2R_C_P<7>	C8069	0.22UF	PEG_D2R_P<7>	OUT 8 93
93 75 6		PEG_D2R_C_N<7>	C8070	0.22UF	PEG_D2R_N<7>	OUT 8 93

OMIT_TABLE

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93 92 75 6	PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0>	6 75 93
93 92 75 6	PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0>	6 75 93
93 75 6	PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1>	6 75 93
93 75 6	PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1>	6 75 93
93 92 75 6	PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2>	6 75 93
93 92 75 6	PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2>	6 75 93
93 92 75 6	PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3>	6 75 93
93 92 75 6	PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3>	6 75 93
93 75 6	PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4>	6 75 93
93 75 6	PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4>	6 75 93
93 92 75 6	PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5>	6 75 93
93 92 75 6	PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5>	6 75 93
93 75 6	PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6>	6 75 93
93 75 6	PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6>	6 75 93
93 92 75 6	PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7>	6 75 93
93 92 75 6	PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7>	6 75 93
NC		AP20	PEX_RX8	PEX_TX8	AK20	NC	
NC		AP21	PEX_RX8*	PEX_TX8*	AJ20	NC	
NC		AN21	PEX_RX9	PEX_TX9	AH20	NC	
NC		AM21	PEX_RX9*	PEX_TX9*	AG20	NC	
NC		AN23	PEX_RX10	PEX_TX10	AK21	NC	
NC		AM23	PEX_RX10*	PEX_TX10*	AJ21	NC	
NC		AP23	PEX_RX11	PEX_TX11	AL22	NC	
NC		AP24	PEX_RX11*	PEX_TX11*	AK22	NC	
NC		AN24	PEX_RX12	PEX_TX12	AK23	NC	
NC		AM24	PEX_RX12*	PEX_TX12*	AJ23	NC	
NC		AN26	PEX_RX13	PEX_TX13	AH23	NC	
NC		AM26	PEX_RX13*	PEX_TX13*	AG23	NC	
NC		AP26	PEX_RX14	PEX_TX14	AK24	NC	
NC		AP27	PEX_RX14*	PEX_TX14*	AJ24	NC	
NC		AN27	PEX_RX15	PEX_TX15	AL25	NC	
NC		AM27	PEX_RX15*	PEX_TX15*	AK25	NC	

=PP3V3_GPU_VDD33 (83 82 81 7) — R8001 10K 1% 1/20W MF 201 — PEX_CLKREQ_L_R (82 75)

NOSTUFF R8002 200 1% 1/20W MF 201 — 96 PEX_TSTCLK_O_P

96 16 IN PEG_CLK100M_P → AL13 PEX_REFCLK
96 16 IN PEG_CLK100M_N → AK13 PEX_REFCLK*
PEX_TSTCLK_OUT AJ26 — PEX_TSTCLK_OUT* AK26 — 96 PEX_TSTCLK_O_N

R8000 0 MF 5% 1/20W 201: GPU_RESET_L (82 8 IN) — GPU_RESET_R_L → AJ12 PEX_RST*

PEX_TERMP AP29 — R8005 2.49K 1% 1/20W MF 201 — GPU_PEX_TERMP

82 75 OUT PEX_CLKREQ_L_R → AK12 PEX_CLKREQ*

PEX_SVDD_3V3 AG12 — PP3V3_GPU_PEX_PLL_HVDD (83)

NC → AJ11 PEX_WAKE*

SYNC_MASTER=J31_SREE	SYNC_DATE=10/25/2013
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Apple Inc.	DRAWING NUMBER 051-9585 · SIZE D
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	BRANCH
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=PP1V35_GPU_FBVDDQ
80 79 76 7

=PP1V35_GPU_FBVDDQ
7 76 79 80

AA27 AA30 AB27 AB33 AC27 AD27 AE27 AF27 AG27 B13 B16 B19 E13 E16 E19 H10 H11 H12 H13 H14 H15 H16

FBVDDQ FBVDDQ

H18 H19 H20 H21 H22 H23 H24 H8 H9 L27 M27 N27 P27 R27 T27 T30 T33 V27 W27 W30 W33 Y27

OMIT_TABLE

U8000
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BGA
(10 OF 10)

=PPVCORE_GPU
83 76 7

=PPVCORE_GPU
7 76 83

AA12 AA14 AA16 AA19 AA21 AA23 AB13 AB15 AB17 AB18 AB20 AB22 AC12 AC14 AC16 AC19 AC21 AC23 M12 M14 M16 M19 M21 M23 N13 N15 N17 N18 N20 N22 P12 P14 P16 P19 P21 P23 R13 R15 R17 R18 R20 R22 T12 T14 T16 T19 T21 T23 U13 U15 U17 U18 U20 U22 V13 V15

VDD

V17 V18 V20 V22 W12 W14 W16 W19 W21 W23 Y13 Y15 Y17 Y18 Y20 Y22

VDD

XVDD

U1 U2 U3 U4 U5 U6 U7 U8 V1 V2 V3 V4 V5 V6 V7 V8 W2 W3 W4 W5 W7 W8 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8

NC

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PPVSS_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

=PPVCORE_GPU
83 76 7

EDP = 30 A

GPUDEC:NORMAL	GPUDEC:NORMAL CRITICAL	GPUDEC:NORMAL CRITICAL	GPUDEC:EXP CRITICAL	GPUDEC:EXP CRITICAL	GPUDEC:EXP CRITICAL	GPUDEC:EXP CRITICAL	NOSTUFF CRITICAL	NOSTUFF CRITICAL		
C8161 47UF 20% 6.3V X5R-CERM 0805	C8198 22UF 20% 6.3V X5R 0603	C8199 22UF 20% 6.3V X5R 0603	C8162 22UF 20% 4V X5R 402	C8163 22UF 20% 4V X5R 402	C8164 22UF 20% 4V X5R 402	C8165 22UF 20% 4V X5R 402	C8182 22UF 20% 4V X5R 402	C8183 22UF 20% 4V X5R 402	C8166 10UF 20% 10V X5R-CERM 0402-1	C8167 10UF 20% 10V X5R-CERM 0402-1

GPUDEC:EXP CRITICAL	GPUDEC:EXP CRITICAL	GPUDEC:EXP CRITICAL	GPUDEC:EXP CRITICAL	NOSTUFF CRITICAL	NOSTUFF CRITICAL	NOSTUFF CRITICAL	GPUDEC:NORMAL CRITICAL	GPUDEC:NORMAL CRITICAL	GPUDEC:NORMAL CRITICAL	GPUDEC:NORMAL CRITICAL
C8145 22UF 20% 4V X5R 402	C8146 22UF 20% 4V X5R 402	C8147 22UF 20% 4V X5R 402	C8148 22UF 20% 4V X5R 402	C8149 22UF 20% 4V X5R 402	C8150 22UF 20% 4V X5R 402	C8151 22UF 20% 4V X5R 402	C8130 22UF 20% 6.3V X5R 0603	C8131 22UF 20% 6.3V X5R 0603	C8132 22UF 20% 6.3V X5R 0603	C8133 22UF 20% 6.3V X5R 0603

C8168 10UF 20% 10V X5R-CERM 0402-1	C8169 10UF 20% 10V X5R-CERM 0402-1	C8170 10UF 20% 10V X5R-CERM 0402-1	C8171 10UF 20% 10V X5R-CERM 0402-1	C8172 10UF 20% 10V X5R-CERM 0402-1	C8173 10UF 20% 10V X5R-CERM 0402-1	C8174 10UF 20% 10V X5R-CERM 0402-1	C8175 10UF 20% 10V X5R-CERM 0402-1	C8176 10UF 20% 10V X5R-CERM 0402-1	C8177 10UF 20% 10V X5R-CERM 0402-1

C8178 10UF 20% 10V X5R-CERM 0402-1	C8179 10UF 20% 10V X5R-CERM 0402-1	C8180 10UF 20% 10V X5R-CERM 0402-1	C8181 10UF 20% 10V X5R-CERM 0402-1	C8184 10UF 20% 10V X5R-CERM 0402-1	C8185 10UF 20% 10V X5R-CERM 0402-1	C8186 1UF 20% 6.3V X5R 0201	C8187 1UF 20% 6.3V X5R 0201	C8188 1UF 20% 6.3V X5R 0201	C8189 1UF 20% 6.3V X5R 0201

C8190 1UF 20% 6.3V X5R 0201	C8191 0.1UF 10% 6.3V X5R 201	C8192 0.1UF 10% 6.3V X5R 201	C8193 0.1UF 10% 6.3V X5R 201	C8194 0.1UF 10% 6.3V X5R 201	C8195 0.1UF 10% 6.3V X5R 201	C8196 1000PF 10% 16V X7R-CERM 0201	C8197 1000PF 10% 16V X7R-CERM 0201

GPU VCORE DE-COUPLING

NOTE: ATLEAST 2 GND VIAS & 2 POWER VIAS PER CAP

=PP1V35_GPU_FBVDDQ
80 79 76 7

GPU FB DE-COUPLING

EDP = 6500 MA

C8125 22UF 20% 4V X5R 402	C8126 22UF 20% 4V X5R 402	C8127 22UF 20% 4V X5R 402	C8128 22UF 20% 4V X5R 402	C8101 10UF 20% 4V X5R 402	C8102 10UF 20% 4V X5R 402	C8103 10UF 20% 4V X5R 402	C8104 10UF 20% 4V X5R 402

C8105 4.7UF 20% 6.3V X5R-CERM1 402	C8106 4.7UF 20% 6.3V X5R-CERM1 402	C8107 4.7UF 20% 6.3V X5R-CERM1 402	C8108 4.7UF 20% 6.3V X5R-CERM1 402	C8109 4.7UF 20% 6.3V X5R-CERM1 402	C8110 4.7UF 20% 6.3V X5R-CERM1 402	C8111 1UF 20% 6.3V X5R 0201	C8112 1UF 20% 6.3V X5R 0201	C8113 1UF 20% 6.3V X5R 0201	C8114 1UF 20% 6.3V X5R 0201

C8115 0.1UF 10% 6.3V X5R 201	C8118 0.1UF 10% 6.3V X5R 201	C8119 0.1UF 10% 6.3V X5R 201	C8120 0.1UF 10% 6.3V X5R 201	C8121 0.1UF 10% 6.3V X5R 201	C8122 0.1UF 10% 6.3V X5R 201	C8123 0.1UF 10% 6.3V X5R 201	C8124 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=D2_MLB_2P SYNC_DATE=01/18/2013

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KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

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MEM INTERFACE A

FBA_D0 L28
FBA_D1 M29
FBA_D2 L29
FBA_D3 M28
FBA_D4 N31
FBA_D5 P29
FBA_D6 R29
FBA_D7 P28
FBA_D8 J28
FBA_D9 H29
FBA_D10 J29
FBA_D11 H28
FBA_D12 G29
FBA_D13 E31
FBA_D14 E32
FBA_D15 F30
FBA_D16 C34
FBA_D17 D32
FBA_D18 B33
FBA_D19 C33
FBA_D20 F33
FBA_D21 F32
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FBA_D23 H32
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FBA_D61 AG34
FBA_D62 AG32
FBA_D63 AG33

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FBA_WCK45* AG31
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FBA_WCK67* AK34
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FBA_WCKB67 AJ32
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FBA_CMD1 T31
FBA_CMD2 U29
FBA_CMD3 R34
FBA_CMD4 R33
FBA_CMD5 U32
FBA_CMD6 U33
FBA_CMD7 U28
FBA_CMD8 V28
FBA_CMD9 V29
FBA_CMD10 V30
FBA_CMD11 U34
FBA_CMD12 U31
FBA_CMD13 V34
FBA_CMD14 V33
FBA_CMD15 Y32
FBA_CMD16 AA31
FBA_CMD17 AA29
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FBA_CMD24 Y29
FBA_CMD25 W31
FBA_CMD26 Y30
FBA_CMD27 AA34
FBA_CMD28 Y31
FBA_CMD29 Y34
FBA_CMD30 Y33
FBA_CMD31 V31

FBA_CLK0 R30
FBA_CLK0* R31
FBA_CLK1 AB31
FBA_CLK1* AC31

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FBA_DQM1 F31
FBA_DQM2 F34
FBA_DQM3 M32
FBA_DQM4 AD31
FBA_DQM5 AL29
FBA_DQM6 AM32
FBA_DQM7 AF34

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FBA_DQS_RN5 AK31 NC
FBA_DQS_RN6 AM34 NC
FBA_DQS_RN7 AF32 NC

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FBA_DQS_WP1 G31
FBA_DQS_WP2 E33
FBA_DQS_WP3 M33
FBA_DQS_WP4 AE31
FBA_DQS_WP5 AK30
FBA_DQS_WP6 AN33
FBA_DQS_WP7 AF33

FBA_DLL_AVDD K27 PP1V05_GPU_FB_DLL_AVDD 77
FBA_PLL_AVDD U27 PP1V05_GPU_FB_PLL_AVDD 77

FBA_DEBUG R28 GPU_FBA_DEBUG0
FBA_DEBUG AC28 GPU_FBA_DEBUG1

FBA_CAL_PD_VDDQ J27 FB_CAL_PD_VDDQ 77
FBA_CAL_PU_GND H27 FB_CAL_PU_GND 77
FBA_CAL_TERM_GND H25 FB_CAL_TERM_GND
R8201 60.4 1% 1/20W MF 201 PLACE_NEAR=U8000.H25:8.4MM

FBA_CLAMP E1 FB_CLAMP
R8261 10K 1% 1/20W MF 201

FBA_CMD_RFU R32 NC
FBA_CMD_RFU AC32 NC

FB_VDDQ_SENSE F1 GPU_FBVDDQ_SENSE_P OUT 78 101
FB_GND_SENSE F2 GPU_FBVDDQ_SENSE_N OUT 78 101

PLACE CLOSE TO BGA

77 FB_CAL_PU_GND
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R8205 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.J27:8.4MM
FB_CAL_PD_VDDQ 77

100 79 77 FB_A0_RESET_L
R8250 10K 1% 1/20W MF 201
100 79 77 FB_A1_RESET_L
R8251 10K 1% 1/20W MF 201

FB_A0_CKE_L 77 79 100
R8252 10K 1% 1/20W MF 201
FB_A1_CKE_L 77 79 100
R8253 10K 1% 1/20W MF 201

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NOSTUFF R8258 1.33K 1% 1/20W MF 201 PLACE_NEAR=U8000.H26:8.4MM
FB_VREF 77
NOSTUFF R8259 1.33K 1% 1/20W MF 201
NOSTUFF C8260 0.1UF 10% 6.3V X5R 201 PLACE_NEAR=U8000.H26:8.4MM
FB VREF GEN (TEST ONLY)

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R8203 60.4 1% 1/20W MF 201
R8202 60.4 1% 1/20W MF 201
R8270 100 1% 1/20W MF 201
R8271 100 1% 1/20W MF 201

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MEM INTRERFACE B

FBB_D0 G9
FBB_D1 E9
FBB_D2 G8
FBB_D3 F9
FBB_D4 F11
FBB_D5 G11
FBB_D6 F12
FBB_D7 G12
FBB_D8 G6
FBB_D9 F5
FBB_D10 E6
FBB_D11 F6
FBB_D12 F4
FBB_D13 G4
FBB_D14 E2
FBB_D15 F3
FBB_D16 C2
FBB_D17 D4
FBB_D18 D3
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FBB_D27 B11
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FBB_D29 A8
FBB_D30 C8
FBB_D31 B8
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FBB_D33 G23
FBB_D34 E24
FBB_D35 G24
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FBB_D37 E21
FBB_D38 G21
FBB_D39 F21
FBB_D40 G27
FBB_D41 D27
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FBB_D46 E30
FBB_D47 D30
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FBB_D49 C31
FBB_D50 C32
FBB_D51 B32
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FBB_D53 A29
FBB_D54 C29
FBB_D55 B29
FBB_D56 B21
FBB_D57 C23
FBB_D58 A21
FBB_D59 C21
FBB_D60 B24
FBB_D61 C24
FBB_D62 B26
FBB_D63 C26

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FBB_WCK01* E8
FBB_WCK23 A5
FBB_WCK23* A6
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FBB_WCK45* D25
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FBB_WCK67* C27
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FBB_WCKB01* D7
FBB_WCKB23 C6
FBB_WCKB23* B6
FBB_WCKB45 F26
FBB_WCKB45* E26
FBB_WCKB67 A26
FBB_WCKB67* A27

FBB_CMD0 D13
FBB_CMD1 E14
FBB_CMD2 F14
FBB_CMD3 A12
FBB_CMD4 B12
FBB_CMD5 C14
FBB_CMD6 B14
FBB_CMD7 G15
FBB_CMD8 F15
FBB_CMD9 E15
FBB_CMD10 D15
FBB_CMD11 A14
FBB_CMD12 D14
FBB_CMD13 A15
FBB_CMD14 B15
FBB_CMD15 C17
FBB_CMD16 D18
FBB_CMD17 E18
FBB_CMD18 F18
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FBB_CMD20 B20
FBB_CMD21 C18
FBB_CMD22 B18
FBB_CMD23 G18
FBB_CMD24 G17
FBB_CMD25 F17
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FBB_CMD27 A18
FBB_CMD28 D17
FBB_CMD29 A17
FBB_CMD30 B17
FBB_CMD31 E17

FBB_CLK0 D12
FBB_CLK0* E12
FBB_CLK1 E20
FBB_CLK1* F20

FBB_DQM0 E11
FBB_DQM1 E3
FBB_DQM2 A3
FBB_DQM3 C9
FBB_DQM4 F23
FBB_DQM5 F27
FBB_DQM6 C30
FBB_DQM7 A24

FBB_DQS_RN0 D9 NC
FBB_DQS_RN1 E4 NC
FBB_DQS_RN2 B2 NC
FBB_DQS_RN3 A9 NC
FBB_DQS_RN4 D22 NC
FBB_DQS_RN5 D28 NC
FBB_DQS_RN6 A30 NC
FBB_DQS_RN7 B23 NC

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FBB_DQS_WP1 D5
FBB_DQS_WP2 C3
FBB_DQS_WP3 B9
FBB_DQS_WP4 E23
FBB_DQS_WP5 E28
FBB_DQS_WP6 B30
FBB_DQS_WP7 A23

FBB_PLL_AVDD H17 77 PP1V05_GPU_FB_PLL_AVDD
FBB_DEBUG0 G14 GPU_FBB_DEBUG0 77
FBB_DEBUG1 G20 GPU_FBB_DEBUG1 77
FBB_VREF H26 FB_VREF 77
FBB_CMD_RFU0 C12 NC
FBB_CMD_RFU1 C20 NC

C8206 1UF 20% 6.3V X5R 0201
C8207 0.1UF 10% 6.3V X5R 201

=PP1V35_GPU_S0_FB 7 77
R8206 60.4 1% 1/20W MF 201
R8207 60.4 1% 1/20W MF 201
GPU_FBB_DEBUG0 77
GPU_FBB_DEBUG1 77

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_REG
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V05_GPU_PEX_IOVDD 7 77 83
L8201 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
PP1V05_GPU_FB_PLL_AVDD 77
C8201 22UF 20% 6.3V X5R-CERM2 0603
C8202 1UF 20% 6.3V X5R 0201
C8203 0.1UF 10% 6.3V X5R 201
FB PLL & DLL VDD

=PP1V05_GPU_PEX_IOVDD
L8202 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
PP1V05_GPU_FB_DLL_AVDD 77
C8208 22UF 20% 6.3V X5R-CERM2 0603
C8204 1UF 20% 6.3V X5R 0201
C8205 0.1UF 10% 6.3V X5R 201

100 80 77 FB_B0_RESET_L
R8254 10K 1% 1/20W MF 201
100 80 77 FB_B1_RESET_L
R8255 10K 1% 1/20W MF 201

FB_B0_CKE_L 77 80 100
R8256 10K 1% 1/20W MF 201
FB_B1_CKE_L 77 80 100
R8257 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH

80 79 FB_SW_LEG OUT
CRITICAL
Q8265 SSM3K15FV SOD-VESM-HF
GPU_ALT_VREF IN 82

SYNC_MASTER=J31_SREE SYNC_DATE=10/25/2013
PAGE TITLE
KEPLER FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER 051-9585
SIZE D
REVISION 3.0.0
BRANCH
PAGE 82 OF 132
SHEET 77 OF 105

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GPU FB SUPPLY

VOUT = 1.5V / 1.35V

11A MAX OUTPUT

F = 500 KHZ

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

GPU 1V05 SUPPLY

VOUT = 1.05V

5.3A MAX OUTPUT

F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=J31_JACK	SYNC_DATE=11/16/2011
PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 83 OF 132
	SHEET 78 OF 105

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

CK TERMINATION - A0

PLACE_NEAR=U8400.J11:8.4MM

R8401 40.2 1% 1/20W MF 201
R8402 40.2 1% 1/20W MF 201
C8490 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - A1

PLACE_NEAR=U8450.J11:8.4MM

R8451 40.2 1% 1/20W MF 201
R8452 40.2 1% 1/20W MF 201
C8491 0.01UF 10% 10V X5R-CERM 0201

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

PLACE CLOSE TO U8400

PLACE CLOSE TO U8450

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

SYNC_MASTER=J31_SREE	SYNC_DATE=10/25/2013
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 84 OF 132
	SHEET 79 OF 105

Page Notes

Power aliases required by this page:

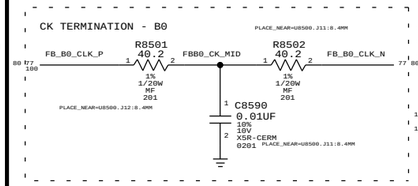
- =PP1V5R1V35_S0_FB_VDD

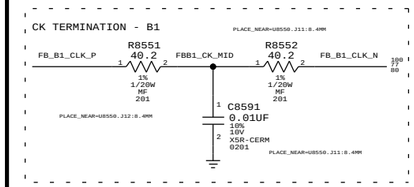
Signal aliases required by this page:

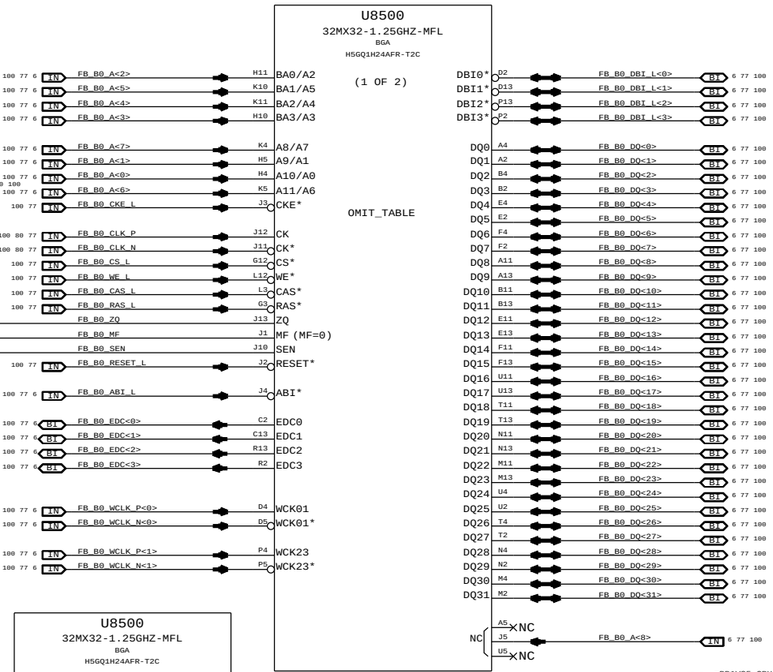
(NONE)

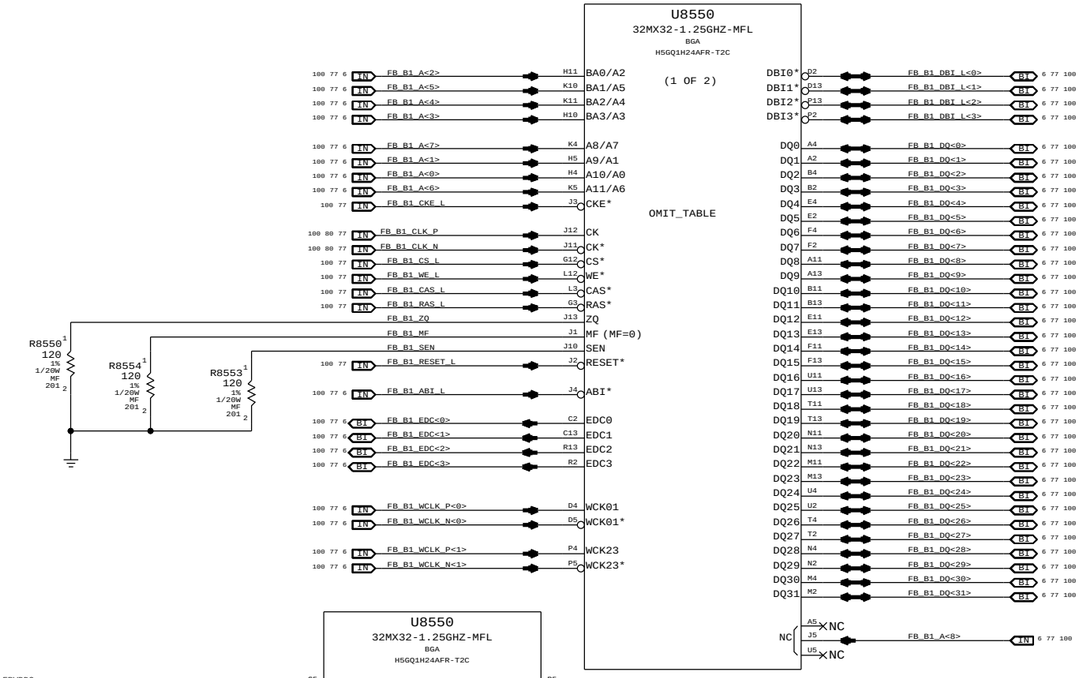
BOM options provided by this page:

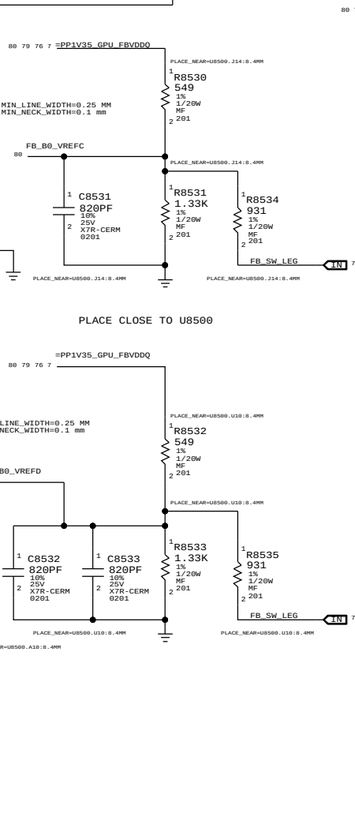
(NONE)

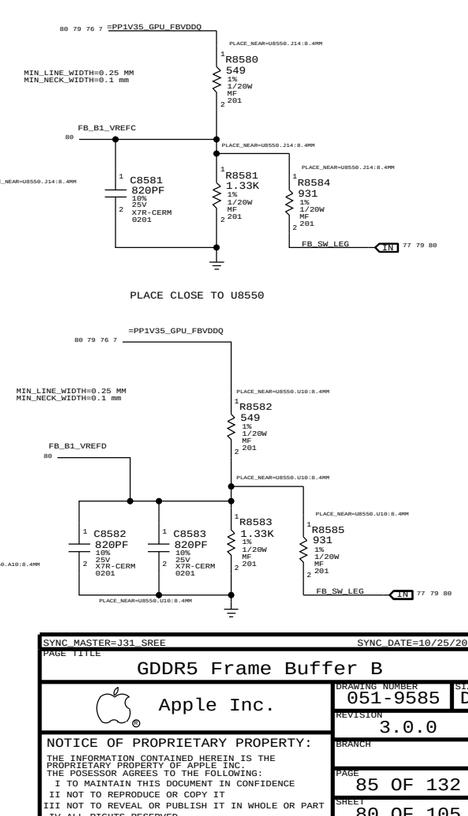












SYNC_MASTER=J31_SREE	SYNC_DATE=10/25/2013
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9585 SIZE D
	REVISION 3.0.0
	BRANCH
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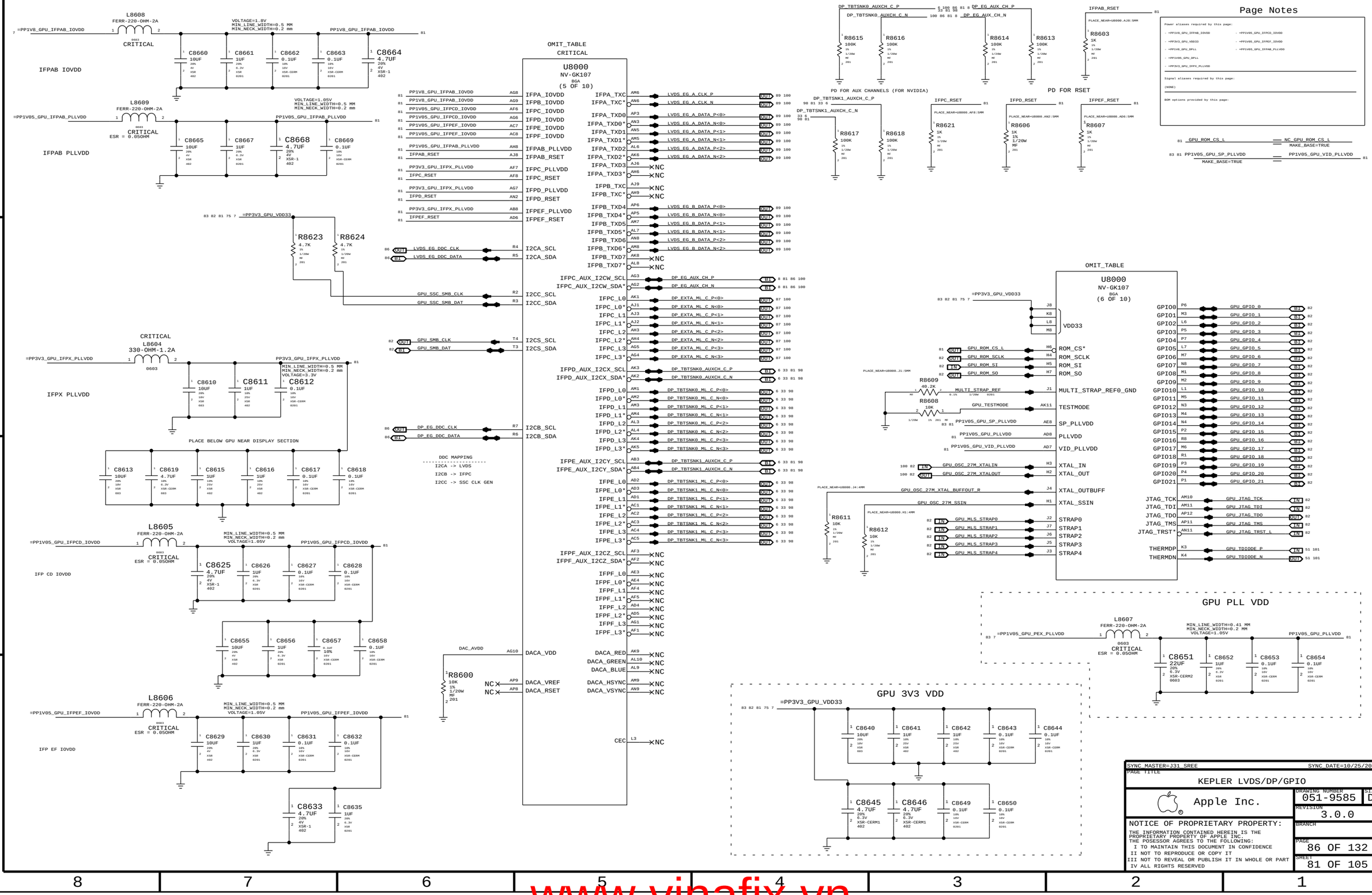
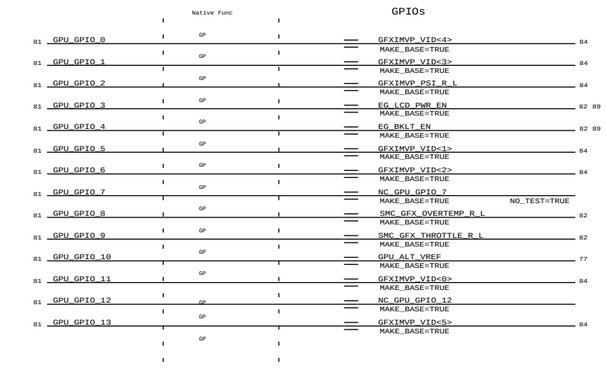
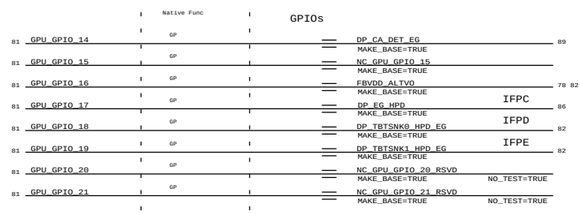
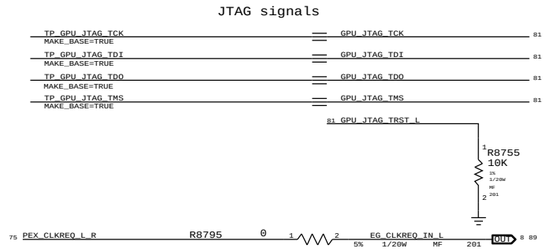
	SHEET 80 OF 105









STRAP NOTES:

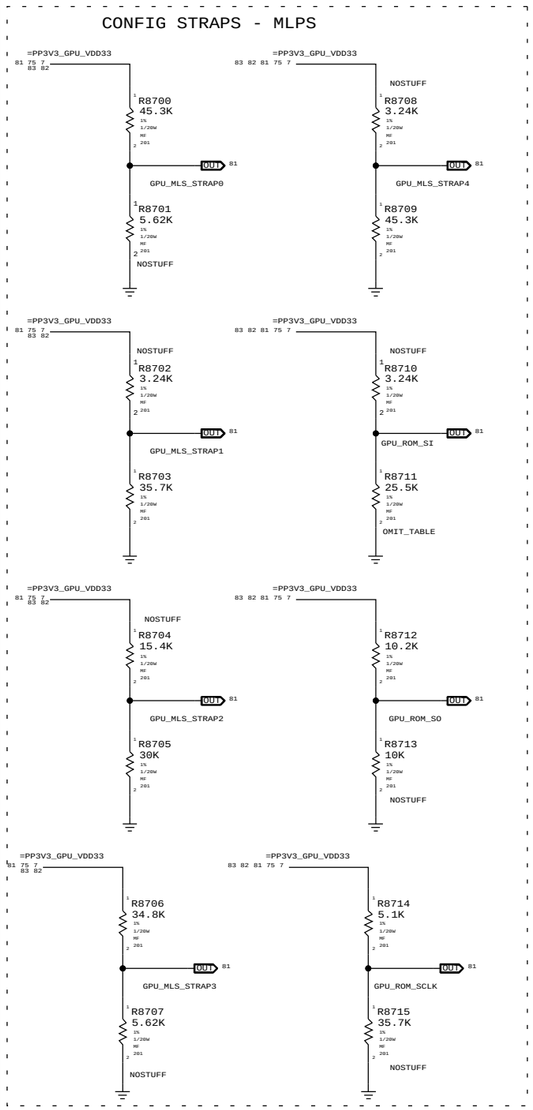
CURRENTLY STUFFED FOR GK107-GTX (R8705)

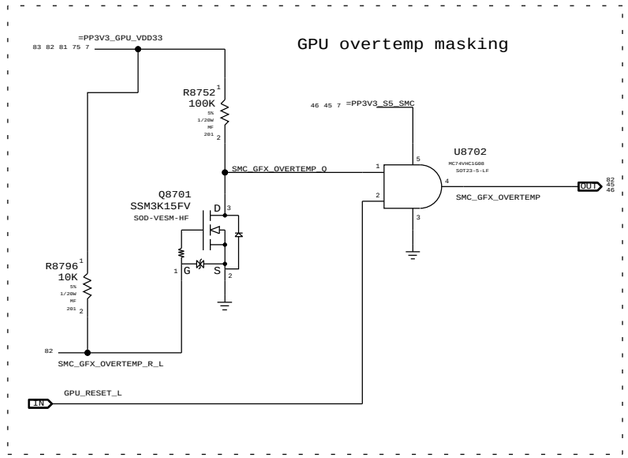
STUFF R8711 = 5KOHM FOR HYNIX 1GB - M die
STUFF R8711 = 10KOHM FOR SAMSUNG 1GB
STUFF R8711 = 15KOHM FOR HYNIX 512MB
STUFF R8711 = 20KOHM FOR SAMSUNG 512MB
STUFF R8711 = 24.9KOHM FOR HYNIX 1GB - A die

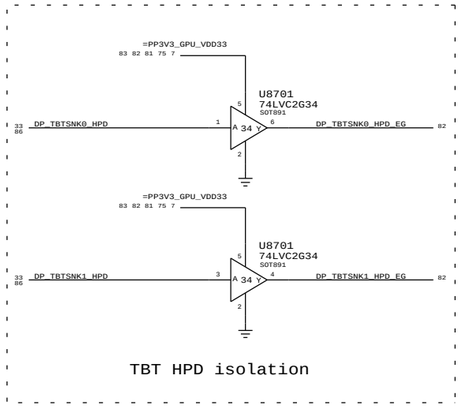
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0019	1	RES, 10.2KOHM, 0201	R8711	CRITICAL	FB_1G_SAMSUNG
118S0414	1	RES, 5.1KOHM, 0201	R8711	CRITICAL	FB_1G_HYNIX_M_DIE
118S0105	1	RES,15KOHM, 0201	R8711	CRITICAL	FB_512_HYNIX
118S0175	1	RES, 20KOHM, 0201	R8711	CRITICAL	FB_512_SAMSUNG
118S0230	1	RES, 24.9KOHM, 0201	R8711	CRITICAL	FB_1G_HYNIX_A_DIE

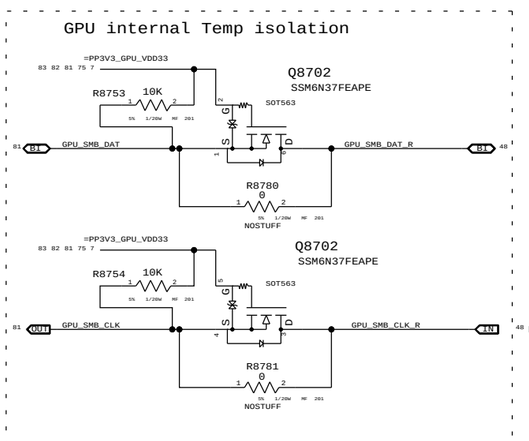
Strap values

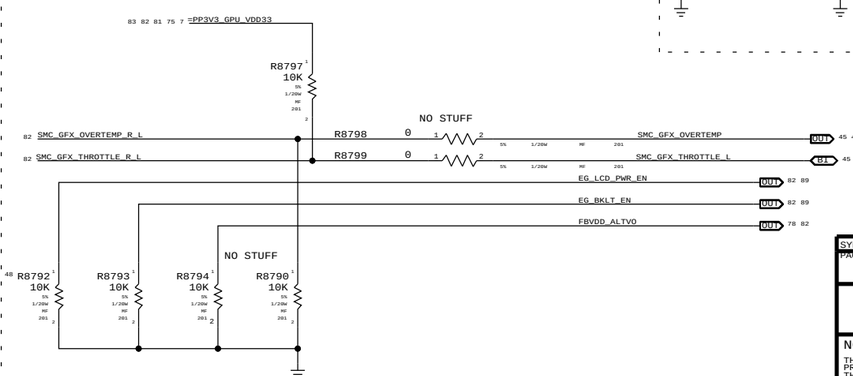
0x01
0x00
0x02
0x03
0x04

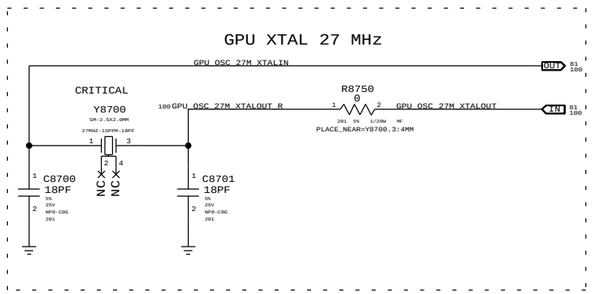












SYNC_MASTER=J31_SREE SYNC_DATE=11/16/2011

PAGE TITLE: KEPLER GPIOS,CLK & STRAPS

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
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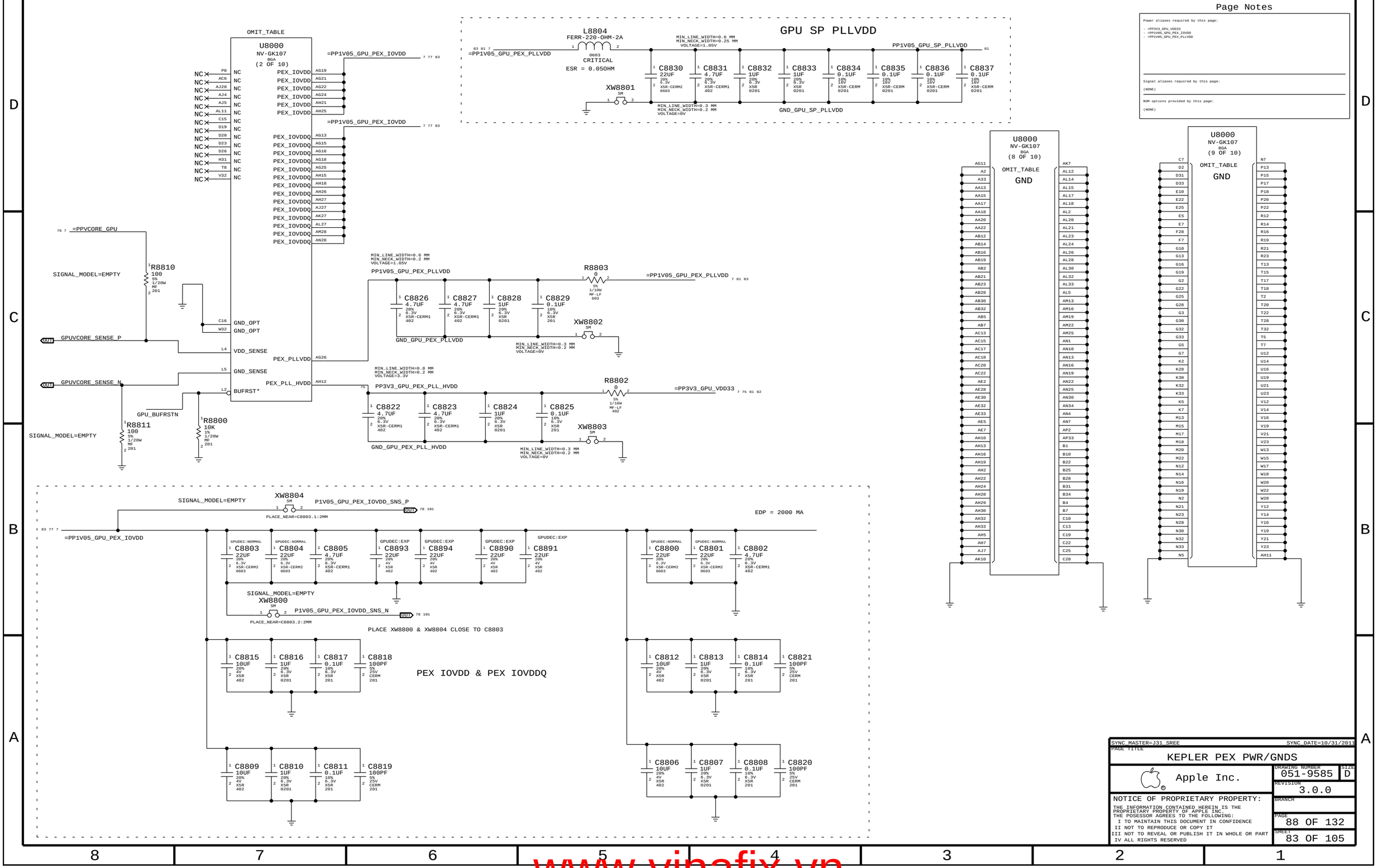

SYNC_MASTER=J31_SREE SYNC_DATE=10/31/2011

PAGE TITLE: KEPLER PEX PWR/GNDS

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 88 OF 132

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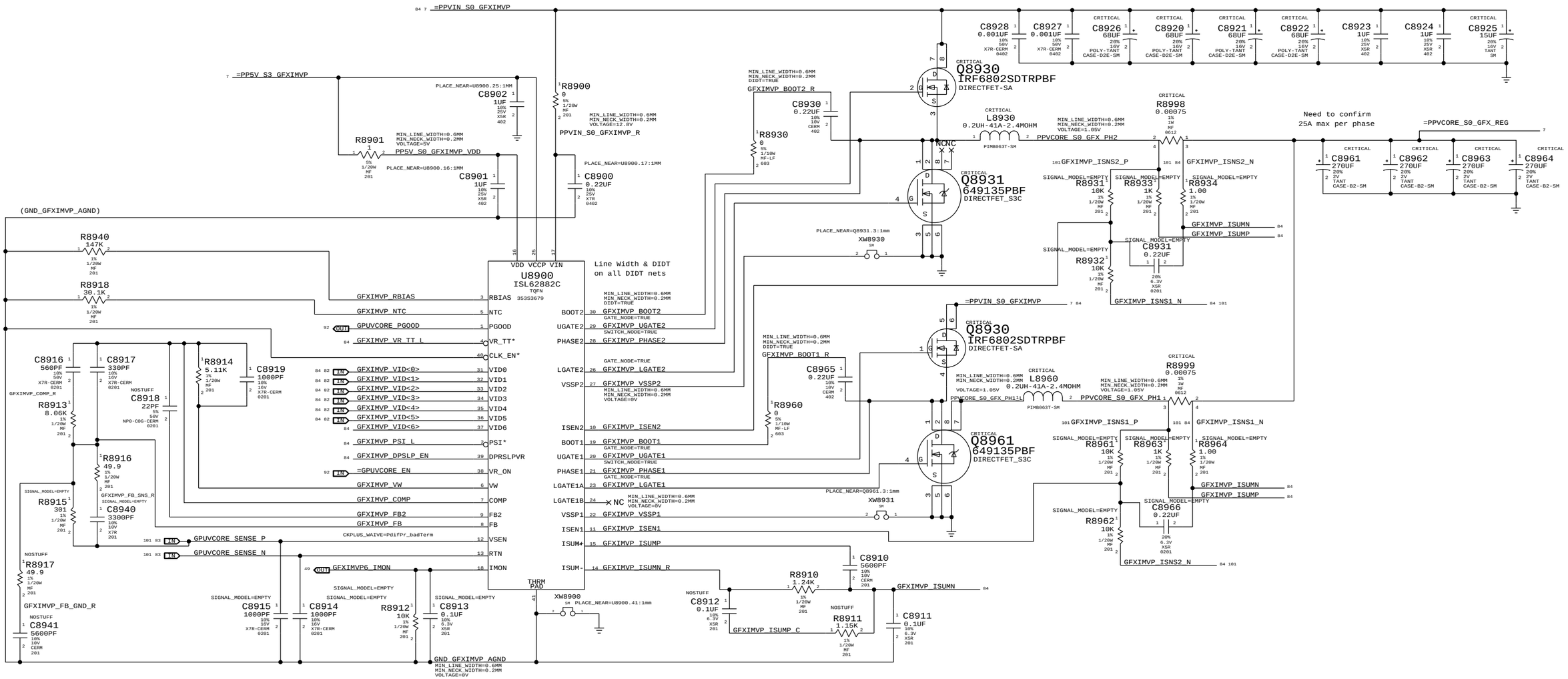

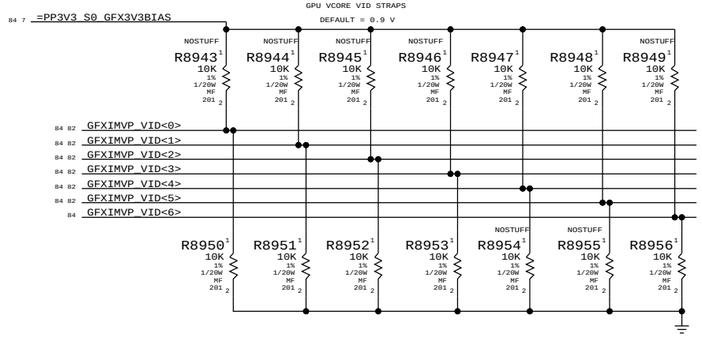

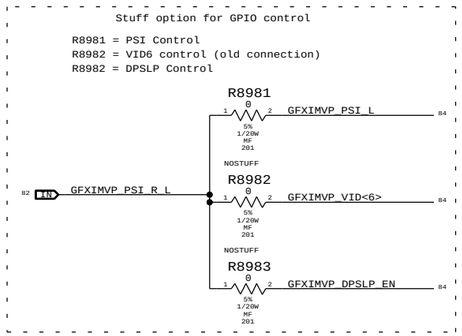

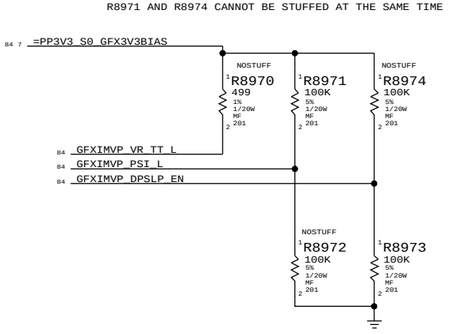

SYNC_MASTER=D2_MLB_2P SYNC_DATE=01/18/2012

PAGE TITLE

GFX IMVP VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

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LCD (LVDS) INTERFACE

89 LCD_PWR_EN

R9094 10K 5% 1/16W MF-LF 402

CRITICAL U9000 FPF1009 MFET-2X2-8IN
ON, VIN_1, VIN_2, VOUT_1, VOUT_2, GND, THRM PAD

7 =PP3V3_S5_LCD

C9009 0.1UF 10% 10V X5R 402-1

C9011 0.1UF 10% 16V X5R 402-1

C9012 10UF 20% 6.3V X5R 603

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

CRITICAL L9000 FERR-250-OHM SM

C9001 0.1UF 10% 16V X5R 402-1

C9002 0.001UF 10% 50V X7R 402

518S0852

CRITICAL J9000 20525-140E-01 F-RT-SM

7 =PP3V3_S0_DDC_LCD

R9010 100K 5% 1/16W MF-LF 402

R9011 100K 5% 1/16W MF-LF 402

100K pull-ups are for no-panel case (development).
Panel has 2K pull-ups

6 PP3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

86 6 LVDS_DDC_CLK
86 6 LVDS_DDC_DATA

C9010 0.001UF 10% 50V X7R 402

CRITICAL L9010 90-OHM-100MA DLP11S SYM_VER-1

100 86 LVDS_CONN_A_CLK_N
100 86 LVDS_CONN_A_CLK_P

Place close to the connector

CRITICAL L9011 90-OHM-100MA DLP11S SYM_VER-1

100 86 LVDS_CONN_B_CLK_N
100 86 LVDS_CONN_B_CLK_P

Place close to the connector

NC

100 86 6 LVDS_CONN_A_DATA_N<0>
100 86 6 LVDS_CONN_A_DATA_P<0>
100 86 6 LVDS_CONN_A_DATA_N<1>
100 86 6 LVDS_CONN_A_DATA_P<1>
100 86 6 LVDS_CONN_A_DATA_N<2>
100 86 6 LVDS_CONN_A_DATA_P<2>
100 6 LVDS_CONN_A_CLK_F_N
100 6 LVDS_CONN_A_CLK_F_P
100 86 6 LVDS_CONN_B_DATA_N<0>
100 86 6 LVDS_CONN_B_DATA_P<0>
100 86 6 LVDS_CONN_B_DATA_N<1>
100 86 6 LVDS_CONN_B_DATA_P<1>
100 86 6 LVDS_CONN_B_DATA_N<2>
100 86 6 LVDS_CONN_B_DATA_P<2>
100 6 LVDS_CONN_B_CLK_F_N
100 6 LVDS_CONN_B_CLK_F_P
90 6 LED_RETURN_6
90 6 LED_RETURN_5
90 6 LED_RETURN_4
90 6 LED_RETURN_3
90 6 LED_RETURN_2
90 6 LED_RETURN_1

NC

104 8 6 PPVOUT_S0_LCDBKLT

C9000 0.001UF 10% 50V CERM 402

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: LVDS Display Connector

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
BRANCH:
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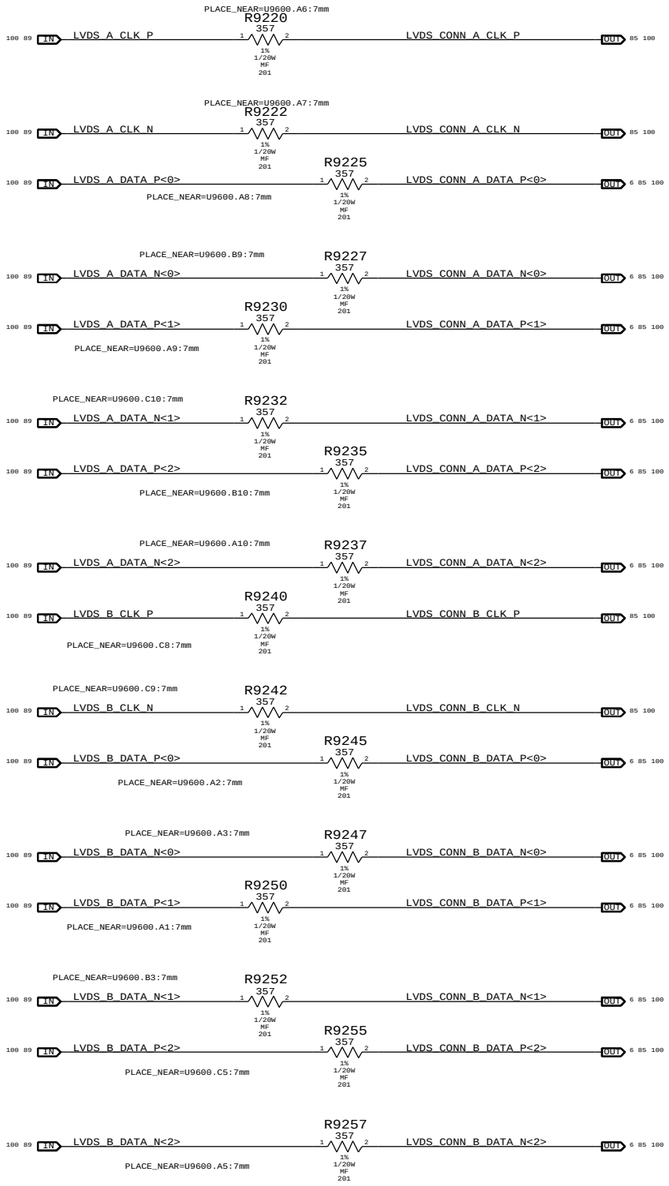
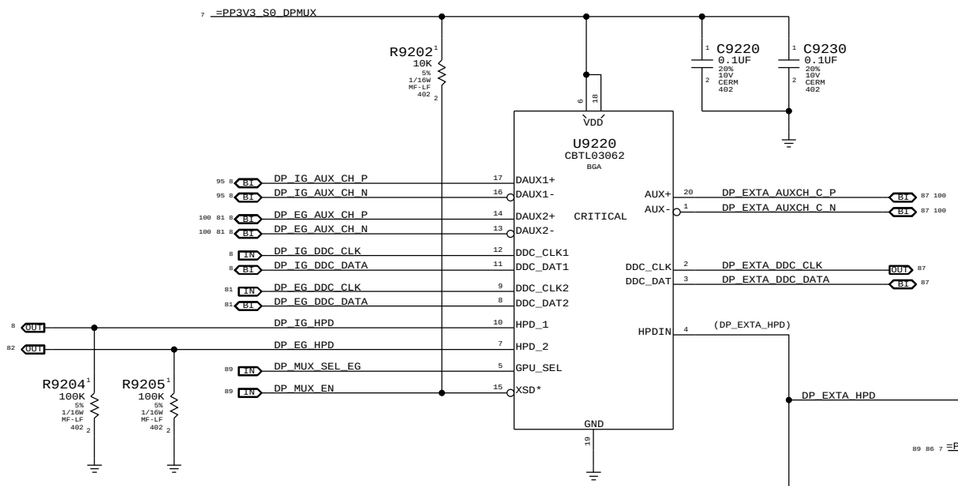
LVDS Transmitter Termination

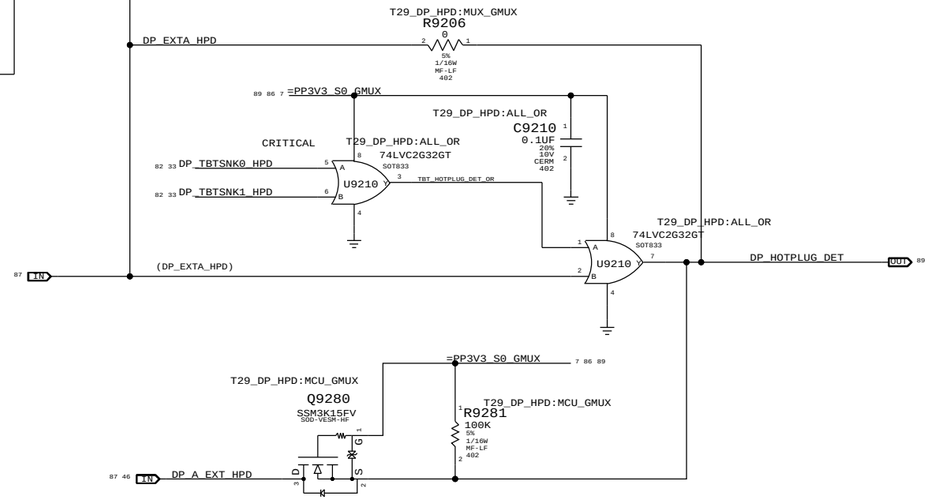
All emulated LVDS outputs require this termination



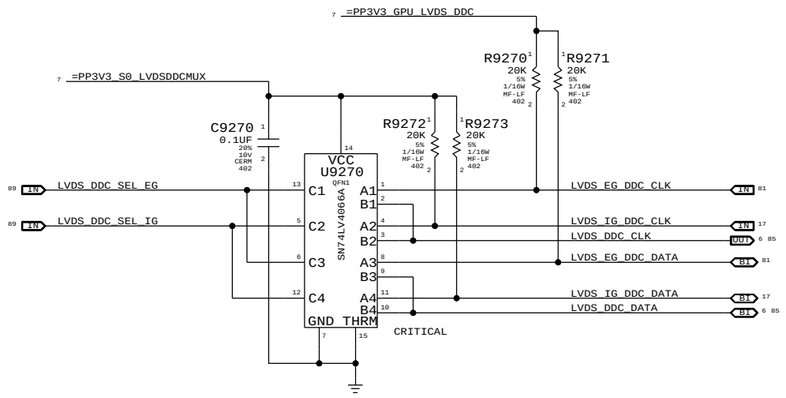
DP AUX, DDC, & HPD muxing to IG/EG



TBT/DP HOT PLUG IN



LVDS DDC MUX



SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010

PAGE TITLE

Muxed Graphics Support

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

BRANCH

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SHEET 86 OF 105

DP A Super-Driver

DP_EXTA_ML_C_P<0> C9300 0.1UF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1UF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1UF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1UF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1UF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1UF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1UF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1UF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N

=PP3V3_S0_DPSDRVA
R9309 1M
R9308 1M

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

=PP3V3_S0_DPSDRVA
C9310 2.2UF
C9311 0.1UF
C9312 0.1UF

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF
R9311 1K
R9310 1K
R9312 1K

U9310
PS8301TQFN40GTR-A2
QFN
CRITICAL

DP_EXTA_ML_P<0>	IN_D0P	OUT_D0P	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	IN_D0N	OUT_D0N	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	IN_D1P	OUT_D1P	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	IN_D1N	OUT_D1N	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	IN_D2P	OUT_D2P	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	IN_D2N	OUT_D2N	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	IN_D3P	OUT_D3P	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	IN_D3N	OUT_D3N	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	IN_SCL	AC_AUXP	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	IN_SDA	AC_AUXN	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	IN_HPD	OUT_HPD	DP_SDRVA_HPD
DPSDRVA_I2C_CTL_EN	I2C_CTL_EN (IPU)		
DPSDRVA_I2C_ADDR0	I2C_ADDR0 (IPD)		
DPSDRVA_I2C_ADDR1	I2C_ADDR1 (IPD)		
=I2C_DPSDRVA_SCL	SCL_CTL		
=I2C_DPSDRVA_SDA	SDA_CTL		
DPSDRVA_REXT	REXT		
DP_AUXCH_ISOL	AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	PD (IPD)		
	GND THMPAD	CA_DET	DP_A_CA_DET
		CEXT	DPSDRVA_CEXT

PLACE_NEAR=U9310.11:2mm
C9319 2.2UF

R9319 value depends on layout. 4.99K is vendor recommendation.

SDRV_PD
R9319 4.99K
R9318 0

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

Port A MCU

=PP3V3_S0_DPSDRVA
DP_A_PWRDWN
See Bill C. for layout-specific guidelines for =DP_A_BIAS.
C9359 0.1UF
U9359 74LVC1G04DBDCK SC70 CRITICAL
=DP_A_BIAS
IC supports input high while Vcc = 0V.

=TBT_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=TBT_WAKE_L
OMIT R9330 0
TBT_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SWCLK
SWDIO

=PP3V3_S0_TBTAPWR
Must be 3.3V DP A port power

U9330
LPC1112A
HVQFN25
CRITICAL
OMIT_TABLE

DP_A_CA_DET	RESET#/PIO0_0	R/PIO1_0/AD1	TBT_A_CONFIG1_RC
TBT_LSEO<0>	PIO0_1/CLKOUT	R/PIO1_1/AD2	TBT_A_CONFIG2_RC
	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3	TBT_A_HV_EN_R
=I2C_TBTAMCU_SCL	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4	TBT_A_UC_ADDR
=I2C_TBTAMCU_SDA	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP	
TBT_A_HPD	PIO0_6/SCK	PIO1_6/RXD	TBT_A_LSX_P2R
=TBT_A_BIAS	PIO0_7/CTS#	PIO1_7/TXD	TBT_A_LSX_R2P
TBT_LSOE<0>	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0	TBT_LSEO<1>
TBT_LSOE<1>	PIO0_9/MOSI/CT16B0_MAT1		
TBT_PWR_REQ_L	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
	R/PIO0_11/AD0 (OD)	XTALIN	
	VSS THRM PAD		

C9330 0.1UF
C9331 0.1UF
R9335 1K
R9336 10K
R9338 10K
R9334 10K

I2C Addr: 0x26/0x27 (Wr/Rd)

R9339 1M

P2R = Plug to Receptacle
R2P = Receptacle to Plug

TBT A High-Speed Signals

TBT_A_BIAS0P VOLTAGE=3.3V
TBT_D2R_N<0> C9370 0.47UF TBT_D2R_C_P<0>
TBT_D2R_P<0> C9371 0.47UF TBT_D2R_C_N<0>
GND_VOID=TRUE (C9370/C9371)
GND_VOID=TRUE (C9372.1&2)
TBT_R2D_C_N<0> C9372 0.47UF TBT_R2D_P<0>
TBT_R2D_C_P<0> C9373 0.47UF TBT_R2D_N<0>
GND_VOID=TRUE (C9373.1&2)
TBT_A_BIAS0N VOLTAGE=3.3V

TBT signals are P/N-swapped after AC caps to improve layout.

TBT_A_BIAS2P VOLTAGE=3.3V
GND_VOID=TRUE (C9380/C9381)
TBT_D2R_N<1> C9380 0.47UF TBT_D2R_C_P<1>
TBT_D2R_P<1> C9381 0.47UF TBT_D2R_C_N<1>
GND_VOID=TRUE (C9383.1&2)
TBT_R2D_C_N<1> C9382 0.47UF TBT_R2D_P<1>
TBT_R2D_C_P<1> C9383 0.47UF TBT_R2D_N<1>
GND_VOID=TRUE (C9383.1&2)
TBT_A_BIAS2N VOLTAGE=3.3V

TBT Path Biasing

R9372 1.5K
R9373 1.5K
R9382 1.5K
R9383 1.5K

D9364 BAR90-02LRH (D9364.2)
D9372 BAR90-02LRH TBT: TX_0
D9373 BAR90-02LRH
D9365 BAR90-02LRH
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K
R9375 1.5K

D9360 BAR90-02LRH (D9360.2)
D9382 BAR90-02LRH TBT: TX_1
D9383 BAR90-02LRH
D9361 BAR90-02LRH
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN
(D9382/D9383)
SIGNAL_MODEL=EMPTY
(D9360/D9361)
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K
R9385 1.5K

DP Path Biasing

R9354 30
R9355 30
R9350 30
R9351 30
R9352 270
R9353 270
C9364 0.22UF DP_SDRVA_ML_P<0>
C9365 0.22UF DP_SDRVA_ML_N<0>
C9360 0.22UF DP_SDRVA_ML_P<2>
C9361 0.22UF DP_SDRVA_ML_N<2>

R9361 1.5K DP_A_BIAS0 VOLTAGE=3.3V
R9360 1.5K
R9365 1.5K DP_A_BIAS2 VOLTAGE=3.3V
R9364 1.5K

C9367 0.1UF DP_SDRVA_ML_P<3>
C9366 0.1UF DP_SDRVA_ML_N<3>
C9363 0.1UF DP_SDRVA_ML_P<1>
C9362 0.1UF DP_SDRVA_ML_N<1>

AUXCH Snoop Port, used by PS8301 during training.

C9369 0.1uF
C9368 0.1uF

DP/TBT A Low-Speed MUX

PP3V3_SW_TBTAPWR
Must be V3P3 output from U9410

C9390 0.1UF
C9391 0.1UF
R9399 100K

U9390
CBTL04DP081
HVQFN
CRITICAL
OMIT_TABLE

(DP_SDRVA_ML_N<3>)	DIN1_0+	DOUT_0+	TBT_A_ML_N<3>
(DP_SDRVA_ML_P<3>)	DIN1_0-	DOUT_0-	TBT_A_ML_P<3>
(DP_SDRVA_ML_N<1>)	DIN1_1+		
(DP_SDRVA_ML_P<1>)	DIN1_1-	DOUT_1+	TBT_A_ML_N<1>
DP_SDRVA_AUXCH_P	AUX1+	DOUT_1-	TBT_A_ML_P<1>
DP_SDRVA_AUXCH_N	AUX1-		
(DP_SDRVA_HPD)	HPD_1	AUX+	DP_A_EXT_AUXCH_P
TBT_A_RSVDN	DIN2_0+	AUX-	DP_A_EXT_AUXCH_N
TBT_A_RSVDP	DIN2_0-	HPD_IN	DP_A_EXT_HPD
(TBT_A_LSX_P2R)	DIN2_1+		
(TBT_A_LSX_R2P)	DIN2_1-		
TBT_D2R1_BIASP	AUX2+		
TBT_D2R1_BIASN	AUX2-		
	HPD_2		
DP_A_PWRDWN	GPU_SEL		
=TBT_A_BIAS	AUX_SEL		
	NC		

SIGNAL_MODEL=T29DP_MUX

R9392 51
R9393 51
R9396 1K
R9397 1K
R9398 100K

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S - 9-12.6V, 1W minimum)

=PP3V3_S4_TBTAPWRSW
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402
V3P3OUT
V3P3
PP3V3_SW_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
=PPHV_SW_TBTAPWRSW 20V Max
OUT
PPHV_SW_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1
VHV
CRITICAL U9410 CD3210A0RGP QFN
C9485 0.1UF 20% 10V CERM 402
C9486 10UF 20% 6.3V X5R 603
C9411 0.1UF 10% 50V X7R 603-1
RSVD
RSVD
=TBTAPWRSW_EN
EN
ISET_V3P3
TBTAPWRSW_ISET_V3P3
TBT_A_HV_EN
HV_EN
ISET_S0
TBTAPWRSW_ISET_S0
=TBT_S0_EN
S0
ISET_S3
TBTAPWRSW_ISET_S3
GND
THRM PAD
TBTHV:P15V
R9410 22.6K 1% 1/16W MF-LF 402
12V: See below
<RHVS3>
TBTHV:P15V
R9411 22.6K 1% 1/16W MF-LF 402
<RHVS0>
R9412 36.5K 1% 1/16W MF-LF 402
<RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
TBTHV:P15V
R9413 22.6K 1% 1/16W MF-LF 402
TBTHV:P15V
R9414 22.6K 1% 1/16W MF-LF 402

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,384K,1,0402,SMD,LF	R9410		TBTHV:P12V
114S0368	1	RES,MTL FILM,1/16W,36.5K,1,0402,SMD,LF	R9411		TBTHV:P12V

	Nominal	Min	Max
IHVS0	1120mA	1090mA	1170mA (12W minimum)
IHVS3	125mA	124mA	126mA (1W minimum)

Thunderbolt Connector A

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9400 0.01UF 10% 50V X7R 402

TBT Dir DP Dir

TBT_D2R_C_P<0>
TBT_D2R_C_N<0>
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
TBT_A_ML_P<3>
TBT_A_ML_N<3>
Thunderbolt: Unused
TBT_A_BIAS1N VOLTAGE=3.3V
TBT_A_BIAS1P VOLTAGE=3.3V
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
TBT_D2R_C_P<1>
TBT_D2R_C_N<1>
D9498 BAR90-02LRH TSLP-2-7 SIGNAL_MODEL=T29PIN
D9499 BAR90-02LRH TSLP-2-7 SIGNAL_MODEL=T29PIN
CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
TBT_A_D2R1_AUXCH_P
TBT_A_D2R1_AUXCH_N
DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N
C9498 30PF 5% 25V C0G-CERM 0201
C9499 30PF 5% 25V C0G-CERM 0201
C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402
TBTACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
R9401 12 5% 1/10W MF-LF 402
R9441 100K 5% 1/10W MF-LF 402

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/10W MF-LF 402
R9451 1M 5% 1/10W MF-LF 402
C9494 330PF 10% 50V C0G 402
C9495 330PF 10% 50V C0G 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

For J9400 TBT SMT pads (3, 5, 17 & 19):
GND_VOID=TRUE

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS	
2	HOT_PLUG_DETECT	1	GND
4	CONFIG1	3	ML_LANE0P
6	CONFIG2	5	ML_LANE0N
8	GND	7	GND
10	ML_LANE3P	9	ML_LANE1P
12	ML_LANE3N	11	ML_LANE1N
14	GND	13	GND
16	AUX_CHP	15	ML_LANE2P
18	AUX_CHN	17	ML_LANE2N
20	DP_PWR	19	RETURN
SHIELD PINS		22 21	

TBTACONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
C9405 0.01UF 10% 50V X7R 402 GND_VOID=TRUE
(0-20V)
DP Dir TBT Dir
TBT_A_ML_P<0>
TBT_A_ML_N<0>
TBT: TX_0
C9406 0.01UF 10% 50V X7R 402 GND_VOID=TRUE
TBTACONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
(0-20V)
TBT_A_ML_P<1>
TBT_A_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_ML_P<2>
TBT_A_ML_N<2>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_ML_C_P<0>
TBT_A_ML_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_ML_C_P<2>
TBT_A_ML_C_N<2>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

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GMUX CPLD

R9600 0 5% 1/10W MF-LF 402 — =PP3V3_S0_GMUX

C9610 0.1UF 10% 6.3V X5R 201 — =PP3V3_S0_GMUX
C9621 0.1UF 10% 6.3V X5R 201
C9622 0.1UF 10% 6.3V X5R 201
C9623 0.1UF 10% 6.3V X5R 201
C9624 0.1UF 10% 6.3V X5R 201
C9625 0.1UF 10% 6.3V X5R 201
C9626 0.1UF 10% 6.3V X5R 201
C9627 0.1UF 10% 6.3V X5R 201
C9628 0.1UF 10% 6.3V X5R 201
C9629 0.1UF 10% 6.3V X5R 201

PP3V3_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

R9610 0 5% 1/10W MF-LF 402 — =PP1V8_S0_GMUX

C9611 0.1UF 10% 6.3V X5R 201 — =PP1V8_S0_GMUX
C9612 0.1UF 10% 6.3V X5R 201
C9613 0.1UF 10% 6.3V X5R 201
C9614 0.1UF 10% 6.3V X5R 201
C9615 0.1UF 10% 6.3V X5R 201
C9616 0.1UF 10% 6.3V X5R 201
C9617 0.1UF 10% 6.3V X5R 201

PP1V8_S0_GMUX_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=1.8V

C9600 4.7UF 20% 4V X5R-1 402 — =PP1V2_S0_GMUX
C9604 0.1UF 10% 6.3V X5R 201
C9605 0.1UF 10% 6.3V X5R 201
C9606 0.1UF 10% 6.3V X5R 201
C9607 0.1UF 10% 6.3V X5R 201
C9608 0.1UF 10% 6.3V X5R 201
C9609 0.1UF 10% 6.3V X5R 201

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9621 FERR-220-OHM 0402
C9631 0.1UF 10% 6.3V X5R 201

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.09 mm
VOLTAGE=3.3V

L9620 FERR-220-OHM 0402
C9630 0.1UF 10% 6.3V X5R 201

R9645 10K 1% 1/20W MF 201 — =PP3V3_S0_GMUX
R9640 10K 1% 1/20W MF 201 — =PP3V3_S0_GMUX

NO STUFF
R9646 10K 1% 1/20W MF 201
R9641 10K 1% 1/20W MF 201

VCC: C4, J3, J13, N11, P8
VCCAUX: C11, J2, J14, M8
VCCIO0: B5
VCCIO1: B7
VCCIO2: A12
VCCIO3: C14
VCCIO4: F13
VCCIO5: M12
VCCIO6: M9
VCCIO7: M3
VCCJ: C3
ULC_VCCPLL: A4
LRC_VCCPLL: P11

OMIT
CRITICAL
U9600
XP25-5
CSBGA

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB7A	BANK5
LCD_BKLT_PWM	N2	PB7B	BANK5
LVDS_DDC_SEL_EG	P4	PB14A	BANK5
LVDS_DDC_SEL_IG	N4	PB14B	BANK5
DP_MUX_EN	N3	PB15A(OD)	BANK5
DP_MUX_SEL_EG	M4	PB15B	BANK5
EG_RESET_L	P5	PB16A	BANK5
EG_RAIL1_EN	M5	PB16B	BANK5
EG_RAIL2_EN	P6	PB17A	BANK5
EG_RAIL3_EN	M6	PB17B	BANK5
EG_RAIL4_EN	P7	PB18A	BANK5
EG_CLKREQ_OUT_L	M7	PB18B(OD)	BANK5
DP_CA_DET_EG	N7	PB19A	BANK5
LCD_PWR_EN	N8	PB19B	BANK5
LPC_AD<0>	P9	PB20A	BANK4
LPC_AD<1>	N9	PB20B	BANK4
LPC_AD<2>	P10	PB26A	BANK4
LPC_AD<3>	M10	PB26B	BANK4
LPC_FRAME_L	P12	PB27A	BANK4
LPC_RESET_L	P13	PB27B	BANK4
LPC_CLK33M_GMUX	N12	PB28A	BANK4
GMUX_INT	P14	PB28B	BANK4
LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	B2	PL2B	BANK7
GMUX_PL6A	C2	PL6A	BANK7
TP_GMUX_PL6B	D3	PL6B	BANK7
LVDS_IG_A_DATA_P<0>	D1	PL7A	BANK7
LVDS_IG_A_DATA_N<0>	E1	PL7B	BANK7
LVDS_IG_A_DATA_P<1>	D2	PL8A	BANK7
LVDS_IG_A_DATA_N<1>	E3	PL8B	BANK7
LVDS_IG_A_DATA_P<2>	F1	PL9A	BANK7
LVDS_IG_A_DATA_N<2>	G1	PL9B	BANK7
LVDS_IG_B_DATA_P<0>	F3	PL10A	BANK7
LVDS_IG_B_DATA_N<0>	G2	PL10B	BANK7
LVDS_IG_B_DATA_P<1>	H2	PL11A	BANK7
LVDS_IG_B_DATA_N<1>	G3	PL11B	BANK7
LVDS_IG_A_CLK_P	H1	PL12A	BANK7
LVDS_IG_A_CLK_N	H3	PL12B	BANK7
LVDS_MUX_SEL_EG	L1	PL14A	BANK6
TP_GMUX_PL14B	L3	PL14B	BANK6
=GMUX_PCIE_RESET_L	K3	PL15A	BANK6
TP_GMUX_PL15B	L2	PL15B	BANK6
ALL_EG_PGOOD	N1	PL25A	BANK6
EG_CLKREQ_IN_L	P1	PL25B	BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

PT7A	A2	LVDS_B_DATA_P<0>	BANK0
PT7B	A3	LVDS_B_DATA_N<0>	BANK0
PT8A	A1	LVDS_B_DATA_P<1>	BANK0
PT8B	B3	LVDS_B_DATA_N<1>	BANK0
PT9A	C5	LVDS_B_DATA_P<2>	BANK0
PT9B	A5	LVDS_B_DATA_N<2>	BANK0
PT14A	B6	EG_PWRSEQ_EN	BANK0
PT14B	C7	GMUX_DEBUG_RESET_L	BANK0
PT15A	A6	LVDS_A_CLK_P	BANK0
PT15B	A7	LVDS_A_CLK_N	BANK0
PT16A	C8	LVDS_B_CLK_P	BANK0
PT16B	C9	LVDS_B_CLK_N	BANK0
PT17A	A8	LVDS_A_DATA_P<0>	BANK0
PT17B	B9	LVDS_A_DATA_N<0>	BANK0
PT18A	A9	LVDS_A_DATA_P<1>	BANK0
PT18B	C10	LVDS_A_DATA_N<1>	BANK0
PT19A	B10	LVDS_A_DATA_P<2>	BANK0
PT19B	A10	LVDS_A_DATA_N<2>	BANK0
PT20A	A11	TP_GMUX_PT20A	BANK1
PT20B	B12	TP_GMUX_PT20B	BANK1
PT28A	B13	TP_GMUX_PT32A	BANK1
PT28B	A13	TP_GMUX_PT32B	BANK1
PR2A	A14	DP_A_CA_DET	BANK2
PR2B	B14	DP_HOTPLUG_DET	BANK2
PR6A	D12	LVDS_EG_A_DATA_P<0>	BANK2
PR6B	D13	LVDS_EG_A_DATA_N<0>	BANK2
PR7A	D14	LVDS_EG_A_DATA_P<1>	BANK2
PR7B	E14	LVDS_EG_A_DATA_N<1>	BANK2
PR8A	E12	LVDS_EG_A_DATA_P<2>	BANK2
PR8B	F12	LVDS_EG_A_DATA_N<2>	BANK2
PR9A	F14	LVDS_EG_B_DATA_P<0>	BANK2
PR9B	G14	LVDS_EG_B_DATA_N<0>	BANK2
PR10A	G12	LVDS_EG_B_DATA_P<1>	BANK2
PR10B	G13	LVDS_EG_B_DATA_N<1>	BANK2
PR11A	H13	LVDS_EG_B_DATA_P<2>	BANK2
PR11B	H12	LVDS_EG_B_DATA_N<2>	BANK2
PR12A	H14	LVDS_EG_A_CLK_P	BANK2
PR12B	J12	LVDS_EG_A_CLK_N	BANK2
PR14A	L14	IG_LCD_PWR_EN	BANK3
PR14B	M13	EG_LCD_PWR_EN	BANK3
PR24A	N14	IG_BKLT_EN	BANK3
PR24B	N13	EG_BKLT_EN	BANK3

GND: J1, B8, C6, C12, E13, M14, N10, N5, P3, M2, C1, E2, B4, M11
ULC_GNDPLL
LRC_GNDPLL
GNDIO0
GNDIO1
GNDIO2
GNDIO3
GNDIO4
GNDIO5
GNDIO6
GNDIO7

CRITICAL
J9600 1909782 M-RT-SM
GMUX_JTAG_CONN
1 =PP3V3_S0_GMUX
2 JTAG_GMUX_TDO
3 JTAG_GMUX_TDI
4 JTAG_GMUX_TMS
5
6 JTAG_GMUX_TCK
8

NO STUFF
R9647 10K 1% 1/20W MF 201

R9605 1K 5% 1/20W MF 201 — =PP3V3_T29_JTAG — T29_JTAG_FET

SSM6N37FEAPE Q9605 SOT563 — JTAG_GMUX_TDI — JTAG_ISP_TDI
SSM6N37FEAPE Q9605 SOT563 — JTAG_GMUX_TDO — JTAG_ISP_TDO

R9676 100K 5% 1/20W MF 201 — =PP3V3_S3_GMUX — GMUX_S3_PD_EN
SSM6N37FEAPE Q9607 SOT563 — ALL_SYS_PWRGD
SSM6N37FEAPE Q9607 SOT563 — GMUX_S3_PD_GND
R9675 0 5% 1/20W MF 201 — NO STUFF

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.F3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.F12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX

EG_PWRSEQ_EN	R9684	1K	
JTAG_GMUX_TDI	R9685	10K	
JTAG_GMUX_TDO	R9686	10K	
GMUX_DEBUG_RESET_L	R9680	1K	

NO STUFF
R9679 10K 5% 1/20W MF 201
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K
LVDS_DDC_SEL_IG	R9682	10K
LVDS_DDC_SEL_EG	R9683	10K
EG_RESET_L	R9691	100K
LCD_BKLT_PWM	R9693	100K

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF

EG_RAIL4_EN — R9674 4.7K 5% 1/20W MF 201
EG_RAIL3_EN — R9673 4.7K 5% 1/20W MF 201
EG_RAIL2_EN — R9672 4.7K 5% 1/20W MF 201
EG_RAIL1_EN — R9671 4.7K 5% 1/20W MF 201
LCD_PWR_EN — R9678 4.7K 5% 1/20W MF 201

SYNC_MASTER=K91_MARY
SYNC_DATE=08/03/2016
PAGE TITLE: Graphics MUX (GMUX)
Apple Inc.
DRAWING NUMBER: 051-9585
SIZE: D
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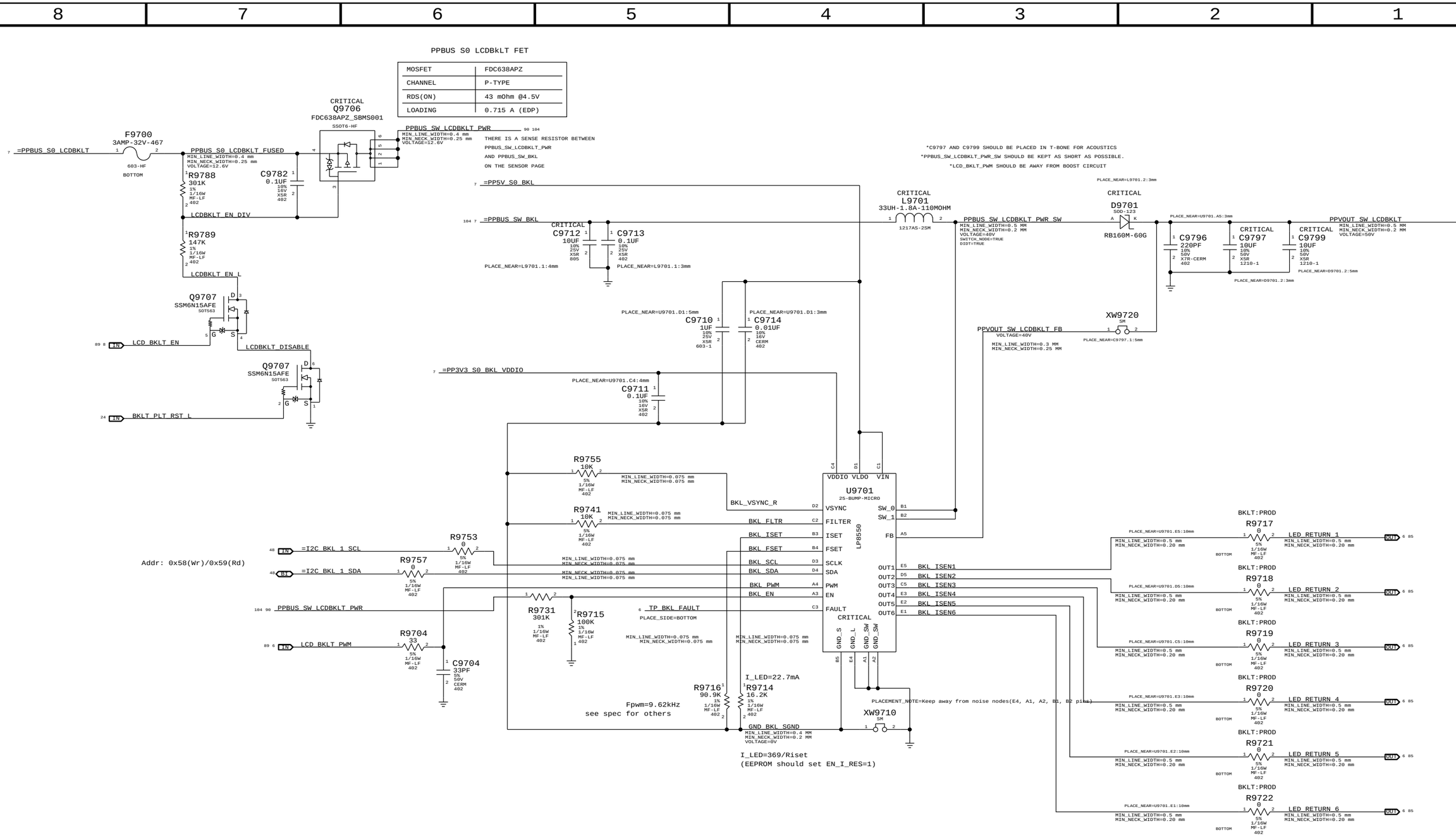

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMR	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMR	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J31_KIRAN SYNC_DATE=03/21/2011

PAGE TITLE: LCD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

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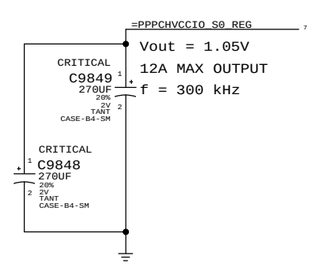
PCH VCCIO (1.05V S0) REGULATOR



SYNC_MASTER=J31_JACK SYNC_DATE=09/16/2011

PAGE TITLE

PCH VCCIO (1.05V) POWER SUPPLY

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

1) GPU_3.3V

2) IFPX IOVDD - 1.8V

3) GPUVCORE

4) FBVDDQ/GDDR5 1.35V

5) PEXVDD/Q OR IFPY IOVDD - 1.05V

89 EG_RAIL1_EN — P3V3GPU_EN — =P3V3GPU_EN — OUT 73
MAKE_BASE=TRUE

89 EG_RAIL2_EN — P1V8GPU_EN — =P1V8GPU_EN — OUT 73
MAKE_BASE=TRUE

89 EG_RAIL3_EN — GPUVCORE_EN — =GPUVCORE_EN — OUT 84
MAKE_BASE=TRUE

89 EG_RAIL4_EN

P1V35FB1V05GPU_R_EN — MAKE_BASE=TRUE

R9931 0 5% 1/20W MF 201

P1V35FB_EN — MAKE_BASE=TRUE — =P1V35FB_EN — OUT 78

R9932 20 5% 1/20W MF 201

P1V05GPU_EN — MAKE_BASE=TRUE — =P1V05_GPU_EN — OUT 78

C9932 0.47UF 10% 6.3V CERM-X5R 402

C9931 0.47UF 10% 6.3V CERM-X5R 402

PCH S0 PWRGD

7 =PP3V3_S5_PCHPWRGD

24 7 =PP3V3_S0_SB_PM

R9950 1K 5% 1/10W MF-LF 402

C9950 0.1UF 20% 10V CERM 402

89 74 45 23 IN ALL_SYS_PWRGD

69 IN CPUIMVP_PGOOD

U9950 74LVC2G08GT SOT833 08

PLACE_NEAR=U1800.p12:7mm

PM_S0_PGOOD

NC

U9950 74LVC2G08GT SOT833 08

NC

SYS_PWROK_R

R9962 1K 5% 1/10W MF-LF 402

PM_PCH_SYS_PWROK — OUT 17 23 45

92 46 45 35 SMC_DELAYED_PWRGD

ALL_SYS_PWRGD--> SMC delayed 99 ms -->SMC_DELAYED_PWRGD

92 46 45 35 SMC_DELAYED_PWRGD — R9960 0 5% 1/16W MF-LF 402 — PM_PCH_PWROK — MAKE_BASE=TRUE — OUT 17 24

PM_PCH_APWROK — 17

EXT GPU PWRGD Pullup

92 74 7 =PP3V3_S0_PWRCTL

PLACE_NEAR=U8000.AH16:7mm

R9990 100K 5% 1/16W MF-LF 402

84 IN GPUVCORE_PGOOD — R9901 0 — GPUVCORE_PGOOD_R

78 IN GPUFB_PGOOD — R9902 0 — GPUFB_PGOOD_R

78 IN P1V05_S0GPU_PGOOD — R9903 0 — P1V05_S0GPU_PGOOD_R

PM_ALL_GPU_PGOOD — MAKE_BASE=TRUE — OUT 8

NO STUFF C9905 0.001UF 20% 50V CERM 402

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_R2D_P<0> — 6 75 93

PLACE_NEAR=U8000.AN12:10MM

R9910 82 5% 1/20W MF 201

NOSTUFF

PEG_R2D_N<0> — 6 75 93

PEG_R2D_P<5> — 6 75 93

PLACE_NEAR=U8000.AP17:10MM

R9915 82 5% 1/20W MF 201

NOSTUFF

PEG_R2D_N<5> — 6 75 93

PEG_R2D_P<3> — 6 75 93

PLACE_NEAR=U8000.AN15:10MM

R9913 82 5% 1/20W MF 201

NOSTUFF

PEG_R2D_N<3> — 6 75 93

PEG_R2D_P<7> — 6 75 93

PLACE_NEAR=U8000.AN20:10MM

R9917 82 5% 1/20W MF 201

NOSTUFF

PEG_R2D_N<7> — 6 75 93

PLACE R9910 - R9917 CLOSE TO U8000

Unused PGOOD signal

92 74 7 =PP3V3_S0_PWRCTL

NO STUFF

R9991 10K 5% 1/16W MF-LF 402

CPUIMVP_AXG_PGOOD — IN 69

TP_DDRREG_PGOOD — MAKE_BASE=TRUE — DDRREG_PGOOD — IN 68

TP_P1V5S3RS0_RAMP_DONE — MAKE_BASE=TRUE — P1V5S3RS0_RAMP_DONE — IN 73

SYNC_MASTER=J31_SREE SYNC_DATE=09/19/2011

PAGE TITLE

Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	15 MIL	?

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RXRX	*	=3X_DIELECTRIC	?
PEG_TXTX	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RXRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	6 9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3:0>	8 9
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3:0>	8 9
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	8 9
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	8 9
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	9
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	9 23
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	8
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	8
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
XDP_RESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 24
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10 45
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 19
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	10 19 46
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 46 69
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	10 19 46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	10
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 69
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 69
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 69
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	12 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCSENSE_P	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCSENSE_N	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCIOSENSE_P	12 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCCIOSENSE_N	12 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_SENSE_P	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_SENSE_N	12 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCC_VALSENSE_P	12
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCC_VALSENSE_N	12
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_VALSENSE_P	12
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_AXG_VALSENSE_N	12
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	12 66
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	9 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	9 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	27 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	27 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	6 75 92
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	6 75 92
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	8 75
	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	8 75
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>	8 75
	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>	8 75
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	6 75
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	6 75

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D
REVISION: 3.0.0
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_*	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 6 11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 6 11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 6 11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 6 11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 6 11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 6 11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 6 11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 6 11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 6 11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 6 11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 6 11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 6 11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 6 11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 6 11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 6 11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 6 11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 6 11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 6 11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 6 11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 6 11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 6 11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 6 11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 6 11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 6 11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 6 11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 6 11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 6 11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 6 11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 6 11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 6 11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 6 11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 6 11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 6 11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 6 11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 6 11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 6 11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 6 11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 6 11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 6 11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 6 11 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 6 11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 6 11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 6 11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 6 11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 6 11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 6 11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 6 11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 6 11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 6 11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 6 11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 6 11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 6 11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 6 11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 6 11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 6 11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 6 11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 6 11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 6 11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 6 11 28

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	1to3, 1to4, 1to5, 1to10	=4:1_SPACING	?
LVDS	1to3, 1to4, 1to5, 1to10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D_ALT	*	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT	=90_OHM_DIFF_ALT
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

USB 3.0 Interface Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=5:1_SPACING	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 86
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 86
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 17 89
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 17 89
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 17 89
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 17 89
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<3> 8 17
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<3> 8 17
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 17 89
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 17 89
	SATA_90D_ALT	SATA	SATA_HDD_R2D_C_P 16 41
	SATA_90D_ALT	SATA	SATA_HDD_R2D_C_N 16 41
	SATA_90D_ALT	SATA	SATA_HDD_R2D_RC_P 41
	SATA_90D_ALT	SATA	SATA_HDD_R2D_RC_N 41
1239 SATA_HDD_R2D	SATA_90D_ALT	SATA	SATA_HDD_R2D_P 6 41
1240	SATA_90D_ALT	SATA	SATA_HDD_R2D_N 6 41
SATA_HDD_D2R	SATA_90D_ALT	SATA	SATA_HDD_D2R_P 16 41
	SATA_90D_ALT	SATA	SATA_HDD_D2R_N 16 41
	SATA_90D_ALT	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D_ALT	SATA	SATA_HDD_D2R_C_N 6 41
1242	SATA_90D_ALT	SATA	SATA_HDD_D2R_RC_P 41
1243	SATA_90D_ALT	SATA	SATA_HDD_D2R_RC_N 41
1244	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDROUT_P 41
1245	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDROUT_N 41
1246	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDRIN_P 41
1247	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDRIN_N 41
1248	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDROUT_P 41
1249	SATA_90D_ALT	SATA	SATA_HDD_D2R_RDROUT_N 41
1250	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDRIN_P 41
1251	SATA_90D_ALT	SATA	SATA_HDD_R2D_RDRIN_N 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_C_N 6 41
1213 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_EXTA	USB_85D	USB	USB_EXTA_P 18 42
	USB_85D	USB	USB_EXTA_N 18 42
USB_EXTB_MUX	USB_85D	USB	USB_EXTB_MUX_P 25 43
USB_EXTB_MUX	USB_85D	USB	USB_EXTB_MUX_N 25 43
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 18
	USB_85D	USB	USB_EXTC_N 8 18
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 32
	USB_85D	USB	USB_CAMERA_CONN_N 6 32
1223 USB_CAMERA	USB_85D	USB	USB_CAMERA_P 18 32
1224	USB_85D	USB	USB_CAMERA_N 18 32
USB_BT	USB_85D	USB	USB_BT_P 8 32
	USB_85D	USB	USB_BT_N 8 32
USB_BT	USB_85D	USB	USB_BT_CONN_P 6 32
1228	USB_85D	USB	USB_BT_CONN_N 6 32
USB_TPAD	USB_85D	USB	USB_TPAD_P 8 53
	USB_85D	USB	USB_TPAD_N 8 53
USB_TPAD	USB_85D	USB	USB_TPAD_R_P 25 53 101
1269	USB_85D	USB	USB_TPAD_R_N 25 53 101
1273	USB_85D	USB	USB_EXTD_XHCI_P 18 25
1274	USB_85D	USB	USB_EXTD_XHCI_N 18 25
1276	USB_85D	USB	USB_HUB_UP_P 18 25
1277	USB_85D	USB	USB_HUB_UP_N 18 25
USB_IR	USB_85D	USB	USB_IR_P 8 44
	USB_85D	USB	USB_IR_N 8 44
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
1221 USB3_EXT_TX	USB_85D	USB3	USB3_EXTA_TX_P 6 18 42
1220	USB_85D	USB3	USB3_EXTA_TX_N 6 18 42
1222 USB3_EXT_RX	USB_85D	USB3	USB3_EXTA_RX_P 6 18 42
1223	USB_85D	USB3	USB3_EXTA_RX_N 6 18 42
1256 USB3_EXT_TX	USB_85D	USB3	USB3_EXTA_TX_F_P 6 42
1258	USB_85D	USB3	USB3_EXTA_TX_F_N 6 42
1257 USB3_EXT_RX	USB_85D	USB3	USB3_EXTA_RX_F_P 6 42
1259	USB_85D	USB3	USB3_EXTA_RX_F_N 6 42
1260 USB3_EXT_TX	USB_85D	USB3	USB3_EXTA_TX_C_P 6 42
1261	USB_85D	USB3	USB3_EXTA_TX_C_N 6 42
1265 USB3_EXT_TX	USB_85D	USB3	USB3_EXTB_TX_C_P 6 43
1267	USB_85D	USB3	USB3_EXTB_TX_C_N 6 43
1264 USB3_EXT_TX	USB_85D	USB3	USB3_EXTB_TX_F_P 6 43
1266	USB_85D	USB3	USB3_EXTB_TX_F_N 6 43
1262 USB3_EXT_RX	USB_85D	USB3	USB3_EXTB_RX_F_P 6 43
1263	USB_85D	USB3	USB3_EXTB_RX_F_N 6 43
1224 USB3_EXT_TX	USB_85D	USB3	USB3_EXTB_TX_P 6 18 43
1225	USB_85D	USB3	USB3_EXTB_TX_N 6 18 43
1226 USB3_EXT_RX	USB_85D	USB3	USB3_EXTB_RX_P 6 18 43
1227	USB_85D	USB3	USB3_EXTB_RX_N 6 18 43
1230	USB_85D	USB	USB_EXTB_EHCI_P 18 25
1231	USB_85D	USB	USB_EXTB_EHCI_N 18 25
1232	USB_85D	USB	USB_EXTB_XHCI_P 18 25
1233	USB_85D	USB	USB_EXTB_XHCI_N 18 25
1234 USB_EXTB_MUX	USB_85D	USB	USB_EXTB_F_P 43
1235 USB_EXTB_MUX	USB_85D	USB	USB_EXTB_F_N 43
1236 USB_SMC	USB_85D	USB	USB_SMC_N 8
1237 USB_SMC	USB_85D	USB	USB_SMC_P 8
1253 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P 42
1252	USB_85D	USB	USB_EXTA_MUXED_N 42
1254 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_F_P 42
1255	USB_85D	USB	USB_EXTA_MUXED_F_N 42

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47 89
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47 89
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	24 89
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 24
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	24 45
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 24 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 48
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 48
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16 24
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE	PCIE_AP_D2R_N	16 32
I270	PCIE_85D	PCIE	PCIE_AP_D2R_R_P	32
I269	PCIE_85D	PCIE	PCIE_AP_D2R_R_N	32
	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
I253	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
I254	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
I262	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 33
I261	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 33
I255	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
I257	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
I256	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
I259	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
I258	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
I260	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 24
I272	CLK_PCIE_90D	CLK_PCIE	PEX_TSTCLK_O_P	75
I270	CLK_PCIE_90D	CLK_PCIE	PEX_TSTCLK_O_N	75
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 75
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 75
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
I263	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	8 33
I264	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	8 33
I266	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	8 33
I268	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	8 33
I273	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	33
I274	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	33
I275	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	33
I276	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	33

SYNC_MASTER=J31_YONAS SYNC_DATE=05/05/2013

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

REVISION: 3.0.0

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
ENET_RESET_L	ENET_50S	ENET_3X	ENET_RESET_L	30 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
H169	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	30 36
H170	CR_DATA_A0	ENET_CR	SDCONN_CMD	30 36
H171	CR_CLK	ENET_CR	SDCONN_CLK	30 36
H172		ENET_CR	SDCONN_CLK_R	30
H173		ENET_CR	SDCONN_CLK_R_L	30
H174		ENET_CR	SDCONN_R_DATA<7..0>	30

FireWire Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	38 40
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	38 40
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	38 40
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	38 40

Port 2 Not Used

SYNC_MASTER=K91_ERIC SYNC_DATE=08/03/2010

PAGE TITLE: Ethernet/FW Constraints

Apple Inc.

DRAWING NUMBER: 051-9585 SIZE: D

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
TBTDP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius’s Thunderbolt Routing Notes

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	6 33 81
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	6 33
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	6 33 81
DP_TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	6 33
DP_TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	6 33 81
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	6 33
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	6 33 81
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	6 33 81
DP_TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	6 33
DP_TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
	TBT_I2C_55S	TBT_I2C	I2C_TBT_SCL	33 48
	TBT_I2C_55S	TBT_I2C	I2C_TBT_SDA	33 48
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	33
	TBTDP_80D	TBTDP	TBT_R2D_C_P<3..0>	6 8 33 87
	TBTDP_80D	TBTDP	TBT_R2D_C_N<3..0>	6 8 33 87
	TBTDP_100D	TBTDP	TBT_D2R_P<3..0>	8 33 87
	TBTDP_100D	TBTDP	TBT_D2R_N<3..0>	8 33 87

Only used on hosts supporting Thunderbolt video-in

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_R2D0	TBTDP_80D	TBTDP	TBT_R2D_P<0>	87
TBT_R2D0	TBTDP_80D	TBTDP	TBT_R2D_N<0>	87
TBT_R2D1	TBTDP_80D	TBTDP	TBT_R2D_P<1>	87
TBT_R2D1	TBTDP_80D	TBTDP	TBT_R2D_N<1>	87
TBT_D2R0	TBTDP_100D	TBTDP	TBT_D2R_C_P<0>	87 88
TBT_D2R0	TBTDP_100D	TBTDP	TBT_D2R_C_N<0>	87 88
TBT_D2R1	TBTDP_100D	TBTDP	TBT_D2R_C_P<1>	87 88
TBT_D2R1	TBTDP_100D	TBTDP	TBT_D2R_C_N<1>	87 88
	TBTDP_100D	TBTDP	TBT_A_D2R1_AUXCH_P	88
	TBTDP_100D	TBTDP	TBT_A_D2R1_AUXCH_N	88
	TBTDP_80D	TBTDP	DP_SDRVA_ML_C_P<3..0>	6 87
	TBTDP_80D	TBTDP	DP_SDRVA_ML_C_N<3..0>	6 87
	TBTDP_80D	TBTDP	DP_SDRVA_ML_R_P<3..0>	87
	TBTDP_80D	TBTDP	DP_SDRVA_ML_R_N<3..0>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<3>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<3>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<1>	87
DP_SDRVA_ML_ODD	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<1>	87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<2>	6 87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<2>	6 87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_P<0>	6 87
DP_SDRVA_ML_EVEN	TBTDP_80D	TBTDP	DP_SDRVA_ML_N<0>	6 87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_P	87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_N	87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_C_P	87
	TBTDP_80D	TBTDP	DP_SDRVA_AUXCH_C_N	87
	TBTDP_80D	TBTDP	TBT_A_ML_P<3..0>	87 88
	TBTDP_80D	TBTDP	TBT_A_ML_N<3..0>	87 88
	TBTDP_80D	TBTDP	TBT_A_ML_C_P<3..0>	87 88
	TBTDP_80D	TBTDP	TBT_A_ML_C_N<3..0>	87 88
	TBTDP_80D	TBTDP	DP_A_EXT_AUXCH_P	87 88
	TBTDP_80D	TBTDP	DP_A_EXT_AUXCH_N	87 88

SYNC_MASTER=T29_REF SYNC_DATE=06/14/2011

PAGE TITLE: Thunderbolt Constraints

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DRAWING NUMBER: 051-9585 SIZE: D

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	45 48
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	45 48
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	45 48
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	45 48
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	6 45 48
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	6 45 48
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	45 48
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	45 48
SMBUS_SMC_5_G3_SCL	SMB_50S	SMB	SMBUS_SMC_5_G3_SCL	6 45 48
SMBUS_SMC_5_G3_SDA	SMB_50S	SMB	SMBUS_SMC_5_G3_SDA	6 45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	65
	1TO1_DIFFPAIR		CHGR_CSI_N	65
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	65
	1TO1_DIFFPAIR		CHGR_CSO_N	65

SYNC_MASTER=J31_YONAS SYNC_DATE=08/11/2011

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-9585 SIZE D

REVISION 3.0.0

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	77 79
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	77 79
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	77 79
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>	6 77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>	6 77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L	6 77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L	6 77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L	77 79
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L	77 79
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L	77 79
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L	77 79
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L	77 79
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 77 79
293 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 77 79
294 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 77 79
295 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 77 79
296 FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 77 79
297 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 77 79
298 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 77 79
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 77 79
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 77 79
299 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 77 79
300 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 77 79
301 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 77 79
302 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 77 79
303 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 77 79
304 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 77 79
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 77 79
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 77 79
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 77 79
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 77 79
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 77 79
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 77 79
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 77 79
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 77 79
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 77 79
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 77 79
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 77 79
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 77 79
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 77 79
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 77 79
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 77 79
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 77 79
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 77 79
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L	77 79
323 FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L	77 79

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	77 80
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	77 80
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	77 80
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>	6 77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>	6 77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L	6 77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L	6 77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L	77 80
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L	77 80
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L	77 80
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L	77 80
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L	77 80
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 77 80
1305 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 77 80
1306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 77 80
1307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 77 80
1310 FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 77 80
1309 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 77 80
1308 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 77 80
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 77 80
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 77 80
1311 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 77 80
1312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 77 80
1313 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 77 80
1316 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 77 80
1315 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 77 80
1314 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 77 80
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 77 80
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 77 80
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 77 80
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 77 80
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 77 80
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 77 80
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 77 80
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 77 80
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 77 80
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 77 80
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 77 80
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 77 80
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 77 80
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 77 80
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 77 80
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 77 80
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 77 80
1324 FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L	77 80
1325 FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L	77 80

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	86 89
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	86 89
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	86 89
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	86 89
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	86 89
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	86 89
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	86 89
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	86 89
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 85
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 85
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 85
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 85
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	85 86
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	85 86
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 85 86
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 85 86
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	85 86
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	85 86
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 85 86
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 85 86

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M_IN	CLK_SLOW_45S	CLK_SLOW	GPU_OSC_27M_XTALIN	81 82
GPU_CLK27M_OUT	CLK_SLOW_45S	CLK_SLOW	GPU_OSC_27M_XTALOUT	81 82
1326	CLK_SLOW_45S	CLK_SLOW	GPU_OSC_27M_XTALOUT_R	82
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	81 89
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	81 89
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	81 89
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	81 89
LVDS_EG_A_DATA3	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<3>	
LVDS_EG_A_DATA3	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<3>	
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	81 89
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	81 89
LVDS_EG_B_DATA3	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<3>	
LVDS_EG_B_DATA3	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<3>	
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	81 87
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	81 87
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	86 87
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	86 87
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P	8 81 86
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N	8 81 86
1322	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	87
1320	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	87
1321	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	87
1318	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	87

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE
GPU (Kepler) CONSTRAINTS

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

J31 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
		ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
		THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
287	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_P	51
288		THERM_1TO1_55S	THERM	CPUTHMSNS_D1_N	51
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
		THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 81
		THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 81
1150	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUVCORE_SENSE_P	83 84
1151	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUVCORE_SENSE_N	83 84
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	49 66
		SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	49 66
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_P	49
		SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_N	49
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIO50_CS_P	49 71
		SENSE_1TO1_55S	SENSE	CPUVCCIO50_CS_N	49 71
1154	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_R_P	
1155		SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_R_N	
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_P	
		SENSE_1TO1_55S	SENSE	GFXIMVP6_CS_N	
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	103
1256		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	103
1254	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	41 103
1255		SENSE_1TO1_55S	SENSE	ISNS_HDD_P	41 103
1283	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
1284		SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
1300	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS2_P	84
1301		SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS2_N	84
1222	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	101
1221		SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	101
1220	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_P	101
1302		SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_N	101
1303	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS1_P	84
1304		SENSE_1TO1_55S	SENSE	GFXIMVP_ISNS1_N	84
1363	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0GPU_R_P	103
1364		SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0GPU_R_N	103
1305	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S0GPU_P	
1306		SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S0GPU_N	
1308	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P	
1307		SENSE_1TO1_55S	SENSE	ISNS_TBT_N	
1329	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	50 70
1330		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	50 70
1337	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	50
1338		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	50
1359	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	50 70
1360		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	50 70
1361	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	50 69 70
1362		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	50 69 70
1353	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	50 69 70
1354		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	50 70
1356	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS3_P	50 69 70
1355		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS3_N	50 70
1333	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
1332		SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
1353	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	50
1334		SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	50
1335	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
1336		SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
1342	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	50
1341		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	50
1340	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	101
1345		SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	101
1347	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	
1348		SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	
1349	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VCORE_RMC_P	105
1352		SENSE_1TO1_55S	SENSE	CPU_VCORE_RMC_N	105
1350	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_P	101
1351		SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_N	101
1363	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPU_R_P	
1364		SENSE_1TO1_55S	SENSE	ISNS_GPU_R_N	
1367	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVCCSA_R_P	49
1368		SENSE_1TO1_55S	SENSE	ISNS_CPUVCCSA_R_N	49
1369	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVCCIO_R_P	49
1370		SENSE_1TO1_55S	SENSE	ISNS_CPUVCCIO_R_N	49
1371	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	50
1372		SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	50
1373	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	50
1374		SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	50
1375	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_R_P	103
1376		SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S3_R_N	103
1378	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PPGPUFB_S0_R_P	103
1377		SENSE_1TO1_55S	SENSE	ISNS_PPGPUFB_S0_R_N	103
1380	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P	78 103
1379		SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N	78 103
1381	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_P	78 103
1383		SENSE_1TO1_55S	SENSE	GPUFB_CS_N	78 103
1382	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	103
1384		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	103
1387	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_R_P	104
1388		SENSE_1TO1_55S	SENSE	ISNS_TBT_R_N	104
1395	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_PEX_IOVDD_SNS_P	78 83
1396		SENSE_1TO1_55S	SENSE	P1V05_GPU_PEX_IOVDD_SNS_N	78 83
1398	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPU_FBVDDQ_SENSE_P	77 78
1397		SENSE_1TO1_55S	SENSE	GPU_FBVDDQ_SENSE_N	77 78

J31 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
		1TO1_DIFFPAIR		CHGR_CSI_R_P	65
		1TO1_DIFFPAIR		CHGR_CSI_R_N	65
		1TO1_DIFFPAIR		CHGR_CSO_R_P	65
		1TO1_DIFFPAIR		CHGR_CSO_R_N	65
1197	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	BI_MIC_P	6 62 63
1196		AUDIODIFF	AUDIO	BI_MIC_N	6 62 63
1194	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	
1195		AUDIODIFF	AUDIO	AUD_LO1_L_N	
1191	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	57 61
1193		AUDIODIFF	AUDIO	AUD_LO1_R_N	57 61
1192	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	57 61
1190		AUDIODIFF	AUDIO	AUD_LO2_L_N	57 61
1188	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	57 61
1189		AUDIODIFF	AUDIO	AUD_LO2_R_N	57 61
1187	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	61
1186		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	61
1184	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	61
1185		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	61
1021	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	61
1022		AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	61
1024	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	61
1025		AUDIODIFF	AUDIO	SSM2375L_N	61
1180	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	61
1181		AUDIODIFF	AUDIO	SSM2375R_N	61
1182	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	61
1183		AUDIODIFF	AUDIO	SSM2375S_N	61
	SPK_OUT		AUDIO	SPKRCONN_L_OUT_P	6 61 62
			AUDIO	SPKRCONN_L_OUT_N	6 61 62
	SPK_OUT		AUDIO	SPKRCONN_R_OUT_P	6 61 62
			AUDIO	SPKRCONN_R_OUT_N	6 61 62
	SPK_OUT		AUDIO	SPKRCONN_S_OUT_P	6 61 62
			AUDIO	SPKRCONN_S_OUT_N	6 61 62
		USB_85D	USB	USB_TPAD_R_P	25 53 95
		USB_85D	USB	USB_TPAD_R_N	25 53 95
			SB_POWER	PP3V3_S5	6 7
			SB_POWER	PP3V3_S0	6 7
			SB_POWER	PP1V5_S3RS0	7
			GND	GND	

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Project Specific Constraints

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J31 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.091 MM		0.120 MM	0.080 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.091 MM		0.120 MM	0.080 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?
10X_DIELECTRIC	*	0.700 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF_ALT	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF_ALT	ISL3,ISL4,ISL9,ISL10	Y	0.099 MM	0.099 MM		0.280 MM	0.280 MM
90_OHM_DIFF_ALT	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.280 MM	0.280 MM
90_OHM_DIFF_ALT	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.300 MM	0.300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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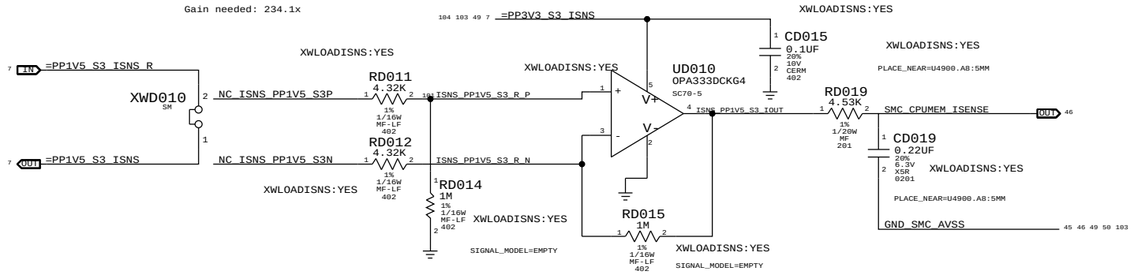
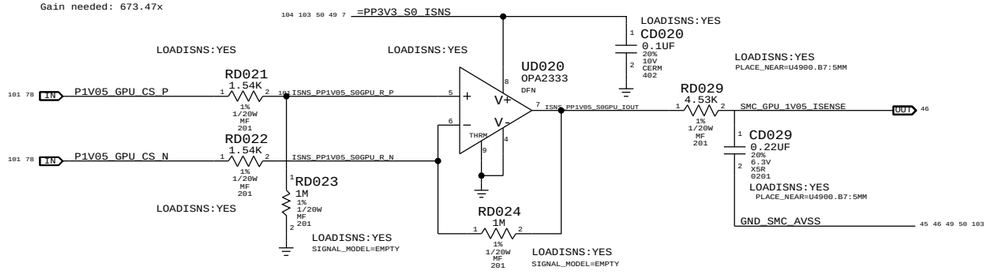
DDR 1.5V S3 (CPU & Memory) Current Sense (IM1C)

Gain: 231.4x, EDP: 14.1 A
Rsense: 0.001 (RD010)
V accross Rsense: 14.1 mV
Gain needed: 234.1x



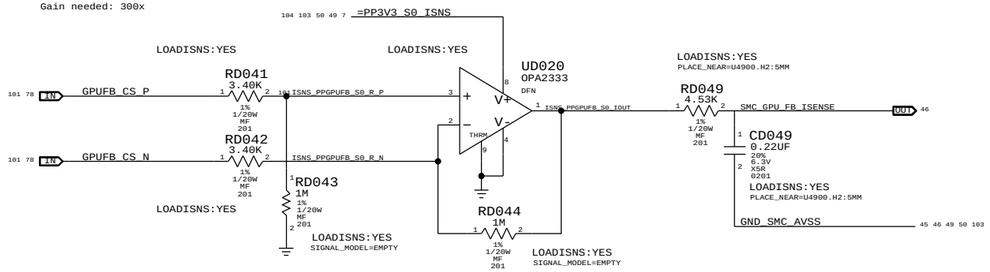
GPU 1.05V Current Sense (IG1C)

Gain: 649.35x, EDP: 4.9 A
Rsense: 0.001 (RD8310)
V accross Rsense: 4.9 mV
Gain needed: 673.47x

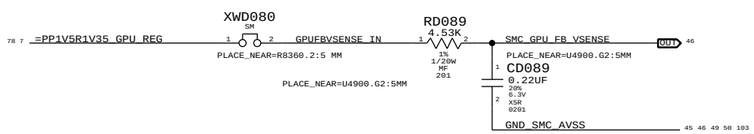


GPU FB (1.35V/1.5V) Current Sense (IG3C)

Gain: 294.12x, EDP: 11 A
Rsense: 0.001 (R8360)
V accross Rsense: 11 mV
Gain needed: 300x

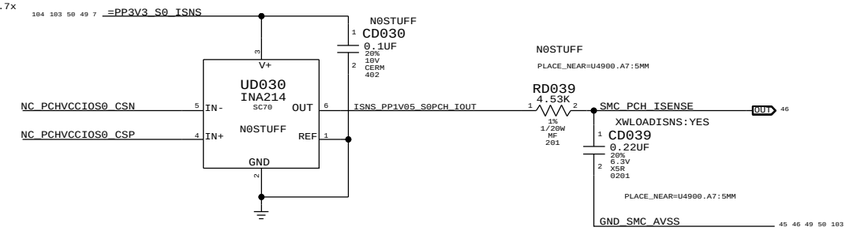


GPU FB (1.35V/1.5V) Voltage Sense (VG3C)



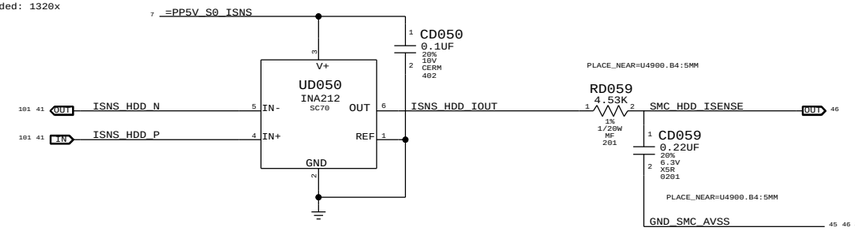
PCH Core (PCH VCCIO) Current Sense (ISBC)

Gain: 100x, EDP: 11.4 A
Rsense: 0.002 (R9840)
V accross Rsense: 22.8 mV
Gain needed: 144.7x



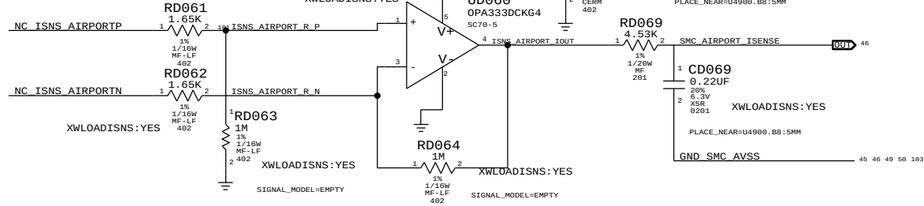
HDD Current Sense (IHDC)

Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R4599)
V accross Rsense: 2.5 mV
Gain needed: 1320x



Airport Current Sense (IAPC)

Gain: 606x, EDP: 1 A
Rsense: 0.005 (R3552)
V accross Rsense: 5 mV
Gain needed: 660x



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,100K,201	CD029,CD049		LOADISNS:NO
117S0008	3	RES,100K,201	CD019,CD039,CD069		XWLOADISNS:NO

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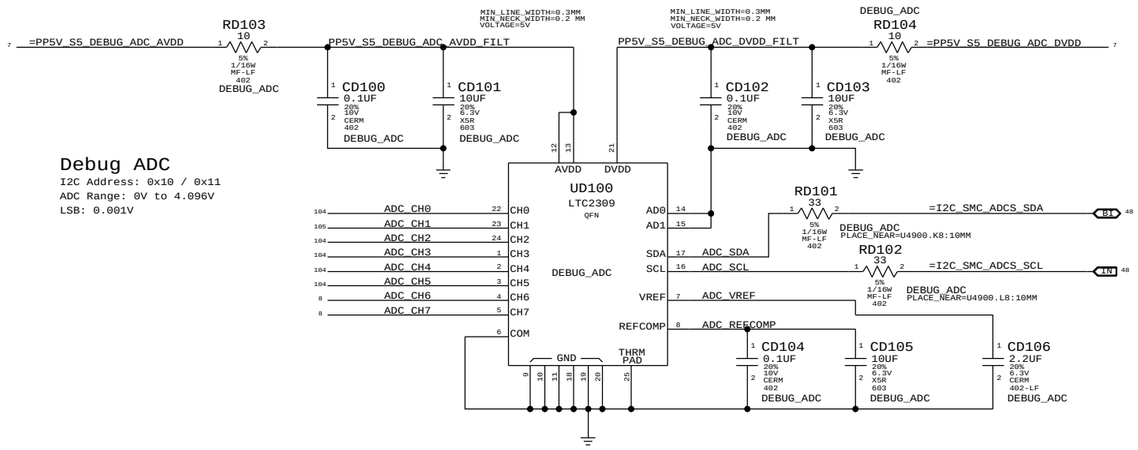
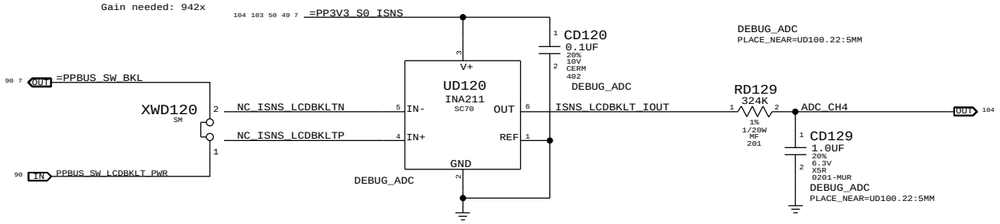
Debug ADC

I2C Address: 0x10 / 0x11
ADC Range: 0V to 4.096V
LSB: 0.001V



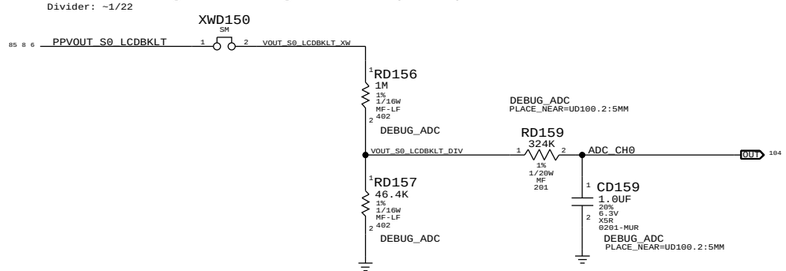
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.7 A
Rsense: 0.005 (RD120)
V across Rsense: 3.5 mV
Gain needed: 942x



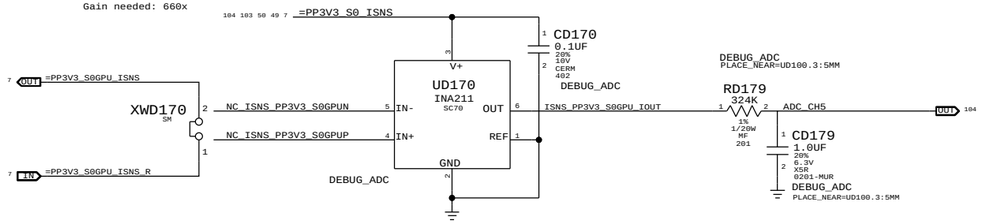
LCD Backlight Voltage Sense (VBLC)

Divider: ~1/22



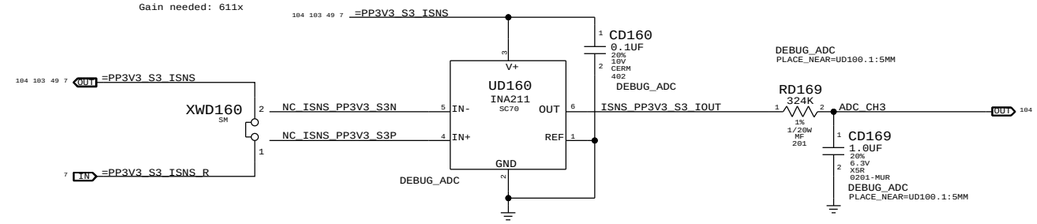
GPU 3.3V S0 Current Sense (IG2C)

Gain: 500x. EDP: 1.0 A
Rsense: 0.005 (RD170)
V across Rsense: 5 mV
Gain needed: 660x



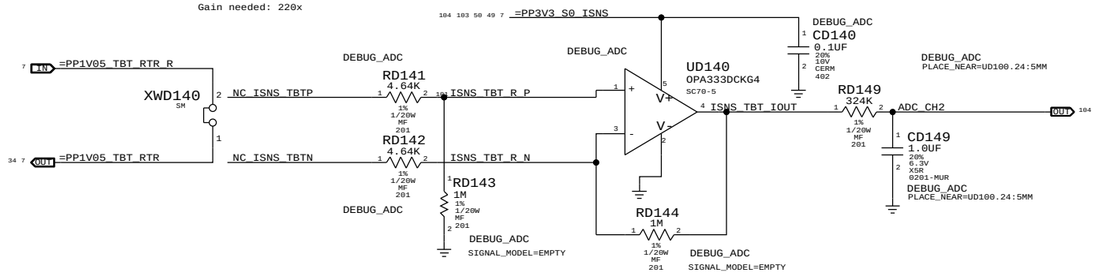
3.3V S3 Current Sense (IR1C)

Gain: 500x. EDP: 1.8 A
Rsense: 0.003 (RD164)
V across Rsense: 5.4 mV
Gain needed: 611x



T29 Current Sense (IHSP)

Gain: 215.5x. EDP: 3 A
Rsense: 0.005 (RD140)
V across Rsense: 15 mV
Gain needed: 220x



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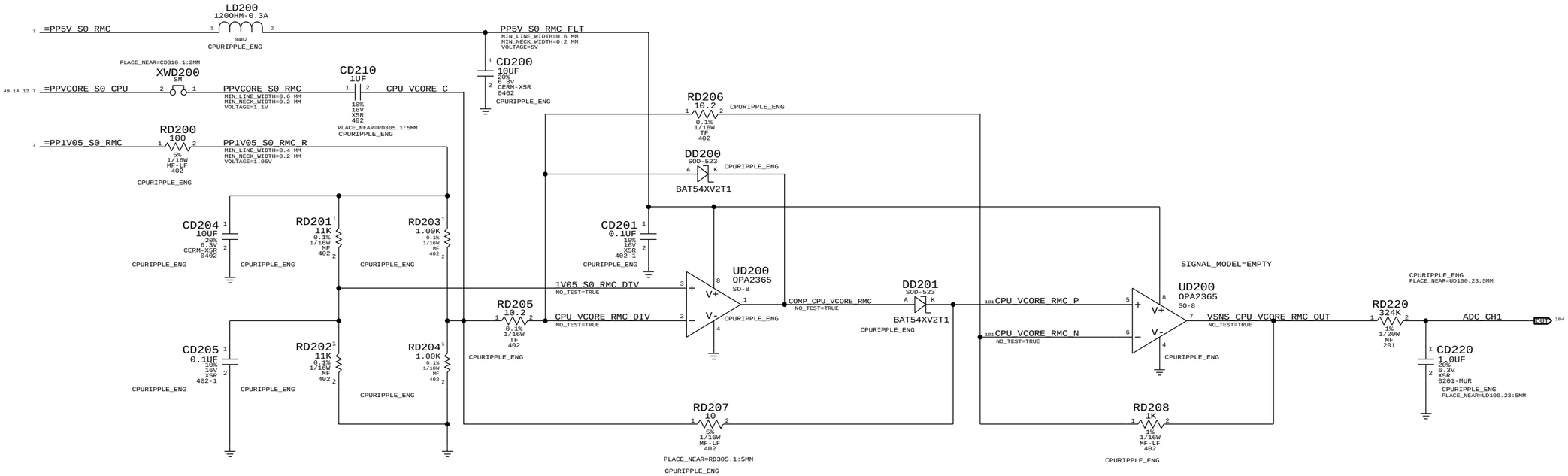
CPU Rippler Voltage Sense (VCRP)



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