J44 MLB-4GB SCHEMATIC
08/20/2013

ALIASES RESOLVED

www.rosefix.com
## Programmables (All Builds)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>DIFFERENCE DES</th>
<th>CRITICAL</th>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

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<thead>
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<th>PART NUMBER</th>
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</tr>
</thead>
<tbody>
<tr>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<td></td>
<td></td>
</tr>
</tbody>
</table>

## BOM Configuration

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## Table A: DRAM Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>22300701</td>
<td>1</td>
<td>IC, SDRAM, 4GBIT, DDR3L-1600, HUMA, 96B FBGA333S0700</td>
<td>CAMDRAM:MICRON</td>
<td>CRITICAL</td>
<td>CRITICAL:U40001</td>
</tr>
<tr>
<td>22300698</td>
<td>1</td>
<td>IC, SDRAM, 4GBIT, DDR3L-1600, REV E, 96B FBGA U40003</td>
<td>CAMDRAM:MICRON</td>
<td>CRITICAL</td>
<td>CRITICAL:U40003</td>
</tr>
</tbody>
</table>

## Table B: DRAM SPD Straps

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAMDRAM:MICRON</td>
<td>CAMDRAM_TYPE:MICRON</td>
</tr>
<tr>
<td>CAMDRAM:ELPIDA</td>
<td>CAMDRAM_TYPE:ELPIDA</td>
</tr>
<tr>
<td>CAMDRAM:HYNIX_H</td>
<td>CAMDRAM_TYPE:HYNIX_H</td>
</tr>
</tbody>
</table>

## Table C: BOM Configuration

- Development/Base ROM:
  - Part Number: 485-1001
    - QTY: 1
    - Description: J44 GPS Tuning ROM
    - Reference DES: CRITICAL
    - Critical: BASE
    - ROM Option: DEVI, ROM

- Base ROM:
  - Part Number: 485-1072
    - QTY: 1
    - Description: V40E_FLY, V30_E, V40E_FLY
    - Reference DES: CRITICAL
    - Critical: V40E_FLY

## Table D: Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1533655</td>
<td>1</td>
<td>IC, SDRAM, 4GBIT, 256MX16, DDR3-1866, REV E, 96FBGA333S0720</td>
<td>U2300, U2320, U2340, U2360, U2500, U2520, U2540, U2560</td>
<td>CRITICAL</td>
<td>CRITICAL:U2300</td>
</tr>
<tr>
<td>1533655</td>
<td>1</td>
<td>IC, SDRAM, 4GBIT, 256MX16, DDR3-1866, F DIE, 96FBGA333S0704</td>
<td>U2300, U2320, U2340, U2360, U2500, U2520, U2540, U2560</td>
<td>CRITICAL</td>
<td>CRITICAL:U2300</td>
</tr>
</tbody>
</table>

### Notes
- 1866 Parts being strapped to run at 1600.
Shield Cans

Mounting Holes & Slots

Rubber Mount Standoffs (860-1448)

THERMAL MODULE STANDOFF (860-1645)

SSD STANDOFF (806-5375)  FAN STANDOFF (806-5376)

POGO PINS (870-2451)

RIO FLEX BRACKET BOSSES (860-2354)
CPU VCC Decoupling

Intel recommendation (Table 5-1): 1x 22uf 0805, 7x 22uf 0805

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff

Added 2 extra 2.2uf per Harris Beach v0.9 schematic

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System RTC Power Source & 32kHz / 25MHz Clock Generator
Chipset uses 32kHz crystal, 25MHz helps to save in 32kHz crystal & in 32kHz crystal

PCH Reset Button
CPU output is an NRZ signal (1.2V), TPS61191 has 1.8V Vin(min).

PCH ME Disable Strap
Q1920 6K, PCH ME Disable Strap

PCH PWROK Generation

Chipset Support
Apple Inc.
DDC Crossbar

Only necessary on dual-port hosts. On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC. NEVER SEND AUXCH THROUGH CROSSBAR!

Current pull-up is needed for dual-port designs. Connect to DDC_ADJ_0 +1.5V DC, on page 12.

DDC Pull-Ups

2.3k pull-ups are required by DDC to transmit active display interface.

DP== open violation, should remove:

NOTE: only DDC_CLK is sensed, so DDC_CLK pull-ups are optional.

2.2k pull-ups are required by PCH DP++ spec violation, should remove!

On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.

DDC Crossbar
Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux
The signal lines for clamp voltage to the internal USB pin

USB Port Power Switch

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Keyboard Backlight Connector

51660899
CRITICAL
J4915
AA17A-0012-VA1

PHI 8 WAS USED KEYBOARD BKLT DETECTION
NOT USED ANYMORE

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SHEET IV
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Debug Power "Buttons"

SMC Reset "Button", Supervisor & AVREF Supply

Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups now on VCC, not Vr.

SMC Crystal Circuit

SMC clock reference source (VCR)

SMC Power "Button"
CPU High Side (ICOR) Peak Detection Support

Battery BMON Discrete Current Sense (IPOR) & Threshold Alert

Power Sensors: Extended

Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)

LCD Panel Current Sense (ILDC)

Camera (S2 Controller) Current Sense (ICMC)
Thermal Sensor A:
Thunderbolt Die (THSD)
- I2C Write: 0x98, I2C Read: 0x99
- CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0xD8, I2C Read: 0xD9
- Thunderbolt Die, MLB Proximity
- Thermal Sensor B & CPU High Peak Detection:

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity
- I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (THSD)
- The P leg connects to THERMDA pin of the TBT
- The N leg connect to pin AA8.

Thermal Diode: MLB Proximity (TMLB)
- Place Q5873 under the CPU
- Place Q5872 between two rows of Memory devices

Thermal Diode: Memory Proximity (THMD)
- Place Q5871, Airflow thermal indicator, above

Thermal Diode: Airflow (TAOF)
- Place Q5870 on the TOP side, on the left portion
  of the board, 1” to the right of USB connector.

Thermal Diode: CPU Proximity (TCOP)
- Place Q5874, THERMDA pin of the TBT
- Place Q5873 on the bottom side.

Thermal Diode: Fin Stack Proximity (Th1S)
- Place Q5875, Fin Stack Proximity (Th1H) on the TOP side.

Thermal Sensor: Pin Stack Proximity (Th1S)
- Place Q5876, Pin Stack Proximity (Th1H) on the TBT side.

Thermal Sensor: Fin Stack Proximity (Th1H)
- Make BASE = TRUE
- NO_XNET_CONNECTION = TRUE

Thermal Sensor: MLB Proximity (TMLB)
- Use GND pin AA8 on U2800 for N leg.

Placement Note:
- Thermal Diode: Memory Proximity (TM0P)
- Thermal Diode: CPU Proximity (TC0P)
- Thermal Diode: Airflow (TA0P)

Note: Use GND pin AA8 on U2800 for N leg.

KEEP THE 5 PIN CONNECTOR FROM D1
SPI ROM
Dual-IO mode (Mode 0 & 2) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
NOTE: Not all ROM APNs currently used
support Quad-IO. Also not compatible with
Matt card ROM override. Quad-IO support
is for experimentation only.

LPC+SPI Connector
(Matt Card Connector)

SPI Bus Series Termination
4.5V POWER SUPPLY FOR CODEC

PLACE XW6201 NEAR 5V SOURCE
R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)

50 77
50 77
50 77
50 77
49 50 77
49 50 77
49 50 77
49 50 77
47
0402
25VNP0-C0G
1000PF5%
C65011
47
0402
25VNP0-C0G
1000PF5%
C65021
send transients onto ADAPTER_SENSE when AC is connected.

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

When input voltage is 2V the FET will be off, blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will be on and power charger and 3.425V supply needs to guarantee 3.31V delivered to SMC VRef generator.

3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator.
1.5V S0 Switcher

Vout = 0.8V \times (1 + \frac{R_a}{R_b})

1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups \( R_a \) must be 5\( \Omega \) to support SSEP (not required in production).

Vout is required to support pull-ups. Alternative is string voltage divider (200/100) to 3.3V 5\( \Omega \), which burns 100mA in all S-states.

Max Current = 0.35A

Misc Power Supplies

- PP1V05_SUSP1V5S0_PGOOD
- PP3V3_SUS
- P1V5_S0_SW
- SWITCH_NODE=TRUE
- DIDT=TRUE
- PP3V3_S5

www.rosefix.com

www.vinafix.vn
1.5V S0 Audio Switch (BYPASSED) Loading specs per J41/43_PowerBudget_Riviera_rev0.99a

3.3V SUS Switch

3.3V S4 Switch

3.3V SSD Switch

3.3V S3 Switch

3.3V S0 Switch

3.3V Sensor Switch

1.05V PCH HSIO Switch

5V S0 Switch

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

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LCD PANEL INTERFACE (eDP)
NEEDS FINAL CHECK AGAINST UPDATE FOR NEW PANEL

CURRENT R(on) TYPE

R83311 1/20W 5%
R833012
201 MF
1KR8319
402 CERM
2
0
8 11 12 13 15 17 18 24 28 30
5 76 58 68 5
2

NO STUFF
1/20W 5%
0 201 MF

SOT833
B
A
B
A

VCC
GND
48

26.3V 10%

SLG5AP1443V
U8300
CRITICAL
VDD
GND
1

1M
201 MF
1/20W 5%

R83101
0.1 UF
1/16W 5%

C83091
0.1 UF
0201
402 MF-LF

0402 X7R-CERM
2
10 % 16V

R83091
100K
1/16W 5%

C83111
0.1 UF
16V 10%

0402 X7R-CERM

2

1 W
201 MF
1/20W 5%

NO_XNET_CONNECTION=TRUE

1 M
201 MF

1/20W 5%

NO_XNET_CONNECTION=TRUE

WWW.ROSEFIX.COM
WWW.VINAFIX.VN
RIO Power Connector

RIO FLEX CONNECTOR

NOTE: This connector is shielded 72P SineWave flat FPC 3659205-0, mates with FPC 3659205.

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<table>
<thead>
<tr>
<th>Stackup-Defined Spacing Rules</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width</td>
</tr>
<tr>
<td>0.058 mm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Width</th>
<th>Maximum Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>0.058 mm</td>
<td>0.101 mm</td>
</tr>
<tr>
<td>Bottom</td>
<td>0.058 mm</td>
<td>0.101 mm</td>
</tr>
</tbody>
</table>
CPU Signal Constraints

- CPU_VCCSENSE
- CPU_25MIL
- CPU_08MIL

- CPU_VCCSENSE
- CPU_27P4S
- CPU_VCCSENSE
- CPU_VCCSENSE_N

PCI Express Constraints

- PCIE_85D
- PCIE_TX
- PCIE_CAMERA_R2D

- PCIE_CLK100M_TBT
- PCIE_CLK100M_SSD

- PCIE_AP_D2R
- PCIE_AP_R2D

- PCIE_TBT_R2D
- PCIE_SSD_R2D

- PCIE_TBT_D2R
- PCIE_SSD_D2R

PCIE Express Properties

- PCIE_85D
- PCIE_TX
- PCIE_CAMERA_R2D

- PCIE_CLK100M_TBT
- PCIE_CLK100M_SSD

- PCIE_AP_D2R
- PCIE_AP_R2D

- PCIE_TBT_R2D
- PCIE_SSD_R2D

- PCIE_TBT_D2R
- PCIE_SSD_D2R
### SPI Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Electrical Coust Out</th>
<th>Physical Coust Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_LPC_45S</td>
<td>=45_OHM_SE</td>
<td>STANDARD</td>
</tr>
<tr>
<td>PCH_12MIL</td>
<td>0.305 MM</td>
<td>=27P4_OHM_SE</td>
</tr>
<tr>
<td>PCH_45S</td>
<td>*</td>
<td>7 MIL</td>
</tr>
<tr>
<td>SMB_45S</td>
<td>*</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>LPC_45S</td>
<td>*</td>
<td>45_OHM_SE</td>
</tr>
</tbody>
</table>

### SMBus Interface Constraints

<table>
<thead>
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</tr>
</thead>
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</tr>
<tr>
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<td>*</td>
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</tr>
<tr>
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<td>*</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>LPC_45S</td>
<td>*</td>
<td>45_OHM_SE</td>
</tr>
</tbody>
</table>

### HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Electrical Coust Out</th>
<th>Physical Coust Out</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0.305 MM</td>
<td>=27P4_OHM_SE</td>
</tr>
<tr>
<td>PCH_45S</td>
<td>*</td>
<td>7 MIL</td>
</tr>
<tr>
<td>SMB_45S</td>
<td>*</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>LPC_45S</td>
<td>*</td>
<td>45_OHM_SE</td>
</tr>
</tbody>
</table>

### SPI Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Electrical Coust Out</th>
<th>Physical Coust Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_LPC_45S</td>
<td>=45_OHM_SE</td>
<td>STANDARD</td>
</tr>
<tr>
<td>PCH_12MIL</td>
<td>0.305 MM</td>
<td>=27P4_OHM_SE</td>
</tr>
<tr>
<td>PCH_45S</td>
<td>*</td>
<td>7 MIL</td>
</tr>
<tr>
<td>SMB_45S</td>
<td>*</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>LPC_45S</td>
<td>*</td>
<td>45_OHM_SE</td>
</tr>
</tbody>
</table>

### PCH Single Net Constraints

<table>
<thead>
<tr>
<th>Net</th>
<th>Electrical Coust Out</th>
<th>Physical Coust Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCH_12MIL</td>
<td>0.305 MM</td>
<td>=27P4_OHM_SE</td>
</tr>
<tr>
<td>PCH_45S</td>
<td>0.355 OHM</td>
<td>2</td>
</tr>
<tr>
<td>PCH_15MIL</td>
<td>0.355 OHM</td>
<td>2</td>
</tr>
<tr>
<td>PCH_20MIL</td>
<td>0.355 OHM</td>
<td>2</td>
</tr>
</tbody>
</table>

### PCH Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>Electrical Coust Out</th>
<th>Physical Coust Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCH_12MIL</td>
<td>0.305 MM</td>
<td>=27P4_OHM_SE</td>
</tr>
<tr>
<td>PCH_45S</td>
<td>*</td>
<td>7 MIL</td>
</tr>
<tr>
<td>SMB_45S</td>
<td>*</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>LPC_45S</td>
<td>*</td>
<td>45_OHM_SE</td>
</tr>
</tbody>
</table>

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Drawn by:  

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Printed by:  

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Part number:  

Revision:  

Drawn at:  

Date:  

Location:  

Scale:  

Printed at:  

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### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Hspice / Netlist</th>
<th>Area Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_CTL2CTL_BM</td>
<td>=2x_DIELECTRIC*</td>
<td></td>
</tr>
<tr>
<td>MEM_CMD2CTL</td>
<td>=2x_DIELECTRIC</td>
<td></td>
</tr>
</tbody>
</table>

### Memory Net Properties

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_B_DQBYTE</td>
<td>0.305 MM</td>
</tr>
<tr>
<td>MEM_B_DQ</td>
<td>TOP, BOTTOM</td>
</tr>
</tbody>
</table>

### Spacing Rule Sets

<table>
<thead>
<tr>
<th>Rule Set</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_*</td>
<td>=2x_DIELECTRIC*</td>
</tr>
<tr>
<td>MEM_PWR</td>
<td>=SAME</td>
</tr>
</tbody>
</table>

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Group Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_<em><em>DQS</em></em></td>
<td>MEM_2OTHER</td>
</tr>
<tr>
<td>MEM_12MIL</td>
<td>0.305 MM</td>
</tr>
<tr>
<td>MEM_2GND</td>
<td>=2x_DIELECTRIC*</td>
</tr>
</tbody>
</table>

### Memory to GND Spacing

<table>
<thead>
<tr>
<th>Group Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_*<em>DQBYTE</em></td>
<td>=40_OHM_SE</td>
</tr>
<tr>
<td>MEM_2OTHER</td>
<td>=STANDARD*</td>
</tr>
</tbody>
</table>

### Haswell ULT Memory Down DDR3L 1x8 Length Matching

<table>
<thead>
<tr>
<th>Signal Group</th>
<th>Max Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLE to CLE</td>
<td>CLE + 500</td>
</tr>
<tr>
<td>ADDR (CMD)</td>
<td>ADDR + 100</td>
</tr>
<tr>
<td>SDRAM_DQS (DSM)</td>
<td>500</td>
</tr>
<tr>
<td>SDRAM_CLK (DSM)</td>
<td>250</td>
</tr>
<tr>
<td>SDRAM_DQS (DSM)</td>
<td>500</td>
</tr>
</tbody>
</table>

### Memory to Power Spacing

<table>
<thead>
<tr>
<th>Group Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_B_DQBYTE_</td>
<td>=85_OHM_DIFF</td>
</tr>
<tr>
<td>MEM_B_DQ</td>
<td>=85_OHM_DIFF</td>
</tr>
<tr>
<td>MEM_B_CTRL</td>
<td>=85_OHM_DIFF</td>
</tr>
<tr>
<td>MEM_B_CLK</td>
<td>=85_OHM_DIFF</td>
</tr>
</tbody>
</table>

### Memory Constraints

<table>
<thead>
<tr>
<th>Constraint Set</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_B_DQBYTE_</td>
<td>=85_OHM_DIFF</td>
</tr>
<tr>
<td>MEM_B_DQ</td>
<td>=85_OHM_DIFF</td>
</tr>
<tr>
<td>MEM_B_CTRL</td>
<td>=85_OHM_DIFF</td>
</tr>
<tr>
<td>MEM_B_CLK</td>
<td>=85_OHM_DIFF</td>
</tr>
</tbody>
</table>

---

Thunderbolt, DP, HDMI Constraints

Thunderbolt & DisplayPort Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source Layer</th>
<th>Connection Type</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_2SAME</td>
<td>TOP, BOTTOM</td>
<td>3x DIELECTRIC</td>
<td>&gt;6X</td>
<td>&gt;6X</td>
<td>&gt;3X</td>
<td>&gt;3X</td>
<td></td>
</tr>
<tr>
<td>HDMI_DATA</td>
<td>SAME</td>
<td>2x DIELECTRIC</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td></td>
</tr>
<tr>
<td>HDMI_DATA</td>
<td>OTHER</td>
<td>2x DIELECTRIC</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td></td>
</tr>
</tbody>
</table>

DisplayPort & HDMI Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source Layer</th>
<th>Connection Type</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D</td>
<td>DP_INT_ML_C</td>
<td>10X DIELECTRIC</td>
<td>&gt;10X</td>
<td>&gt;10X</td>
<td>&gt;10X</td>
<td>&gt;10X</td>
<td></td>
</tr>
<tr>
<td>DP_85D</td>
<td>DP_INT_ML_P</td>
<td>4X DIELECTRIC</td>
<td>&gt;4X</td>
<td>&gt;4X</td>
<td>&gt;4X</td>
<td>&gt;4X</td>
<td></td>
</tr>
</tbody>
</table>

Thunderbolt SPI Signal Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Source Layer</th>
<th>Connection Type</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBT_DP_2SAME</td>
<td>TOP, BOTTOM</td>
<td>3x DIELECTRIC</td>
<td>&gt;6X</td>
<td>&gt;6X</td>
<td>&gt;3X</td>
<td>&gt;3X</td>
<td></td>
</tr>
<tr>
<td>HDMI_DATA</td>
<td>SAME</td>
<td>2x DIELECTRIC</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td></td>
</tr>
<tr>
<td>HDMI_DATA</td>
<td>OTHER</td>
<td>2x DIELECTRIC</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td>&gt;2X</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- HDMI and DVI not used from DISPLAYPORT on TBT20.00 because it's not high speed, and no need routing space.
- Only used on dual-port hosts.
### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Type</th>
<th>Bandwidth</th>
<th>Distance</th>
<th>Layer</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2_MEM_CTRL</td>
<td>MIPI</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
<tr>
<td>S2_MEM_DATA</td>
<td>MIPI</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
<tr>
<td>S2_CMD2CMD</td>
<td>MIPI</td>
<td>2x</td>
<td>10x</td>
<td>TOP</td>
<td>DIELECTRIC</td>
</tr>
<tr>
<td>S2_MEM_DQS</td>
<td>MIPI</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
</tbody>
</table>

### Memory to Power Spacing

<table>
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<tr>
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</tr>
<tr>
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<td>DIELECTRIC</td>
</tr>
</tbody>
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### Memory to GND Spacing

<table>
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<tr>
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<td>S2_MEM_DQS</td>
<td>MIPI</td>
<td>2x</td>
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<td>DIELECTRIC</td>
</tr>
<tr>
<td>S2_MEM_DQS</td>
<td>MIPI</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
</tbody>
</table>

### Spacing Rule Sets

<table>
<thead>
<tr>
<th>Rule Set</th>
<th>Weight</th>
<th>Type</th>
<th>Bandwidth</th>
<th>Distance</th>
<th>Layer</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>RULE_1</td>
<td>70</td>
<td>DYNAMIC</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>RULE_2</td>
<td>70</td>
<td>DYNAMIC</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
<td></td>
</tr>
</tbody>
</table>

### MIPI Interface Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Bandwidth</th>
<th>Distance</th>
<th>Layer</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPI.Interface</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
<tr>
<td>MIPI.Interface</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
</tbody>
</table>

### Camera Net Properties

<table>
<thead>
<tr>
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<th>Bandwidth</th>
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<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPI.Interface</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
<tr>
<td>MIPI.Interface</td>
<td>2x</td>
<td>10x</td>
<td>BOTTOM</td>
<td>DIELECTRIC</td>
</tr>
</tbody>
</table>

---

**Sync:**
- Master: J44
- Date: 08/12/2013

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