### Table of Contents

<table>
<thead>
<tr>
<th>Page</th>
<th>Contents</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Table of Contents</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Power Block Diagram</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>ROM Configuration</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Revision History</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Functional / I/O Test</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Power Aliases</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Signal Aliases</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>LVDS</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>CPU Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>GPU Decoupling</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Extended Bus Alignments</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>MGP TP Interface</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>MGP Memory Interface</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>MGP Memory HSIC</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>MGP Rise Interfaces</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>MGP MOSFET &amp; Logic</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>MGP I/O &amp; I/Os</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>MGP Decoupling</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>MGP GND &amp; Bias</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>MGP Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>MGP Standard Decoupling</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>MGP Graphics Support</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>MGP Memory Decoupling</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>MGP DC/DC Power</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>MGP SD/MMC Decoupling</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>MGP SD/MMC Decoupling</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>MGP Support</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>High Current Connector</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>High Density Card Reader</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Ethernet PHY (STM32F1)</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Ethernet &amp; Network Support</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Ethernet PHY</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Firewire I/O (PCI) (FWM14)</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>Firewire I/O (PCI) (FWM14)</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>Firewire Ports</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>SATA Connectors</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>Serial I/O Connectors</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>Front Panel Support</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>IMM</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>NIC Support</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>LPC/PS/USB Debug Connector</td>
<td></td>
</tr>
</tbody>
</table>

### Integration Issues to be Resolved

- [ ] LVDS Signals must be referenced to +3.3V/0V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
- [ ] LVDS Signals must be referenced to +3.3V
- [ ] USB Signal Calm to +3.3V
- [ ] Power Supplies must be referenced to +3.3V
- [ ] IO Interconnect must be referenced to +3.3V
## BOM Variant

<table>
<thead>
<tr>
<th>Part Number</th>
<th>BOM Group</th>
<th>BOM Options</th>
<th>Critical</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## BOM Groups

<table>
<thead>
<tr>
<th>Part Number</th>
<th>BOM Options</th>
<th>Critical</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Module Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Programmable Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Development BOM

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Alternate Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## BOM Configuration

<table>
<thead>
<tr>
<th>BOM Variant</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it
II. Not to reveal or publish in whole or part
III. To maintain the document in confidence

NOTICE OF PROPRIETARY PROPERTY
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
Current numbers from Merom for Santa Rosa EMTs, doc #20905.

SYNC FROM T18

8 7 6 5 4 3 2 1

AB18
AB17
AB15
AB14
AB12
AB10
AA20
AA18
AA17
AA15
AA13
AA12
AA10
AA9
AA7
D18
D17
D15
B20
B18
B17
B15
A15
C18
C17
C15
C13
C12
F20
F18
F17
E18
E17
E15
F14
E13
E12
D15
B20
E10
D14
B18
D12
B17
D10
B15
A15
C10
B14
A13
B12
A12
B10
A20
A17
A10
A18

www.vinafix.vn
CHANGE C1240-C1243 AND C1260 FROM 128S0241 (9 MILLI-OHM) TO 128S0231 (6 MILLI-OHM)

REMOVE C1244 & C1245

REMOVE NO STUFF CAPS C1220 TO C1231

SYNC FROM T18

CPU VCore HF and Bulk Decoupling

PLACEMENT NOTE (C1240-C1243):
Place inside socket cavity on secondary side.

PLACEMENT NOTE (C1250-C1260):
Place inside socket cavity on secondary side.

PLACEMENT NOTE (C1200-C1219):
4X 330UF, 20X 22UF 0805

CPU VCore HF and Bulk Decoupling

SYNC_DATE=02/05/2009
SYNC_MASTER=K24_MLB

APPLE INC.

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

NOTICE OF PROPRIETARY PROPERTY

DRAWING NUMBER
SHT OF
REV.
SIZE
SCALE

www.vinafix.vn
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0630 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

on even-numbered side of J1300

Please avoid any obstructions
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.
If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

Apple: 1x 2.2uF 0402 (2.2 uF)

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

190 mA (A01, 1.8V)
16 mA (A01)

Apple: ???

206 mA (A01)

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
RTC Power Source

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

System Reset Circuit

Platform Reset Connections

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)
DDR3 RESET Support

Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

3.3V S5 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

PP3V3_S5

MEM_RESET
MEM_RESET_L

PP1V5_S3

MEM_RESET
MEM_RESET_L

R3309
R3310
C3300
R3300
R3301
Q3305

R3305
10K
R3309
100K

1/16W
MF-LF
5%

10V
0.1UF
20%
CERM
402

1/16W
MF-LF
5%

1K

www.vinafix.vn
WLAN Enable Generation

NOTE: S3 term is guaranteed by 33 pull-up on open-drain AP_PWR_EN signal.

1.05V ENET FET

RDL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PPM is powered whenever RMGT rails are, or use separate crystal.

Ethernet & AirPort Support
The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it
II. Not to reveal or publish in whole or part
III. To maintain the document in confidence

NOTICE OF PROPRIETARY PROPERTY
DRAWING NUMBER
SHT OF
SIZE

Page Notes

Transformers should be mirrored on opposite sides of the board.

PLACEMENT_NOTE=Place one of 0.1uf caps close to each center tap pin of transformer

R3900, R3901, R3902, R3903

Critical

402-1
10PF
50V
CERM

PLACEMENT_NOTE=Place on MDI lines so there are no stubs all 8 caps.

C3902, C3903, C3904, C3905, C3906

0.1UF
10%
16V
402X5R

Critical

Enet_Conn_CTAP

Enet Conn_CTAP

EnetConn_CTAP
We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

Left USB Port B

Port Power Switch

Left USB Port A

External USB Connectors

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: NOT TO REPRODUCE OR COPY IT, NOT TO REVEAL OR PUBLISH IN WHOLE OR PART, TO MAINTAIN THE DOCUMENT IN CONFIDENCE.
MCP MEM VDD Current Sense / Filter

MCP VCore Current Sense Filter

MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter

Battery (BMON) Current Sense, MUX & Filter

CPU VCore Load Side Current Sense / Filter

DC-IN (AMON) Current Sense Filter

**Current Sensing**

---

**PLACEMENT_NOTE:** Place near sense resistor.

**PLACEMENT_NOTE:** Place close to SMC (For R's and C)

**PLACEMENT_NOTE:** Place close to SMC

**PLACEMENT_NOTE:** Place close to SMC

**PLACEMENT_NOTE:** Place near sense resistor.

**PLACEMENT_NOTE:** Place close to SMC (For R and C)

**PLACEMENT_NOTE:** Place close to SMC

**PLACEMENT_NOTE:** Place close to SMC

**PLACEMENT_NOTE:** Place close to SMC

**PLACEMENT_NOTE:** Place close to SMC

---

**APPLE INC.**

---

**III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

**PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR**

**THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY**

**PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR**

**NOTICE OF PROPRIETARY PROPERTY**

---

www.vinafix.vn
CPU T-Diode Thermal Sensor

DETECT CPU DIE TEMPERATURE

DETECT FIN-STACK TEMPERATURE

PLACEMENT NOTE: PLACE U5515 NEAR CPU

MCP T-Diode Thermal Sensor

DETECT MCP DIE TEMPERATURE

DETECT HEAT-PIPE TEMPERATURE

PLACEMENT NOTE: PLACE U5535 NEAR MCP

REPLACED 518S0521 WITH 518S0519

NOTE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT

II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

NOTICE OF PROPRIETARY PROPERTY

SMC_FAN_0_CTL

PP5V_S0

PP3V3_S0

SMC_FAN_0_TACH

FAN_RT_TACH

FAN_RT_PWM

CRITICAL

CRITICAL

SYNC_MASTER=K24_MLB

SYNC_DATE=02/05/2009
Analog SMS

R5921 pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC.

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.

Sudden Motion Sensor (SMS)

SMS_X_AXIS
SMS_Y_AXIS
SMS_Z_AXIS
SMS_PWRDN
SMS_SELFTEST
PP3V3_S3

Circle indicates pin 1 location when placed in correct orientation.

www.vinafix.vn
### Frequency Selection

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI_MUX</th>
<th>SPI_CLK_MUX</th>
</tr>
</thead>
<tbody>
<tr>
<td>42 MHz</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>25 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>31 MHz</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- Any of the 4 frequencies can be selected.

25MHz is selected with R5190 and R5191.

Any of the 4 frequencies may be selected with R6190, R6191, R5190 and R5191.
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 Hz
VIN = 2VRMS, CODEC VIN = 1.21 VRMS

R6301 10K 1/16W MF-LF
R6302 10K 1/16W MF-LF
R6311 16.5K 1/16W MF-LF
R6300 10K 1/16W MF-LF
C6301 3.3UF 10 V CERM-X5R805-1
C6311 3.3UF 10 V CERM-X5R805-1
C6302 3.3UF 10 V CERM-X5R805-1
C6312 3.3UF 10 V CERM-X5R805-1
C6303 15PF 50 V CERM402
C6313 15PF 50 V CERM402

AUDIO: LINE INPUT FILTER

MIN_NECK_WIDTH=.1MM
MIN_LINE_WIDTH=.1MM
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

- **R6501**: 5%1/16W
- **C6500**: 0.1UF X7R-CERM 402 10% 16V
- **R6502**: 5%1/16W
- **C6501**: 0.0022UF CERM402 10% 50V
- **R6510**: 5%1/16W
- **C6510**: 0.0022UF CERM402 10% 50V
- **R6511**: 5%1/10W
- **C6511**: 0.1UF X7R-CERM 402 10% 16V
- **R6512**: 5%1/10W
- **C6512**: 0.0022UF CERM402 10% 50V
MagSafe DC Power Jack

1-Wire OverVoltage Protection

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

3.425V "G3Hot" Supply

DC-In & Battery Connectors

www.vinafix.vn
1.5V 5.0FET

MCP79 DDR VT FET

MCP79 power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage闩锁, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 DDR VT FET

5.0V S0 FET

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.

MCP79 Power path leakage is high enough that MCP79 must be bypassed to prevent damage. Removing MCP79 in order to bypass overvoltage latch, however, may cause damage to the VTT rail. Before VTT rail is turned off, ensure that all of the signals used to pull the MCP79 output low are turned off. Ensure that any bypass capacitors are fully discharged before VTT rail is turned off. The MCP79 must be bypassed permanently.
Display Port Interoperability says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP or sinks which do both DP and DVI has 10k pull up on the lines).
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

NOTICE OF PROPRIETARY PROPERTY

LCD Backlight Support

MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

LOADING 0.4 A (EDP)

FDC638APZ

43 mOhm @4.5V

P-TYPE MOSFET

PPBUS S0 LCDBKLT_PWR

VOLTAGE=12.6V

MIN_LINE_WIDTH=0.4 mm

MIN_NECK_WIDTH=0.25 mm

PPBUS S0 LCDBKLT_EN_DIV

PPBUS S0 LCDBKLT_EN_L

PPBUS_G3H

MIN_LINE_WIDTH=0.4 mm

MIN_NECK_WIDTH=0.25 mm

VOLTAGE=12.6V

LCD_BKLT_PWM

8 17 73

8 17 72 74
MCP FSB COMP Signal Constraints

Some signals require 27.4-ohm single-ended impedance.
Most CPU signals with impedance requirements are 55-ohm single-ended.

Design Guide recommends each stray/signal group is routed on the same layer. Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: 7 mil gap is for VCCsense pairs, which Intel says to route with 7 mil spacing without specifying a target impedance.

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
**Memory Bus Spacing Group Assignments**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>Spacing Rule Set</th>
<th>Net Spacing Type 1</th>
<th>Net Spacing Type 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_CTRL</td>
<td>MEM_CTRL2MEM</td>
<td>MEM_DATA</td>
<td>MEM_DATA2MEM</td>
</tr>
<tr>
<td>MEM_DQS</td>
<td>MEM_DQS2MEM</td>
<td>MEM_CLK</td>
<td>MEM_CLK2MEM</td>
</tr>
</tbody>
</table>

**Memory Bus Constraints**

- DQ signals should be matched within 3 ps of associated DQS pair.
- DDR2: intra-pair matching should be within 1 ps, no inter-pair matching requirement.
- DDR3: intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
- CLA intra-pair matching should be within 1 ps, no inter-pair matching requirement.
- All memory signals maximum length is 1.05 ps. CLK minimum length is 586 ps (lengths include substrate).
- DQ/CLK/CLA signal spacing in 3x dielectric, DQ/CLK is 3x dielectric.

**Memory Net Properties**

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_B_DQ_BYTE7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;7&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Memory Constraints**

- Need to support MEM_*-style wildcards!
# SPI Interface Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI_MISO</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>SPI_MOSI</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# SMBus Interface Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMB_MCLK</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>SMB_MDATA</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# USB 2.0 Interface Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_DP</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>USB_DM</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# LPC Bus Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPC_CLK0</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>LPC_CLK1</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# PCI Bus Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI_D0</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>PCI_D1</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDA_SDIN</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>HDA_SDOUT</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# SIO Signal Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIO_SIN</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>SIO_SOUT</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

# MCP Constraints 2

<table>
<thead>
<tr>
<th>Signal</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
<th>Differential Pair Separation</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP_CS0</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>MCP_CS1</td>
<td>8 MIL</td>
<td>6 MIL</td>
<td>100 MIL</td>
<td>20 MIL</td>
</tr>
</tbody>
</table>

---

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.x.
### SD Card Net Properties

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SD_CLK</td>
<td>DIFFPAIR AUDIO</td>
<td>1</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
<tr>
<td>SD_D&lt;7&gt;</td>
<td>DIFFPAIR AUDIO</td>
<td>1</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
<tr>
<td>SD_D&lt;5&gt;</td>
<td>DIFFPAIR AUDIO</td>
<td>1</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
<tr>
<td>SD_D&lt;4&gt;</td>
<td>DIFFPAIR AUDIO</td>
<td>1</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
</tbody>
</table>

### SD Card Interface Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Type</th>
<th>Min. Size</th>
<th>Max. Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRIMARY GAP</td>
<td>DIFFPAIR</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
<tr>
<td>DIFFPAIR NECK GAP</td>
<td>PHYSICAL RULE SET</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
</tbody>
</table>

### Memory Constraint Relaxations

Memory constraint relaxations are provided for specific nets, allowing 0.127 mm necks for >0.127 mm lines for MCP fanout.

### MCP Fanout Constraint Relaxations

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Type</th>
<th>Min. Size</th>
<th>Max. Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRIMARY GAP</td>
<td>DIFFPAIR</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
<tr>
<td>DIFFPAIR NECK GAP</td>
<td>PHYSICAL RULE SET</td>
<td>0.09 mm</td>
<td>5.8 mm</td>
</tr>
</tbody>
</table>

---

**K19i Specific Net Properties**

**K19i Specific Constraints**

The information contained herein is the proprietary property of Apple Inc. Its reproduction or distribution in whole or in part is not permitted without the express written consent of Apple Inc.
<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ST otarian</td>
<td>0.330 MM</td>
<td>0.330 MM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
</tr>
</tbody>
</table>

**Area Type**

- **Size**: 8383
- **Drawing Number**: SHT 051-7903

**Page Numbers**: A, B, C, D

**NOTE**: Not to reveal or publish in whole or part.

**Notice of Proprietary Property**: I agree to maintain the document in confidence.

---

**K19i Board-Specific Physical & Spacing Constraints**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
</tr>
</tbody>
</table>

**Table of Physical Rule Head**:

- **TABLE_PHYSICAL_RULE_HEAD**
  - **ON LAYER?**
    - STANDARD
  - **MINIMUM LINE WIDTH**
    - 0.077 MM
  - **ALLOW ROUTE**
    - 1.1 MM
  - **TABLE_PHYSICAL_RULE_ITEM**
    - 110_OHM_DIFF
    - 0.095 MM
    - 0.095 MM
    - 0.095 MM
    - 0.095 MM

**Table of Physical Assignment Item**

- **TABLE_PHYSICAL_ASSIGNMENT_ITEM**
  - **ISL3, ISL4, ISL9, ISL10**
  - **ISL3, ISL4, ISL9, ISL10**
  - **ISL3, ISL4, ISL9, ISL10**

**Table of Spacing Rule Item**

- **TABLE_SPACING_RULE_ITEM**
  - **LINE-TO-LINE SPACING**
    - **LAYERS**
      - 0.1 MM
    - **SPACING_RULE_SET**
      - 0.1 MM
    - **WEIGHT**
      - 0.1 MM

**Table of Spacing Assignment Item**

- **TABLE_SPACING_ASSIGNMENT_ITEM**
  - **AREA_TYPE**
    - **SPACING_RULE_SET**
      - **NET_PHYSICAL_TYPE**
        - **NET_SPACING_TYPE1**
          - **NET_SPACING_TYPE2**
            - 0.1 MM
            - 0.1 MM
            - 0.1 MM
            - 0.1 MM

**Table of Board Info**

- **TABLE_BOARD_INFO**
  - **5X_DIELECTRIC**
    - **TOP, BOTTOM**
      - 0.350 MM
  - **4X_DIELECTRIC**
    - **TOP, BOTTOM**
      - 0.280 MM
  - **3X_DIELECTRIC**
    - **TOP, BOTTOM**
      - 0.210 MM
  - **2X_DIELECTRIC**
    - **TOP, BOTTOM**
      - 0.140 MM

**K19i PCB Rule Definitions**

**TABLE_SPACING_ASSIGNMENT_HEAD**

- **SYNC MASTER**
  - **WFERRY_K19I**
  - **SYNC DATE**
    - 12/12/2008