K23F MLB

LAST_MODIFIED=Mon Dec 7 09:47:19 2009

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/-5%.
2. ALL CAPACITANCE VALUES ARE IN MICRO-FARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
This page contains a diagram labeled "CPU/PCH GFX DECOUPLING." The diagram includes various annotations and details such as:

- Grounding the rail because Integrated Graphics won't be used.
- R1750, R1751, R1760, R1765: Resistor values and tolerances are specified.
- PP3V3_S0_PCH_VCCA_DAC = PP3V3_S0_PCH_VCCADAC
- PP1V05_S0_PCH_VCCAD_PLLA
- PP1V05_S0_PCH_VCCAD_PLLB
- VOLTAGE = 3.3V
- MIN NECK WIDTH = 0.2 MM
- MIN LINE WIDTH = 0.4 MM
- VOLTAGE = 1.05V
- PPVAXG_S0_CPU

The diagram also includes a notice of proprietary property and copyright information.

www.vinafix.vn
DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

EXTRA DECOUPLING CAPS FOR CPU MEM RAIL

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

www.vinafix.vn
AP POWER ENABLE CIRCUIT

AP_PWR_EN = S0 || (S3 && AP_EN)

L3400 518S0731

C3400 10V 0.1uF 402 20%

C3401 CERM 0.1uF 10V 20% 402

C3402 10uF 6.3V X5R 20% 603

C3430 0.1uF 16V 10% X5R 402

C3431 0.1uF 16V 10% X5R 402

L3400 0402-LF FERR-120-OHM-1.5A

L3430 DLP11S 90-OHM-100MA PLACEMENT_NOTE=PLACE CLOSE TO J3400.

Q3401 NOSTUFF FDC606P_G SOT-6

Q3402 NOSTUFF SOT-6

Q3403 NOSTUFF SOT23-HF1 2N7002

Q3407 NOSTUFF SOT23-HF1 2N7002

R3461 10K 402 LF 5% 1/16W

R3462 0.805 LF 5% 1/8W

C3461 0.1UF X5R 402

C3462 0.1UF X5R 402

R3466 805 1/8W LF 5%

SYNC_DATE=07/16/2009
SYNC_MASTER=K23_AARON

PP3V3_MINI_FILT VOLTAGE=3.3V MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.5 mm

PP3V3_MINI VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
CAESAR II DECOUPLING

ENET POWER ENABLE CIRCUIT

ENET_PWR_EN = "SS" || (S2 power && SML_ERR)

CAESAR II 1V2 RAIL SUPPLY

CAESAR II LED SUPPORT

PP3V3_ENET
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=3.3V

www.vinafix.vn
For single-port systems, all FW power should come from bus power. For multi-port systems, FW power is required to be used for all ports. The FW power should be connected to the designated pins on the PCB. The power supply should be designed to handle the required current for each port. The capacitors and resistors should be selected based on the power requirements and the available supply voltage. The components should be placed according to the placement notes provided in the schematic.
POUT = 6.76 W INTO 8 OHMS # 1% THD+N
AMP VOUT = 7.355VRMS
CODEC OUT = 1.335VRMS
GAIN = -4.8(20K/17.4K)
**MIKEY RECEIVER CKT**

WRITE: 0x72  READ: 0x73  APN 353S2256

---

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>PIN</th>
<th>Converter</th>
<th>Volume</th>
<th>Enable/</th>
<th>Ctrl Type</th>
<th>Detect/Interrupt</th>
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</table>

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Audio: Mikey

Apple Inc.

051-8233

G.0.0

61 of 92
IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT  = 1.05V
PEAK  = 7.5A
AVG   = 3A

PP12V_S0_PCH_CORE_VREG
PP5V_S0_PCH_CORE_VREG
PP3V3_S0_PCH

PCHCORE_REG_5V_FLT
PCHCORE_REG_BOOT_R
PCHCORE_REG_UGATE
PCHCORE_REG_BOOT
PCHCORE_REG_TON
PCHCORE_REG_EN
PCHCORE_REG_VFB
PCHCORE_REG_PGOOD
AGND_PCHCORE_REG
PCHCORE_REG_TRIP
PCHCORE_REG_PGND_XW
PCHCORE_REG_PHASE_C
PCHCORE_REG_PCHCORE_REG_PHASE
PCHCORE_REG_MIN_LINE_WIDTH=0.6MM
PCHCORE_REG_MIN_NECK_WIDTH=0.2MM
PCHCORE_REG_DIDT=TRUE

IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

IBEX PEAK CORE

Apple Inc.
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

1.05V S5 SUPPLY

REMOVE for K60/K61
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Any options provided by this page:

Pullups & Pulldowns at MXM Connector

Aliases required by this page:

Page Notes

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MXM I/O

Apple Inc.

MXM I/O

Page Notes

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### MXM TX CAPS

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<thead>
<tr>
<th>Component</th>
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<th>Location</th>
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</tr>
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<td>C8659</td>
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<td>IN</td>
</tr>
<tr>
<td>C8657</td>
<td>0.1UF</td>
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<td>IN</td>
</tr>
<tr>
<td>C8654</td>
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Unused MXM Interfaces

- MXM_CLKX2_A_CLK_P
- MXM_CLKX2_A_CLK_N
- MXM_CLKX2_B_CLK_P
- MXM_CLKX2_B_CLK_N
- MXM_CLKX2_C_CLK_P
- MXM_CLKX2_C_CLK_N
- MXM_CLKX2_D_CLK_P
- MXM_CLKX2_D_CLK_N

Unused MXM DP Interfaces

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- MXM_DP_B_ML_N<0..3>
- MXM_DP_B_AUX_P
- MXM_DP_B_AUX_N
- MXM_DP_D_ML_P<0..3>
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- MXM_DP_D_AUX_P
- MXM_DP_D_AUX_N

Display: Aliases

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- MXM_LVDS_B_CLK_N
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- MXM_LVDS_A_CLK_P
- MXM_LVDS_A_CLK_N
- NO_TEST=TRUE
- MAKE_BASE=TRUE

Power aliases required by this page:

- NONE

Signal aliases required by this page:

- NONE

BOM options provided by this page:

- NONE
INTERNAL DP INTERFACE

Panel Power Control

- LCD PANEL_PWR_L
- LCD PANEL_PWR_L_RC
- LCD PANEL_PWR_L_DIV
- LCD PANEL_PWR_G

Options for GPU or MLB HW controlled backlight enable are included only when Panel has valid video guarantee backlight is enabled.

Backlight Control Support

Supports backlight is only on when Panel has valid video. Options for GPU or MLB controlled backlight enable are included.

Display: Int DP Connector
Apple Inc. 051-8233 D

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Apple Inc.
EQ & Re-Driver for DP source

DisplayPort Mux 1
Analog mux at External Connector

Common mode bias for Tx EQ AUX interception

From iMac GPU

IN
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Display: BiDiVi Mux1

Apple Inc.

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### PHYSICAL RULE SET

#### PHYSICAL CONSTRAINTS

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<th>MINIMUM LINE WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
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<td>0.320 MM</td>
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#### TABLE PHYSICAL ASSIGNMENT ITEM

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<td>TOP</td>
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<td>0.320 MM</td>
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<tr>
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#### TABLE PHYSICAL RULE_ITEM

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**HD Audio Interface Constraints**

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**LPC Bus Constraints**

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**USB 2.0 Interface Constraints**

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**SPI Interface Constraints**

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**XTAL Constraints**

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</table>
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
### SMBus Interface Constraints

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<thead>
<tr>
<th>PHYSICAL_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
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### SNS_NET PROPERTIES

- **SNS_CPU_THERMD_P**: SNS_CPU_THERMD_P
- **SNS_CPU_THERMD_N**: SNS_CPU_THERMD_N
- **SNS_AMB_P**: SNS_AMB_P
- **SNS_AMB_N**: SNS_AMB_N
- **SNS_SKIN_P**: SNS_SKIN_P
- **SNS_SKIN_N**: SNS_SKIN_N
- **SNS_CPU_H_P**: SNS_CPU_H_P
- **SNS_CPU_H_N**: SNS_CPU_H_N
- **SNS_ODD_P**: SNS_ODD_P
- **SNS_ODD_N**: SNS_ODD_N
- **SNS_LCD_P**: SNS_LCD_P
- **SNS_LCD_N**: SNS_LCD_N
- **SNS_T_DP1_DN6**: SNS_T_DP1_DN6
- **SNS_T_DP2_DN3**: SNS_T_DP2_DN3

### SMC THERMAL NET PROPERTIES

- **SMCU2 núi**: NCU2 núi
- **SMCU2 núi**: NCU2 núi
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### SMC VOLTAGE/CURRENT NET PROPERTIES

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### SMC GPU VSENSE NET PROPERTIES

- **SENSE_CPU_VTT1_P**: SENSE_CPU_VTT1_P
- **SENSE_CPU_VTT_N**: SENSE_CPU_VTT_N

### SMC CPU VTT nets

- **SENSE_CPU_VTT1_P**: SENSE_CPU_VTT1_P
- **SENSE_CPU_VTT_N**: SENSE_CPU_VTT_N