K24 MLB SCHEMATIC

PVT RELEASE

5/6/2009
### K24 BOARD STACK-UP

**Top**
- **2** SIGNAL
- **3** SIGNAL (High Speed)
- **4** SIGNAL (High Speed)
- **5** POWER
- **6** GROUND
- **7** SIGNAL (High Speed)
- **8** SIGNAL (High Speed)
- **9** GROUND
- **10** SIGNAL (High Speed)
- **11** GROUND

**Bottom**
- **SIGNAL**

---

### DEVELOPMENT BOM

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<th>PART NUMBER</th>
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### Module Parts

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### Bar Code Labels / EEE #'s

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### BOM Configuration

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www.vinafix.vn
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CHANGE C1240-C1243 AND C1260 FROM 128S0241 (9 MILLI-OHM) TO 128S0231 (6 MILLI-OHM)

REMOVE C1244 & C1245

REMOVE NO STUFF CAPS C1220 TO C1231

SYNC FROM T18
Mini-XDP Connector

NOTE: This is not the standard XDP pinout. Use with XDP-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

998-1571
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

www.vinafix.vn
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

www.vinafix.vn
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: 20K pull-down required on DP_HPD_DET.

DP_IG_AUX_CH_P/N = MCP_HDMI_DDC_CLK
= MCP_HDMI_TXD_P/N<1>
= MCP_HDMI_TXD_P/N<0>

TMDS_IG_TXD_P/N<2>
TMDS_IG_TXD_P/N<1>
TMDS_IG_TXD_P/N<0>
TMDS_IG_TXC_P/N
TMDS/HDMI

= PP3V3_ENET_MCP_RMGT

DP_IG_CA_DET
LPCPLUS_GPIO

Flattened diagram.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

**NOTE:** All Apple products set strap to 0. Apple products will enable feature via software. This avoids a leakage issue since MII, RGMII products will enable feature even if strap is set to 1.

**SYNC_MASTER=T18_MLB**

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Current numbers from email: January 2021

MCP SATA & USB

If all GND pins are not used, ground GND9, GND7, and GND4, GND6. If all GND pins are not used, ground GND1, GND3, and GND5, GND6.

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### MCP Decoupling

**MCP 3.3V/1.5V HDA Power**
- MCP 3.3V AUX/USB Power: 450 mA (A01)
- MCP Memory Power: 1182 mA (A01)
- MCP FSB (VTT) Power: 131 mA (A01)

**MCP 1.05V AUX Power**
- 57 mA (A01)

**MCP PCIE (DVDD) Power**
- 105 mA (A01)

**MCP Standard Decoupling**

- Apple: 1x 2.2uF 0402 (2.2 uF)
- NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
- NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
- NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)

**Current Numbers from Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).**
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
WF in 4.7uF 0603, in 0.1uF 0402 (4.8 uF)
Apple in 2.2uF 0402 (2.2 uF)

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

8765432187654321

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MCP Graphics Support

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for but results in MCP79 ROMSIP sequence happening after CPU powers up.

NO STUFF

SUPERCAP_YES

NO STUFF

R2816

MCP 25MHz Crystal

RTC Crystal

MCP 25MHz Crystal
**DDR3 RESET Support**

Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

2.3V is used because MEM_RESET must be high before 1.8V starts to rise to avoid glitch on MEM_RESET_L.

---

**DDR3 Support**

- **SYNC_MASTER=T18_MLB**
- **SYNC_DATE=04/04/2008**

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RXDLY = 0  (RXCLK transitions with data)

Configuration Settings:

HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.

ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM

This page contains diagrams and schematics related to the Ethernet PHY (RTL8211CL)

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WLAN Enable Generation

3.3V ENET FET

1.05V ENET FET

RTL8211 25MHz Clock

Ethernet & AirPort Support
FireWire Design Guide (FWDG 0.6, 5/14/03)

The FireWire PHY page is used to implement the FireWire TPA/TPB XNets to their proper terminations and signal integrity.

**Signal aliases required by this page:**
- PP3V3_FW_LATEVG
- PPVP_FW_PORT1

**Power aliases required by this page:**
- FW_P1_TPA_P
- FW_P1_TPB_P
- FW_PHY_DS1
- FW_PHY_DS2
- FW_PHY_DS3
- FW_PHY_DS0

**Netlist elements:**
- R4364: 4.99K Ohm, 1/16W, MF-LF, 1%
- R4382: 10K Ohm, 1/16W, MF-LF, 1%
- C4310: 0.01uF, X7R, 50V, 10%
- C4319: 0.1uF, X7R, 50V, 10%
- C4311: 0.01uF, X7R, 50V, 10%
- C4314: 0.01uF, X7R, 50V, 10%

**Notes:**
- PP2V4_FW_LATEVG needs to be biased to at least 2.1V for FW signal integrity when connected to a non-loopback device, and should be biased as close to 2.1V for operation.
- PP2V4_FW_LATEVG needs to be biased to at least 2.1V for FW signal integrity when connected to a non-loopback device, and should be biased as close to 2.1V for operation.
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- PP2V4_FW_LATEVG needs to be biased to at least 2.1V for FW signal integrity when connected to a non-loopback device, and should be biased as close to 2.1V for operation.
- PP2V4_FW_LATEVG needs to be biased to at least 2.1V for FW signal integrity when connected to a non-loopback device, and should be biased as close to 2.1V for operation.
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

PLACEMENT_NOTE=PLACE C4525 NEXT TO C4526
PLACEMENT_NOTE=PLACE FL4501 close to J4501
PLACEMENT_NOTE=PLACE L4500 close to J4501
PLACEMENT_NOTE=Place C4516 close to J4501
PLACEMENT_NOTE=PLACE C4520 CLOSE TO MCP79
PLACEMENT_NOTE=Place FL4525 close to J4500
PLACEMENT_NOTE=Place C4510 close to MCP79
PLACEMENT_NOTE=Place C4511 next to C4510
PLACEMENT_NOTE=PLACE C4502 CLOSE TO J4501

CRITICAL
SYM VER-1
We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

External USB Connectors
Alternate SPI ROM Support

SPI MUX BYPASS

LPC+SPI Connector
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A THERMAL SENSORS

SIGNAL_MODOL=EMPTY

MIN_LINE_WIDTH=0.25 mm

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.25 mm

REPLACED 518S0521 WITH 518S0519

DETECT HEAT-PIPE TEMPERATURE

REPLACED 518S0519 WITH 518S0521

DETECT MCP PROXIMITY TEMPERATURE

DETECT MCP DIE TEMPERATURE

DETECT CPU DIE TEMPERATURE

DETECT FIN-STACK TEMPERATURE

CPU T-Diode Thermal Sensor

INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE

INTERNAL DIODE IN U5515 DETECTS CPU PROXIMITY TEMPERATURE

INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE

INTERNAL DIODE IN U5515 DETECTS CPU PROXIMITY TEMPERATURE

PLACEMENT NOTE: PLACE U5515 NEAR CPU

PLACEMENT NOTE: PLACE U5535 NEAR MCP

CPU THERM/ADDR

ALERT*

THRM_PAD

DN2/DP3

DP2/DN3

VDD

SMDATA

SMCLK

GND

DN1

DP1

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REV. A

DRAWING NUMBER

SHT OF SIZE

A4 R

DATE

4.7.0

W/1

9C6

80D3

9C6

80D3

20C3

80D3

20C3

80D3

M-RT-SM

NOSTUFF

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To detect Keyboard backlight, SMC will
LOW = keyboard backlight present
HIGH = keyboard backlight not present

R5811, R5812, C5818 modified

- R5812, R5813, C5818 modified
- BOOST_FB = VLF3010AT-SM-HF
- Z2_BOOST_EN = VPS02-4.5V-S3
- Z2_CLKIN = 10UH-0.58A-0.35OHM
- Z2_SCLK = 1098AS-SM
- Z2_MOSI = CRITICAL
- Z2_MISO = CRITICAL
- Z2_RESET = CRITICAL
- Z2_CS_L = CRITICAL
- Z2_DEBUG3 = CRITICAL
- Z2_LED = 4.7K
- Z2_MISO = 10K
- C5817 = 0.1UF
- C5819 = 603-1
- R5811 = 100K
- R5813 = 71.5K
- C5818 = 39PF
- C5838 = 0.1UF
- C5850 = 7
- R5873 = 2.2UF
- C5854 = 4.7UF
- R5836 = 1/16W
- R5852 = 1/16W
- R5853 = 1/16W
- R5856 = 1/16W
- R5857 = 1/16W
- R5858 = 1/16W
- R5859 = 1/16W
- R5860 = 1/16W
- R5861 = 1/16W
- R5862 = 1/16W
- R5863 = 1/16W
- R5864 = 1/16W
- R5865 = 1/16W
- R5866 = 1/16W
- R5867 = 1/16W
- R5868 = 1/16W
- R5869 = 1/16W
- R5870 = 1/16W
- R5871 = 1/16W
- R5872 = 1/16W
- R5873 = 1/16W
- R5874 = 1/16W
- R5875 = 1/16W
- R5876 = 1/16W
- R5877 = 1/16W
- R5878 = 1/16W
- R5879 = 1/16W
- R5880 = 1/16W
- R5881 = 1/16W
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- R5884 = 1/16W
- R5885 = 1/16W
- R5886 = 1/16W
- R5887 = 1/16W
- R5888 = 1/16W
- R5889 = 1/16W
- R5890 = 1/16W
- R5891 = 1/16W
- R5892 = 1/16W
- R5893 = 1/16W
- R5894 = 1/16W
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.

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LINE INPUT VOLTAGE DIVIDER

- CODEC RIN = 20K OHMS
- CODEC GND = 10.16K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
- FC_HP = 3.6 HZ
- FC_LP = 43KHZ
- MIN_LINE_WIDTH=.1MM
- MIN_NECK_WIDTH=.1MM

**Audio: Line Input Filter**

- VIN = 2VRMS, CODEC VIN = 1.14 VRMS
- MIN_LINE_WIDTH=.1MM
- MIN_NECK_WIDTH=.1MM

**Component Values:**
- C6301: 2.2UF, X5R-CERM, 20%
- C6302: 2.2UF, X5R-CERM, 20%
- C6303: 820PF, CERM, 10%
- C6311: 820PF, CERM, 10%
- R6300: 7.87K MF-LF, 1/16W, 1%
- R6301: 7.87K MF-LF, 1/16W, 1%
- R6302: 21.5K MF-LF, 1/16W, 1%
- R6311: 21.5K MF-LF, 1/16W, 1%
- R6312: 21.5K MF-LF, 1/16W, 1%

**Critical Components:**

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MCP VCORE POWER SUPPLY

- MCP CORE REGULATOR
  - f = 300 kHz
- MCP VIDEO
  - SW
  - FDMC8678S MICROFET3X3
  - Q7565 FDMC8676 POWER33-SM CRITICAL

- MCP VVID<2>
  - MCP_VVID<1>
  - XW7562 XW7563
  - OMIT SM

- MCPCORES0_VDIFF
  - MCPCORES0_VW
  - MCPCORES0_COMP
  - MCPCORES0_VSEN

- MCPCORES0_PGOOD
  - MCPCORES0_FB
  - MCPCORES0_RTN

- MCPCORES0_RSEN_N
  - MCPCORES0_ICOMP
  - MCPCORES0_ISP
  - MCPCORES0_ISN
  - MCPCORES0_OSET

- MCPCORES0_VO
  - MCPCORES0_BOOT
  - MCPCORES0_UGATE
  - MCPCORES0_UFET
  - MCPCORES0_PGND

- MCPCORES0_EN
  - MCPCORES0_FDE
  - MCPCORES0_SOFT
  - MCPCORES0_RBIAS

- MCPCORES0_VDIFF
  - MCPCORES0_VW
  - MCPCORES0_COMP
  - MCPCORES0_VSEN

- MCPCORES0_PGOOD
  - MCPCORES0_FB
  - MCPCORES0_RTN

- MCPCORES0_RSEN_N
  - MCPCORES0_ICOMP
  - MCPCORES0_ISP
  - MCPCORES0_ISN
  - MCPCORES0_OSET

- MCPCORES0_VO
  - MCPCORES0_BOOT
  - MCPCORES0_UGATE
  - MCPCORES0_UFET
  - MCPCORES0_PGND

- MCPCORES0_EN
  - MCPCORES0_FDE
  - MCPCORES0_SOFT
  - MCPCORES0_RBIAS

- MIN_NECK_WIDTH=0.2 MM
- MIN_LINE_WIDTH=0.5 MM
- DIDT=TRUE

- SWITCH_NODE=TRUE
- CRITICAL
- SWITCHNODE CRITICAL

- f = 300 kHz

- APPLE INC.
- REV. III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART I TO MAINTAIN THE DOCUMENT IN CONFIDENCE AGREES TO THE FOLLOWING

- THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

- 051-7898

- X7R-CERM
- 1UF
- 16V
- 10%

- X7R
- 0.001UF
- X5R
- 10UF
- 2V

- X7R
- 0.001UF
- X5R
- 10UF
- 2V

- 270UF
- 2V

- 0.82UH-16A
- MF-LF
- 1/16W

- 603
- 5%

- 0.2 MM
- 0.25 MM

- POWER33-SM
- CRITICAL

- APPLE INC.

- www.vinafix.vn
CPUVTT POWER SUPPLY

VOUT = 1.062V
F = 320 KHZ
8A max output

Vout = 0.75V * (1 + Ra / Rb)

Place XW7601 by C7660.
Place XW7600 between Pin 7 and Pin 15 of U7600.

C7665
1
2
603
6.3V
2
10UF
X5R

C7660
1
2
330UF
20%
2.5V
TANT
CASE-B2-SM

R7670
MF-LF
1%
1/16W
20.0K
2
1
402
1%
402
1/16W

R7603
MF-LF
1%
200K
2
1
66C1
66A5
2
1/16W
1%

C7630
CRITICAL
20%
16V
33UF

C7695
1UF
1
2
CASED2E-SM
POLY-TANT

C7601
10%
603-1
25V
2
1

C7604
603
X5R-CERM
6.3V

C7603
2
4.7UF
10%
2
1

C7600
1UF
X5R
10V

C7661
CRITICAL
CERM
0.001UF
50V
20%
2
1

C7696
402
1
2

C7630
CRITICAL
20%
16V
33UF

C7691
X7R
0.1UF
10%
50V
603-1
2
1

C7603
2
4.7UF
10%
2
1

C7600
1UF
X5R
10V

C7661
CRITICAL
CERM
0.001UF
50V
20%
2
1

L7620
2.2A-8.0A

Q1
Q2
SW

DIDT=TRUE
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
GND_CPUVTTS0_SGND

DIDT=TRUE
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
PP5V_S0_CPUVTTS0_V5FILT

DIDT=TRUE
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CPUVTTS0_VOUT

DIDT=TRUE
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CPUVTTS0_DRVH

DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CPUVTTS0_LL

DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CPUVTTS0_TRIP

DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CPUVTTS0_VFB

DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
CPUVTTS0_PGOOD

=PPCPUVTT_S0_REG

=PP5V_S0_CPUVTTS0

=CPUVTTS0_EN

=PPVIN_S0_CPUVTTS0

SYNC_DATE=02/08/2008
SYNC_MASTER=RAYMOND
1.8V S0 SWITCHER

VOUT = 0.8V * (1 + RA / RB)

1.05V S0 PLL LDO

VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY

VOUT = 0.8V * (1 + RA / RB)
Display Port Interoperability spec says that sources AUX CH has 100K pull up/down on the MLB (which DVI and DP has 10K pull up/down on the MLB).

DP_AUX_CH_C_N

DP_AUX_CH_C_P

DP_AUX_CH_SW_P

DP_CA_DET

DP_DDC_CLK

DDC_CA_DET_LS5V_L

DP_IG_AUX_CH_P

DP_IG_AUX_CH_N

DP_IG_AUX_MUX

DP_IG_CA_DET

SYNC_DATE=04/18/2008

SYNC_MASTER=AMASON

www.vinafix.vn
B A D Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MΩ.

75C3 69D1 75B3 69D4 69C4 70C8 70B8 69B7 BI BI IN =PP3V3_S0_DPCONN DP_AUX_CH_C_N DP_ML_P<3> DP_ML_N<3> BI BI IN =PP3V3_S5_DP_PORT_PWR PM_SLP_S3_L 12 10% X5R 2N7002DW-X-G DP_ML_C_N<3> DP_ML_C_P<3> 16V 16V 6.3V 20% 2 100K MF-LF 1/16W 402 1 100K if DP_HPD is used.

down HPD input with C9415 C9414 C9413 C9412 0.1uF 0.1uF 0.1uF 0.1uF =PP3V3_S5_DP_PORT_PWR PM_SLP_S3_L 12 10% X5R 2N7002DW-X-G DP_ML_C_N<3> DP_ML_C_P<3> 16V 16V 6.3V 20% 2 100K MF-LF 1/16W 402 1 100K if DP_HPD is used.

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**MCP FSB COMP Signal Constraints**

Some signals require 27.4-ohm single-ended impedance.

**NOTE:** 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

**CPU Signal Constraints**

**NOTE:** Intel Design Guide allows closer spacing if signal lengths can be shortened.

Intel Design Guide recommends FSB signals be routed only on internal layers.

Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

FSB 2X signals / groups shown in signal table on right.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 4X signals / groups shown in signal table on right.

### Table: Signal Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Layer</th>
<th>Max. Neck Length</th>
<th>Min. Neck Width</th>
<th>Line-To-Line Spacing</th>
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<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_COMP</td>
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<td>CPU_IERR_L</td>
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</tr>
<tr>
<td>FSB_CLK_CPU</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_ITP</td>
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</tr>
<tr>
<td>FSB_DSTB</td>
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<td></td>
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</tr>
<tr>
<td>FSB_DSTB_L_P</td>
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<tr>
<td>FSB_DSTB_L_N</td>
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</tr>
<tr>
<td>FSB_DSTB0</td>
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<tr>
<td>FSB_DSTB2</td>
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<tr>
<td>FSB_DSTB3</td>
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<tr>
<td>FSB_ADDR</td>
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<tr>
<td>FSB_ADDR_GROUP1</td>
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<td>FSB_ADDR_GROUP2</td>
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<tr>
<td>FSB_DATA</td>
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<td>FSB_BREQ0_L</td>
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<td>FSB_DSTB_L_P</td>
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<tr>
<td>FSB_DSTB3</td>
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</table>

**CPU FSB Net Properties**

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min. Separation</th>
<th>Max. Separation</th>
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</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
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<td>FSB_CLK_ITP</td>
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<td>FSB_DSTB_L_N</td>
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<td>FSB_ADDR</td>
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<tr>
<td>FSB_DSTB3</td>
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</tbody>
</table>
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
### PCI Bus Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>PCI BUS</th>
<th>LANE</th>
<th>DIRECTION</th>
<th>NET</th>
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<tbody>
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### LPC Bus Constraints

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<tbody>
<tr>
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<td>IN</td>
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### SMBus Interface Constraints

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<th>VALUE</th>
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</thead>
<tbody>
<tr>
<td>MCP</td>
<td>SMB D C</td>
<td>IN</td>
<td>PIPE</td>
<td>SMB D C PIPE</td>
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### USB 2.0 Interface Constraints

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<th>LANE</th>
<th>DIRECTION</th>
<th>NET</th>
<th>VALUE</th>
<th>VALUE</th>
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<tbody>
<tr>
<td>MCP</td>
<td>USB D C</td>
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<td>PIPE</td>
<td>USB D C PIPE</td>
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### SPI Interface Constraints

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<tbody>
<tr>
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<td>PIPE</td>
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</tr>
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</table>

### SPI Interface Table

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>SPI_CS0</th>
<th>SPI_MISO</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
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</thead>
<tbody>
<tr>
<td>SPI_55S</td>
<td>SPI_55S</td>
<td>SPI_55S</td>
<td>SPI_55S</td>
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### SMBus Interface Table

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<tr>
<th>NET_TYPE</th>
<th>SMBUS_MCP_0_DATA</th>
<th>SMBUS_MCP_1_DATA</th>
<th>SMBUS_MCP_1_CLK</th>
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<tbody>
<tr>
<td>SMB_55S</td>
<td>SMB_55S</td>
<td>SMB_55S</td>
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### HD Audio Interface Table

<table>
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<tr>
<th>NET_TYPE</th>
<th>HDA_SDOUT_R</th>
<th>HDA_SDOUT</th>
<th>HDA_SDIN_CODEC</th>
<th>HDA_RST_L</th>
<th>HDA_SYNC_R</th>
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</thead>
<tbody>
<tr>
<td>HDA_55S</td>
<td>HDA_55S</td>
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### PCI Bus Table

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<tr>
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<th>PCI_CNTL</th>
<th>PCI_CNTL</th>
<th>PCI_CNTL</th>
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<tbody>
<tr>
<td>PCI_55S</td>
<td>PCI_CNTL</td>
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### SIO Signal Constraints

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<tr>
<th>Source</th>
<th>SIO BUS</th>
<th>LANE</th>
<th>DIRECTION</th>
<th>NET</th>
<th>VALUE</th>
<th>VALUE</th>
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<tbody>
<tr>
<td>MCP</td>
<td>SIO D C</td>
<td>IN</td>
<td>PIPE</td>
<td>SIO D C PIPE</td>
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<td>0</td>
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</table>

### MCP Constraints 2

<table>
<thead>
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<th>MCP BUS</th>
<th>LANE</th>
<th>DIRECTION</th>
<th>NET</th>
<th>VALUE</th>
<th>VALUE</th>
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<tbody>
<tr>
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</tr>
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### MCP RGMII (Ethernet) Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
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<tbody>
<tr>
<td>MINIMUM LINE WIDTH</td>
<td>Allow route on layer?</td>
</tr>
<tr>
<td>MINIMUM NECK WIDTH</td>
<td>MAXIMUM NECK LENGTH</td>
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### PHYSICAL_RULE_SET

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<tr>
<td>MCP RGMII (Ethernet) Constraints</td>
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<tr>
<td>88E1116R (Ethernet PHY) Constraints</td>
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### MCP MII_COMP

- **MCP_MII_COMP**
  - **MCP_MII_COMP**
  - **MCP_MII_COMP**
  - **MCP_MII_COMP**

### MCP_BUF0_CLK

- **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**

### ENET_MII_55S

- **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**

### ENET_MII_55S

- **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**

### Ethernet Constraints

- **SYNC_MASTER**
  - **SYNC_DATE**
  - **SYNC_DATE**
  - **SYNC_DATE**

- **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**
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- **ENET_MII_55S**
  - **ENET_MII_55S**
  - **ENET_MII_55S**
  - **ENET_MII_55S**

- **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**
  - **ENET_MII**

- **ENET_MII_P<3..0>**
  - **ENET_MII_P<3..0>**
  - **ENET_MII_P<3..0>**
  - **ENET_MII_P<3..0>**

- **ENET_MII_N<3..0>**
  - **ENET_MII_N<3..0>**
  - **ENET_MII_N<3..0>**
  - **ENET_MII_N<3..0>**

- **ENET_RESET_L**
  - **ENET_RESET_L**
  - **ENET_RESET_L**
  - **ENET_RESET_L**

- **ENET_CLK125M_RXCLK_R**
  - **ENET_CLK125M_RXCLK_R**
  - **ENET_CLK125M_RXCLK_R**
  - **ENET_CLK125M_RXCLK_R**

- **ENET_RESET_L**
  - **ENET_RESET_L**
  - **ENET_RESET_L**
  - **ENET_RESET_L**

- **ENET_CLK125M_TXCLK**
  - **ENET_CLK125M_TXCLK**
  - **ENET_CLK125M_TXCLK**
  - **ENET_CLK125M_TXCLK**

- **ENET_CLK125M_TXCLK_R**
  - **ENET_CLK125M_TXCLK_R**
  - **ENET_CLK125M_TXCLK_R**
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  - **ENET_INTR_L**

- **ENET_CLK125M_RXCLK**
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- **ENET_CLK125M_TXCLK**
  - **ENET_CLK125M_TXCLK**
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  - **ENET_CLK125M_TXCLK**

- **ENET_CLK125M_TXCLK_R**
  - **ENET_CLK125M_TXCLK_R**
  - **ENET_CLK125M_TXCLK_R**
  - **ENET_CLK125M_TXCLK_R**

- **ENET_MDC**
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  - **ENET_MDC**
  - **ENET_MDC**

- **ENET_MDIO**
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  - **ENET_MDIO**

- **RTL8211_CLK25M_CKXTAL1**
  - **RTL8211_CLK25M_CKXTAL1**
  - **RTL8211_CLK25M_CKXTAL1**
  - **RTL8211_CLK25M_CKXTAL1**

- **ENET_MII**
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- **ENET_RXD<0>**
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  - **ENET_RXD<0>**
  - **ENET_RXD<0>**

- **ENET_PWRDWN_L**
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  - **ENET_PWRDWN_L**
  - **ENET_PWRDWN_L**

- **ENET_RXD<3..1>**
  - **ENET_RXD<3..1>**
  - **ENET_RXD<3..1>**
  - **ENET_RXD<3..1>**

- **ENET_RXD<3..1>**
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- **ENET_RXD<3..1>**
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  - **ENET_PWRDWN_L**

- **ENET_POWERDWN_L**
  - **ENET_POWERDWN_L**
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  - **ENET_POWERDWN_L**

- **ENET_PWRDWN_L**
  - **ENET_PWRDWN_L**
  - **ENET_PWRDWN_L**
  - **ENET_PW...
SD CARD INTERFACE CONSTRAINTS

SD CARD NET PROPERTIES

FireWire Interface Constraints

FireWire Net Properties

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SD CARD NET PROPERTIES

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|-------------------------|------------|-----------------|------------------|-----------------------|-------------------|

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PHYSICAL_RULE_SET

TABLE_PHYSICAL_RULE_HEAD

K24 SENSOR NET PROPERTIES

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<th>Designation</th>
<th>Description</th>
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<tr>
<td>40100</td>
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K24 SPECIAL CONSTRAINTS

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<td>40100</td>
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www.vinafix.vn
### Table: Physical Rule Set

<table>
<thead>
<tr>
<th>Layer</th>
<th>MINIMUM LINE WIDTH</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>Net Spacing Type 1</th>
<th>Net Spacing Type 2</th>
<th>Net Spacing Type 3</th>
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</thead>
<tbody>
<tr>
<td>TOP, BOTTOM</td>
<td>0.075 mm</td>
<td>0.095 mm</td>
<td>0.112 mm</td>
<td>0.230 mm</td>
<td>0.230 mm</td>
<td>MEM_40S</td>
<td>BGA_P1MM</td>
<td>5X_DIELECTRIC</td>
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<td>LAYER</td>
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<td>12.7 mm</td>
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<td>2:1_SPACING</td>
<td>0.200 mm</td>
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<tr>
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</tr>
<tr>
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<td>BGA_P2MM</td>
<td>3:1_SPACING</td>
<td>0.224 mm</td>
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<td>0.220 mm</td>
<td>0.220 mm</td>
<td>MEM_40S</td>
<td>BGA_P2MM</td>
<td>2.5:1_SPACING</td>
<td>0.190 mm</td>
<td>0.190 mm</td>
<td>0.190 mm</td>
</tr>
</tbody>
</table>

**Legend:**
- **MINIMUM LINE WIDTH:** The minimum line width for each layer.
- **MINIMUM NECK WIDTH:** The minimum neck width for each layer.
- **MAXIMUM NECK LENGTH:** The maximum neck length for each layer.
- **DIFFPAIR PRIMARY GAP:** The primary gap for each layer.
- **DIFFPAIR NECK GAP:** The neck gap for each layer.
- **NET_PHYSICAL_TYPE:** The physical type for each net.
- **AREA_TYPE:** The area type for each net.
- **SPACING_RULE_SET:** The spacing rule set for each net.