**K36 MLB SCHEMATIC**

**REFERRED FROM M70**

**7/13/2007**

---

**DVT-LEVEL BUILD**

---

### Table of Contents

<table>
<thead>
<tr>
<th>Page (of)</th>
<th>Contents</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Table of Contents</td>
<td>RX</td>
</tr>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td>RX</td>
</tr>
<tr>
<td>3</td>
<td>Power Block Diagram</td>
<td>RX</td>
</tr>
<tr>
<td>4</td>
<td>CONFIGURATION OPTIONS</td>
<td>RX</td>
</tr>
<tr>
<td>5</td>
<td>Revision History</td>
<td>RX</td>
</tr>
<tr>
<td>6</td>
<td>FUNC 1 OF 2</td>
<td>RX</td>
</tr>
<tr>
<td>7</td>
<td>Power Aliases</td>
<td>RX</td>
</tr>
<tr>
<td>8</td>
<td>SIGNAL Alias / RESET</td>
<td>RX</td>
</tr>
<tr>
<td>9</td>
<td>CPU FSB</td>
<td>RX</td>
</tr>
<tr>
<td>10</td>
<td>CPU Power &amp; Ground</td>
<td>RX</td>
</tr>
<tr>
<td>11</td>
<td>CPU Decoupling &amp; VID</td>
<td>RX</td>
</tr>
<tr>
<td>12</td>
<td>NB CPU Interface</td>
<td>RX</td>
</tr>
<tr>
<td>13</td>
<td>NB FSB / Video Interfaces</td>
<td>RX</td>
</tr>
<tr>
<td>14</td>
<td>NB Misc Interfaces</td>
<td>RX</td>
</tr>
<tr>
<td>15</td>
<td>NB DDR Interfaces</td>
<td>RX</td>
</tr>
<tr>
<td>16</td>
<td>NB Power 1</td>
<td>RX</td>
</tr>
<tr>
<td>17</td>
<td>NB Power 2</td>
<td>RX</td>
</tr>
<tr>
<td>18</td>
<td>NB Grounds</td>
<td>RX</td>
</tr>
<tr>
<td>19</td>
<td>NB Standard Decoupling</td>
<td>RX</td>
</tr>
<tr>
<td>20</td>
<td>NB Graphics Decoupling</td>
<td>RX</td>
</tr>
<tr>
<td>21</td>
<td>NB Elct, Dqhs, FSB, LPC</td>
<td>RX</td>
</tr>
<tr>
<td>22</td>
<td>SB FSB, DIOSM, SMI, USB</td>
<td>RX</td>
</tr>
<tr>
<td>23</td>
<td>SB FSB, Gpio, Clock, SDC</td>
<td>RX</td>
</tr>
<tr>
<td>24</td>
<td>SB Power &amp; Ground</td>
<td>RX</td>
</tr>
<tr>
<td>25</td>
<td>SB Decoupling</td>
<td>RX</td>
</tr>
<tr>
<td>26</td>
<td>SB Misc</td>
<td>RX</td>
</tr>
<tr>
<td>27</td>
<td>Clock (270Y)</td>
<td>DR</td>
</tr>
<tr>
<td>28</td>
<td>Clock Termination</td>
<td>DP</td>
</tr>
<tr>
<td>29</td>
<td>DDR2 SO-DIMM Connector A</td>
<td>LD</td>
</tr>
<tr>
<td>30</td>
<td>DDR2 SO-DIMM Connector S</td>
<td>LD</td>
</tr>
<tr>
<td>31</td>
<td>Memory Active Termination</td>
<td>LD</td>
</tr>
<tr>
<td>32</td>
<td>Ethernet (Yukos)</td>
<td>LT</td>
</tr>
<tr>
<td>33</td>
<td>Yukos Power Control</td>
<td>LT</td>
</tr>
<tr>
<td>34</td>
<td>Ethernet Connector</td>
<td>LT</td>
</tr>
<tr>
<td>35</td>
<td>FIREWIRE CONTROLLER</td>
<td>LT</td>
</tr>
<tr>
<td>36</td>
<td>FIREWIRE PORT</td>
<td>LT</td>
</tr>
<tr>
<td>37</td>
<td>SATA Connector</td>
<td>DA</td>
</tr>
<tr>
<td>38</td>
<td>USB External Connectors</td>
<td>LT</td>
</tr>
<tr>
<td>39</td>
<td>CONNECTOR MISC</td>
<td>LA</td>
</tr>
<tr>
<td>40</td>
<td>IS CONTROLLER &amp; BT INTERFACE</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>SMC</td>
<td>DA</td>
</tr>
<tr>
<td>42</td>
<td>SMC SUPPORT</td>
<td>LD</td>
</tr>
</tbody>
</table>

---

**K36 EE DRIS:**

RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFFER
LT-LAWRENCE TAN
LD-LINDA DUNN
MM-MARY(YUAN) MA

---

**DVT-LEVEL BUILD**

---

**Schematic / PCB #’s**

<table>
<thead>
<tr>
<th>PCB #’s</th>
<th>Description</th>
<th>Reference No.</th>
<th>Critical</th>
<th>NW Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>97-7455</td>
<td></td>
<td>DVT-LEVEL BUILD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**COPYRIGHT NOT TO BE REVEALED OR PUBLISHED IN WHOLE OR PART**

---

**APPLE COMPUTER INC.**

---

**Schematic, MLB, K36**

---

**www.vinafix.vn**
NOTICE OF PROPRIETARY PROPERTY

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

III NOT TO REPRODUCE OR COPY IT

AGREES TO THE FOLLOWING

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

SCALE

NONE

CONN 051-7455 01

www.vinafix.vn
### Functional Test Points

#### Fan Connectors

<table>
<thead>
<tr>
<th>No.</th>
<th>Function</th>
<th>Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CPU FAN 1</td>
<td>P7_1812</td>
</tr>
<tr>
<td>2</td>
<td>CPU FAN 2</td>
<td>P7_1813</td>
</tr>
<tr>
<td>3</td>
<td>CPU FAN 3</td>
<td>P7_1814</td>
</tr>
</tbody>
</table>

#### Battery Digital Connector

<table>
<thead>
<tr>
<th>No.</th>
<th>Function</th>
<th>Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>SMPS 5V</td>
<td>P7_1815</td>
</tr>
<tr>
<td>5</td>
<td>SMPS 12V</td>
<td>P7_1816</td>
</tr>
</tbody>
</table>

#### LPC+ Debug Connector

<table>
<thead>
<tr>
<th>No.</th>
<th>Function</th>
<th>Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>LPC AD0</td>
<td>P7_1817</td>
</tr>
<tr>
<td>7</td>
<td>LPC AD1</td>
<td>P7_1818</td>
</tr>
<tr>
<td>8</td>
<td>LPC AD2</td>
<td>P7_1819</td>
</tr>
</tbody>
</table>

#### Other Func Test Points

<table>
<thead>
<tr>
<th>No.</th>
<th>Function</th>
<th>Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>CPU FAN 1</td>
<td>P7_1820</td>
</tr>
<tr>
<td>10</td>
<td>CPU FAN 2</td>
<td>P7_1821</td>
</tr>
</tbody>
</table>

### Other Functional Test Points

- **Audio Func Test**
  - TP_USB_EXTC_P
  - TP_USB_EXTC_N
- **SMP4**
  - SMC_BATT_TRICKLE_EN_L
- **USB Func Test**
  - USB2_3G_F_P
  - USB2_3G_F_N
- **MIC Func Test**
  - MIC_SHLD_CONN
  - MIC_HI_CONN
- **SPEAKER Func Test**
  - SPKRCONN_SUB_P_OUT
  - SPKRCONN_L_P_OUT
- **THERMAL Func Test**
  - THERM_FAN1
  - THERM_FAN2
  - THERM_FAN3

---

www.vinafix.vn
"S0, S0M" RAILS
- REGULATOR OUTPUT CPU VCORE PWR
- REGULATOR OUTPUT CPU 0.90V PWR
- REGULATOR OUTPUT CPU 0.90V PWR
- REGULATOR OUTPUT CPU 0.90V PWR
- REGULATOR OUTPUT CPU 0.90V PWR
- DDR2 TERMINATION 0.9V PWR
- DDR2 TERMINATION 0.9V PWR
- CPU VCORE PWRE
- CPU VCORE PWRE
- MAKE_BASE=TRUE
- VOLTAGE=1.05V
- VOLTAGE=5V
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.6 mm
- MAKE_BASE=TRUE
- VOLTAGE=1.8V
- MIN_NECK_WIDTH=0.2 mm
- MAKE_BASE=TRUE
- VOLTAGE=1.25V
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.6 mm
- MAKE_BASE=TRUE
- VOLTAGE=1.5V
- MIN_LINE_WIDTH=0.5 mm
- MAKE_BASE=TRUE
- VOLTAGE=1.2V
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.3 mm
- MAKE_BASE=TRUE
- VOLTAGE=1.5V
- MIN_LINE_WIDTH=0.5 mm
- www.vinafix.vn

"S" RAILS
- "S" RAILS
- "S" RAILS
- "S" RAILS
- "S" RAILS
- "S" RAILS
- "S" RAILS
- "S" RAILS
- "S" RAILS

"S5" RAILS
- "S5" RAILS
- "S5" RAILS
- "S5" RAILS
- "S5" RAILS
- "S5" RAILS
- "S5" RAILS
- "S5" RAILS
- "S5" RAILS

"G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS
- "G3H" RAILS

Power Aliases
www.vinafix.vn
Current numbers from Merom for Santa Rosa EMTS, doc #22221.
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR’S TCK PIN TO CPU'S TCK PIN AND THEN FLEX BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S TCK PIN.
Current numbers from Crestline EDS, doc #21749.

- **831D2**: 7700 mA (Int Graphics)
- **1395 mA (1 ch, 533MHz)**
- **1700 mA (1 ch, 667MHz)**
- **2700 mA (2 ch, 533MHz)**

- **1310 mA (Ext Graphics)**

These connections can break without impacting part performance.

**HINT**

*Not to reveal or publish in whole or part to maintain the document in confidence.*

**NOTICE OF PROPRIETARY PROPERTY**
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDB = _NB_TDE_FORCE

=NB_GROUND

NB Grounds

NONE

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING NOTICE OF PROPRIETARY PROPERTY

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

www.vinafix.vn
L2702 MAY HAVE CHANGE TO 0.5UH PART OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE CAPS < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE CAPS AT EDGE OF SB

PLACE CAPS < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS AA3...Y7
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AA11
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AC12
PLACE < 2.54MM OF SB ON SECONDARY PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:

PLACEMENT NOTE:
This part is never stuffed, it provides a set of pads on the board to short up to solder a reset button.

Initial resistor values are based on CRB, but may change after characterization.
One cap for each side of every RPAK, one cap for every two discrete resistors.

- **NOTICE OF PROPRIETARY PROPERTY:**
  - The information contained herein is proprietary to the manufacturer and is the property of the manufacturer.
  - I, the recipient of this document, agree to the following:
  - **NOT TO REPRODUCE OR COPY IT**
  - **NOT TO MAINTAIN THE DOCUMENT IN CONFIDENCE**
  - **AGREES TO THE FOLLOWING**

**Memory Active Termination**

- **LAYOUT NOTE:** PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM.
Yukon Ultra schematic support.

Instructions for dual Yukon EC / Yukon Ultra.

**NOTE:** See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

- **YUKON_ULTRA** - Selects Yukon Ultra RSET.
- BOM options provided by this page:
  - =ENET_VMAIN_AVLBL
  - =PP1V2_ENET_PHY
  - =YUKON_EC_PP2V5_ENET

---

**PART NUMBER**

<table>
<thead>
<tr>
<th>Description</th>
<th>REFERENCE</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIGNAL_MODEL=EMPTY</td>
<td>U3700</td>
<td>4</td>
</tr>
<tr>
<td>ENET_MDI0, ENET_MDI1, ENET_MDI2</td>
<td>C3740, C3739, C3741</td>
<td>1</td>
</tr>
<tr>
<td>ENET_RESET_L</td>
<td>C3710</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_WAKE_L</td>
<td>C3711</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_ENET_R2D_P</td>
<td>C3712</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_ENET_R2D_N</td>
<td>C3713</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_ENET_D2R_C_P</td>
<td>C3714</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_ENET_D2R_C_N</td>
<td>C3715</td>
<td>1</td>
</tr>
<tr>
<td>ENET_CLK25M_XTALI</td>
<td>R3746</td>
<td>1</td>
</tr>
<tr>
<td>ENET_MDI3</td>
<td>C3742</td>
<td>1</td>
</tr>
<tr>
<td>ENET_MDI4</td>
<td>C3743</td>
<td>1</td>
</tr>
<tr>
<td>ENET_MDI5</td>
<td>C3744</td>
<td>1</td>
</tr>
<tr>
<td>ENET_MDI6</td>
<td>C3745</td>
<td>1</td>
</tr>
<tr>
<td>ENET_MDI7</td>
<td>C3746</td>
<td>1</td>
</tr>
<tr>
<td>XPD_BOOST</td>
<td>C3747</td>
<td>1</td>
</tr>
</tbody>
</table>

---

**DESCRIPTION**

- **SIGNAL_MODEL=EMPTY**
- **ENET_MDI0, ENET_MDI1, ENET_MDI2**
- **ENET_RESET_L**
- **PCIE_WAKE_L**
- **PCIE_ENET_R2D_P**
- **PCIE_ENET_R2D_N**
- **PCIE_ENET_D2R_C_P**
- **PCIE_ENET_D2R_C_N**
- **ENET_CLK25M_XTALI**
- **ENET_MDI3**
- **ENET_MDI4**
- **ENET_MDI5**
- **ENET_MDI6**
- **ENET_MDI7**
- **XPD_BOOST**

---

**REFERENCE**

- **U3700**
- **C3740, C3739, C3741**
- **C3710**
- **C3711**
- **C3712**
- **C3713**
- **C3714**
- **C3715**
- **R3746**
- **C3742**
- **C3743**
- **C3744**
- **C3745**
- **C3746**
- **C3747**

---

**QUANTITY**

- **4**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**

---

**To support Yukon EC and Ultra on the same board:**

- **YUKON_RSET**
- **TP_YUKON_CTRL18**
- **YUKON_VPD_DATA**
- **YUKON_VPD_CLK**

---

**APPENDIX**

- **SYNC_MASTER=USB**
- **THRML_PAD**
- **SWITCH_VCC**
- **VAUX_AVLBL**
- **VDDO_TTL0**
- **VDDO_TTL1**
- **VDD1**
- **VDD2**
- **VDD3**
- **VDD4**
- **VDD5**
- **VDD6**
- **VDD7**
- **VCC**
- **VSS**
- **AVDD1**
- **AVDD3**
- **AVDDH**
- **AVDD1**
- **TEST/RSVD**
- **TESTMODE**
- **VPD ROM**
- **YUKON_VPD_DATA**
- **YUKON_VPD_CLK**
- **YUKON_RSET**

---

**FILE NAME:**

- **Yukon EC**
- **Yukon Ultra**

---

**DESCRIPTION**

- **ENET_MDI0, ENET_MDI1, ENET_MDI2**
- **ENET_RESET_L**
- **PCIE_WAKE_L**
- **PCIE_ENET_R2D_P**
- **PCIE_ENET_R2D_N**
- **PCIE_ENET_D2R_C_P**
- **PCIE_ENET_D2R_C_N**
- **ENET_CLK25M_XTALI**
- **ENET_MDI3**
- **ENET_MDI4**
- **ENET_MDI5**
- **ENET_MDI6**
- **ENET_MDI7**
- **XPD_BOOST**

---

**REFERENCE**

- **U3700**
- **C3740, C3739, C3741**
- **C3710**
- **C3711**
- **C3712**
- **C3713**
- **C3714**
- **C3715**
- **R3746**
- **C3742**
- **C3743**
- **C3744**
- **C3745**
- **C3746**
- **C3747**

---

**QUANTITY**

- **4**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**
- **1**

---

**SDT:/vue/49/57/300**

**Reference:**

- **www.vinafix.vn**
PLACE ONE PAIR OF CAPS AT EACH PIN 3 AND 6 OF TRANSFORMERS

PLACE C3911 AND C3912 ON EACH SIDE OF J3900
Enables port power whenever machine AC Adapter is plugged or system at run time with battery only.
If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating.
IN
V-
V+
SD
GD
SIZE
OF
SHT
DRAWING NUMBER
NOTICE OF PROPRIETARY PROPERTY
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
III AGREES TO THE FOLLOWING

Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits

CPU CURRENT SENSE

CPU VOLTAGE SENSE

GPU VOLTAGE SENSE

CPU Current & Voltage Sense

www.vinafix.vn
HEAT-PIPE/FIN-STACK TEMPERATURE ZONE

CPU TEMPERATURE ZONE

WRITE: 0x98 READ: 0x99

TEMPERATURE SENSE

CHECK sums: 0x98-0x99

SYNC_DATE=06/21/2006
SYNC_MASTER=GPU
1.8V/0.9V POWER SUPPLY

\[ V_{out} = 0.75V \times (1 + \frac{R_a}{R_b}) \]

Routing Note:
- Place C7504 near U7501 pin 7

Placement Note:
- Connect CS_GND to VTTSNS

Connect VTTSNS to C7507 pin 1

Connect VDDQSNS to C7542 pin 1

MIN_LINE_WIDTH = 1 mm
MIN_NECK_WIDTH = 0.25 mm

Notice of Proprietary Property
II NOT TO REPRODUCE OR COPY IT
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

LATEST ISSUE: 2006/12/22

www.vinafix.vn
3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

1.25V S0 REGULATOR

Vout = 0.8V * (1 + Ra / (Rb + Rc))

LATEST ISSUE: 2007/3/8
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL

1.8V S3 RUN/SS CONTROL

S3 FET & S3/S5 Control

LATEST ISSUE: 2006/12/22

www.vinafix.vn
Some signals require 27.4-ohm single-ended impedance.

CPU Signal Constraints

- NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
- All FSB signals with impedance requirements are 55-ohm single-ended.
- Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
- FSB complementary pairs are spaced 1:1 and routed as differential pairs.
- Design Guide recommends each stretch/bus group be routed on the same layer.
- Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to VCCSense pair, assumed 3:1.

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

- DG recommends at least 25 mils, >50 mils preferred

CPU / FSB Net Properties

- NOTE: 7 mil gap is for VCCSense pair, which allows a minimum of 7 mil spacing without specifying a target differential impedance.

Many CPU signals with impedance requirements are 27-ohm single-ended.

- Some signals require 27.4-ohm single-ended impedance.

NOTE: This page contains confidential information and is the property of Apple Computer, Inc. The possessor is to maintain the document in confidence. The possession of this document constitutes notice of proprietary property.
Video Signal Constraints

<table>
<thead>
<tr>
<th>Source (Source)</th>
<th>Nominal</th>
<th>Min</th>
<th>Max</th>
<th>Min (Nominal)</th>
<th>Max (Nominal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRT_SYNC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT_50S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT_55S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT_2CRT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT_SYNC2SYNC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT Blue</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT Green</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT RED</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRT_TVO_IREF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS_IBG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS_100D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMI_100D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCIE_100D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LVDS signals are 100-ohm +/- 20% differential impedances. CRT & TVDAC signals are 55-ohm +/- 15% single-ended impedances.
- 55-ohm +/- 15% from second termination resistor to connector.
- 50-ohm +/- 15% from first to second termination resistor.
- 37.5-ohm +/- 15% from GMCH to first termination resistor.

CRT & TVDAC signals single-ended impedances vary by location:

- CRT_SYNC: 55-ohm +/- 15% from GMCH to first termination resistor.
- CRT_50S: 50-ohm +/- 15% from first to second termination resistor.
- CRT_55S: 55-ohm +/- 15% from second termination resistor to connector.

PCI-Express / DMI Bus Constraints
### Controller Link (AMT) Constraints

**Table**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>5 mils</td>
<td>55 Ohm SE</td>
<td>30 mils</td>
<td>50 mils</td>
<td>50 mils</td>
</tr>
<tr>
<td>6</td>
<td>5 mils</td>
<td>55 Ohm SE</td>
<td>30 mils</td>
<td>50 mils</td>
<td>50 mils</td>
</tr>
<tr>
<td>5</td>
<td>5 mils</td>
<td>55 Ohm SE</td>
<td>30 mils</td>
<td>50 mils</td>
<td>50 mils</td>
</tr>
<tr>
<td>4</td>
<td>5 mils</td>
<td>55 Ohm SE</td>
<td>30 mils</td>
<td>50 mils</td>
<td>50 mils</td>
</tr>
</tbody>
</table>

**Notes:**
- DG says 30 mils min separation.
- SB says 30 mils min separation.
- See SB Constraints (2 of 2).
Clock Signal Constraints

Clock Net Properties

Clock Constraints