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**K36A EE DRIS:**

DK-DINESH KUMAR

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**Schematic / PCB #s**

<table>
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<th>Schematic / PCB #s</th>
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**Date**

- 06/12/2006
- 07/17/2006
- 10/30/2006

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**Dimensions**

X.XXXX

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**Release**

- 04/26/2006
- 06/15/2006
- 07/13/2005
- 05/23/05
- 08/19/2005
- 06/23/2006
- 07/26/2005
- 10/30/2006
- 10/07/2006
- 06/20/2005
- 12/06/2005
- 09/05/2006

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**ECN**

N/A

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**Dimensions are in millimeters**

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- CONNECTED MIC_SHLD_CONN TO GND CHASSIS AUDIO_MIC THROUGH R6854.
- ADDED SMALL 15PF COMPENSATION CAP. TO U6201 FEEDBACK NETWORK (C6224).
- ADDED A NO STUFF PULL-UP TO CODEC_DVDD AT GPIO1.

CSA PAGE 62:
- CHANGE L2902 AND L2903 FROM 155S0302 TO 0OHM R2906 AND R2907.
- CHANGE R2514 TO 100K.
- RENAME LVDS_VREFH/L TO TP_LVDS_VREFH/L.

CSA PAGE 15:
- REMOVE R1290 TO R1296 ON CPU_VID<0:6>.

CSA PAGE 12:
- ADD SPN ALIASES FOR CK505_PCI2/4_CLK.
- ADD SPN ALIASES FOR TP_CK505_SRC7_N/P.

CSA PAGE 44:
- CHANGE J9000 FROM 518S0369 TO 518S0521.
- CHANGE J6703 FROM 518S0369 TO 518S0521.

CSA PAGE 67:
- CHANGE J5601 FROM 518S0369 TO 518S0521.
- CHANGE J4810 FROM 518S0369 TO 518S0521.
- REMOVE R4660 AND R4601 (U4675 BYPASS RESISTORS).
- REPLACE ALL M70 WITH K36 (TEXT, BOM OPTIONS, 630 NUMBERS).

7/5/2006
CSA PAGE 94:
- REPLACE BATTERY INTERFACE CIRCUIT WITH THE ONE ON M42B ESTAR.
- CHANGE J6900 FROM 518S0287 TO 518S0526.
- ADD NOSTUFF R4660 AND R4661.
- REMOVE MIN_NECK_WIDTH=0.3MM FROM PP5V_S3_USB2_EXTA/B.
- EDIT BOM OPTION TABLE.
- CHANGE GFX_VID<1:4> TO GFX_VID<0:3>.
- SIZING DOWN R2205 FROM 0603 TO 0402 FOR PLACEMENT.
- 5282756 ADD C2207 (0.1UF, 0402).

CSA PAGE 22:
- CHANGE NB FROM 338S0426(500M) TO 343S0448(667M).
- CHANGE BETTER CPU FROM 337S3456(2.0G) TO 337S3464(2.2G).
- CHANGE GOOD CPU FROM 337S3471(1.8G) TO 337S3463(2.0G).

M70 DVT TO K36 CHANGES

SYNC FROM AUDIO TEAM.
- CHANGE U1400 FROM 343S0448 TO 338S0516(NB667, PRQ).
- PP5V_S5_REG_P BECOMES =PP5V_S5_REG.
- PP3V3_S5_REG_P BECOMES =PP3V3_S5_REG.
- PP1V5_S0_REG_P BECOMES =PP1V5_S0_REG.
- DELETE XW7320.
- ADD OMIT TO L9405, L9406 AND L9407.
- ADD ALTERNATE TABLE TO MAKE 155S0310 ALTERNATE OF 155S0322.
- ADD ALTERNATE TABLE TO MAKE 155S0369 ALTERNATE OF 155S0326.

CSA PAGE 43:
(C2205,C4800,C4804,C7305,C7500,C7605,C7902,C7911,C7912)

K36 DVT1 TO DVT2 CHANGES

- CHANGE R9211 AND R9212 FROM 16.5K TO 9.09K.

7/24/2007
- UPDATE SYMBOL FOR U5930, VENDOR PART NUMBER CHANGES FROM SMB380 TO BMA150.

CSA PAGE 59:
- CHANGE BEST CPU FROM 337S3465(2.4GHZ) TO 337S3464(2.2GHZ).

7/13/2007
- NORMAL CHANGES FROM 514-0375 TO 514-0480, FANCY CHANGES FROM 514-0376 TO 514-0481.

CSA PAGE 62:
- SMC MANAGEMENT SMBUS CONNECTION:
  - SMB_ME_CLK AND SMB_ME_DATA ON SOUTHBRIDGE DISCONNECTED FROM SMB_MGMT_CLK AND SMB_MGMT_DATA FROM SMC.
  - ICH8-M ME SMBUS:
    - REMOVE ALIAS FOR =SMC_SMS_INT TO SMC_PG1 - SIGNAL SHOULD JUST BE CALLED SMC_SMS_INT.

CSA PAGE 49:
- ADD CRITICAL TO U4401.

9/13/2007
- SMC PART NUMBER CHANGES FROM 341S2088 TO 341S2198.
<table>
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</table>

**Standard Voltages:**

- 1.0 V (Clamp Unused)
- 2.0 V (Clamp Unused)
- 2.5 V (Clamp Unused)
- 3.0 V (Clamp Unused)
- 3.3 V (Clamp Unused)

**Low Voltages:**

- 1.8 V (Clamp Unused)
- 2.6 V (Clamp Unused)
- 3.4 V (Clamp Unused)
- 4.0 V (Clamp Unused)
- 4.8 V (Clamp Unused)

**Ultra Low Voltages:**

- 5.0 V (Clamp Unused)
- 6.0 V (Clamp Unused)
- 7.0 V (Clamp Unused)
- 8.0 V (Clamp Unused)
- 9.0 V (Clamp Unused)

**CPU Core Power:**

- 9.4 A (Enhanced Deeper Sleep)
- 11.5 A (Deeper Sleep)
- 16.0 A (Deep Sleep SuperLFM)
- 16.8 A (Sleep SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)

**Low Voltage:**

- 2500 mA (after VCC stable)
- 4500 mA (before VCC stable)

**CPU VCC (Core Power):**

- 130 mA

**CPU VID (Core Power):**

- 7C7

**CPU VCCP:**

- 7C7

**CPU VCCSENSE:**

- 7C7

**CPU VSSSENSE:**

- 7C7

**CPU INTERNAL PLL POWER (1.5V):**

- 11B3

**CPU IO POWER (1.05V):**

- 2500 mA (after VCC stable)

**CPU INTERNAL PLL POWER (1.5V):**

- 7C7

**TBD A (Enhanced Deeper Sleep):**

- 18.7 A (LFM)
- 21.0 A (HFM)

**TBD A (Deep Sleep LFM):**

- 17.0 A (Design Target)
CPU VCORE HF AND BULK DECOUPLING
4x 330uF, 20x 10uF 0805

PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1200, C1201, C1202 AND C1203 NEED TO USE 6mOHM CAPS.

CRITICAL
critical
C1204
10UF
X5R
6.3V

VCCP (CPU I/O) DECOUPLING
1x 330uF, 6x 5.1uF

PLACE C1281 NEAR PIN B26 OF U1000

VCCA (CPU AVdd) DECOUPLING
1x 10uF, 1x 0.01uF

PLACE C1280 NEAR C1281

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SYNC_DATE=04/26/2006

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CPU ITP700FLEX DEBUG SUPPORT

XDP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR’S TCK PIN TO CPU’S TCK PIN AND THEN FINE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR’S TCK PIN.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.

TV_DCONSELx to GND.

Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and follow instructions for LVDS and CRT & TV-Out Disable above.

VCCD_CRT, VCCD_QDAC and VCC_SYNC.

Can tie the following rails to GND:

VSYNC and CRT_TVO_IREF to GND.

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, CRT_DISABLE / TV_OUT_ENABLE.

TV-OUT Disable / CRT Enable

CRT Disable / TV-OUT Enable

S-Video: DACB & DACC only.

decoupling. Otherwise, tie VCCD_LVDS to GND also.

LVDS Disable
Current numbers from Crestline EDS, doc #21749.

80 mA @ 667MHz DDR (1.05V)
730 mA @ 806MHz DDR (1.09V)
540 mA @ 1067MHz DDR (1.25V)

PP1V5_S0_NB_VCCD_TVDAC
PP1V5_S0_NB_VCCD_CRT
PP3V3_S0_NB_VCCA_TVDACA
PP3V3_S0_NB_VCCA_TVDACB
PP3V3_S0_NB_VCCA_TVDACC
PP1V25_S0M_NB_VCCA_SM_CK2
PP1V25_S0M_NB_VCCA_SM_CK
PP1V25_S0M_NB_VCCA_SM
PP1V25_S0M_NB_VCCA_SM_CK1
PP1V25_S0M_NB_VCCA_SM_CK3
PP1V25_S0M_NB_VCCA_SM_CK4
PP1V25_S0M_NB_VCCA_SM_CK5
PP1V25_S0M_NB_VCCA_SM_CK6
PP1V25_S0M_NB_VCCA_SM_CK7
PP1V25_S0M_NB_VCCA_SM_CK8
PP1V25_S0M_NB_VCCA_SM_CK9
PP1V25_S0M_NB_VCCA_SM_CK10

PP1V8_S3M_NB_VCCSMCK
PP1V25_S0_NB_VCCDMI
PP1V25_S0_NB_VCCAXF
PP1V25_S0M_NB_VCCAXD
PP3V3_S0_NB_VCCA_PEG_PLL
GND_NB_VSSA_PEG_BG
PP3V3_S0_NB_VCCA_PEG_BG
GND_NB_VSSA_LVDS
PP1V8_S0_NB_VCCTXLVDS
PP1V25_S0M_NB_VCCA_MPLL
PP1V25_S0_NB_VCCA_DPLLA
GND_NB_VSSA_DAC_BG
PP3V3_S0_NB_VCCA_DAC_BG
PP3V3_S0_NB_VCCA_CRT_DAC2
PP3V3_S0_NB_VCCA_CRT_DAC1
VCC_SYNC

LVDS
TV/CRT
SM CK
PEG
AXF
AXD
HVTTL
VCC_RXR_DMI2
VCC_RXR_DMI1
VCC_PEG5
VCC_PEG4
VCC_PEG3
VCC_PEG2
VCC_AXF3
VCC_AXF2
VCC_AXF1
VCC_AXD6
VCC_AXD5
VCC_AXD3
VCC_AXD2
VCC_AXD1
VCC_HV2
VCC_DMI
VTTLF3
VTTLF1
VTT21
VTT19
VTT18
VTT14
VTT13
VTT12
VTT11
VTT10
VTT9
VTT8
VTT7
VTT6
VTT5
VTT4
VTT3
VTT2
VTT1

NB Power 2

SHT 19
REV. 1
SCALE 1
SIZE 1

SYNC_DATE=10/30/2006

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Current numbers from Crestline EDS Addendum, doc #20127.

VCCD_TVDAC also powers internal thermal sensors.

NOTE: This filter is required even if using only external graphics.

VID<3:0>=1001=1.05575V
GFX_VID<1>
GFX_VID<0>
0011=1.21025V
1000=1.08150V
GFX_VID<3>

MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.2 MM

R2205
100
MF-LF

18B3
15B7

C2205
X5R
10V
10%

402
CERM
10V
10%

22K
402
2
1
NO STUFF

22000pF-1000mA

R2247
402
1/16W

CRITICAL
CRITICAL
NFM18

(1.7V - 5.5V)

WARNING VOLTAGE DROP

=PP1V8_S0_NB_VCCD_LVDS

1.5V

MIN_LINE_WIDTH=0.6 MM

VOLTAGE=1.5V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.2 MM

PP1V5_S0_NB_VCCD_CRT

PP1V5_S0_NB_VCCD_QDAC

VOLTAGE=1.5V

MIN_LINE_WIDTH=0.2 MM

MIN_NECK_WIDTH=0.2 MM

PP1V5_S0_NB_FOLLOW

PP1V5_S0_NB_VCCSYNC

PP1V25_S0_NB_DPLL

PP1V25_S0_NB_DPLL_RF

PP3V3_S0_NB_CRTDAC_F

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.4 MM

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.6 MM

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.4 MM

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.4 MM

PP3V3_S0_NB_TVDAC

VOLTAGE=1.25V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.2 MM

PP3V3_S0_NB_VCCA_DAC_BG

VOLTAGE=1.25V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.2 MM

PP3V3_S0_NB_VCCA_CRTDAC

VOLTAGE=1.25V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.2 MM

PP3V3_S0_NB_VCCSYNC

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.4 MM

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.4 MM
This will allow us to sequence this part under wireless card. It may take a few days before this is done through.

2-input NAND gate-APN:311S0304

Pulled a new APN for U2803(0.6mm max)

This part is never stuffed, this is done through.

This will allow us to sequence this part under wireless card.
SELIGO RECOMMEND TO REMOVE L2903, R2900, C2907, C2910
R2901, L2902, C2916, C2911, C2914 and R2902

ORIGINAL DESIGN:
USE 1550302 FOR L2902(R2906) AND L2903(R2907)
STUFF C2907, C2910, C2916, C2911, C2914
USE 2.1OHM FOR R2906, R2901 AND 10OHM FOR R2902

NEED TO CHECK CAP VALUE

U2900 HAS INTERNAL PU ON PGMODE
(ICH8M PCI 33MHZ)
(PCI SLOT)
(FW PCI 33MHZ)

CRITICAL

VDD_A
VDD_PCI
VDD_CPU

Pink-Power 125-0.025-.1 R

MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm

Out of Pin 8 TO Enable INT Ready (B)

PP3V3_S0_CK505_VDDA_R
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm

R2901

Out of Pin 8 TO Enable INT Ready (A)

R2907

Out of Pin 8 TO Enable INT Ready (C)

Out of Pin 8 TO Enable INT Ready (D)

acao. This document is not intended for public distribution or use as a substitute for the manufacturer's original instruction manual.

www.vinafix.vn
One cap for each side of every RPAK, one cap for every two discrete resistors

**LAYOUT NOTE:** PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP3309_80_MEM_TERM
ENET Enable Generation

3.3V ENET FET

```
Vout = 1.2246V * (1 + R3821 / R3822)
```

1.9V ENET LDO

```
Vout = 1.2246V * (1 + R3821 / R3822)
```

1.2V ENET LDO

```
Vout = 1.2246V * (1 + R3821 / R3822)
```

Yukon Power Control

```
ENET Enable Generation
```

```
CRITICAL
Q3810
NOSTUFF
0.01UF
CERM
402
21
C3810
100K
MF-LF
5%
62B8 58B7 45A6 44C5 33C7 24D3
57C4 45B3 44D5 38C6 33C7
6C1
```

Apple Inc. 051-7559
PLACE ONE PAIR OF CAPS AT EACH PIN 3 AND 6 OF TRANSFORMERS.

ETHERNET CONNECTOR

PLACE C3911 AND C3912 ON EACH SIDE OF J3900

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PORT POWER CLASS

[Diagrams showing connections and circuitry]

LATE-VG DETECTION CIRCUIT

(R4350)

- [Description of circuit components and connections]

Enables port power whenever machine AC Adapter is plugged or system at run state with battery only.
both pull up resistors on SB page.

ICH8 GPIO5

**ODD_PWR_EN_L** is OD and core well

**ODD_RST_5V**

CORE RAIL 5V

**ODD detect** need less than 100ms include OS latency

**ODD_PWR_EN_L** is OD and core well

BLEED CIRCUIT TO DISCHARGE ODD POWER RAIL WHEN ODD IS DISABLED.
GEYSER AND DIMM0 REMOTE TEMP SENSORS

PLACE L4701 NEAR J4700
PLACE C4700 NEAR J4700

516S0588

10% 0.01uF CERM 16V 402

R4710

20% 0.1UF 10V CERM 402

C4700

CRITICAL D4700

L4700

53307-1032 F-ST-SM

J4700

L4702

CRITICAL

 loneliness

L4703

10% 0.01uF CERM 16V 402

R4700

20% 0.1UF 10V CERM 402

C4703

L4701

TCM1005 90-OHM-100MA CRITICAL 439 3 2 1

R4710

1.2 1.2

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=0V

PP5V_S3_GEYSER_F

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

PP5V_S3_GEYSER_F
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as inputs can be left floating, those designated as inputs require pull-ups.

1. If SMS interrupt is not used, pull up to SMC rail.

2. Unused pins have "SMC_Pxx" names.
SMBUS CONNECTIONS

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DRAWING NUMBER
SHT OF
SIZE

Apple Inc.
051-7559

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SPI ROMs

PLACEMENT NOTE: Place R6190 within 12.7mm of U2300

PLACEMENT NOTE: Place R6191 within 12.7mm of U2300

PLACEMENT NOTE: Place R6114 within 12.7mm of U2300

PLACEMENT NOTE: Place R6193 within 12.7mm of U2300

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SATELLITE & SUB TWEETER AMPLIFIER  APN:353S1595

SATELLITE  169 Hz < FC < 282 Hz
SUB  80 Hz < FC < 132 Hz
GAIN  12dB

VOLTAGE=5V
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 mm

RIGHT SATELLITE

LEFT SATELLITE

SUB-TWEETER

SATELLITE & SUB TWEETER AMPLIFIER  APN:353S1595

SATELLITE  169 Hz < FC < 282 Hz
SUB  80 Hz < FC < 132 Hz
GAIN  12dB

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GAIN  12dB

VOLTAGE=5V
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 mm

RIGHT SATELLITE

LEFT SATELLITE

SUB-TWEETER
DC-JACK INTERFACE

INRUSH LIMITER

ACIN DETECTION

BATTERY INTERFACE

LID HALL EFFECT SENSOR
IMVP6 CPU VCORE REGULATOR

NOTE 1: C7132, C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

---

**IMVP6 CPU VCORE REGULATOR**

**LATEST ISSUE: 2007/01/23**
1.5V/1.05V POWER SUPPLY

LATEST ISSUE: 2006/12/22

Vout = 0.758V * (1 + Ra / Rb)

Routing Note:
- The discharge path (VO1) should have a separate trace from the output voltage sensing trace.
- The discharge path (VO2) should have a separate trace from the output voltage sensing trace.

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=1 mm

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=1 mm

Routing Note:
- Place R7328 close to SMC.
- Place C7390, C7391 near NB.
- Place C7329, C7341 near SMC.

Placement Note:
- Place C7303 near U7301 pin 7.

Placement Note:
- Place RC close to SMC.

Routing Note:
- Place C7301 close to U7600 pin 16.

VOLTAGE=1.05V

PWM FREQ. = 300 kHz

PWM FREQ. = 360 kHz

MAX CURRENT = 8A

MAX CURRENT = 4A

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=1 mm

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=1 mm

1.5V / 1.05V Supplies

@Apple Inc. 2006, patent pending, Date: 07/11/2005

1.5V / 1.05V Supplies

1.5V / 1.05V Supplies

1.5V / 1.05V Supplies

1.5V / 1.05V Supplies

1.5V / 1.05V Supplies

1.5V / 1.05V Supplies

1.5V / 1.05V Supplies
1.8V/0.9V POWER SUPPLY

LATEST ISSUE: 2006/12/22

Vout = 0.75V * (1 + Ra / Rb)

Routing Note:
- Place XW7500, XW7501 near C7542 PIN 2

Placement Note:
- Using Kevin connection.
  - Q7521 PIN 1, 2, 3
  - Connect CS_GND to

Routing Note:
- Using separate trace.
  - Connect VDDQSNS to C7542 PIN 1

Placement Note:
- Place C7509 near NB

**1.8V/0.9V Supplies**

SYNC_MASTER = POWER

(*NOTICE OF PROPRIETARY PROPERTY*)
3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.25V S0 REGULATOR

Vout = 1.25V * (1 + Ra / Rb)

Continuous
Connect RUNSS off-page to control
If unconnected, powers up with PVIN.

3.42V/1.25V Switcher

LATEST ISSUE: 2007/3/8
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL

1.8V S3 RUN/SS CONTROL

5V S3 FET

3.3V S3 FET

LATEST ISSUE: 2006/12/22
Most CPU signals with impedance requirements are 55-ohm single-ended.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

Design Guide recommends FSB signals be routed only on internal layers.

Design Guide recommends each strobe/signal group is routed on the same layer.

DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.

All FSB signals with impedance requirements are 55-ohm single-ended.

NOTE: 7 mil gap is for VCCSense pair, which is allowed to space with 7 mil spacing without specifying a target differential impedance.

NOTE: CPU says to route with 7 mil spacing without specifying a target differential impedance. Note that 7 mil gap is for VCCSense pair, which is allowed to space with 7 mil spacing without specifying a target differential impedance.

SOURCE: Santa Rosa Platform DG, Rev 3.9 (#25517), Sections 4.2 & 4.3

CPU / FSB Net Properties

Cpu / FSB Constraints

CPU/FSB Constraints

NOTICE OF PROPRIETARY PROPERTY

SIZE

DRAWING NUMBER

051-7559

A

B

C

D

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### DDR2 Memory Bus Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Net Type</th>
<th>Spacing</th>
<th>Area Type</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MEM_DATA</td>
<td>1.5:1</td>
<td>MEM_45S</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>2</td>
<td>MEM_DATA</td>
<td>3:1</td>
<td>MEM_55S</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>3</td>
<td>MEM_DATA</td>
<td>2:1</td>
<td>MEM_85D</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>4</td>
<td>MEM_DATA</td>
<td>4:1</td>
<td>MEM_85D</td>
<td>85_OHM_DIFF</td>
</tr>
</tbody>
</table>

### Memory Net Properties

<table>
<thead>
<tr>
<th>Layer</th>
<th>Net Type</th>
<th>Spacing</th>
<th>Area Type</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MEM_DATA</td>
<td>1.5:1</td>
<td>MEM_45S</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>2</td>
<td>MEM_DATA</td>
<td>3:1</td>
<td>MEM_55S</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>3</td>
<td>MEM_DATA</td>
<td>2:1</td>
<td>MEM_85D</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>4</td>
<td>MEM_DATA</td>
<td>4:1</td>
<td>MEM_85D</td>
<td>85_OHM_DIFF</td>
</tr>
</tbody>
</table>

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Revision: 06/08/2006

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Vina Fix Inc.
### PCI Bus Constraints

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<tbody>
<tr>
<td>CB</td>
<td>100</td>
<td>5</td>
<td>300</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>CB</td>
<td>55</td>
<td>5</td>
<td>300</td>
<td>55</td>
<td>55</td>
<td>55</td>
</tr>
</tbody>
</table>

**Adjusted**: 30 mils min separation.

### Controller Link (AMT) Constraints

<table>
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<tr>
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<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>CB</td>
<td>100</td>
<td>5</td>
<td>300</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>CB</td>
<td>55</td>
<td>5</td>
<td>300</td>
<td>55</td>
<td>55</td>
<td>55</td>
</tr>
</tbody>
</table>

**Adjusted**: 30 mils min separation.

### Platform LAN (Nineveh) Constraints

<table>
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<tbody>
<tr>
<td>CB</td>
<td>100</td>
<td>5</td>
<td>300</td>
<td>100</td>
<td>100</td>
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<td>CB</td>
<td>55</td>
<td>5</td>
<td>300</td>
<td>55</td>
<td>55</td>
<td>55</td>
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</tbody>
</table>
# Clock Signal Constraints

**PHYSICAL_RULE_SET**

- **CLK_SLOW_55S**
- **CLK_MED**
- **CLK_FSB**

**TABLE_PHYSICAL_RULE_ITEM**

<table>
<thead>
<tr>
<th>Component</th>
<th>Name</th>
<th>Value</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>CK505_SRC6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_SRC5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_SRC4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_SRC1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

---

# Clock Net Properties

<table>
<thead>
<tr>
<th>Clock Net Name</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK505_DOT96</td>
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<td></td>
</tr>
<tr>
<td>CPU_BSEL0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_PCI4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_PCIF1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_NB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_PCI2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_PCI1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_USB48_FSA</td>
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<td></td>
</tr>
<tr>
<td>CK505_PCI4_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK505_PCI1_CLK</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Source:** www.vinafix.vn