1. All capacitance values are in microfarads.
2. All resistance values are in ohms, 0.1 watt +/- 5%.
### TABLE 5

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
</table>

### CRITICAL BOM OPTION

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
</table>

### ALTERNATES OPTION

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
</table>

### BOARD STACK-UP AND CONSTRUCTION

**Top**
- SIGNAL
- GROUND
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- GROUND
- POWER
- POWER
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- GROUND
- SIGNAL

**Bottom**
- SIGNAL
NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.
1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)

From XDP connector or via level translator

U0500
CPU

U1000
CPU

To XDP connector and/or level translator

From XDP connector

U1400
MCP

XDP connector

XDP connector

JTAG Scan Chain

SYNC_DATE=08/17/2008
SYNC_MASTER=K36B_MLB

JTAG_LVL_TRANS_EN_L = PP1V05_S0_CPU
JTAG_MCP_TRST_L = TRUE
JTAG_MCP_TMS = TRUE
JTAG_MCP_TDI = TRUE
JTAG_MCP_TCK = TRUE
JTAG_MCP_TDO = TRUE
JTAG_MCP_TDO_CONN = TRUE
JTAG_MCP_TRST_L = TRUE
JTAG_MCP_TMS = TRUE
JTAG_MCP_TDI = TRUE
JTAG_MCP_TCK = TRUE
JTAG_MCP_TDO = TRUE
JTAG_MCP_TDO_CONN = TRUE
Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC FROM T18

CPU Power & Ground

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Three lines are not to be reproduced or copied in any form.

30.4 A (SV LFM)

41 A (SV HFM)

44 A (SV Design Target)

23 A (LV Design Target)

2500 mA (after VCC stable)

4500 mA (before VCC stable)

VCC (CORE POWER)

VCC (CORE POWER)

PLACEMENT NOTE=Place R1101 within 25.4mm of CPU, no stubs.

PLACEMENT NOTE=Place R1100 within 25.4mm of CPU, no stubs.
CPU VCore HF and Bulk Decoupling

CPU Decoupling

VCCA (CPU AVdd) DECOUPLING

VCCP (CPU I/O) DECOUPLING
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
See with XDP-XDP adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module
Use with 920-0620 adapter board to support CPU, MCP debugging.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

24 16 8

\[=PP1V8R1V5_S0_MCP_MEM\]

R1611 40.2 MF-LF 1/16W
R1610 402 1% MF-LF 1/16W
R1610 402 1% MF-LF 1/16W

\[87 \text{ mA} \ (A01)\]

\[=PP1V05_S0_MCP_PLL_CORE\]

TP_MEM_A_CLK4N
TP_MEM_A_CLK5N
TP_MEM_A_CLK5P
MCP_MEM_COMP_VDD
TP_MEM_A_CLK3N
TP_MEM_A_CLK3P
TP_MEM_A_CKE<2>
TP_MEM_A_ODT<3>
TP_MEM_A_ODT<2>
TP_MEM_A_CS_L<2>

39 mA
12 mA
17 mA

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MCP Memory Misc
SIZE
SCALE
DRAWING NUMBER
REV.
051-7852
A.0.1

SYNC_DATE=08/17/2008
SYNC_MASTER=K36B_MLB
MCP PCIe Interfaces

IF PCI EXPRESS IS NOT USED, VIOLATE COPRy AND BLOCK GEP

SYNC_DATE=08/17/2008
SYNC_MASTER=K36B_MLB
SYNC FROM T18
REMOVE MCP 27MHz CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
Apples: ???
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
Apples: 1x 2.2uF 0402 (2.2 uF)

206 mA (A01)
NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

190 mA (A01, 1.8V)
WF: Open question on which packge option(s) nVidia can support.
Apple: 1x 2.2uF 0402 (2.2 uF)

HDCP ROM
WF: Open question on which packge option(s) nVidia can support.
CHANGE Y2810 AND U2850 TO SMALLER PARTS
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE RESET BUTTOM TO RESET PADS
SYNC FROM T18

RTC Power Sources

RTC Crystal

MCP 25MHz Crystal

Reset Button

MCP 50 PWRGD

Platform Reset Connections
LPC Reset (Unbuffered)
PCIE Reset (Unbuffered)

SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS
Voltage divider resistor values at op-amp outputs not yet finalized.

**ROM OPTION TO SELECT VREF SOURCE**

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2901</td>
<td>100K MF-LF</td>
<td>1</td>
<td>VREFMRGN_DQ_SODIMMB_EN</td>
</tr>
<tr>
<td>R2902</td>
<td>100K MF-LF</td>
<td>1</td>
<td>VREFMRGN_DQ_SODIMMA_BUF</td>
</tr>
<tr>
<td>R2903</td>
<td>100K MF-LF</td>
<td>1</td>
<td>VREFMRGN_CPUFSB_BUF</td>
</tr>
<tr>
<td>R2904</td>
<td>100K MF-LF</td>
<td>1</td>
<td>VREFMRGN_DQ_SODIMMB_BUF</td>
</tr>
<tr>
<td>R2905</td>
<td>100K MF-LF</td>
<td>1</td>
<td>VREFMRGN_CPUFSB_EN</td>
</tr>
</tbody>
</table>

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.25 mm

SYNC_DATE=08/17/2008

IEEE Standard for Switching and Timing
The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.
One cap for each side of every RPAK, one cap for every two discrete resistors
BOM OPTION shown at the top of each group applies to every part below it.

LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO FPDV9_SO_MEM_TERM
WLAN Enable Generation

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

WLAN Enable Generation

3.3V ENET FET

I(max) = 1.7A (85C)
Rds(on) = 90mOhm max
@ 2.5V Vgs:

3.3V ENET FET

1.05V ENET FET

R3800

10K
5%
402
1/16W
MF-LF

CRITICAL

R3842

69.8K
1/16W
1%
402
MF-LF

PLACEMENT_NOTE=Place close to U1400

R3810

100K
1%
402
5W
MF-LF

CRITICAL

R3841

22
1/16W
20.0K
1%
402
MF-LF

CRITICAL

R3841

SOT563
SSM6N15FEAPE

Q3801

SOT563
SSM6N15FEAPE

Q3805

SSM6N15FEAPE

Q3805

SSM6N15FEAPE

Q3840

SI2312BDS
SOT23

Q3841

SSM6N15FEAPE

SOT563

C3810

10%
402
0.01UF
16V
CERM

C3811

0.033UF
20%
402
X5R
10V

C3841

10%
402
0.01UF
16V
CERM

C3841

0.1UF
20%
CERM
10V

CERM

C3840

0.1UF
20%
CERM
10V

R3800

10K
5%
402
1/16W
MF-LF

R3810

10K
5%
402
1/16W
MF-LF

R3840

20.0K
1%
402
1/16W
MF-LF

R3841

10K
402
1/16W
1%
MF-LF

R3842

69.8K
1/16W
1%
402
MF-LF

R3841

22
1/16W
20.0K
1%
402
MF-LF

R3841

SOT563
SSM6N15FEAPE

Q3801

SOT563
SSM6N15FEAPE

Q3805

SSM6N15FEAPE

Q3841

SSM6N15FEAPE

SOT563

Ethernet & AirPort Support

SYNCHRONISATION
SYNC_DATE=04/04/2008
SYNC_MASTER=SUMA

MCP_CLK25M_BUF0_R
RTL8211_CLK25M_CKXTAL1

P1V05ENET_EN
SMC_ADAPTER_EN
AC_OR_S0_L

P3V3ENET_EN_L
P1V05ENET_EN_L
PM_SLP_S3_L
PM_WLAN_EN_L

PP3V3_ENET_FET=PP3V3_S5_P3V3ENETFET
PP1V05_ENET_P1V05ENETFET
PP1V05_ENET_FET
PP3V3_S5_P1V05ENETFET
PP3V3ENET_SS
P1V05ENET_SS
P3V3ENET_SS
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ETHERNET CONNECTOR

ENET_CONN_CTAP
ENET_MDI_N<0>
ENET_MDI_TRAN_P<0>
ENET_MDI_TRAN_N<0>
ENET_MDI_TRAN_P<2>
ENET_MDI_TRAN_N<2>
ENET_MDI_TRAN_N<3>
ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>
ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_N<3>
ENET_MDI_P<0>
ENET_MDI_P<1>
ENET_MDI_P<2>
ENET_MDI_P<3>
ENET_CNTR_TAP<0>
ENET_CNTR_TAP<1>
ENET_CNTR_TAP<2>
ENET_CNTR_TAP<3>
ENET_CENTER_TAP<0>
ENET_CENTER_TAP<1>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<3>

R3900
R3901
R3902
R3903

C3900
C3901
C3902
C3903

X5R
16V
10%
0.1UF

T3901
T3902

CRITICAL

CERM
1206
10%
1000PF
2KV

CRITICAL

TLA-6T213HF

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If SMS interrupt is not used, pull up to SMC rail.
ADD NC ALIASES FOR FAN1 SIGNALS

SMC Reset "Button" / Poweron Detect

SMC Crystal Circuit

SMC AVREF Supply

System (Sleep) LED Circuit

SMC Support

PAGE 1 OF 1
CPU Voltage Sense / Filter

MCP Voltage Sense / Filter

PBUS VOLTAGE SENSE ENABLE & FILTER

---

C5359
6.3V
0.22UF
X5R
402
20%

R5359
4.53K
1%
1/16W
MF-LF
402

C5385
402
6.3V
20%
X5R
0.22UF

R5385
1%
402
MF-LF
1/16W
27.4K

R5386
1%
1/16W
MF-LF
402
5.49K

---

R5315
1/16W
1%
402

---

R5309
1/16W
1%
402
4.53K

---

PLACEMENT_NOTE=Place near U1400 center

---

PLACEMENT_NOTE=Place near U1000 center

---

APPLE INC. 50-5905-01
ARCHIVE:D:01:01
DRAWING NUMBER
SHT OF
SIZE

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NOTICE OF PROPRIETARY PROPERTY
CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor

DETECT CPU PROXIMITY TEMPERATURE

DETECT MCP PROXIMITY TEMPERATURE

DETECT CPU DIE TEMPERATURE

DETECT MCP DIE TEMPERATURE

DETECT FIN-STACK TEMPERATURE

DETECT HEAT-PIPE TEMPERATURE

Placement Note: Place U5515 near CPU

Placement Note: Place U5535 near MCP

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25MHz is selected with R5164 and R5144
Any of the 4 frequencies can be selected
with R6190, R6191, R5164 and R5144
DO WE NEED TO CHANGE BATTERY CONNECTOR?

- MagSafe DC Power Jack

1-Wire OverVoltage Protection

LID HALL EFFECT SENSOR

BATTERY/LID CONNECTOR

DC-In & Battery Connectors

- Battery/Lid connector
- MagSafe DC Power Jack
- 1-Wire OverVoltage Protection
- LID HALL EFFECT SENSOR
- BATTERY/LID CONNECTOR

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MCP VCORE/5V_S3 LEFT REGULATOR

- Changed R7514 to 280K, R7564 to 180K.
- C7500 changed to 138S0638.
- R7591 to 237K.
- R7580 to 475K.
- R7581 to 214K.
- MCP_VID1_RC.
- MCP_VID1_L.
- MCPCORES0_ILIM.
- MCPCORES0_UGATE.
- MCPCORES0_PHASE.
- MCPCORES0_LGATE.
- MCP_VID1_LGATE.
- MCP_VID1_PHASE.

Rev A01 Production

<table>
<thead>
<tr>
<th>VID</th>
<th>Voltage</th>
<th>Voltage</th>
<th>Voltage</th>
<th>MCP Target</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>+1.224V</td>
<td>+1.060V</td>
<td>+1.050V</td>
<td></td>
</tr>
<tr>
<td>001</td>
<td>+1.150V</td>
<td>+0.994V</td>
<td>+0.980V</td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>+1.105V</td>
<td>+0.927V</td>
<td>+0.905V</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>+0.849V</td>
<td>+0.645V</td>
<td>+0.905V</td>
<td></td>
</tr>
<tr>
<td>500</td>
<td>+0.950V</td>
<td>+0.830V</td>
<td>+0.830V</td>
<td></td>
</tr>
<tr>
<td>501</td>
<td>+0.850V</td>
<td>+0.780V</td>
<td>+0.800V</td>
<td></td>
</tr>
<tr>
<td>510</td>
<td>+0.810V</td>
<td>+0.720V</td>
<td>+0.700V</td>
<td></td>
</tr>
<tr>
<td>511</td>
<td>+0.870V</td>
<td>+0.710V</td>
<td>+0.700V</td>
<td></td>
</tr>
</tbody>
</table>

- VOUT = 0.7V * (1 + Ra / Rb)
- Vout = 0.7V * (1 + Ra / Rb)
FireWire 1.0V (Core) Supply

1.5V S0 SWITCH
EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch.

TMDS (MINI DVI) INTERFACE

PLACE THE RESISTOR CLOSE TO MCP79 AND THE CAP NEAR J4001

DVI power DIO: on page 95 (D9050)

PLACE THE RESISTOR CLOSE TO MCP79 AND THE CAP NEAR J4001

For 10 signals, we need follow MIT’s recommendations. Do we need change the segment impedance base on SD design rule.

For 1 segment, 35 ohm from 0K to 150 ohm. Top/bottom layer width is 0.13 mm
For 2 segments, 35 ohm from 0K to connector, top/bottom layer width is 0.17 mm

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The MINI-DVI CONNECTOR

Apple Inc.
### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
</table>

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Properties</th>
</tr>
</thead>
</table>

### CPU Signal Constraints

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
</table>

### MCP FSB Comp Signal Constraints

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
</table>

### FSB Clock Constraints

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
</table>

### CPU/FSB Constraints

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
</table>

---

**Notes:**
- All signals with impedance requirements are to be single-ended.
- FSB 4X signals shown in signal table on right.
- FSB 1X signals shown in signal table on right.
- CPU/FSB signals have impedance requirements as per the document.
- PAR signals have impedance requirements as per the guidelines.
- FSB DSTB# complementary pairs should be matched within 300 ps of each other.
- All DSTB#s should be matched to +/- 300 ps.
- Signals within each 4x group should be matched within 5 ps of strobe.
- All 4X/2X/1X FSB signals with impedance requirements are 50-ohm single-ended.

---

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**Memory Bus Constraints**

<table>
<thead>
<tr>
<th>MCP MEM COMP</th>
<th>Signal Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.</td>
<td></td>
</tr>
</tbody>
</table>

**Memory Bus Spacing Group Assignments**

<table>
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<tr>
<th>MCP MEM COMP</th>
<th>Memory Bus Spacing Group Assignments</th>
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**MCU MEM COMP Signal Constraints**

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**MCU MEM COMP Signal Constraints**

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<th>Memory Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.</td>
<td></td>
</tr>
</tbody>
</table>
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

- 75-ohm from output of three-pole filter to connector (if possible).
- 50-ohm from first to second termination resistor.
- 37.5-ohm from MCP to first termination resistor.
## SPI Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

## SIO Signal Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

## SMBus Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

## USB 2.0 Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

## LPC Bus Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

## PCI Bus Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

---

### Table: Layer Minimum Neck Width

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table: Physical Rule Set

<table>
<thead>
<tr>
<th>Line-To-Line Spacing</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table: Spacing Rule Item

<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

### Table: Physical Rule Set

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>Line-To-Line Spacing</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table: Spacing Rule Item

<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>Net Type</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>Line-To-Line Spacing</th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>Net Type</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>Line-To-Line Spacing</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>Net Type</th>
<th>Layer</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table: Spacing Rule Item

<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
MCP RGMII (Ethernet) Constraints

88E1116R (Ethernet PHY) Constraints

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

Ethernet Constraints
FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Port 1</th>
<th>Port 2</th>
<th>Port 3</th>
<th>Port 4</th>
<th>Port 5</th>
<th>Port 6</th>
<th>Port 7</th>
<th>Port 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FireWire Net Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 2</td>
<td>Hot</td>
</tr>
</tbody>
</table>

FireWire Constraints

- FW_P1_TPB
- FW_110D
- FW_PP1_TPB_P
- FW_PP1_TPB_N
- FW_P1_TPA
- FW_110D
- FW_PP1_TPA_P
- FW_PP1_TPA_N
- FW_PORT_A_P
- FW_P1_TPA_P
- FW_PP1_TPA_N
- FW_PP1_TPB_P
- FW_PP1_TPB_N
- FW_PORT_B_P
- FW_P0_TPB_P
- FW_P0_TPB_N
- FW_PP0_TPB_P
- FW_PP0_TPB_N
- FW_PP0_TPA_P
- FW_PP0_TPA_N
- FW_PP0_TPA_P
- FW_PP0_TPA_N
- FW_PP0_TPB_P
- FW_PP0_TPB_N
### SMC SMBus Net Properties

<table>
<thead>
<tr>
<th>NET</th>
<th>NETTYPE</th>
<th>WIDTH</th>
<th>LENGTH</th>
<th>GAP</th>
<th>RULESET</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_SA_SCL</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_SA_SDA</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
</tbody>
</table>

### SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>NET</th>
<th>NETTYPE</th>
<th>WIDTH</th>
<th>LENGTH</th>
<th>GAP</th>
<th>RULESET</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSI_P</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>CHGR_CSO_P</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>CHGR_CSO_N</td>
<td>=STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>=STANDARD</td>
<td>1TO1_DIFFPAIR</td>
<td></td>
</tr>
<tr>
<td>LAYER MINIMUM NECK WIDTH</td>
<td>MAXIMUM NECK LENGTH</td>
<td>DIFFPAIR PRIMARY GAP</td>
<td>DIFFPAIR NECK GAP</td>
<td>PHYSICAL_RULE_SET</td>
<td></td>
<td></td>
</tr>
<tr>
<td>--------------------------</td>
<td>---------------------</td>
<td>----------------------</td>
<td>------------------</td>
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<td></td>
</tr>
<tr>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

For example:

- **TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, BOTTOM**
- **STANDARD**
- **DEFAULT**
- **0.185 MM**
- **TOP, BOTTOM**

Other details include:

- **BGA_P1MM**
- **1.5:1_SPACING**
- **0.15 MM**
- **STANDARD**

This document contains specific physical constraints and spacing rules for a board, ensuring proper layout and functionality in device manufacturing.