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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# K36B MLB SCHEMATIC

REFERENCED FROM T18  
01/06/2009

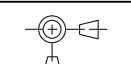
REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
?		?	?		
				DATE	DATE
				?	?

Page	(.csm)	Contents	Date
1	1	Table of Contents	K36B_MLB 08/22/2007
2	2	System Block Diagram	K36B_MLB 08/17/2008
3	3	Power Block Diagram	K36B_MLB 08/17/2008
4	4	CONFIGURATION OPTIONS	K36B_MLB 08/17/2008
5	5	Revision History	K36B_MLB
6	6	JTAG Scan Chain	K36B_MLB 08/17/2008
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8	8	Power Aliases	K36B_MLB
9	9	SIGNAL ALIAS	K36B_MLB
10	10	CPU FSB	K36B_MLB 08/18/2008
11	11	CPU Power & Ground	K36B_MLB 08/17/2008
12	12	CPU Decoupling	K36B_MLB 08/17/2008
13	13	eXtended Debug Port (MiniXDP)	M99_MLB 01/08/2008
14	14	MCP CPU Interface	K36B_MLB 08/17/2008
15	15	MCP Memory Interface	K36B_MLB 08/17/2008
16	16	MCP Memory Misc	K36B_MLB 08/17/2008
17	17	MCP PCIe Interfaces	K36B_MLB 08/17/2008
18	18	MCP Ethernet & Graphics	K36B_MLB 08/17/2008
19	19	MCP PCI & LPC	K36B_MLB 08/17/2008
20	20	MCP SATA & USB	K36B_MLB 08/17/2008
21	21	MCP HDA & MISC	K36B_MLB 08/17/2008
22	22	MCP Power & Ground	K36B_MLB 08/17/2008
23	24	MCP79 A01 Silicon Support	K36B_MLB 08/17/2008
24	25	MCP Standard Decoupling	K36B_MLB 08/17/2008
25	26	MCP Graphics Support	K36B_MLB 08/17/2008
26	28	SB Misc	K36B_MLB 08/17/2008
27	29	FSB/DDR2 VREF MARGINING	K36B_MLB 08/17/2008
28	31	DDR2 SO-DIMM Connector A	K36B_MLB 08/17/2008
29	32	DDR2 SO-DIMM Connector B	K36B_MLB 08/17/2008
30	33	Memory Active Termination	K36B_MLB 08/17/2008
31	34	Right Clutch Connector	K36B_MLB 08/17/2008
32	37	Ethernet PHY (RTL8211CL)	SUMA 03/20/2008
33	38	Ethernet & AirPort Support	SUMA 04/04/2008
34	39	ETHERNET CONNECTOR	SUMA 04/04/2008
35	41	FireWire LLC/PHY(FW643E)	K36B_MLB 08/17/2008
36	42	FireWire Port Power	K36B_MLB 08/17/2008
37	43	FireWire Ports	K36B_MLB (MASTER)

Page	(.csm)	Contents	Date
38	45	SATA Connectors	K36B_MLB 08/17/2008
39	46	External USB Connectors	K36B_MLB 08/17/2008
40	48	Front Flex Support	K36B_MLB 07/17/2008
41	49	SMC	K36B_MLB 08/17/2008
42	50	SMC Support	K36B_MLB 08/17/2008
43	51	LPC+SPI Debug Connector	K36B_MLB 08/17/2008
44	52	SMBUS CONNECTIONS	K36B_MLB 08/17/2008
45	53	VOLTAGE SENSING	K36B_MLB 08/17/2008
46	54	Current Sensing	K36B_MLB 08/17/2008
47	55	Thermal Sensors	K36B_MLB 08/17/2008
48	56	Fan	K36B_MLB 08/17/2008
49	58	GEYSER	K36B_MLB 08/17/2008
50	59	SMS	K36B_MLB 08/17/2008
51	61	SPI ROM	K36B_MLB 08/17/2008
52	62	AUDIO: CODEC	K36A_MLB 08/29/2008
53	66	AUDIO: SPEAKER AMP	K36A_MLB 08/29/2008
54	67	AUDIO: JACK	K36A_MLB 08/29/2008
55	68	AUDIO: JACK TRANSLATORS	K36A_MLB 08/29/2008
56	69	DC-In & Battery Connectors	RAYMOND 08/17/2008
57	70	PBUS Supply/Battery Charger	K36B_MLB 08/17/2008
58	72	5V/3.3V SUPPLY	K36B_MLB 08/17/2008
59	73	1.8V/0.9V DDR2 SUPPLY	K36B_MLB 08/17/2008
60	74	IMVP6 CPU VCore Regulator	K36B_MLB 08/17/2008
61	75	MCP VCore REGULATOR	K36B_MLB 08/17/2008
62	76	CPU VTT(1.05V) SUPPLY	K36B_MLB 08/17/2008
63	77	MISC POWER SUPPLIES	K36B_MLB 08/17/2008
64	78	POWER SEQUENCING	K36B_MLB 08/17/2008
65	79	POWER FETS	K36B_MLB 08/17/2008
66	90	INVERTER, LVDS	K36B_MLB 08/17/2008
67	93	TMDS ALIASES	K36B_MLB 08/17/2008
68	94	MINI-DVI CONNECTOR	K36B_MLB 08/17/2008
69	100	CPU/FSB Constraints	K36B_MLB 08/17/2008
70	101	Memory Constraints	K36B_MLB 08/17/2008
71	102	MCP Constraints 1	K36B_MLB 08/17/2008
72	103	MCP Constraints 2	K36B_MLB 08/17/2008
73	104	Ethernet Constraints	K36B_MLB 08/17/2008
74	105	FireWire Constraints	K36B_MLB 08/17/2008
75	106	SMC Constraints	K36B_MLB 08/17/2008
76	109	K36B RULE DEFINITIONS	K36B_MLB 08/17/2008

### Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7852	1	SCHEM, MLB, K36B	SCH	CRITICAL	
820-2496	1	PCBF, MLB, K36B	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
XX :	_____	DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX :	_____	ENG APPD	MFG APPD		
X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				051-7852	REV. A.0.1
				SHT 1 OF 76	

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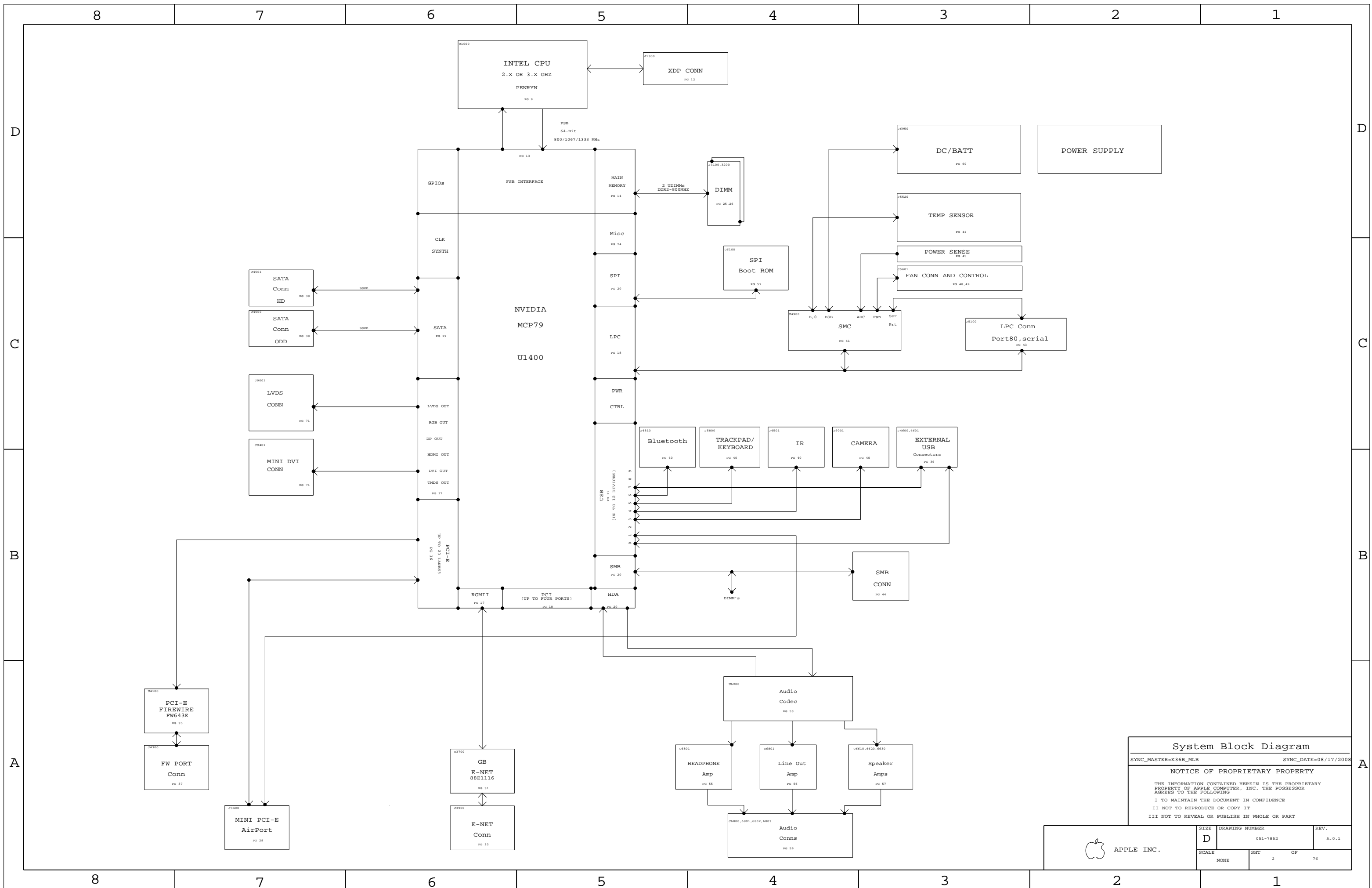
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**System Block Diagram**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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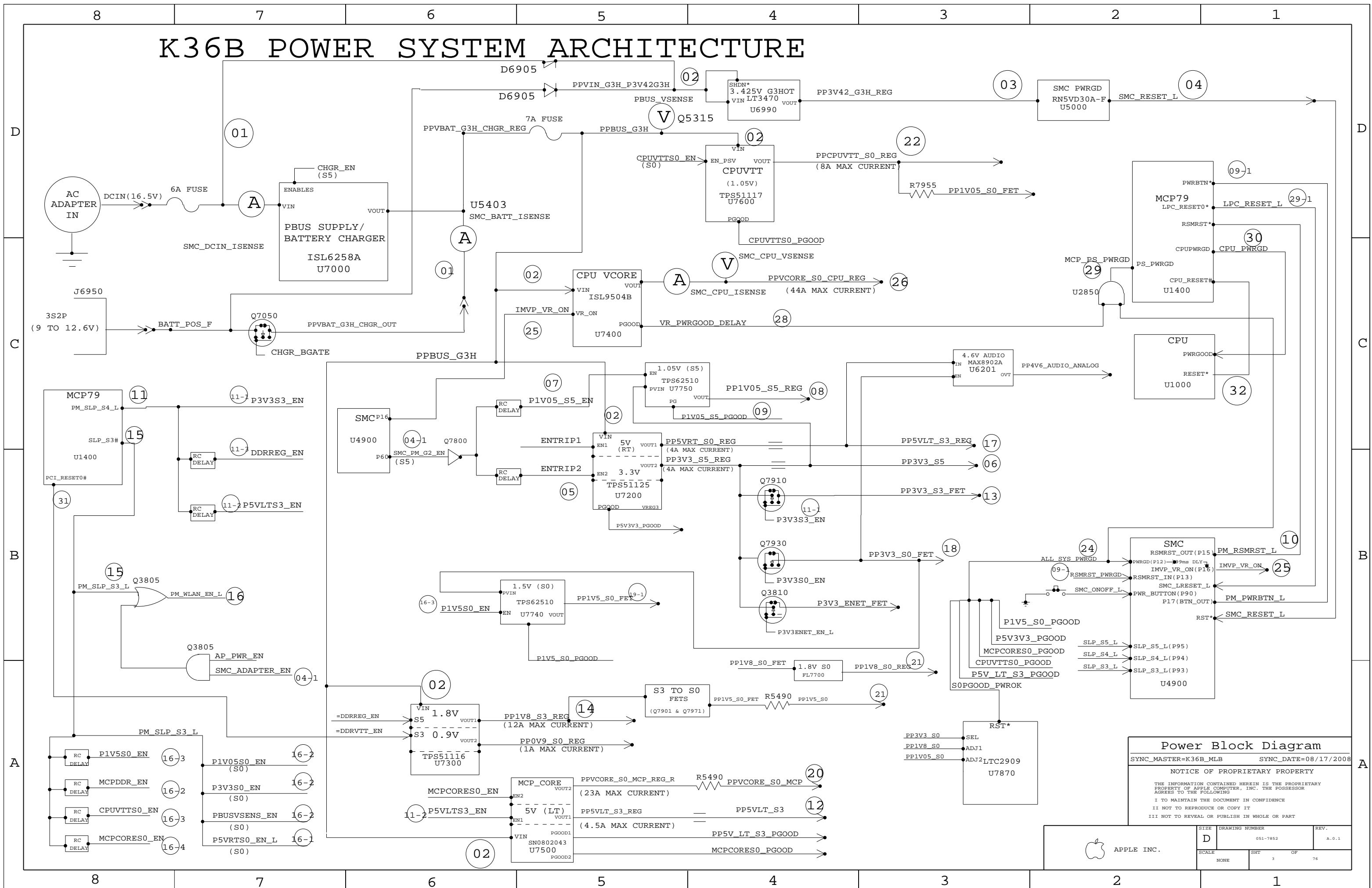
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	
NONE	2	76	

# K36B POWER SYSTEM ARCHITECTURE



**Power Block Diagram**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	3		

# Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

## BOM OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2420	1	IC, SMC, HSB/2117, 9X9MM, TLP, HF, BLANK	U4900	CRITICAL	SMC_PROG
341S2418	1	IC, FLASH, SPT, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_PROG
341S2093	1	IC, CYPRESS, CY7C63833	U4800	CRITICAL	
338S0654	1	IC, P8643N, 1394B PHY/ONCI LINK/PCI-E, 127	U4100	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	[EEE:3TN]	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3693	1	PC, SLG63, PRO, 2.00Hz, 25W, 1066, RD, 3M, BGA	U1000	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0702	1	IC, ONCE, MCP79, 35X35MM, BGA1437, B03	U1400	CRITICAL	

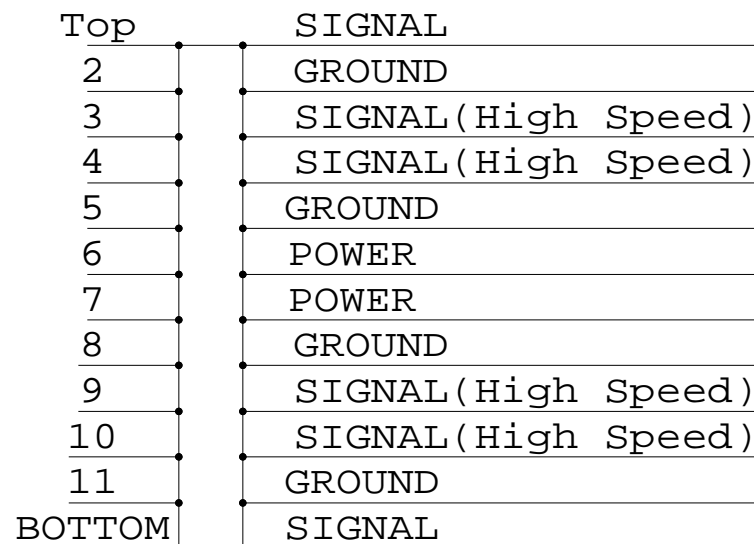
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0694	1	IC, RTL8251CA-VB-GR, GIGE TRANSDUCER, 4SP	U3700	CRITICAL	

## ALTERNATES OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0218		ALL	ALTERNATE PER CYNDI
152S0694	152S0138		ALL	ALTERNATE PER CYNDI
152S0847	152S0586		ALL	ALTERNATE PER CYNDI
152S0874	152S0516		ALL	ALTERNATE PER CYNDI
152S0796	152S0685		ALL	ALTERNATE PER CYNDI
152S0778	152S0693		ALL	ALTERNATE PER CYNDI
157S0058	157S0055		ALL	ALTERNATE PER CYNDI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0665	1	CONN, RCPT, MINI-DVI, 32P, R/A	J9401	CRITICAL	
514-0666	1	CONN, RCPT, 3.5MM AUDIO IN, R/A	J6750	CRITICAL	
514-0667	1	CONN, RCPT, 3.5MM AUDIO OUT, R/A	J6700	CRITICAL	
514-0668	1	CONN, RCPT, RJ45, NO FILTER, 8P	J3900	CRITICAL	
514-0669	1	CONN, RCPT, USB, 4P, MIDPLANE	J4600	CRITICAL	
514-0669	1	CONN, RCPT, USB, 4P, MIDPLANE	J4601	CRITICAL	

## BOARD STACK-UP AND CONSTRUCTION



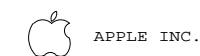
### CONFIGURATION OPTIONS

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	4	76

Revision History

\*\*\*\*\*2008/08/21\*\*\*\*\*
PAGE 61:
- U7500 PIN V5DRV1 LINK TO PP5V\_S0\_MCPREG\_VCC.
- U7500 PIN TONSEL LINK TO GND DIRECTLY.
PAGE 64:
- R7859 CHANGE TO 100 OHM.
- R7879 CHANGE TO 100K OHM.
PAGE 65:
- DELETE 1.05V S0 FET CIRCUIT.
PAGE 57:
- R7011 CHANGE TO 9.31K OHM, 1%
\*\*\*\*\*2008/08/22\*\*\*\*\*
PAGE 7:
- ADD SMC\_EXCARD\_PWR\_EN TEST\_POINT
PAGE 8:
- ADD =PP3V42\_G3H\_RTC\_D LINK TO =PP3V42\_G3H\_REG
PAGE 14:
- R1410 CHANGE TO 49.9 OHM
- CHANGE R1440 TO 150.5% AND NO STUFF
PAGE 26:
- R2872 CHANGE TO 0OHM
- RTC FOLLOW M97 DESIGN AND USE SUPERCAP SOLUTION
- MCP S0 PWRGD FOLLOW M97 DESIGN
PAGE 29:
- PULL R3240 DOWN TO GND. PULL R3241 HIGH
PAGE 32,33,34
- FOLLOW M97 DESIGN
PAGE 39:
- D4600/D4601/PIN-6 CONNECT TO USB VBUS (FOLLOW M97D)
PAGE 44:
- R5270/R5271 = 1K (FOLLOW M97D)
- R5280/R5281 = 1K (FOLLOW M97D)
PAGE 68:
- CHANGE C9411, C9412 TO 220PF
- CHANGE R9462, R9463 TO 2.7KOHM
- ADD C9480 0.1UF\_16V\_0402 FROM GND\_CHASSIS\_TMDS\_DOWN TO GND
- CHANGE R9460,R9461 TO 0OHM,
- CHANG C9442 AND C9443 TO 47PF
\*\*\*\*\*2008/08/23\*\*\*\*\*
MODIFY ALL NOSTUFF TO NO STUFF.
PAGE 6:
- REMOVE ETHERNET CIRCUIT.
PAGE 8:
- ADD =PP3V3\_S5\_P3V3ENETFET LINK TO PP3V3\_S5
- ADD =PP1V05\_ENET\_PHY LINK TO PP1V2R1V05\_ENET.
PAGE 9:
- ADD =RTL8211\_ENSWRE LINK TO GND.
- ADD =PP3V3\_ENET\_PHY\_VDDREG LINK TO TP\_PP3V3\_ENET\_PHY\_VDDREG.
- ADD =RTL8211\_REGOUT LINK TO NC\_RTL8211\_REGOUT.
- =P3V3ENET\_EN\_L LINK TO PM\_SLP\_RMG\_T\_L
- =P1V05ENET\_EN LINK TO PM\_SLP\_RMG\_T\_L
PAGE 10:
- CHANGE XDP\_TDO\_CONN TO XDP\_TDO
PAGE 13:
- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.
PAGE 23:
- DELETE R2400-R2413 FOR MCP A01 VERSION.
PAGE 31:
- REMOVE R3400, R3401
- L3401 FROM NO STUFF CHANGE TO STUFF.
PAGE 39
- DELETE R4699.
- R4690 FROM NO STUFF CHANGE TO STUFF.
PAGE 41:
- SMC\_NB\_DDR\_ISENSE CHANGE TO SMC\_MCP\_DDR\_ISENSE
- SMC\_NB\_CORE\_ISENSE CHANGE TO SMC\_MCP\_CORE\_ISENSE
PAGE 46:
- SMC\_NB\_DDR\_ISENSE CHANGE TO SMC\_MCP\_DDR\_ISENSE
- SMC\_NB\_CORE\_ISENSE CHANGE TO SMC\_MCP\_CORE\_ISENSE
- R5417 ADD BOM OPTION FOR NO STUFF
- R5416 ADD BOM OPTION FOR NO STUFF
PAGE 50:
- ADD C5926 (10UF,20%,0603) TO =PP3V3\_S3\_SMS
PAGE 63:
- REMOVE USB\_PWR\_EN\_S3
PAGE 66:
- REMOVE R9010, R9011
\*\*\*\*\*2008/08/24\*\*\*\*\*
PAGE 6:
- R0602 BOMOPTION FROM JTAG\_1DEV CHANGE TO NO STUFF.
PAGE 13:
- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.
PAGE 18:
- R1860 AND R1861 CHANGE TO PAGE 68.
PAGE 25:
- C2504-C2507 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
- C2516-C2517 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
PAGE 35:
- R4150 FROM 118S0343 (0201) CHANGE TO 116S0056(0402)
PAGE 58:
- C7281, C7241, C7272 FROM 138S0555(603) CHANGE TO 138S0615(603-1)
- C7280, C7240 FROM 128S0092(POLY) CHANGE TO 128S0128(POLY-TANT)
- C7291, C7292, C7252, C7251 FROM 128S0115(POLY,CASE-B2) CHANGE TO 128S0222(POLY,CASE-B2-SM)
- Q7260, Q7261 FROM 376S0512 CHANGE TO 376S0652 (H-F)
PAGE 59:
- Q7320 FROM 376S0512 CHANGE TO 376S0652 (H-F)
- Q7321 FROM 376S0511 CHANGE TO 376S0651 (H-F)
- C7321 FROM 128S0111(POLY) CHANGE TO 128S0218 (POLY,CASE-D2E-SM)
- C7343 FROM 128S0073 CHANGE TO 128S0233.
PAGE 60:
- XW7400 ADD BOMOPTION OMIT.
- Q7400, Q7402 FROM 376S0472 CHANGE TO 376S0617.
PAGE 61:
- L7500 FROM 152S0869 CHANGE TO 152S0685.
- Q7500 FROM 376S0512 CHANGE TO 376S0652.
- C7560 FROM 128S0092 CHANGE TO 128S0218.
PAGE 62:
- Q7620 FROM 376S0512 CHANGE TO 376S0652.
- C7601 FROM 138S0578 CHANGE TO 138S0614.

\*\*\*\*\*2008/08/25\*\*\*\*\*
CHANGE CSA BASE ON WILL'S SUGGESTION.
PAGE 9:
- ADD GMUX\_JTAG\_TMS AND GMUX\_JTAG\_TDI IN MISC NC MCP79 ALIASES.
PAGE 18:
- NETNAME ENET\_INTR\_L CHANGE TO TP\_ENET\_INTR\_L.
- ENET\_PWRDWN\_L CHANGE TO TP\_ENET\_PWRDWN\_L
PAGE 19:
- DELETE R1987,R1988,R1995,R1970,R1971,R1972,R1973,R1996,R1997,R1998,R1999,R1978,R1979
(FOLLOW M97 DESIGN).
- NET DPMUX\_LOWPWR\_L SYNC M97 NETNAME AUD\_IPHS\_SWITCH\_EN
- NET LVDSMUX\_SEL\_IG\_L SYNC M97 NETNAME
- NET DPMUX\_SEL\_IG\_L SYNC M97 NETNAME
PAGE 28:
- REMOVE NET DIMM\_OVERTEMPA\_L
PAGE 29:
- REMOVE NET DIMM\_OVERTEMPA\_L
PAGE 42:
- ADD SMC\_EXCARD\_PWR\_EN TO TP\_SMC\_EXCARD\_PWR\_EN
- ADD SMC\_RSTGATE\_L TO TP\_SMC\_RSTGATE\_L
- ADD ALS\_GAIN TO NC\_ALS\_GAIN
- ADD ESTARLDO\_EN TO NC\_ESTARLDO\_EN
- ADD SMC\_ANALOG\_ID TO NC\_SMC\_ANALOG\_ID
- ADD SMC\_SYS\_KBDLED TO NC\_SMC\_SYS\_KBDLED
- ADD R5054 10KOHM LINK SMC\_GPU\_ISENSE PULL DOWN TO GND.
- ADD R5055 10KOHM LINK SMC\_NB\_MISC\_ISENSE PULL DOWN TO GND.
PAGE 43:
- R5142 CHANGE TO NO STUFF.
PAGE 46:
- R5416 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5417 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.
PAGE 57:
- NETNAME FROM CHGR LOWCURRENT REF CHANGE TO CHGR\_LOWCURRENT\_REF
- NETNAME FROM CHGR LOWCURRENT GATE CHANGE TO CHGR\_LOWCURRENT\_GATE
PAGE :
- REMOVE R7884 AND C7884
PAGE 66:
- REMOVE J9001 PIN 20 AND PIN21 NET.
\*\*\*\*\*2008/09/02\*\*\*\*\*
PAGE 45:
- CHANGE ODD CONNECTOR FROM 516S0720 TO 516S0719
\*\*\*\*\*2008/09/27\*\*\*\*\*
PAGE 9:
- ADD STANDOFF 860-0964 X 4
- ADD STANDOFF 860-0723 X 1
- ADD STANDOFF 860-0749 X 1
PAGE 29:
- REMOVE BOMOPTION TABLE OF R2903/R2905/R2909/R2911
PAGE 66:
- C6601/C6603 CHANGE TO APN 128S0135, and REMOVE BOMOPTION OMIT
- C6605 CHANGE TO APN 128s0148, HF APN 128s0221, and REMOVE BOMOPTION OMIT
PAGE 68:
- C6830/C6831 CHANGE TO APN 128S0220, and REMOVE BOMOPTION OMIT
PAGE 72:
- R7272 CHANGE FROM 57.6K 1%(114s0389) TO 75K 1%(114s0399)
\*\*\*\*\*2008/10/20\*\*\*\*\*
PAGE 29:
- ADD R2903/R2905 BOMOTION AND CHANGE VALUE TO 200 OHM
PAGE 50:
- REMOVE ALT TABLE
PAGE 74:
- REMOVE ALT TABLE
PAGE 94:
- REMOVE K36 BOM OPTION TABLE AND ALT TABLE
\*\*\*\*\*2008/10/22\*\*\*\*\*
PAGE 12:
- C1200 - C1219 CHANGE TO 138S0580
PAGE 28:
- C2870 CHANGE TO 138S0614
PAGE 37:
- ADD R3731 (116s0026 22 ohm 5% 0402) FOR EMI 125MHZ NOISE
- TP\_RTL8211\_CLK125 CHANGE TO RTL8211\_CLK125
PAGE 48:
- C4803 CHANGE TO 138S0614
PAGE 66:
- C6605 CHANGE TO HF APN 128S0221
PAGE 70:
- C7040/C7041/C7047 CHANGE TO 138S0614
PAGE 90:
- L9002 CHANGE TO 116S0004(0ohm,5%,0402)
- C9003 CHANGE TO 116S0004(0ohm,5%,0402)
\*\*\*\*\*2008/10/24\*\*\*\*\*
PAGE 19:
- R1950/R1951/R1952/1953 CHANGE TO 116s0004 (0 OHM,5%,0402)
PAGE 28:
- R2825/R2826 CHANGE TO 116s0004 (0 OHM,5%,0402)
PAGE 34:
- J3400 516S0635 CHANGE TO HF APN 516S0729
PAGE 52:
- ADD C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281 131S1104 (22pF,5%,0402) NO STUFF
- TEXT "ALS" CHANGE TO "MINI-PCIE"
- I2C\_ALS\_SCL CHANGE TO I2C\_MINI\_PCIE\_SCL
- I2C\_ALS\_SDA CHANGE TO I2C\_MINI\_PCIE\_SDA
PAGE 67:
- J6700 514-0604 CHANGE TO HF APN 514-0521
- J6750 514-0603 CHANGE TO HF APN 514-0519
PAGE 69:
- J6950 516S0620 CHANGE TO HF APN 516S0735
\*\*\*\*\*2008/10/25\*\*\*\*\*
PAGE 52:
- STUFF C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281
\*\*\*\*\*2008/10/28\*\*\*\*\*
PAGE 34:
- J3400 516S0729 CHANGE TO 516S0635
\*\*\*\*\*2008/10/30\*\*\*\*\*
PAGE 69:
- J6950 516S0735 CHANGE TO 516S0620

\*\*\*\*\*2008/10/31\*\*\*\*\*
PAGE 41:
- U4100 CHANGE FROM 338S0523 TO 338S0654
\*\*\*\*\*2008/11/01\*\*\*\*\*
PAGE 4:
- BOM change U1400 CHANGE FROM 338S0678 TO 338S0702
\*\*\*\*\*2008/11/05\*\*\*\*\*
PAGE 62:
- C6210 CHANGE FROM 127S0062 TO 127S0108
PAGE 68:
- C6832, C6833 CHANGE FROM 127S0062 TO 127S0108
PAGE 45:
- DELETE L4502, NET SATA\_HDD\_D2R\_UF\_P / SATA\_HDD\_D2R\_UF\_N
- L4501 / F14520 / FL4525 CHANGE FROM 155S0303 TO 155S0371
PAGE 102:
- DELETE PHYSICAL/SPACING SETTING OF SATA\_HDD\_D2R\_UF\_P / SATA\_HDD\_D2R\_UF\_N
\*\*\*\*\*2008/11/06\*\*\*\*\*
- U5413 CHANGE FROM 353S1432 TO 353S2220
- R7417 CHANGE FROM 5.36K(114S0289) TO 4.42K(114S0280)
\*\*\*\*\*2008/11/12\*\*\*\*\*
- U1000 CHANGE FROM 373S3646 TO 373S3702
\*\*\*\*\*2008/11/19\*\*\*\*\*
- J6950 CHANGE FROM 516S0620 TO 516S0735
- J9401 CHANGE FROM 514-0517 TO 514-0665
- J6750 CHANGE FROM 514-0519 TO 514-0666
- J6700 CHANGE FROM 514-0521 TO 514-0667
- J3900 CHANGE FROM 514-0523 TO 514-0668
- J4600, J4601 CHANGE FROM 514-0527 TO 514-0669
- U3700 CHANGE FROM 338S0570 TO 338S0694
\*\*\*\*\*2008/11/26\*\*\*\*\*
- PAGE 61 NOTE : CORRECT REFERENCE TO R5164 AND R5144
- J3400 CHANGE TO 516S0729
\*\*\*\*\*2008/12/12\*\*\*\*\*
- R5144 and R5164 changed to 10K 5% 0402 (116S0090)
\*\*\*\*\*2008/12/17\*\*\*\*\*
- U4900 symbol update
\*\*\*\*\*2008/12/20\*\*\*\*\*
- R5156, R5157, R5158 change from 0 to 33 ohm, 5%, 0402(116s0030)
\*\*\*\*\*2008/12/23\*\*\*\*\*
- U1000 change to 337S3693 in csa page4

D

C

B

A

D

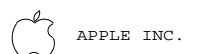
C

B

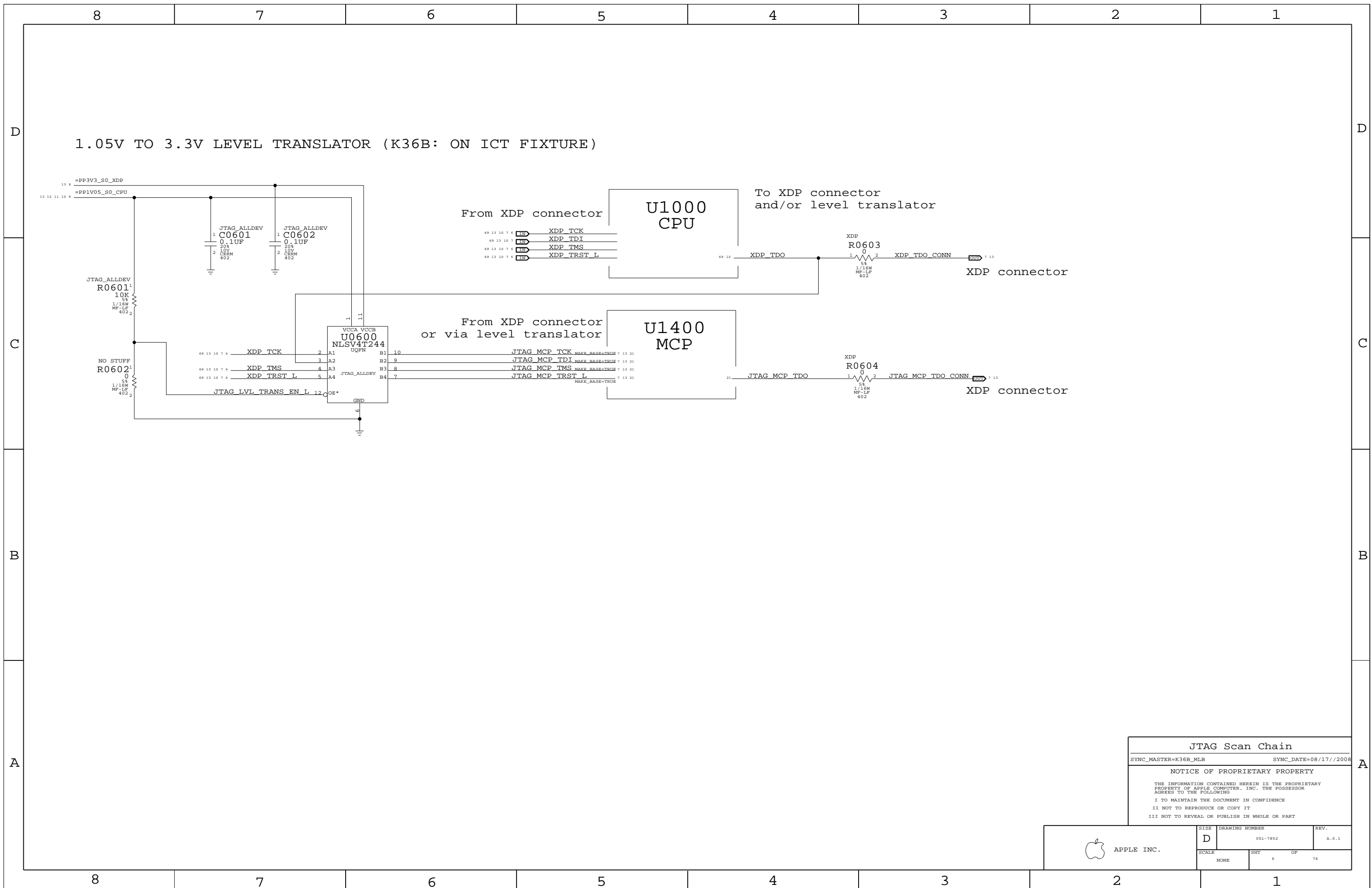
A

Revision History
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Table with columns: SCALE, SHEET, OF, DRAWING NUMBER, REV. Values: NONE, 5, 76, D, 051-7852, A.0.1



NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.



1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)

From XDP connector **U1000 CPU** To XDP connector and/or level translator

From XDP connector or via level translator **U1400 MCP**

**JTAG Scan Chain**  
 SYNC\_MASTER=K36H\_MLB SYNC\_DATE=08/17//2008  
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	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	6		

# Functional Test Points

## #J5601 Fan Connectors

#J5601 TRUE PP5VRT\_S0 7 8  
 #J5601 TRUE FAN\_RT\_PWM 48  
 #J5601 TRUE FAN\_RT\_TACH 48  
 #J5601 TRUE GND

## #J6950 Battery/Lid Connector

#J6950 TRUE SMC\_BS\_ALERT\_L\_F 56  
 #J6950 TRUE SMBUS\_BATT\_SCL\_F 56  
 #J6950 TRUE SMBUS\_BATT\_SDA\_F 56  
 #J6950 TRUE PPVBAT\_G3H\_CONN\_F 56  
 #J6950 TRUE SMC\_LID\_F 56  
 #J6950 TRUE GND\_SMC\_LID\_F 56  
 #J6950 TRUE PP3V42\_G3H\_LIDSWITCH\_F 56  
 #J6950 TRUE GND Need 6 TP

## #J6900 MagSafe DC Power Jack

#J6900 TRUE PP18V5\_DCN\_FUSE Need 2 TP 56  
 #J6900 TRUE ADAPTER\_SENSE 56  
 #J6900 TRUE GND Need 2 TP

## #J9000 INVERTER Connector

#J9000 TRUE PPBUS\_ALL\_INV\_CONN Need 2 TP 66  
 #J9000 TRUE INV\_GND 66  
 #J9000 TRUE PP5V\_INV\_F 66  
 #J9000 TRUE INV\_BKLIGHT\_PWM\_L Need 4 TP 66

## #J9001 LCD + CAMERA CONNECTOR

#J9001 TRUE PP3V3\_LCDVDD\_SW\_F 66  
 #J9001 TRUE PP3V3\_S0\_LCD\_F 66  
 #J9001 TRUE LVDS\_IG\_DDC\_CLK 18 66  
 #J9001 TRUE LVDS\_IG\_DDC\_DATA 18 66  
 #J9001 TRUE LVDS\_IG\_A\_DATA\_N<0> 18 66 71  
 #J9001 TRUE LVDS\_IG\_A\_DATA\_P<0> 18 66 71  
 #J9001 TRUE LVDS\_IG\_A\_DATA\_N<1> 18 66 71  
 #J9001 TRUE LVDS\_IG\_A\_DATA\_P<1> 18 66 71  
 #J9001 TRUE LVDS\_IG\_A\_DATA\_N<2> 18 66 71  
 #J9001 TRUE LVDS\_IG\_A\_DATA\_P<2> 18 66 71  
 #J9001 TRUE LVDS\_IG\_A\_CLK\_F\_N 66  
 #J9001 TRUE LVDS\_IG\_A\_CLK\_F\_P 66  
 #J9001 TRUE USB2\_CAMERA\_CONN\_P 66 72  
 #J9001 TRUE USB2\_CAMERA\_CONN\_N 66 72  
 #J9001 TRUE PP5V\_S3\_CAMERA\_F 66  
 #J9001 TRUE GND

## # J6701 MIC CONNECTOR

#J6701 TRUE MIC\_LO\_CONN 54  
 #J6701 TRUE MIC\_HI\_CONN 54  
 #J6701 TRUE MIC\_SHLD\_CONN 54 55

## #J6702 Left SPEAKER CONNECTOR

#J6702 TRUE SPKRCONN\_L\_P\_OUT 53 54  
 #J6702 TRUE SPKRCONN\_L\_N\_OUT 53 54

## #J6703 Right SUB SPEAKER CONNECTOR

#J6703 TRUE SPKRCONN\_SUB\_P\_OUT 53 54  
 #J6703 TRUE SPKRCONN\_SUB\_N\_OUT 53 54  
 #J6703 TRUE SPKRCONN\_R\_P\_OUT 53 54  
 #J6703 TRUE SPKRCONN\_R\_N\_OUT 53 54

## # J5800 GEYSER AND DIMMO REMOTE TEMP SENSORS

#J5800 TRUE TPAD\_GND\_F 49  
 #J5800 TRUE CONN\_TPAD\_ONOFF\_FLTR\_L 49  
 #J5800 TRUE CONN\_TPAD\_USB\_P 49 72  
 #J5800 TRUE CONN\_TPAD\_USB\_N 49 72  
 #J5800 TRUE SMC\_LID\_LC 49  
 #J5800 TRUE PP5V\_S3\_TPAD\_F 49

## #J5520 CPU/MCP Thermal Sensor

#J5520 TRUE CPUTHSNS\_D2\_P 47  
 #J5520 TRUE CPUTHSNS\_D2\_N 47  
 #J5520 TRUE MCPTHMSNS\_D2\_P 47  
 #J5520 TRUE MCPTHMSNS\_D2\_N 47

## #J4810 BLUETOOTH

#J4810 TRUE PP3V3\_S3\_BT\_F\_CONN 40  
 #J4810 TRUE USB2\_BT\_F\_N\_CONN 40 72  
 #J4810 TRUE USB2\_BT\_F\_P\_CONN 40 72  
 #J4810 TRUE GND\_BT\_F\_CONN 40

## #J4500 SATA ODD

#J4500 TRUE SATA\_ODD\_R2D\_UF\_P 38 71  
 #J4500 TRUE SATA\_ODD\_R2D\_UF\_N 38 71  
 #J4500 TRUE SATA\_ODD\_D2R\_C\_N 38 71  
 #J4500 TRUE SATA\_ODD\_D2R\_C\_P 38 71  
 #J4500 TRUE PP3V3\_S0 Need 4 TP 7 8  
 #J4500 TRUE SMC\_ODD\_DETECT 38 41  
 #J4500 TRUE GND Need 6 TP

## # J4501 SATA HD System LED and IR

#J4501 TRUE SATA\_HDD\_R2D\_P 38 71  
 #J4501 TRUE SATA\_HDD\_R2D\_N 38 71  
 #J4501 TRUE SATA\_HDD\_D2R\_C\_N 38 71  
 #J4501 TRUE SATA\_HDD\_D2R\_C\_P 38 71  
 #J4501 TRUE PP5V\_S0\_HDD\_FLT Need 4 TP 38  
 #J4501 TRUE SYS\_LED\_ANODE\_L 38  
 #J4501 TRUE IR\_RX\_OUT 38 40  
 #J4501 TRUE PP5V\_S3\_IR\_CONN 38  
 #J4501 TRUE GND Need 4 TP

## #J3400 Airport

#J3400 TRUE PCIE\_WAKE\_L 17 31  
 #J3400 TRUE MINI\_CLKREQ\_L 17 31  
 #J3400 TRUE PCIE\_CLK100M\_MINI\_N 17 31 71  
 #J3400 TRUE PCIE\_CLK100M\_MINI\_P 17 31 71  
 #J3400 TRUE PCIE\_MINI\_D2R\_N 17 31 71  
 #J3400 TRUE PCIE\_MINI\_D2R\_P 17 31 71  
 #J3400 TRUE PCIE\_MINI\_R2D\_N 31 71  
 #J3400 TRUE PCIE\_MINI\_R2D\_P 31 71  
 #J3400 TRUE PP3V3\_WLAN Need 4 TP 31  
 #J3400 TRUE PP1V5\_S0\_R Need 3 TP 7 8  
 #J3400 TRUE MINI\_RESET 31  
 #J3400 TRUE PP3V3\_S3\_AIRPORT\_CONN 31  
 #J3400 TRUE I2C\_MINI\_PCIE\_SCL 31 44  
 #J3400 TRUE I2C\_MINI\_PCIE\_SDA 31 44  
 #J3400 TRUE USB2\_AIRPORT\_N 31 72  
 #J3400 TRUE USB2\_AIRPORT\_P 31 72  
 #J3400 TRUE GND Need 6 TP

## # Other Func Test Points

#Other TRUE ALL\_SYS\_PMRGD 26 41 44  
 #Other TRUE PPVCORE\_S0\_CPU 8  
 #Other TRUE PPCPUVTT\_S0 7 8  
 #Other TRUE PPVCORE\_S0\_MCP\_R 8  
 #Other TRUE PPVCORE\_S0\_MCP 8  
 #Other TRUE PP0V9\_S0 8  
 #Other TRUE PP1V05\_S0 7 8  
 #Other TRUE PP1V5\_S0\_R 7 8  
 #Other TRUE PP1V8\_S0 8  
 #Other TRUE PP1V8\_S0\_R 8  
 #Other TRUE PP1V05\_S0\_MCP\_PEX\_AVDD 8 24  
 #Other TRUE PP1V05\_S0 7 8  
 #Other TRUE PP1V05\_S0\_MCP\_SATA\_AVDD 8 24  
 #Other TRUE PP1V05\_S0 7 8  
 #Other TRUE PP5VRT\_S0 7 8  
 #Other TRUE PP3V3\_S0 7 8  
 #Other TRUE PP1V0\_FW 8  
 #Other TRUE PP1V8\_S3 8  
 #Other TRUE PP3V3\_S3 8  
 #Other TRUE PP5VLT\_S3 8  
 #Other TRUE PPVTT\_S3\_DDR\_BUF 8  
 #Other TRUE PP1V05\_S5\_REG 8  
 #Other TRUE PP3V3\_S5 8  
 #Other TRUE PP3V42\_G3H 7 8  
 #Other TRUE PP18V5\_G3H 8  
 #Other TRUE PPBUS\_G3H 8  
 #Other TRUE PPBUS\_G3H\_CPU\_ISNS 8  
 #Other TRUE PP3V3\_ENET\_PHY 8  
 #Other TRUE PP1V2R1V05\_ENET 8  
 #Other TRUE PPVP\_FW 8

## #J1300 XDP

#J1300 TRUE XDP\_BPM\_L<5> 10 13 69  
 #J1300 TRUE XDP\_BPM\_L<4> 10 13 69  
 #J1300 TRUE XDP\_BPM\_L<3> 10 13 69  
 #J1300 TRUE XDP\_BPM\_L<2> 10 13 69  
 #J1300 TRUE XDP\_BPM\_L<1> 10 13 69  
 #J1300 TRUE XDP\_BPM\_L<0> 10 13 69  
 #J1300 TRUE TP\_XDP\_OBSFN\_B0 13  
 #J1300 TRUE TP\_XDP\_OBSFN\_B1 13  
 #J1300 TRUE TP\_XDP\_OBSDATA\_B0 13  
 #J1300 TRUE TP\_XDP\_OBSDATA\_B1 13  
 #J1300 TRUE TP\_XDP\_OBSDATA\_B2 13  
 #J1300 TRUE TP\_XDP\_OBSDATA\_B3 13  
 #J1300 TRUE XDP\_PWRGD 13  
 #J1300 TRUE XDP\_OBS20 13  
 #J1300 TRUE PM\_LATRIGGER\_L 13 19  
 #J1300 TRUE JTAG\_MCP\_TCK 6 13 21  
 #J1300 TRUE SMBUS\_MCP\_0\_DATA 13 21 44 72  
 #J1300 TRUE SMBUS\_MCP\_0\_CLK 13 21 44 72  
 #J1300 TRUE XDP\_TCK 6 10 13 69  
 #J1300 TRUE PPCPUVTT\_S0 7 8  
 #J1300 TRUE PP3V3\_S0 7 8  
 #J1300 TRUE JTAG\_MCP\_TDO\_CONN 6 13  
 #J1300 TRUE JTAG\_MCP\_TRST\_L 6 13 21  
 #J1300 TRUE MCP\_DEBUG<0> 13 19 72  
 #J1300 TRUE MCP\_DEBUG<1> 13 19 72  
 #J1300 TRUE MCP\_DEBUG<2> 13 19 72  
 #J1300 TRUE MCP\_DEBUG<3> 13 19 72  
 #J1300 TRUE JTAG\_MCP\_TDI 6 13 21  
 #J1300 TRUE JTAG\_MCP\_TMS 6 13 21  
 #J1300 TRUE MCP\_DEBUG<4> 13 19 72  
 #J1300 TRUE MCP\_DEBUG<5> 13 19 72  
 #J1300 TRUE MCP\_DEBUG<6> 13 19 72  
 #J1300 TRUE MCP\_DEBUG<7> 13 19 72  
 #J1300 TRUE FSB\_CLK\_ITP\_P 13 14 69  
 #J1300 TRUE FSB\_CLK\_ITP\_N 13 14 69  
 #J1300 TRUE XDP\_CPURST\_L 13 69  
 #J1300 TRUE XDP\_DBRESET\_L 10 13 26  
 #J1300 TRUE XDP\_TDO\_CONN 6 13  
 #J1300 TRUE XDP\_TRST\_L 6 10 13 69  
 #J1300 TRUE XDP\_TDI 6 10 13 69  
 #J1300 TRUE XDP\_TMS 6 10 13 69  
 #J1300 TRUE GND Need 8 TP

## # J5100 LPC+SPI Connector

#J5100 TRUE PP3V42\_G3H 7 8  
 #J5100 TRUE PP5VRT\_S0 7 8  
 #J5100 TRUE LPC\_AD<0> 19 41 43 72  
 #J5100 TRUE LPC\_AD<1> 19 41 43 72  
 #J5100 TRUE SPI\_ALT\_MOSI 43  
 #J5100 TRUE SPI\_ALT\_MISO 43  
 #J5100 TRUE LPC\_FRAME\_L 19 41 43 72  
 #J5100 TRUE PM\_CLKRUN\_L 19 41 43  
 #J5100 TRUE SMC\_TMS 41 42 43  
 #J5100 TRUE DEBUG\_RESET\_L 26 43  
 #J5100 TRUE SMC\_TDO 41 42 43  
 #J5100 TRUE SMC\_TRST\_L 41 43  
 #J5100 TRUE SMC\_MD1 41 43  
 #J5100 TRUE SMC\_TX\_L 39 41 42 43  
 #J5100 TRUE LPC\_CLK33M\_LPCPLUS 26 43 72  
 #J5100 TRUE LPC\_AD<2> 19 41 43 72  
 #J5100 TRUE LPC\_AD<3> 19 41 43 72  
 #J5100 TRUE SPIROM\_USE\_MLB 43  
 #J5100 TRUE SPI\_ALT\_CLK 43  
 #J5100 TRUE SPI\_ALT\_CS\_L 43  
 #J5100 TRUE LPC\_SERIRQ 19 41 43  
 #J5100 TRUE LPC\_PWRDWN\_L 19 41 43  
 #J5100 TRUE SMC\_TDI 41 42 43  
 #J5100 TRUE SMC\_TCK 41 42 43  
 #J5100 TRUE SMC\_RESET\_L 41 42 43  
 #J5100 TRUE SMC\_NMI 41 43  
 #J5100 TRUE SMC\_RX\_L 39 41 42 43  
 #J5100 TRUE LPCPLUS\_GPIO 18 43  
 #J5100 TRUE GND Need 2 TP

## FUNC TEST

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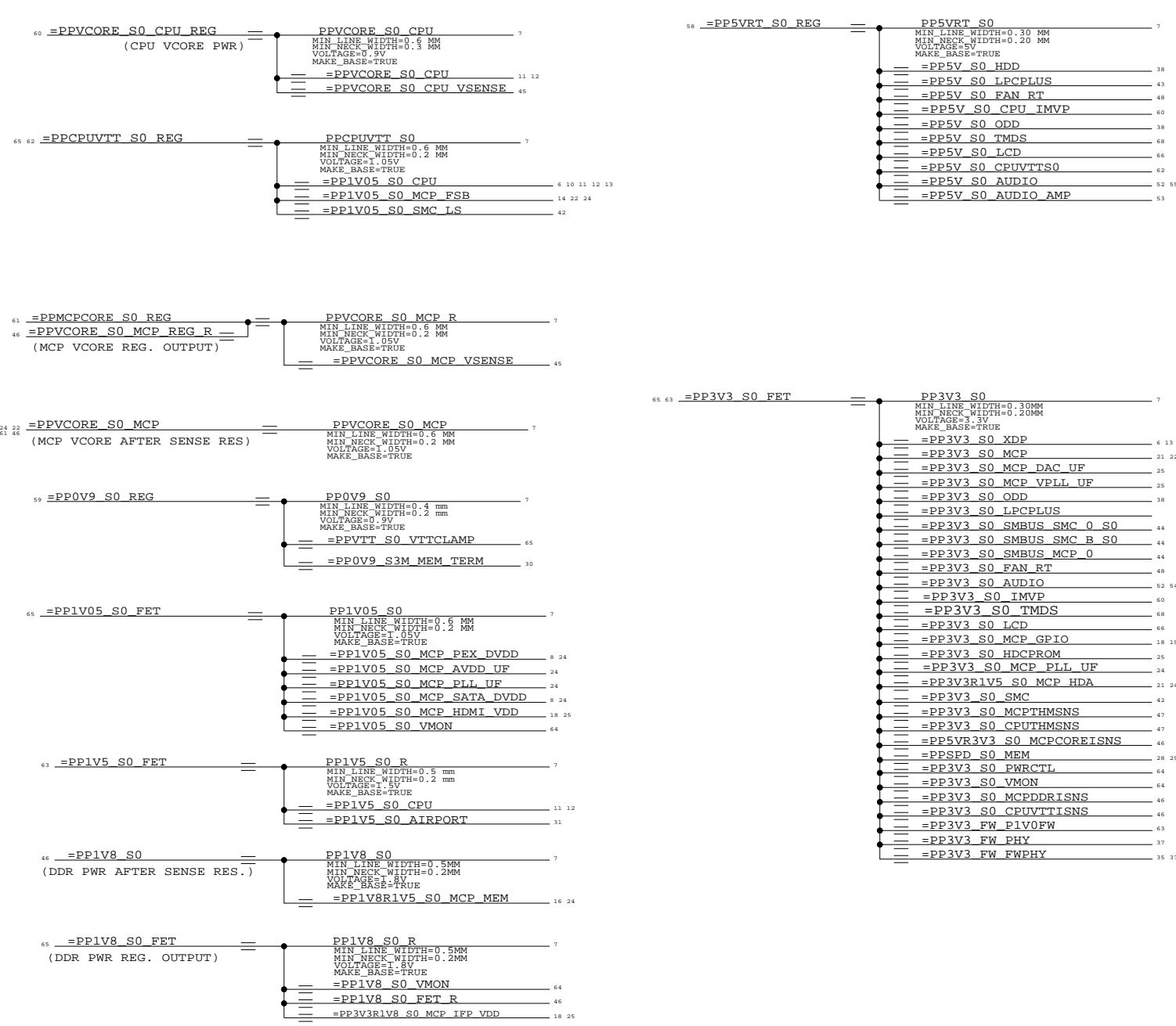
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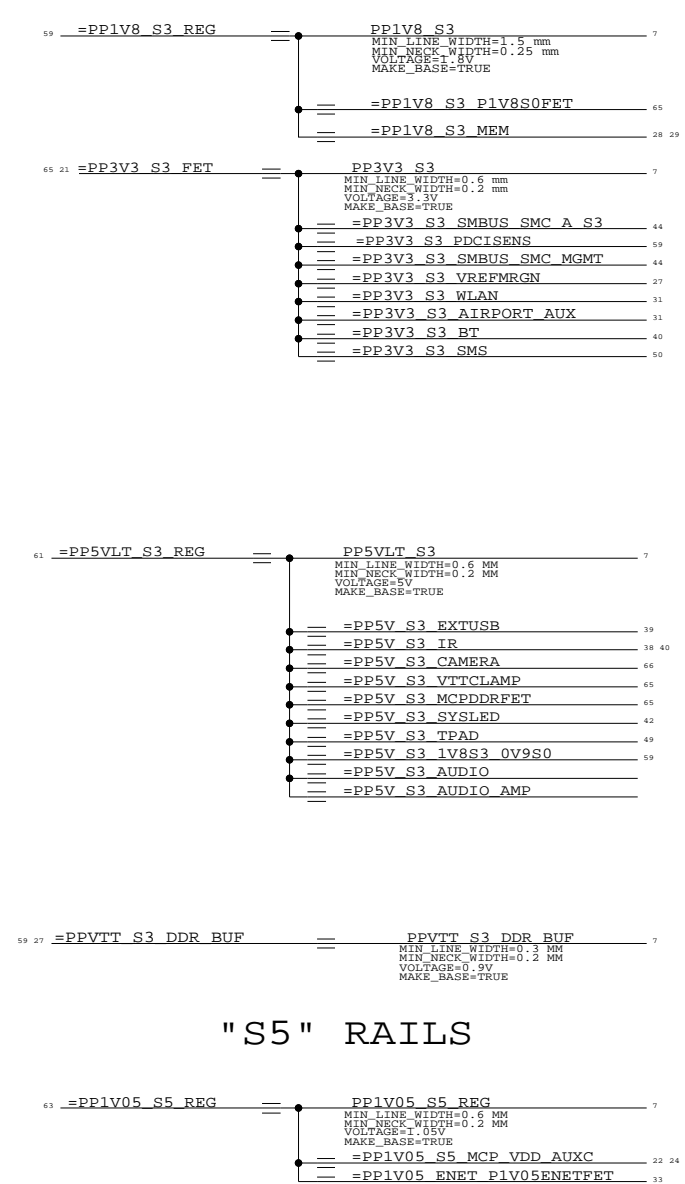
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	7	76

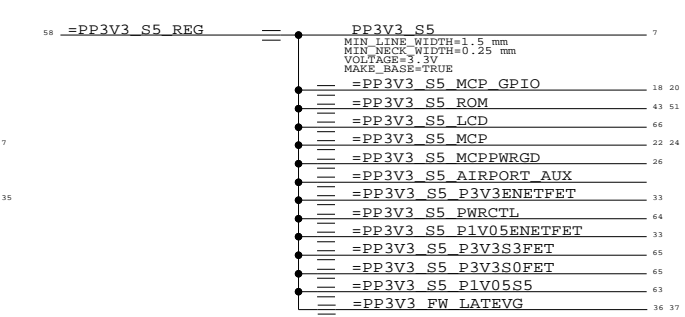
## "S0,S0M" RAILS



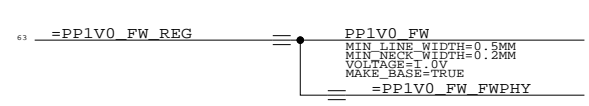
## "S3" RAILS



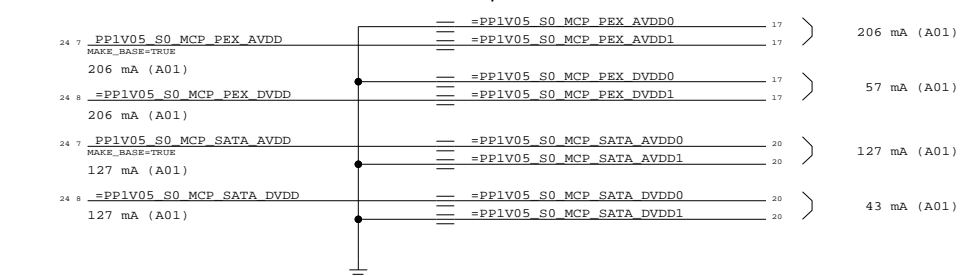
## "S5" RAILS



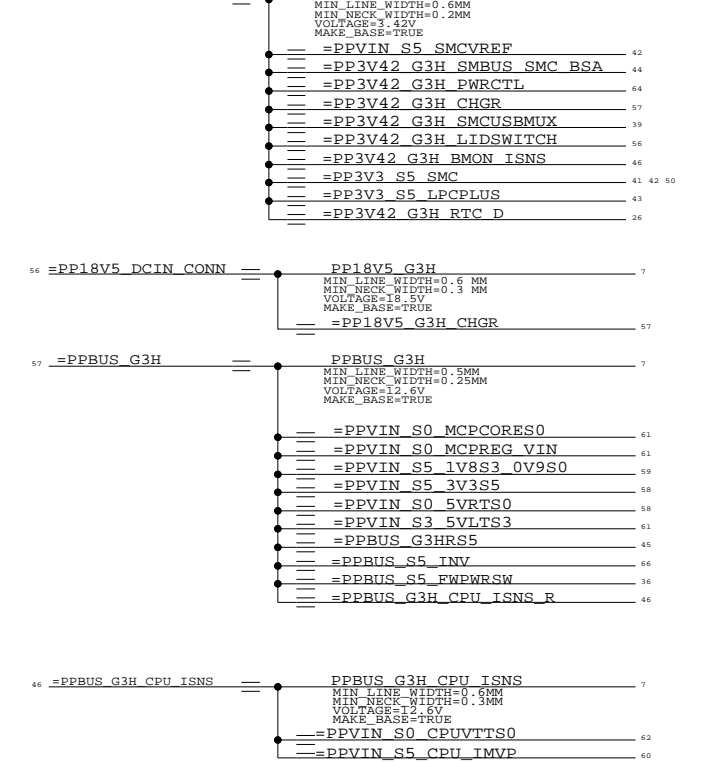
## "FW" RAILS



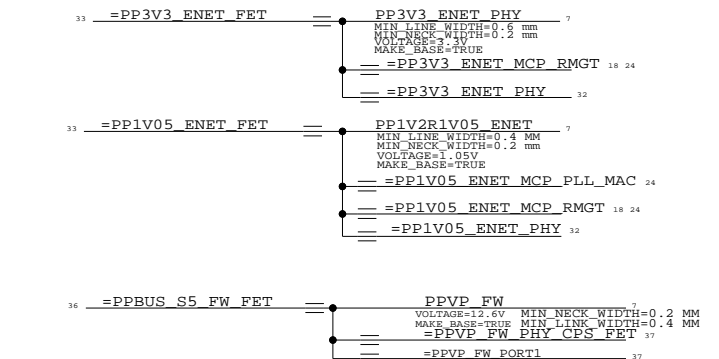
## PEX & SATA AVDD/DVDD aliases



## "G3H" RAILS



## "ENET" RAILS



## Power Aliases

SYNC\_MASTER=K36B\_MLB

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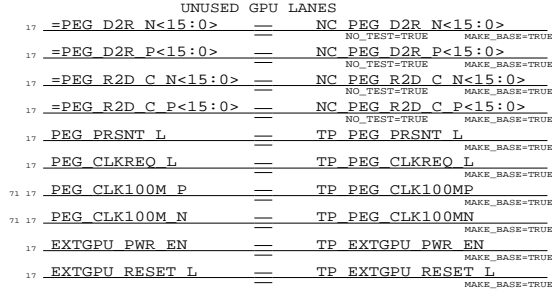
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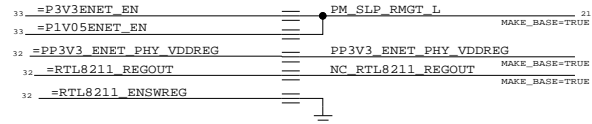
APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	76
NONE	8		



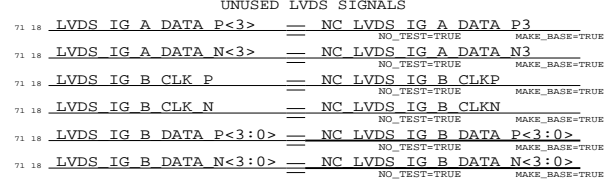
### PCI-E ALIASES



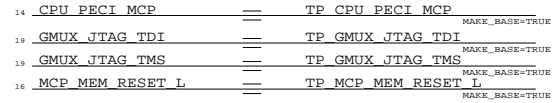
### ETHERNET ALIASES



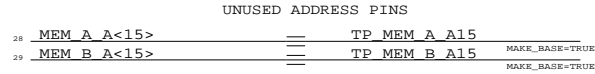
### LVDS ALIASES



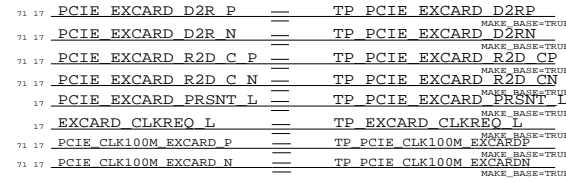
### MISC NC MCP79 ALIASES



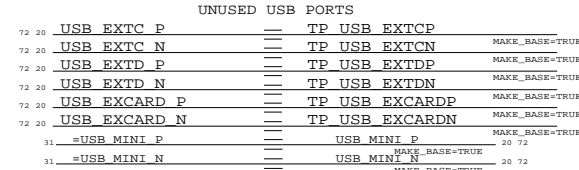
### SO-DIMM ALIASES



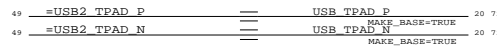
### UNUSED EXPRESS CARD LANE



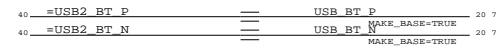
### USB ALIASES



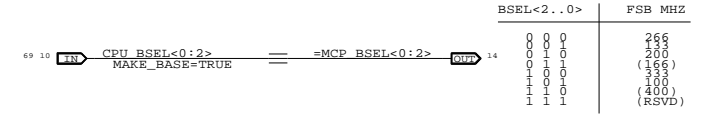
### TRACKPAD (WELLSPRING)



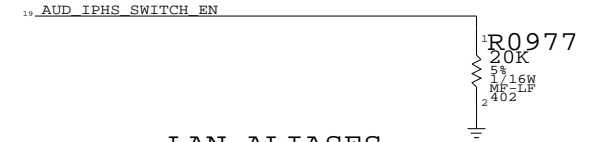
### BLUETOOTH



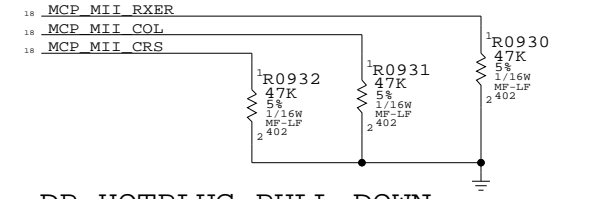
### CPU FSB FREQUENCY STRAPS



### HDA PULL-DOWN



### LAN ALIASES



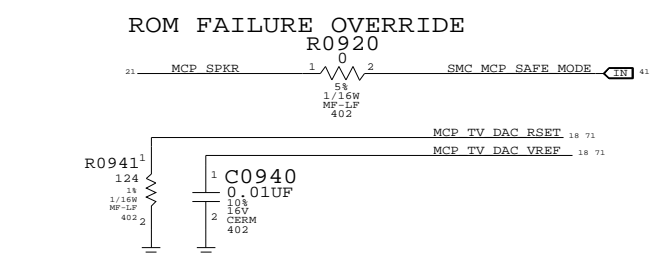
### DP HOTPLUG PULL-DOWN



### FW PULL-DOWN

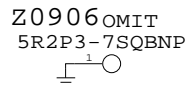


### MCP\_SAFE\_MODE SIGNAL TO SUPPORT

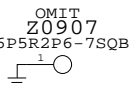


### Screw Holes

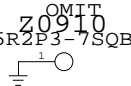
BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND



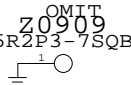
SATA,LVDS CONNECTOR CHASSIS GND



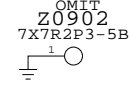
DIP DIMM CONNECTOR CHASSIS GND



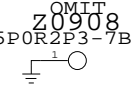
DIP DIMM CONNECTOR CHASSIS GND



DCIN CONNECTOR CHASSIS GND

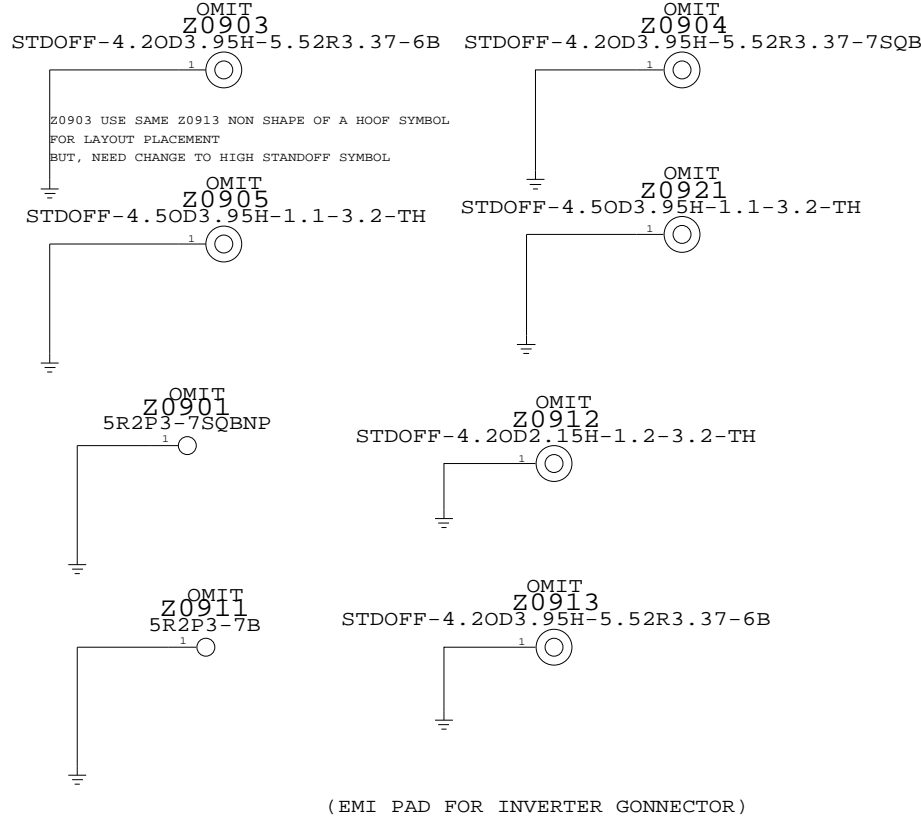


I/O CONNECTOR CHASSIS GND

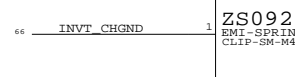


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
860-0964	4	THERMAL STANDOFF	Z0903,Z0904,Z0905,Z0921	?	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0912	?	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0913	?	STANDOFF

### CPU HEATSINK STANDOFF SCREW HOLE



(EMI PAD FOR INVERTER GONNECTOR)



### SIGNAL ALIAS

SYNC\_MASTER=K36B\_MLB

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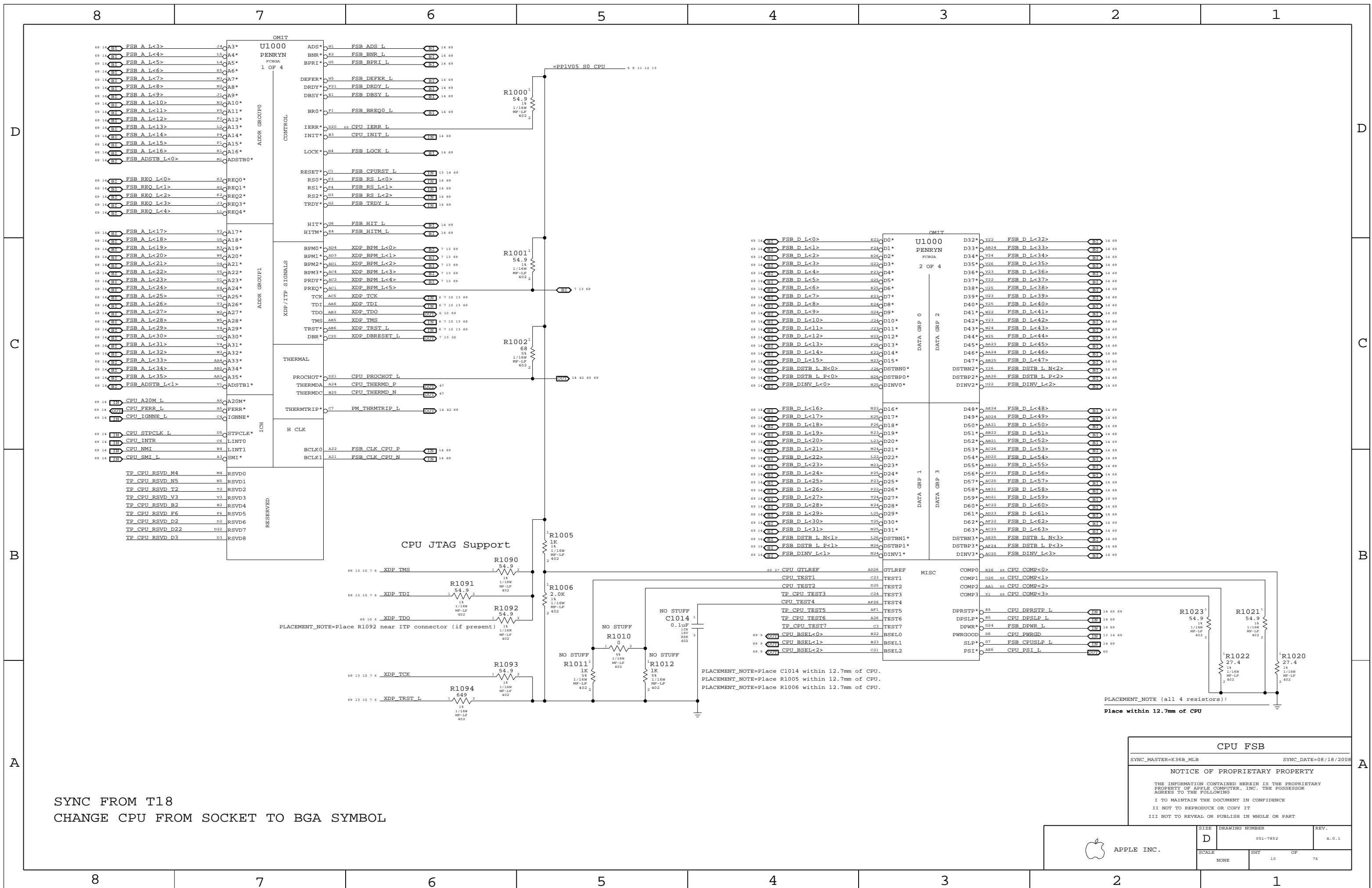
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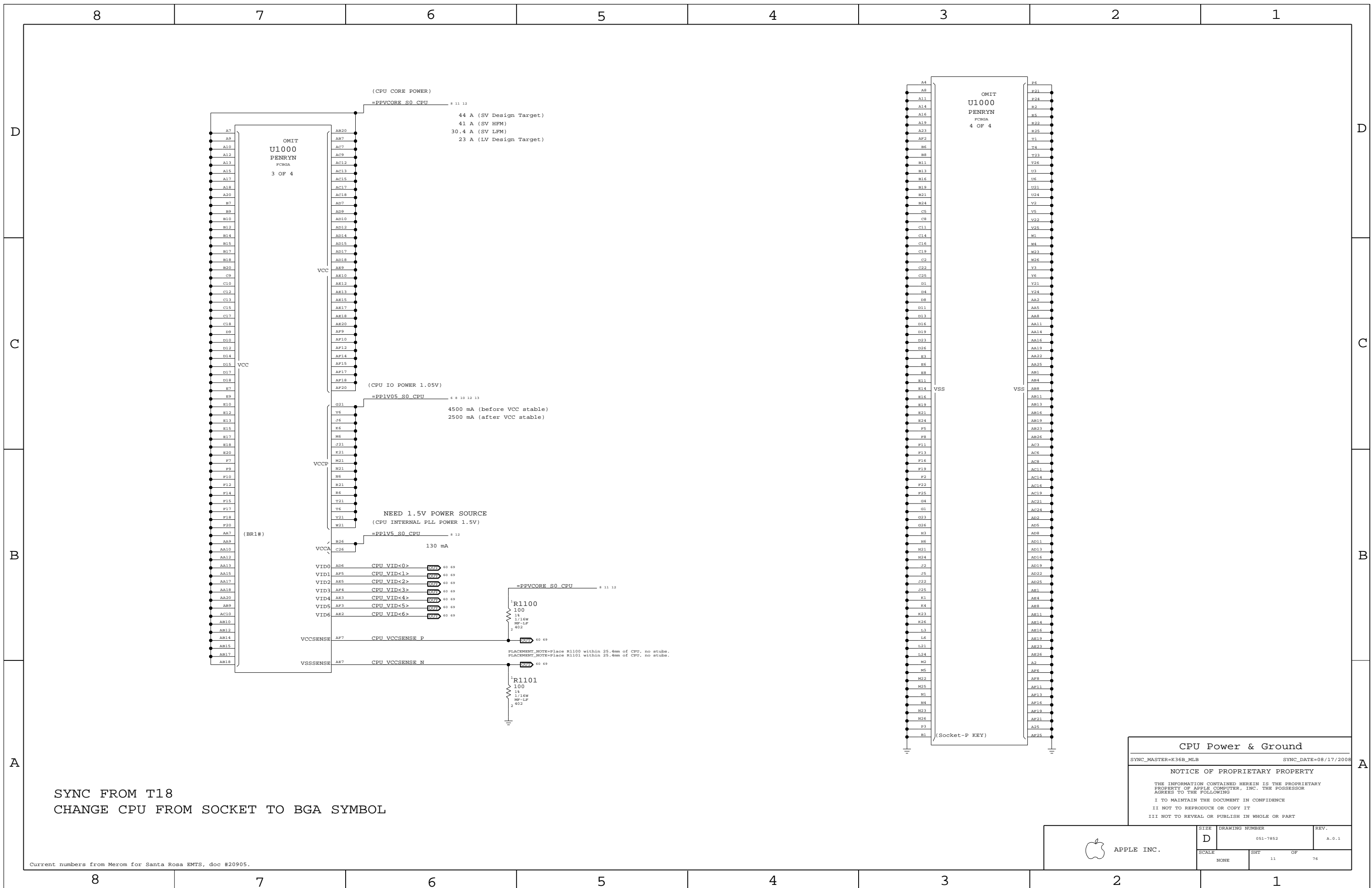
SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	9	76



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

**CPU FSB**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/18/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHEET		OF
NONE	10		76



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

**CPU Power & Ground**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	11		

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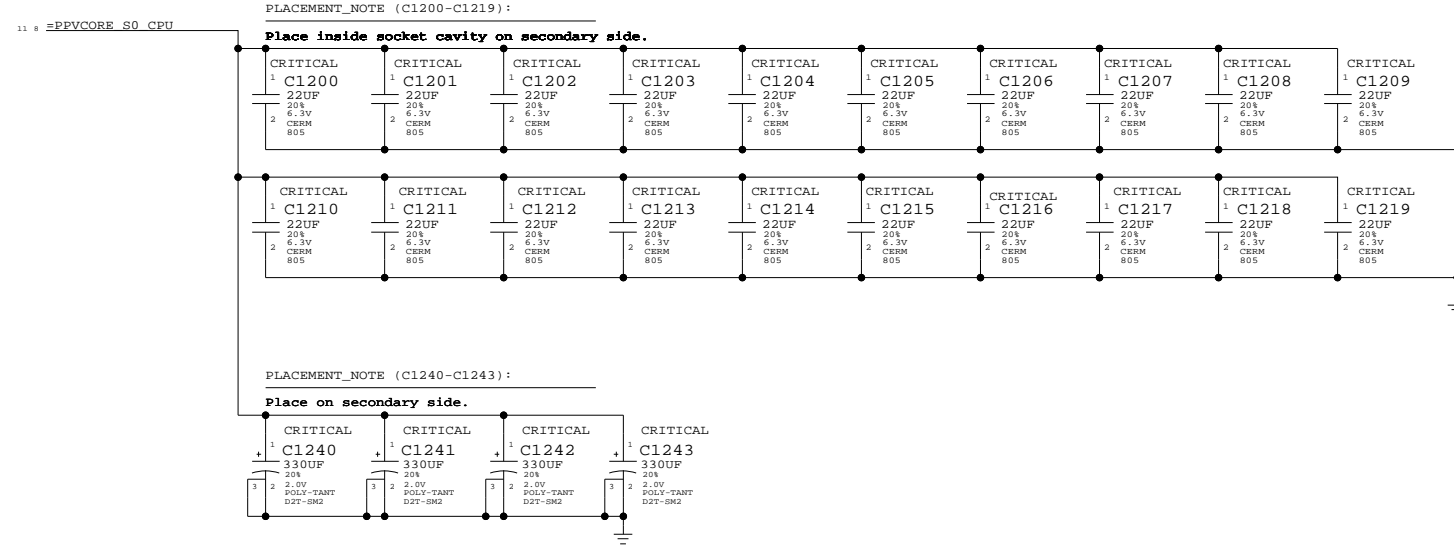
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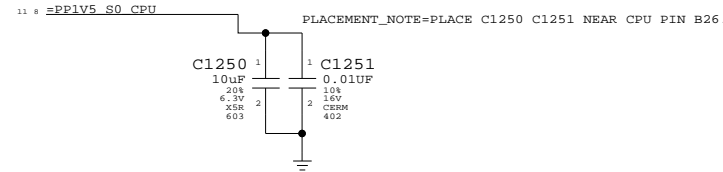
### CPU VCore HF and Bulk Decoupling

6x 330uF, 32x 22uF 0805 (20 stuffed)



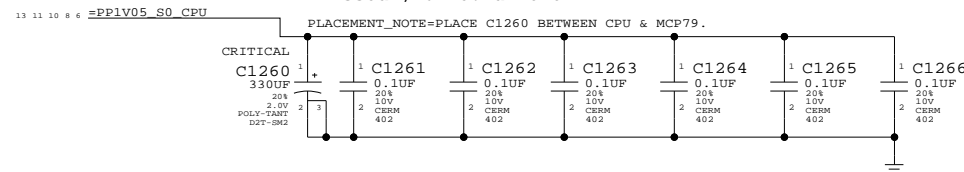
### VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



### VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18

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### CPU Decoupling

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	12	76

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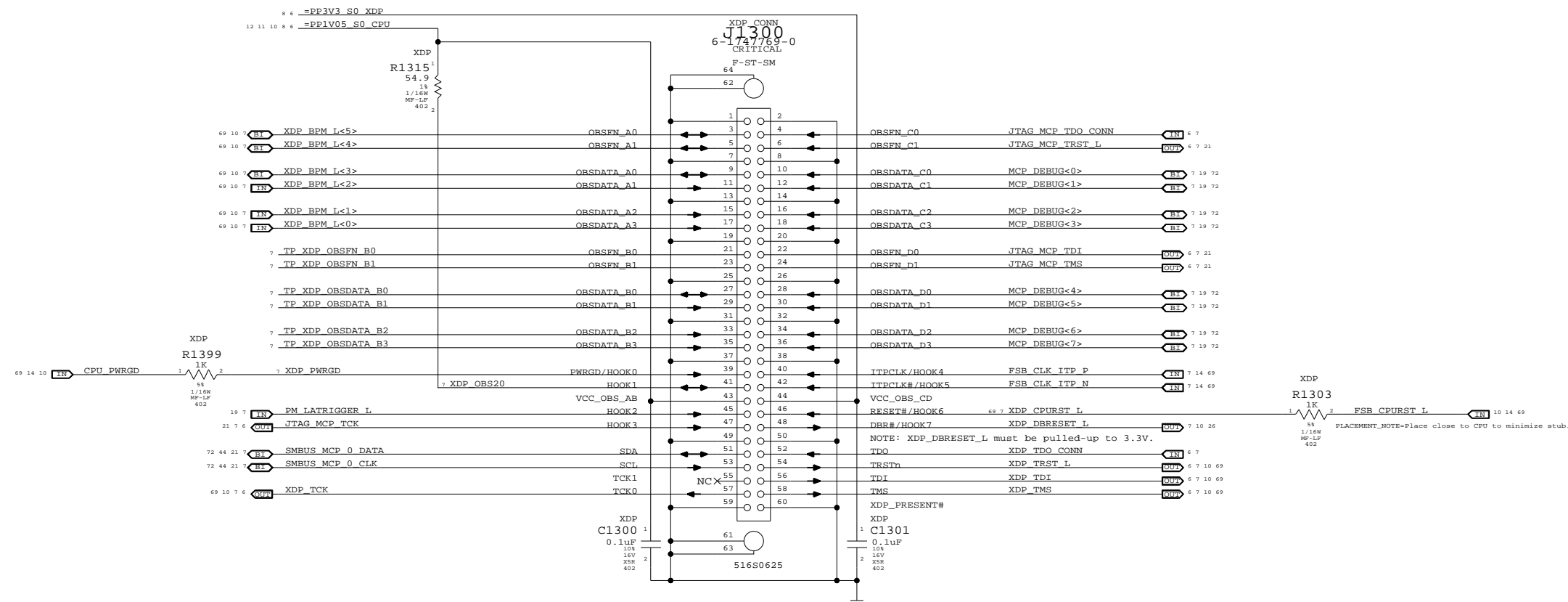
2

1

### Mini-XDP Connector

NOTE: This is not the standard XDP pinout.  
Use with 920-0620 adapter board to support CPU, MCP debugging.

### MCP79-specific pinout



← Direction of XDP module  
Please avoid any obstructions  
on even-numbered side of J1300

eXtended Debug Port (MiniXDP)  
SYNC\_MASTER=M99\_MLB SYNC\_DATE=01/08/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT		OF
NONE	13		76

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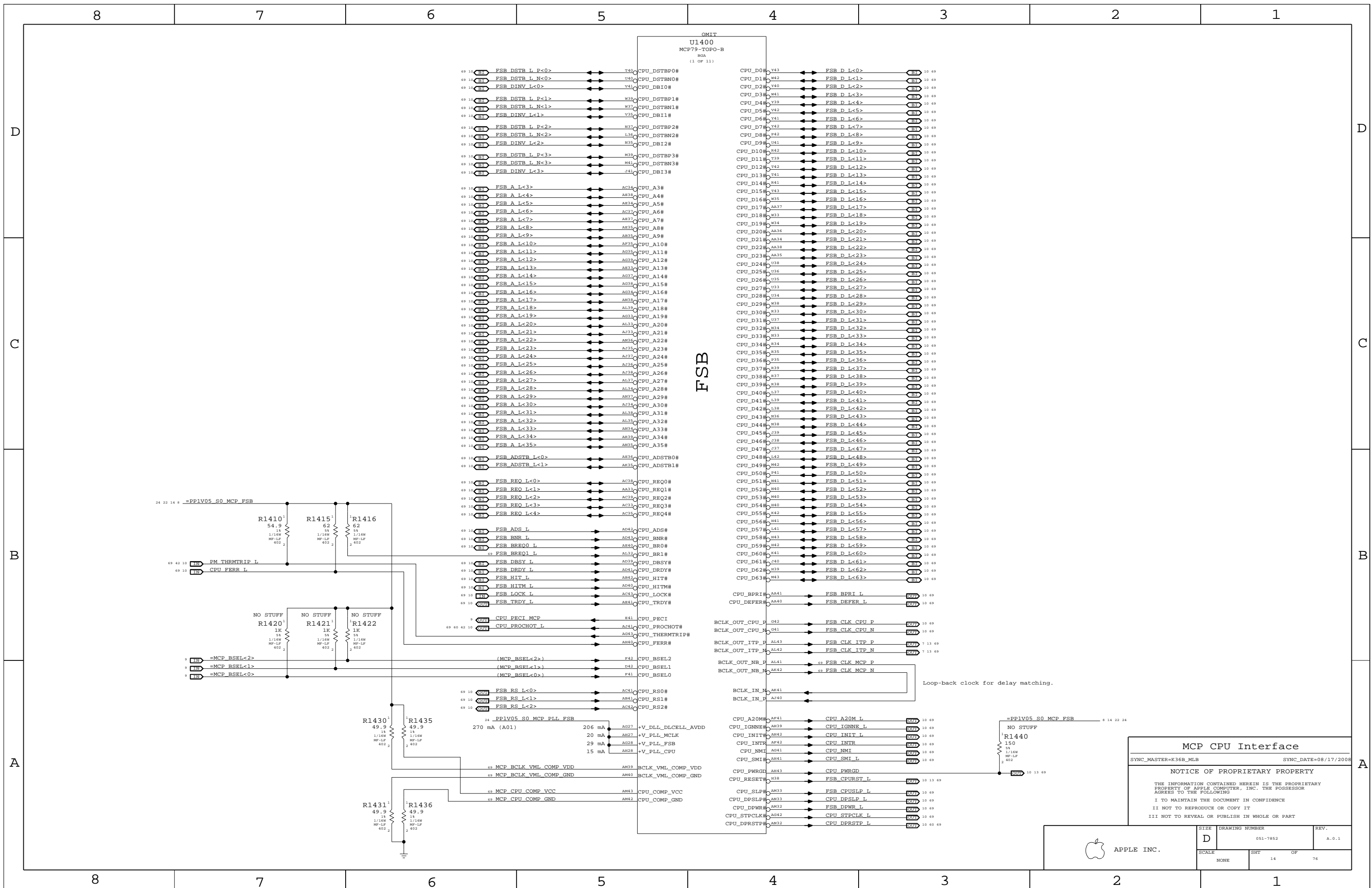
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**MCP CPU Interface**

SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

**NOTICE OF PROPRIETARY PROPERTY**

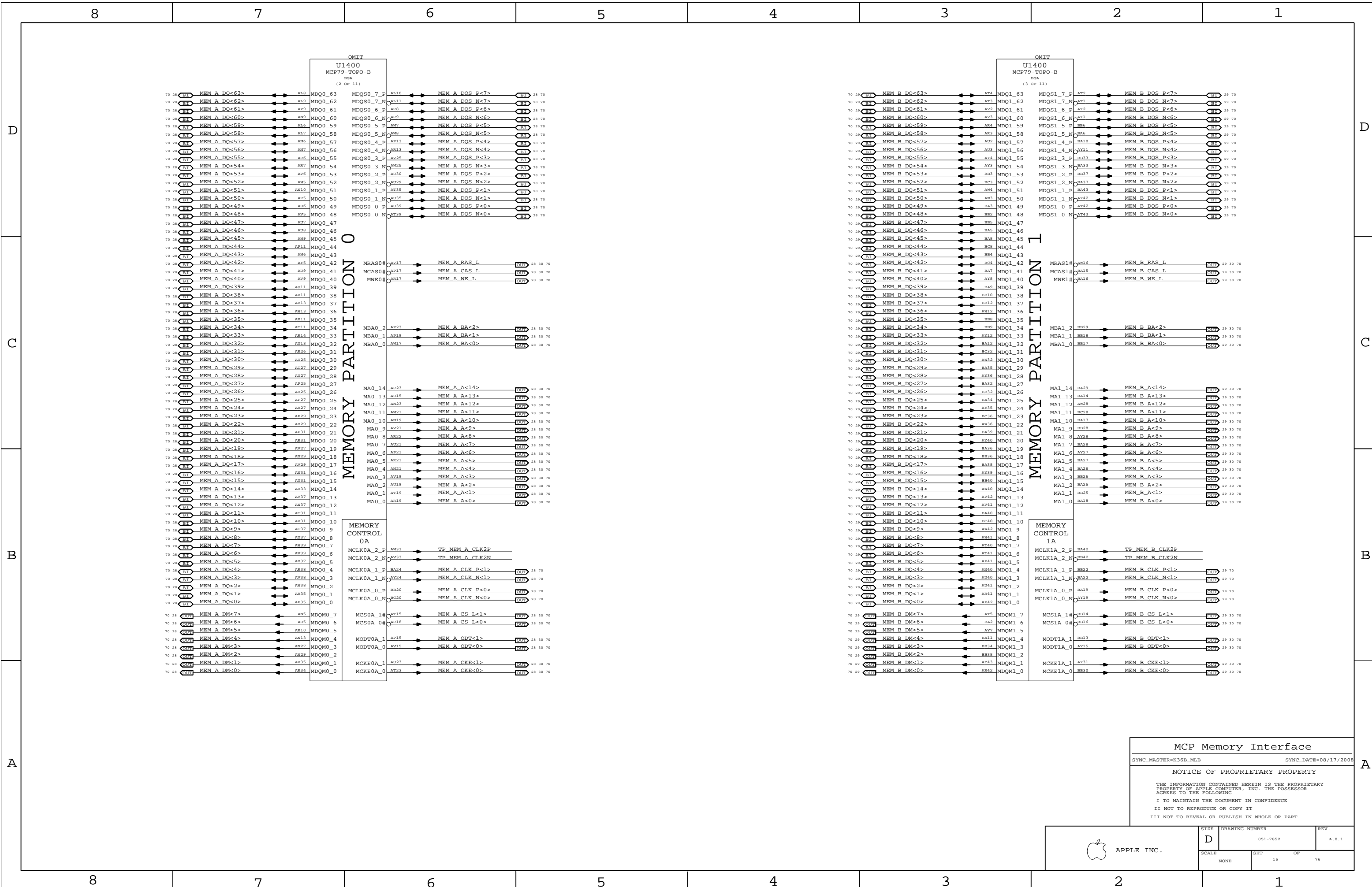
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	D	051-7852	A.0.1
SCALE		SHT	OF
NONE		14	76



**MCP Memory Interface**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

**NOTICE OF PROPRIETARY PROPERTY**

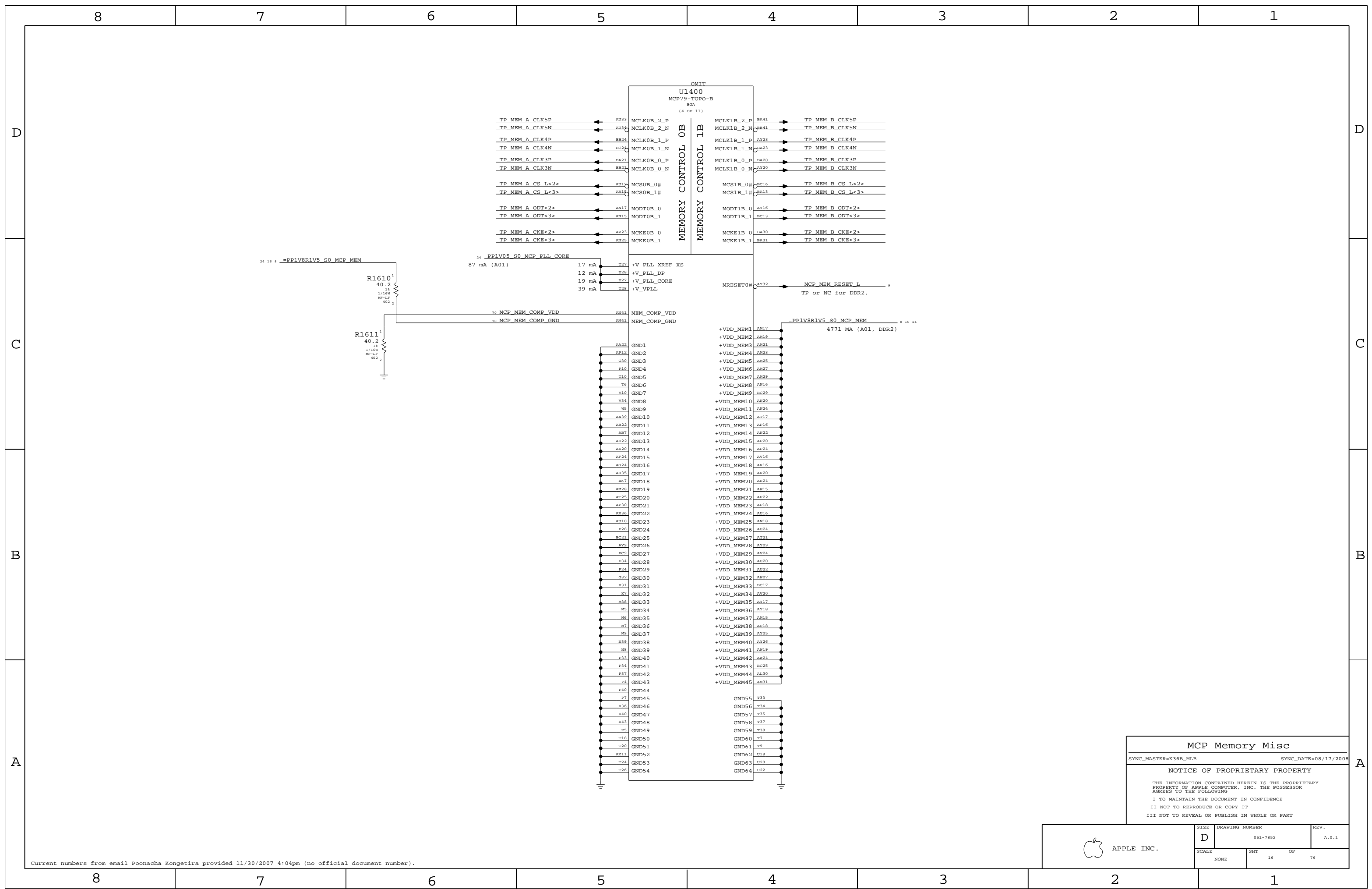
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	SCALE NONE	SHEET 15	OF 76



**MCP Memory Misc**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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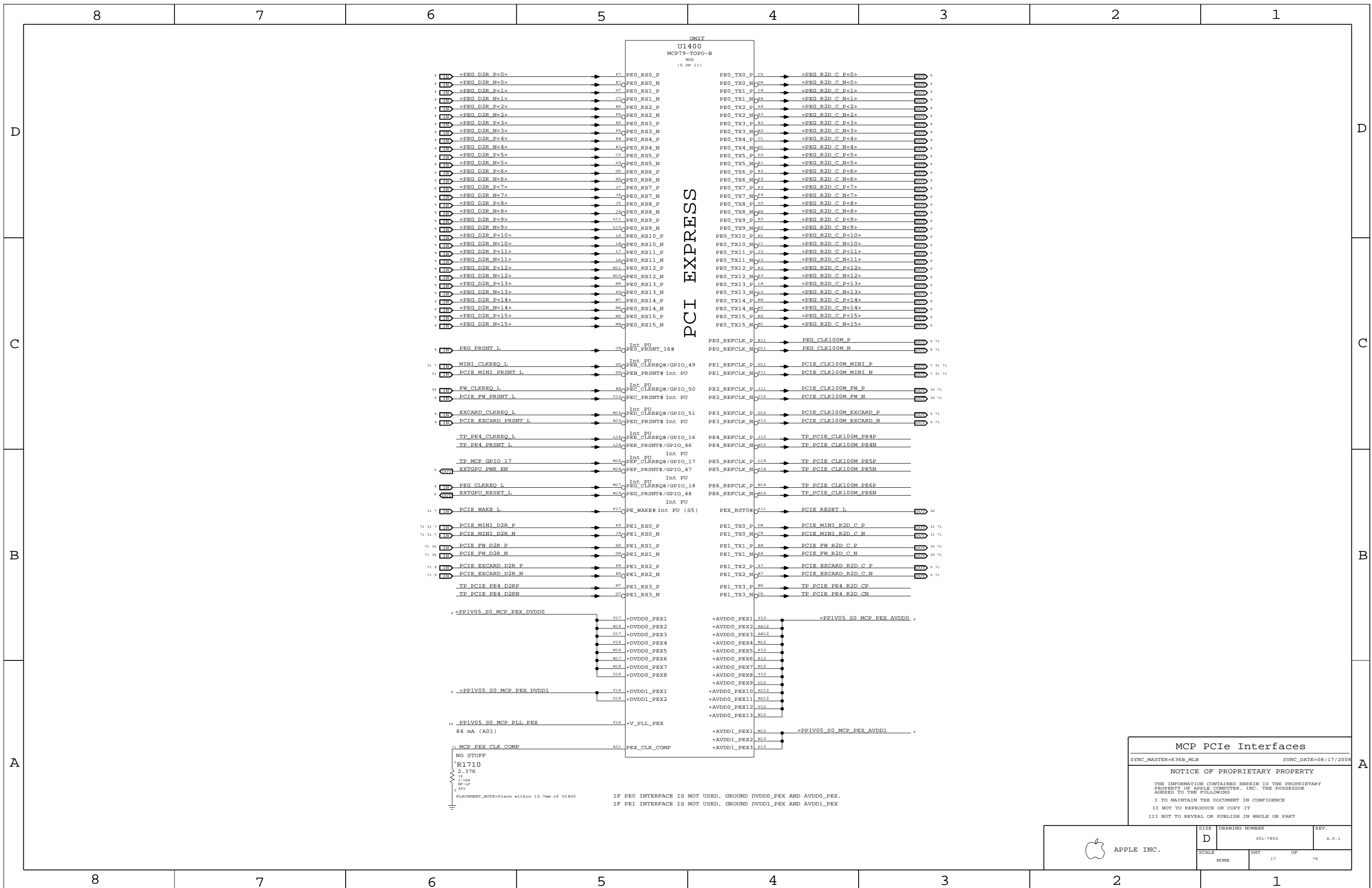
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	SCALE NONE	SHEETS 16	OF 76

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).





**MCP PCIe Interfaces**

SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

**NOTICE OF PROPRIETARY PROPERTY**

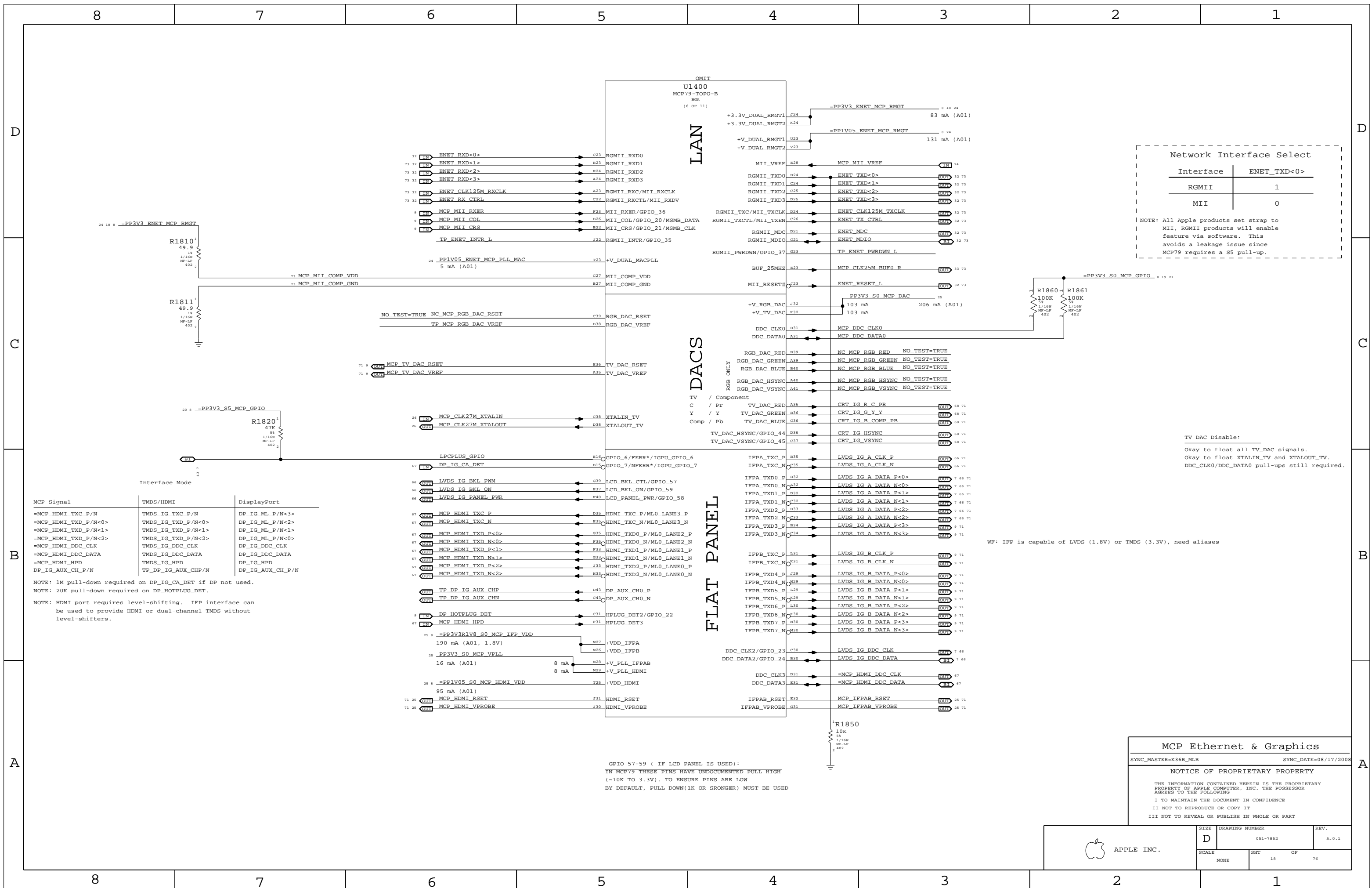
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	SCALE NONE	SHEETS 17	OF 76



Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMI products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

TV DAC Disable:  
 Okay to float all TV\_DAC signals.  
 Okay to float XTALIN\_TV and XTALOUT\_TV.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

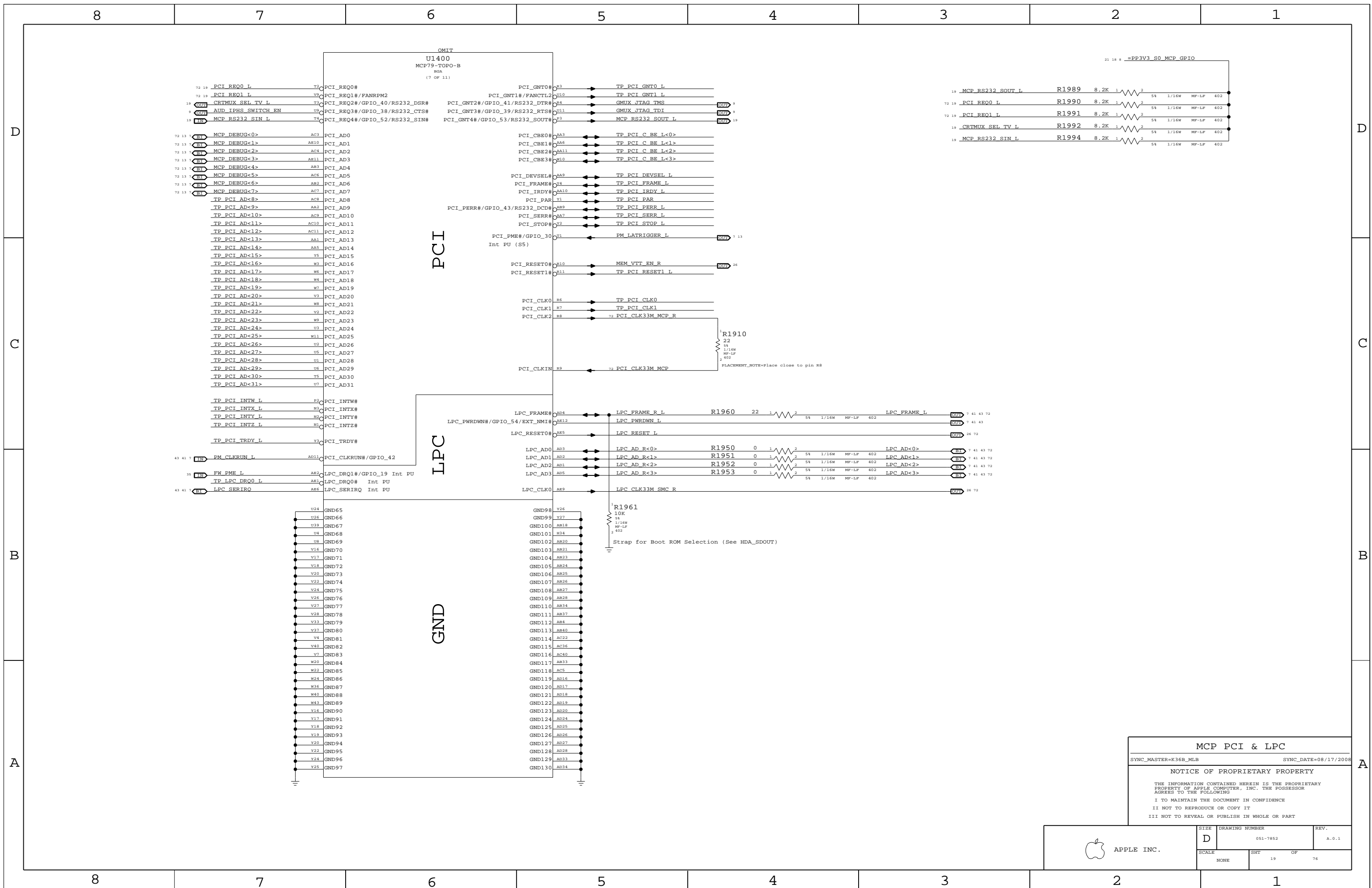
NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
 NOTE: 20K pull-down required on DP\_HOTPLUG\_DET.  
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

GPIO 57-59 ( IF LCD PANEL IS USED ):  
 IN MCP79 THESE PINS HAVE UNDOCUMENTED PULL HIGH  
 (~10K TO 3.3V). TO ENSURE PINS ARE LOW  
 BY DEFAULT, PULL DOWN(1K OR STRONGER) MUST BE USED

**MCP Ethernet & Graphics**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	18		



**MCP PCI & LPC**

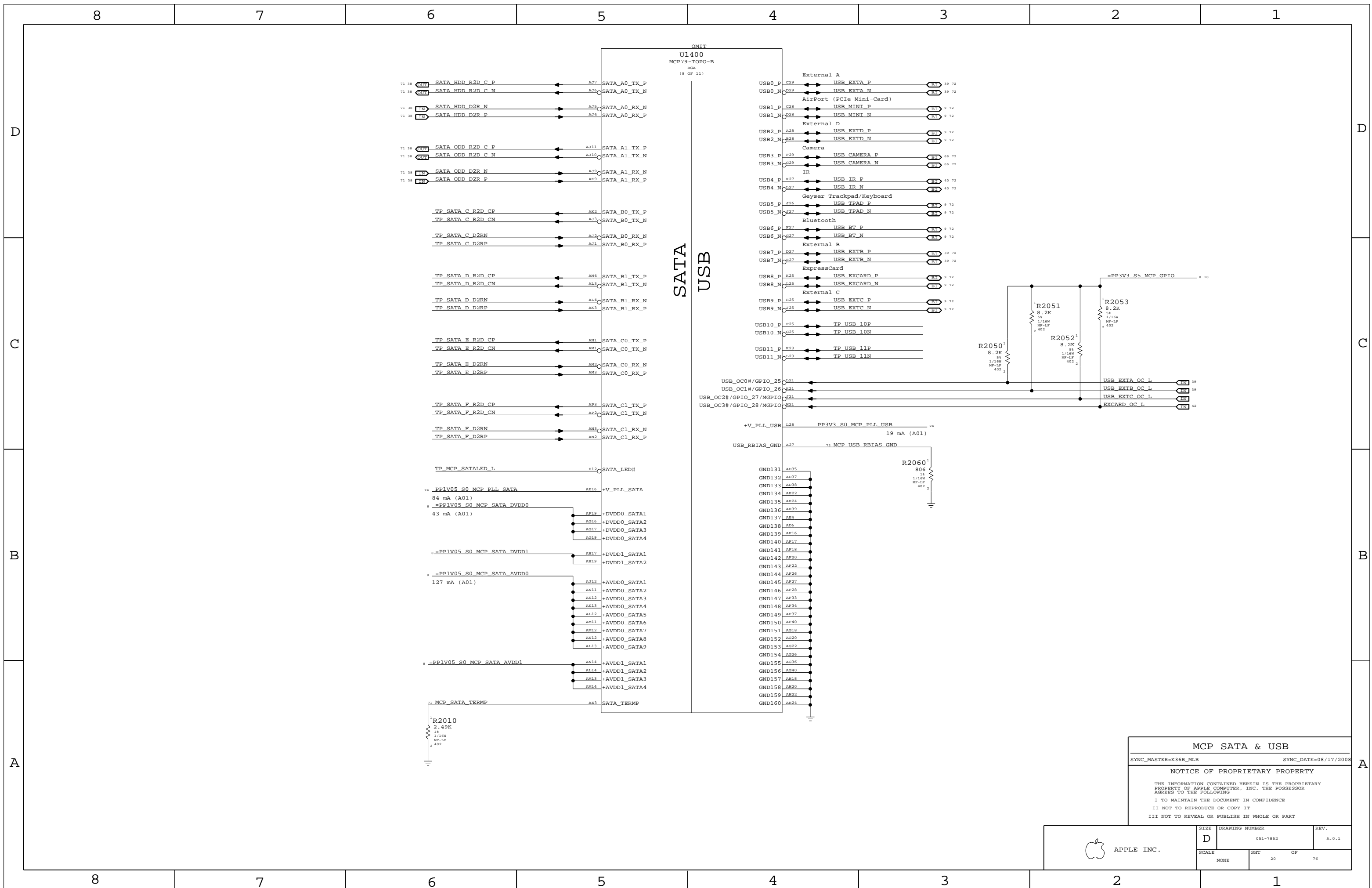
SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

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	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	19		



**MCP SATA & USB**

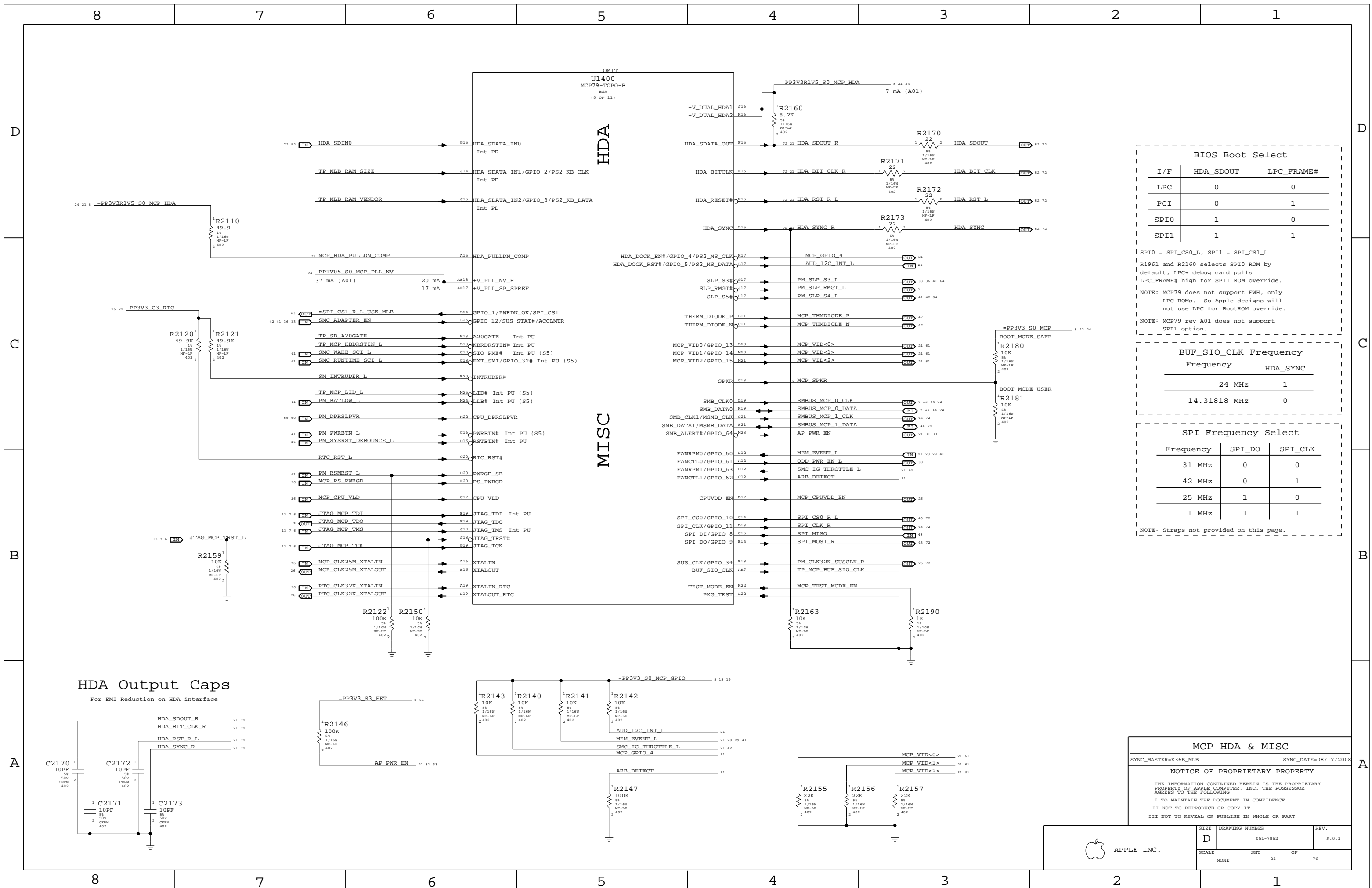
SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7852	REV. A.0.1
	SCALE NONE	SHT 20	OF 76



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L  
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.  
 NOTE: MCP79 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.  
 NOTE: MCP79 rev A01 does not support SPI1 option.

BUF\_SIO\_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

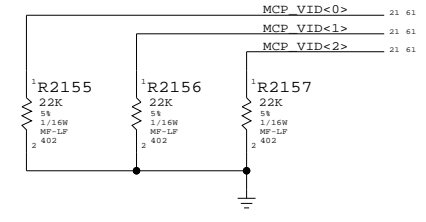
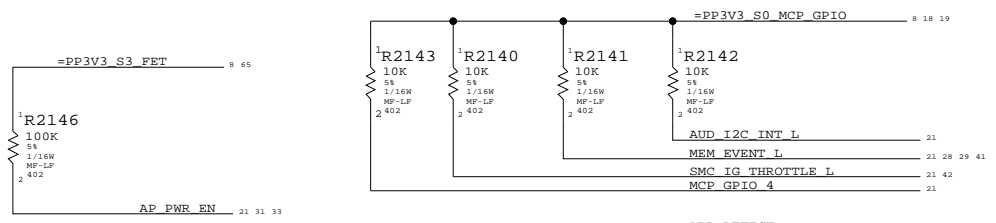
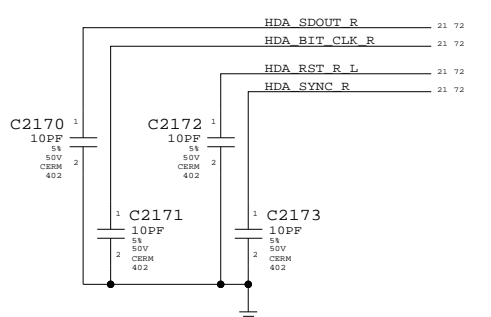
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



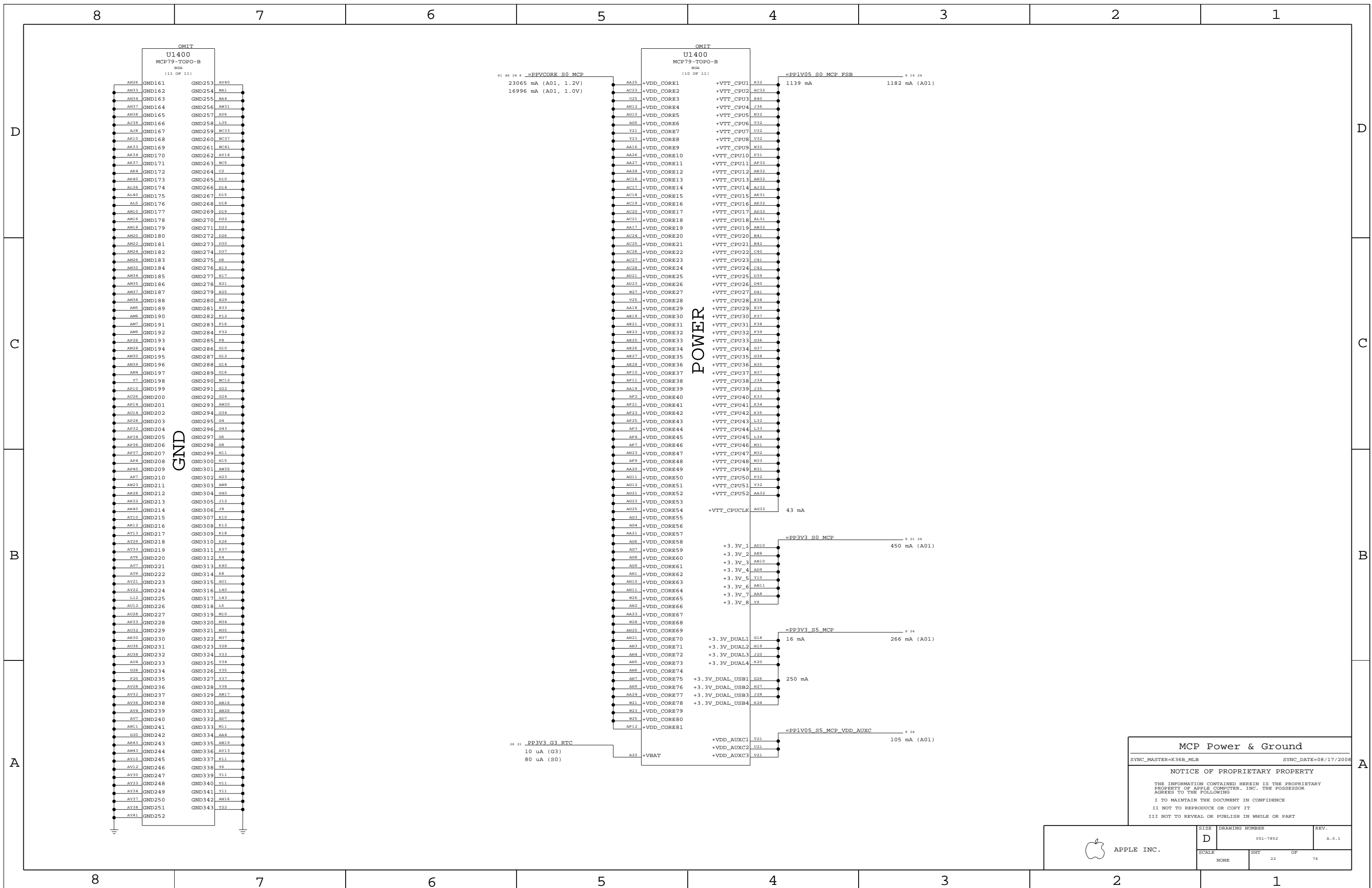
MCP HDA & MISC

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	21	76



**MCP Power & Ground**

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	DRAWING NUMBER		REV.
	D	051-7852	A.0.1
SCALE		SHT	OF
NONE		22	76

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MCP79 A01 Silicon Support

SYNC\_MASTER=K36H\_MLB SYNC\_DATE=08/17/2008


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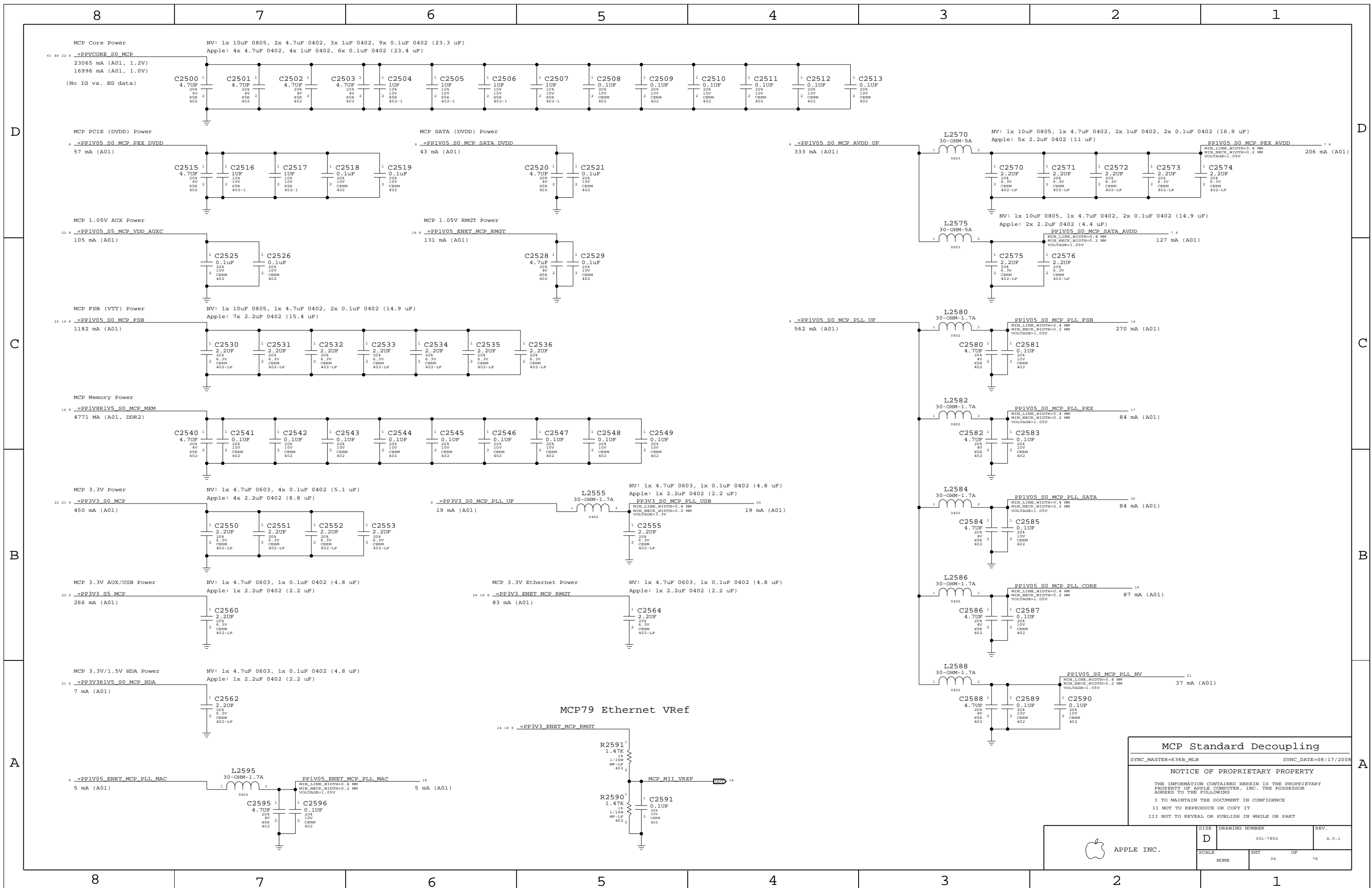
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	D	051-7852	A.0.1
SCALE	SHT	OF	
NONE	23	76	



**MCP Standard Decoupling**  
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SCALE	DRAWING NUMBER		REV.
	D 051-7852		A.0.1
SCALE	SHT	OF	76
NONE	24		





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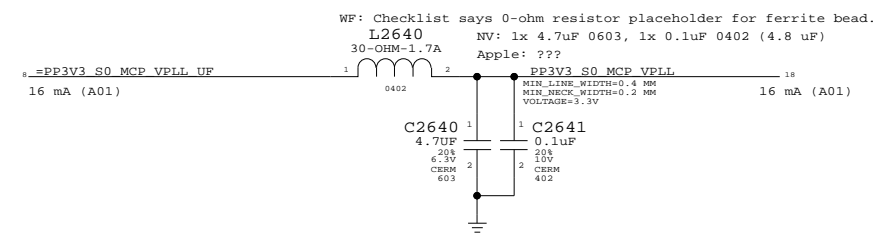
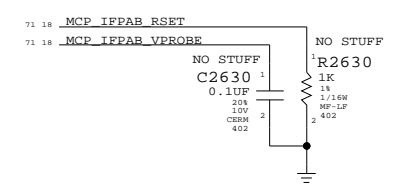
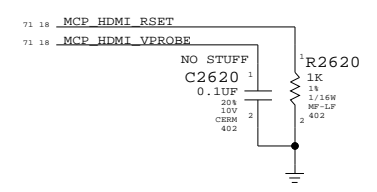
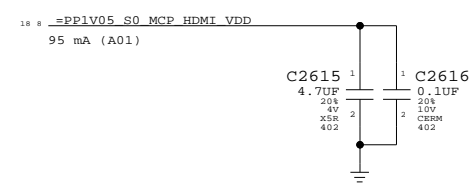
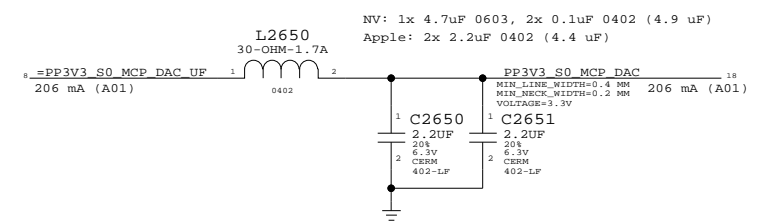
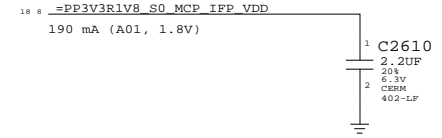
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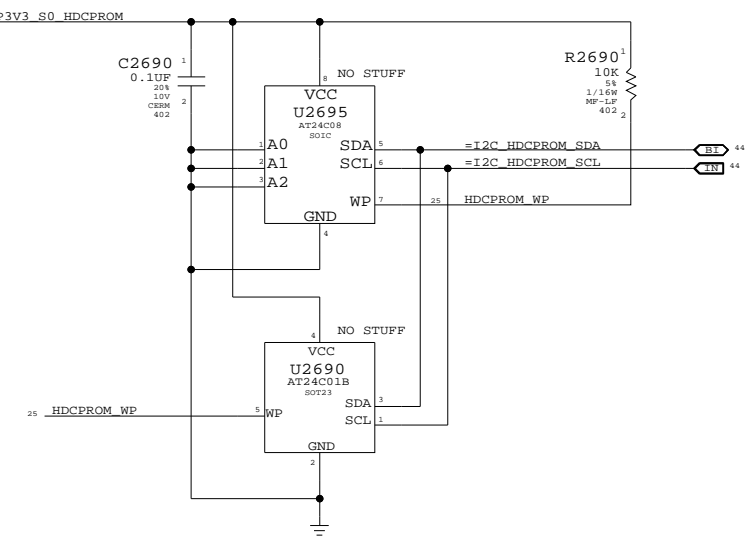
D

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.  
 NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
 Apple: 1x 2.2uF 0402 (2.2 uF)



### HDCP ROM

WF: Open question on which package option(s) nVidia can support.



C

C

B

B

A

A

SYNC FROM T18  
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT  
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672

MCP Graphics Support  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	25		

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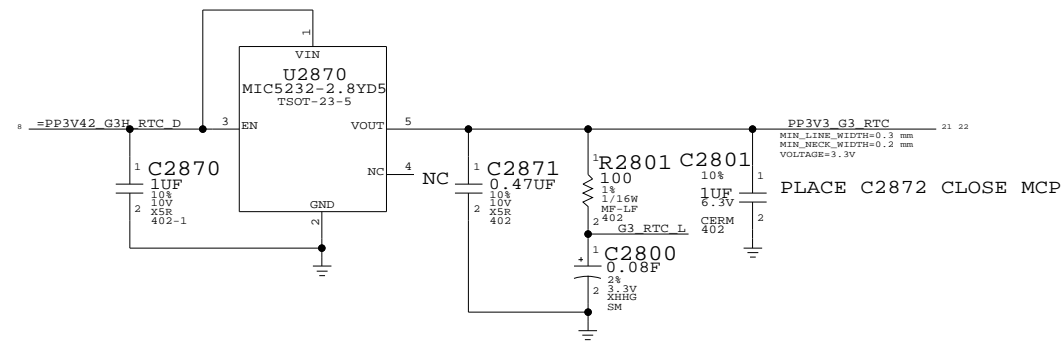
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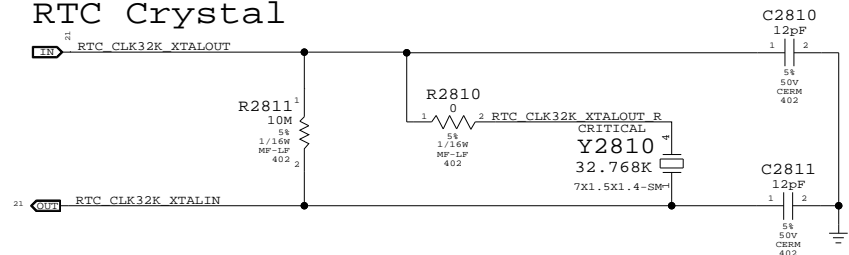
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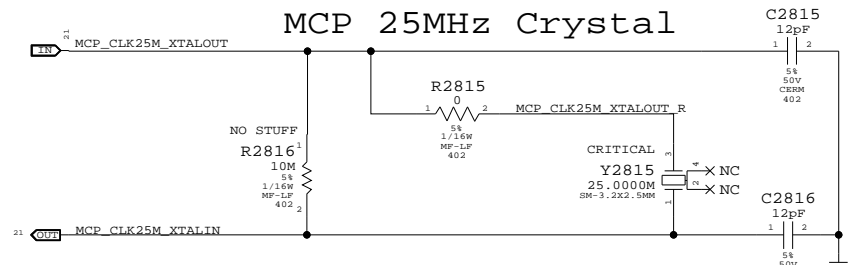
### RTC Power Sources



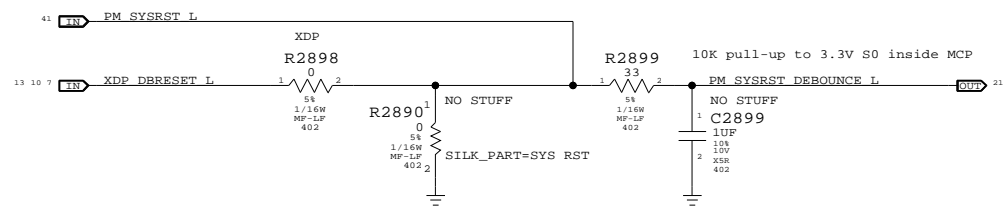
### RTC Crystal



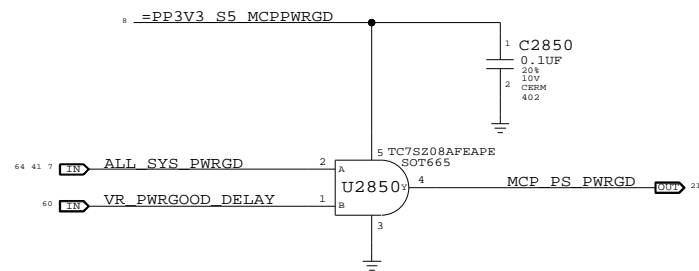
### MCP 25MHz Crystal



### Reset Button

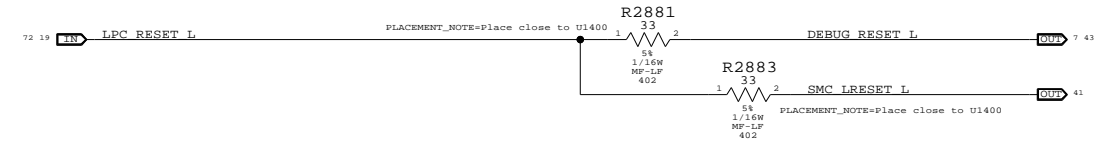


### MCP S0 PWRGD

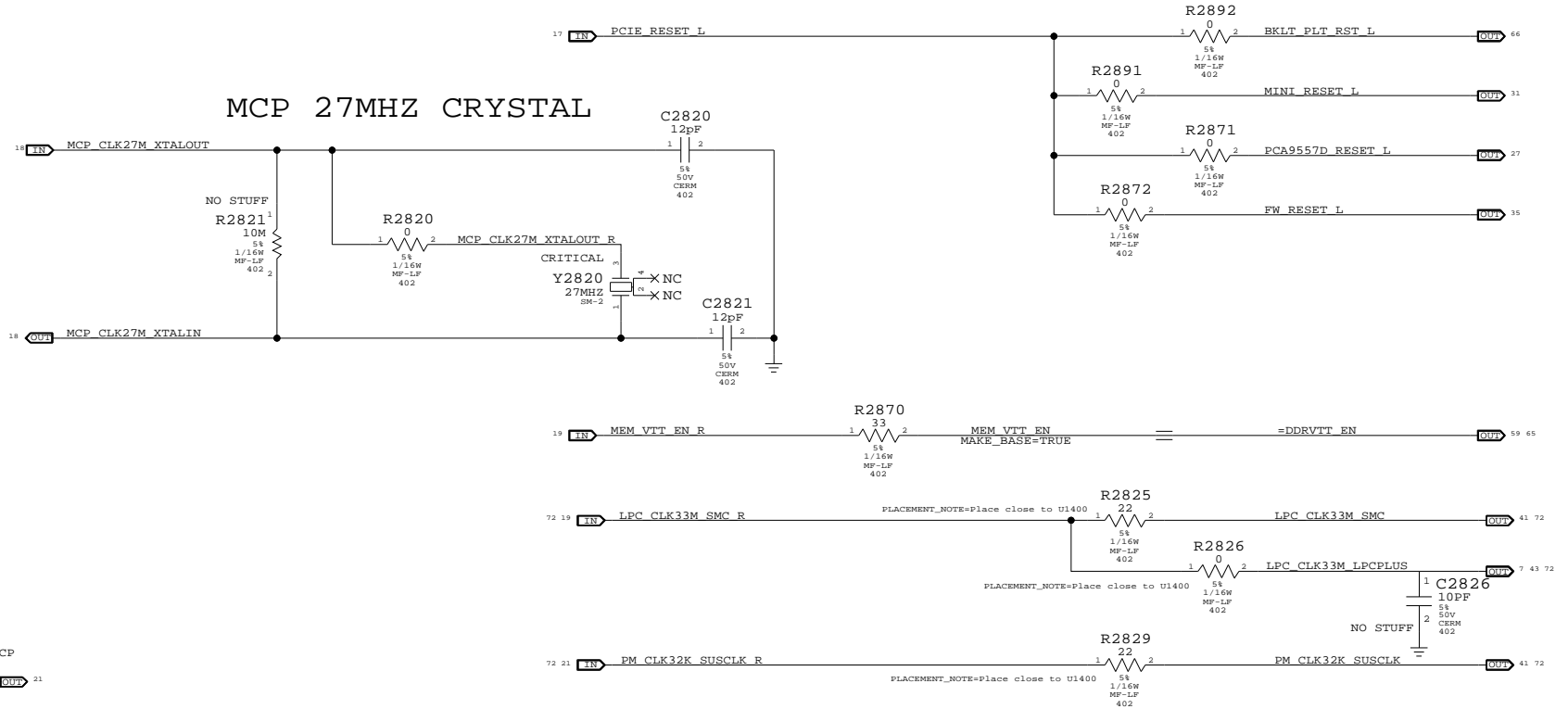


### Platform Reset Connections

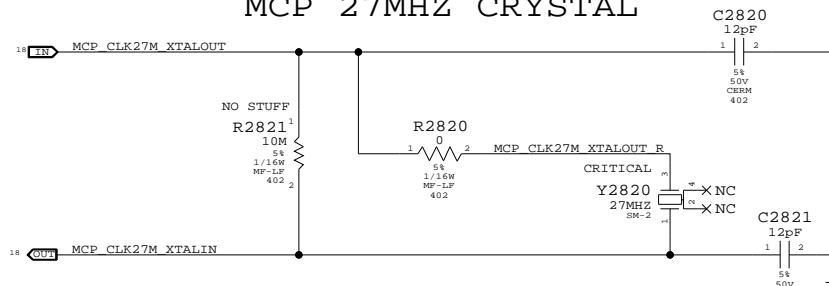
#### LPC Reset (Unbuffered)



#### PCIE Reset (Unbuffered)



### MCP 27MHZ CRYSTAL



SYNC FROM T18  
 CHANGE RESET BUTTON TO RESET PADS  
 REMOVE UNUSED PCIE RESET SIGNALS  
 REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
 CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS  
 ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
 CHANGE Y2810 AND U2850 TO SMALLER PARTS

SB Misc		
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008	
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APPLE INC.	SCALE	SHT	OF	REV.
	NONE	26	76	A.0.1

# Page Notes

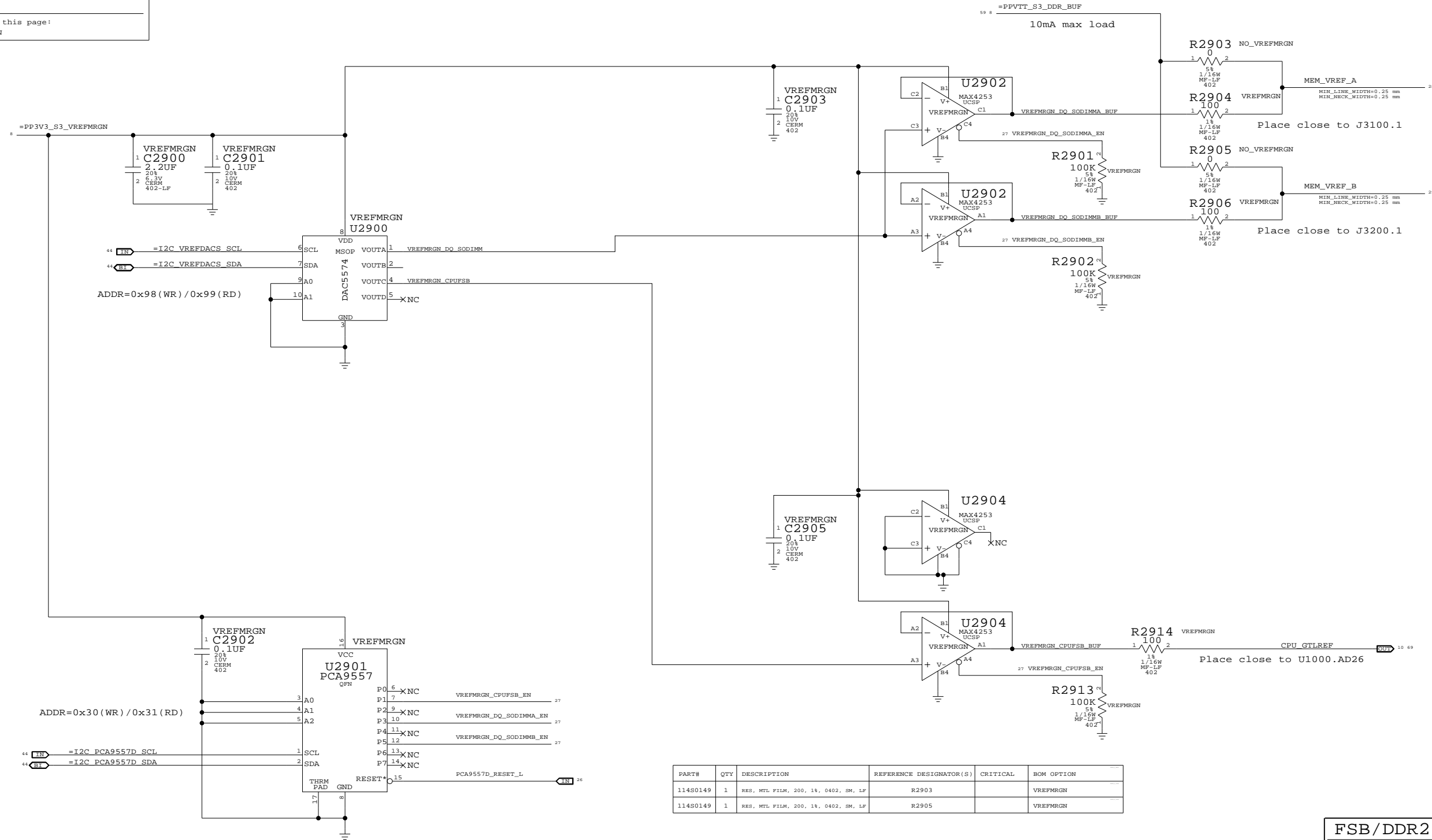
Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMRGN  
 - =PP3V3\_S5\_VREFMRGN  
 - =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
 - =I2C\_VREFDACS\_SCL  
 - =I2C\_VREFDACS\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
 VREFMRGN AND NO VREFMRGN

Voltage divider resistor values at op-amp outputs not yet finalized.

## BOM OPTION TO SELECT VREF SOURCE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES, MTL FILM, 200, 1%, 0402, SM, LF	R2903		VREFMRGN
114S0149	1	RES, MTL FILM, 200, 1%, 0402, SM, LF	R2905		VREFMRGN

### FSB/DDR2 VREF MARGINING

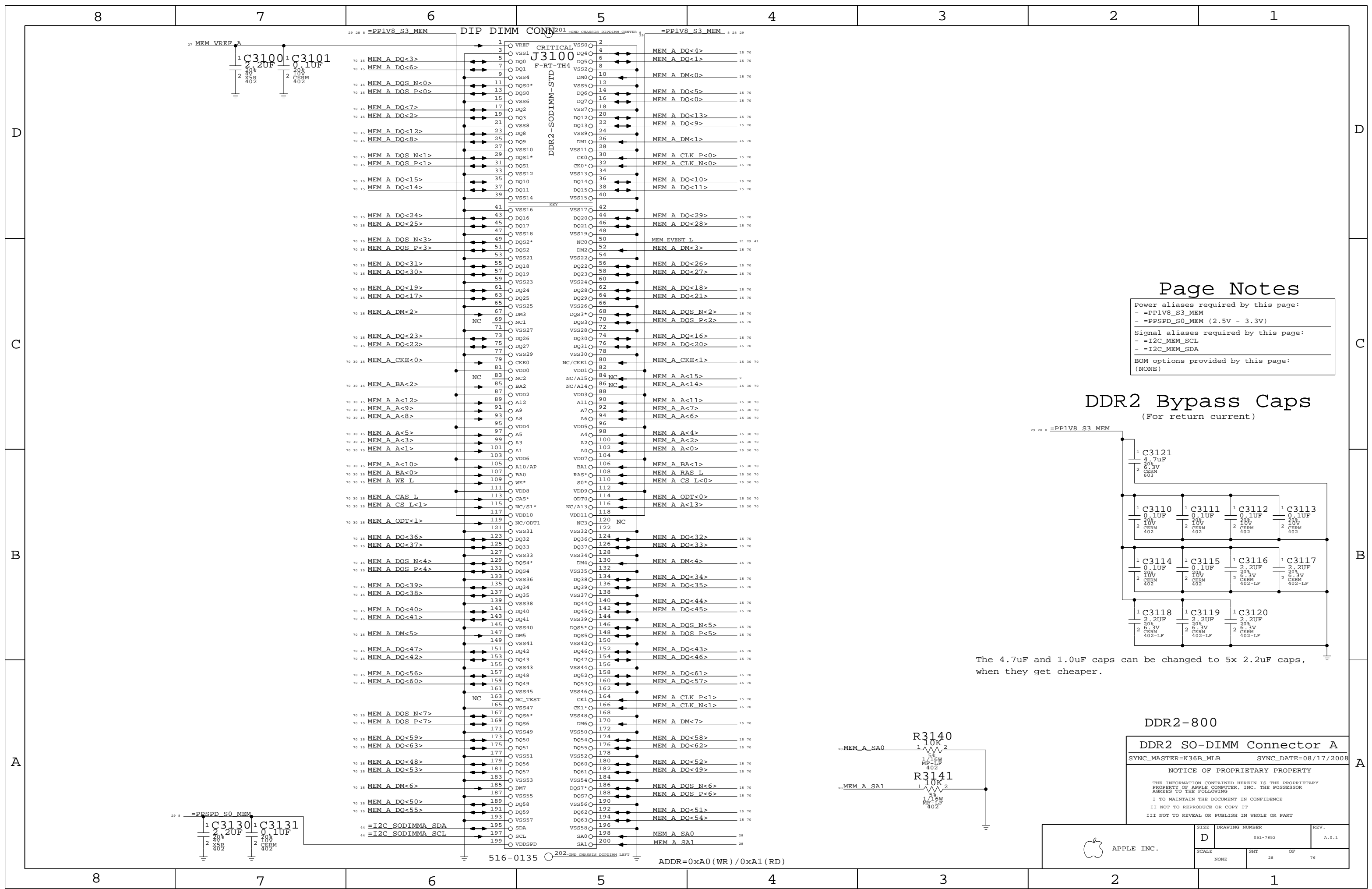
SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	27	76



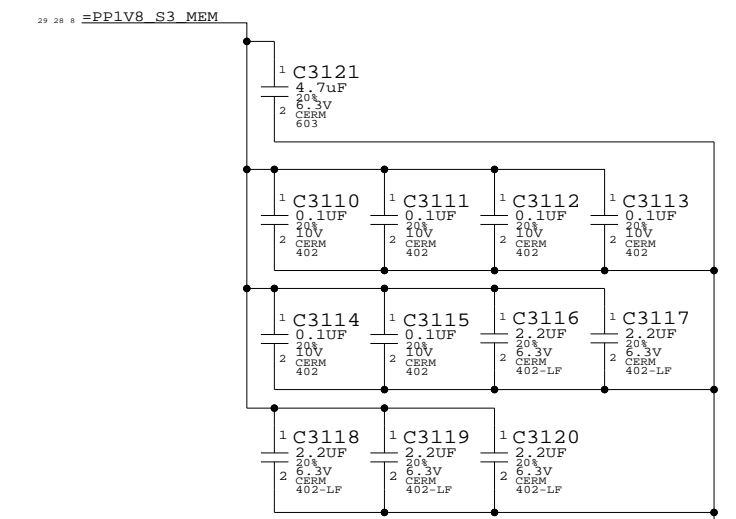
### Page Notes

Power aliases required by this page:  
 - =PP1V8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

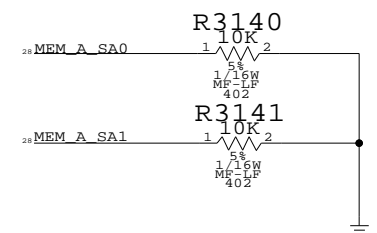
Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

### DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



### DDR2-800

**DDR2 SO-DIMM Connector A**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

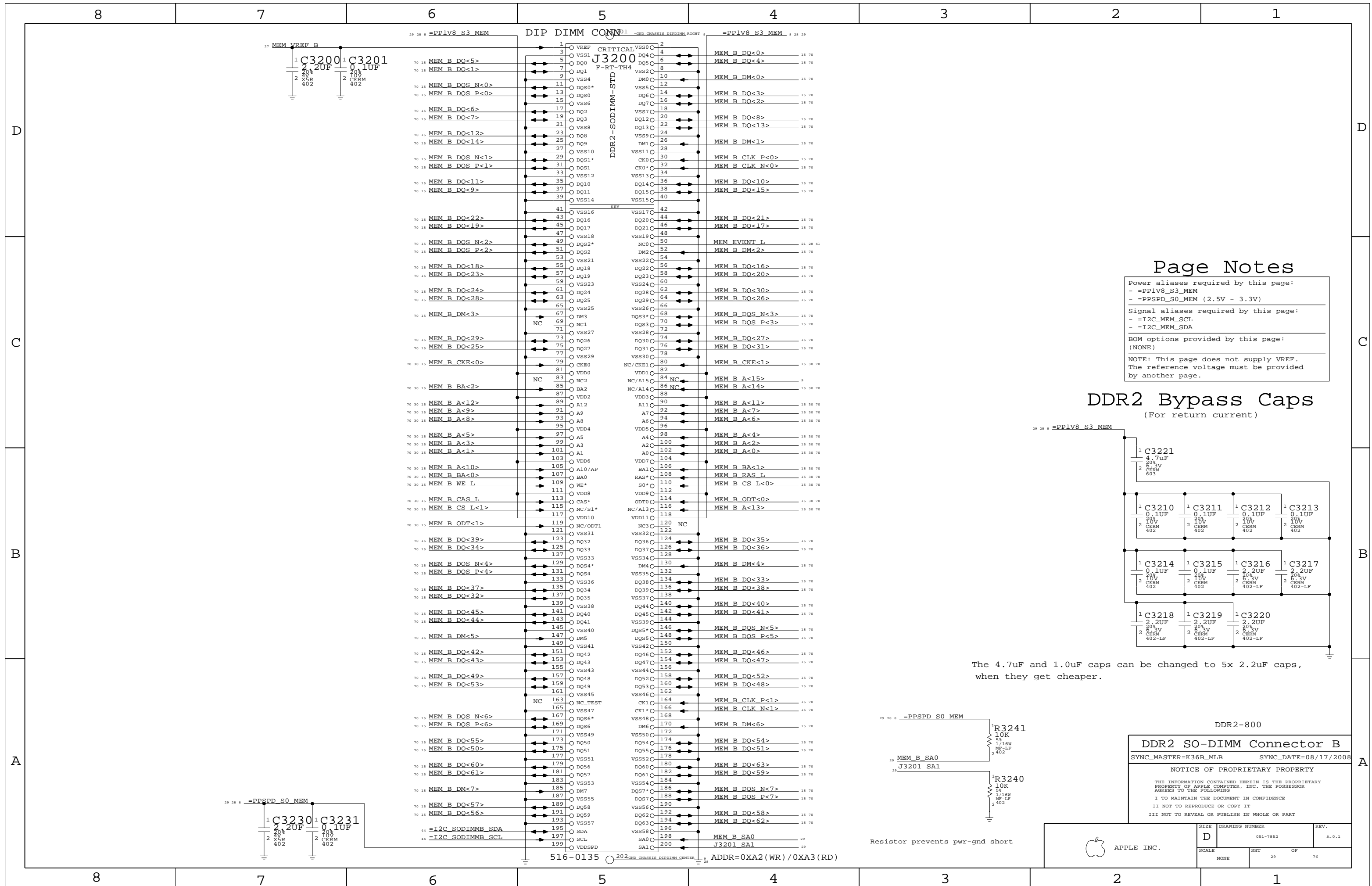
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	NONE	SHT	OF
		28	76

ADDR=0xA0 (WR) / 0xA1 (RD)



### Page Notes

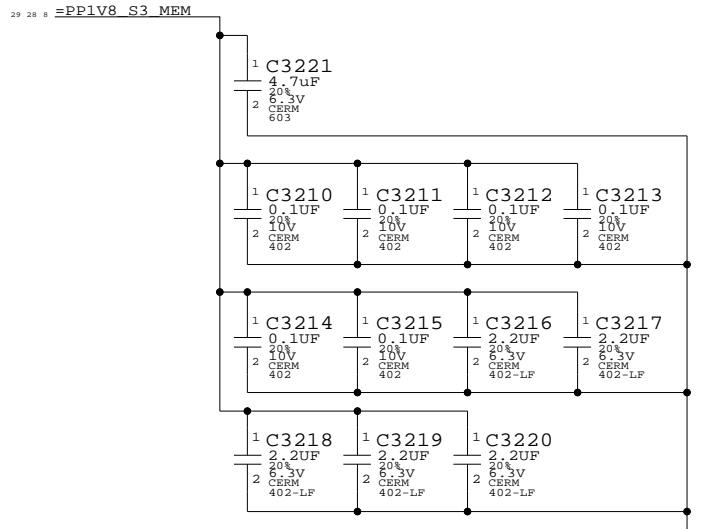
Power aliases required by this page:  
 - =PP1V8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

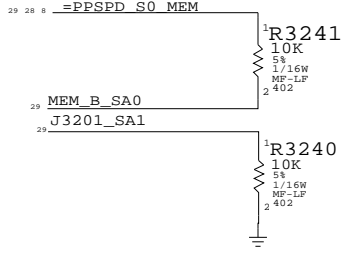
BOM options provided by this page:  
 (NONE)

NOTE: This page does not supply VREF.  
 The reference voltage must be provided by another page.

### DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



DDR2-800

**DDR2 SO-DIMM Connector B**

SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

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8

7

6

5

4

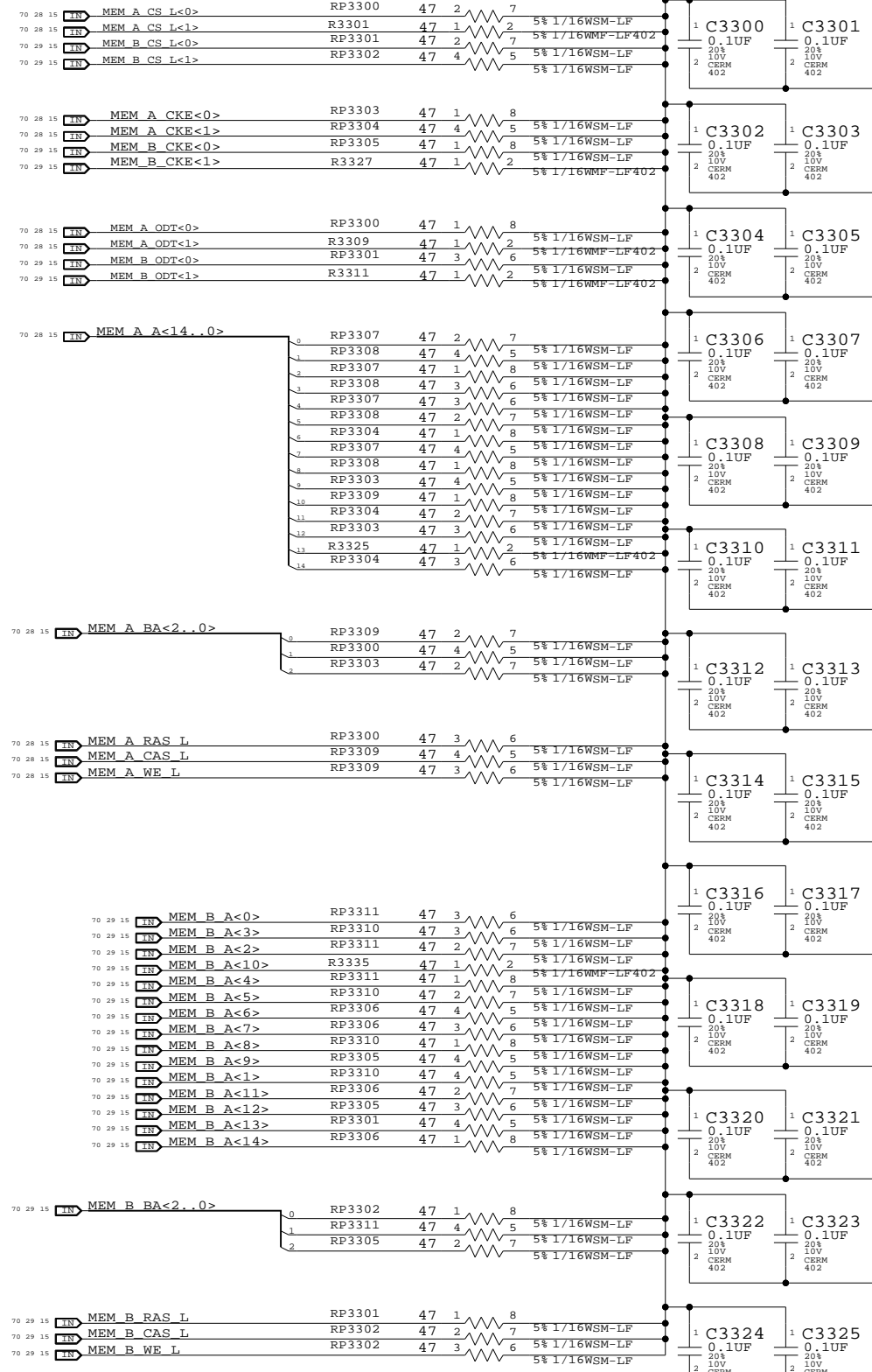
3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it

\*=PP0V9\_S3M\_MEM\_TERM

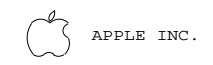


LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9\_S0\_MEM\_TERM

Memory Active Termination

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	30	76

8

7

6

5

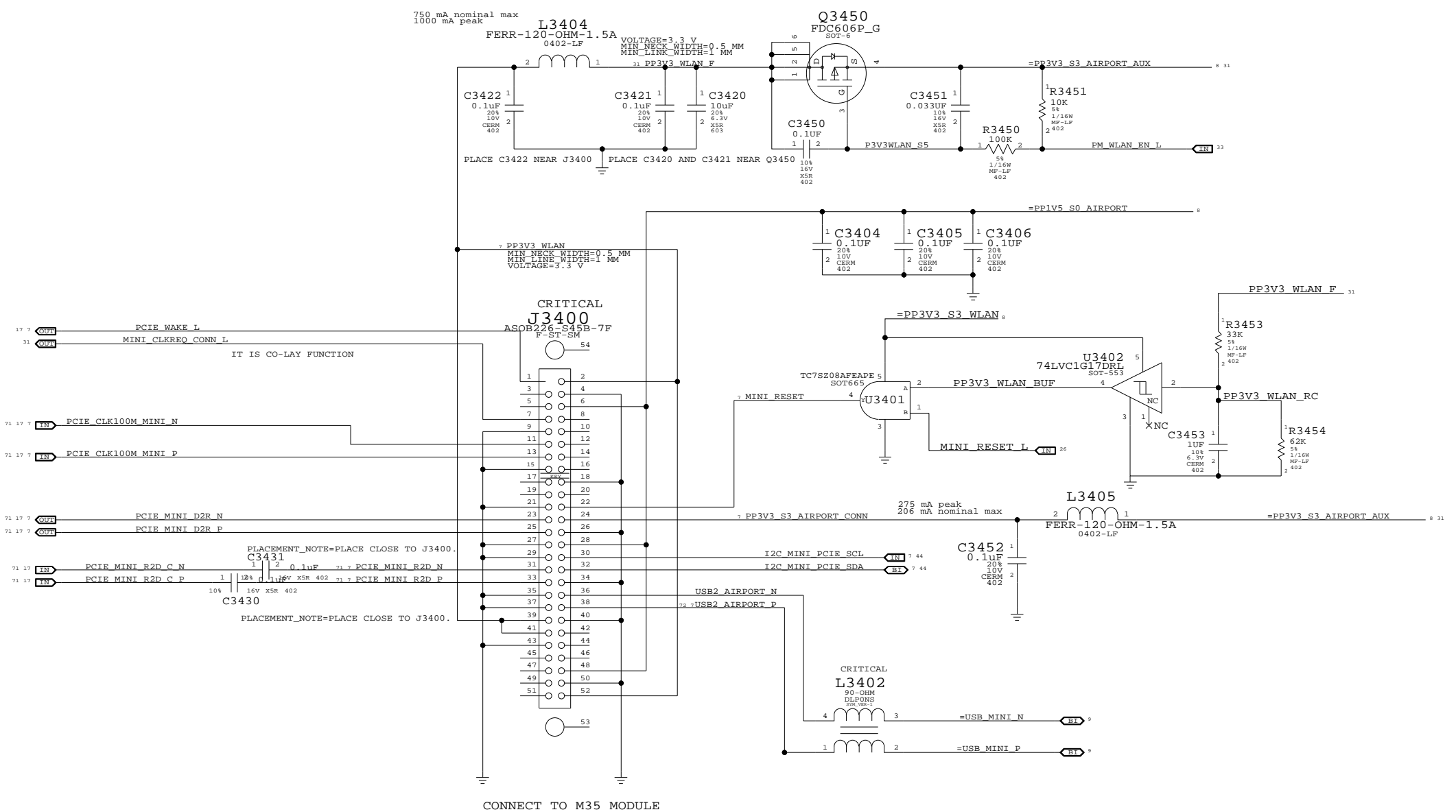
4

3

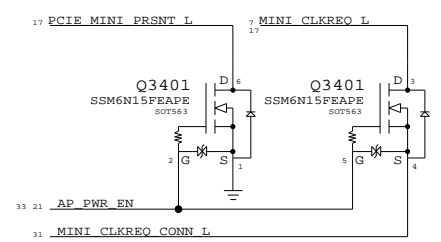
2

1

# AIRPORT

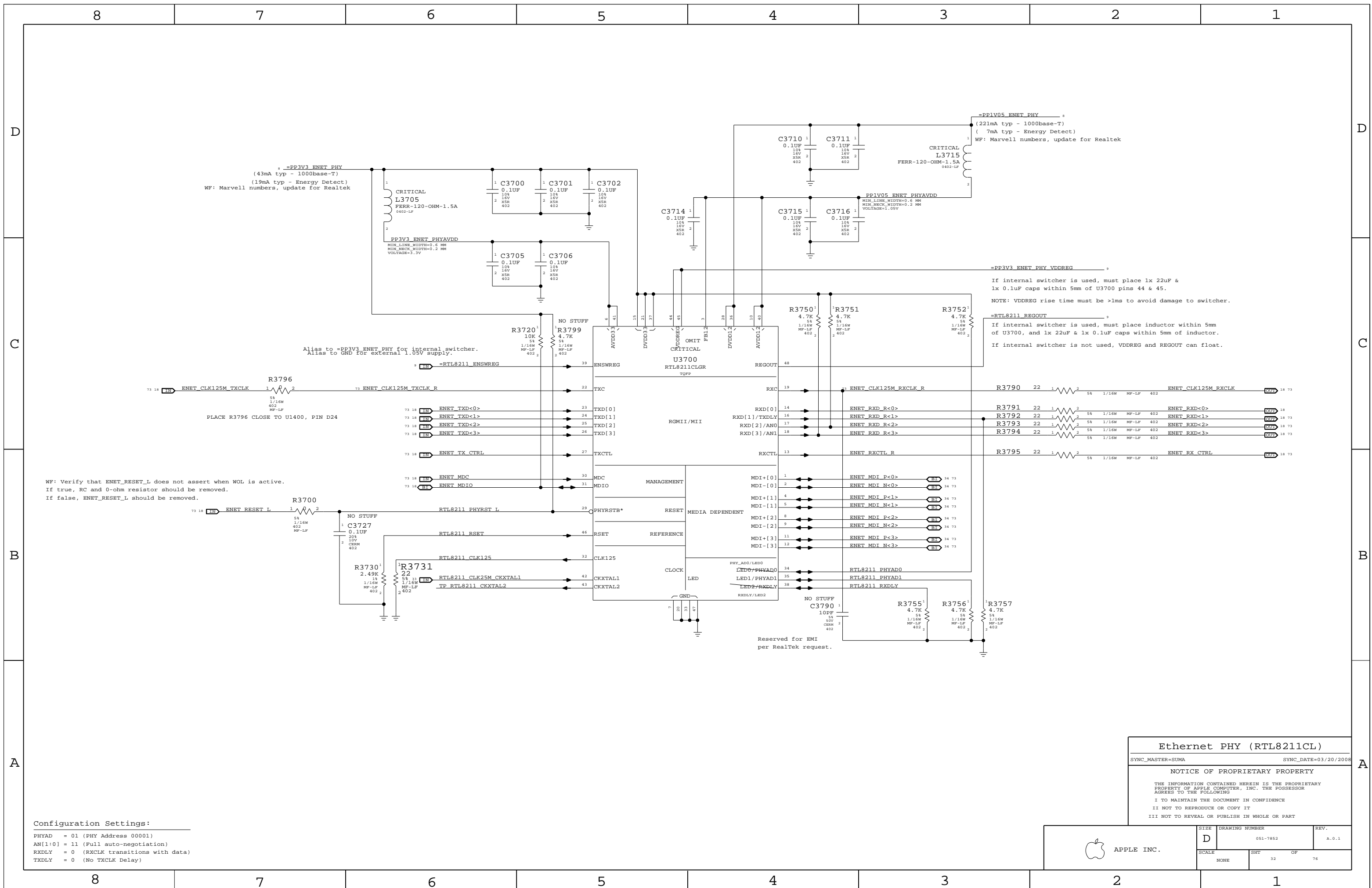


OLD:516S0406 (FOXCONN ONLY)  
 NEW:516S0635 (FOXCONN & ACON)



**Right Clutch Connector**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	31		



**Ethernet PHY (RTL8211CL)**

SYNC\_MASTER=SUMA      SYNC\_DATE=03/20/2008

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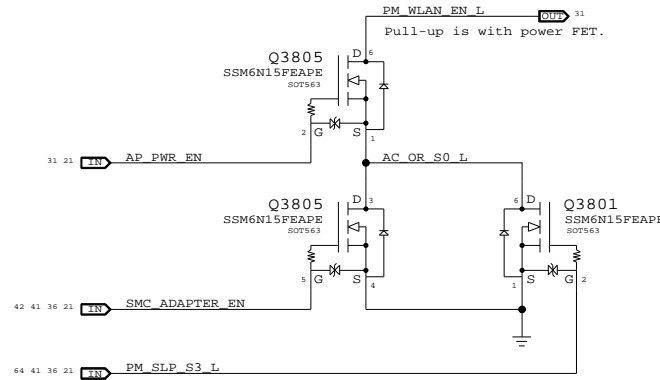
APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7852	REV. A.0.1
	SCALE NONE	SHEET 32	OF 76



### WLAN Enable Generation

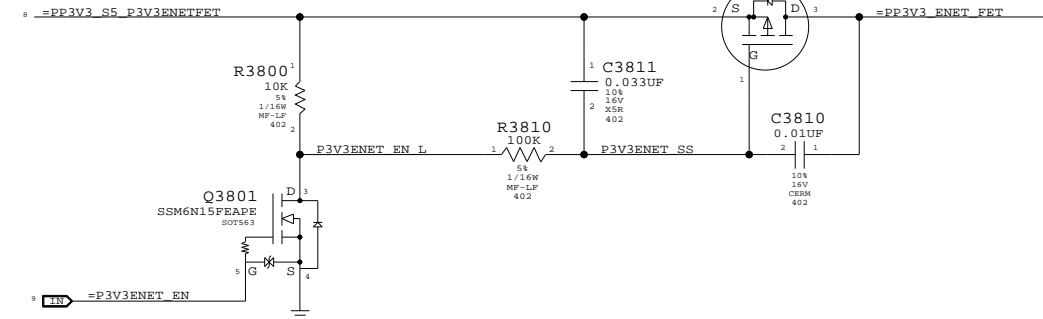
"WLAN" = ("S3" && "AP\_PWR\_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.



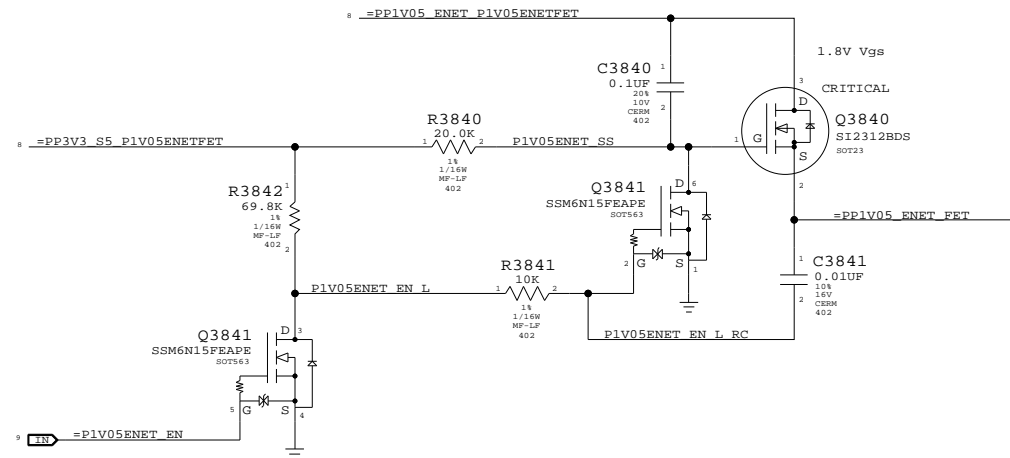
### 3.3V ENET FET

@ 2.5V Vgs:  
Rds(on) = 90mOhm max  
I(max) = 1.7A (85C)



MOBILE:  
Recommend aliasing PM\_SLP\_RMGT\_L and =P3V3ENET\_EN. Nets separated on ARB for alternate power options.

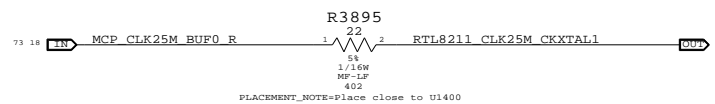
### 1.05V ENET FET



Non-ARB:  
Recommend aliasing PM\_SLP\_RMGT\_L and =P1V05ENET\_EN. Nets separated on ARB for alternate power options.

### RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

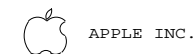


### Ethernet & AirPort Support

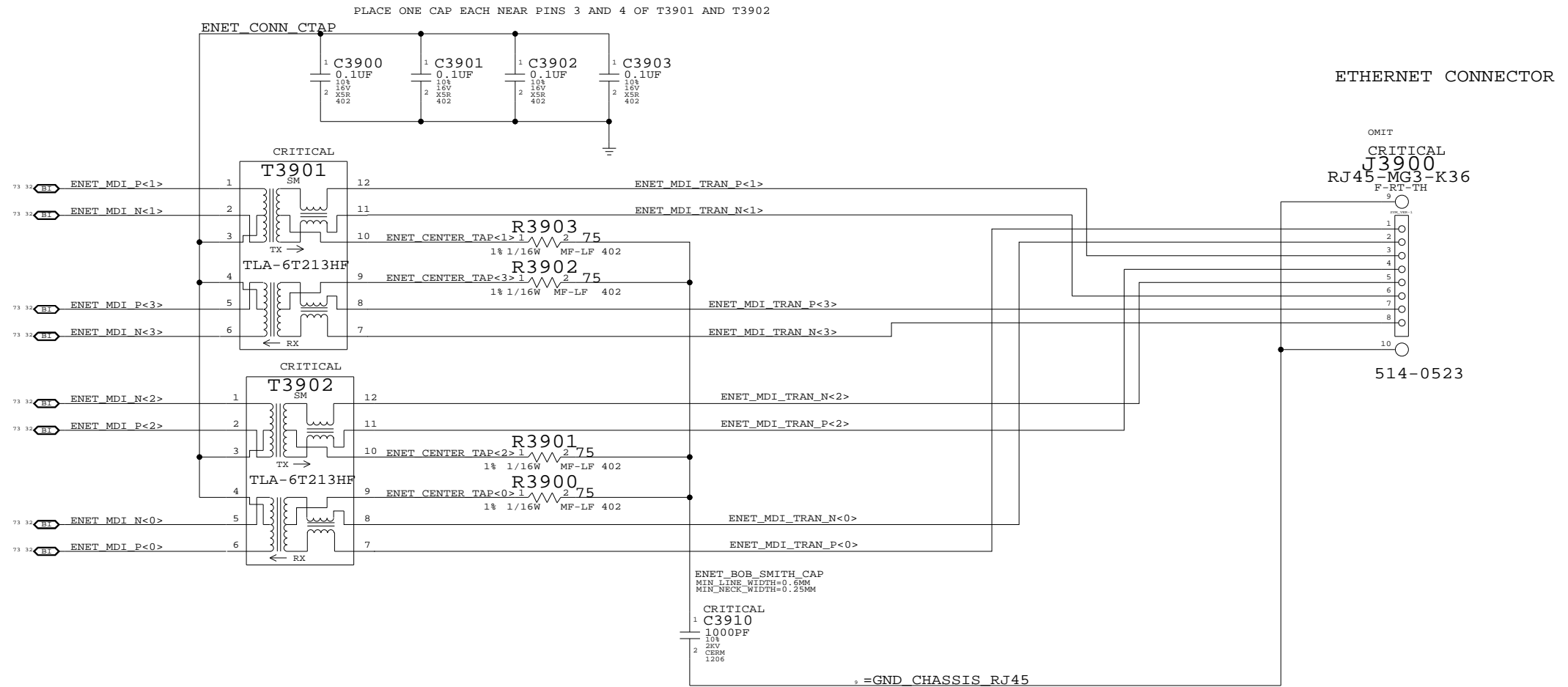
SYNC\_MASTER=SUMA SYNC\_DATE=04/04/2008

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D	051-7852	A.0.1
SCALE	SHT	OF
NONE	33	76



ETHERNET CONNECTOR

SYNC\_MASTER=SUMA SYNC\_DATE=04/04/2008

NOTICE OF PROPRIETARY PROPERTY

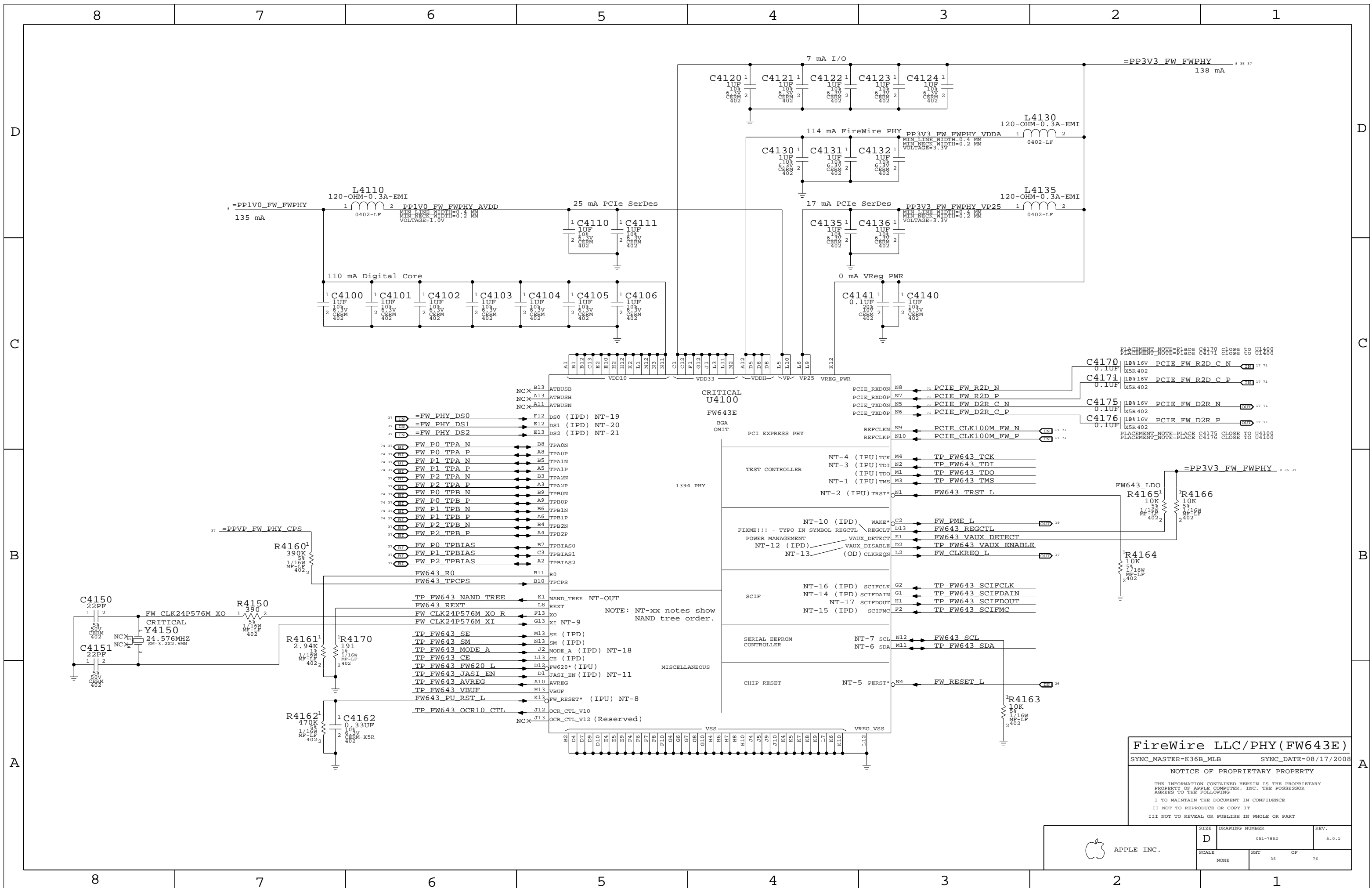
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	34		



**FireWire LLC/PHY (FW643E)**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	35		

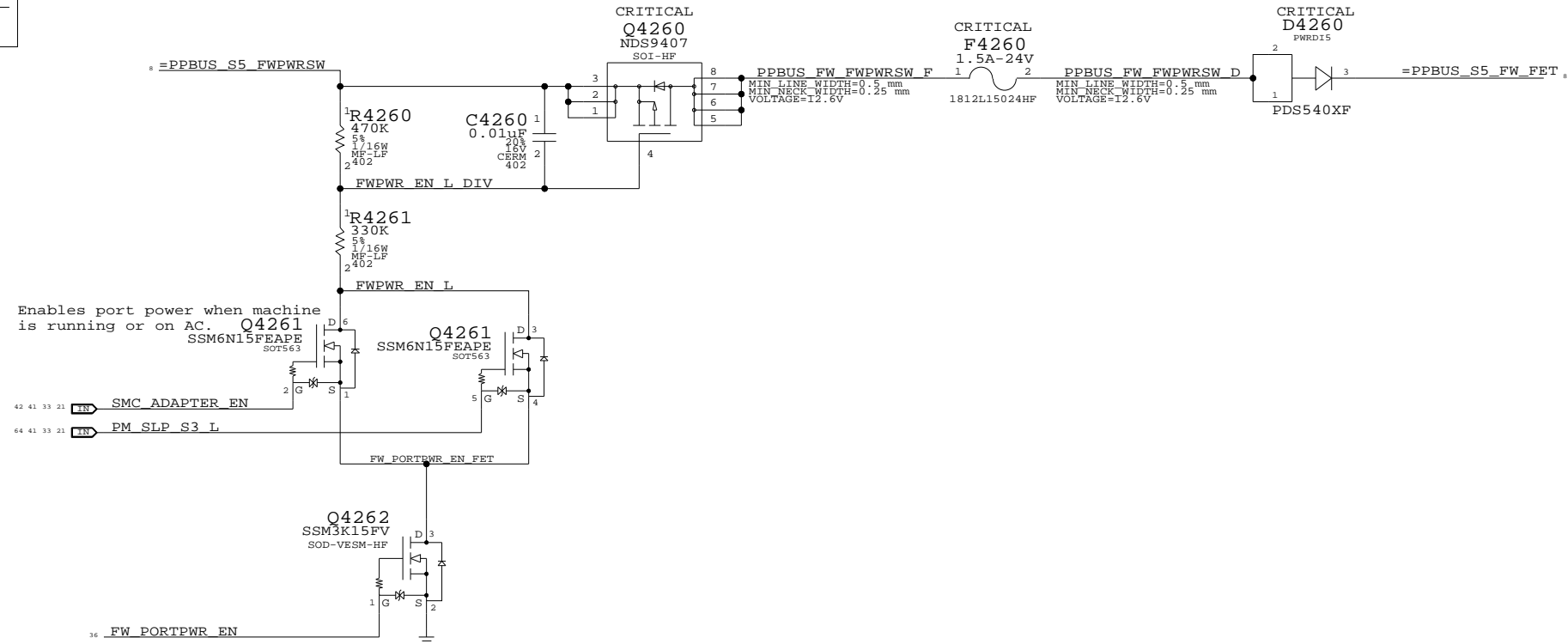
# Page Notes

Power aliases required by this page:  
 - =PPBUS\_S5\_FWPWR SW (system supply for bus power)  
 - =PP3V3\_FW\_LATEVG\_ACTIVE  
 - =PPVP\_FW\_SUMNODE (power passthru summation node)

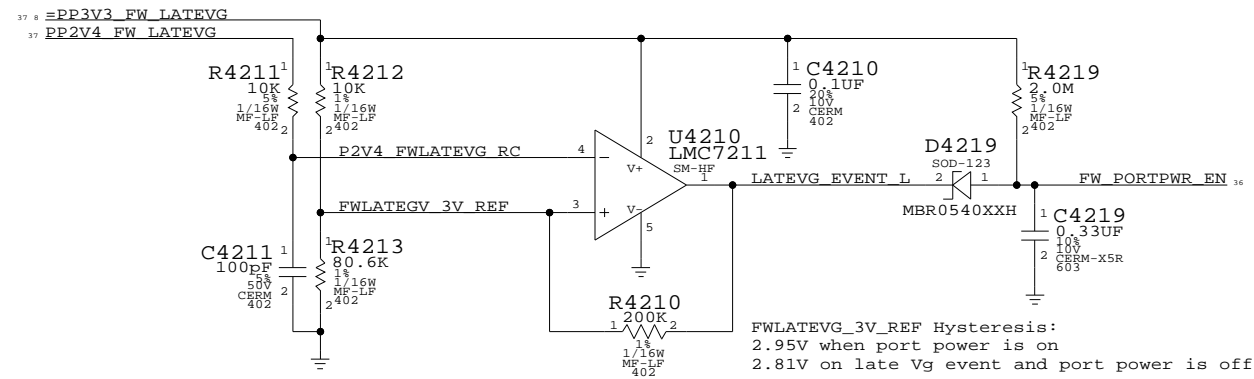
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - FW\_PORT\_FAULT\_PU

## FireWire Port Power Switch



## Late-VG Event Detection

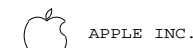


### FireWire Port Power

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	36	76

# Page Notes

Power aliases required by this page:  
 - =PPVP\_FW\_PORT1  
 - =PP3V3\_FW\_LATEVG

Signal aliases required by this page:  
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

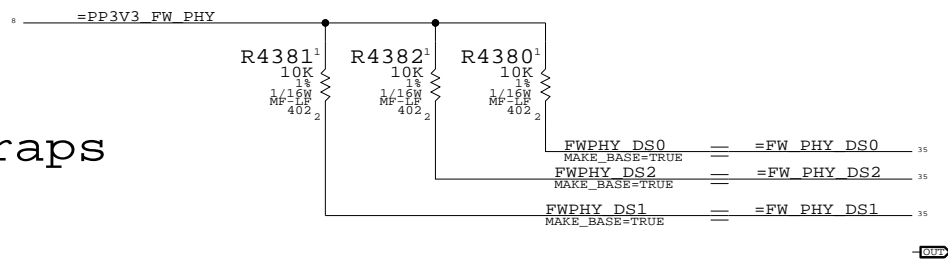
BOM options provided by this page:  
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

## FireWire PHY Config Straps

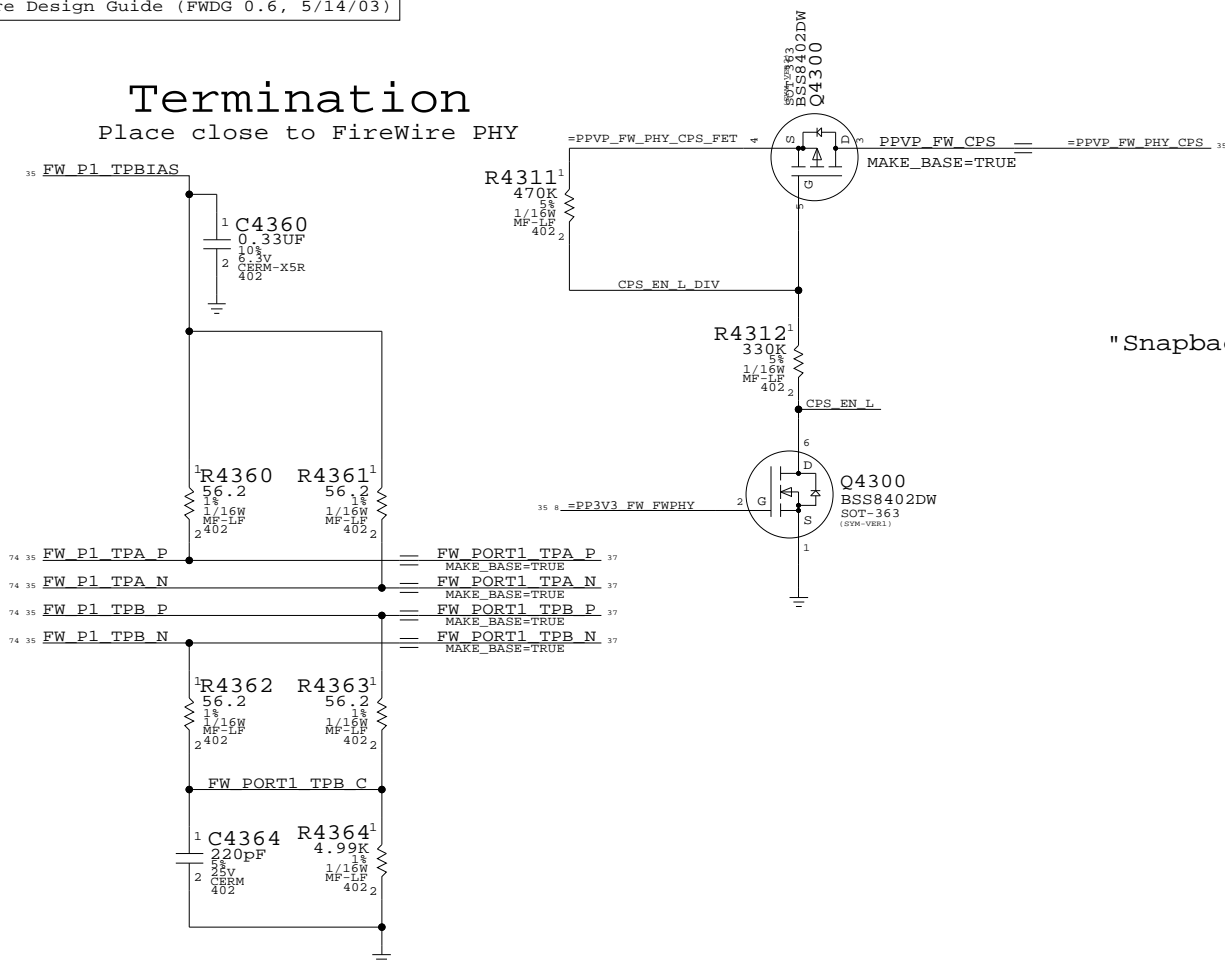
Configures PHY for:  
 - 1-port Portable Power Class (0)



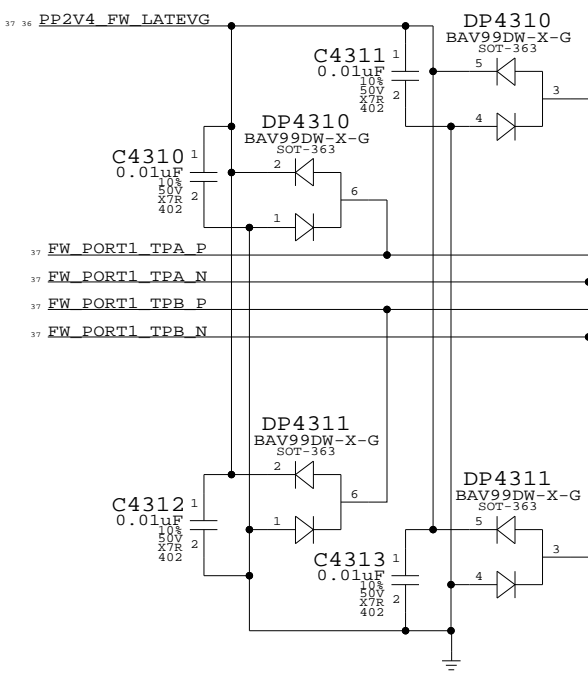
35	FW_P0_TPBIAS	==	NC_FW0_TPBIAS	MAKE_BASE=TRUE
35	FW_P2_TPBIAS	==	NC_FW2_TPBIAS	MAKE_BASE=TRUE
74	FW_P0_TPA_N	==	NC_FW0_TPAN	MAKE_BASE=TRUE
74	FW_P0_TPA_P	==	NC_FW0_TPAP	MAKE_BASE=TRUE
35	FW_P2_TPA_N	==	NC_FW2_TPAN	MAKE_BASE=TRUE
35	FW_P2_TPA_P	==	NC_FW2_TPAP	MAKE_BASE=TRUE
74	FW_P0_TPB_N	==	NC_FW0_TPNB	MAKE_BASE=TRUE
35	FW_P0_TPB_P	==	NC_FW0_TPNP	MAKE_BASE=TRUE
35	FW_P2_TPB_N	==	NC_FW2_TPNB	MAKE_BASE=TRUE
35	FW_P2_TPB_P	==	NC_FW2_TPNP	MAKE_BASE=TRUE

## Termination

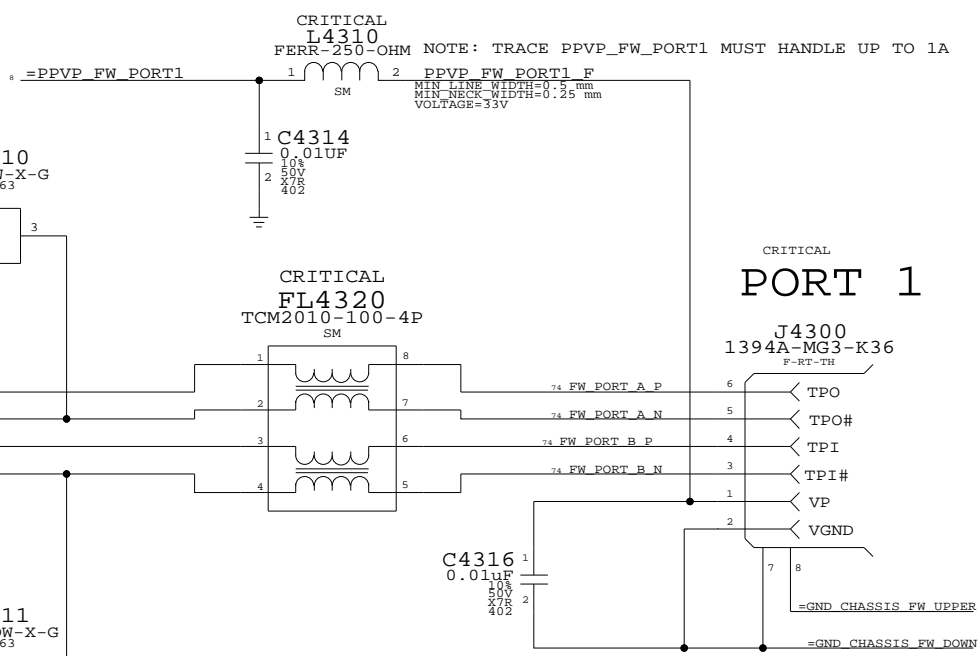
Place close to FireWire PHY



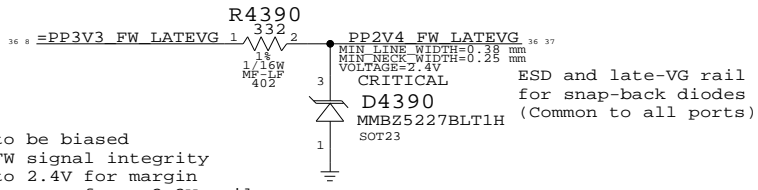
## "Snapback" & "Late VG" Protection



## Cable Power



## Late-VG Protection Power



PP2V4\_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin. R4390 should be 390 Ohms max for a 3.3V rail.

FireWire Ports		
SYNC_MASTER=K36B_MLB	SYNC_DATE=(MASTER)	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	37		

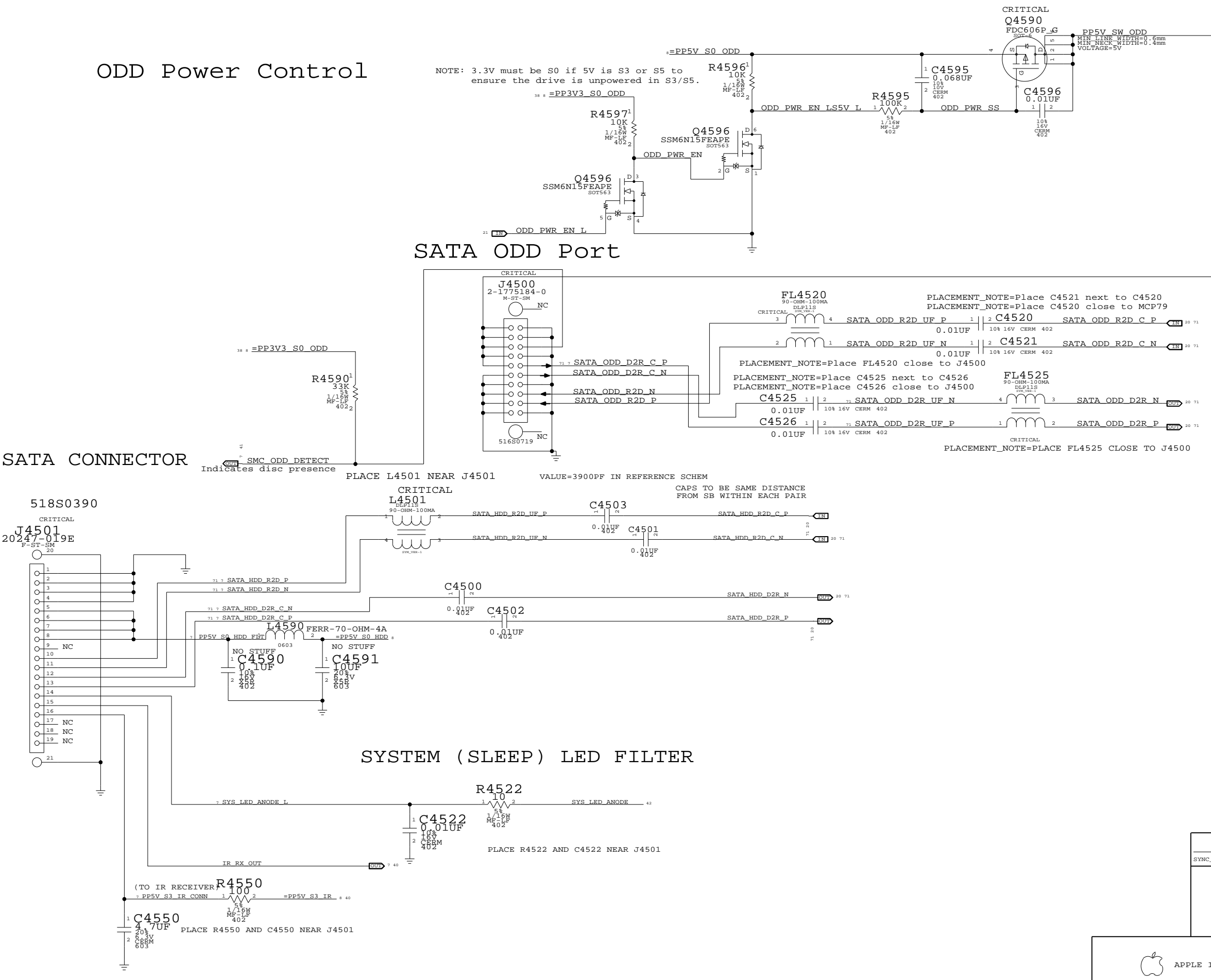
# ODD Power Control

NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

## SATA ODD Port

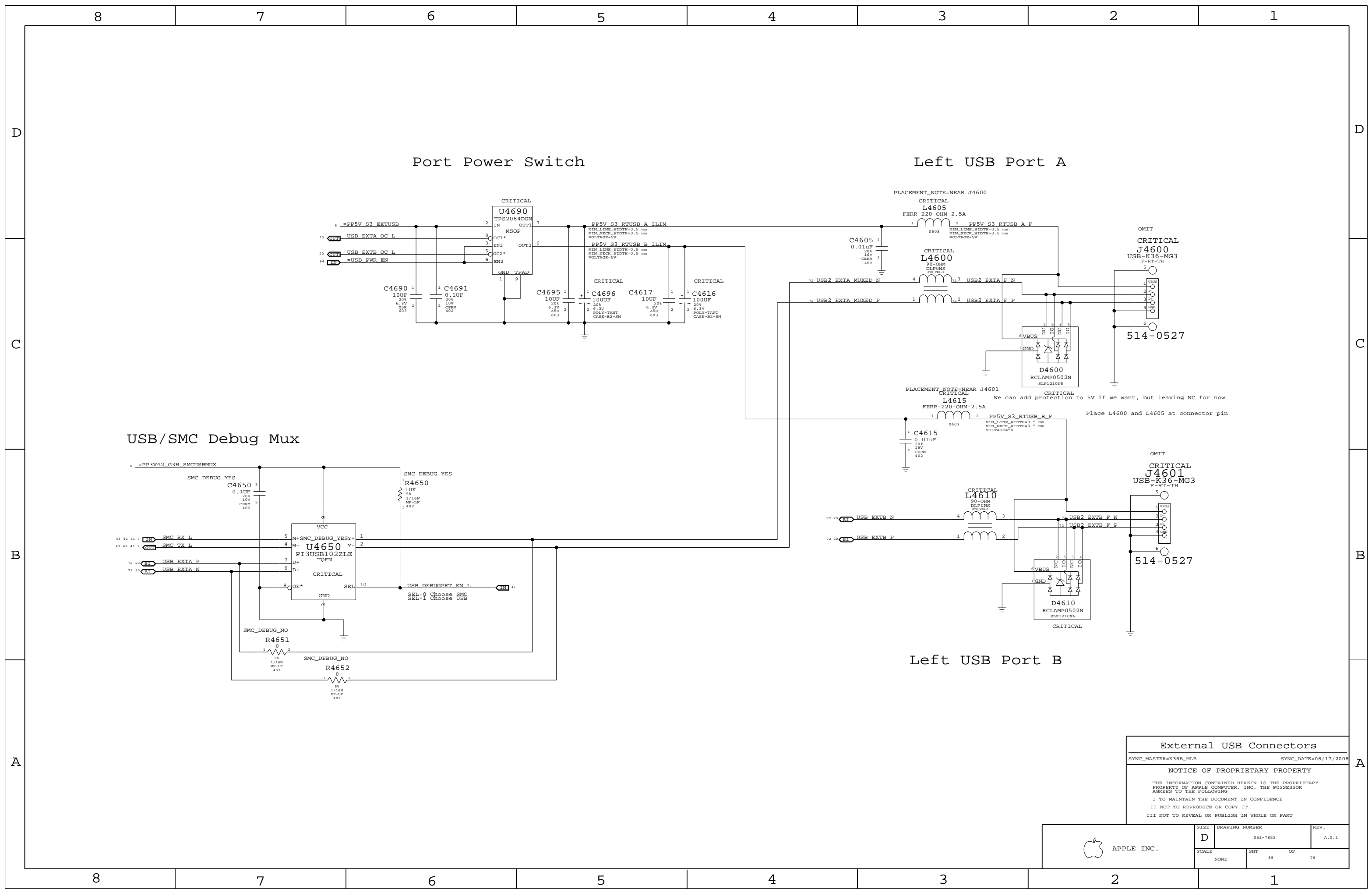
## SATA CONNECTOR

## SYSTEM (SLEEP) LED FILTER



SATA Connectors		
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	38		



Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

**External USB Connectors**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	39		

D

D

C

C

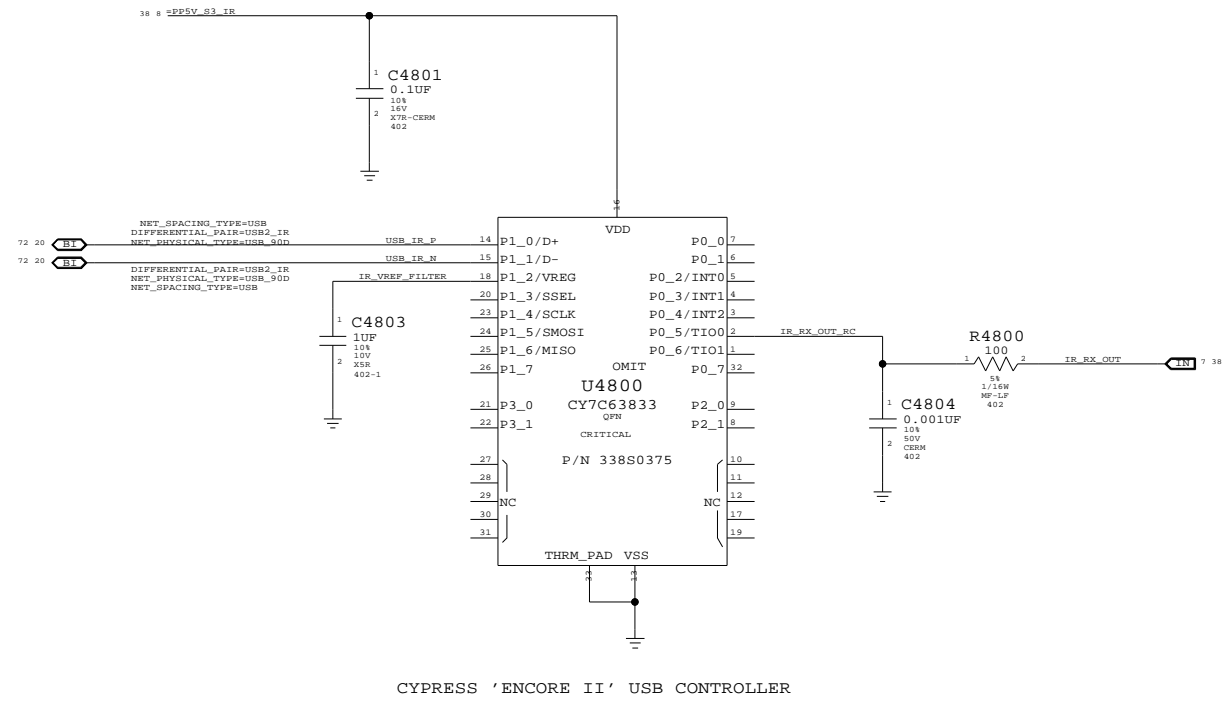
B

B

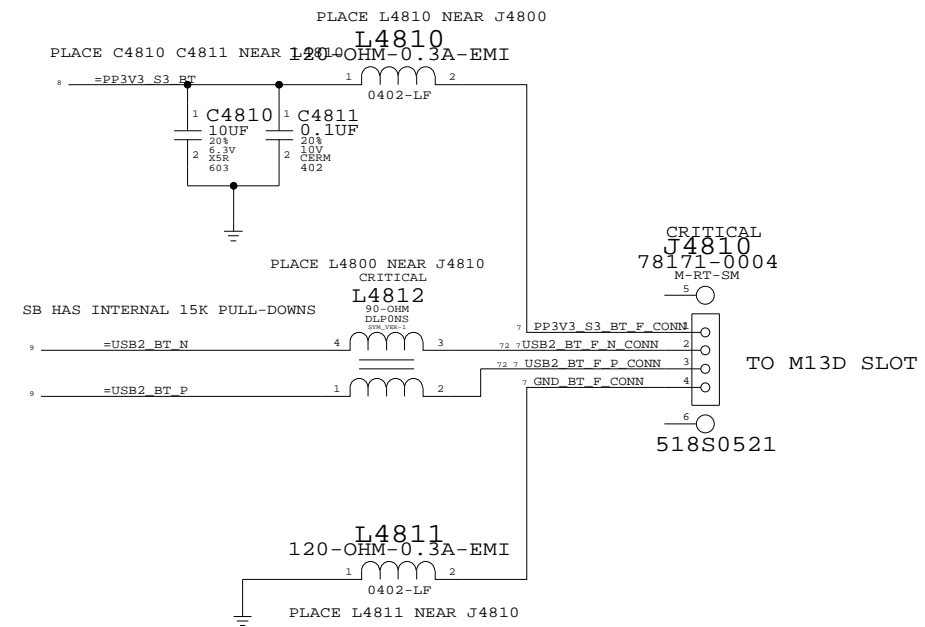
A

A

### IR CTRL



### BLUETOOTH

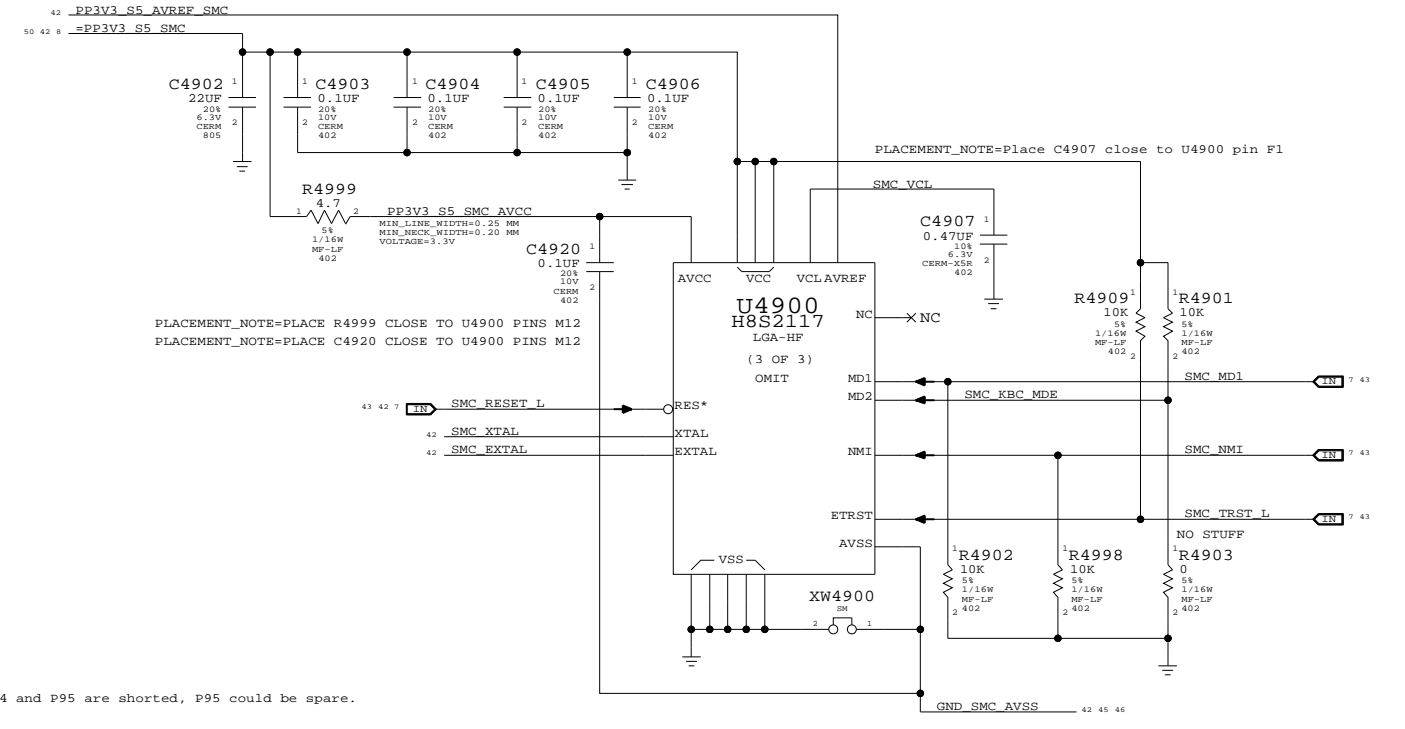
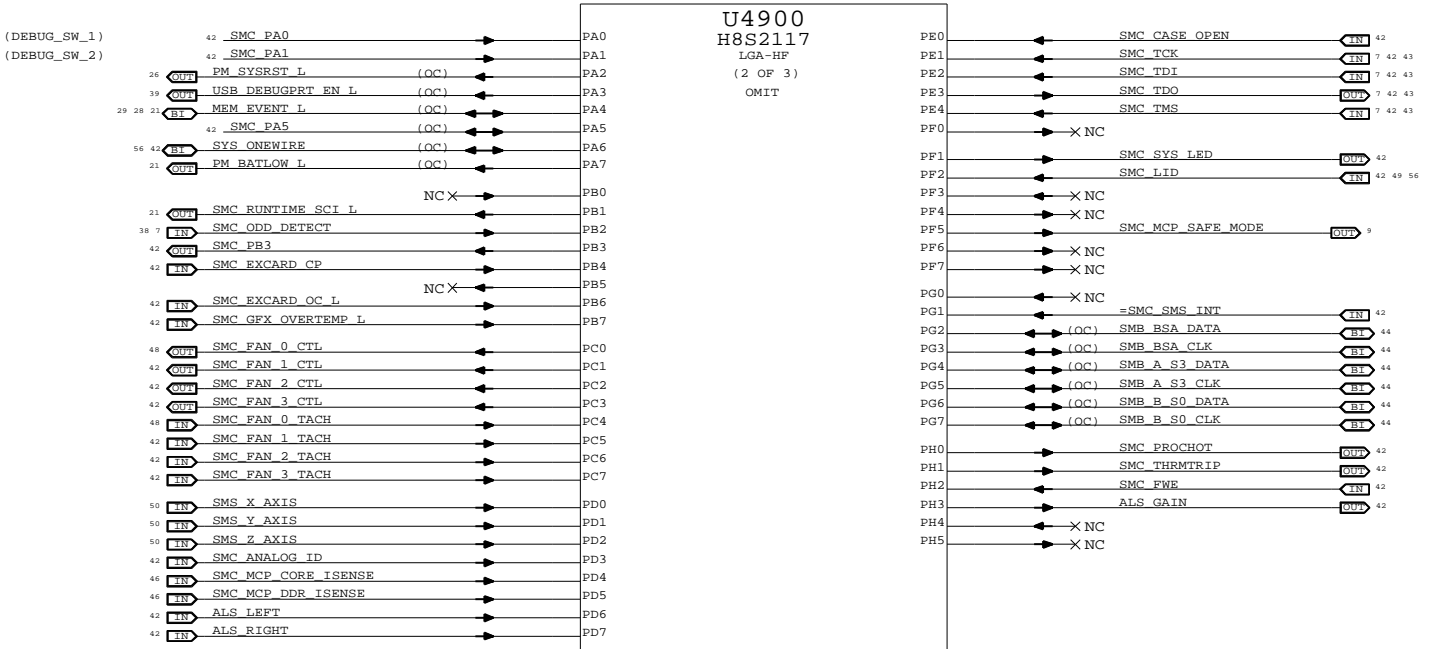
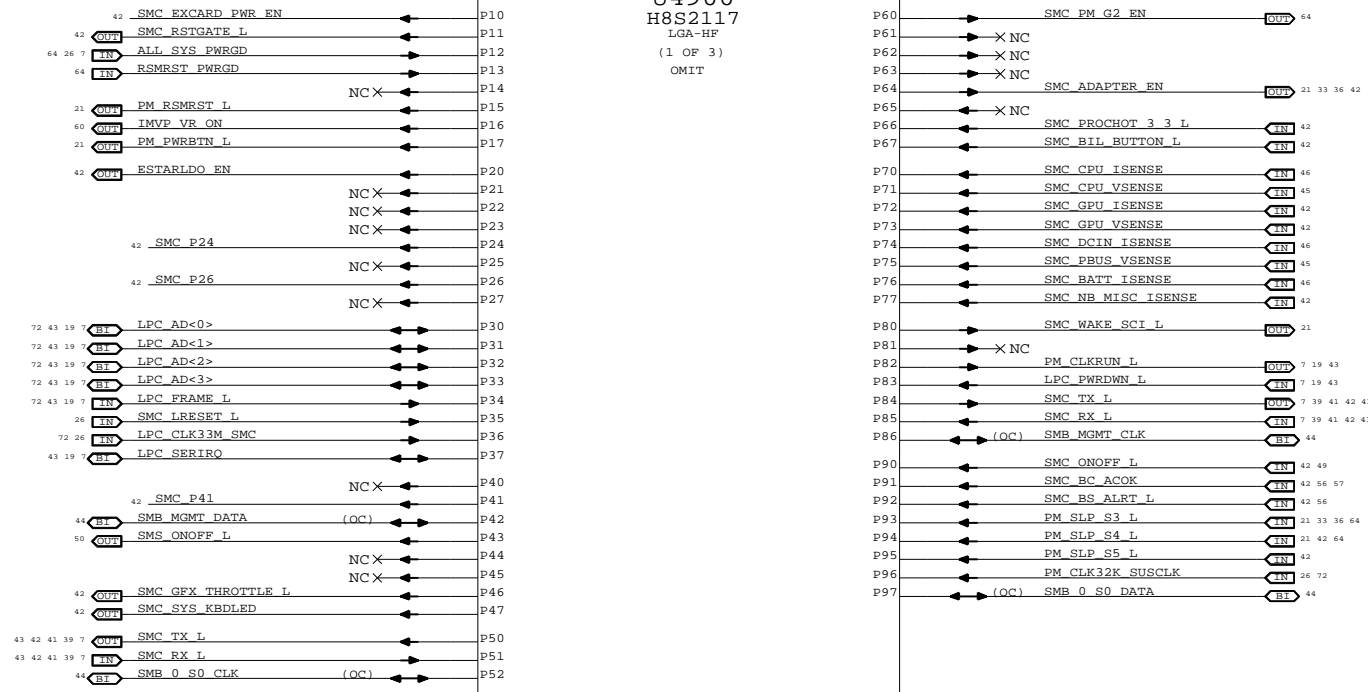


Front Flex Support  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=07/17/2008  
 NOTICE OF PROPRIETARY PROPERTY  
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	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT		OF
NONE	40		76



NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



PLACEMENT\_NOTE=PLACE R4999 CLOSE TO U4900 PINS M12  
 PLACEMENT\_NOTE=PLACE C4920 CLOSE TO U4900 PINS M12

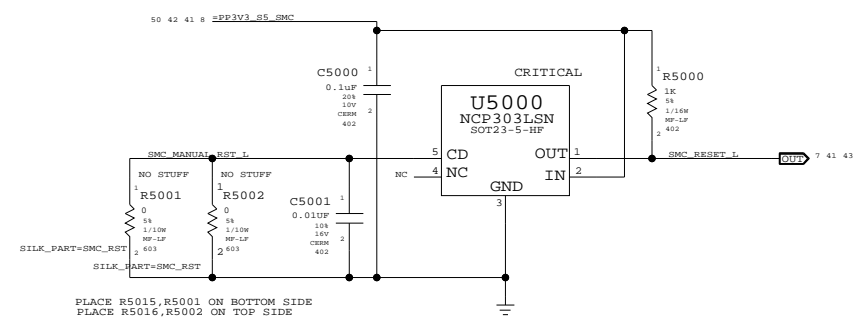
NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS interrupt can be active high or low, rename net accordingly.  
 If SMS interrupt is not used, pull up to SMC rail.

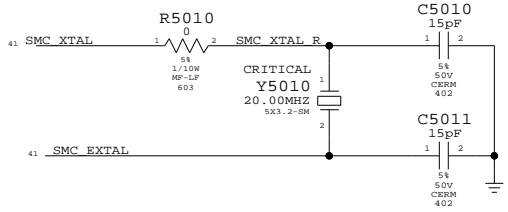
SMC  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT OF		76
NONE	41		

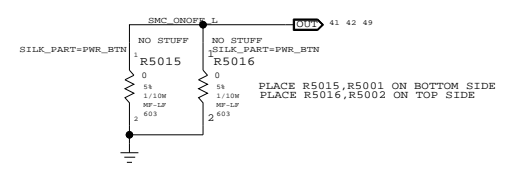
SMC Reset "Button" / Brownout Detect



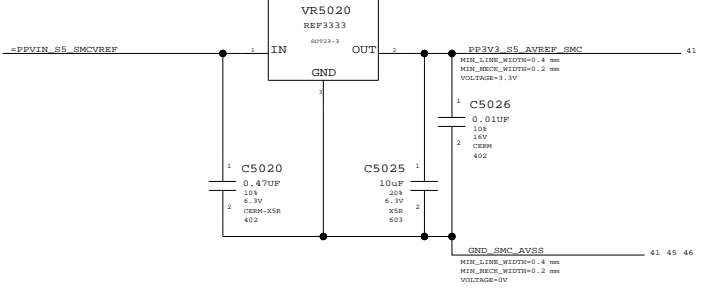
SMC Crystal Circuit



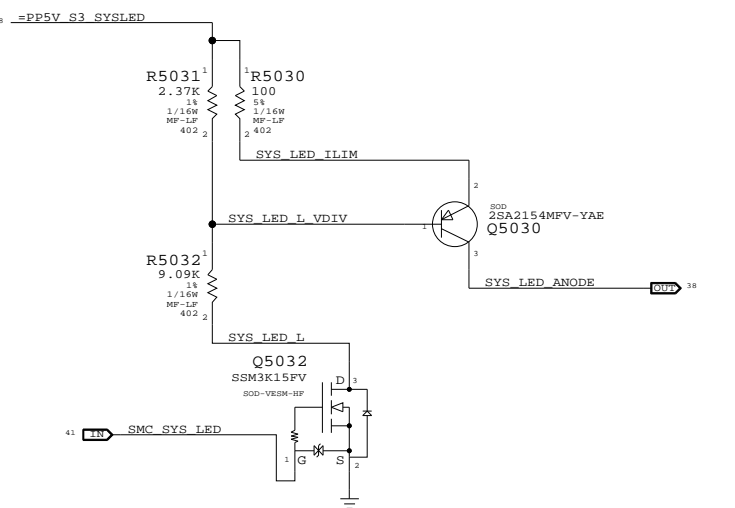
Debug Power "Button"



SMC AVREF Supply

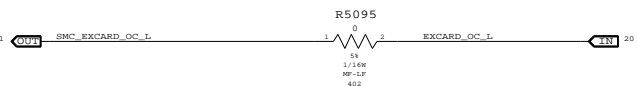
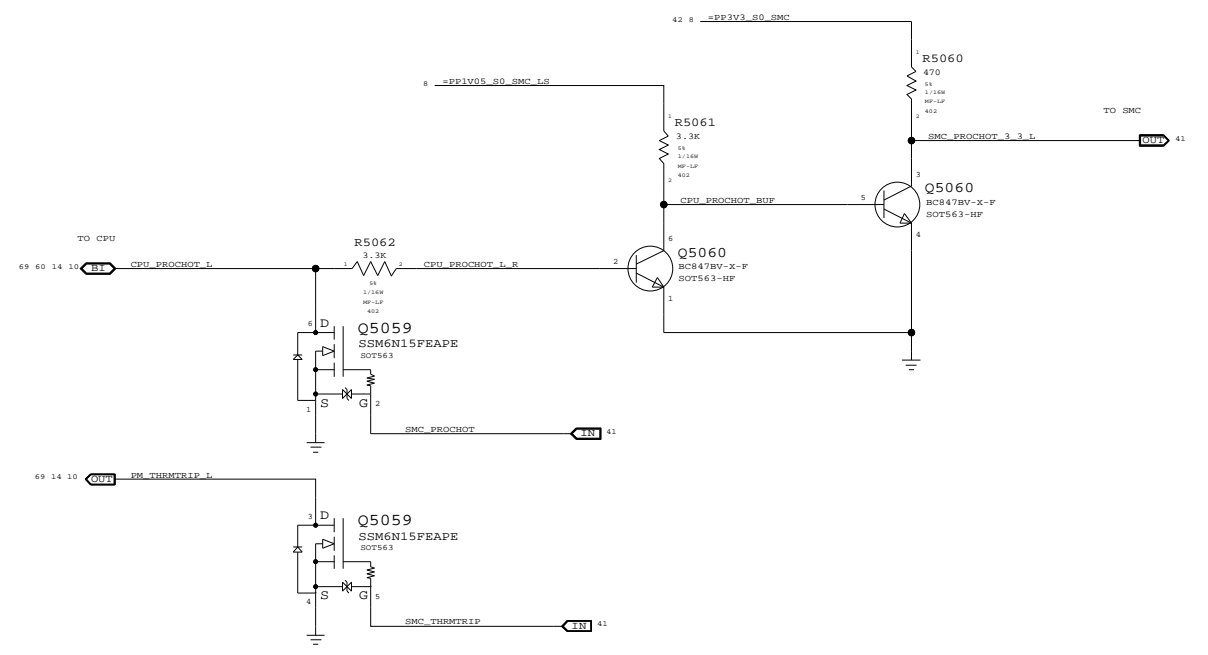


System (Sleep) LED Circuit

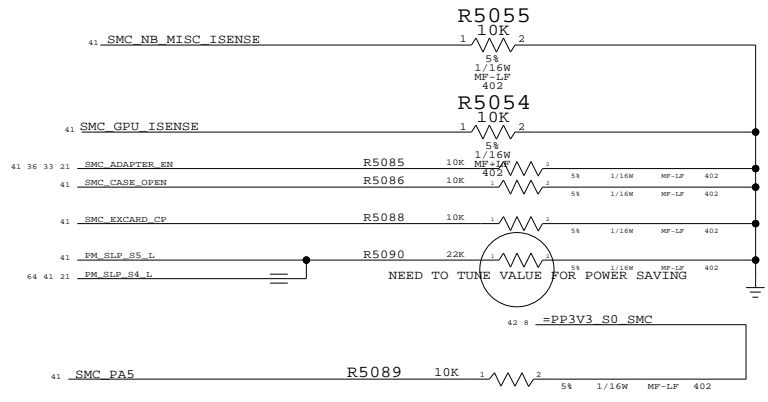


41	_SMC_FAN_1_CTL	==	NC_SMC_FAN_1_CTL	41	_SMC_PB3	==	NC_SMC_PB3		
41	_SMC_FAN_1_TACH	==	MAKE_BASE=TRUE NO_TEST=TRUE	41	_SMC_P24	==	TP_SMC_P24		
41	_SMC_FAN_2_CTL	==	MAKE_BASE=TRUE NO_TEST=TRUE	41	_SMC_P26	==	MAKE_BASE=TRUE SMC_BROWN_MIX_SEL		
41	_SMC_FAN_2_TACH	==	MAKE_BASE=TRUE NO_TEST=TRUE	41	_SMC_P41	==	TP_SMC_P41		
41	_SMC_FAN_3_CTL	==	MAKE_BASE=TRUE NO_TEST=TRUE	41	_SMC_RSTGATE_L	==	MAKE_BASE=TRUE TP_SMC_RSTGATE_L		
41	_SMC_FAN_3_TACH	==	MAKE_BASE=TRUE NO_TEST=TRUE	41	_SMC_EXCARD_PWR_EN	==	TP_SMC_EXCARD_PWR_EN		
41	_SMC_GFX_OVERTEMP_L	==	TP_SMC_GFX_OVERTEMP_L	41	_ALS_RIGHT	==	NC_ALS_RIGHT		
41	_SMC_GFX_THROTTLE_L	==	SMC_IQ_THROTTLE_L	41	_ESTABLDO_EN	==	NC_ESTABLDO_EN		
57	56	42	_SMC_BC_ACLK	==	MAKE_BASE=TRUE NO_TEST=TRUE	41	_SMC_ANALOG_ID	==	NC_SMC_ANALOG_ID
41	_ALS_GAIN	==	NC_ALS_GAIN	41	_SMC_SYS_FENLDD	==	NC_SMC_SYS_FENLDD		
41				41	_SMC_SMS_INT	==	SMS_INT_L		
41				45	_SMC_MCP_VSENSE	==	SMC_GPU_VSENSE		
41				45	_SMC_CPU_PSB_ISENSE	==	ALS_LEFT		

SMC FSB to 3.3V Level Shifting



41	_SMC_BA0	==	R5091 100K	5A	1/16W	MP-LP	402			
41	_SMC_PA1	==	R5092 100K	5A	1/16W	MP-LP	402			
49	42	41	_SMC_ONOFF_L	==	R5070 10K	5A	1/16W	MP-LP	402	
56	49	41	_SMC_LID	==	R5071 100K	5A	1/16W	MP-LP	402	
41			_SMC_PWR	==	R5072 10K	5A	1/16W	MP-LP	402	
43	41	39	_SMC_TX_L	==	R5073 10K	5A	1/16W	MP-LP	402	
43	41	39	_SMC_RX_L	==	R5074 100K	5A	1/16W	MP-LP	402	
56	41		_SYS_ONWIRE	==	R5075 2.0K	5A	1/16W	MP-LP	402	
56	41		_SMC_BS_ALERT_L	==	R5076 100K	5A	1/16W	MP-LP	402	
43	41	7	_SMC_TMS	==	R5077 10K	5A	1/16W	MP-LP	402	
43	41	7	_SMC_TDO	==	R5078 10K	5A	1/16W	MP-LP	402	
43	41	7	_SMC_TDI	==	R5079 10K	5A	1/16W	MP-LP	402	
43	41	7	_SMC_TCK	==	R5080 10K	5A	1/16W	MP-LP	402	
41			_SMC_BTN_BUTTON_L	==	R5081 10K	5A	1/16W	MP-LP	402	
57	56	42	41	_SMC_BC_ACLK	==	R5087 470K	5A	1/16W	MP-LP	402

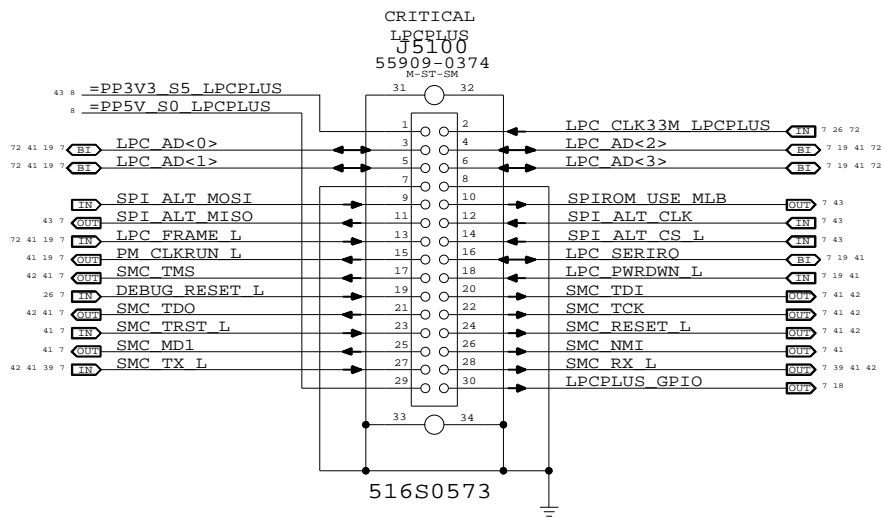


ADD NC ALIASES FOR FAN1 SIGNALS

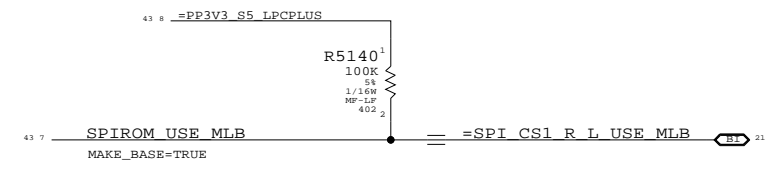
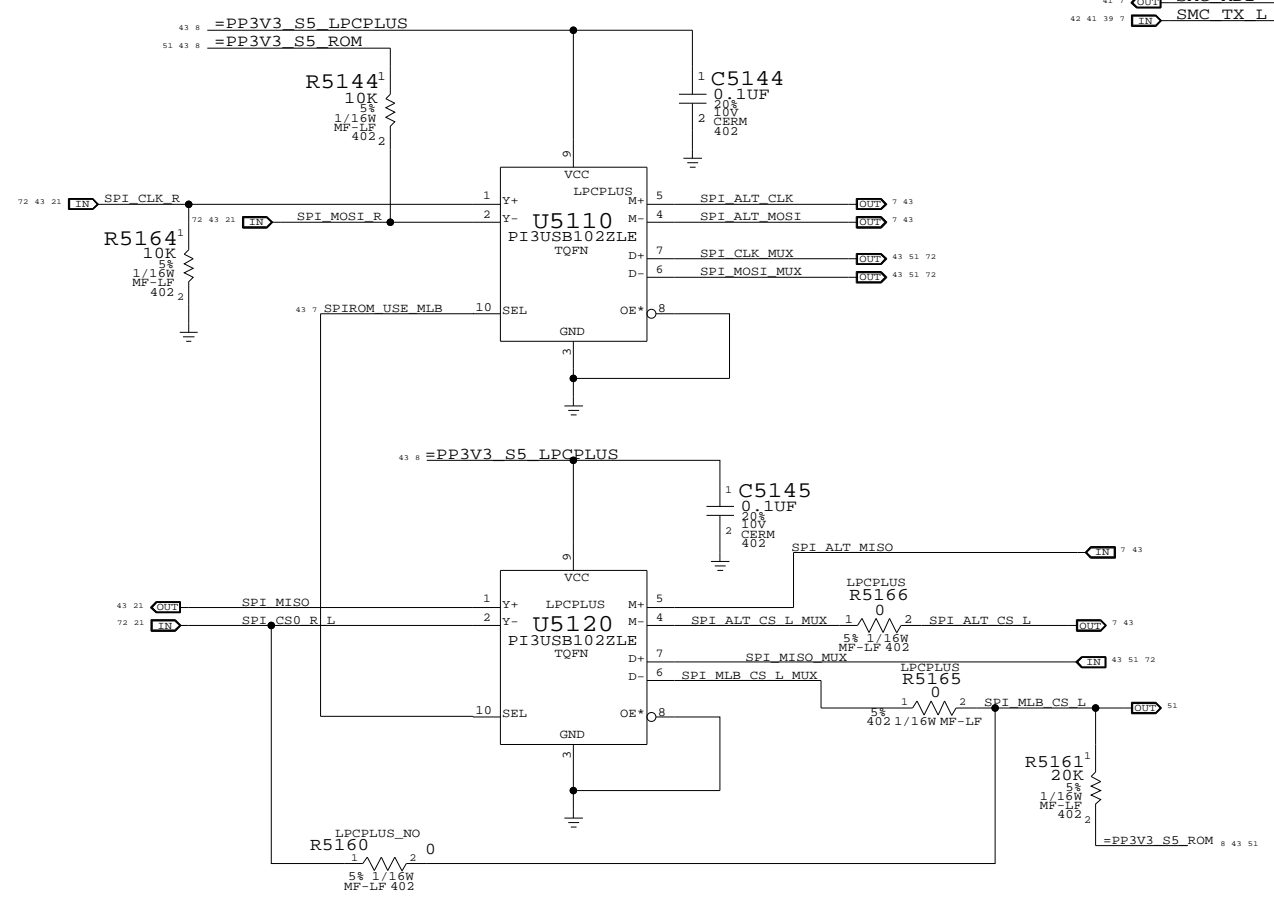
SMC Support  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	42		

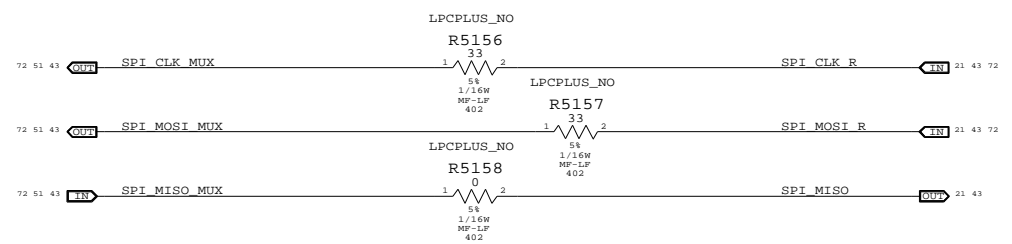
# LPC+SPI Connector



## Alternate SPI ROM Support

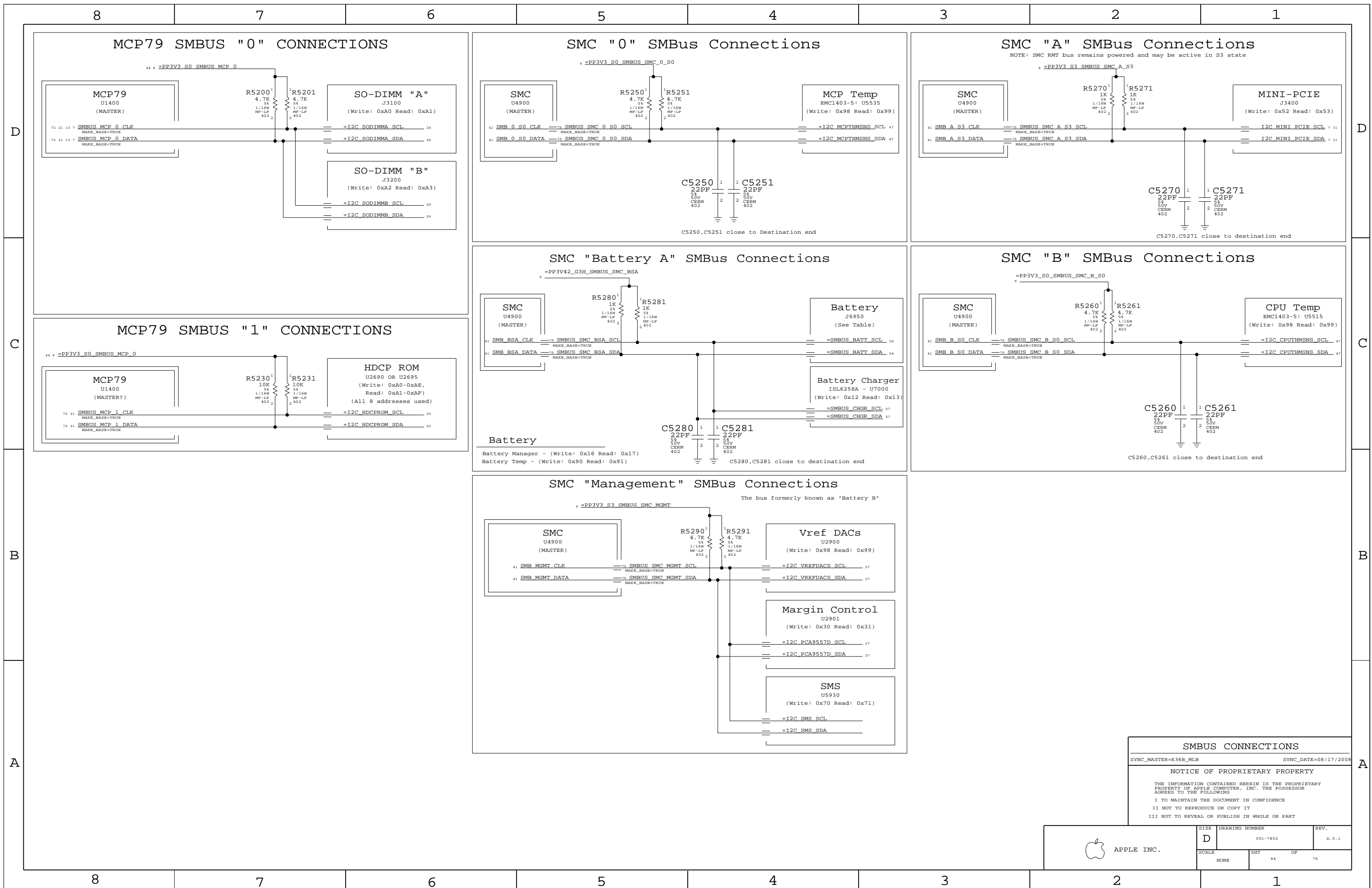


## SPI Bus Series Resistance Option



**LPC+SPI Debug Connector**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT		OF
NONE	43		76



**SMBUS CONNECTIONS**

SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

**NOTICE OF PROPRIETARY PROPERTY**

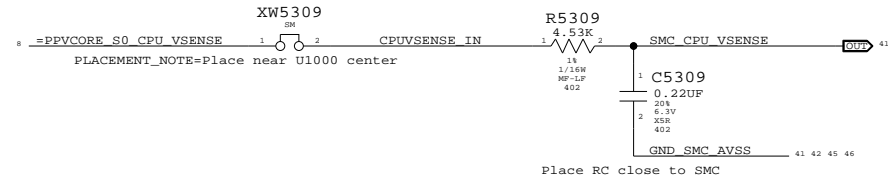
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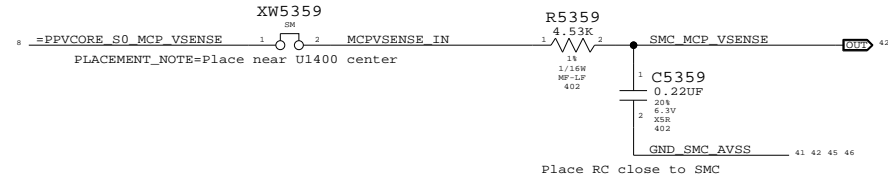
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	44		

8 7 6 5 4 3 2 1

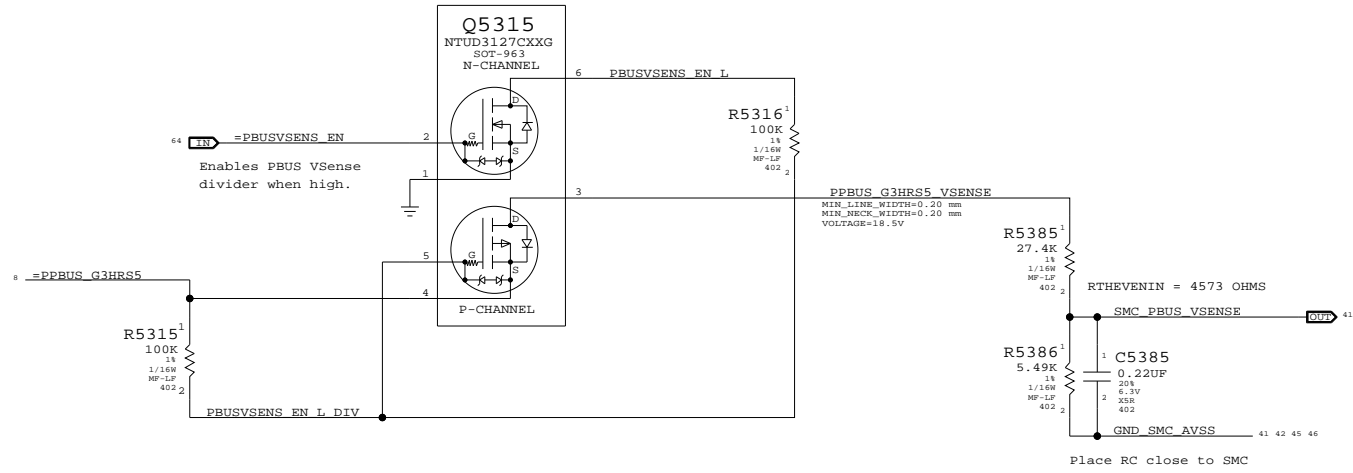
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER

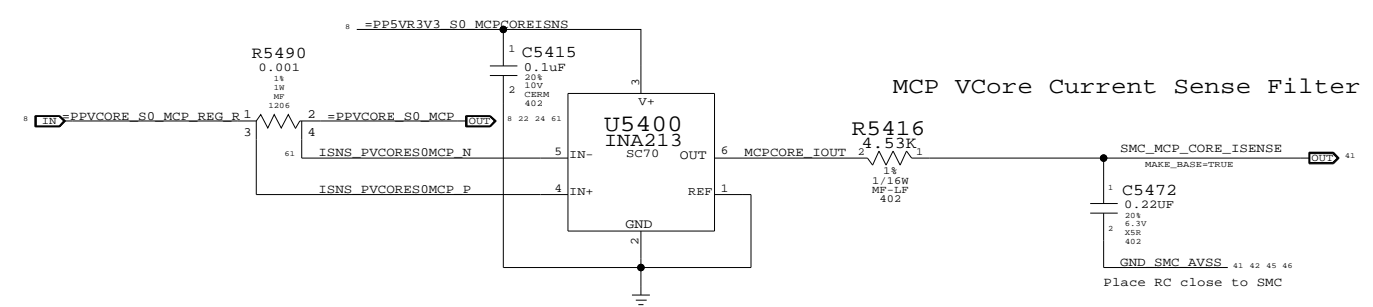


VOLTAGE SENSING  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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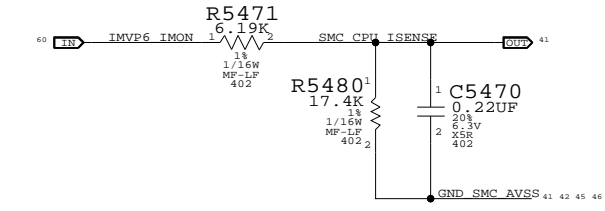
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	45		

8 7 6 5 4 3 2 1

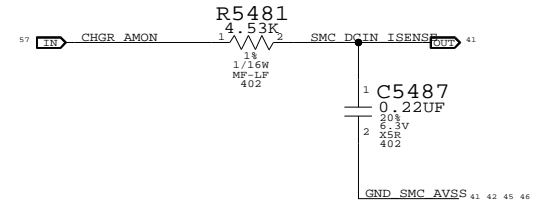
MCP VCore Current Sense



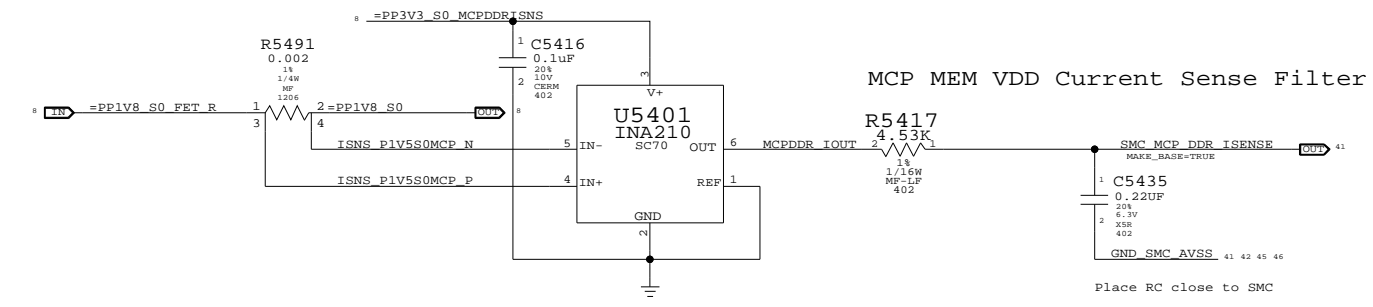
CPU VCore Load Side Current Sensor / Filter



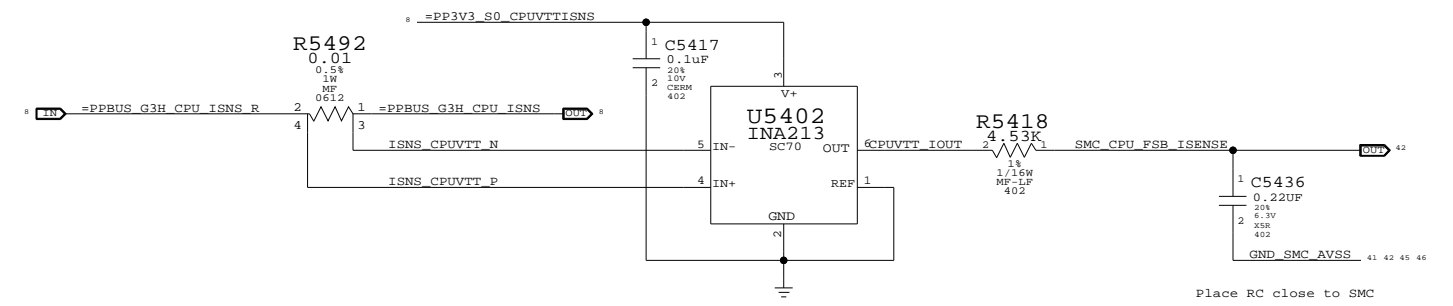
DC-IN (AMON) Current Sense



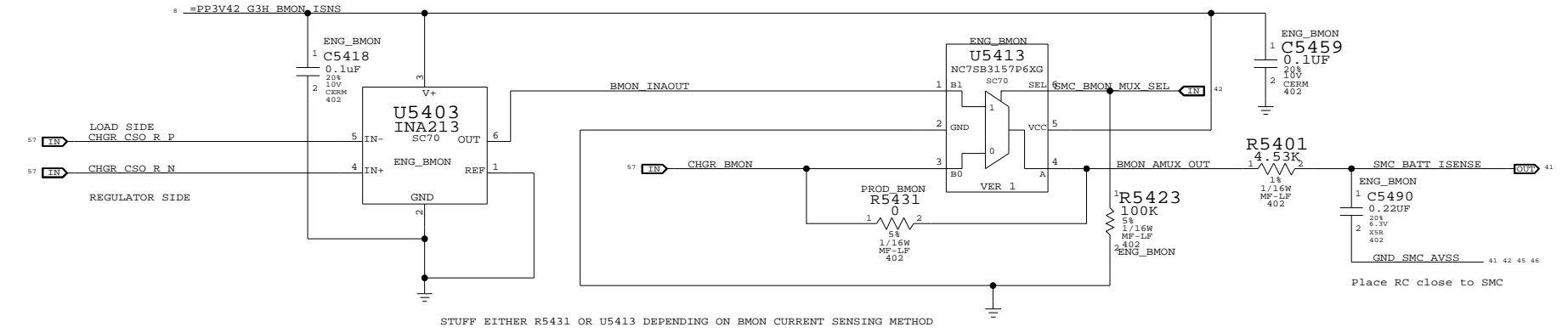
MCP MEM VDD Current Sense



CPU 1.05V Current Sense



CHARGER BMON Current Sense



**Current Sensing**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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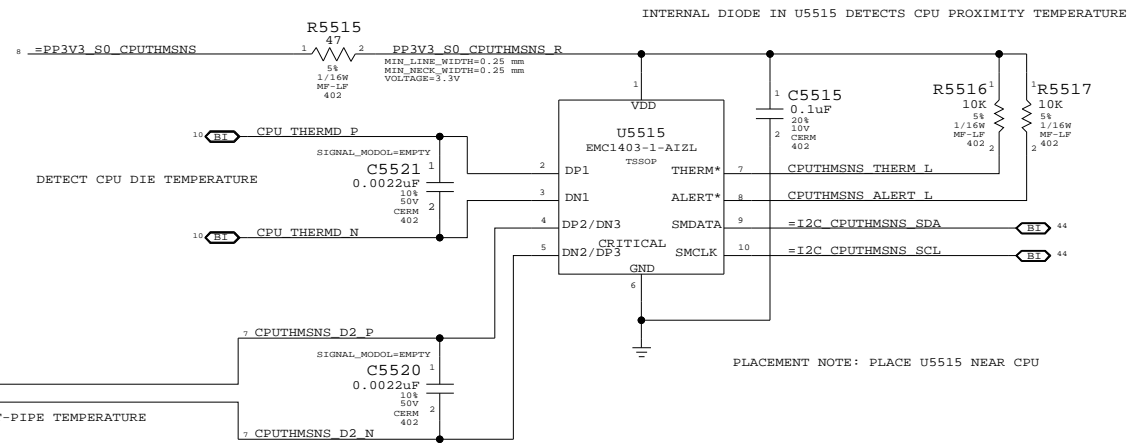
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

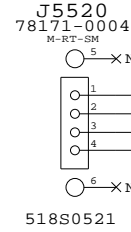
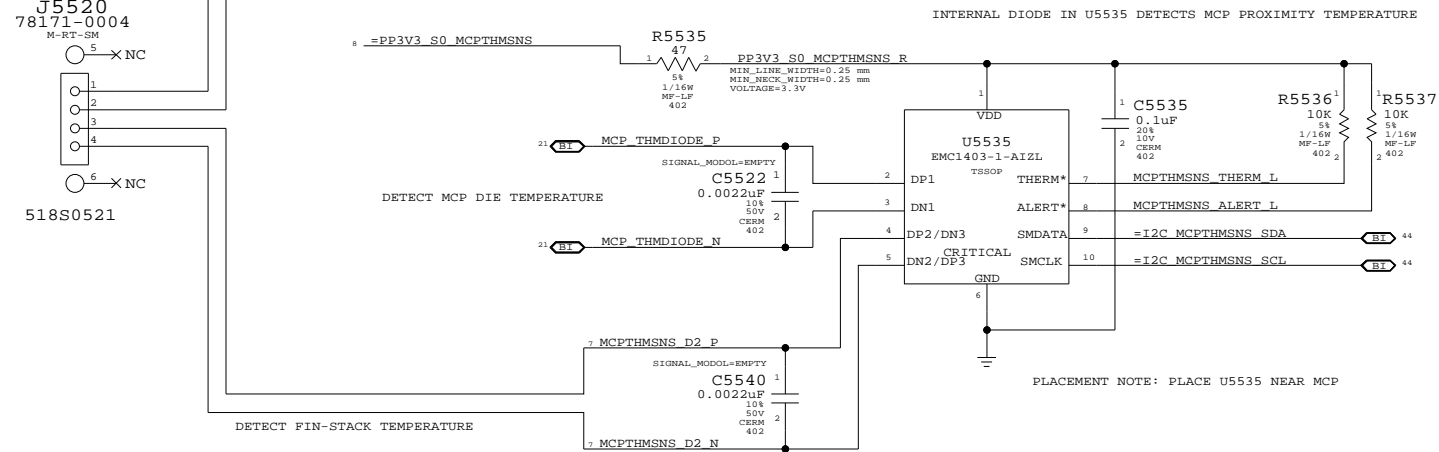
	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	REV.
NONE	46	76	

8 7 6 5 4 3 2 1

### CPU T-Diode Thermal Sensor



### MCP T-Diode Thermal Sensor



Thermal Sensors

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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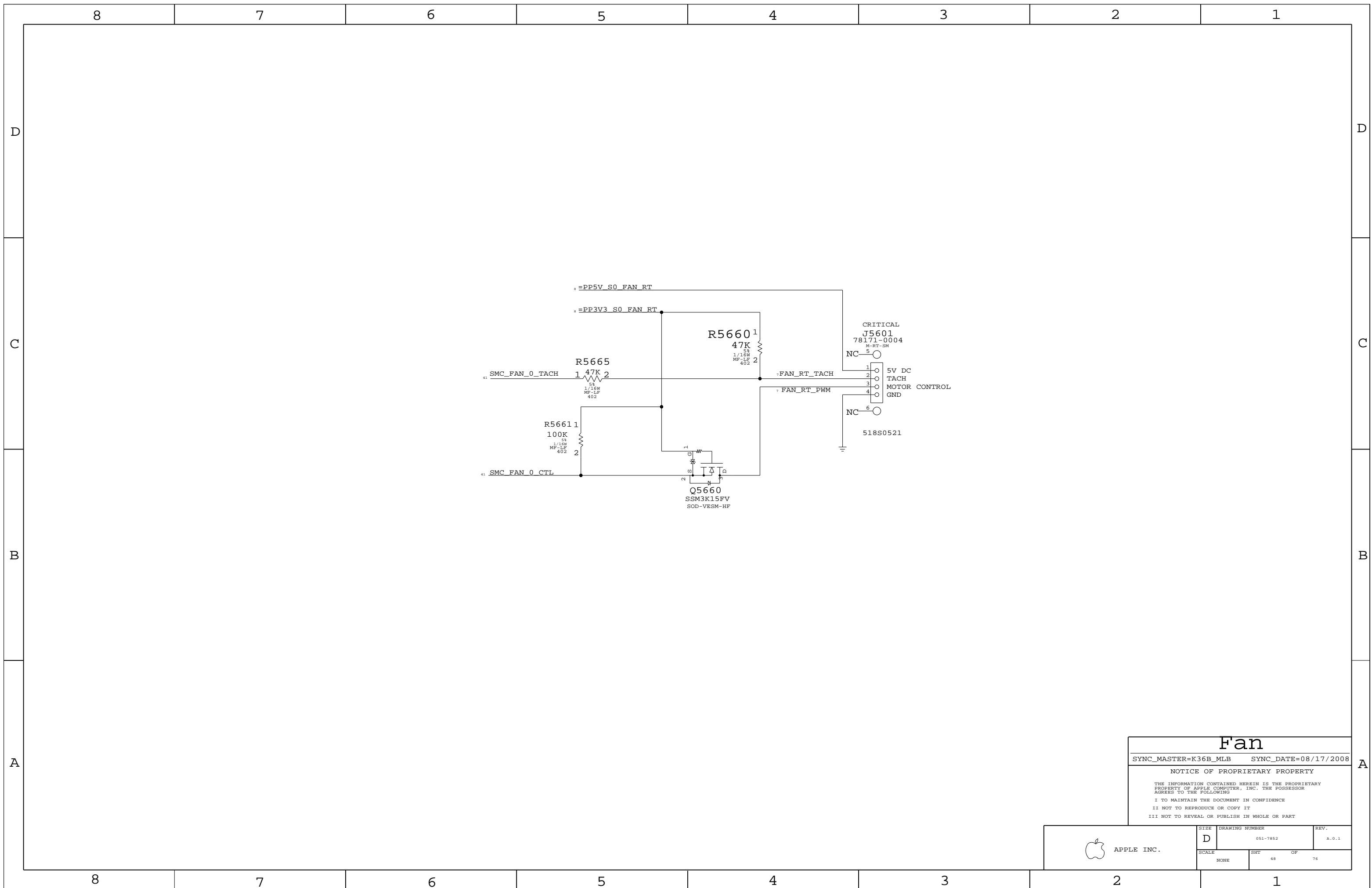
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT OF		
NONE	47 OF		76

8 7 6 5 4 3 2 1



# Fan

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	48	76



8

7

6

5

4

3

2

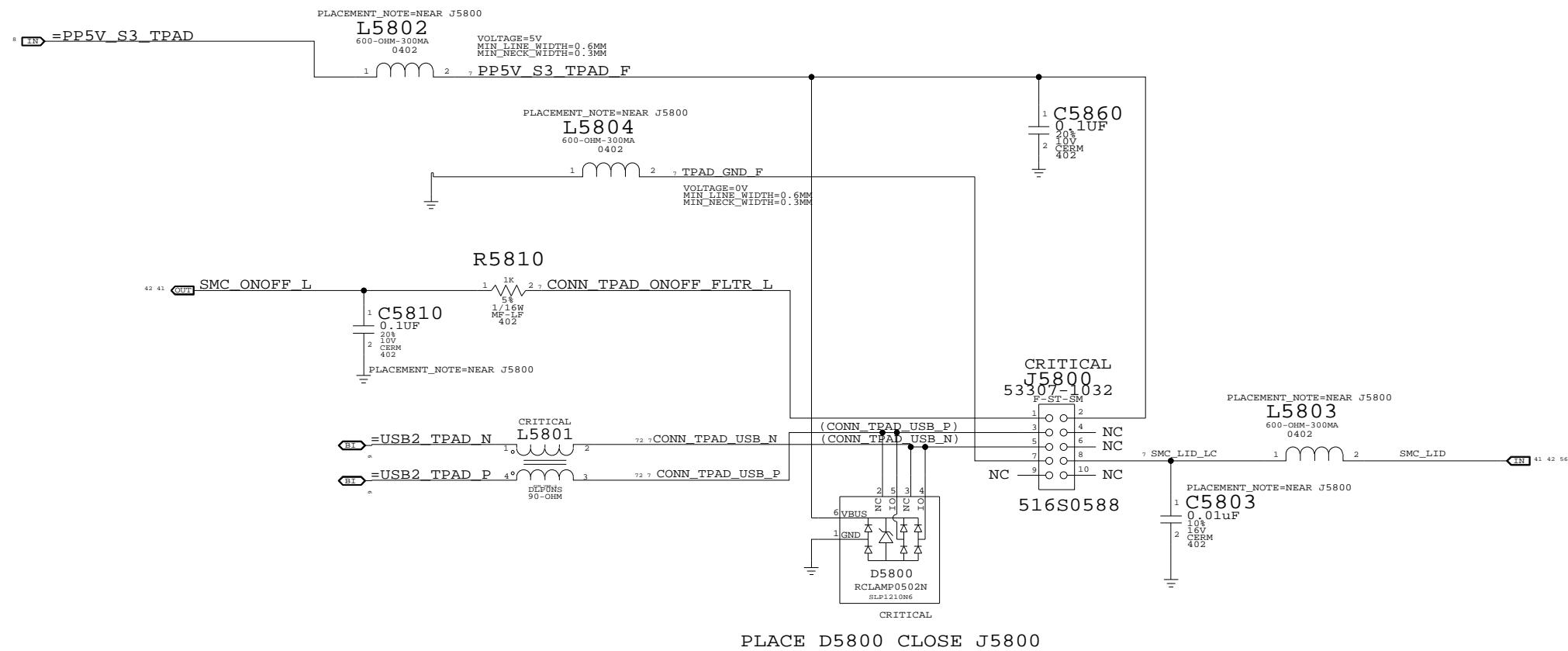
1

- SYNC WITH T18  
- COPY THIS PAGE FROM T18 CSA.58

### PLACEMENT NOTE

PLACE L5800,L5801,L5803 NEAR J5800  
PLACE C5800,C5810,C5803 NEAR J5800  
PLACE D5800 NEAR J5800

# GEYSER




**GEYSER**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	49		

8

7

6

5

4

3

2

1

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

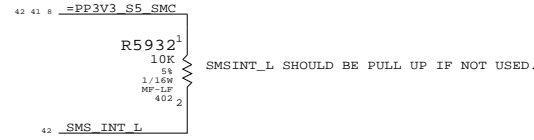
5

4

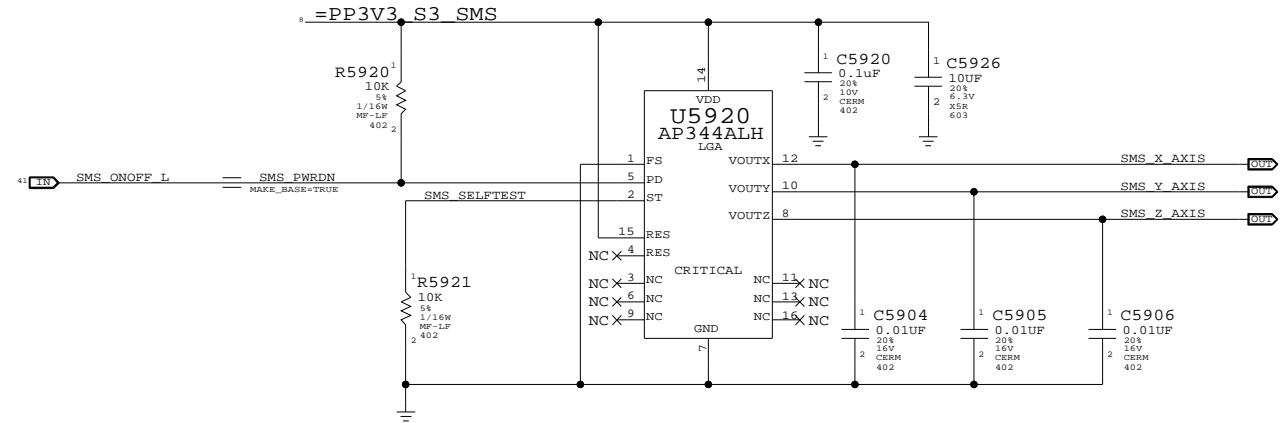
3

2

1

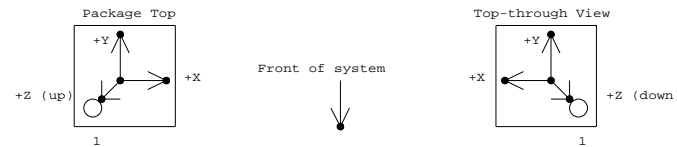


### ANALOG SMS



Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:



### SMS

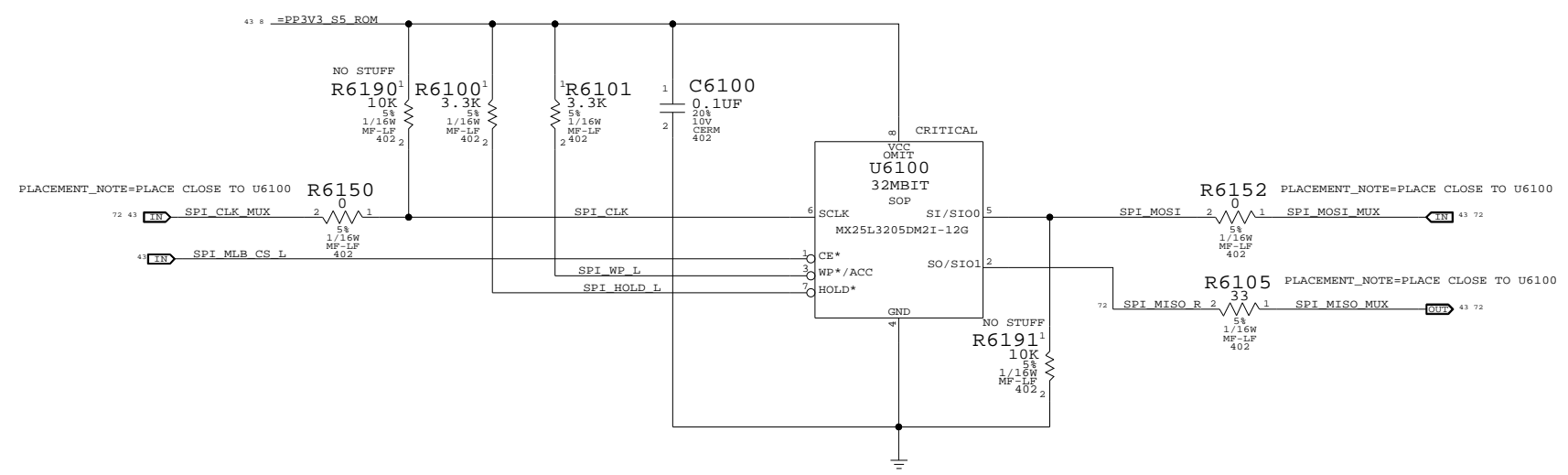
SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	50	76



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHZ IS SELECTED WITH R5164 AND R5144  
 ANY FO THE 4 FREQUENCIES CAN BE SELECTED  
 WITH R6190, R6191, R5164 AND R5144

**SPI ROM**

SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=081/17/2008

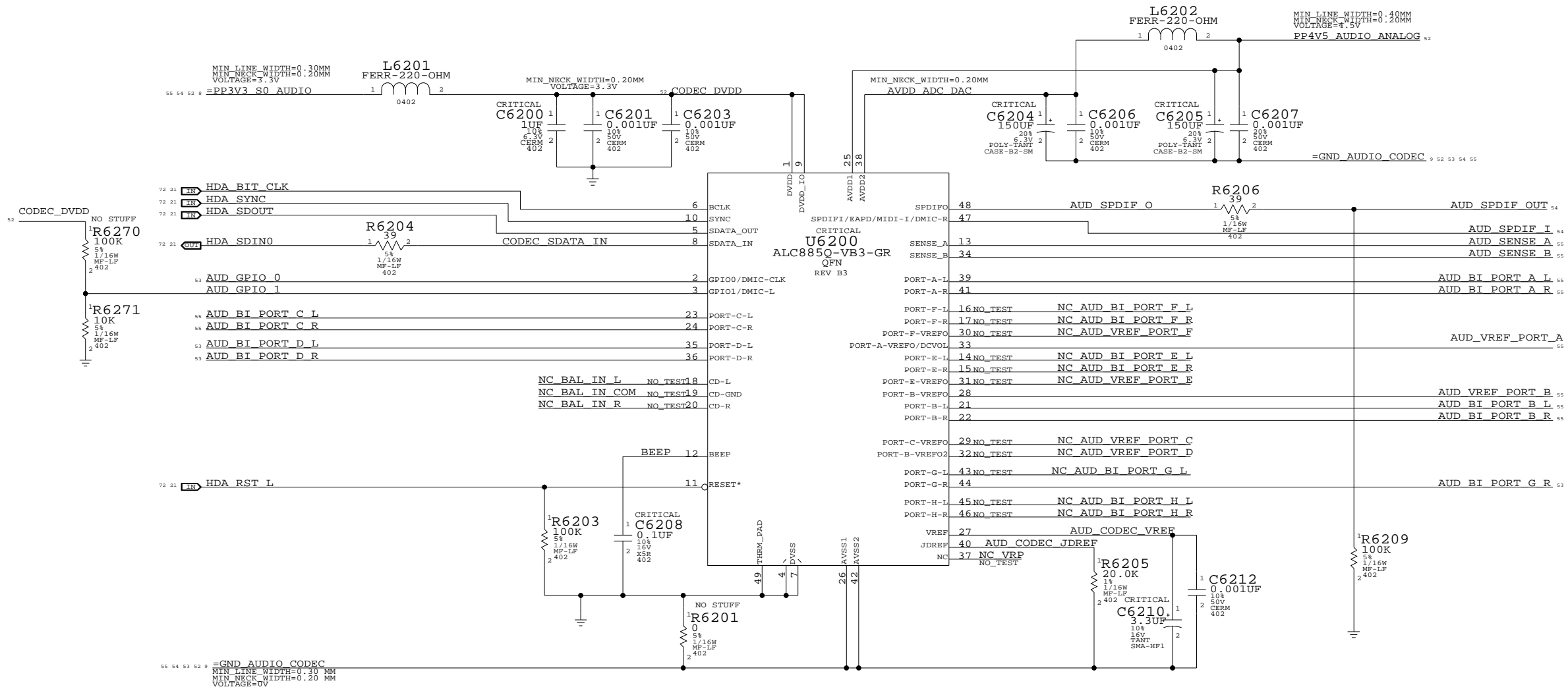
**NOTICE OF PROPRIETARY PROPERTY**

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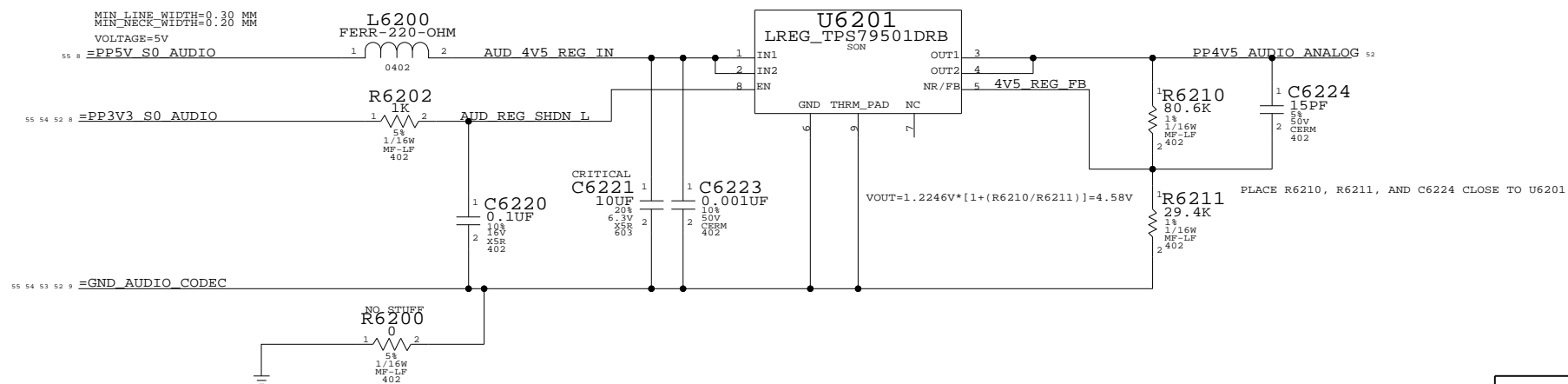
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
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	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	51		

AUDIO CODEC  
APPLE P/N 353S1538



AUDIO 4.5V REGULATOR  
APPLE P/N 353S1576



**AUDIO: CODEC**

SYNC\_MASTER=K36A\_MLB

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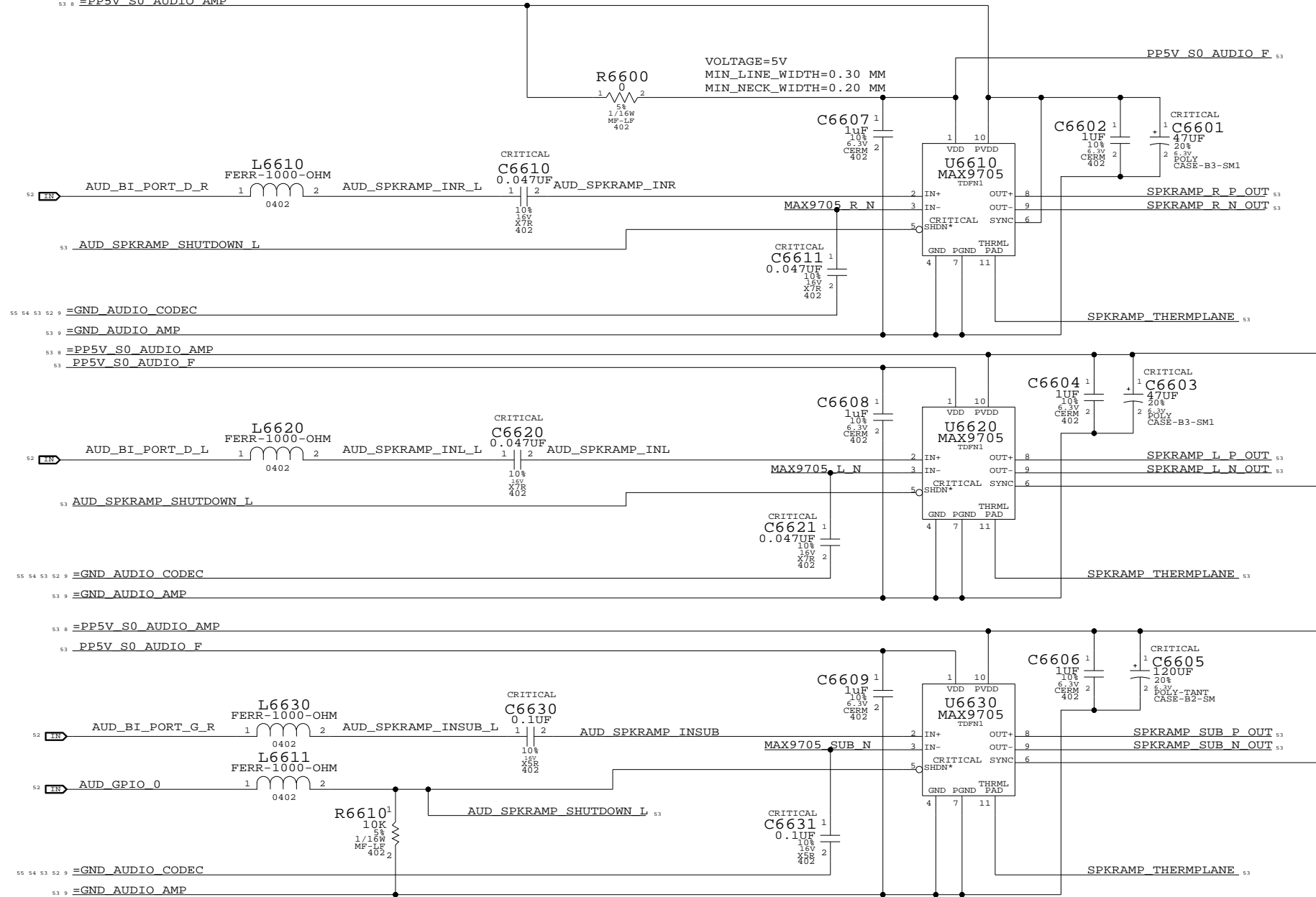
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	52		

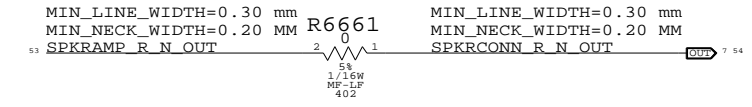
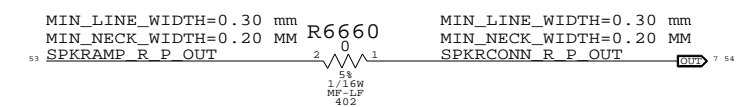
SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ  
 SUB 80 HZ < FC < 132 HZ  
 GAIN 12DB

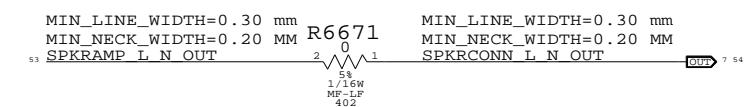
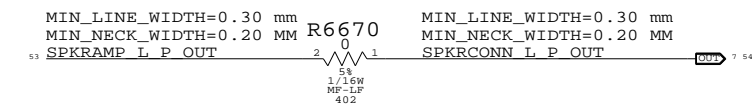
VOLTAGE=5V  
 MIN\_LINE\_WIDTH=0.60 MM  
 MIN\_NECK\_WIDTH=0.20 MM  
 53 9 =PP5V\_S0\_AUDIO\_AMP



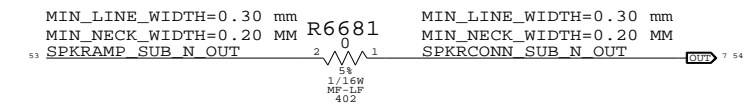
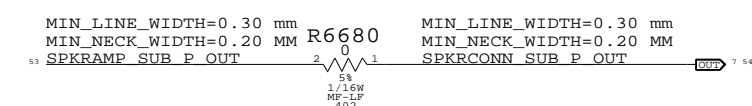
MIN\_LINE\_WIDTH=0.60 MM XW6600  
 MIN\_NECK\_WIDTH=0.20 MM SM  
 53 9 =GND\_AUDIO\_AMP 1 5 2 SPKRAMP\_THERMPLANE 53



RIGHT SATELLITE



LEFT SATELLITE



SUB-TWEETER

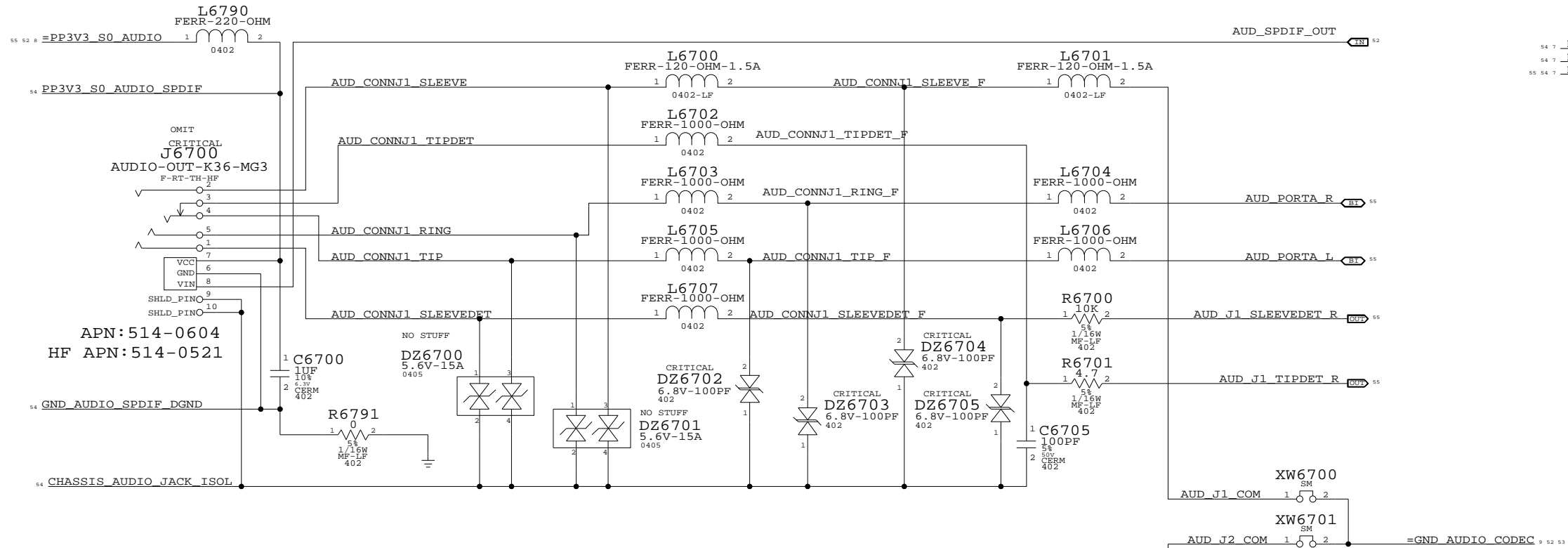
AUDIO: SPEAKER AMP

SYNC\_MASTER=K36A\_MLB SYNC\_DATE=08/29/2008

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	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	53		

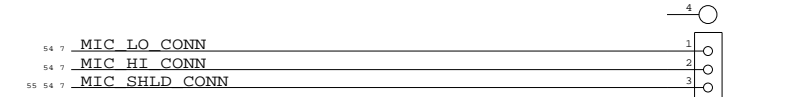
AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX



MIC CONNECTOR

APN: 518S0392

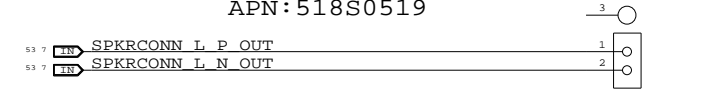
CRITICAL  
J6701  
48227-0301  
M-RT-SM



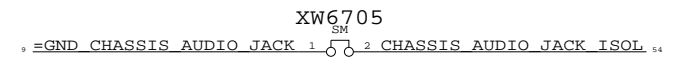
SPEAKER CONNECTOR

APN: 518S0519

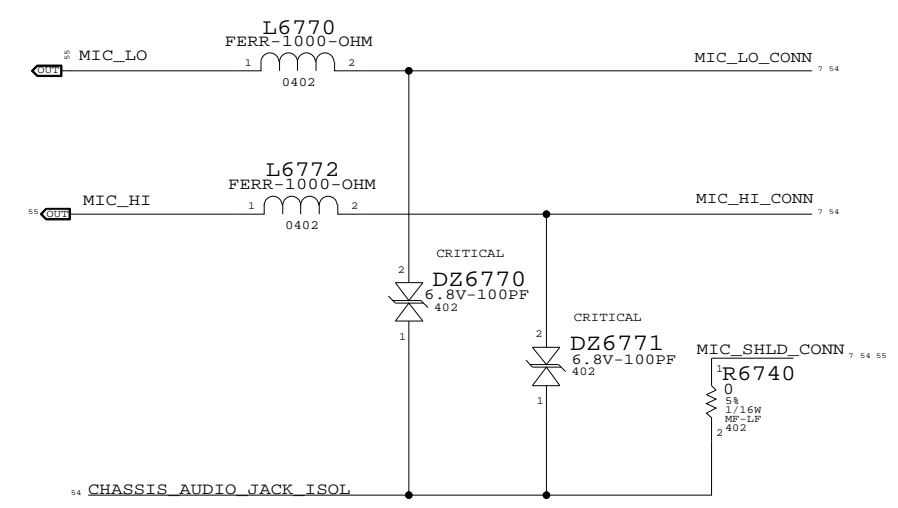
CRITICAL  
J6702  
78171-0002  
M-RT-SM



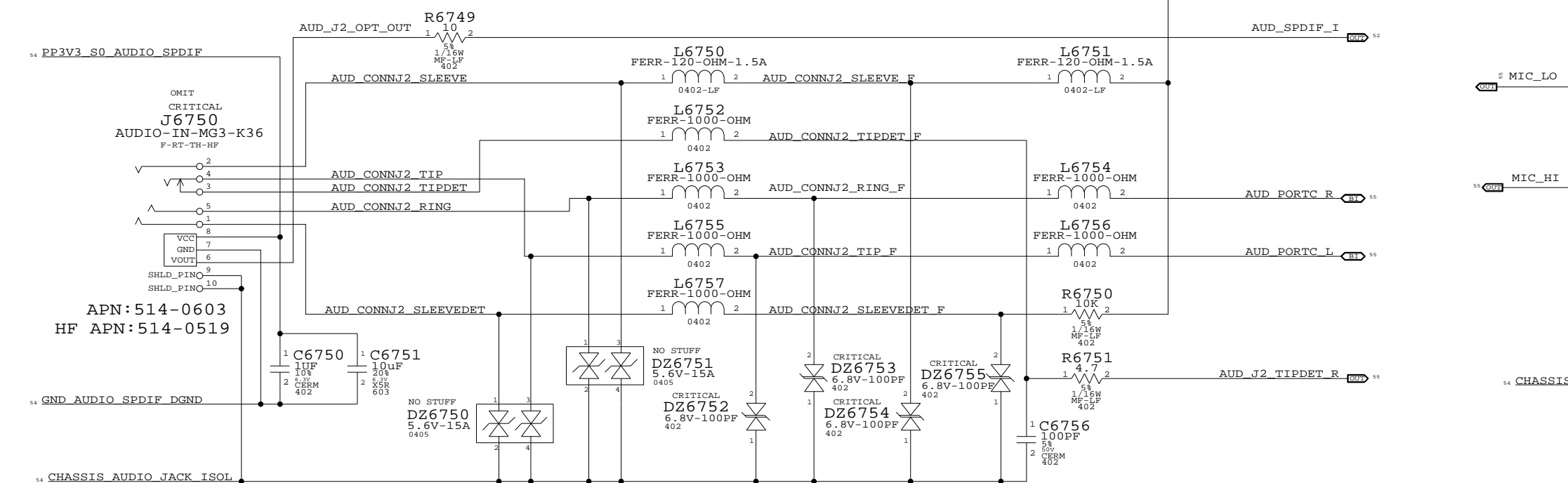
APN: 518S0521



MIC EMI FILTER



AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



**AUDIO: JACK**  
 SYNC\_MASTER=K36A\_MLB SYNC\_DATE=08/29/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	54		

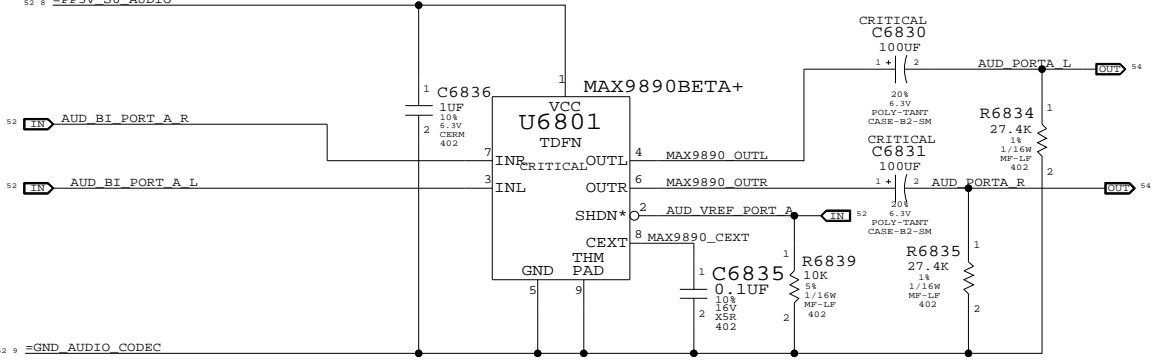
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

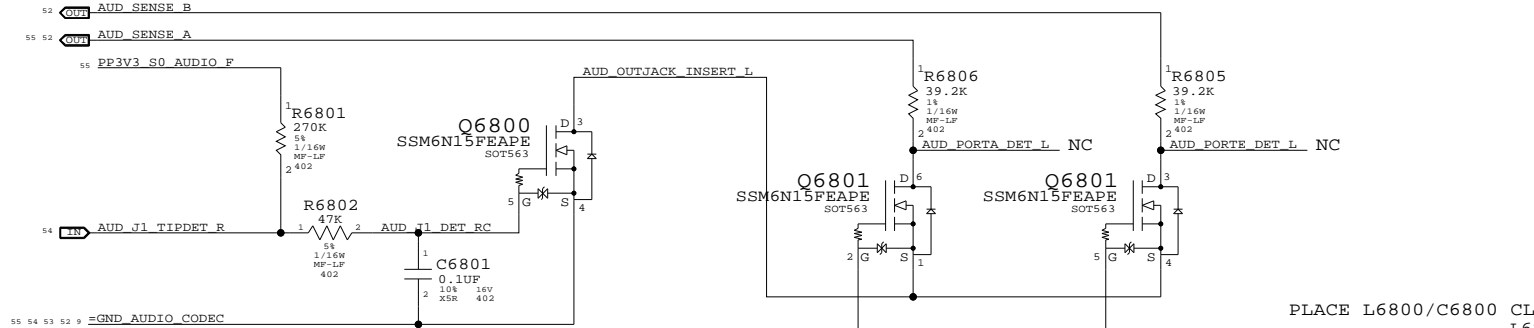
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

HP/LO DE-POP SWITCH  
APN:353S1459  
PORT A HP/LO

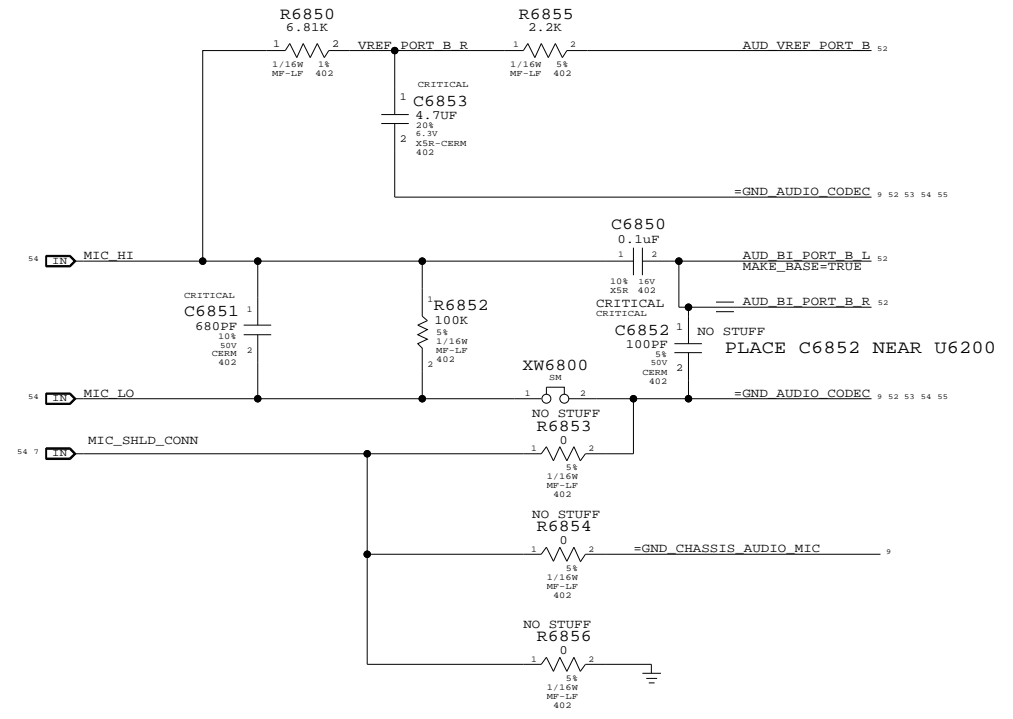


PORT A DETECT PORT E DETECT (SPDIF DELEGATE)

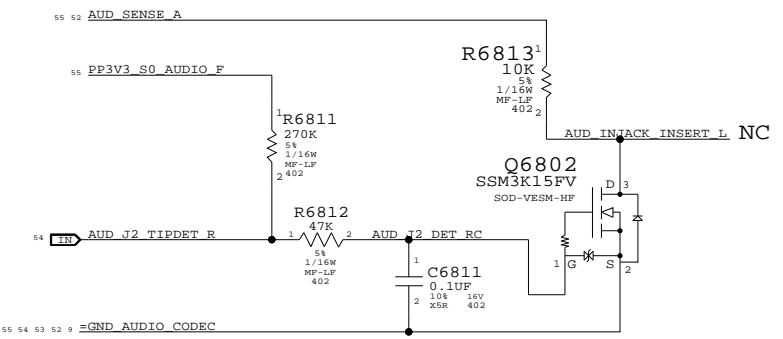


PLACE L6800/C6800 CLOSE TO Q6800

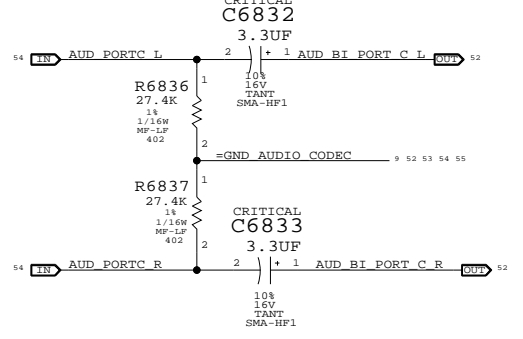
MIC INPUT CIRCUITRY



Line-in (PORT C) DETECT



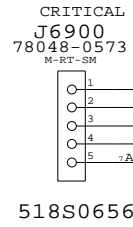
PORT C LI



**AUDIO: JACK TRANSLATORS**  
 SYNC\_MASTER=K36A\_MB SYNC\_DATE=08/29/2008  
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- COPY THIS PAGE FROM T18 CSA.69  
 - DO WE NEED TO CHANGE BATTERY CONNECTOR?

### MagSafe DC Power Jack

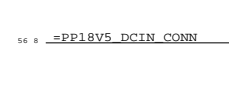
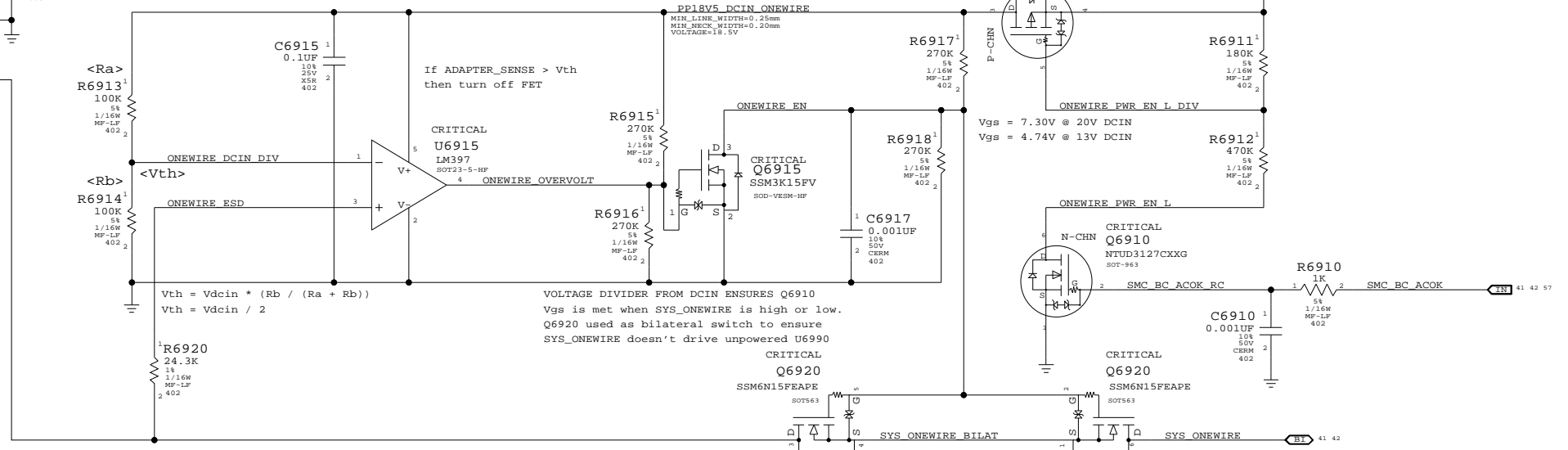


PP18V5 DCIN FUSE  
 MIN\_LINE\_WIDTH=1mm  
 MIN\_NECK\_WIDTH=0.20mm  
 VOLTAGE=18.5V

CRITICAL  
**F6905**  
 6AMP-24V  
 1206

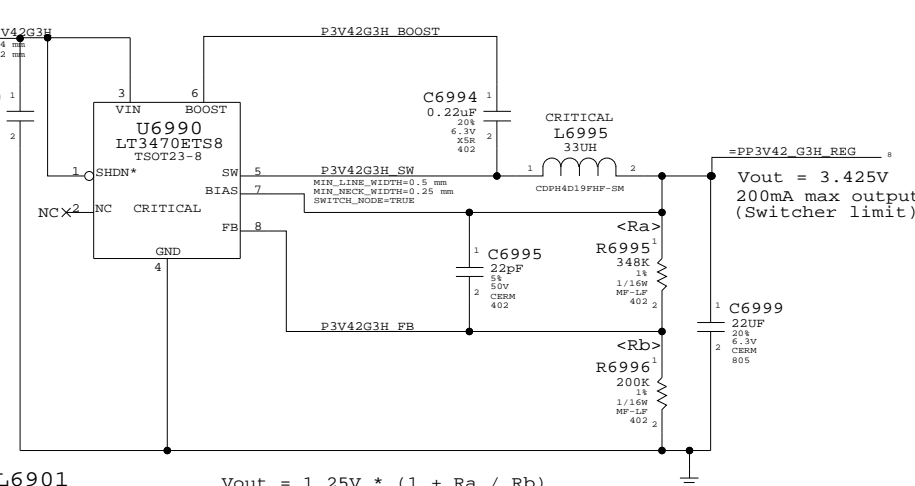
Q6910 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

### 1-Wire OverVoltage Protection

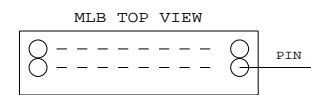


### 3.425V "G3Hot" Supply

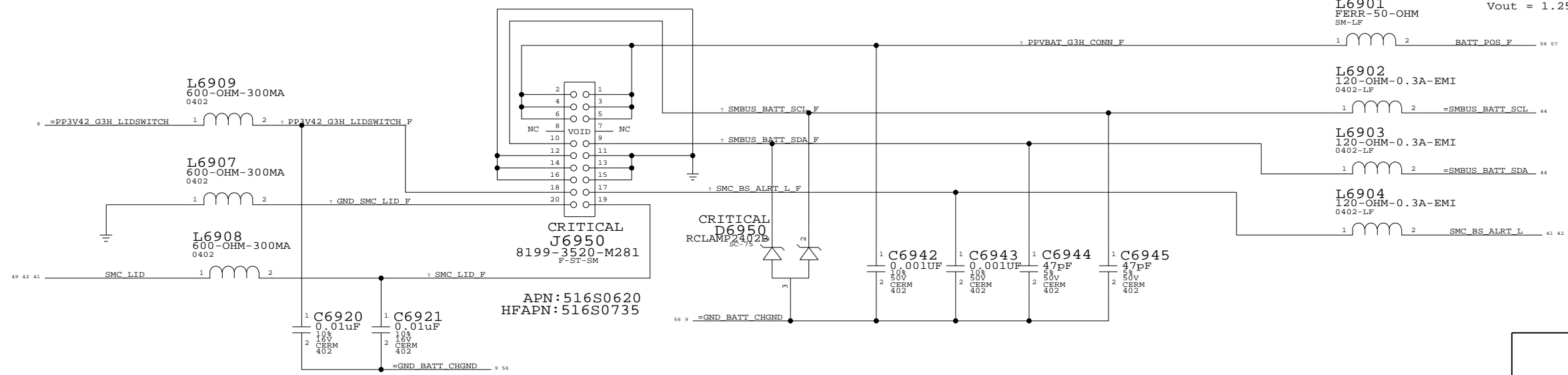
Supply needs to guarantee 3.1V delivered to SMC Vref generator



### LID HALL EFFECT SENSOR



### BATTERY/LID CONNECTOR

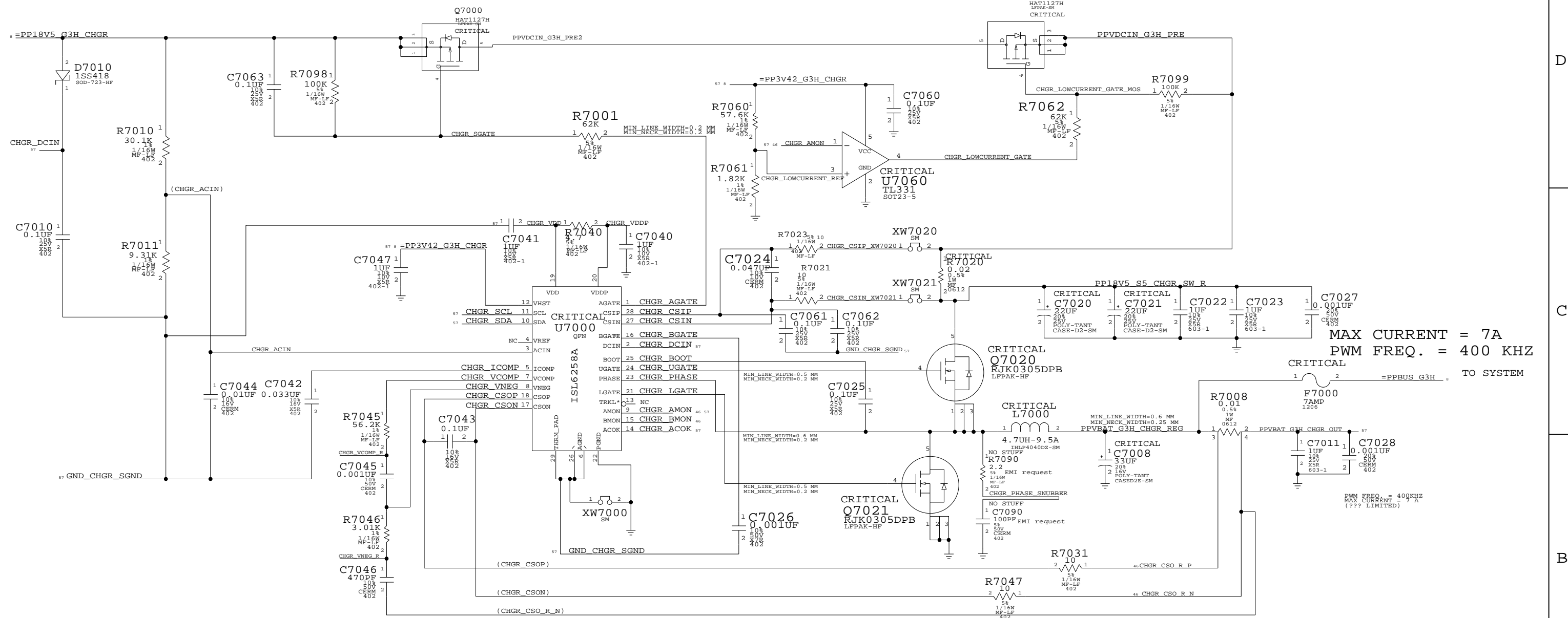


**DC-In & Battery Connectors**  
 SYNC\_MASTER=RAYMOND SYNC\_DATE=08/17/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	NONE	SHT	OF
		56	76

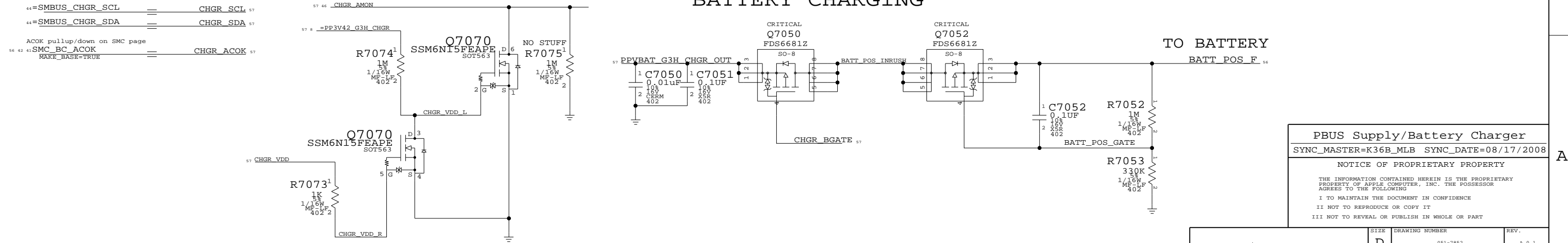


# PBUS SUPPLY / BATTERY CHARGER



AMON PULLDOWN LOGIC

## BATTERY CHARGING



**PBUS Supply/Battery Charger**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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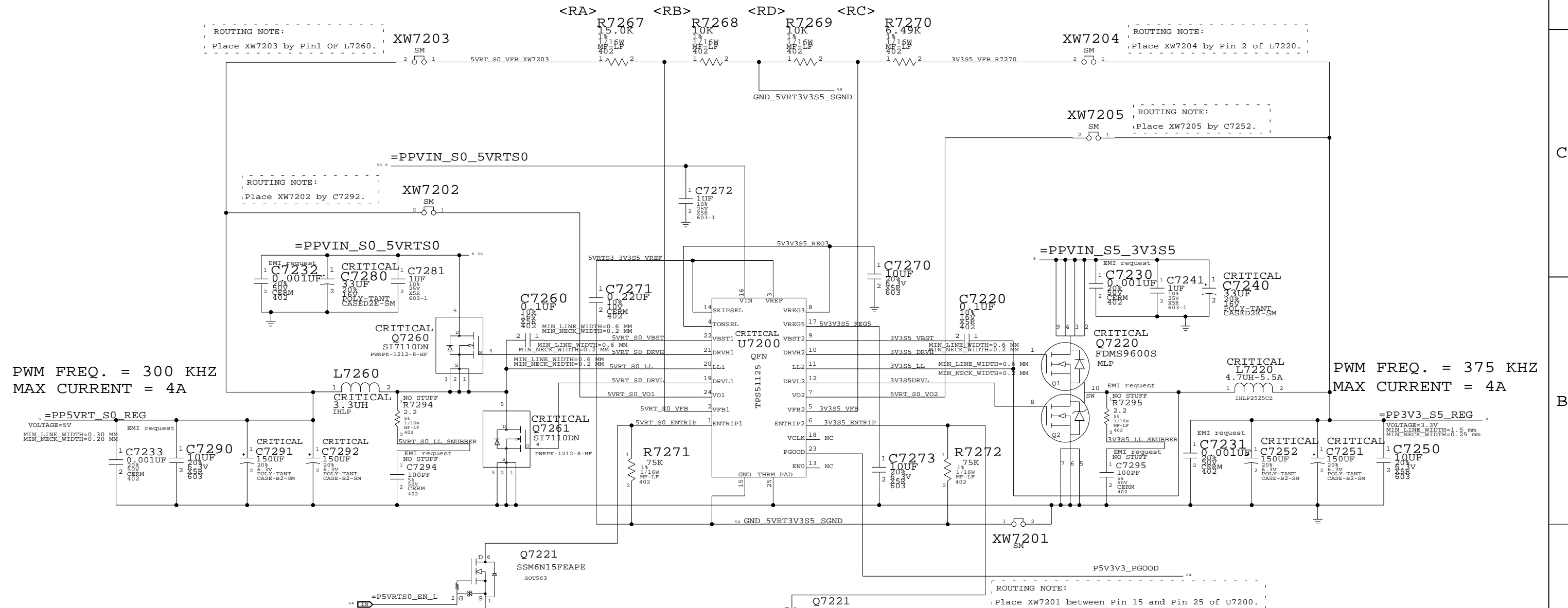
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	NONE	SHT	OF
		57	76

# 5V\_RT/3.3V POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



PWM FREQ. = 300 KHZ  
MAX CURRENT = 4A

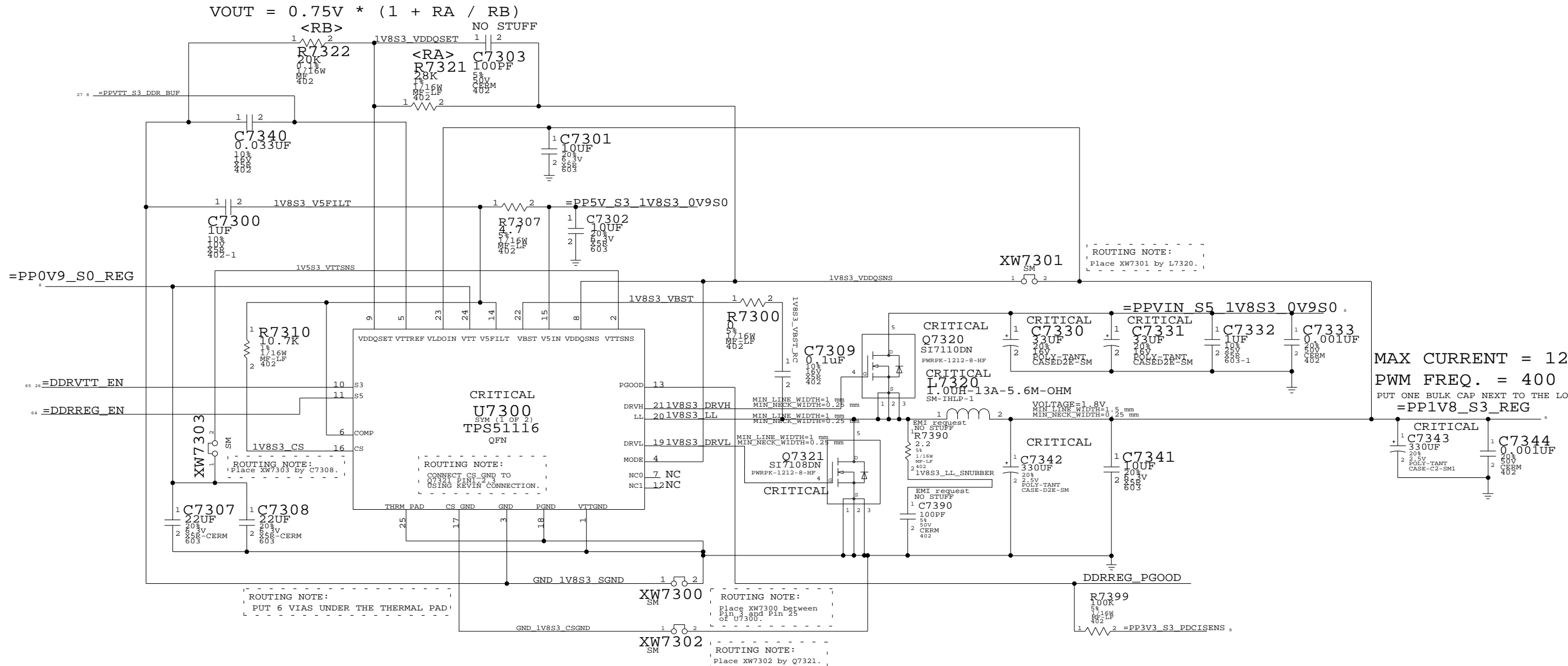
PWM FREQ. = 375 KHZ  
MAX CURRENT = 4A

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

**5V/3.3V SUPPLY**  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	58		

# 1.8V/0.9V(DDR2) POWER SUPPLY

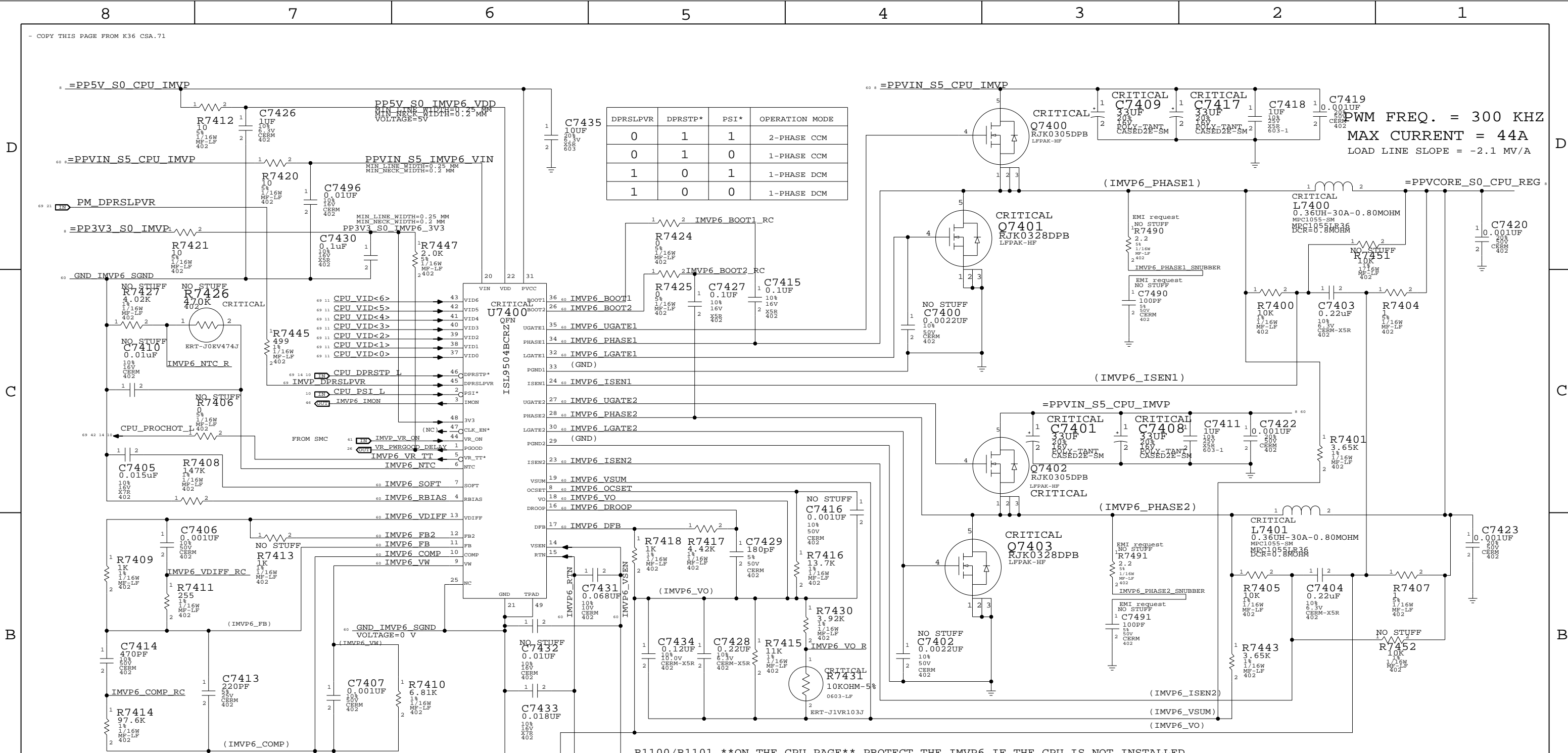


STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

1.8V/0.9V DDR2 SUPPLY  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	59	76



NOTE 1: C7432, C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 \*\*ON THE CPU PAGE\*\* PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

# IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

LATEST ISSUE: 2007/01/23

## IMVP6 CPU VCore Regulator

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

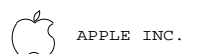
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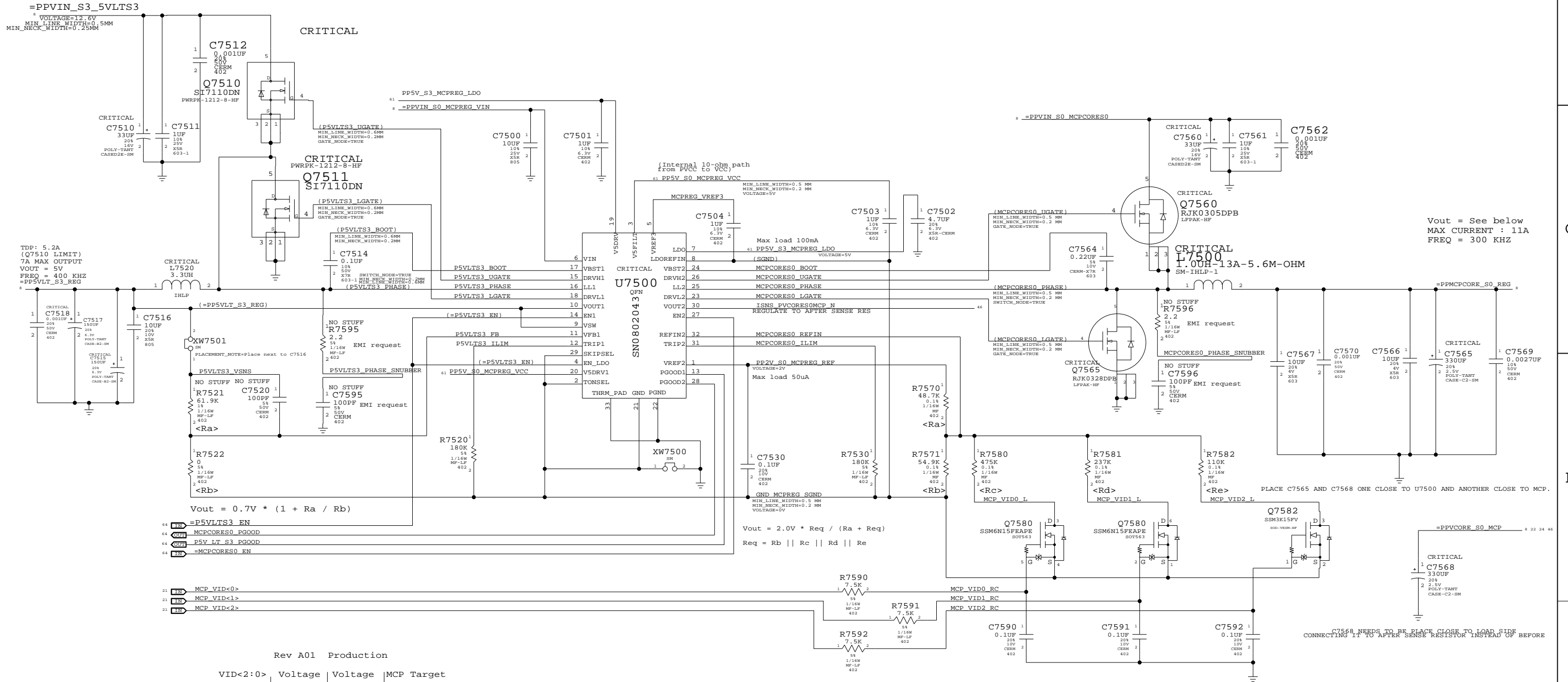
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHEET	OF
NONE	60	76

# MCP VCORE / 5V\_S3 LEFT REGULATOR

- SYNC WITH T18  
- COPY THIS PAGE FROM T18 CSA.75



$V_{out} = 0.7V * (1 + R_a / R_b)$

$V_{out} = 2.0V * R_{eq} / (R_a + R_{eq})$   
 $R_{eq} = R_b || R_c || R_d || R_e$

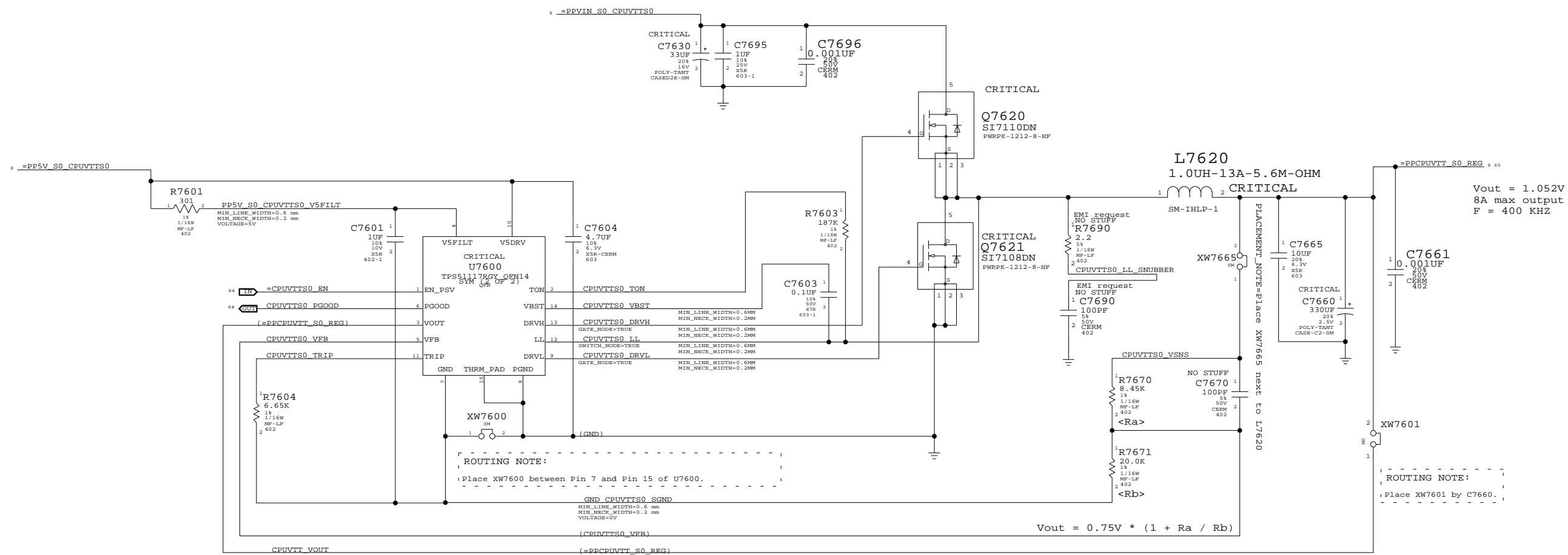
Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:  
 Added C7568 bulk cap on output.  
 Tied TON to REF.  
 Changed Q7510 to 376S0674.  
 C7500 changed to 138S0638.  
 L7560 changed from T18 MLB inductor to 152S0782.  
 Changed Q7565 to 376S0637.  
 Changed R7514 to 280K, R7564 to 180K.

**MCP VCORE REGULATOR**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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# CPUVTT POWER SUPPLY



## CPU VTT(1.05V) SUPPLY

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

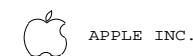
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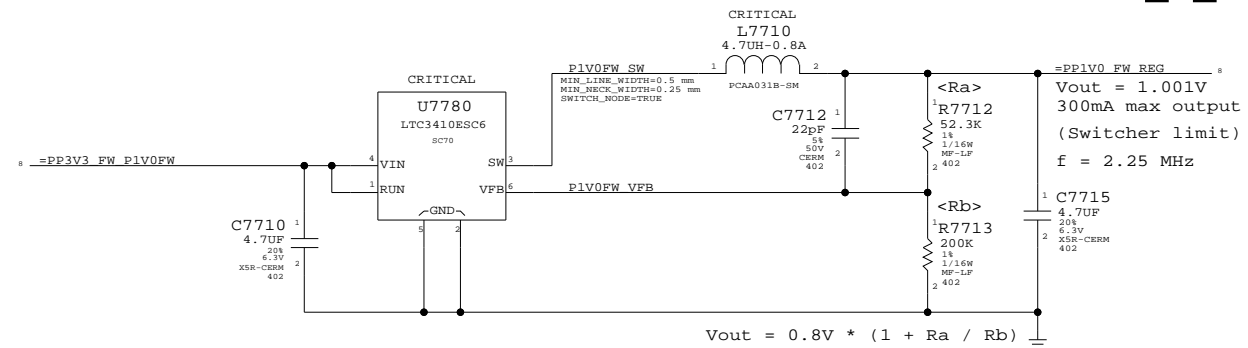
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



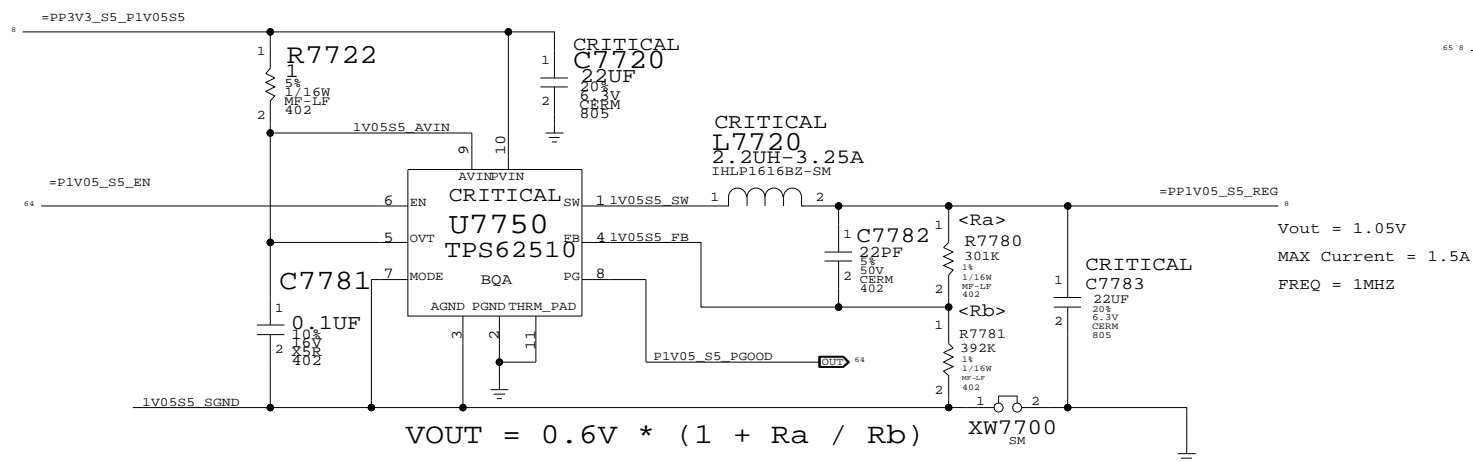
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7852	A.0.1
SCALE	SHT	OF
NONE	62	76

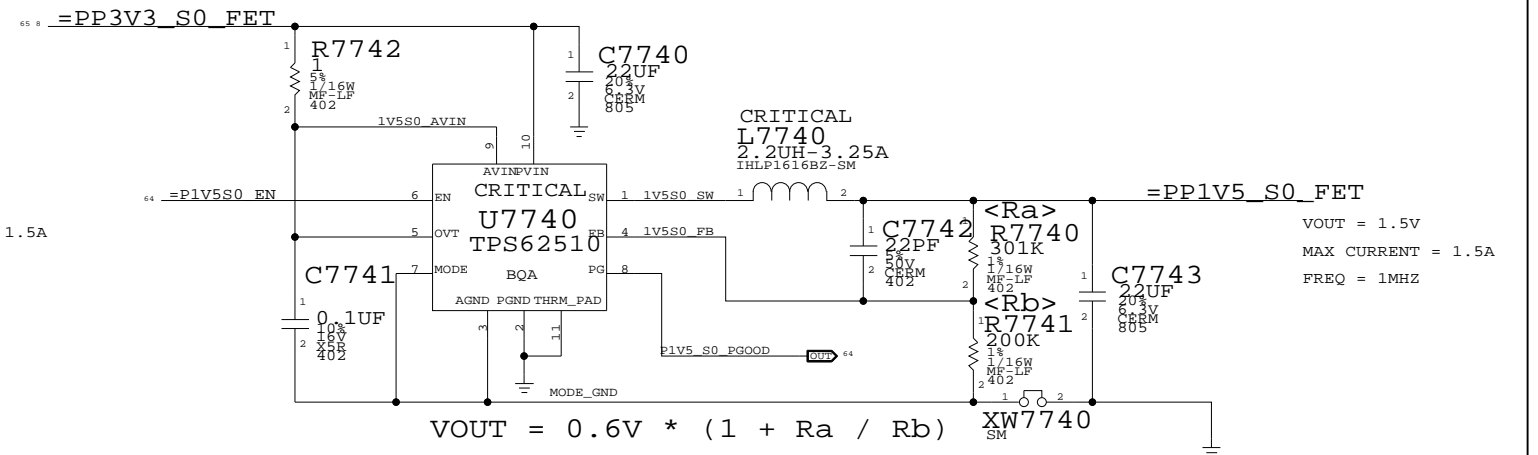
# FireWire 1.0V (Core) Supply



# MCP 1.05V\_S5 AUXC SUPPLY



# 1.5V S0 SWITCH

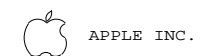


## MISC POWER SUPPLIES

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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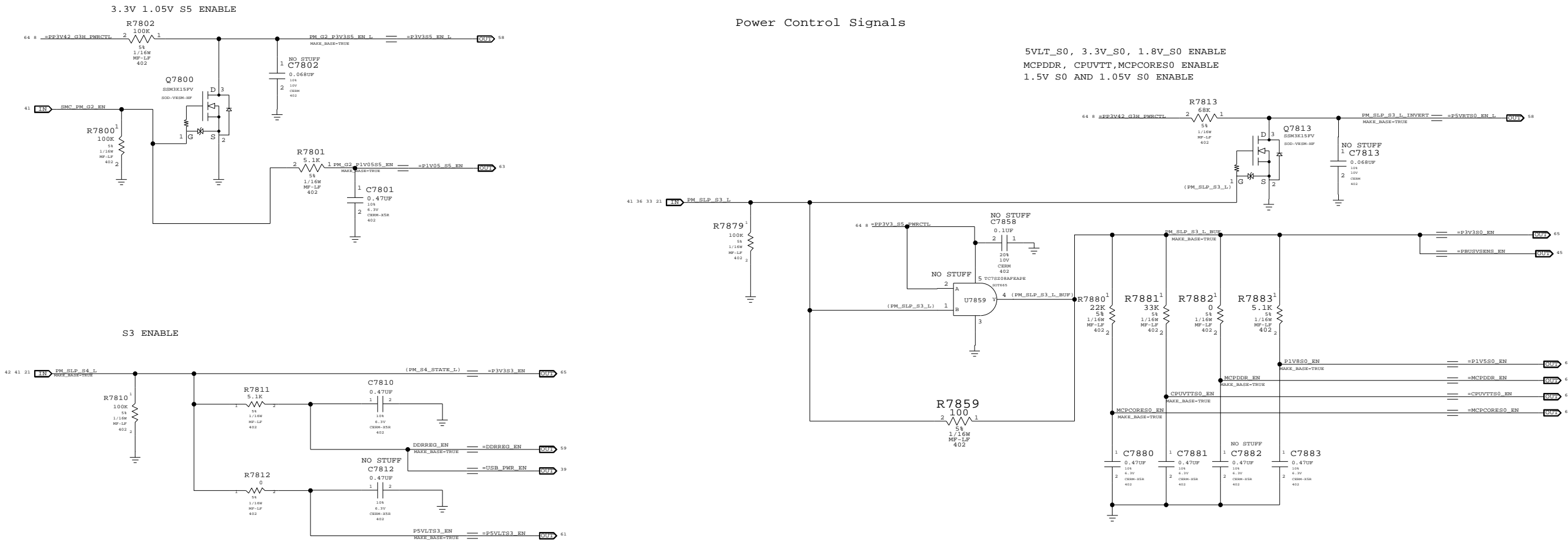


APPLE INC.

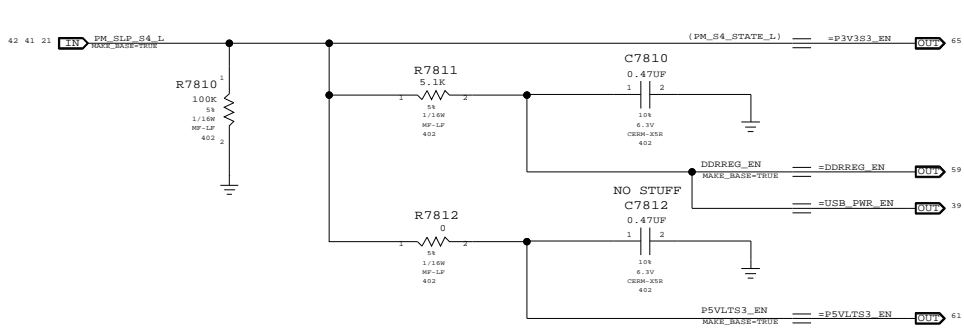
SIZE D	DRAWING NUMBER 051-7852	REV. A.0.1
SCALE NONE	SHT 63	OF 76

Power Control Signals

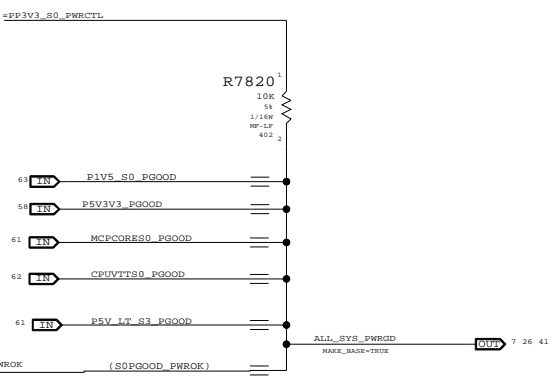
5VLT\_S0, 3.3V\_S0, 1.8V\_S0 ENABLE  
 MCPDDR, CPUVTT, MCPCORES0 ENABLE  
 1.5V S0 AND 1.05V S0 ENABLE



S3 ENABLE

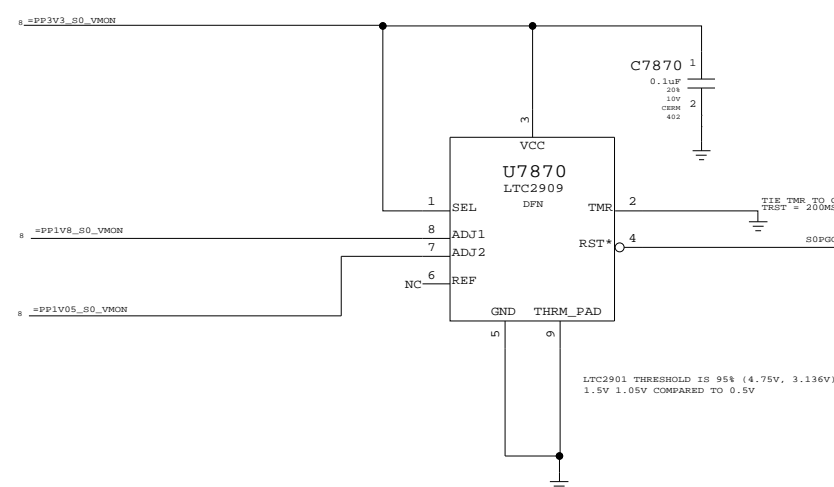


OTHER S0 RAILS PGOOD

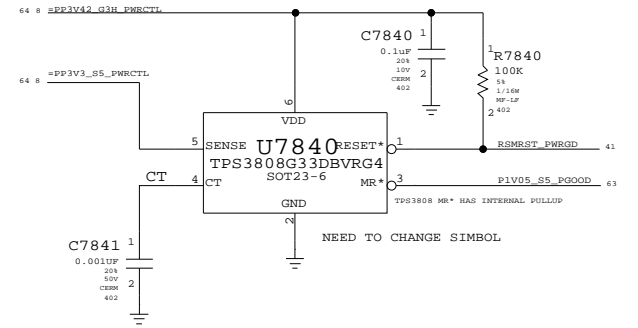


5.0V (RIGHT AND LEFT), 3.3V AND 1.5V S0 RAILS MONITOR CIRCUIT

LAYOUT\_NOTE: ADD XW IF NEEDS TO SAVE SPACE FOR PIN2,10,1,9



LTC2901 THRESHOLD IS 95% (4.75V, 3.136V)  
 1.5V 1.05V COMPARED TO 0.5V



Unused PGOOD signal

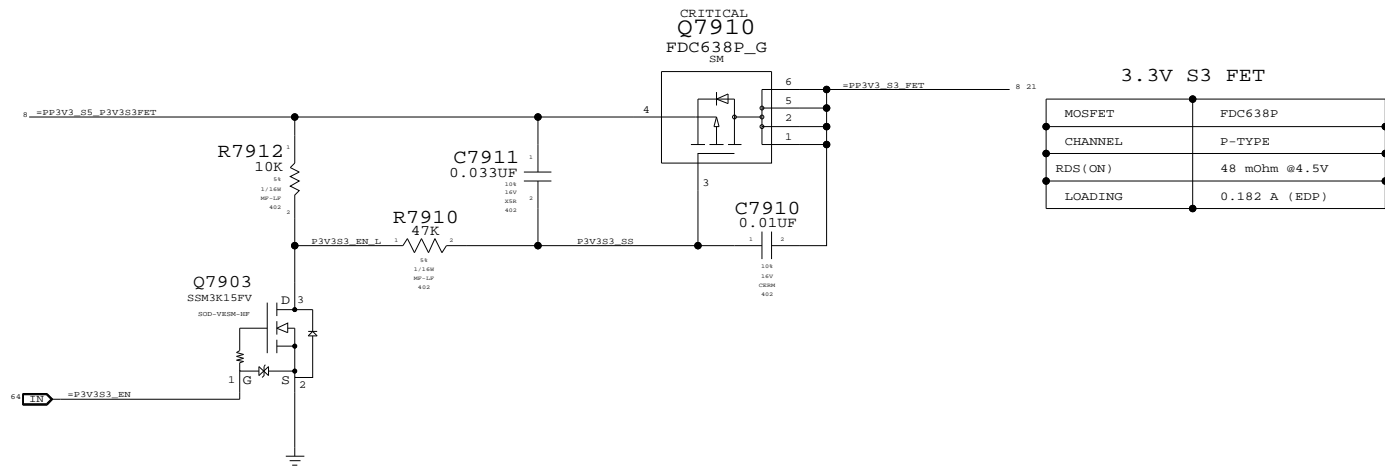
TP\_ENH1V\_PGOOD = ENH1V\_PGOOD

POWER SEQUENCING		
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	NONE	SHT	OF
		64	76

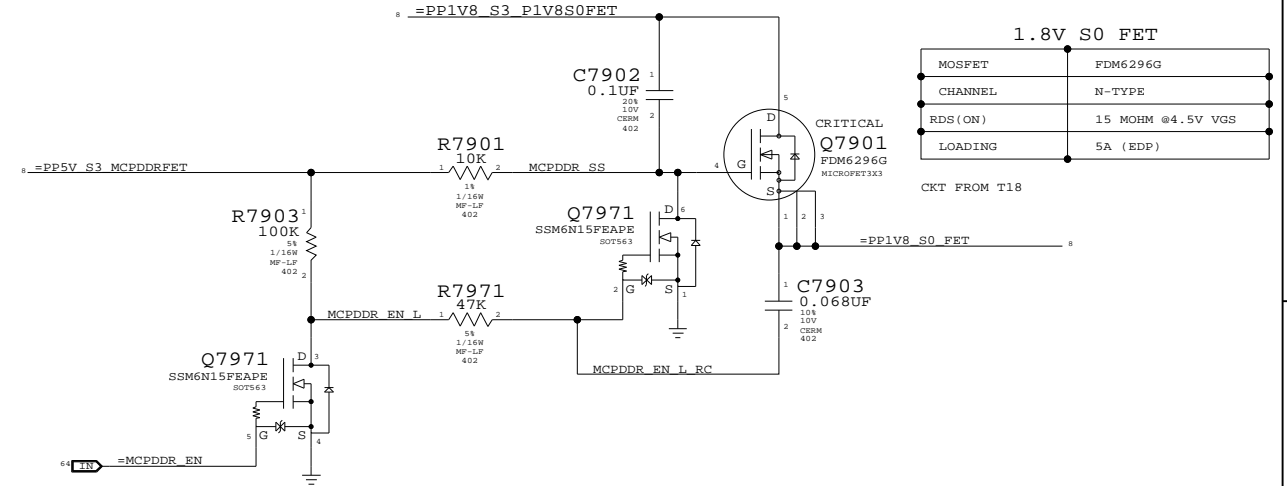


3.3V S3 FET



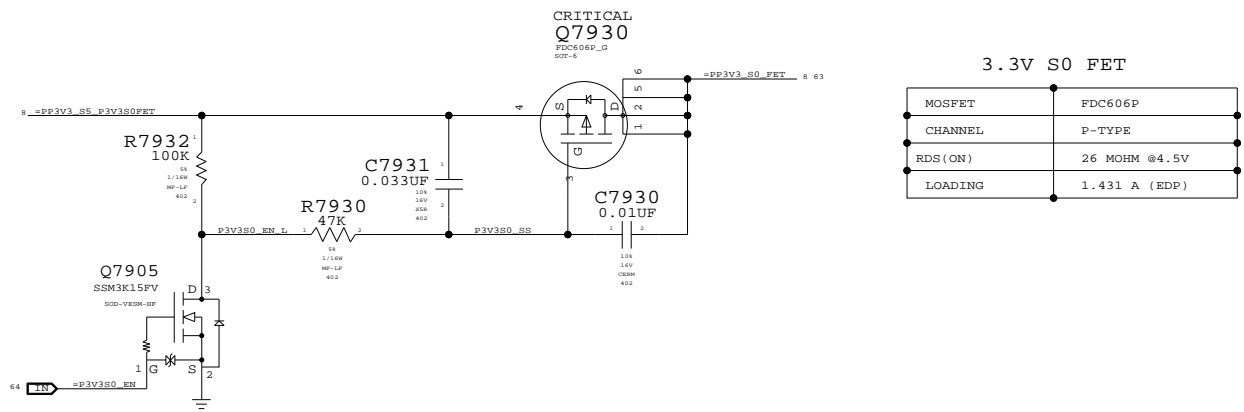
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

1.8V S0 FET  
(1.8V S0 FET FOR DDR2 MEM)



1.8V S0 FET	
MOSFET	FDM6296G
CHANNEL	N-TYPE
RDS(ON)	15 MOHM @4.5V VGS
LOADING	5A (EDP)

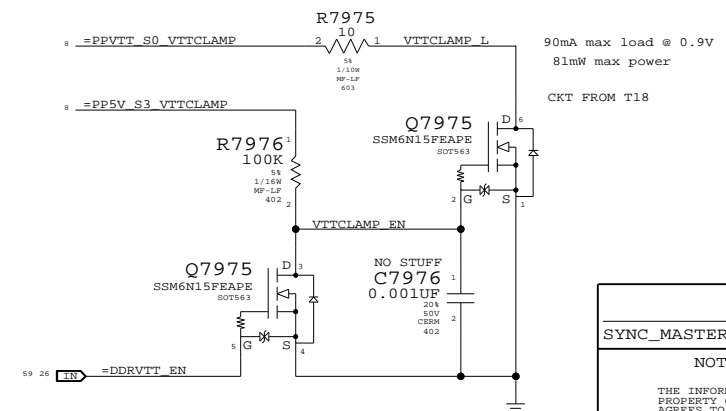
3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.

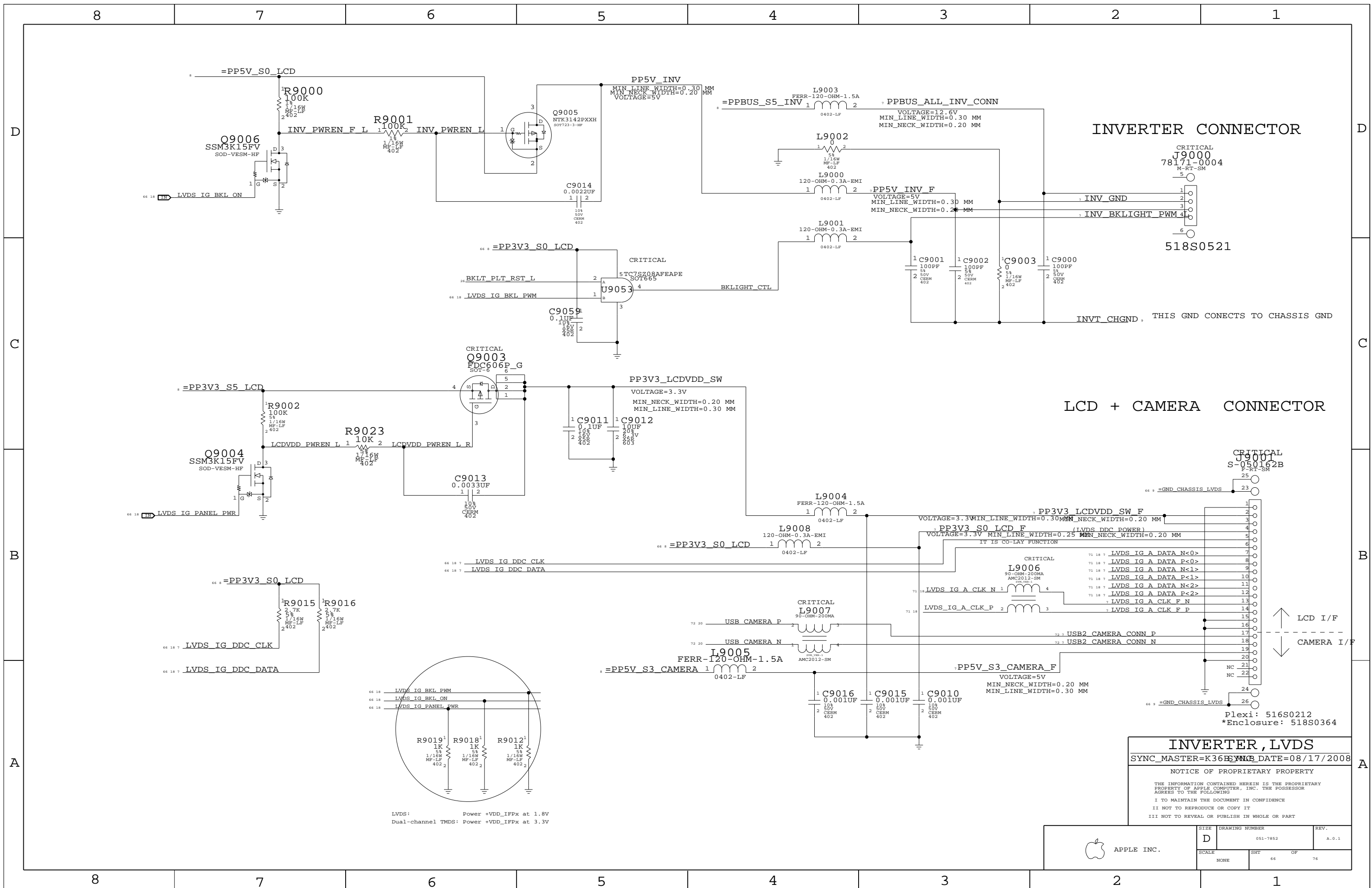


90mA max load @ 0.9V  
81mW max power  
CKT FROM T18



**POWER FETS**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	65		



INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

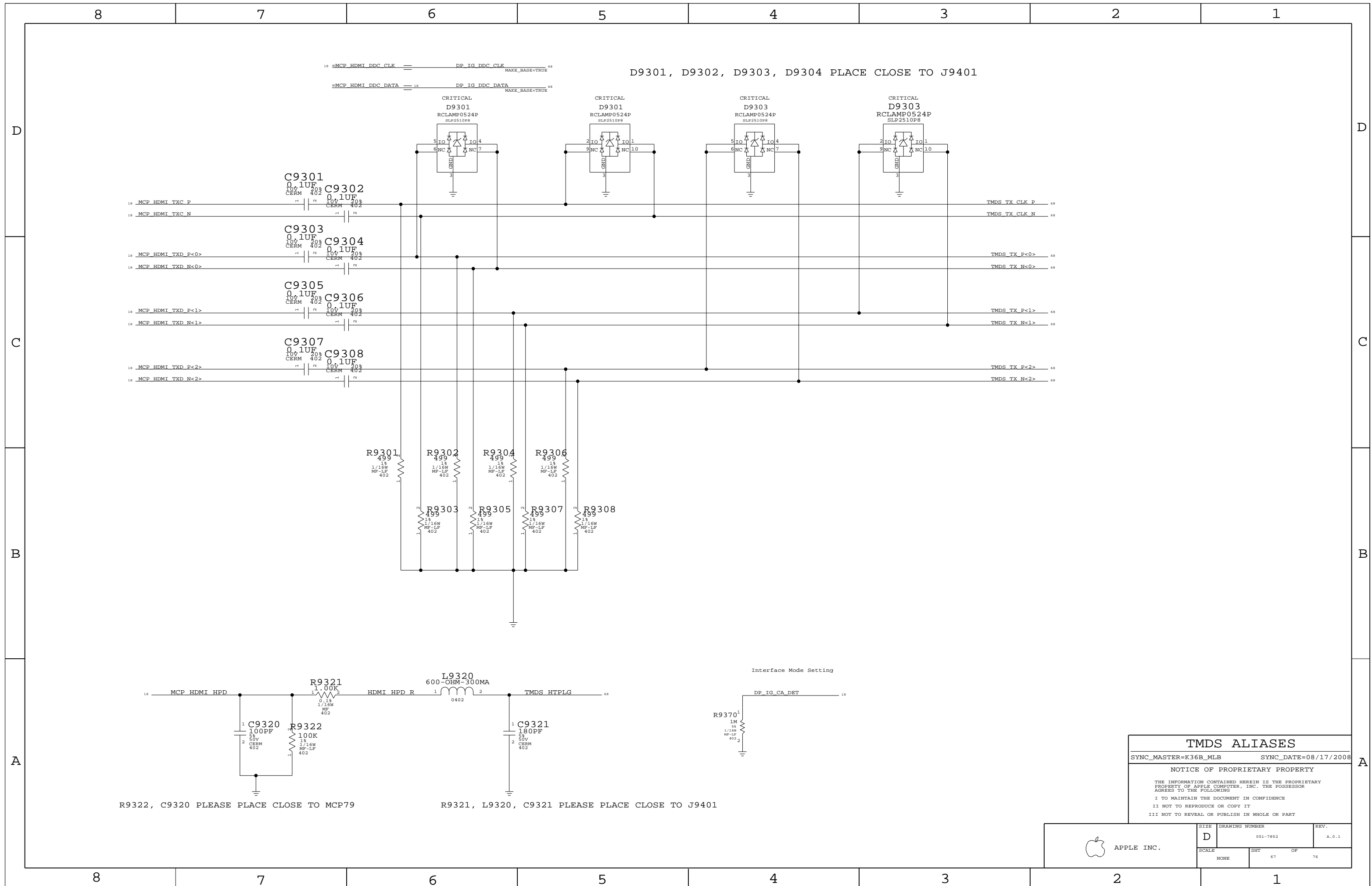
INVERTER, LVDS  
 SYNC\_MASTER=K365 DATE=08/17/2008

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	D	051-7852	A.0.1
SCALE	NONE	SHT	OF
		66	76

LVDS: Power +VDD\_IFPx at 1.8V  
 Dual-channel TMDs: Power +VDD\_IFPx at 3.3V

Plexi: 516S0212  
 \*Enclosure: 518S0364



D9301, D9302, D9303, D9304 PLACE CLOSE TO J9401

R9322, C9320 PLEASE PLACE CLOSE TO MCP79

R9321, L9320, C9321 PLEASE PLACE CLOSE TO J9401

**TMD5 ALIASES**  
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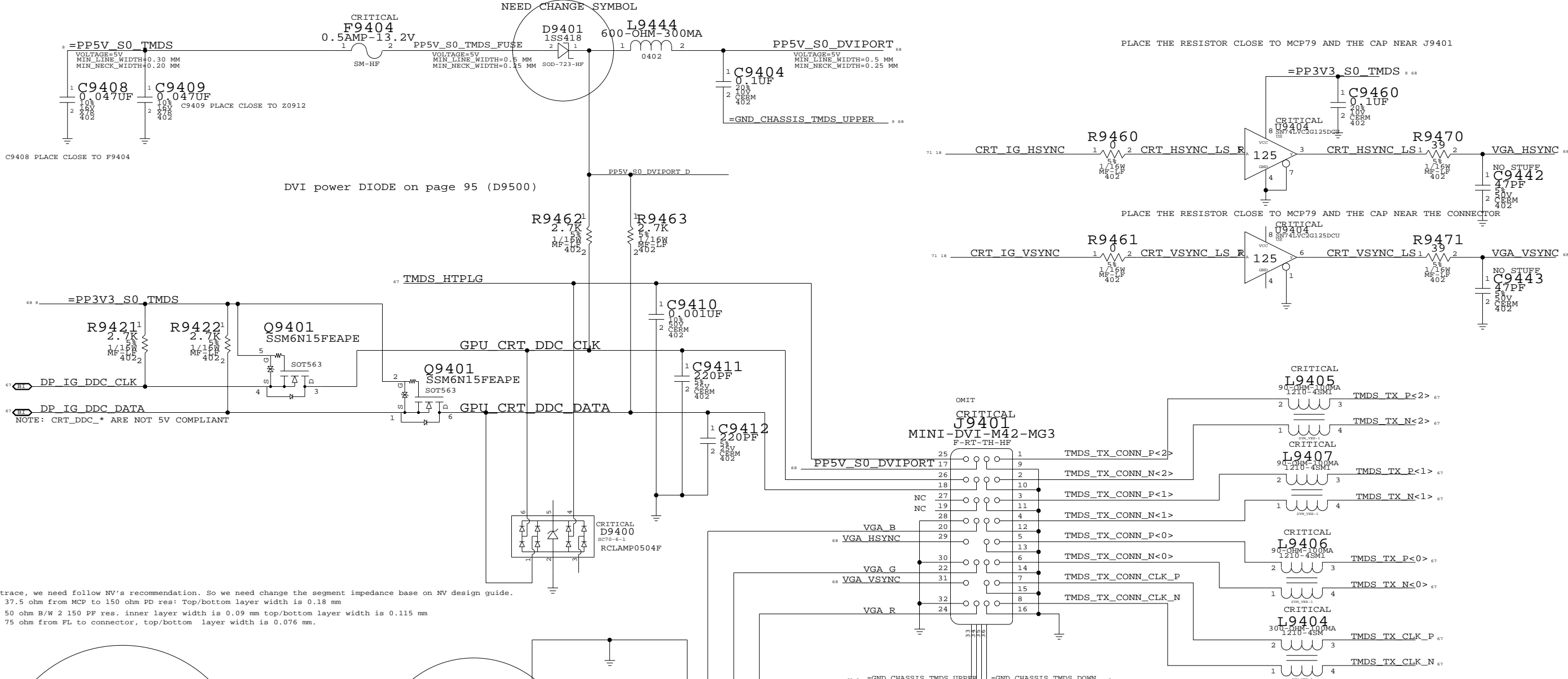
	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	67		

# Video Connectors

## EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

## TMDS (MINI DVI) INTERFACE



for VG signal trace, we need follow NV's recommendation. So we need change the segment impedance base on NV design guide.  
 for A segment: 37.5 ohm from MCP to 150 ohm PD res. Top/bottom layer width is 0.18 mm  
 for B segment: 50 ohm B/W 2 150 PF res. inner layer width is 0.09 mm top/bottom layer width is 0.115 mm  
 for C segment: 75 ohm from FL to connector, top/bottom layer width is 0.076 mm.

### MINI-DVI CONNECTOR

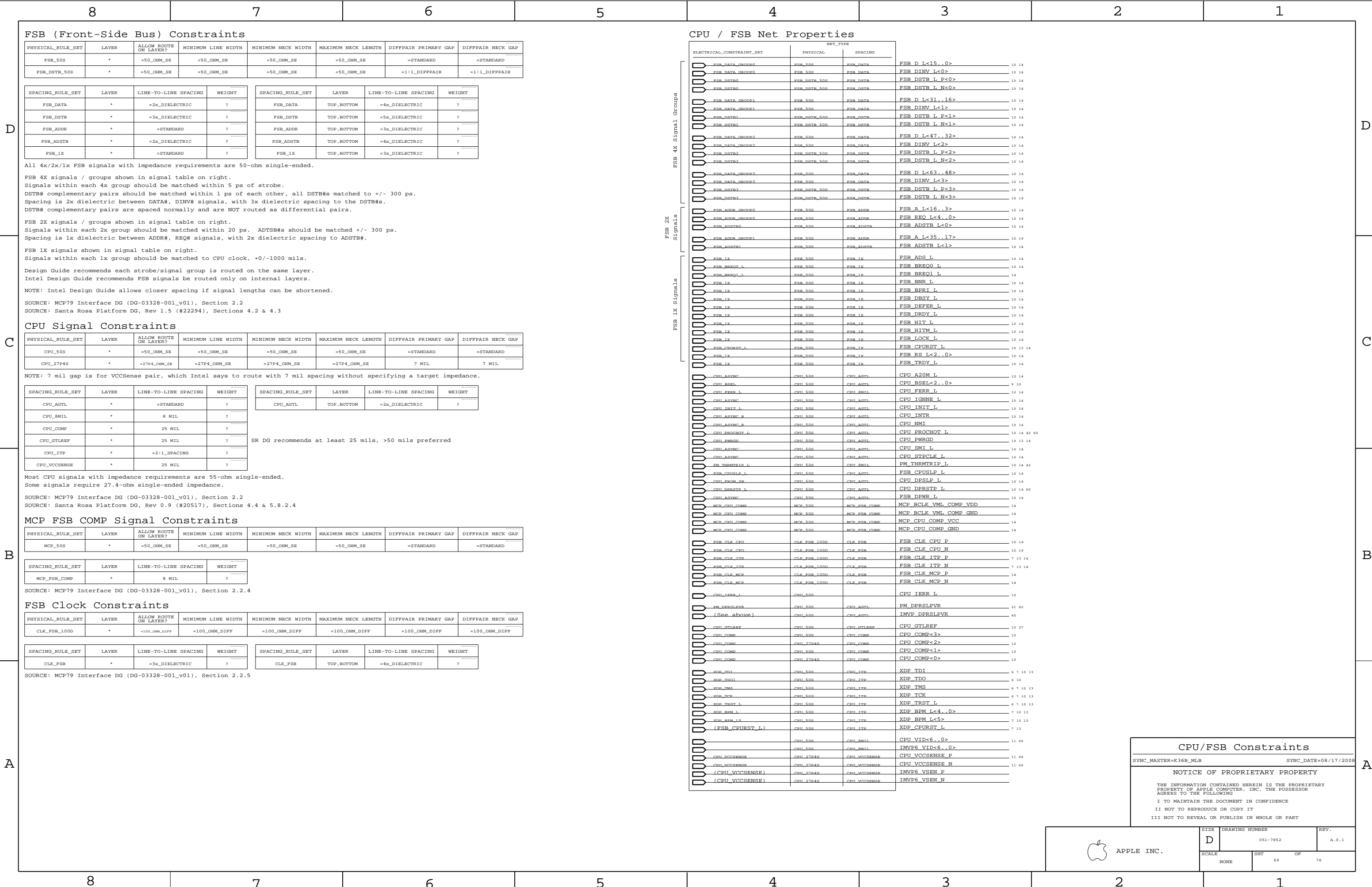
SYNC\_MASTER=K365 SYNC\_DATE=08/17/2008

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	SIZE	DRAWING NUMBER	REV.
	D	051-7852	A.0.1
SCALE	SHT	OF	76
NONE	68		



### FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

### CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

### MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

### FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

### CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>
FSB_1X	FSB_50S	FSB_1X	FSB ADS L
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0 L
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB BREQ1 L
FSB_1X	FSB_50S	FSB_1X	FSB BNR L
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L
FSB_1X	FSB_50S	FSB_1X	FSB HIT L
FSB_1X	FSB_50S	FSB_1X	FSB HITM L
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGARNE L
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB CPURST L
CPU_PERR_SR	CPU_50S	CPU_AGTL	CPU DPSSL P
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N
CPU_IERR_L	CPU_50S		CPU IERR L
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR
(See above)	CPU_50S	CPU_AGTL	IMVP6 DPRSLPVR
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L
CPU_VID<6..0>	CPU_50S	CPU_8MIL	CPU VID<6..0>
CPU_VID<6..0>	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN P
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN N

<b>CPU/FSB Constraints</b>	
SYNC_MASTER=K36B_MLB	SYNC_DATE=08/17/2008
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	SCALE	DRAWING NUMBER	REV.
	NONE	051-7852	A.0.1
	SHEET	OF	
	69	76	

Memory Bus Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include MEM\_40S, MEM\_40S\_VDD, MEM\_70D, MEM\_70D\_VDD.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include MEM\_CLK2MEM, MEM\_CTRL2CTRL, MEM\_CTRL2MEM, MEM\_CMD2CMD, MEM\_CMD2MEM, MEM\_DATA2DATA, MEM\_DATA2MEM, MEM\_DQS2MEM, MEM\_2OTHER.

Memory Bus Spacing Group Assignments

Grid of assignment tables with columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Includes assignments for MEM\_CLK, MEM\_CTRL, MEM\_CMD, MEM\_DATA, MEM\_DQS, MEM\_2OTHER.

Need to support MEM\_\*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair. DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement. All DQS pairs should be matched within 100 ps of clocks. CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps. A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement. All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate). DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair. DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps. No DQS to clock matching requirement. CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps. A/BA/cmd signals should be matched within 5 ps of CLK pairs. All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate). DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row: MCP\_MEM\_COMP.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row: MCP\_MEM\_COMP.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, NET\_TYPE, SPACING. Lists constraints for MEM\_A and MEM\_B signals including CLK, CTRL, CMD, CAS, WE, L, DQ, DQS, and various N<0> through N<7>.

Memory Constraints
SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.  
SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PEG_R2D	PCIE_90D	PCIE	PEG_R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG_R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG_R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG_R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_D2R C N<15..0>
PCIE_MINI_R2D_P	PCIE_90D	PCIE	PCIE_MINI_R2D_P
PCIE_MINI_R2D_N	PCIE_90D	PCIE	PCIE_MINI_R2D_N
PCIE_MINI_R2D_C_P	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N
PCIE_MINI_D2R_P	PCIE_90D	PCIE	PCIE_MINI_D2R_P
PCIE_MINI_D2R_N	PCIE_90D	PCIE	PCIE_MINI_D2R_N
PCIE_FW_R2D_P	PCIE_90D	PCIE	PCIE_FW_R2D_P
PCIE_FW_R2D_N	PCIE_90D	PCIE	PCIE_FW_R2D_N
PCIE_FW_R2D_C_P	PCIE_90D	PCIE	PCIE_FW_R2D_C_P
PCIE_FW_R2D_C_N	PCIE_90D	PCIE	PCIE_FW_R2D_C_N
PCIE_FW_D2R_P	PCIE_90D	PCIE	PCIE_FW_D2R_P
PCIE_FW_D2R_N	PCIE_90D	PCIE	PCIE_FW_D2R_N
PCIE_FW_D2R_C_P	PCIE_90D	PCIE	PCIE_FW_D2R_C_P
PCIE_FW_D2R_C_N	PCIE_90D	PCIE	PCIE_FW_D2R_C_N
PCIE_EXCARD_R2D_P	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P
PCIE_EXCARD_R2D_N	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N
PCIE_EXCARD_R2D_C_P	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P
PCIE_EXCARD_R2D_C_N	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_D2R_P	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P
PCIE_EXCARD_D2R_N	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N
PEG_CLK100M_P	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P
PEG_CLK100M_N	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N
PCIE_CLK100M_MINI_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N
PCIE_CLK100M_FW_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N
PCIE_CLK100M_EXCARD_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P
PCIE_CLK100M_EXCARD_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP
CRT_IG_R_C_PR	CRT_MCP_P	CRT	CRT_IG_R_C_PR
CRT_IG_G_Y_Y	CRT_MCP_P	CRT	CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB	CRT_MCP_P	CRT	CRT_IG_B_COMP_PB
CRT_IG_HSYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC
CRT_IG_VSYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC
MCP_TV_DAC_RSET	MCP_DAC_COMP	MCP_DAC_COMP	MCP_TV_DAC_RSET
MCP_TV_DAC_VREF	MCP_DAC_COMP	MCP_DAC_COMP	MCP_TV_DAC_VREF
TMDS_IG_TXC_P	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P
TMDS_IG_TXC_N	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N
TMDS_IG_TXD_P<2..0>	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>
TMDS_IG_TXD_N<2..0>	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>
DP_IG_ML_P<3..0>	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>
DP_IG_ML_N<3..0>	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>
TP_DP_IG_AUX_CH_P	DP_100D	DISPLAYPORT	TP_DP_IG_AUX_CH_P
TP_DP_IG_AUX_CH_N	DP_100D	DISPLAYPORT	TP_DP_IG_AUX_CH_N
MCP_HDMI_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP_HDMI_RSET
MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP_HDMI_VPROBE
LVDS_IG_A_CLK_P	LVDS_100D	LVDS	LVDS_IG_A_CLK_P
LVDS_IG_A_CLK_N	LVDS_100D	LVDS	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>
LVDS_IG_A_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>
LVDS_IG_A_DATA_P<3>	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>
LVDS_IG_A_DATA_N<3>	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>
LVDS_IG_B_CLK_P	LVDS_100D	LVDS	LVDS_IG_B_CLK_P
LVDS_IG_B_CLK_N	LVDS_100D	LVDS	LVDS_IG_B_CLK_N
LVDS_IG_B_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>
LVDS_IG_B_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>
LVDS_IG_B_DATA_P<3>	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>
LVDS_IG_B_DATA_N<3>	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>
MCP_IFFAB_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP_IFFAB_RSET
MCP_IFFAB_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP_IFFAB_VPROBE
SATA_HDD_R2D_C_P	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P
SATA_HDD_R2D_C_N	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N
SATA_HDD_R2D_P	SATA_100D_HDD	SATA	SATA_HDD_R2D_P
SATA_HDD_R2D_N	SATA_100D_HDD	SATA	SATA_HDD_R2D_N
SATA_HDD_R2D_UF_P	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P
SATA_HDD_R2D_UF_N	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N
SATA_HDD_D2R_P	SATA_100D_HDD	SATA	SATA_HDD_D2R_P
SATA_HDD_D2R_N	SATA_100D_HDD	SATA	SATA_HDD_D2R_N
SATA_HDD_D2R_C_P	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N
SATA_ODD_R2D_C_P	SATA_100D	SATA	SATA_ODD_R2D_C_P
SATA_ODD_R2D_C_N	SATA_100D	SATA	SATA_ODD_R2D_C_N
SATA_ODD_R2D_P	SATA_100D	SATA	SATA_ODD_R2D_P
SATA_ODD_R2D_N	SATA_100D	SATA	SATA_ODD_R2D_N
SATA_ODD_R2D_UF_P	SATA_100D	SATA	SATA_ODD_R2D_UF_P
SATA_ODD_R2D_UF_N	SATA_100D	SATA	SATA_ODD_R2D_UF_N
SATA_ODD_D2R_P	SATA_100D	SATA	SATA_ODD_D2R_P
SATA_ODD_D2R_N	SATA_100D	SATA	SATA_ODD_D2R_N
SATA_ODD_D2R_C_P	SATA_100D	SATA	SATA_ODD_D2R_C_P
SATA_ODD_D2R_C_N	SATA_100D	SATA	SATA_ODD_D2R_C_N
SATA_ODD_D2R_UF_P	SATA_100D	SATA	SATA_ODD_D2R_UF_P
SATA_ODD_D2R_UF_N	SATA_100D	SATA	SATA_ODD_D2R_UF_N
MCP_SATA_TERM	SATA_100D	SATA_TERM	MCP_SATA_TERM

**MCP Constraints 1**

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.14.

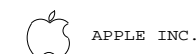
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	7 13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTRL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTRL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTRL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTRL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTRL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTRL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTRL	PCI_55S	PCI	PCI_FRAME_L	
PCI_BE00_I	PCI_55S	PCI	PCI_BE00_I	19
PCI_GNT0_I	PCI_55S	PCI	PCI_GNT0_I	
PCI_BE01_I	PCI_55S	PCI	PCI_BE01_I	19
PCI_GNT1_I	PCI_55S	PCI	PCI_GNT1_I	
PCI_INTX_I	PCI_55S	PCI	PCI_INTX_L	
PCI_INTX_I	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_I	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_I	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R	19
CLK_PCI_55S	CLK_PCI	CLK_PCI	PCI_CLK33M MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	7 19 41 43
LPC_FRAME_L0	LPC_55S	LPC	LPC_FRAME_L	7 19 41 43
LPC_RESET_I	LPC_55S	LPC	LPC_RESET_L	19 26
MCP_LPC_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R	19 26
MCP_LPC_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC	26 41
WR_LPC_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS	7 26 43
USB_EXTN	USB_90D	USB	USB_EXTN_P	20 39
USB_EXTN	USB_90D	USB	USB_EXTN_N	20 39
USB_EXTN	USB_90D	USB	USB2_EXTN_MUXED_P	39
USB_EXTN	USB_90D	USB	USB2_EXTN_MUXED_N	39
USB_EXTN	USB_90D	USB	USB2_EXTN_F_P	39
USB_EXTN	USB_90D	USB	USB2_EXTN_F_N	39
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
USB_MINI	USB_90D	USB	USB_MINI_N	9 20
USB_MINI	USB_90D	USB	USB2_AIRPORT_P	7 31
USB_MINI	USB_90D	USB	USB2_AIRPORT_N	7 31
USB_EXTRN	USB_90D	USB	USB_EXTRN_P	9 20
USB_EXTRN	USB_90D	USB	USB_EXTRN_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 66
USB_CAMERA	USB_90D	USB	USB_CAMERA_N	20 66
USB_CAMERA	USB_90D	USB	USB2_CAMERA_CONN_P	7 66
USB_CAMERA	USB_90D	USB	USB2_CAMERA_CONN_N	7 66
USB_IR	USB_90D	USB	USB_IR_P	20 40
USB_IR	USB_90D	USB	USB_IR_N	20 40
USB_TPAD	USB_90D	USB	USB_TPAD_P	9 20
USB_TPAD	USB_90D	USB	USB_TPAD_N	9 20
USB_TPAD	USB_90D	USB	CONN_TPAD_USB_P	7 49
USB_TPAD	USB_90D	USB	CONN_TPAD_USB_N	7 49
USB_BT	USB_90D	USB	USB_BT_P	9 20
USB_BT	USB_90D	USB	USB_BT_N	9 20
USB_BT	USB_90D	USB	USB2_BT_F_P_CONN	7 40
USB_BT	USB_90D	USB	USB2_BT_F_N_CONN	7 40
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 39
USB_EXTB	USB_90D	USB	USB_EXTB_N	20 39
USB_EXTB	USB_90D	USB	USB2_EXTB_F_P	39
USB_EXTB	USB_90D	USB	USB2_EXTB_F_N	39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	9 20
USB_EXCARD	USB_90D	USB	USB_EXCARD_N	9 20
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
USB_EXTC	USB_90D	USB	USB_EXTC_N	9 20
MCP_USB_BIAS	MCP_USB_BIAS	MCP_USB	MCP_USB_BIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21 52
HDA_BIT_CLK_R	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 52
HDA_SYNC_R	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	21 52
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 52
HDA_SDIN_CODECC	HDA_55S	HDA	HDA_SDIN_CODECC	
HDA_SDOUTT	HDA_55S	HDA	HDA_SDOUTT	21 52
HDA_SDOUTT_R	HDA_55S	HDA	HDA_SDOUTT_R	21
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP	MCP_HDA	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	FM_CLK32K_SUSCLK_R	21 26
CLK_SLOW_55S	CLK_SLOW	CLK_SLOW	FM_CLK32K_SUSCLK	26 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 43
SPI_MOSI	SPI_55S	SPI	SPI_CLK_MUX	43 51
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	43 51
SPI_MOSI_MUX	SPI_55S	SPI	SPI_MOSI_MUX	43 51
SPI_MISO	SPI_55S	SPI	SPI_MISO_MUX	43 51
SPI_MISO	SPI_55S	SPI	SPI_MISO_R	51
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008

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NONE	051-7852	A.0.1
SHT	72	OF
		76



8 7 6 5 4 3 2 1

MCP RGMI (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD 18
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND 18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R 18 33
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0 18 33
ENET_INTR_I	ENET_MII_55S	ENET_MII	ENET_INTR_L 18 32
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC 18 32
ENET_PWRDWN_I	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L 18 32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 18 32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R 32
ENET_RXD_STEAD	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK 18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0> 18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1> 18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL 18 32
ENET_RESET_I	ENET_MII_55S	ENET_MII	ENET_RESET_L 18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0> 32 34
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0> 32 34

D  
C  
B  
A

D  
C  
B  
A

**Ethernet Constraints**  
 SYNC\_MASTER=K36B\_MLB SYNC\_DATE=08/17/2008  
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	D	051-7852	A.0.1
SCALE	SHT		OF
NONE	73		76

8 7 6 5 4 3 2 1

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### FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

### FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	COUNT
	PHYSICAL	SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_P	37
FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_N	37
FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_P	37
FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_N	37

Port 2 Not Used

D

D

C

C

B

B

A

A


**FireWire Constraints**

SYNC\_MASTER=K36B\_MLB      SYNC\_DATE=08/17/2008

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	D	051-7852	A.0.1
SCALE	SHT	OF	
NONE	74	76	

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

### SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB 55G	SMB	SMBUS_SMC_A_S3_SCL 44
SMBUS_SMC_A_S3_SDA	SMB 55G	SMB	SMBUS_SMC_A_S3_SDA 44
SMBUS_SMC_B_S0_SCL	SMB 55G	SMB	SMBUS_SMC_B_S0_SCL 44
SMBUS_SMC_B_S0_SDA	SMB 55G	SMB	SMBUS_SMC_B_S0_SDA 44
SMBUS_SMC_0_S0_SCL	SMB 55G	SMB	SMBUS_SMC_0_S0_SCL 44
SMBUS_SMC_0_S0_SDA	SMB 55G	SMB	SMBUS_SMC_0_S0_SDA 44
SMBUS_SMC_BSA_SCL	SMB 55G	SMB	SMBUS_SMC_BSA_SCL 44
SMBUS_SMC_BSA_SDA	SMB 55G	SMB	SMBUS_SMC_BSA_SDA 44
SMBUS_SMC_MGMT_SCL	SMB 55G	SMB	SMBUS_SMC_MGMT_SCL 44
SMBUS_SMC_MGMT_SDA	SMB 55G	SMB	SMBUS_SMC_MGMT_SDA 44

### SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

D

D

C

C

B

B

A

A


**SMC Constraints**

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	D	051-7852	A.0.1
SCALE	SHT OF		
NONE	75 76		

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K36B BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA_P1MM				MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	30 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM				
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.165 MM				
40_OHM_SE	*	Y	0.145 MM	0.145 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
27F4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM				
27F4_OHM_SE	*	Y	0.275 MM	0.275 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM	
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.109 MM	0.109 MM		0.220 MM	0.220 MM	
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.089 MM	0.089 MM		0.230 MM	0.230 MM	
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM	
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.152 MM	?
3X_DIELECTRIC	*	0.228 MM	?
4X_DIELECTRIC	*	0.304 MM	?
5X_DIELECTRIC	*	0.380 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

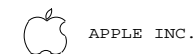
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

K36B RULE DEFINITIONS

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