K36C MLB SCHEMATIC

APR/29/2009

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Schematic / PCB #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE LEG</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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### BOM OPTION

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
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<td>CONN,RCPT,RJ45,NO FILTER,8P</td>
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<td>J3900</td>
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<td>514-0669</td>
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<td>J4600</td>
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<td>514-0665</td>
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<td>J6700</td>
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<td>514-0666</td>
<td>CONN,RCPT,3.5MM AUDIO OUT,R/A</td>
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<tr>
<td>338S0694</td>
<td>IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P</td>
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<td>338S0702</td>
<td>IC,GMCP,MCP79,35X35MM,BGA1437,B03</td>
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<tr>
<td>337S3777</td>
<td>PDC,SLGFF,2.13,,25W,1066,R0,3M,BGA,P7450</td>
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<td>W4100</td>
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<tr>
<td>341S2420</td>
<td>IC,SMC,HS8/2117,9X9MM,TLP,HF,BLANK</td>
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<td>U4100</td>
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<tr>
<td>341S2093</td>
<td>IC,CYPRESS,CY7C63833</td>
<td>1</td>
<td>U4800</td>
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<tr>
<td>341S2418</td>
<td>IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP</td>
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### ALTERNATES OPTION

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<td>U4100</td>
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<tr>
<td>341S2093</td>
<td>IC,CYPRESS,CY7C63833</td>
<td>1</td>
<td>U4800</td>
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<tr>
<td>341S2418</td>
<td>IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP</td>
<td>1</td>
<td>U5100</td>
</tr>
</tbody>
</table>

### BOARD STACK-UP AND CONSTRUCTION

**Top**
- SIGNAL
- GROUND
- SIGNAL(High Speed)
- SIGNAL(High Speed)
- GROUND
- POWER
- POWER
- GROUND
- SIGNAL(High Speed)
- SIGNAL(High Speed)
- GROUND

**Bottom**
- SIGNAL
1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)
<table>
<thead>
<tr>
<th>#35601 Fan Connectors</th>
<th># J4501 SATA HD System LED and IR</th>
<th># J3100 LPC+SPI Connector</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>#3400 Battery/Lid Connector</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td>#3600 MagSafe DC Power Jack</td>
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<tr>
<td>#3800 INVERTER Connector</td>
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</tr>
<tr>
<td>#39001 LCD + CAMERA CONNECTOR</td>
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<tr>
<td># J4701 MIC CONNECTOR</td>
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<tr>
<td># J4702 Left SPEAKER CONNECTOR</td>
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<td></td>
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<tr>
<td># J4703 Right SUB SPEAKER CONNECTOR</td>
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</tr>
<tr>
<td># J5800 GREYER AND DIMMO REMOTE TEMP SENSORS</td>
<td></td>
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<td># J5520 CPU/MB Thermal Sensor</td>
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<tr>
<td>#24800 BLUETOOTH</td>
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<tr>
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<td></td>
<td></td>
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<tr>
<td>#24800 SATA ODD</td>
<td></td>
<td></td>
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<tr>
<td></td>
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<td></td>
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</tbody>
</table>
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 30-9230 adapter board to support Mini-XDP debugging.

MCP79-specific pinout

Direction of XDP module

Please refer to the document on your referenced state of 2008.

CRITICAL
be used to provide HDMI or dual-channel TMDS without level-shifting. IFP interface can be used.

NOTE: HDMI port requires level-shifting. IFP interface can be used.

MII, RGMII products will enable feature.

NOTE: All Apple products set strap to IFP. Apple products will enable feature.

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MCP Ethernet & Graphics
SYNC FROM T18
REMOVE 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672

MCP Graphics Support
Apple Inc.
301-3041 A
A.S.D
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OF SUCH DAMAGE.

www.vinafix.vn
CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS

CHANGE Y2810 AND U2850 TO SMALLER PARTS

ALIAS MEM_VTT_EN TO =DDRVTT_EN

SYNC FROM T18

CHANGE RESET BUTTON TO RESET PADS

REMOVE UNUSED PCIE_RESET SIGNALS

REMOVE R2824 AND NET FCI_CLK33M_SLOT_A

CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS

ALIAS MEM_VTT_EN TO =DDRVTT_EN

CHANGE Y2810 AND U2850 TO SMALLER PARTS
Voltage divider resistor values at op-amp outputs not yet finalized.

RMON OPTION TO SELECT VREF SOURCE

---

10mA max load

---

www.vinafix.vn
Page Notes

Power aliases required by this page:
- \[PP1V8\] MEM
- \[PPSPD\] S0 MEM (2.5V - 3.3V)

Separate winner required by this page:
- \[+/\]4V\_MEM\_50

Power aliases provided by this page:
- \[I2C\] MEM SCL

The 4.7μF and 1.0μF caps can be changed to 5× 2.2μF caps, when they get cheaper.

DDR2 Bypass Caps

For return current:
- C3101
- C3102

The 4.7μF and 1.0μF caps can be changed to 5× 2.2μF caps, when they get cheaper.

DDR2-800

DDR2 SO-DIMM Connector A

Apple Inc.

021-0019

A.0.0

Rev. 0

PIN 1 OF 109

All Design_Sheets

www.vinafix.vn
The 4.7μF and 1.0μF caps can be changed to 5x 2.2μF caps, when they get cheaper.
TXDLY = 0 (No TXCLK Delay)
RXDLY = 0 (RXCLK transitions with data)
PHYAD = 01 (PHY Address 00001)

If false, ENET_RESET_L should be removed.
If true, RC and 0-ohm resistor should be removed.

WF: Verify that ENET_RESET_L does not assert when WOL is active.

WF: Marvell numbers, update for Realtek

IN ENET_CLK125M_TXCLK

IN ENET_RESET_L

(19mA typ - Energy Detect)
(43mA typ - 1000base-T)

IN ENET_CLK125M_RXCLK

R3796 MF-LF 1/16W

C3727 NO STUFF 0.1UF

R3700 MF-LF 5%

C3727 NO STUFF 0.1UF

R3720 MF-LF 1/16W 10K

C3705 C3700 X5R 0.1UF

C3714 X5R 16V

C3715 0.1UF

R3750 MF-LF 4.7K

R3752 MF-LF 1/16W 4.7K

C3716 X5R

C3711 X5R 16V

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

R3793 R3792 R3791 R3790 22

C3711 10% 2

R3757 4.7K

C3714

C3715 0.1UF

VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6 MM
PP3V3_ENET_PHYAVDD
L3705 FERR-120-OHM-1.5A
0402-LF
1
22
MF-LF
1/16W
5%

8
7
6
5
4
3
2
1
A
B
C
D

Configuration Settings:

Max = +1 max address 0x2555
Min = +1 max address 0x2555
Reset = +1 no reset signal
Clear = +1 no clear signal
WLAN Enable Generation

WLAN = (S3 && AP_PWR_EN && (AC || S0))

Pull-up is with power FET.

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

Recommend aliasing PM_SLP_RMGT_L and ARB for alternate power options.

1.8V Vgs

MOBILE:

3.3V ENET FET

Rds(on) = 90mOhm max

I(max) = 1.7A (85°C)

WLAN Enable Generation

WLAN = (S3 && AP_PWR_EN && (AC || S0))

Pull-up is with power FET.

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

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Recommend aliasing PM_SLP_RMGT_L and ARB for alternate power options.

1.8V Vgs

MOBILE:

3.3V ENET FET

Rds(on) = 90mOhm max

I(max) = 1.7A (85°C)
**ODD Power Control**

**SATA ODD Port**

**SATA Connector**

**SYSTEM (SLEEP) LED FILTER**

---

**PLACEMENT NOTE:**
- Place FL4520 close to J4500
- Place C4520 close to MCP79
- Place C4521 next to C4520
- Place C4525 next to C4526
- Place C4526 close to J4500
- Place C4525 close to J4500
- Place FL4525 close to J4500

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**SYNC DATE:** 08/17/2008
**SYNC MASTER:** K36B_MLB

Apple Inc.

---

**PAGE TITLE:** SATA Connectors

**DRAWING NUMBER:** 051-8089
**SIZE:** D

**BRANCH:** A

**REVISION:** A.0.0

**PAGE:** 45 OF 109
Alternate SPI ROM Support

SPI Bus Series Resistance Option

LPC+SPI Connector

Critical components are marked with a star: CRITICAL.
PLACEMENT NOTE
PLACE L5800,L5801,L5803 NEAR J5800
PLACE D5800 NEAR J5800
PLACE D5800 CLOSE J5800

GEYSER

PLACE D5800 CLOSE J5800
Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

Package Top

Top-through View
MCP79 SPI Frequency Select

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
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<tr>
<td>1 MHz</td>
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<td>0</td>
</tr>
<tr>
<td>42 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>25 MHz</td>
<td>1</td>
<td>0</td>
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<tr>
<td>42 MHz</td>
<td>1</td>
<td>1</td>
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</table>

25MHz IS SELECTED WITH R5164 AND R5144
ANY OF THE 4 FREQUENCIES CAN BE SELECTED
WITH R6190, R6191, R5164 AND R5144

www.vinafix.vn
SATELLITE & SUB TWEETER AMPLIFIER  APN:353S1595

SATELLITE  169 Hz < FC < 282 Hz
SUB        80 Hz < FC < 132 Hz
GAIN       12DB

MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM
VOLTAGE=5V

L6620 - L6630
R6610 - R6620
C6601 - C6610
C6611 - C6620
C6621 - C6630

MAX9705_R_N
SPKRAMP_THERMPANE

Sub-Tweeter

Page 1 of 10
1.8V/0.9V (DDR2) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

Place XW7303 by C7308.

ROUTING NOTE:
SM

Put one bulk cap next to the load.

MAX CURRENT = 12A
PWM FREQ. = 400 KHZ

Put one bulk cap next to the cap.

Apple Inc.
IMVP6 CPU VCore Regulator

LATEST ISSUE: 2007/01/23

PWM FREQ. = 300 KHZ
MAX CURRENT = 44A
LOAD LINE SLOPE = -2.1 mV/A

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

www.vinafix.vn
for C segment: 75 ohm from FL to connector, top/bottom layer width is 0.076 mm.

for B segment: 50 ohm B/W 2 150 PF res. inner layer width is 0.09 mm top/bottom layer width is 0.115 mm

for A segment: 37.5 ohm from MCP to 150 ohm PD res: Top/bottom layer width is 0.18 mm

for VG signal trace, we need to follow NV's recommendation. So we need to change the segment impedance based on NV design guide.

NOTE: CRT_DDC_* ARE NOT 5V COMPLIANT

R9493, R9494, R9495 PLACE CLOSE TO U1400

CRT_DDC_B_COMP_PB
CRT_DDC_G_Y_Y

67

8 7 5 4 2 1

8 7 5 4 2 1

R9493

VOLTAGE=5VMIN_LINE_WIDTH=0.30 MM

1%

MF-LF
1/16W

MIN_NECK_WIDTH=0.20 MM

150

R9493

402

1

2.7K

MF-LF
1/16W

1%

150

402

MF-LF
1/16W

1%

150

402

2.7K

402

MF-LF

2

2.7K

402

MF-LF

2

1% 2.7K

0.5 AMP-13.2V

1 2

F9404

CRITICAL
SM-HF

R9490, R9491, R9492 PLACE CLOSE TO FL9400

SOT563

R9490

1%

MF-LF
1/16W

150

MIN_LINE_WIDTH=0.5 MMVOLTAGE=5V

MIN_NECK_WIDTH=0.25 MM

R9490

1%

MF-LF
1/16W

150

R9491

1%

MF-LF
1/16W

150

R9492

1%

MF-LF
1/16W

150

R9490

1%

MF-LF
1/16W

150

R9491

1%

MF-LF
1/16W

150

R9492

1%

MF-LF
1/16W

150
Some signals require 27.4-ohm single-ended impedance.

**NOTE:** 7 mil gap is for VCC_Sense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Signals within each 1x group should be matched to CPU clock, ±0/-1000 mils.

FSB 1x signals shown in signal table on right.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to ±300 ps.

FSB 4x signals / groups shown in signal table on right.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

---

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
</tr>
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<tbody>
<tr>
<td><strong>CPU/FSB Constraints</strong></td>
<td><strong>CPU/FSB Net Properties</strong></td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th><strong>CPU Signal Constraints</strong></th>
<th><strong>CPU/FSB Constraints</strong></th>
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<tbody>
<tr>
<td>Min. recommended at least 90 mils, 65 mils preferred</td>
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<table>
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<tr>
<th><strong>MCP FSB COM# Signal Constraints</strong></th>
<th><strong>CPU/FSB Constraints</strong></th>
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<tbody>
<tr>
<td>Min. recommended at least 90 mils, 65 mils preferred</td>
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<thead>
<tr>
<th><strong>FSB Clock Constraints</strong></th>
<th><strong>CPU/FSB Constraints</strong></th>
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| **SOURCE:** Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4 | **SOURCE:** MCP79 Interface DG (DG-03328-001_v01), Section 2.2 |

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|  |  |
|  |  |

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**SOURCE:** Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

**SOURCE:** MCP79 Interface DG (DG-03328-001_v01), Section 2.2
**MCP MEM COMP Signal Constraints**

- Source: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
- A/BA/cmd signals should be matched within 5 ps of CLK pairs.
- A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
- DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
- DQ signals should be matched within 20 ps of associated DQS pair.

**Memory Bus Spacing Group Assignments**

- Table shows the wire spacing and placement rules for different signal pairs.

**Memory Bus Constraints**

- Table details the constraints for various memory bus connections.

**Memory Net Properties**

- Table provides properties for different memory nets, including signal names and their corresponding values.

---

**Memory Constraints**

Apple Inc.

Sheet: 051-8089

Revision: A.0.0

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**Memory Bus Spacing Group Assignments**

- Table provides spacing rules for different memory bus connections.

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**Memory Constraints**

Apple Inc.

Sheet: 051-8089

Revision: A.0.0

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**Memory Bus Spacing Group Assignments**

- Table provides spacing rules for different memory bus connections.

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**Memory Constraints**

Apple Inc.

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### K36B BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

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#### Physical Rule Definitions

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