3. All crystals & oscillator values are in Hertz.

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**APPLE INC.**

---

**Schematic / PCB #’s**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE NUM</th>
<th>CRITICAL</th>
<th>REV</th>
<th>SHEET OPTION</th>
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</table>

---

**METRIC**

---

**DATE**

**APR/10/2009**
**Board Stack-Up and Construction**

**Top**
- SIGNAL
- GROUND
- SIGNAL (High Speed)
- SIGNAL (High Speed)
-功率
- POWER
- GROUND
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- SIGNAL

**Bottom**
- SIGNAL

---

**Configuration Options**

- Sync Master: K36B_MLB
- Sync Date: 08/17/2008

---

**Table**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Description</th>
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<tbody>
<tr>
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</tr>
<tr>
<td>U4100</td>
<td>Ic, Fw643E, 1394B Phy/OHCI Link/PCI-e, 127</td>
</tr>
<tr>
<td>U4800</td>
<td>Ic, Cypress, Cy7C63833</td>
</tr>
<tr>
<td>U1400</td>
<td>Ic, Gmpc, Mcp79, 35X35Mm, Bga1437, B03</td>
</tr>
<tr>
<td>U3700</td>
<td>Ic, Rtl8251Ca-Vb-Gbe Transceiver, 48P</td>
</tr>
<tr>
<td>U3300</td>
<td>Ic, Smd, Hs8/2117, 9x9Mm, Tlp, Hf, Blank</td>
</tr>
<tr>
<td>U6100</td>
<td>Ic, Flash, Spi, 32MBit, 3.3V, 86Mhz, 8-Sop</td>
</tr>
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</tr>
<tr>
<td>U1400</td>
<td>Ic, Cypress, Cy7C63833</td>
</tr>
</tbody>
</table>
1.05V to 3.3V level translator (K36B: on ICT fixture)

From XDP connector or via level translator

From XDP connector

To XDP connector and/or level translator

CPU

MCP

XDP connector

XDP connector

JTAG scan chain
Functional Test Points

# J4501 SATA HD System LED and IR

# J3400 Airport

# Other Func Test Points

# J1300 XDP

# J5100 LPC+SPI Connector

---

APPLE INC.
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC FROM T18

NEED 1.5V POWER SOURCE

PLACEMENT_NOTE=Place R1101 within 25.4mm of CPU, no stubs.
PLACEMENT_NOTE=Place R1100 within 25.4mm of CPU, no stubs.

24A (LV Design Target)
23A (SV HFM)
44A (SV Design Target)
2500mA (after VCC stable)
4500mA (before VCC stable)
23A (LV Design Target)
41A (SV HFM)
30.4A (SV LFM)

www.vinafix.vn
CPU VCore HF and Bulk Decoupling

VCCA (CPU AVdd) DECOUPLING
- 6x 330uF, 2x 22uF 0805 (20 stuffed)

PLACEMENT NOTE (C1240-C1243):
- VCCP (CPU I/O) DECOUPLING
  - Place inside socket cavity on secondary side.

PLACEMENT NOTE (C1250-C1251):
- Place near CPU pin B26.

PLACEMENT NOTE (C1260-C1261):
- Place inside socket cavity on secondary side.

CPU VCore HF and Bulk Decoupling

VCCP (CPU I/O) DECOUPLING
- 1x 330uF, 2x 0.1uF 0402

PLACEMENT NOTE (C1200-C1203):
- 6x 330uF, 32x 22uF 0805 (20 stuffed)

CPU Decoupling

SYNC FROM T18

www.vinafix.vn
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
See with XDP-ACS adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

Use with 920-0620 adapter board to support CPU, MCP debugging.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

8 7 6 5 4 3 2 1
8 7 6 5 4 3 2 1
8 16 24

=PP1V8R1V5_S0_MCP_MEM

40.2 MF-LF 1/16W R1610 402 40.2 MF-LF 1/16W 1

87 mA (A01) 24

PP1V05_S0_MCP_PLL_CORE 70 70

TP_MEM_A_CKE<3> MCP_MEM_COMP_VDD

TP_MEM_A_ODT<3> TP_MEM_A_CS_L<3>

TP_MEM_A_ODT<2> TP_MEM_A_CS_L<2>

TP_MEM_A_CLK3N TP_MEM_A_CLK3P

TP_MEM_A_CLK5N TP_MEM_A_CLK4P

TP_MEM_A_CLK5P

MCP_MEM_COMP_GND

9 mA

39 mA

12 mA

19 mA

17 mA

4771 MA (A01, DDR2)
IF PE1 INTERFACE IS NOT USED, GROUND DVDD1_PEX AND AVDD1_PEX.

IF PE0 INTERFACE IS NOT USED, GROUND DVDD0_PEX AND AVDD0_PEX.
SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672
CHANGE Y2810 AND U2850 TO SMALLER PARTS

ALIAS MEM_VTT_EN TO =DDRVTT_EN

CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS

REMOVE UNUSED PCIE RESET SIGNALS

SYNC FROM T18

RTC Power Sources

PLATFORM RESET CONNECTIONS

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

RTC Crystal

MCP 25MHZ CRYSTAL

Reset Button

MCP 50 PWRGD
Voltage divider resistor values at op-amp outputs not yet finalized.

**ROM OPTION TO SELECT VREF SOURCE**

- Voltage divider resistor values at op-amp outputs not yet finalized.

**Table 5**

<table>
<thead>
<tr>
<th>CRITICAL BOM OPTION</th>
<th>TABLE 5 HEAD</th>
<th>TABLE 5 ITEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR=0x98(WR)/0x99(RD)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

- Power aliases required by this page:
  - ADDR=0x30(WR)/0x31(RD)

- Signal aliases required by this page:
  - I2C_VREFDACS_SCL
  - I2C_VREFDACS_SDA
  - PP3V3_S3_VREFMRGN
  - PPVTT_S3_DDR_BUF

**BOM options provided by this page:**

- ADDR=0x98(WR)/0x99(RD)

*Voltage divider resistor values at op-amp outputs not yet finalized.*
Signal aliases required by this page:
- =PPSPD_S0_MEM (2.5V - 3.3V)

Scale:

Page Notes

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Signal aliases required by this page:
- =I2C_SODIMMA_SDA

The 4.7μF and 1.0μF caps can be changed to 2x 2.2μF caps, when they get cheaper.

The 4.7μF and 1.0μF caps can be changed to 3x 2.2μF caps, when they get cheaper.
One cap for each side of every BPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it

LAYOUT NOTE: PLACE ONE CAP Close to EVERY TWO PULLUP RESISTORS TERMINATED TO FPDV9_50_MEN_TERM
WLAN Enable Generation

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

WLAN Enable Generation

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

1.05V ENET FET

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

Ethernet & AirPort Support

NOTE: Ethernet & AirPort Support

www.vinafix.vn
Page Notes

- Power aliases required by this page:
  - =PPBUS_S5_FWPWRSW (system supply for bus power)
  - =PPBUS_S5_FET
  - =PPBUS_FW_FWPWRSW
  - =PP3V3_FW_LATEVG
  - =PP2V4_FW_LATEVG

- Signal aliases required by this page:
  - =PPBUS_S5_FW_FET
  - =PPBUS_FW_FWPWRSW
  - =PPBUS_FW_FWPWRSW_D
  - =PPBUS_FW_FWPWRSW_F

BOM options provided by this page:

- NONE

Page Notes

- Notice of Proprietary Property

A

B

C

D

www.vinafix.vn
CPU Voltage Sense / Filter

MCP Voltage Sense / Filter

PBUS VOLTAGE SENSE ENABLE & FILTER

VOLTAGE SENSING
CPU T-Diode Thermal Sensor

- Internal Diode in U5515 detects CPU proximity temperature
- Detect CPU die temperature
- Detect FIn-stack temperature
- Detect Heat-pipe temperature

MCP T-Diode Thermal Sensor

- Internal Diode in U5535 detects MCP proximity temperature
- Detect MCP die temperature
- Detect CPU thermal sensor

Placement Note: Place U5535 near MCP
Placement Note: Place U5515 near CPU

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ANALOG SMS

SMS_X_AXIS = PP3V3_S3_SMS
SMS_Y_AXIS = PP3V3_S5_SMC
SMS_Z_AXIS = SMS_SELFTEST
SMS_ONOFF_L = SMS_PWRDN
MAKE_BASE = TRUE
SYNC_MASTER = K36B_MLB
SYNC_DATE = 08/17/2008

Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

+Z (up) +X Front of system +Y

-20% X5R 603 10UF 6.3V C5926 1 2

1/16W 5% 402 10K MF-LF R5920 1 2

1/16W 5% 402 10K MF-LF R5921 1 2

0.1uF 20% 10V CERM 402 C5920 1 2

0.01UF 20% 16V CERM 402 C5906 1 2

0.01UF 20% 16V CERM 402 C5905 1 2

SMSTXT_L SHOULD BE PULL UP IF NOT USED.

OUT OUT IN OUT

VOUTX VOUTY VOUTZ

VDD

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC

NC NC NC
25MHz is selected with R5164 and R5144
Any of the 4 frequencies can be selected with R6190, R6191, R5164 and R5144
DO WE NEED TO CHANGE BATTERY CONNECTOR?

1-Wire OverVoltage Protection

3.425V "G3Hot" Supply

LID HALL EFFECT SENSOR

BATTERY/LID CONNECTOR

DC-In & Battery Connectors

MagSafe DC Power Jack
5V_RT/3.3V POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2

PWM FREQ. = 300 KHZ
MAX CURRENT = 4A
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V

8 7 6 5 4 3 2 1
8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1
FireWire 1.0V (Core) Supply

MCP 1.05V_S5 AUXC SUPPLY

1.5V S0 SWITCH

VOUT = 0.6V * (1 + Ra / Rb)

VOUT = 0.6V * (1 + Ra / Rb)
Power Control Signals

3.3V (RIGHT AND LEFT), 3.3V AND 1.5V S0 RAILS MONITOR CIRCUIT

Layout Note: Add XW if needed to save space for pin 2,10,1,9

Power Sequencing

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MCP79 DDRVTT FET

MCP79 DDRVTT FET is used to provide the necessary current to ensure the memory is powered during sleep mode. It is connected to the memory VTT rail and provides a low impedance path for the memory to maintain its state during sleep.

**Important Notes:**
- **Power FETs:**
  - MCP79 DDRVTT FET
  - MCPDDR_EN_L
  - MCPDDR_SS

**Components:**
- Q7901, Q7903, Q7910, Q7930
- 3.3V S3 FET
- 1.8V S0 FET

**Resistors:**
- R7901, R7930
- 100K ohm

**Capacitors:**
- C7902, C7903, C7910
- 0.033uF

**Diodes:**
- SSM6N15FEAPE

**Other Components:**
- SOT563
- SOD-VESM-HF

**Schematic Diagram:**
- A to D

**References:**
- www.vinafix.vn
for C segment: 75 ohm from FL to connector, top/bottom layer width is 0.076 mm.

for B segment: 50 ohm B/W 2 150 PF res. inner layer width is 0.09 mm top/bottom layer width is 0.115 mm

for A segment: 37.5 ohm from MCP to 150 ohm PD res. Top/bottom layer width is 0.18 mm

For VG signal trace, we need follow NV's recommendation. So we need change the segment impedance base on NV design guide.
### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Memory Bus Constraints</th>
<th>Min.</th>
<th>Max.</th>
<th>Width</th>
<th>Min.</th>
<th>Max.</th>
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<tbody>
<tr>
<td>MCP Mem Compl Signal Constraints</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DQ/A/BA/cmd signal spacing</td>
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<td></td>
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</tr>
<tr>
<td>DQS/CLK</td>
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### Memory Bus Spacing Group Assignments

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<th>Memory Bus Spacing Group Assignments</th>
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<th>Max.</th>
<th>Width</th>
<th>Min.</th>
<th>Max.</th>
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<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
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### Memory Net Properties

<table>
<thead>
<tr>
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<th>Min.</th>
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<tbody>
<tr>
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<tr>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
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### Memory Constraints

<table>
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<th>Min.</th>
<th>Max.</th>
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<tbody>
<tr>
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<td></td>
</tr>
<tr>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
</tbody>
</table>

### Notes:

- DQ signals should be matched within 5 ps of associated DQS pair.
- CLA intra-pair matching should be within 75 ps, no CLA matching requirement.
- DDR2 intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
- DDR3 intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
- DDR3 DQ signals should be matched within 75 ps, no CLA matching requirement.
- CLA intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
- MCP Mem Compl Signal Constraints
  - MCP Mem Compl Signal Constraints
  - MCP Mem Compl Signal Constraints
### Digital Video Signal Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
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<tbody>
<tr>
<td>50-ohm</td>
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### Analog Video Signal Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>50-ohm</td>
<td>1</td>
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</table>

### Physical Rule Set

<table>
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<tr>
<th>Rule Type</th>
<th>Layer</th>
<th>Minimum Line Width</th>
<th>Allow Route</th>
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<tr>
<td>LAYER_MINIMUM_NECK_WIDTH</td>
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### Electrical Constraint Set

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<tbody>
<tr>
<td>50-ohm</td>
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### Spacing Rule Set

<table>
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<td>LINE-TO-LINE_SPACING</td>
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### Area Type Spacing Rule Set

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<thead>
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<th>Rule Type</th>
<th>Layer</th>
<th>Minimum Line Width</th>
<th>Allow Route</th>
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**FireWire Interface Constraints**

**FireWire Net Properties**

**FireWire Constraints**
### SMC SMBus Net Properties

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### SMC SMBus Charger Net Properties

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### SMC Constraints

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