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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0000729452	ENGINEERING RELEASED		2009-05-21

K36C MLB SCHEMATIC

APR/29/2009

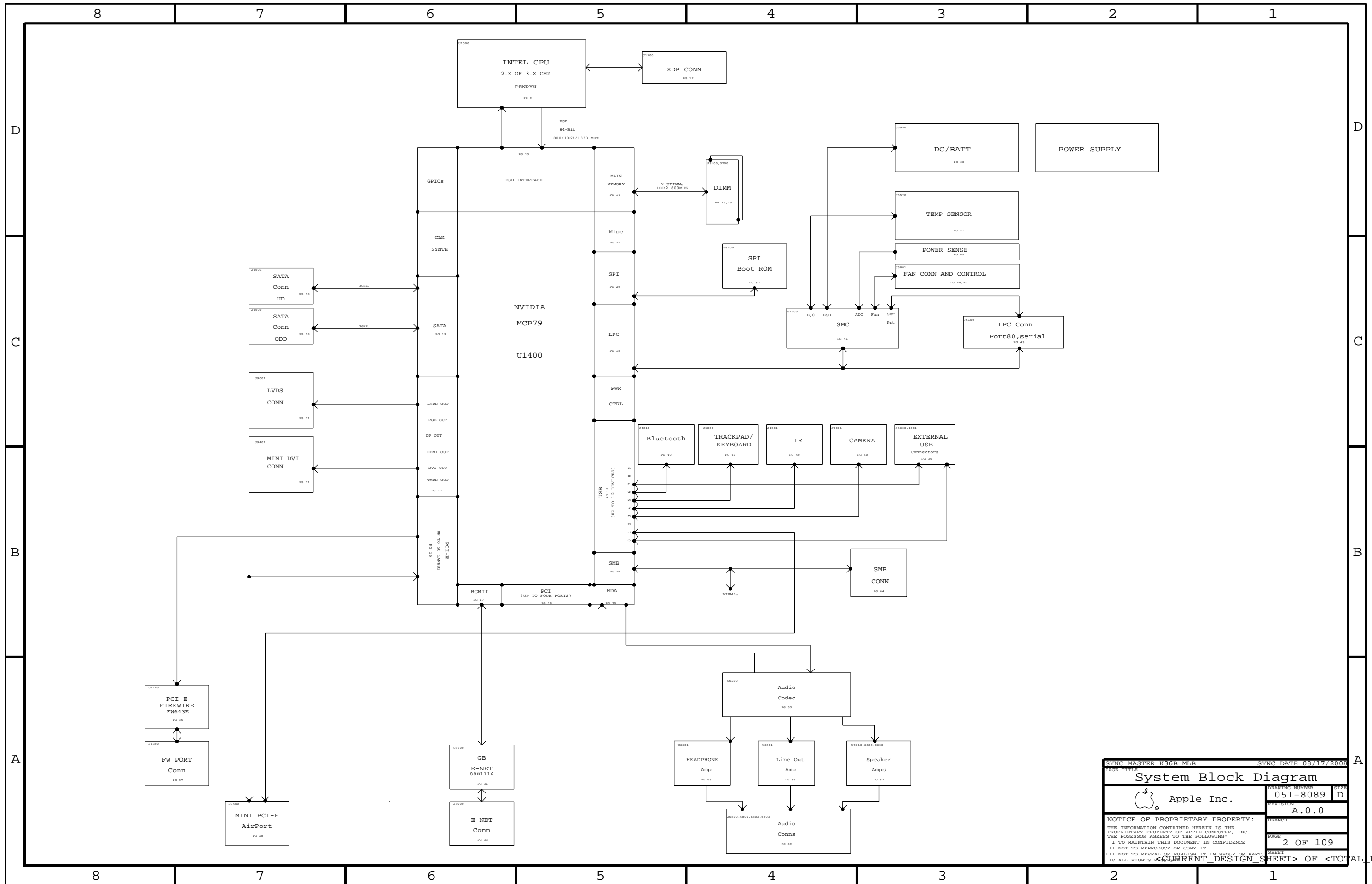
Page	(.csa)	Contents	Date
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2	2	System Block Diagram	K36B_MLB 08/17/2008
3	3	Power Block Diagram	K36B_MLB 08/17/2008
4	4	CONFIGURATION OPTIONS	K36B_MLB 08/17/2008
5	5	Revision History	K36B_MLB 08/17/2008
6	6	JTAG Scan Chain	K36B_MLB 08/17/2008
7	7	FUNC TEST	K36B_MLB 08/17/2008
8	8	Power Aliases	K36B_MLB 08/17/2008
9	9	SIGNAL ALIAS	K36B_MLB 08/17/2008
10	10	CPU FSB	K36B_MLB 08/18/2008
11	11	CPU Power & Ground	K36B_MLB 08/17/2008
12	12	CPU Decoupling	K36B_MLB 08/17/2008
13	13	eXtended Debug Port (MiniXDP)	M99_MLB 01/08/2008
14	14	MCP CPU Interface	K36B_MLB 08/17/2008
15	15	MCP Memory Interface	K36B_MLB 08/17/2008
16	16	MCP Memory Misc	K36B_MLB 08/17/2008
17	17	MCP PCIe Interfaces	K36B_MLB 08/17/2008
18	18	MCP Ethernet & Graphics	K36B_MLB 08/17/2008
19	19	MCP PCI & LPC	K36B_MLB 08/17/2008
20	20	MCP SATA & USB	K36B_MLB 08/17/2008
21	21	MCP HDA & MISC	K36B_MLB 08/17/2008
22	22	MCP Power & Ground	K36B_MLB 08/17/2008
23	24	MCP79 A01 Silicon Support	K36B_MLB 08/17/2008
24	25	MCP Standard Decoupling	K36B_MLB 08/17/2008
25	26	MCP Graphics Support	K36B_MLB 08/17/2008
26	28	SB Misc	K36B_MLB 08/17/2008
27	29	FSB/DDR2 VREF MARGINING	K36B_MLB 08/17/2008
28	31	DDR2 SO-DIMM Connector A	K36B_MLB 08/17/2008
29	32	DDR2 SO-DIMM Connector B	K36B_MLB 08/17/2008
30	33	Memory Active Termination	K36B_MLB 08/17/2008
31	34	Right Clutch Connector	K36B_MLB 08/17/2008
32	37	Ethernet PHY (RTL8211CL)	SUMA 03/20/2008
33	38	Ethernet & AirPort Support	SUMA 04/04/2008
34	39	ETHERNET CONNECTOR	SUMA 04/04/2008
35	41	FireWire LLC/PHY(FW643E)	K36B_MLB 08/17/2008
36	42	FireWire Port Power	K36B_MLB 08/17/2008
37	43	FireWire Ports	K36B_MLB (MASTER)

Page	(.csa)	Contents	Date
38	45	SATA Connectors	K36B_MLB 08/17/2008
39	46	External USB Connectors	K36B_MLB 08/17/2008
40	48	Front Flex Support	K36B_MLB 07/17/2008
41	49	SMC	K36B_MLB 08/17/2008
42	50	SMC Support	K36B_MLB 08/17/2008
43	51	LPC+SPI Debug Connector	K36B_MLB 08/17/2008
44	52	SMBUS CONNECTIONS	K36B_MLB 08/17/2008
45	53	VOLTAGE SENSING	K36B_MLB 08/17/2008
46	54	Current Sensing	K36B_MLB 08/17/2008
47	55	Thermal Sensors	K36B_MLB 08/17/2008
48	56	Fan	K36B_MLB 08/17/2008
49	58	GEYSER	K36B_MLB 08/17/2008
50	59	SMS	K36B_MLB 08/17/2008
51	61	SPI ROM	K36B_MLB 08/17/2008
52	62	AUDIO: CODEC	K36A_MLB 08/29/2008
53	66	AUDIO: SPEAKER AMP	K36A_MLB 08/29/2008
54	67	AUDIO: JACK	K36A_MLB 08/29/2008
55	68	AUDIO: JACK TRANSLATORS	K36A_MLB 08/29/2008
56	69	DC-In & Battery Connectors	RAYMOND 08/17/2008
57	70	PBUS Supply/Battery Charger	K36B_MLB 08/17/2008
58	72	5V/3.3V SUPPLY	K36B_MLB 08/17/2008
59	73	1.8V/0.9V DDR2 SUPPLY	K36B_MLB 08/17/2008
60	74	IMVP6 CPU VCore Regulator	K36B_MLB 08/17/2008
61	75	MCP VCore REGULATOR	K36B_MLB 08/17/2008
62	76	CPU VTT(1.05V) SUPPLY	K36B_MLB 08/17/2008
63	77	MISC POWER SUPPLIES	K36B_MLB 08/17/2008
64	78	POWER SEQUENCING	K36B_MLB 08/17/2008
65	79	POWER FETS	K36B_MLB 08/17/2008
66	90	INVERTER, LVDS	K36B_MLB 08/17/2008
67	93	TMDS ALIASES	K36B_MLB 08/17/2008
68	94	MINI-DVI CONNECTOR	K36B_MLB 08/17/2008
69	100	CPU/FSB Constraints	K36B_MLB 08/17/2008
70	101	Memory Constraints	K36B_MLB 08/17/2008
71	102	MCP Constraints 1	K36B_MLB 08/17/2008
72	103	MCP Constraints 2	K36B_MLB 08/17/2008
73	104	Ethernet Constraints	K36B_MLB 08/17/2008
74	105	FireWire Constraints	K36B_MLB 08/17/2008
75	106	SMC Constraints	K36B_MLB 08/17/2008
76	109	K36B RULE DEFINITIONS	K36B_MLB 08/17/2008

Schematic / PCB #'s

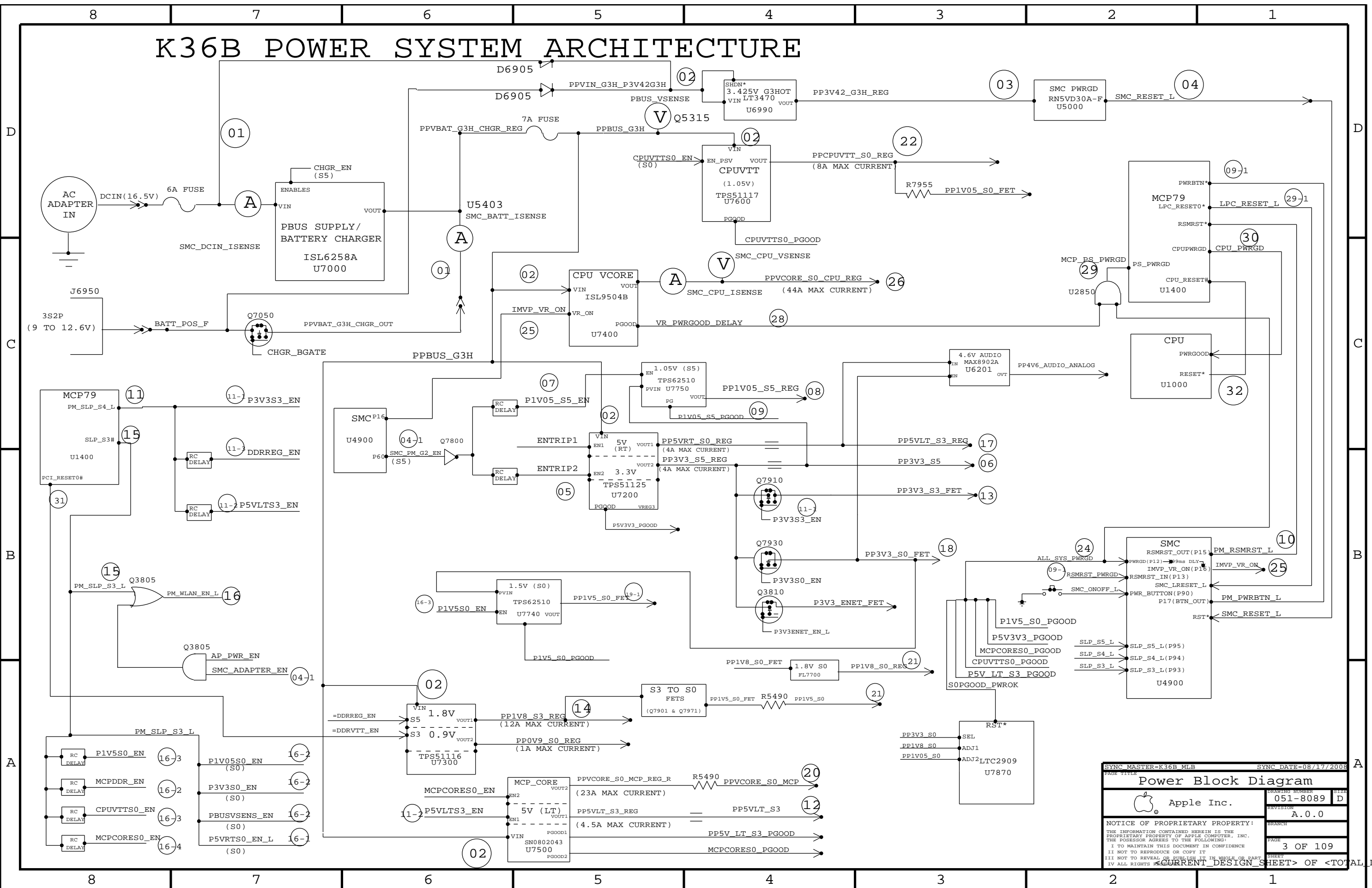
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8089	1	SCHEM, MLB, K36C	SCH	CRITICAL	
820-2496	1	PCBF, MLB, K36B	PCB	CRITICAL	

DRAWING TITLE		DRAWING NUMBER	SIZE
SCHEM, MLB, K36C		051-8089	D
Apple Inc.		REVISION	A.0.0
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SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
System Block Diagram			
		CREATION NUMBER	051-8089 D
		REVISION	A.0.0
		BINCH	
		PAGE	2 OF 109
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K36B POWER SYSTEM ARCHITECTURE



PAGE TITLE		SYNC DATE=08/17/2008	
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Apple Inc.		REVISION	
		A.0.0	
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2420	1	IC, BMC, HSB/2117, 9X99M, TLD, HP, BLANK	U4900	CRITICAL	SMC_PROG
341S2418	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, B-SOP	U6100	CRITICAL	BOOTROM_PROG
341S2093	1	IC, CYPRESS, CY7C63833	U4800	CRITICAL	
338S0654	1	IC, PWRMGR, 1394B, 90V/DMC, 512K/PC1-E, 127	U4100	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	[EEE:9WN]	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3777	1	PCB, SLAPP, 2.13, 25X, 1066, 80, 3M, BGA, P7450	U1000	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0702	1	IC, DMC9, 80279, 10X10MM, BGA1437, 803	U1400	CRITICAL	

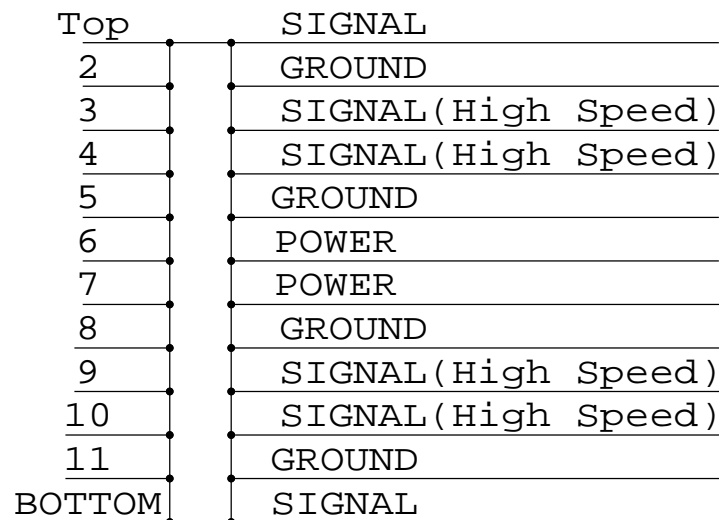
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0694	1	IC, RTL8281CA-VB-GR, GIGE TRANSCEIVER, 48P	U3700	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0665	1	CONN, RCPT, MINI-DVI, 32P, R/A	J9401	CRITICAL	
514-0666	1	CONN, RCPT, 3.5MM AUDIO IN, R/A	J6750	CRITICAL	
514-0667	1	CONN, RCPT, 3.5MM AUDIO OUT, R/A	J6700	CRITICAL	
514-0668	1	CONN, RCPT, RJ45, NO FILTER, SP	J3900	CRITICAL	
514-0669	1	CONN, RCPT, USB, 4P, MIDPLANE	J4600	CRITICAL	
514-0669	1	CONN, RCPT, USB, 4P, MIDPLANE	J4601	CRITICAL	

ALTERNATES OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0218		ALL	ALTERNATE PER CYNDI
152S0694	152S0138		ALL	ALTERNATE PER CYNDI
152S0847	152S0586		ALL	ALTERNATE PER CYNDI
152S0874	152S0516		ALL	ALTERNATE PER CYNDI
152S0796	152S0685		ALL	ALTERNATE PER CYNDI
152S0778	152S0693		ALL	ALTERNATE PER CYNDI
157S0058	157S0055		ALL	ALTERNATE PER CYNDI
516S0727	516S0588		ALL	
518S0704	518S0392		ALL	

BOARD STACK-UP AND CONSTRUCTION



PAGE TITLE		CONFIGURATION OPTIONS	
Apple Inc.		DESIGN NUMBER	051-8089
		REVISION	A.0.0
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Revision History

****2008/08/21****
PAGE 61:
- U7500 PIN V5DRV1 LINK TO PP5V_S0_MCPREG_VCC.
- U7500 PIN TONSEL LINK TO GND DIRECTLY.
PAGE 64:
- R7859 CHANGE TO 100 OHM.
- R7879 CHANGE TO 100K OHM.
PAGE 65:
- DELETE 1.05V S0 FET CIRCUIT.
PAGE 57:
- R7011 CHANGE TO 9.31K OHM, 1k
****2008/08/22****
PAGE 7:
- ADD SMC_EXCARD_PWR_EN TEST_POINT
PAGE 8:
- ADD =PP3V42_G3H_RTC_D LINK TO =PP3V42_G3H_REG
PAGE 14:
- R1410 CHANGE TO 49.9 OHM
- CHANGE R1440 TO 150_5% AND NO STUFF
PAGE 26:
- R2872 CHANGE TO 0OHM
- RTC FOLLOW M97 DESIGN AND USE SUPERCAP SOLUTION
- MCP S0 PWRGD FOLLOW M97 DESIGN
PAGE 29:
- PULL R3240 DOWN TO GND. PULL R3241 HIGH
PAGE 32,33,34
- FOLLOW M97 DESIGN
PAGE 39:
- D4600/D4601/PIN-6 CONNECT TO USB VBUS (FOLLOW M97D)
PAGE 44:
- R5270/R5271 = 1K (FOLLOW M97D)
- R5280/R5281 = 1K (FOLLOW M97D)
PAGE 68:
- CHANGE C9411, C9412 TO 220PF
- CHANGE R9462, R9463 TO 2.7KOHM
- ADD C9480 0.1UF_16V_0402 FROM GND_CHASSIS_TMDS_DOWN TO GND
- CHANGE R9460,R9461 TO 0OHM,
- CHANG C9442 AND C9443 TO 47PF
****2008/08/23****
MODIFY ALL NOSTUFF TO NO STUFF.
PAGE 6:
- REMOVE ETHERNET CIRCUIT.
PAGE 8:
- ADD =PP3V3_S5_P3V3ENETFET LINK TO PP3V3_S5
- ADD =P1V05_ENET_PHY LINK TO P1V2R1V05_ENET.
PAGE 9:
- ADD =RTL8211_ENSWRE LINK TO GND.
- ADD =PP3V3_ENET_PHY_VDDREG LINK TO TP_PP3V3_ENET_PHY_VDDREG.
- ADD =RTL8211_REGOUT LINK TO NC_RTL8211_REGOUT.
- =P3V3ENET_EN_L LINK TO PM_SLP_RMG_T_L
- =P1V05ENET_EN LINK TO PM_SLP_RMG_T_L
PAGE 10:
- CHANGE XDP_TDO_CONN TO XDP_TDO
PAGE 13:
- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.
PAGE 23:
- DELETE R2400-R2413 FOR MCP A01 VERSION.
PAGE 31:
- REMOVE R3400, R3401
- L3401 FROM NO STUFF CHANGE TO STUFF.
PAGE 39:
- DELETE R4699.
- R4690 FROM NO STUFF CHANGE TO STUFF.
PAGE 41:
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE
PAGE 46:
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE
- SMC_NB_CORE_ISENSE CHANGE TO SMC_MCP_CORE_ISENSE
- R5417 ADD BOM OPTION FOR NO STUFF
- R5416 ADD BOM OPTION FOR NO STUFF
PAGE 50:
- ADD C5926 (10UF,20%,0603) TO =PP3V3_S3_SMS
PAGE 63:
- REMOVE USB_PWR_EN_S3
PAGE 66:
- REMOVE R9010, R9011
****2008/08/24****
PAGE 6:
- R0602 BOMOPTION FROM JTAG_LDEV CHANGE TO NO STUFF.
PAGE 13:
- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.
PAGE 18:
- R1860 AND R1861 CHANGE TO PAGE 68.
PAGE 25:
- C2504-C2507 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
- C2516-C2517 FROM 138S0578(402) CHANGE TO 138S0614(402-1)
PAGE 35:
- R4150 FROM 118S0343 (0201) CHANGE TO 116S0056(0402)
PAGE 58:
- C7281, C7241, C7272 FROM 138S0555(603) CHANGE TO 138S0615(603-1)
- C7280, C7240 FROM 128S0092(POLY) CHANGE TO 128S0128(POLY-TANT)
- C7291, C7292, C7252, C7251 FROM 128S0115(POLY,CASE-B2) CHANGE TO 128S0222(POLY,CASE-B2-SM)
- Q7260, Q7261 FROM 376S0512 CHANGE TO 376S0652 (H-F)
PAGE 59:
- Q7320 FROM 376S0512 CHANGE TO 376S0652 (H-F)
- Q7321 FROM 376S0511 CHANGE TO 376S0651 (H-F)
- C7321 FROM 128S0111(POLY) CHANGE TO 128S0218 (POLY,CASE-D2E-SM)
- C7343 FROM 128S0073 CHANGE TO 128S0233.
PAGE 60:
- XW7400 ADD BOMOPTION OMIT.
- Q7400, Q7402 FROM 376S0472 CHANGE TO 376S0617.
PAGE 61:
- L7500 FROM 152S0869 CHANGE TO 152S0685.
- Q7500 FROM 376S0512 CHANGE TO 376S0652.
- C7560 FROM 128S0092 CHANGE TO 128S0218.
PAGE 62:
- Q7620 FROM 376S0512 CHANGE TO 376S0652.
- C7601 FROM 138S0578 CHANGE TO 138S0614.

****2008/08/25****
CHANGE CSA BASE ON WILL'S SUGGESTION.
PAGE 9:
- ADD GMUX_UTAG_TMS AND GMUX_UTAG_TDI IN MISC NC MCP79 ALIASES.
PAGE 18:
- NETNAME ENET_INTR_L CHANGE TO TP_ENET_INTR_L.
- ENET_PWRDWN_L CHANGE TO TP_ENET_PWRDWN_L
PAGE 19:
- DELETE R1987,R1988,R1995,R1970,R1971,R1972,R1973,R1996,R1997,R1998,R1999,R1978,R1979
(FOLLOW M97 DESIGN).
- NET DPMUX_LOWPWR_L SYNC M97 NETNAME AUD_IPHS_SWITCH_EN
- NET LVDSMUX_SEL_IG_L SYNC M97 NETNAME
- NET DPMUX_SEL_IG_L SYNC M97 NETNAME
PAGE 28:
- REMOVE NET DIMM_OVERTEMPA_L
PAGE 29:
- REMOVE NET DIMM_OVERTEMPA_L
PAGE 42:
- ADD SMC_EXCARD_PWR_EN TO TP_SMC_EXCARD_PWR_EN
- ADD SMC_RSTGATE_L TO TP_SMC_RSTGATE_L
- ADD ALS_GAIN TO NC_ALS_GAIN
- ADD ESTARLDO_EN TO NC_ESTARLDO_EN
- ADD SMC_ANALOG_ID TO NC_SMC_ANALOG_ID
- ADD SMC_SYS_KBDLED TO NC_SMC_SYS_KBDLED
- ADD R5054 10KOHM LINK SMC_GPU_ISENSE PULL DOWN TO GND.
- ADD R5055 10KOHM LINK SMC_NR_MISC_ISENSE PULL DOWN TO GND.
PAGE 43:
- R5142 CHANGE TO NO STUFF.
PAGE 46:
- R5416 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5417 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.
PAGE 57:
- NETNAME FROM CHGR_LOWCURRENT REF CHANGE TO CHGR_LOWCURRENT_REF
- NETNAME FROM CHGR_LOWCURRENT GATE CHANGE TO CHGR_LOWCURRENT_GATE
PAGE 5:
- REMOVE R7884 AND C7884
PAGE 66:
- REMOVE J9001 PIN 20 AND PIN21 NET.
****2008/09/02****
PAGE 45:
- CHANGE ODD CONNECTOR FROM 516S0720 TO 516S0719
****2008/09/27****
PAGE 9:
- ADD STANDOFF 860-0964 X 4
- ADD STANDOFF 860-0723 X 1
- ADD STANDOFF 860-0749 X 1
PAGE 29:
- REMOVE BOMOPTION TABLE OF R2903/R2905/R2909/R2911
PAGE 66:
- C6601/C6603 CHANGE TO APN 128S0135, and REMOVE BOMOPTION OMIT
- C6605 CHANGE TO APN 128s0148, HF APN 128s0221, and REMOVE BOMOPTION OMIT
PAGE 68:
- C6830/C6831 CHANGE TO APN 128S0220, and REMOVE BOMOPTION OMIT
PAGE 72:
- R7272 CHANGE FROM 57.6K 1%(114s0389) TO 75K 1%(114s0399)
****2008/10/20****
PAGE 29:
- ADD R2903/R2905 BOMOTION AND CHANGE VALUE TO 200 OHM
PAGE 50:
- REMOVE ALT TABLE
PAGE 74:
- REMOVE ALT TABLE
PAGE 94:
- REMOVE K36 BOM OPTION TABLE AND ALT TABLE
****2008/10/22****
PAGE 12:
- C1200 ~ C1219 CHANGE TO 138S0580
PAGE 28:
- C2870 CHANGE TO 138S0614
PAGE 37:
- ADD R3731 (116s0026 22 ohm 5%,0402) FOR EMI 125MHZ NOISE
- TP_RTL8211_CLK125 CHANGE TO RTL8211_CLK125
PAGE 48:
- C4803 CHANGE TO 138S0614
PAGE 66:
- C6605 CHANGE TO HF APN 128S0221
PAGE 70:
- C7040/C7041/C7047 CHANGE TO 138S0614
PAGE 90:
- L9002 CHANGE TO 116S0004(0ohm,5%,0402)
- C9003 CHANGE TO 116S0004(0ohm,5%,0402)
****2008/10/24****
PAGE 19:
- R1950/R1951/R1952/1953 CHANGE TO 116s0004 (0 OHM,5%,0402)
PAGE 28:
- R2825/R2826 CHANGE TO 116s0004 (0 OHM,5%,0402)
PAGE 34:
- J3400 516S0635 CHANGE TO HF APN 516S0729
PAGE 52:
- ADD C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281 131S1104 (22pf,5%,0402) NO STUFF
- TEXT "ALS" CHANGE TO "MINI-PCIE"
- I2C_ALS_SCL CHANGE TO I2C_MINI_PCIE_SCL
- I2C_ALS_SDA CHANGE TO I2C_MINI_PCIE_SDA
PAGE 67:
- J6700 514-0604 CHANGE TO HF APN 514-0521
- J6750 514-0603 CHANGE TO HF APN 514-0519
PAGE 69:
- J6950 516S0620 CHANGE TO HF APN 516S0735
****2008/10/25****
PAGE 52:
- STUFF C5250/C5251/C5270/C5271/C5260/C5261/C5280/C5281
****2008/10/28****
PAGE 34:
- J3400 516S0729 CHANGE TO 516S0635
****2008/10/30****
PAGE 69:
- J6950 516S0735 CHANGE TO 516S0620

****2008/10/31****
PAGE 41:
- U4100 CHANGE FROM 338S0523 TO 338S0654
****2008/11/01****
PAGE 4:
- BOM change U1400 CHANGE FROM 338S0678 TO 338S0702
****2008/11/05****
PAGE 62:
- C6210 CHANGE FROM 127S0062 TO 127S0108
PAGE 68:
- C6832, C6833 CHANGE FROM 127S0062 TO 127S0108
PAGE 45:
- DELETE L4502, NET SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N
- L4501 / F14520 / FL4525 CHANGE FROM 155S0303 TO 155S0371
PAGE 102:
- DELETE PHYSICAL/SPACING SETTING OF SATA_HDD_D2R_UF_P / SATA_HDD_D2R_UF_N
****2008/11/06****
- U5413 CHANGE FROM 353S1432 TO 353S2220
- R7417 CHANGE FROM 5.36K(114S0289) TO 4.42K(114S0280)
****2008/11/12****
- U1000 CHANGE FROM 373S3646 TO 373S3702
****2008/11/19****
- J6950 CHANGE FROM 516S0620 TO 516S0735
- J9401 CHANGE FROM 514-0517 TO 514-0665
- J6750 CHANGE FROM 514-0519 TO 514-0666
- J6700 CHANGE FROM 514-0521 TO 514-0667
- J3900 CHANGE FROM 514-0523 TO 514-0668
- J4600, J4601 CHANGE FROM 514-0527 TO 514-0669
- U3700 CHANGE FROM 338S0570 TO 338S0694
****2008/11/26****
- PAGE 61 NOTE : CORRECT REFERENCE TO R5164 AND R5144
- J3400 CHANGE TO 516S0729
****2008/12/12****
- R5144 and R5164 changed to 10K 5% 0402 (116S0090)
****2008/12/17****
- U4900 symbol update
****2008/12/20****
- R5156, R5157, R5158 change from 0 to 33 ohm, 5%, 0402(116s0030)

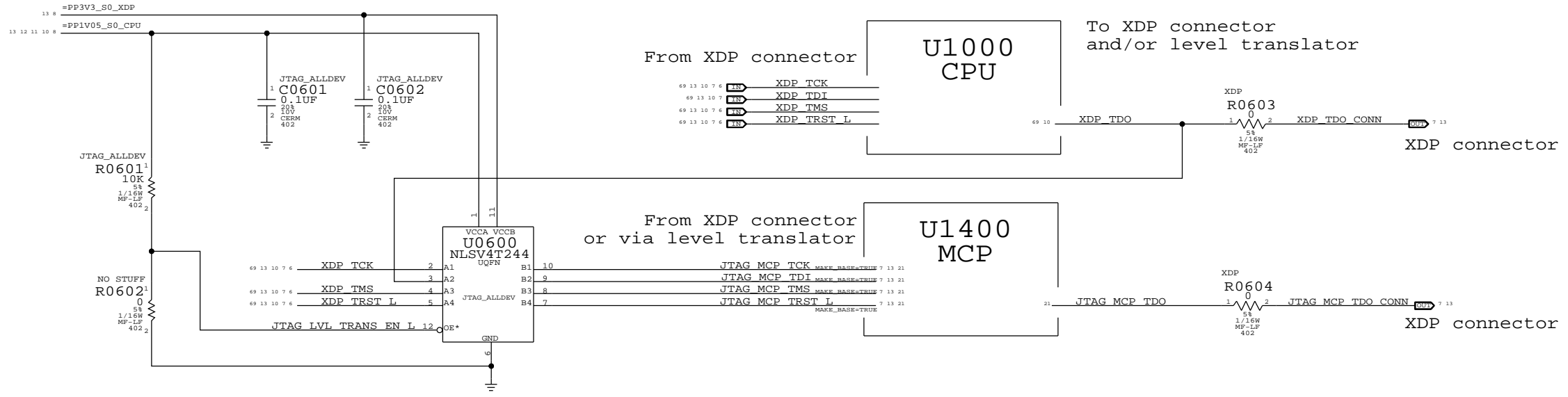
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C
B
A

D
C
B
A

Revision History table with columns: REVISION, DATE, BY, DESCRIPTION. Includes Apple Inc. logo and revision details like 051-8089, A.0.0, 5 OF 109 SHEETS.

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)



SYNC MASTER=K36B MLB		SYNC DATE=08/17//2008	
JTAG Scan Chain			
Apple Inc.		DRAWING NUMBER	051-8089 D
		REVISION	A.0.0
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		PAGE	6 OF 109
		SHEET	
<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>			

Functional Test Points

#J5601 Fan Connectors

```

8800 TRUE PP5VRT_S0 7 8
8801 TRUE FAN_RT_PWM 48
8802 TRUE FAN_RT_TACH 48
8803 TRUE GND
    
```

#J6950 Battery/Lid Connector

```

8970 TRUE SMC_BS_ALERT_L_F 56
8971 TRUE SMBUS_BATT_SCL_F 56
8972 TRUE SMBUS_BATT_SDA_F 56
8973 TRUE PVBAT_G3H_CONN_F 56
8974 TRUE SMC_LID_F 56
8975 TRUE GND_SMC_LID_F 56
8976 TRUE PP3V42_G3H_LIDSWITCH_F 56
8977 TRUE GND Need 6 TP
    
```

#J6900 MagSafe DC Power Jack

```

8920 TRUE PP18V5_DCN_FUSE Need 2 TP 56
8921 TRUE ADAPTER_SENSE 56
8922 TRUE GND Need 2 TP
    
```

#J9000 INVERTER Connector

```

8860 TRUE PPBUS_ALL_INV_CONN Need 2 TP 66
8861 TRUE INV_GND 66
8862 TRUE PP5V_INV_F 66
8863 TRUE INV_BKLIGHT_PWM_L Need 4 TP 66
    
```

#J9001 LCD + CAMERA CONNECTOR

```

8800 TRUE PP3V3_LCDVDD_SW_F 66
8801 TRUE PP3V3_S0_LCD_F 66
8802 TRUE LVDS_IG_DDC_CLK 18 66
8803 TRUE LVDS_IG_DDC_DATA 18 66
8804 TRUE LVDS_IG_A_DATA_N<0> 18 66 71
8805 TRUE LVDS_IG_A_DATA_P<0> 18 66 71
8806 TRUE LVDS_IG_A_DATA_N<1> 18 66 71
8807 TRUE LVDS_IG_A_DATA_P<1> 18 66 71
8808 TRUE LVDS_IG_A_DATA_N<2> 18 66 71
8809 TRUE LVDS_IG_A_DATA_P<2> 18 66 71
8810 TRUE LVDS_IG_A_CLK_F_N 66
8811 TRUE LVDS_IG_A_CLK_F_P 66
8812 TRUE USB2_CAMERA_CONN_P 66 72
8813 TRUE USB2_CAMERA_CONN_N 66 72
8814 TRUE PP5V_S3_CAMERA_F 66
8815 TRUE GND
    
```

J6701 MIC CONNECTOR

```

8816 TRUE MIC_LO_CONN 54
8817 TRUE MIC_HI_CONN 54
8818 TRUE MIC_SHLD_CONN 54 55
    
```

#J6702 Left SPEAKER CONNECTOR

```

8819 TRUE SPKRCONN_L_P_OUT 53 54
8820 TRUE SPKRCONN_L_N_OUT 53 54
    
```

#J6703 Right SUB SPEAKER CONNECTOR

```

8821 TRUE SPKRCONN_SUB_P_OUT 53 54
8822 TRUE SPKRCONN_SUB_N_OUT 53 54
8823 TRUE SPKRCONN_R_P_OUT 53 54
8824 TRUE SPKRCONN_R_N_OUT 53 54
    
```

J5800 GEYSER AND DIMMO REMOTE TEMP SENSORS

```

8825 TRUE TPAD_GND_F 49
8826 TRUE CONN_TPAD_ONOFF_FLTR_L 49
8827 TRUE CONN_TPAD_USB_P 49 72
8828 TRUE CONN_TPAD_USB_N 49 72
8829 TRUE SMC_LID_LC 49
8830 TRUE PP5V_S3_TPAD_F 49
    
```

#J5520 CPU/MCP Thermal Sensor

```

8831 TRUE CPUTHSNS_D2_P 47
8832 TRUE CPUTHSNS_D2_N 47
8833 TRUE MCPPHSNS_D2_P 47
8834 TRUE MCPPHSNS_D2_N 47
    
```

#J4810 BLUETOOTH

```

8835 TRUE PP3V3_S3_BT_F_CONN 40
8836 TRUE USB2_BT_F_N_CONN 40 72
8837 TRUE USB2_BT_F_P_CONN 40 72
8838 TRUE GND_BT_F_CONN 40
    
```

#J4500 SATA ODD

```

8839 TRUE SATA_ODD_R2D_UF_P 38 71
8840 TRUE SATA_ODD_R2D_UF_N 38 71
8841 TRUE SATA_ODD_D2R_C_N 38 71
8842 TRUE SATA_ODD_D2R_C_P 38 71
8843 TRUE PP3V3_S0 Need 4 TP 7 8
8844 TRUE SMC_ODD_DETECT 38 41
8845 TRUE GND Need 6 TP
    
```

J4501 SATA HD System LED and IR

```

8846 TRUE SATA_HDD_R2D_P 38 71
8847 TRUE SATA_HDD_R2D_N 38 71
8848 TRUE SATA_HDD_D2R_C_N 38 71
8849 TRUE SATA_HDD_D2R_C_P 38 71
8850 TRUE PP5V_S0_HDD_FLT Need 4 TP 38
8851 TRUE SYS_LED_ANODE_L 38
8852 TRUE IR_EX_OUT 38 40
8853 TRUE PP5V_S3_IR_CONN 38
8854 TRUE GND Need 4 TP
    
```

#J3400 Airport

```

8855 TRUE PCIE_WAKE_L 17 31
8856 TRUE MINI_CLKREQ_L 17 31
8857 TRUE PCIE_CLK100M_MINI_N 17 31 71
8858 TRUE PCIE_CLK100M_MINI_P 17 31 71
8859 TRUE PCIE_MINI_D2R_N 17 31 71
8860 TRUE PCIE_MINI_D2R_P 17 31 71
8861 TRUE PCIE_MINI_R2D_N 31 71
8862 TRUE PCIE_MINI_R2D_P 31 71
8863 TRUE PP3V3_WLAN Need 4 TP 31
8864 TRUE PP1V5_S0_R Need 3 TP 7 8
8865 TRUE MINI_RESET 31
8866 TRUE PP3V3_S3_AIRPORT_CONN 31
8867 TRUE I2C_MINI_PCIE_SCL 31 44
8868 TRUE I2C_MINI_PCIE_SDA 31 44
8869 TRUE USB2_AIRPORT_N 31 72
8870 TRUE USB2_AIRPORT_P 31 72
8871 TRUE GND Need 6 TP
    
```

Other Func Test Points

```

8872 TRUE ALL_SYS_PWRGD 26 41 44
8873 TRUE PPVCORE_S0_CPU 8
8874 TRUE PPCPUVTT_S0 8
8875 TRUE PPVCORE_S0_MCP_R 8
8876 TRUE PPVCORE_S0_MCP 8
8877 TRUE PP0V9_S0 8
8878 TRUE PP1V05_S0 8
8879 TRUE PP1V5_S0_R 7 8
8880 TRUE PP1V8_S0 8
8881 TRUE PP1V8_S0_R 8
8882 TRUE PP1V05_S0_MCP_PEX_AVDD 8 24
8883 TRUE PP1V05_S0 8
8884 TRUE PP1V05_S0_MCP_SATA_AVDD 8 24
8885 TRUE PP1V05_S0 7 8
8886 TRUE PP5VRT_S0 7 8
8887 TRUE PP3V3_S0 7 8
8888 TRUE PP1V0_PWM 8
8889 TRUE PP1V8_S3 8
8890 TRUE PP3V3_S3 8
8891 TRUE PP5VLT_S3 8
8892 TRUE PPVTT_S3_DDR_BUF 8
8893 TRUE PP1V05_S5_REG 8
8894 TRUE PP3V3_S5 8
8895 TRUE PP3V42_G3H 7 8
8896 TRUE PP18V5_G3H 8
8897 TRUE PPBUS_G3H 8
8898 TRUE PPBUS_G3H_CPU_ISNS 8
8899 TRUE PP3V3_ENET_PHY 8
8900 TRUE PP1V2R1V05_ENET 8
8901 TRUE PPVP_FW 8
    
```

#J1300 XDP

```

8892 TRUE XDP_BPM_L<5> 10 13 69
8893 TRUE XDP_BPM_L<4> 10 13 69
8894 TRUE XDP_BPM_L<3> 10 13 69
8895 TRUE XDP_BPM_L<2> 10 13 69
8896 TRUE XDP_BPM_L<1> 10 13 69
8897 TRUE XDP_BPM_L<0> 10 13 69
8898 TRUE TP_XDP_OBSFN_B0 13
8899 TRUE TP_XDP_OBSFN_B1 13
8900 TRUE TP_XDP_OBSDATA_B0 13
8901 TRUE TP_XDP_OBSDATA_B1 13
8902 TRUE TP_XDP_OBSDATA_B2 13
8903 TRUE TP_XDP_OBSDATA_B3 13
8904 TRUE XDP_PWRGD 13
8905 TRUE XDP_OBS20 13
8906 TRUE PM_LATRIGGER_L 13 19
8907 TRUE JTAG_MCP_TCK 6 13 21
8908 TRUE SMBUS_MCP_0_DATA 13 21 44 72
8909 TRUE SMBUS_MCP_0_CLK 13 21 44 72
8910 TRUE XDP_TCK 6 10 13 69
8911 TRUE PPCPUVTT_S0 7 8
8912 TRUE PP3V3_S0 7 8
8913 TRUE JTAG_MCP_TDO_CONN 6 13
8914 TRUE JTAG_MCP_TRST_L 6 13 21
8915 TRUE MCP_DEBUG<0> 13 19 72
8916 TRUE MCP_DEBUG<1> 13 19 72
8917 TRUE MCP_DEBUG<2> 13 19 72
8918 TRUE MCP_DEBUG<3> 13 19 72
8919 TRUE JTAG_MCP_TDI 6 13 21
8920 TRUE JTAG_MCP_TMS 6 13 21
8921 TRUE MCP_DEBUG<4> 13 19 72
8922 TRUE MCP_DEBUG<5> 13 19 72
8923 TRUE MCP_DEBUG<6> 13 19 72
8924 TRUE MCP_DEBUG<7> 13 19 72
8925 TRUE FSB_CLK_ITP_P 13 14 69
8926 TRUE FSB_CLK_ITP_N 13 14 69
8927 TRUE XDP_CPURST_L 13 69
8928 TRUE XDP_DBRESET_L 10 13 26
8929 TRUE XDP_TDO_CONN 6 13
8930 TRUE XDP_TRST_L 6 10 13 69
8931 TRUE XDP_TDI 6 10 13 69
8932 TRUE XDP_TMS 6 10 13 69
8933 TRUE GND Need 8 TP
    
```

J5100 LPC+SPI Connector

```

8934 TRUE PP3V42_G3H 7 8
8935 TRUE PP5VRT_S0 7 8
8936 TRUE LPC_AD<0> 19 41 43 72
8937 TRUE LPC_AD<1> 19 41 43 72
8938 TRUE SPI_ALT_MOSI 43
8939 TRUE SPI_ALT_MISO 43
8940 TRUE LPC_FRAME_L 19 41 43 72
8941 TRUE PM_CLKRUN_L 19 41 43
8942 TRUE SMC_TMS 41 42 43
8943 TRUE DEBUG_RESET_L 26 43
8944 TRUE SMC_TDO 41 42 43
8945 TRUE SMC_TRST_L 41 43
8946 TRUE SMC_MDI 41 43
8947 TRUE SMC_TX_L 19 41 42 43
8948 TRUE LPC_CLK33M_LPCPLUS 26 43 72
8949 TRUE LPC_AD<2> 19 41 43 72
8950 TRUE LPC_AD<3> 19 41 43 72
8951 TRUE SPIROM_USE_MLB 43
8952 TRUE SPI_ALT_CLK 43
8953 TRUE SPI_ALT_CS_L 43
8954 TRUE LPC_SERIRQ 19 41 43
8955 TRUE LPC_PWRDWN_L 19 41 43
8956 TRUE SMC_TDI 41 42 43
8957 TRUE SMC_TCK 41 42 43
8958 TRUE SMC_RESET_L 41 42 43
8959 TRUE SMC_MMI 41 43
8960 TRUE SMC_RX_L 19 41 42 43
8961 TRUE LPCPLUS_GPIO 18 43
8962 TRUE GND Need 2 TP
    
```

SYNC MASTER=K36B_MLB SYNC DATE=08/17/2008

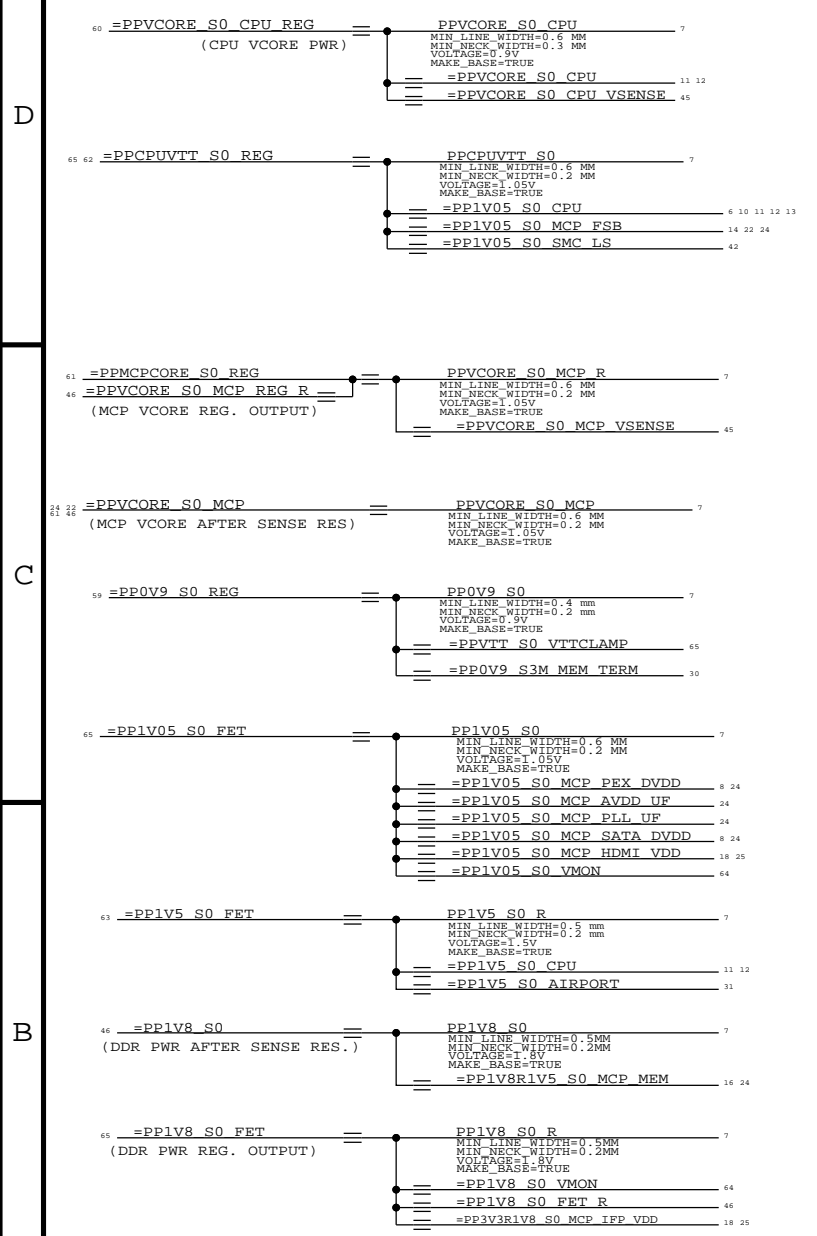
FUNC TEST

Apple Inc. 051-8089 D
 REVISION A.0.0

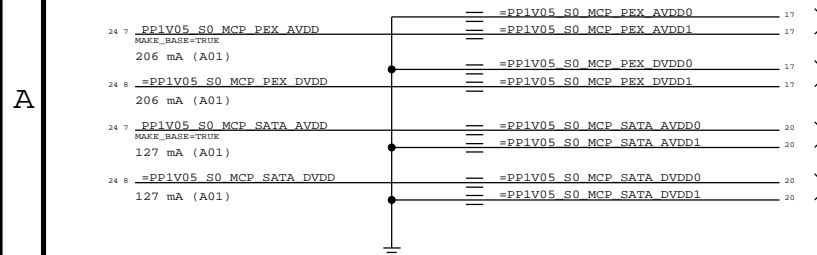
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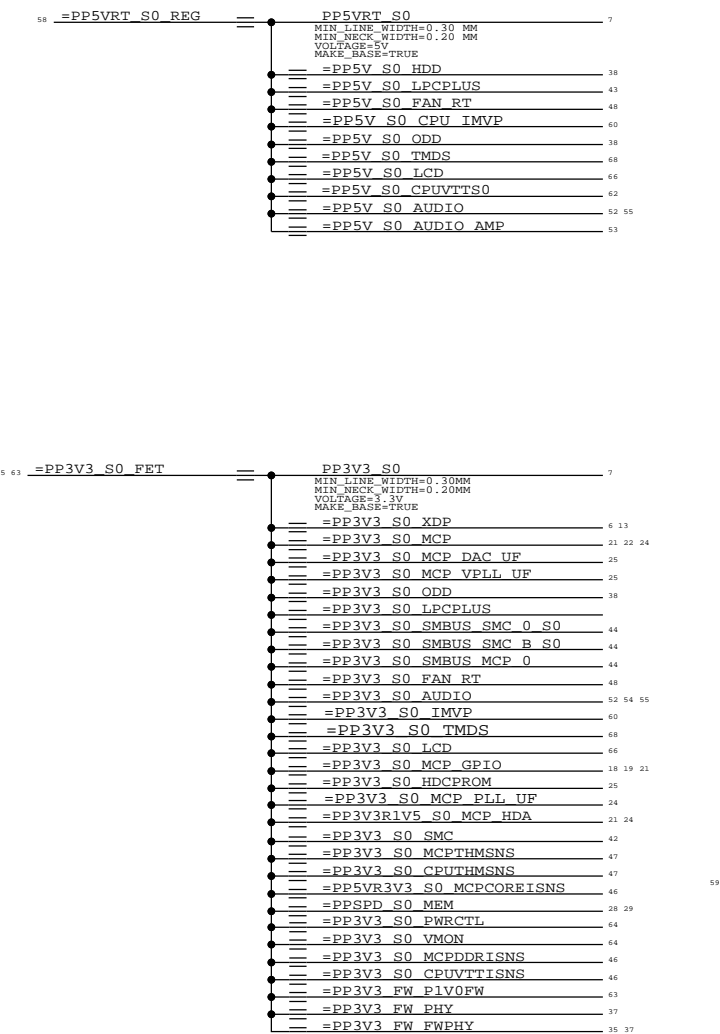
"S0,S0M" RAILS



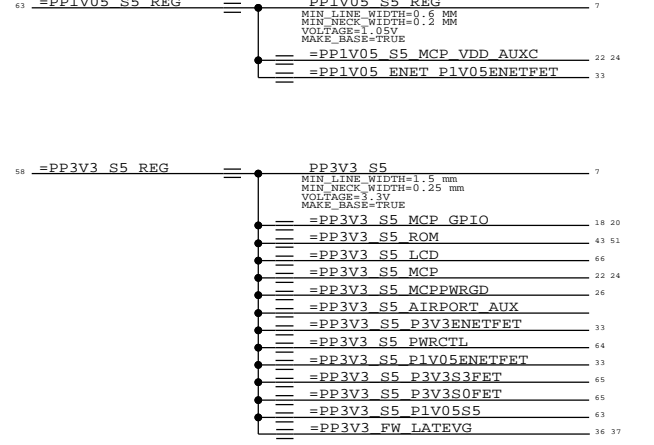
PEX & SATA AVDD/DVDD aliases



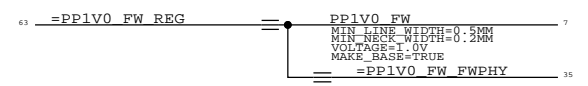
"S3" RAILS



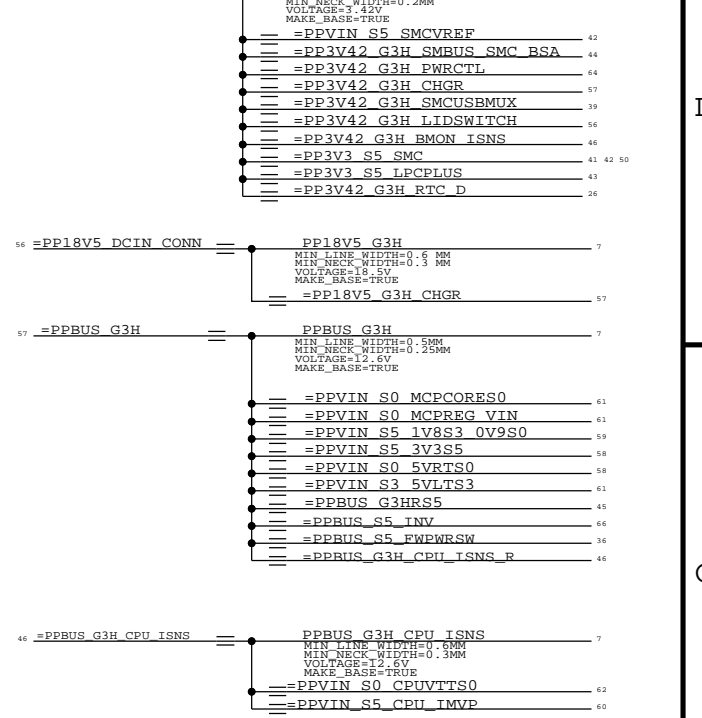
"S5" RAILS



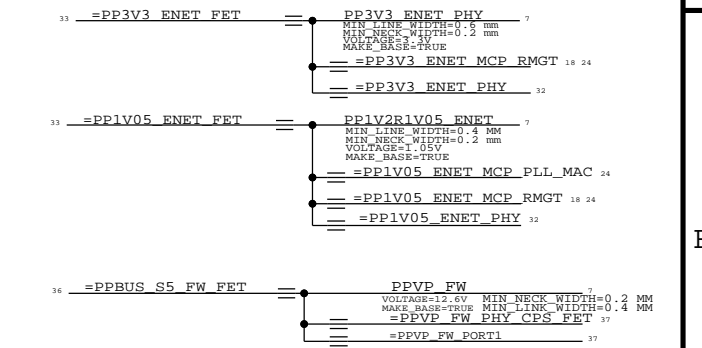
"FW" RAILS



"G3H" RAILS



"ENET" RAILS



SYNC MASTER=K36B MLB

Power Aliases

Apple Inc.

051-8089

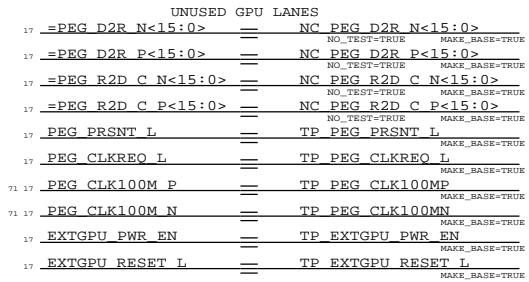
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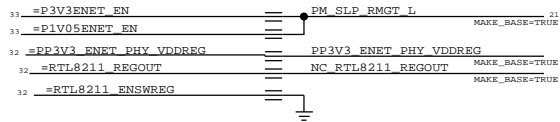
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 REVISION: A.0.0
 SHEET: 8 OF 109
 SHEETS: 109

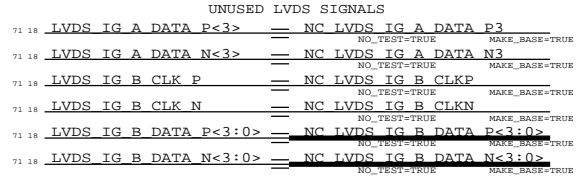
PCI-E ALIASES



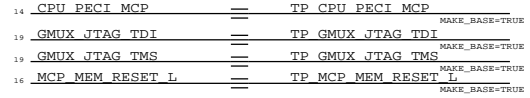
ETHERNET ALIASES



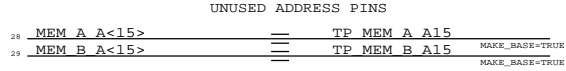
LVDS ALIASES



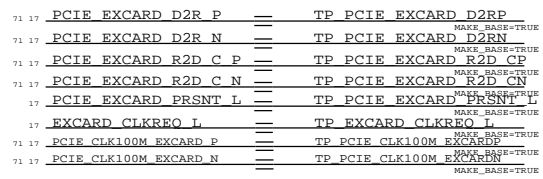
MISC NC MCP79 ALIASES



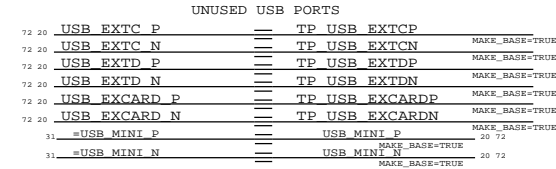
SO-DIMM ALIASES



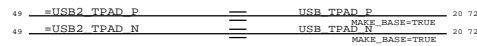
UNUSED EXPRESS CARD LANE



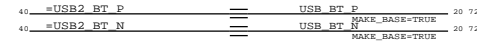
USB ALIASES



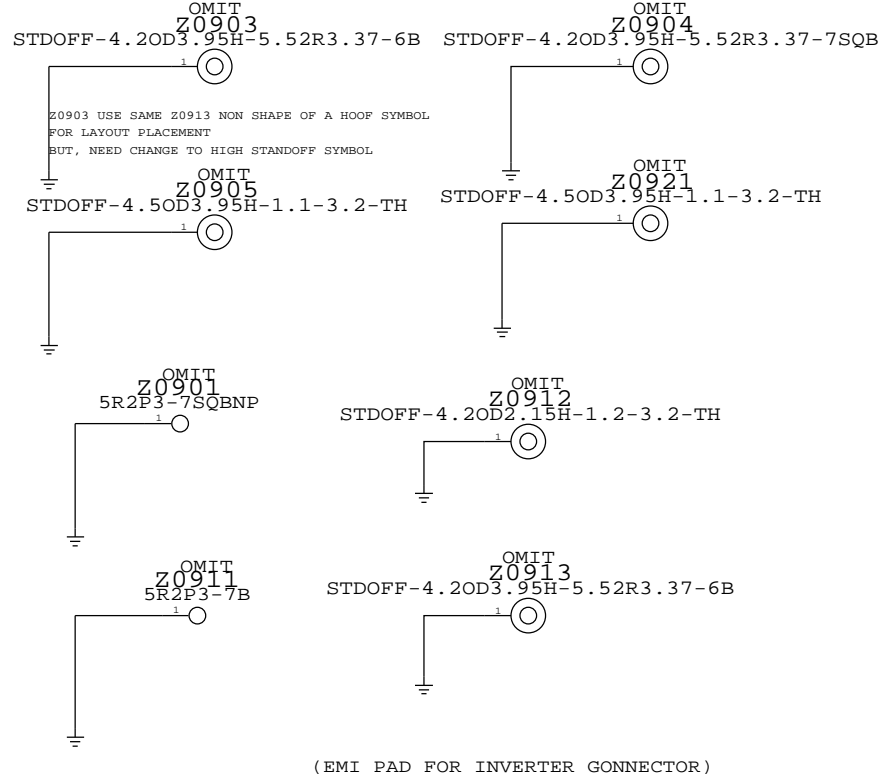
TRACKPAD (WELLSPRING)



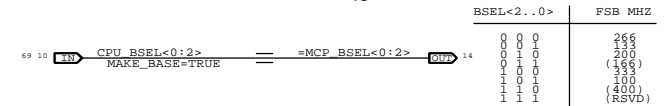
BLUETOOTH



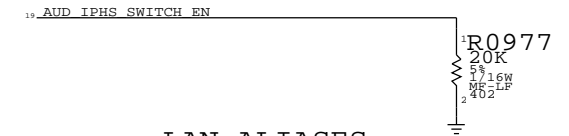
CPU HEATSINK STANDOFF SCREW HOLE



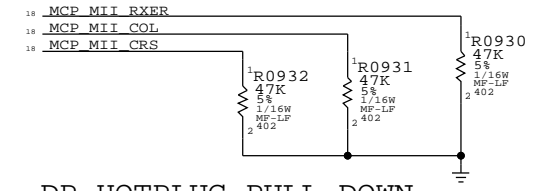
CPU FSB FREQUENCY STRAPS



HDA PULL-DOWN



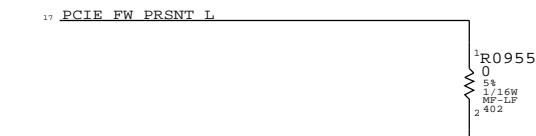
LAN ALIASES



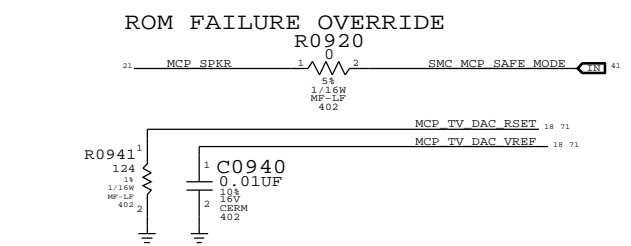
DP HOTPLUG PULL-DOWN



FW PULL-DOWN

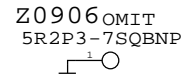


MCP_SAFE_MODE SIGNAL TO SUPPORT

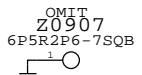


Screw Holes

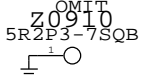
BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND



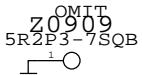
SATA,LVDS CONNECTOR CHASSIS GND



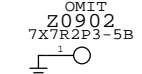
DIP DIMM CONNECTOR CHASSIS GND



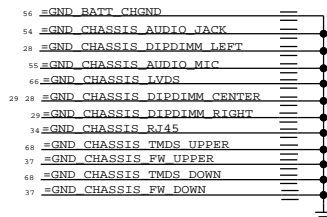
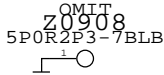
DIP DIMM CONNECTOR CHASSIS GND



DCIN CONNECTOR CHASSIS GND



I/O CONNECTOR CHASSIS GND



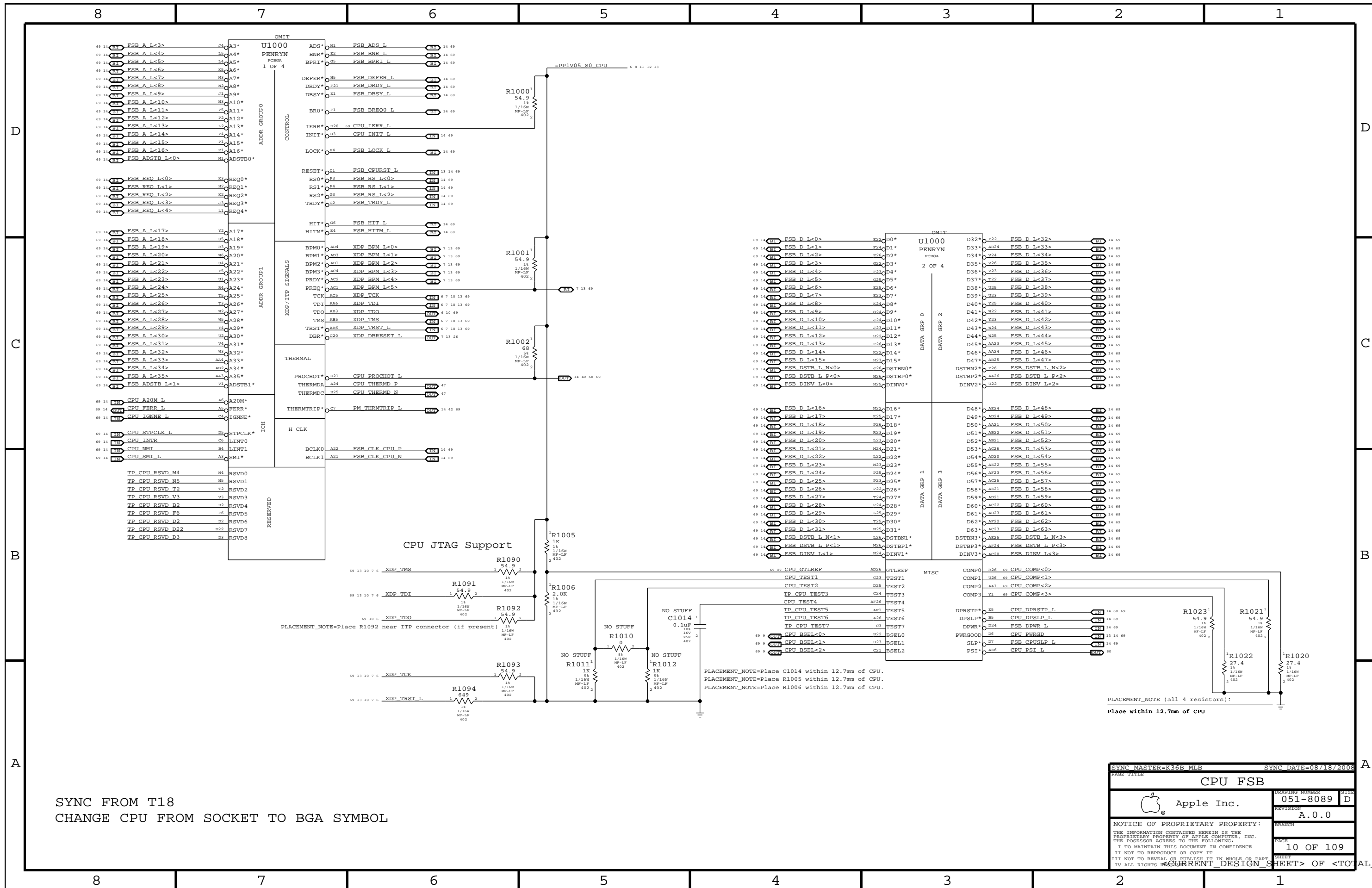
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860-0723	1	STANDOFF WIRELESS	Z0912	?	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0913	?	STANDOFF

SYNC MASTER=K36B MLB

SIGNAL ALIAS

Apple Inc.	051-8089
A.0.0	

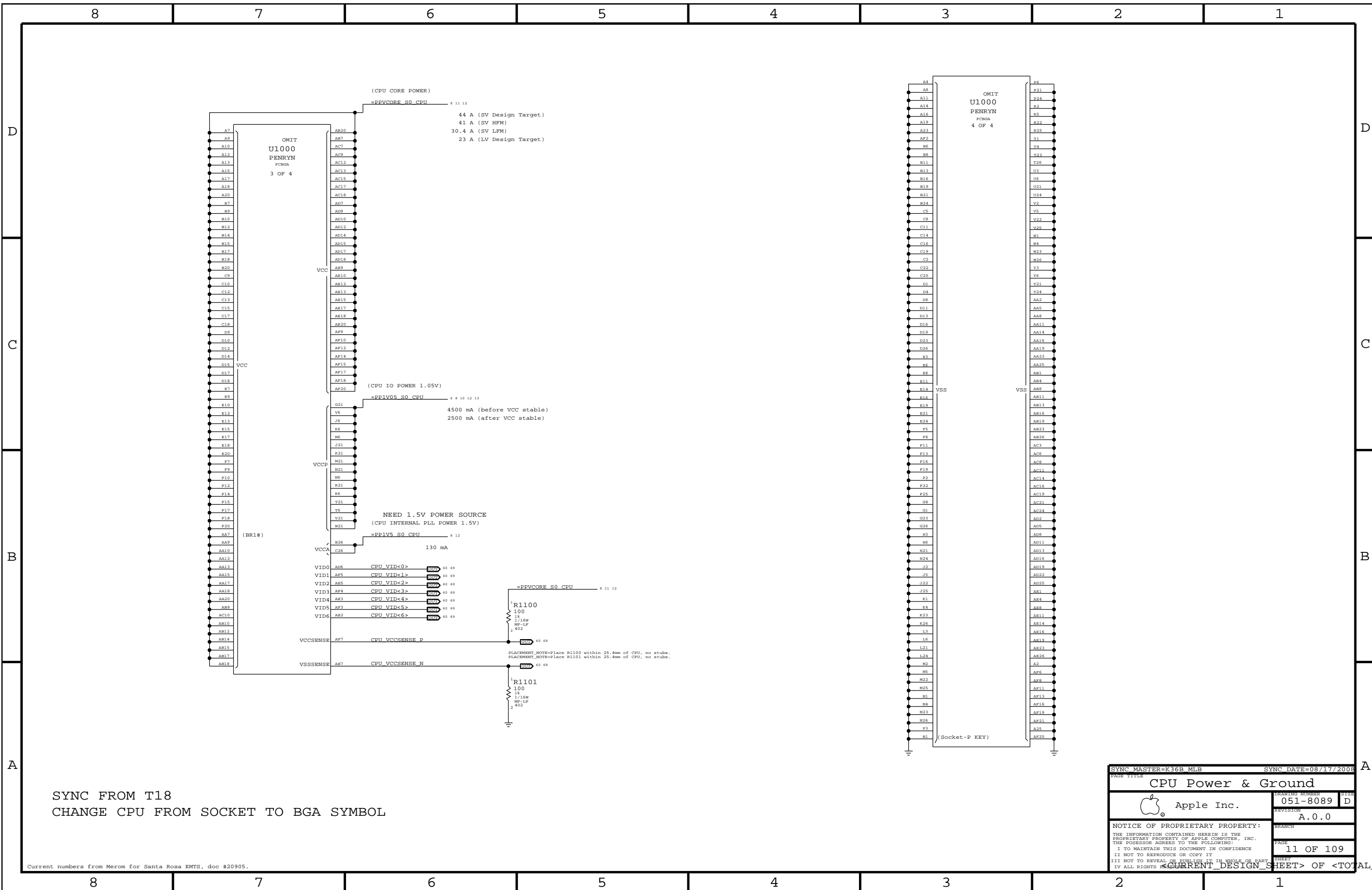
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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K36B MLB SYNC DATE=08/18/2008

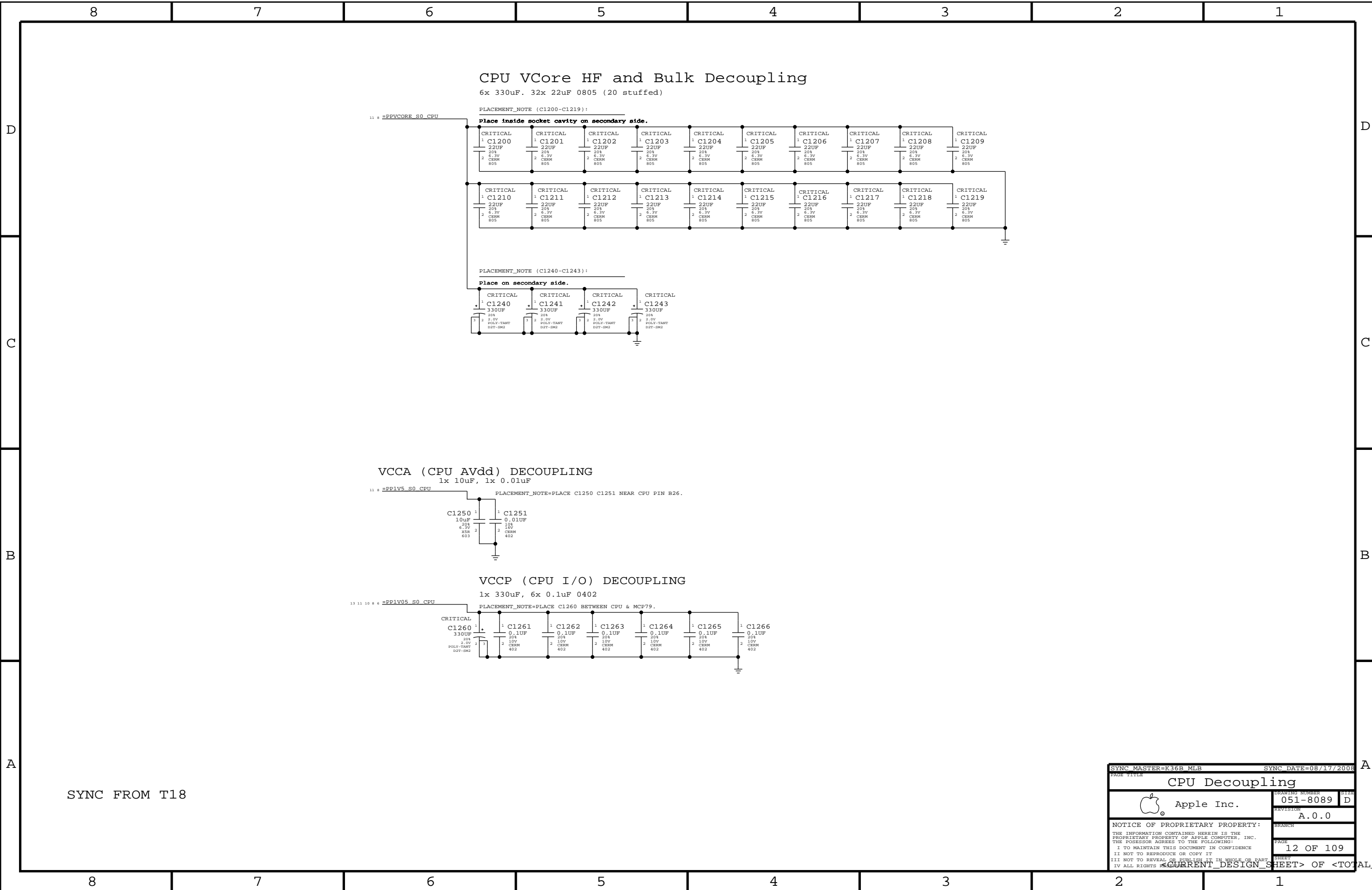
CPU FSB	
Apple Inc.	DRAWING NUMBER 051-8089 D
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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
CPU Power & Ground			
Apple Inc.		051-8089	D
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		SHEET	

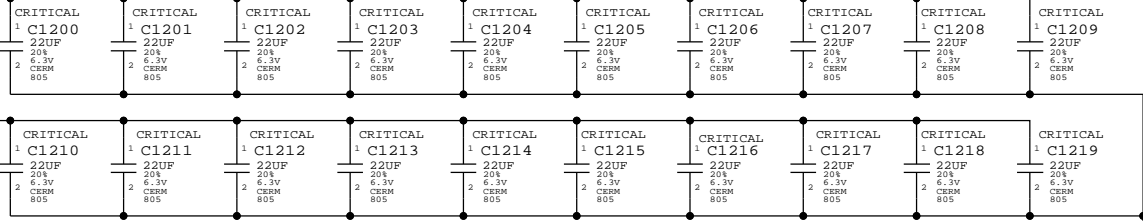


CPU VCore HF and Bulk Decoupling

6x 330uF, 32x 22uF 0805 (20 stuffed)

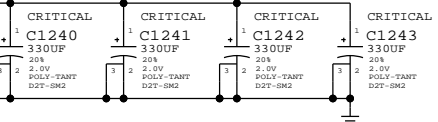
PLACEMENT_NOTE (C1200-C1219):

Place inside socket cavity on secondary side.



PLACEMENT_NOTE (C1240-C1243):

Place on secondary side.

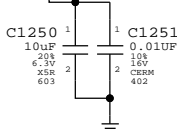


VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

PP1V5_S0_CPU

PLACEMENT_NOTE=PLACE C1250 C1251 NEAR CPU PIN B26.

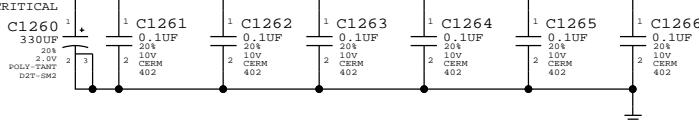


VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

PP1V05_S0_CPU

PLACEMENT_NOTE=PLACE C1260 BETWEEN CPU & MCP79.



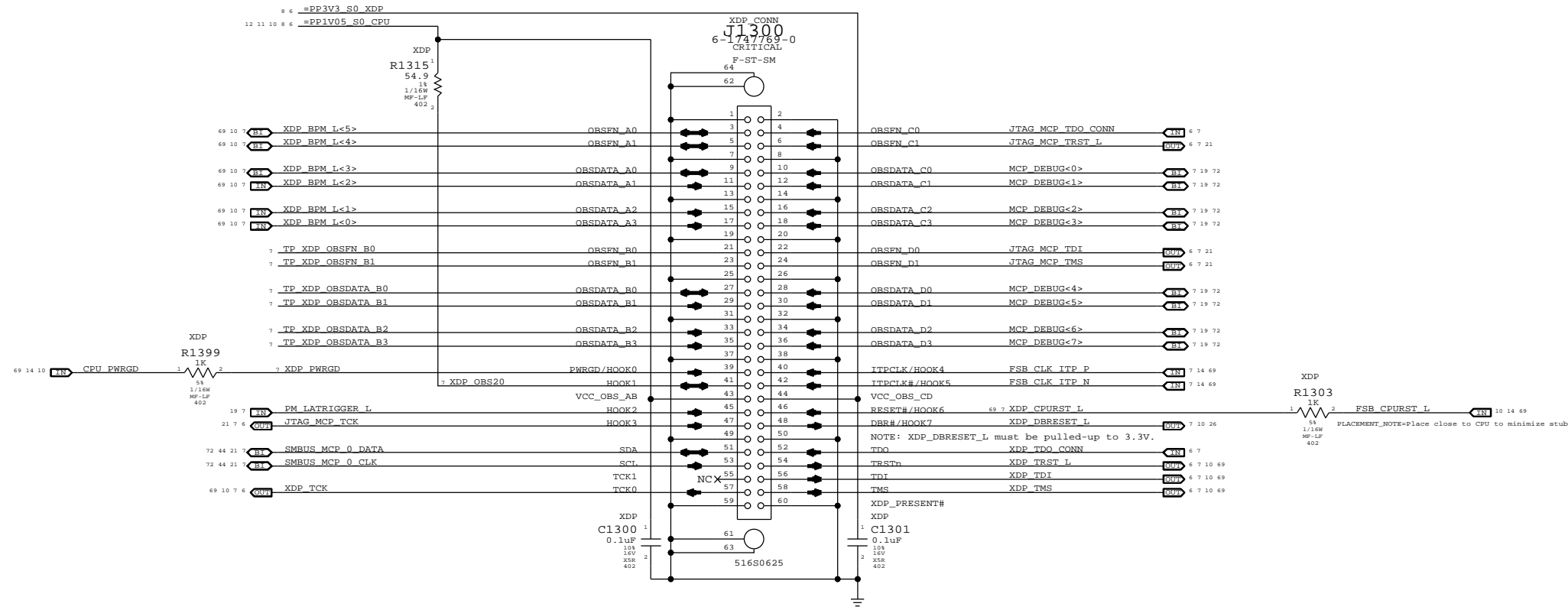
SYNC FROM T18

SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
CPU Decoupling			
Apple Inc.		DRAWING NUMBER 051-8089	SHEET D
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Mini-XDP Connector

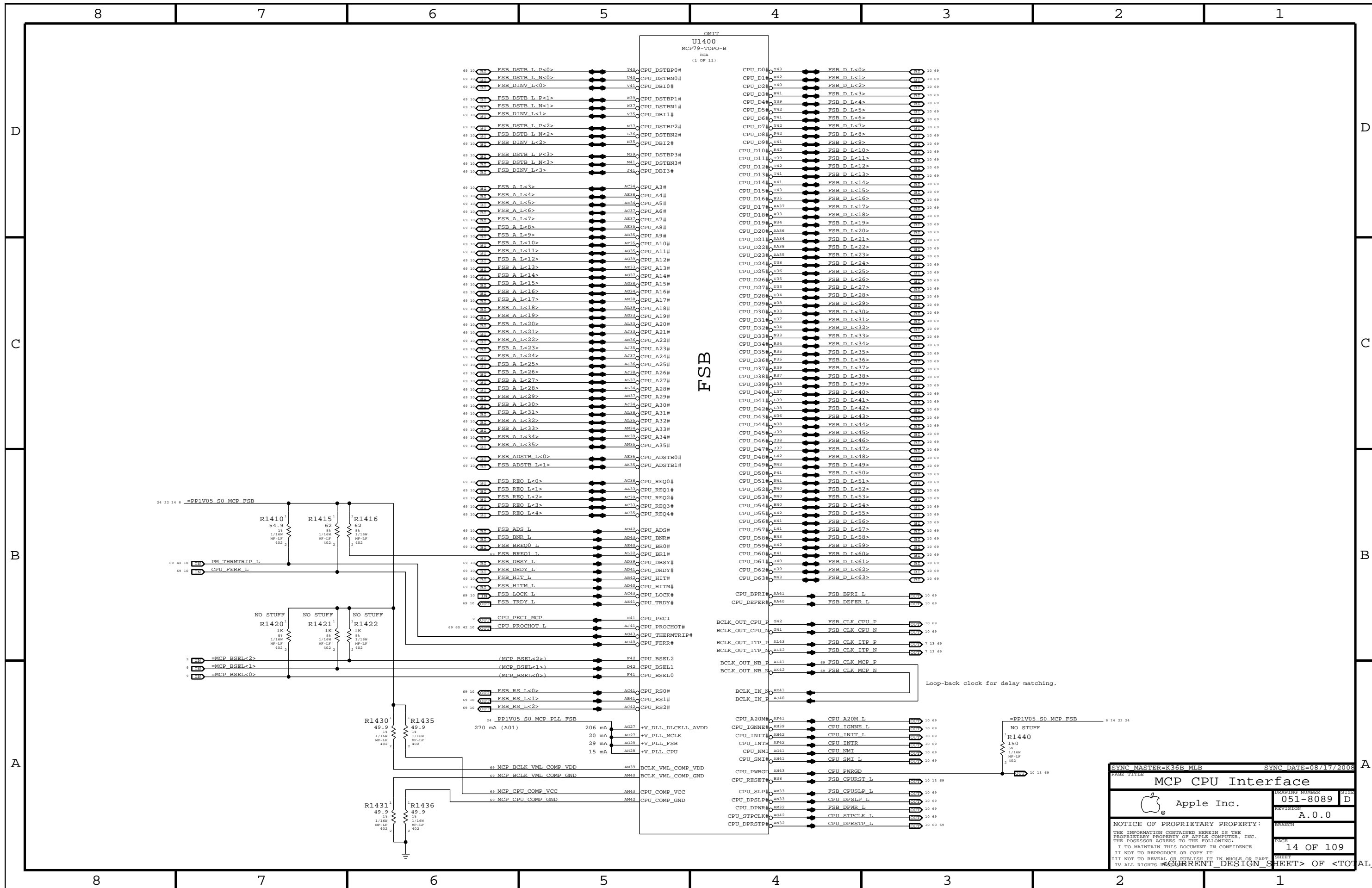
NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



← Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

SYNC MASTER=M99 MLB		SYNC DATE=01/08/2008	
eXtended Debug Port (MiniXDP)			
Apple Inc.		051-8089	D
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SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

MCP CPU Interface

Apple Inc.

051-8089 D

REVISION A.0.0

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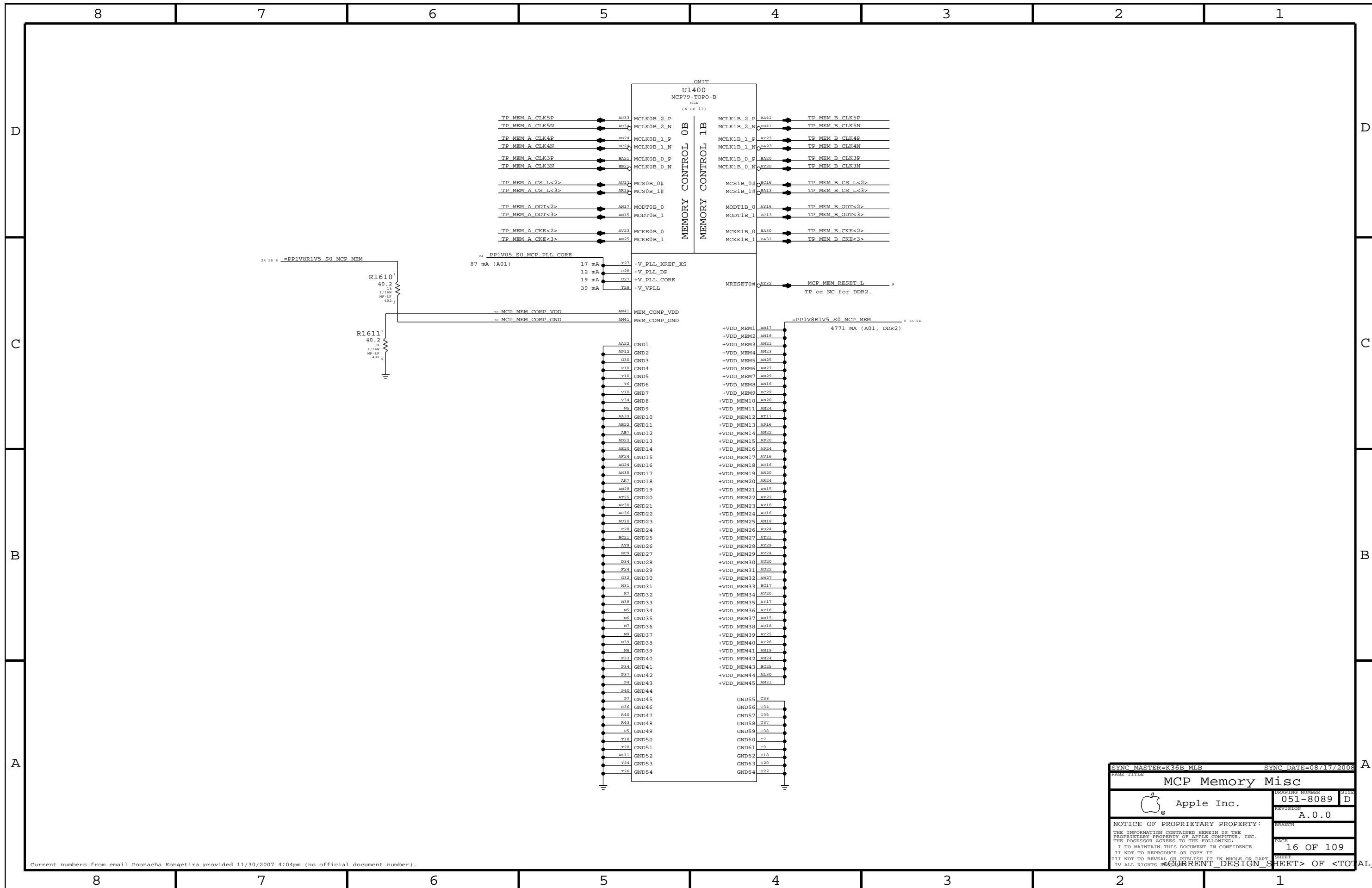


SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

MCP Memory Interface

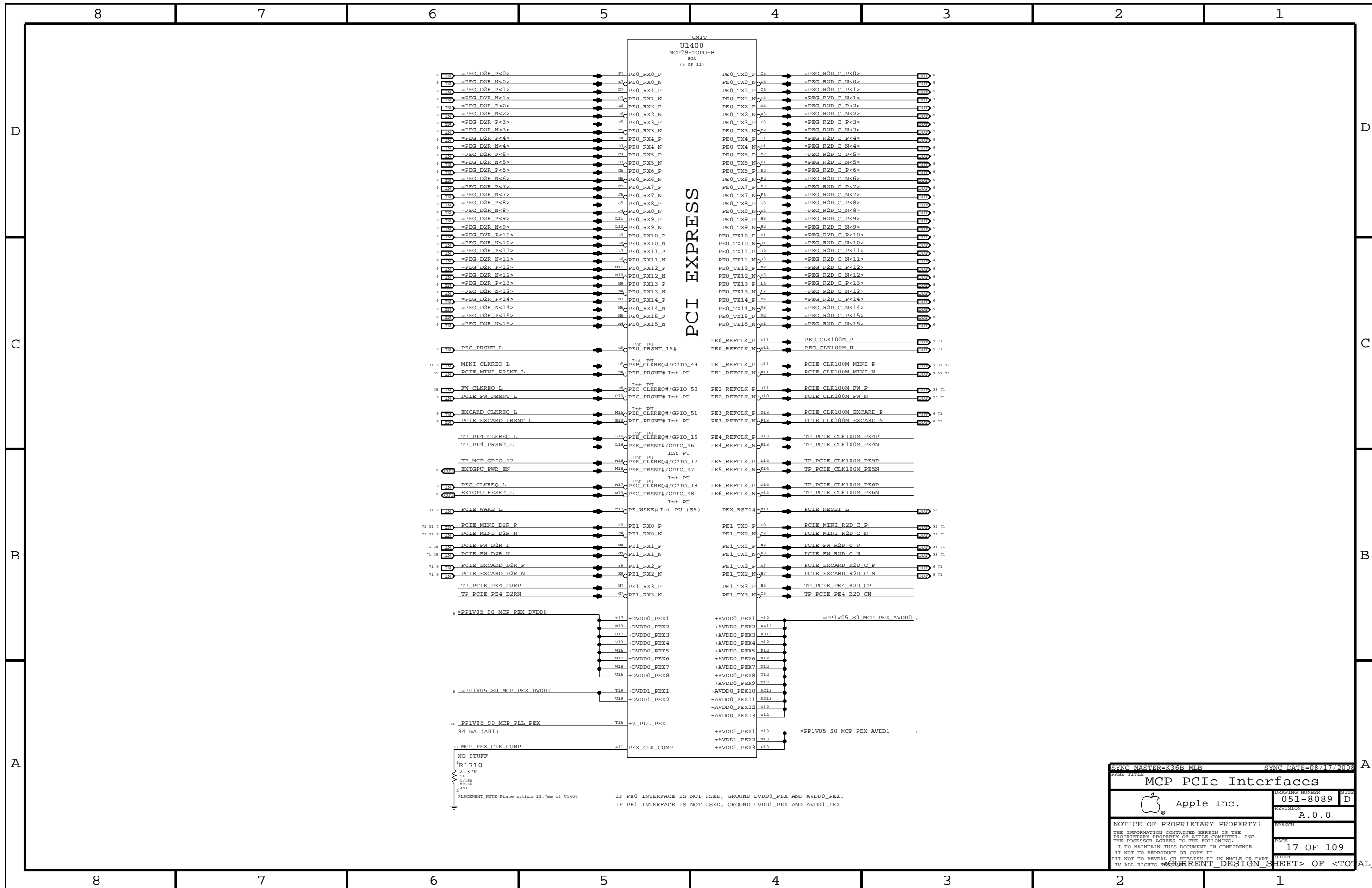
Apple Inc.
 DRAWING NUMBER: 051-8089 D
 REVISION: A.0.0

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 SHEET: 15 OF 109

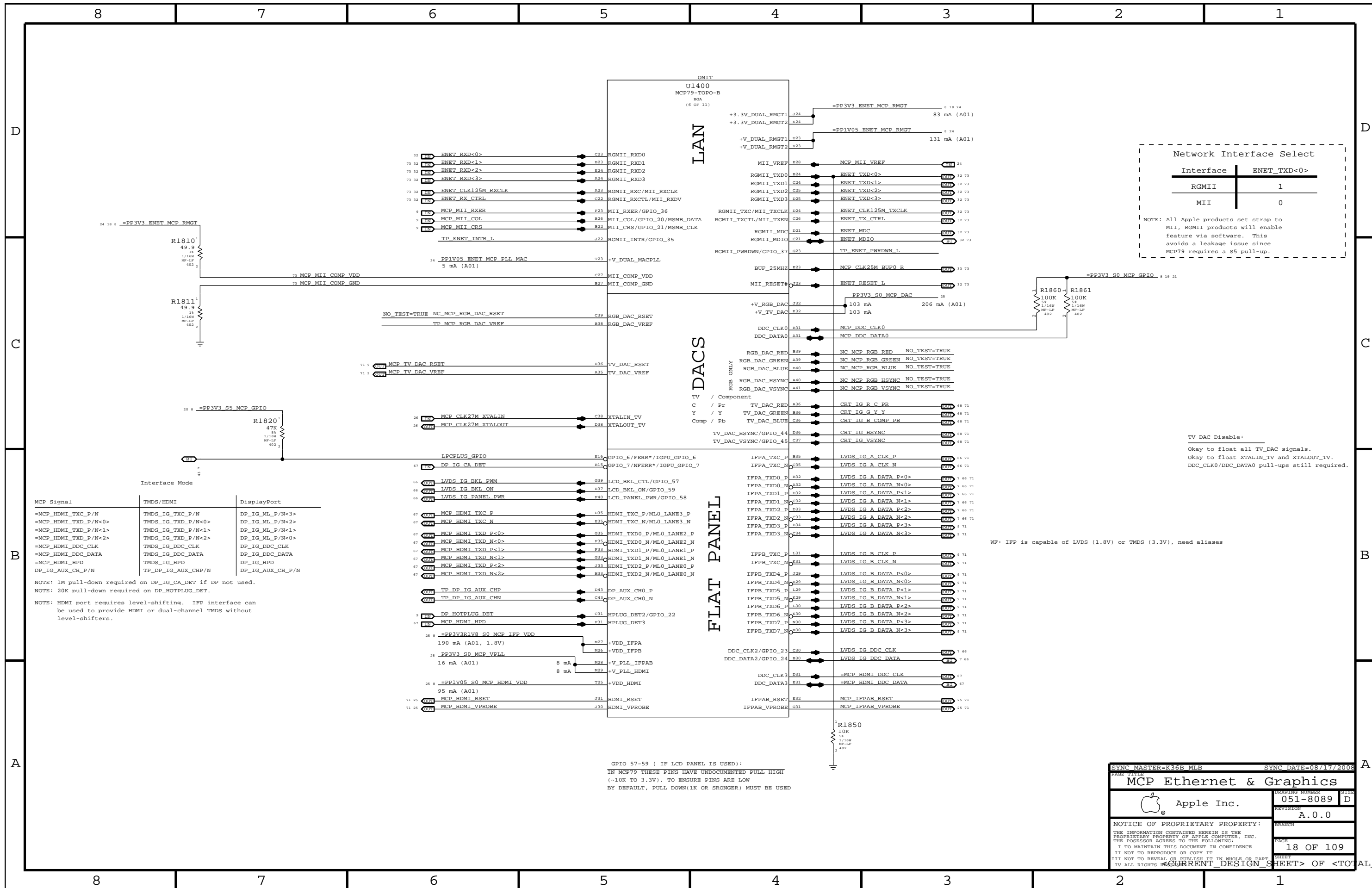


Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE			
MCP Memory Misc			
Apple Inc.		DRAWING NUMBER 051-8089	SHEET D
		REVISION A.0.0	
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IV ALL RIGHTS RESERVED © <CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>			



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE			
MCP PCIe Interfaces			
Apple Inc.		DRAWING NUMBER	051-8089 D
		REVISION	A.0.0
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		SHEET	
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SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

MCP Ethernet & Graphics

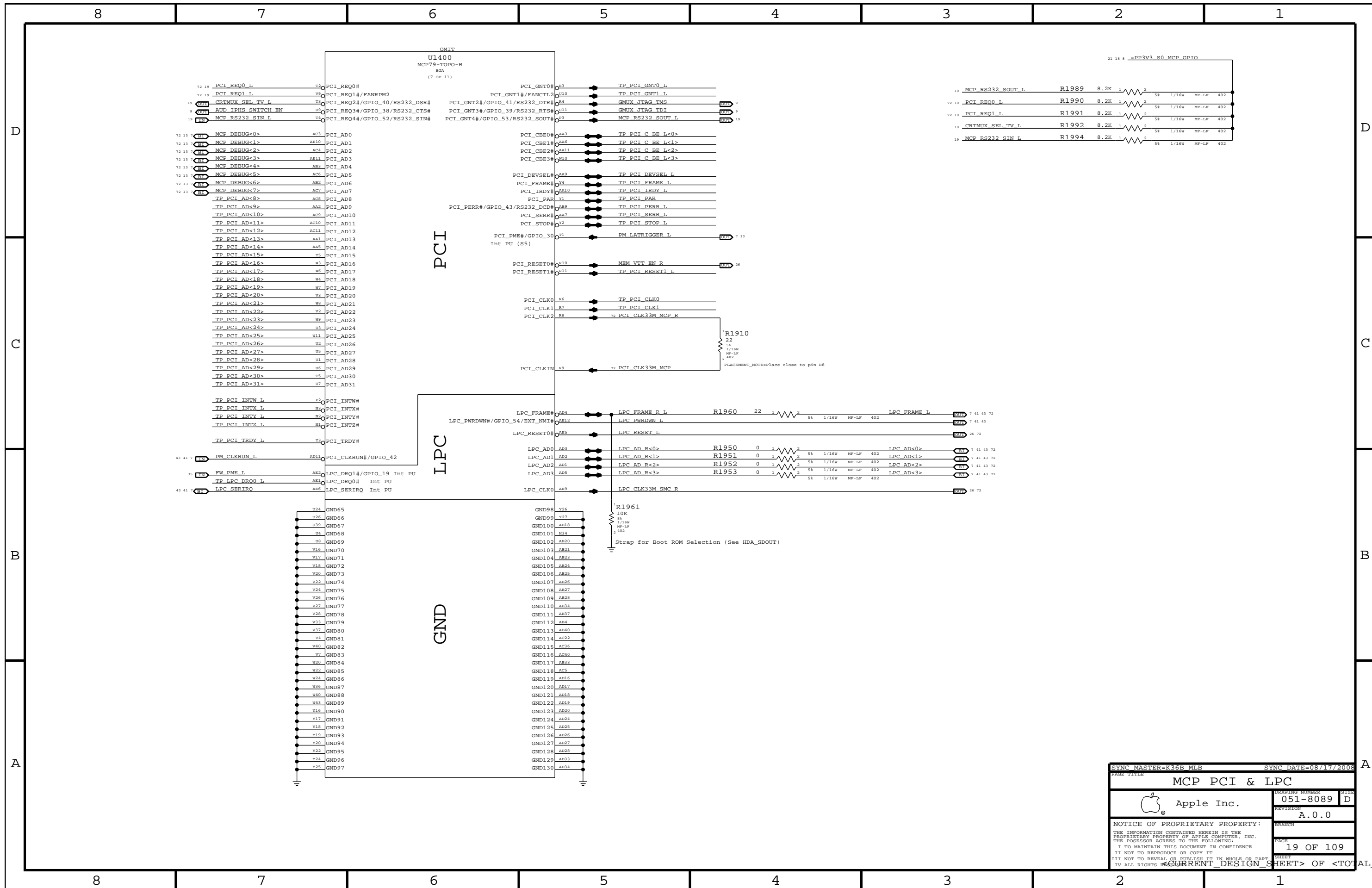
Apple Inc.

CREATION NUMBER: 051-8089 D
 REVISION: A.0.0

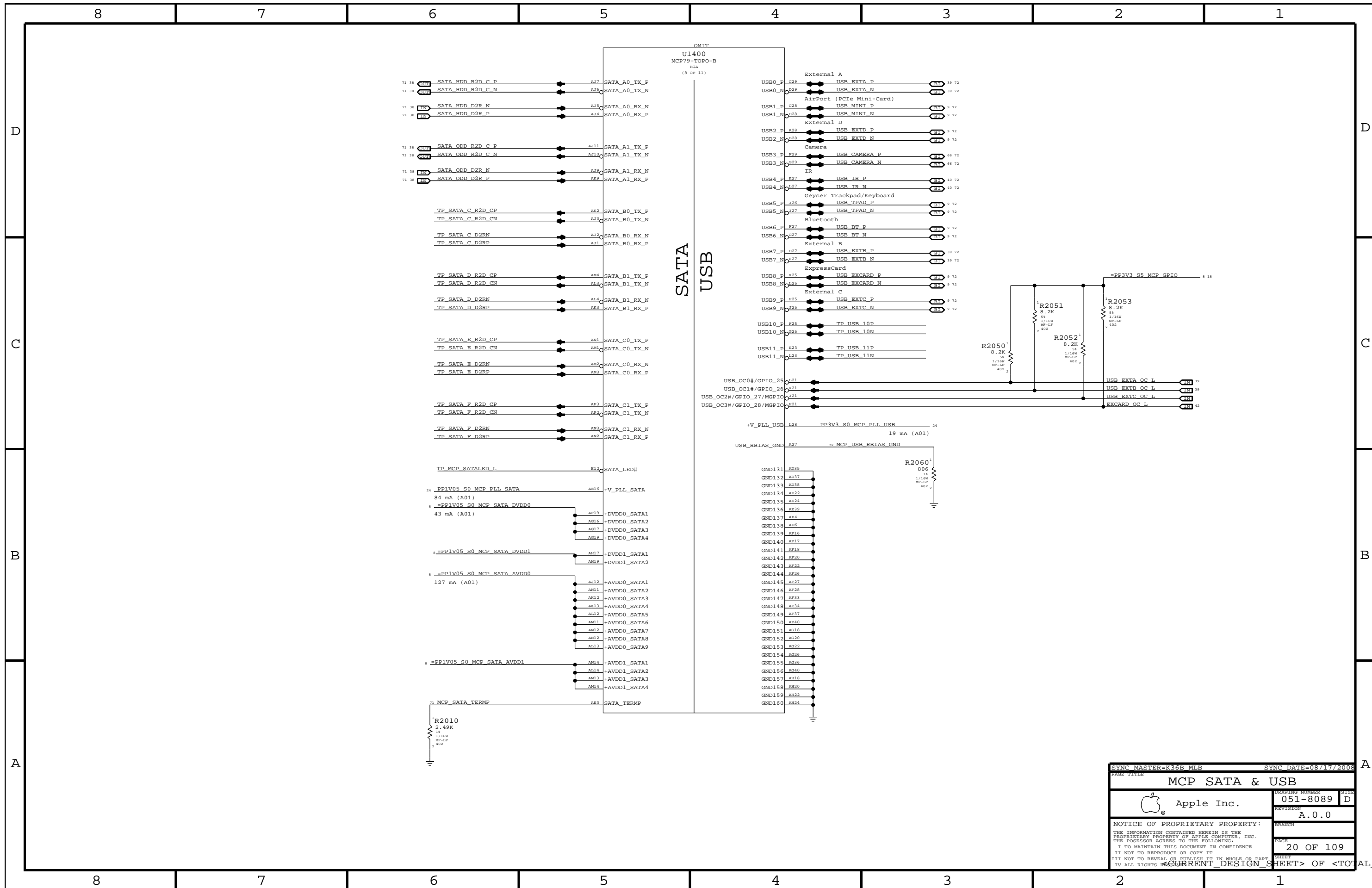
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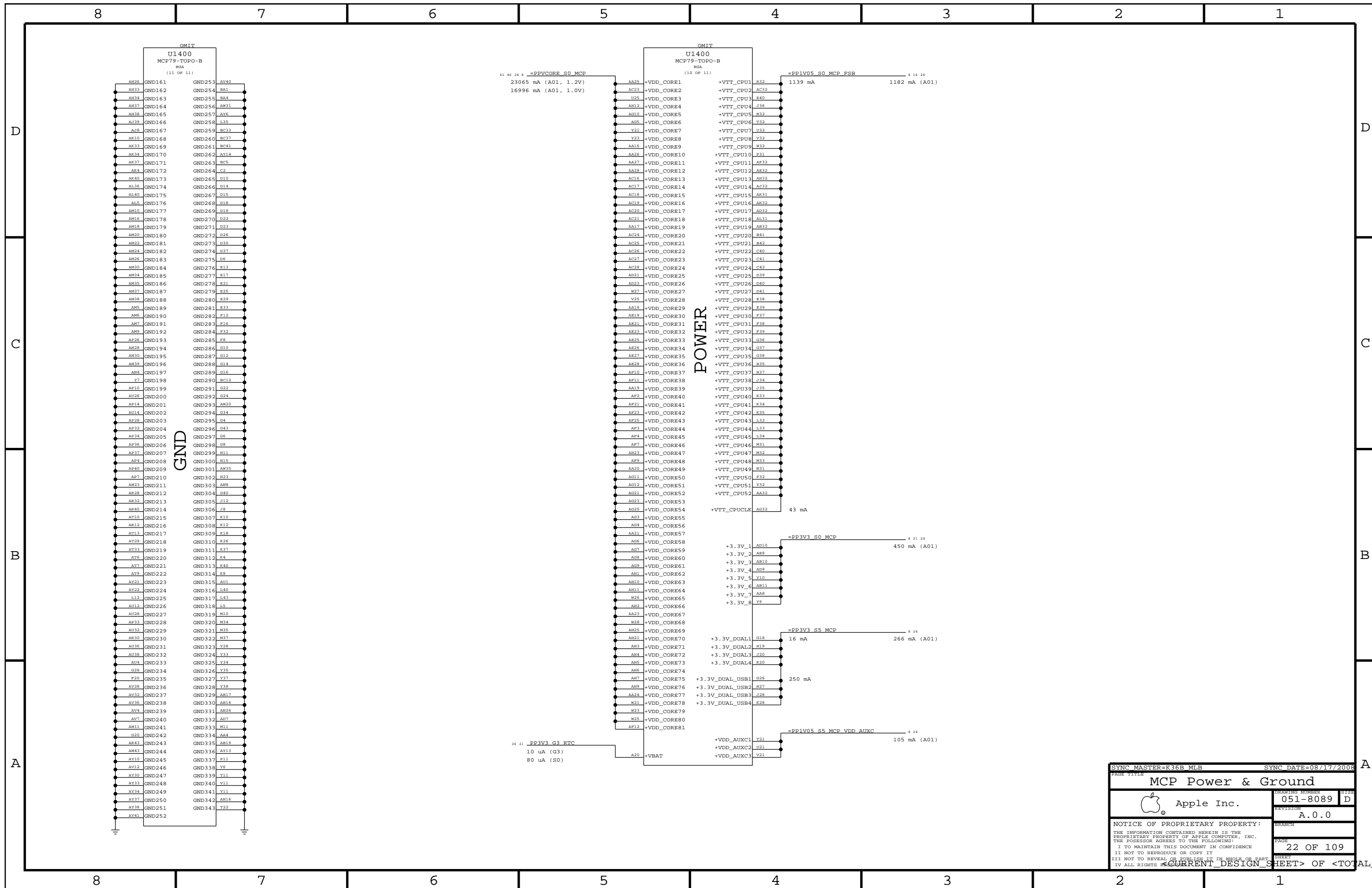
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SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE			
MCP PCI & LPC			
Apple Inc.		DRAWING NUMBER	051-8089 D
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SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE MCP SATA & USB			
DRAWING NUMBER 051-8089		REV D	
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SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE			
MCP Power & Ground			
Apple Inc.		CREATION NUMBER	051-8089 D
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SHEET		OF <TOTAL DESIGN SHEETS>	

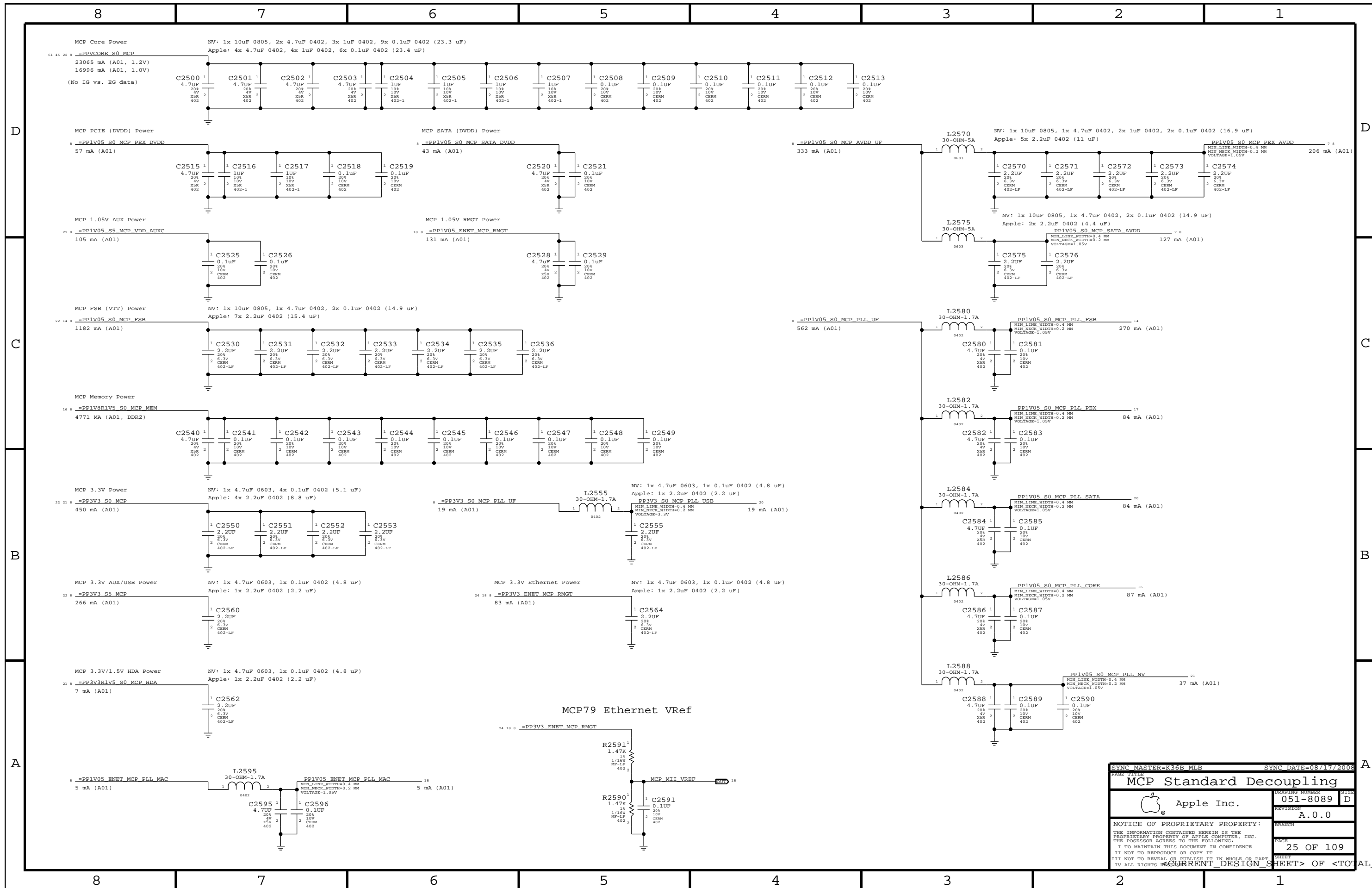
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D									D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE MCP79 A01 Silicon Support			
DRAWING NUMBER 051-8089		REVISION A.0.0	
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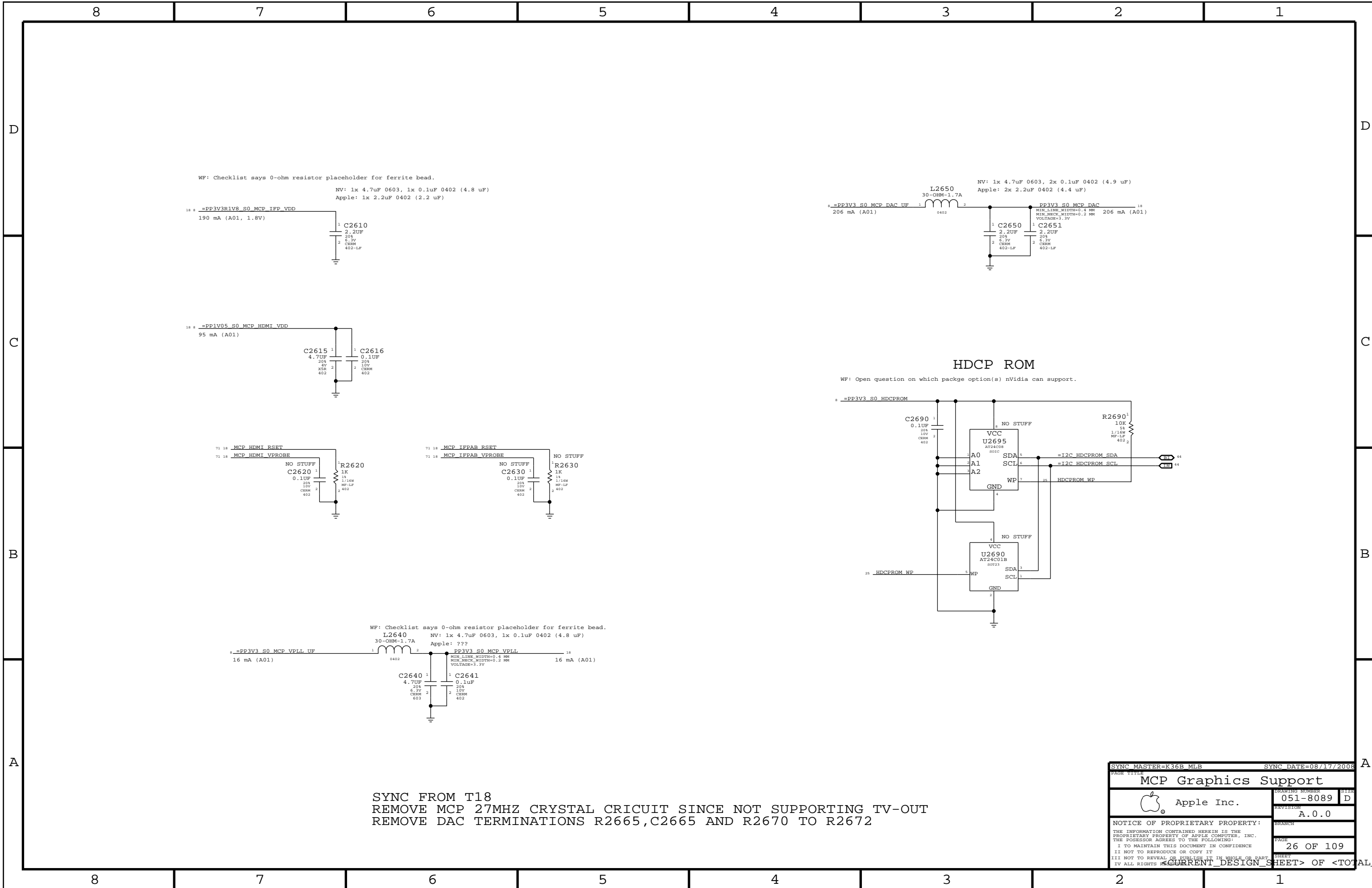


Apple Inc.

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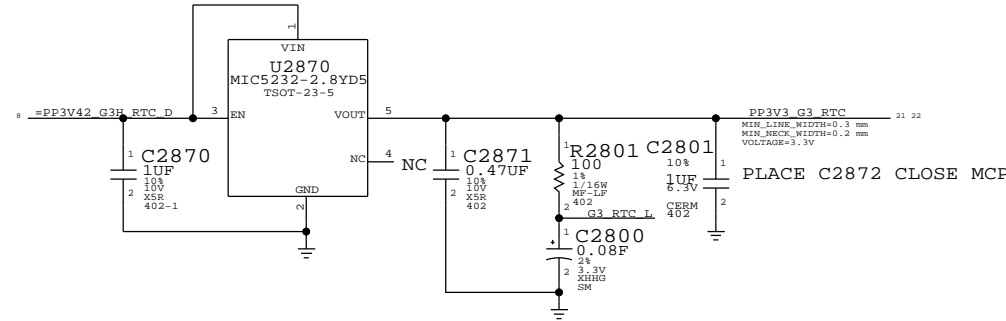
SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
MCP Standard Decoupling			
Apple Inc.		CREATION NUMBER	051-8089
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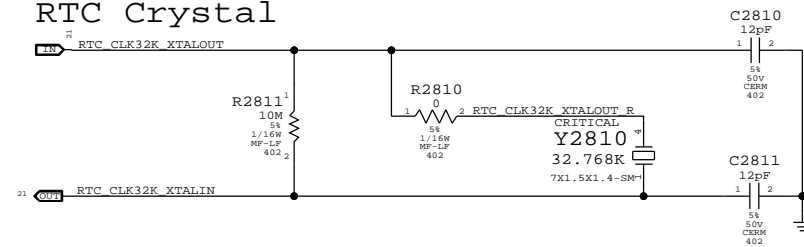
SYNC FROM T18
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672

SYNC MASTER=K36B_MLB		SYNC DATE=08/17/2008	
MCP Graphics Support			
Apple Inc.		DESIGN NUMBER	051-8089
		REVISION	A.0.0
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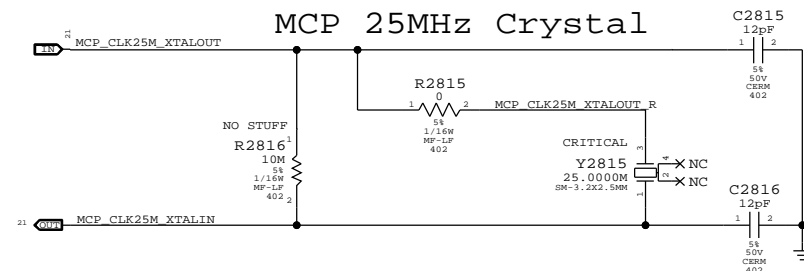
RTC Power Sources



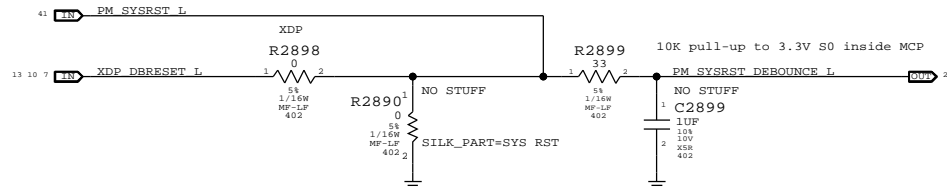
RTC Crystal



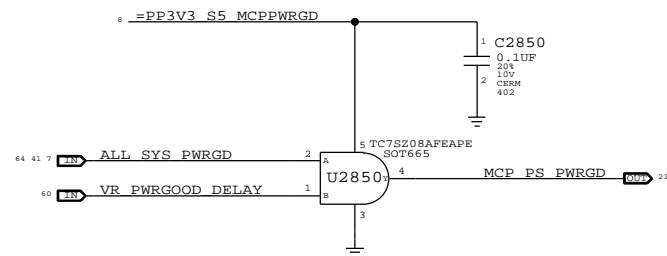
MCP 25MHz Crystal



Reset Button

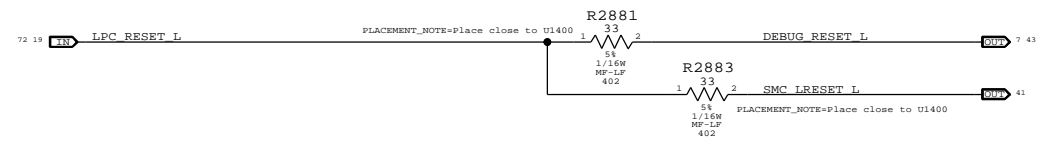


MCP S0 PWRGD

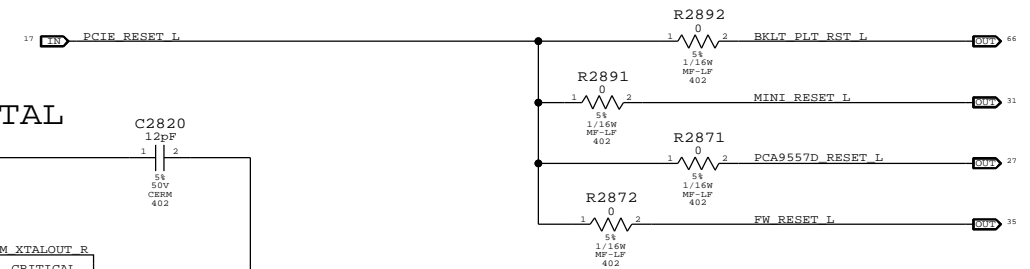


Platform Reset Connections

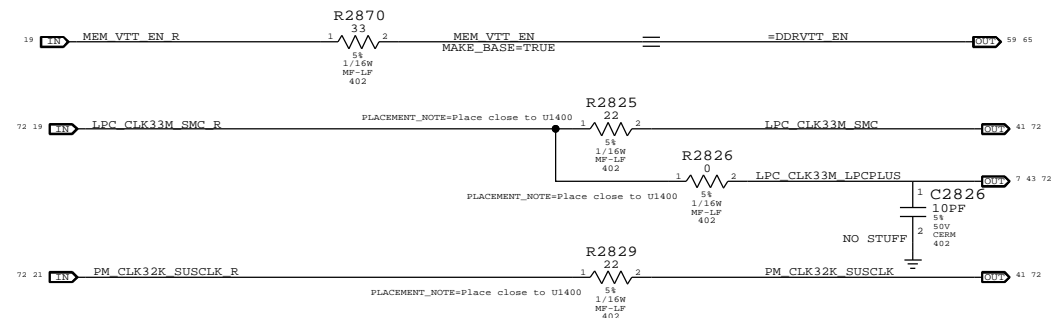
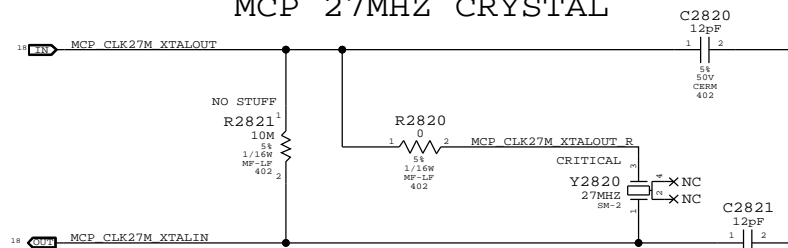
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



MCP 27MHz Crystal



SYNC FROM T18
 CHANGE RESET BUTTON TO RESET PADS
 REMOVE UNUSED PCIE RESET SIGNALS
 REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
 CHANGE RTC POWER SOURCE FROM COIN CELL TO SUPER CAPS
 ALIAS MEM_VTT_EN TO =DDRVTT_EN
 CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE SB Misc			
DRAWING NUMBER 051-8089		REV D	
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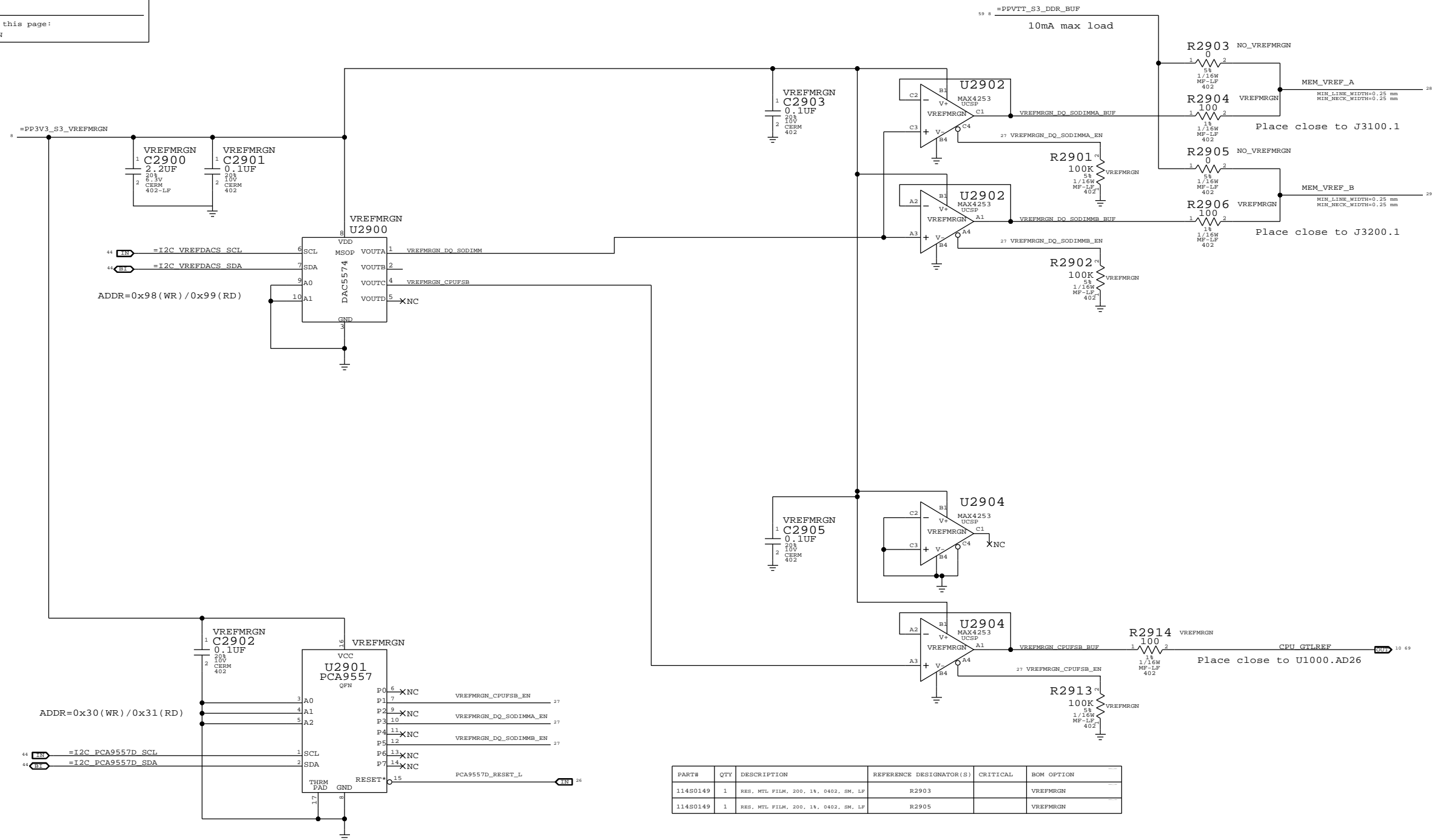
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN AND NO_VREFMRGN

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES. MTL FILM, 200, 1%, 0402, SM, LF	R2903		VREFMRGN
114S0149	1	RES. MTL FILM, 200, 1%, 0402, SM, LF	R2905		VREFMRGN

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

FSB/DDR2 VREF MARGINING

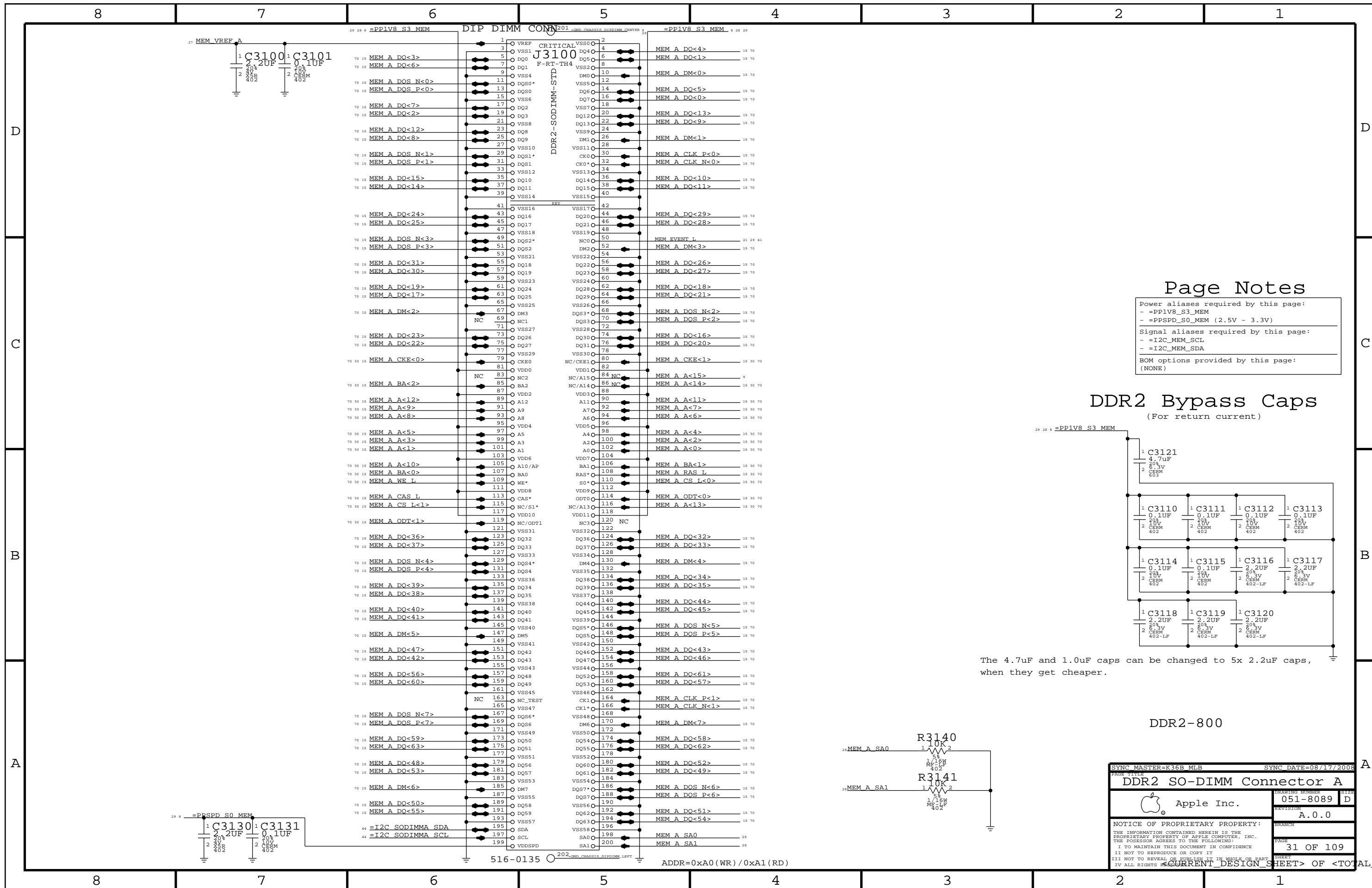
Apple Inc. 051-8089 D

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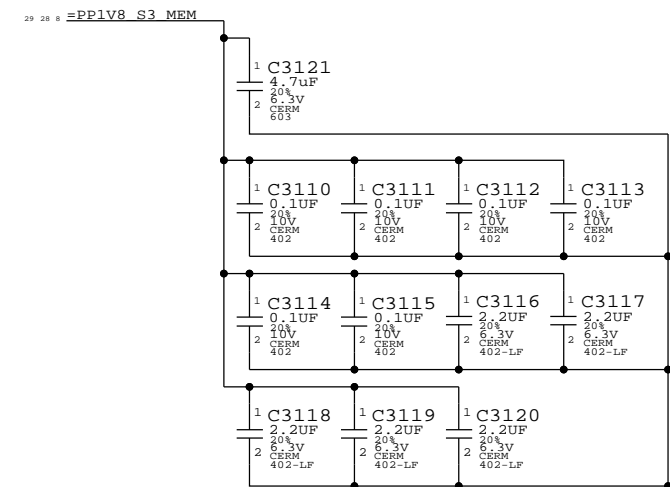
Page Notes

Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

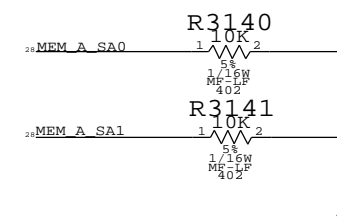
BOM options provided by this page:
 (NONE)

DDR2 Bypass Caps (For return current)

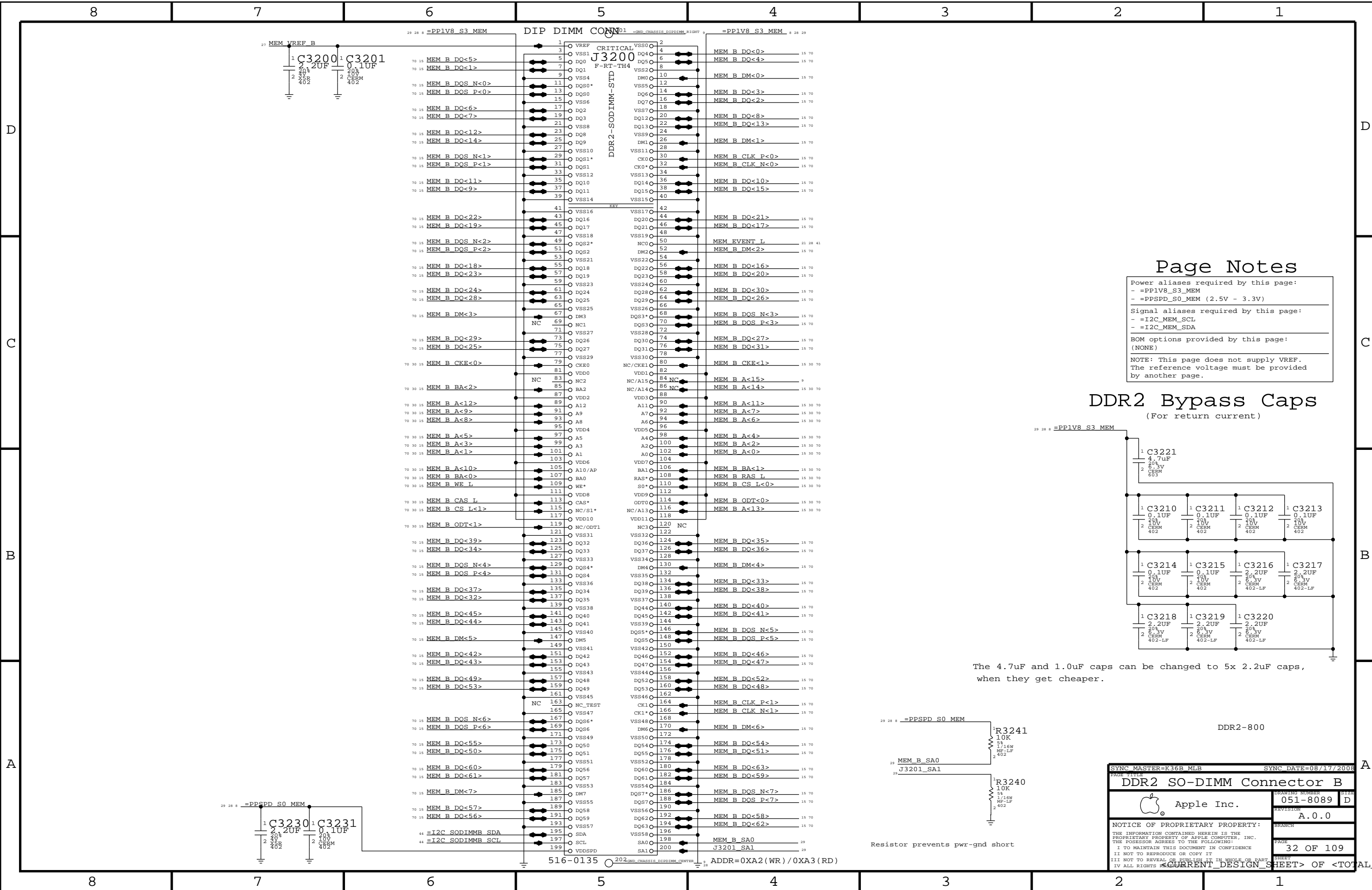


The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

DDR2-800



PAGE TITLE		SYNC DATE=08/17/2008	
DDR2 SO-DIMM Connector A		CREATION NUMBER	1122
Apple Inc.		051-8089	D
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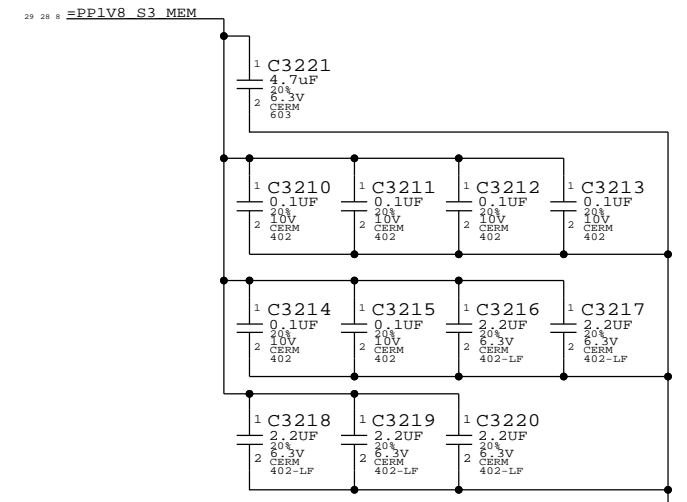
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

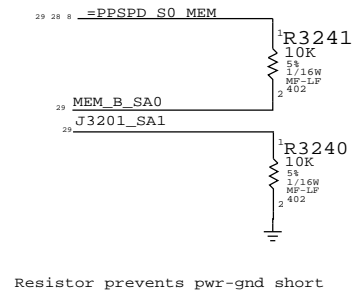
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided
 by another page.

DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



PAGE TITLE		SYNC DATE=08/17/2008	
DDR2 SO-DIMM Connector B		CREATION NUMBER	051-8089
Apple Inc.		REVISION	A.0.0
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8

7

6

5

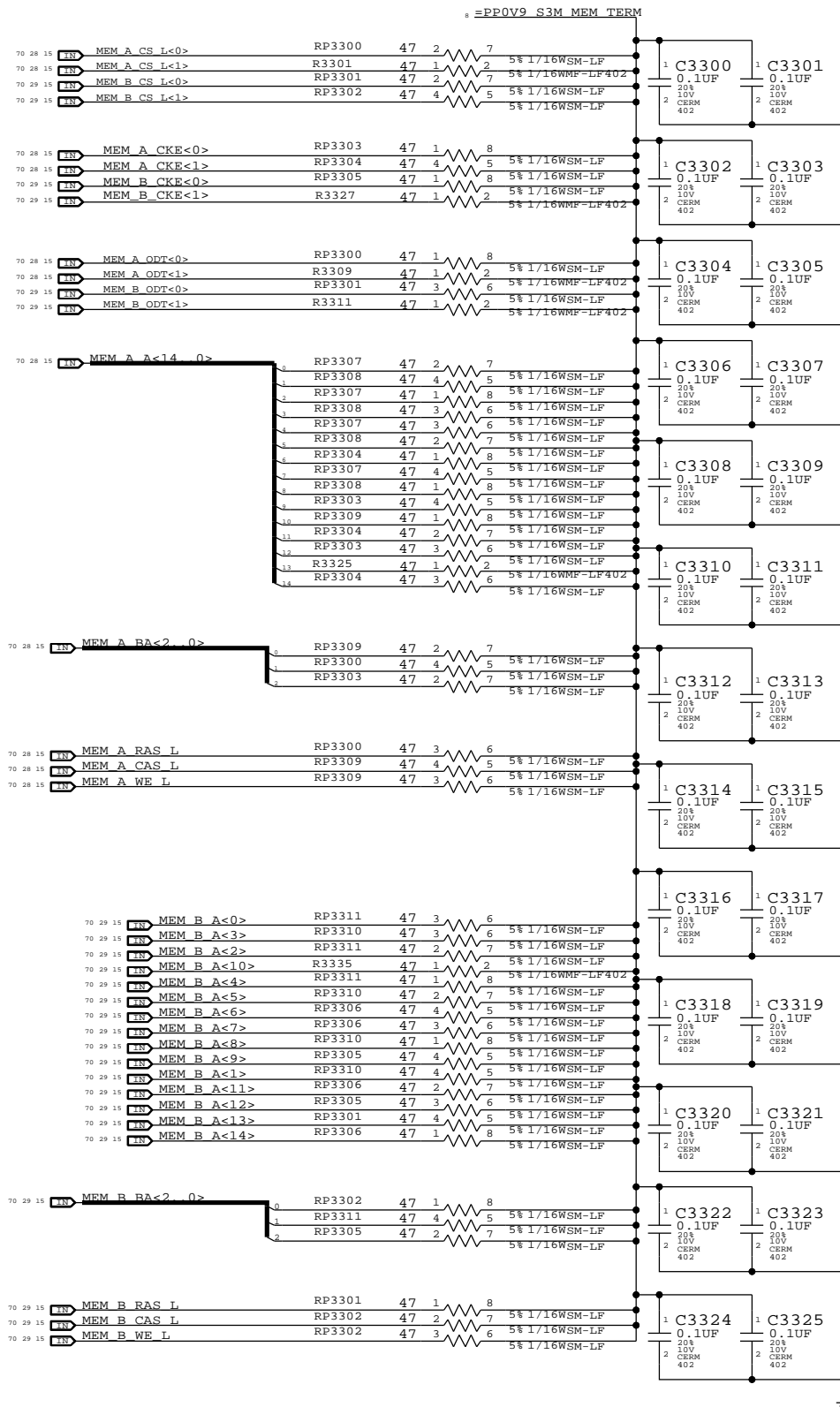
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

Memory Active Termination

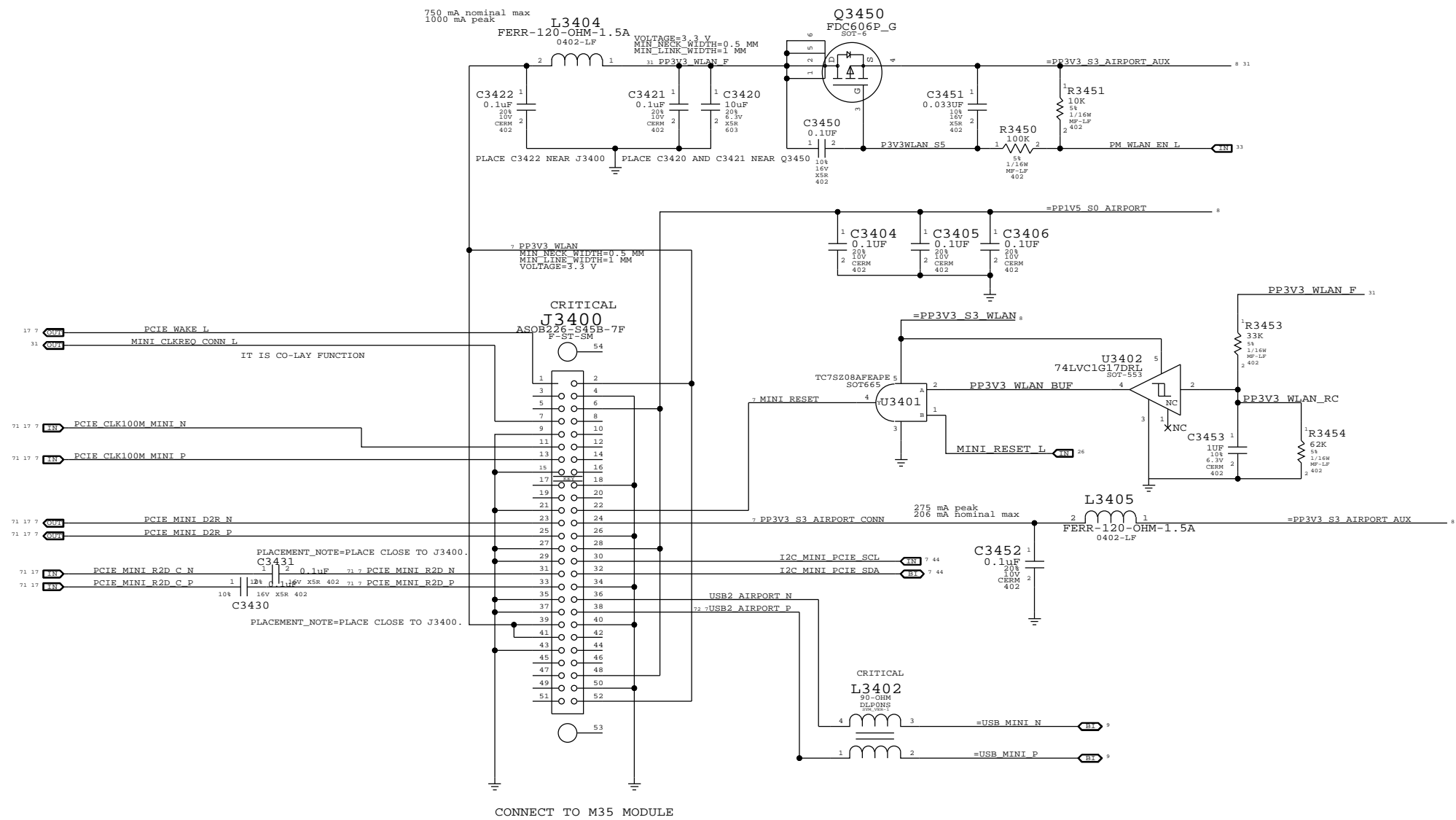
Apple Inc.	051-8089	D
REVISION	A.0.0	
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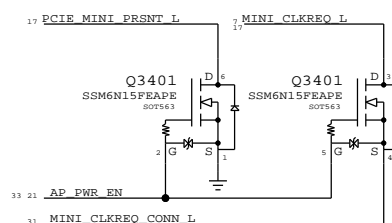
PAGE	33 OF 109
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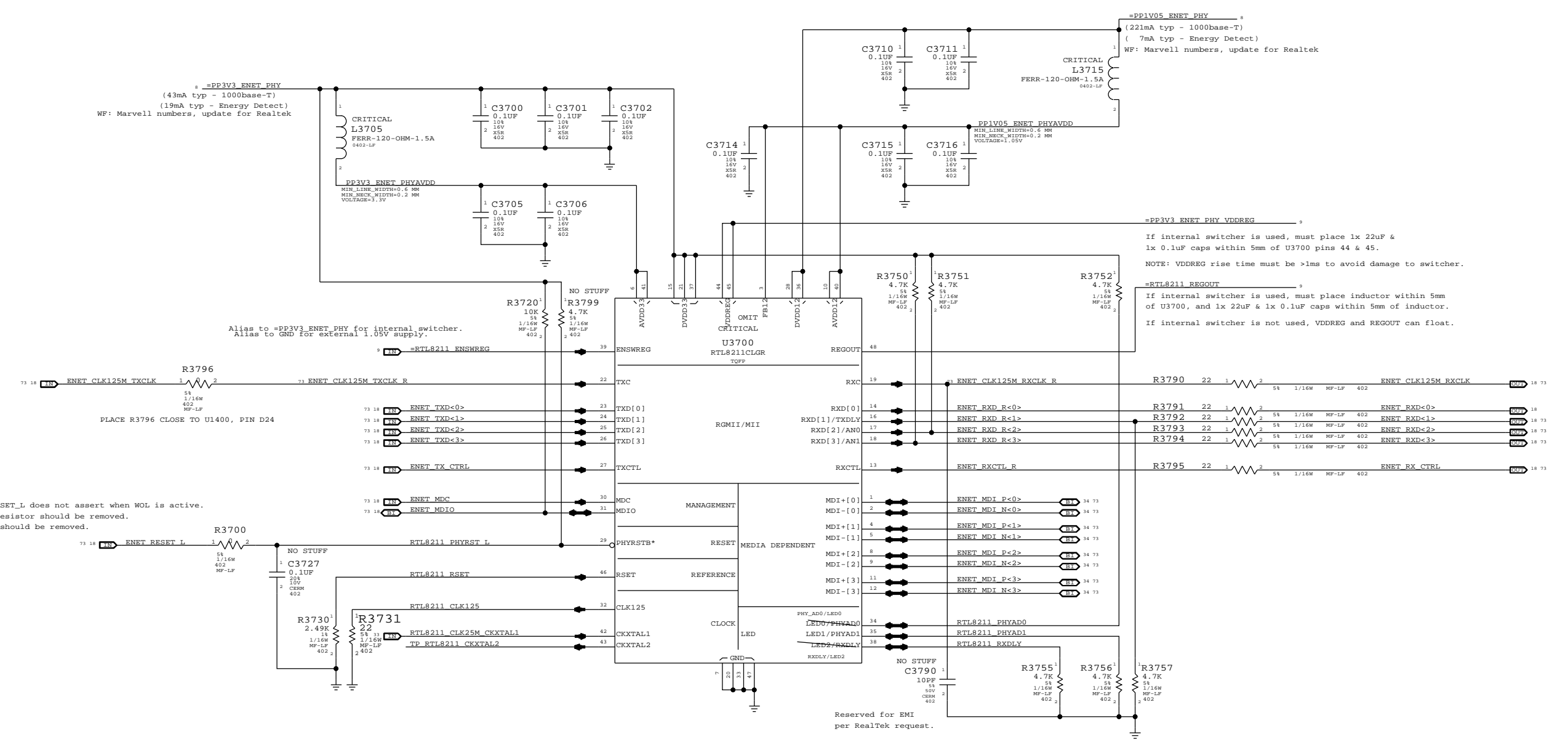
AIRPORT



CONNECT TO M35 MODULE
 OLD:516S0406 (FOXCONN ONLY)
 NEW:516S0635 (FOXCONN & ACON)



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
Right Clutch Connector			
 Apple Inc.		DRAWING NUMBER 051-8089	REVISION A.0.0
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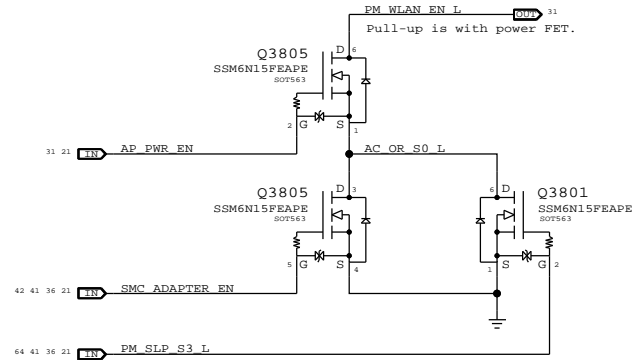
WF: Verify that ENET_RESET_L does not assert when WOL is active. If true, RC and 0-ohm resistor should be removed. If false, ENET_RESET_L should be removed.

Configuration Settings:
 PHYAD = 01 (PHY Address 00001)
 AN[1:0] = 11 (Full auto-negotiation)
 RXDLY = 0 (RXCLK transitions with data)
 TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=SUMA		SYNC DATE=03/20/2008	
Ethernet PHY (RTL8211CL)			
Apple Inc.		DESIGN NUMBER	051-8089
		REVISION	A.0.0
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		PAGE	37 OF 109
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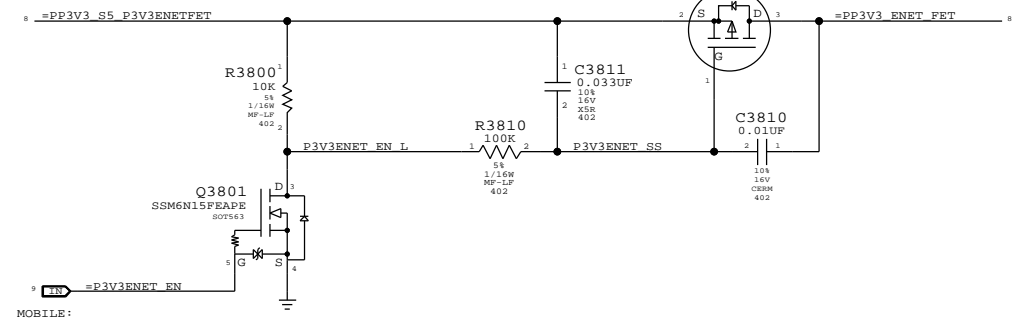
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

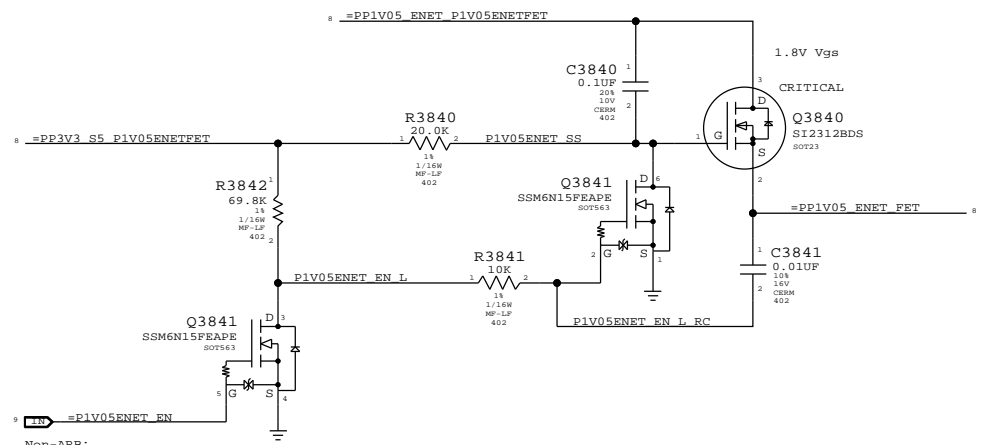
CRITICAL
 @ 2.5V Vgs:
 Rds(on) = 90mOhm max
 I(max) = 1.7A (85C)



MOBILE:
 Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

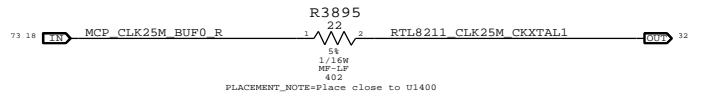
1.8V Vgs
 CRITICAL



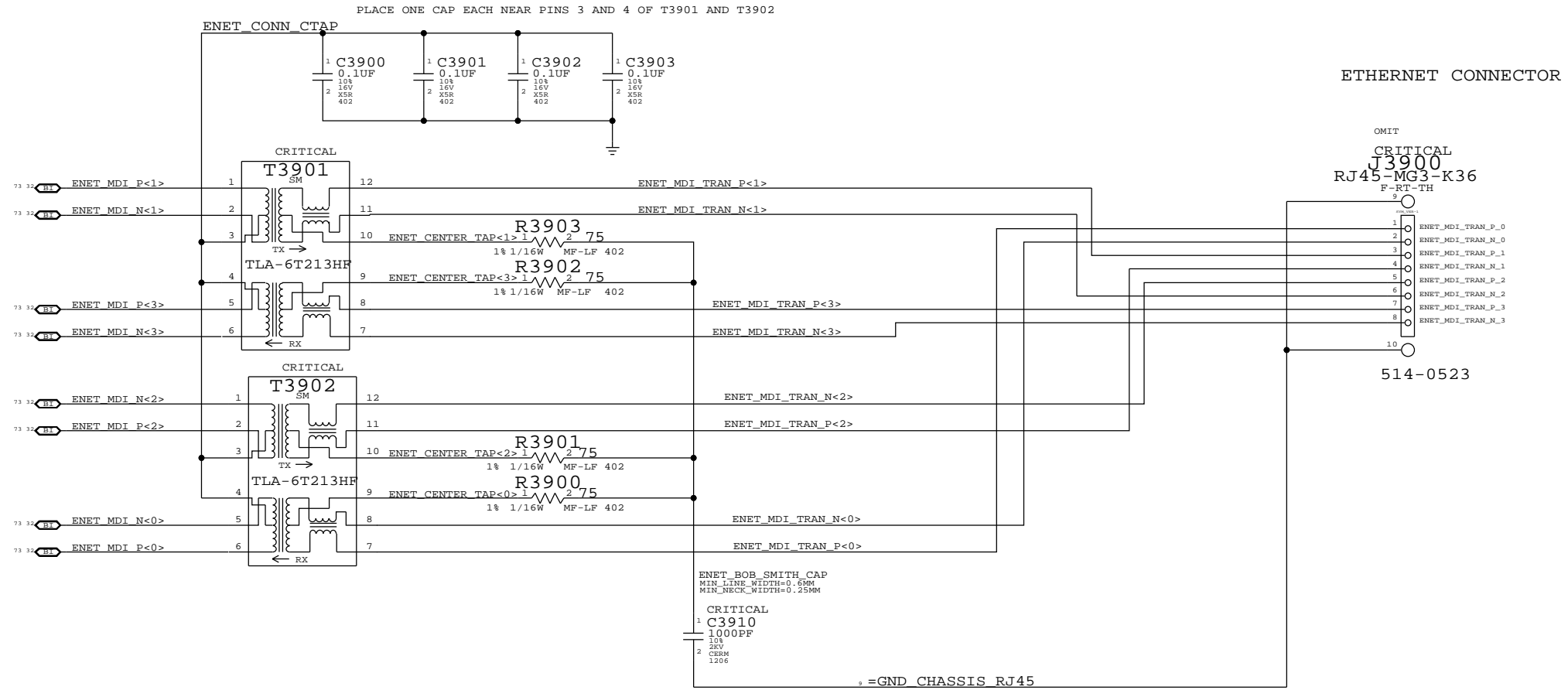
Non-ARB:
 Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

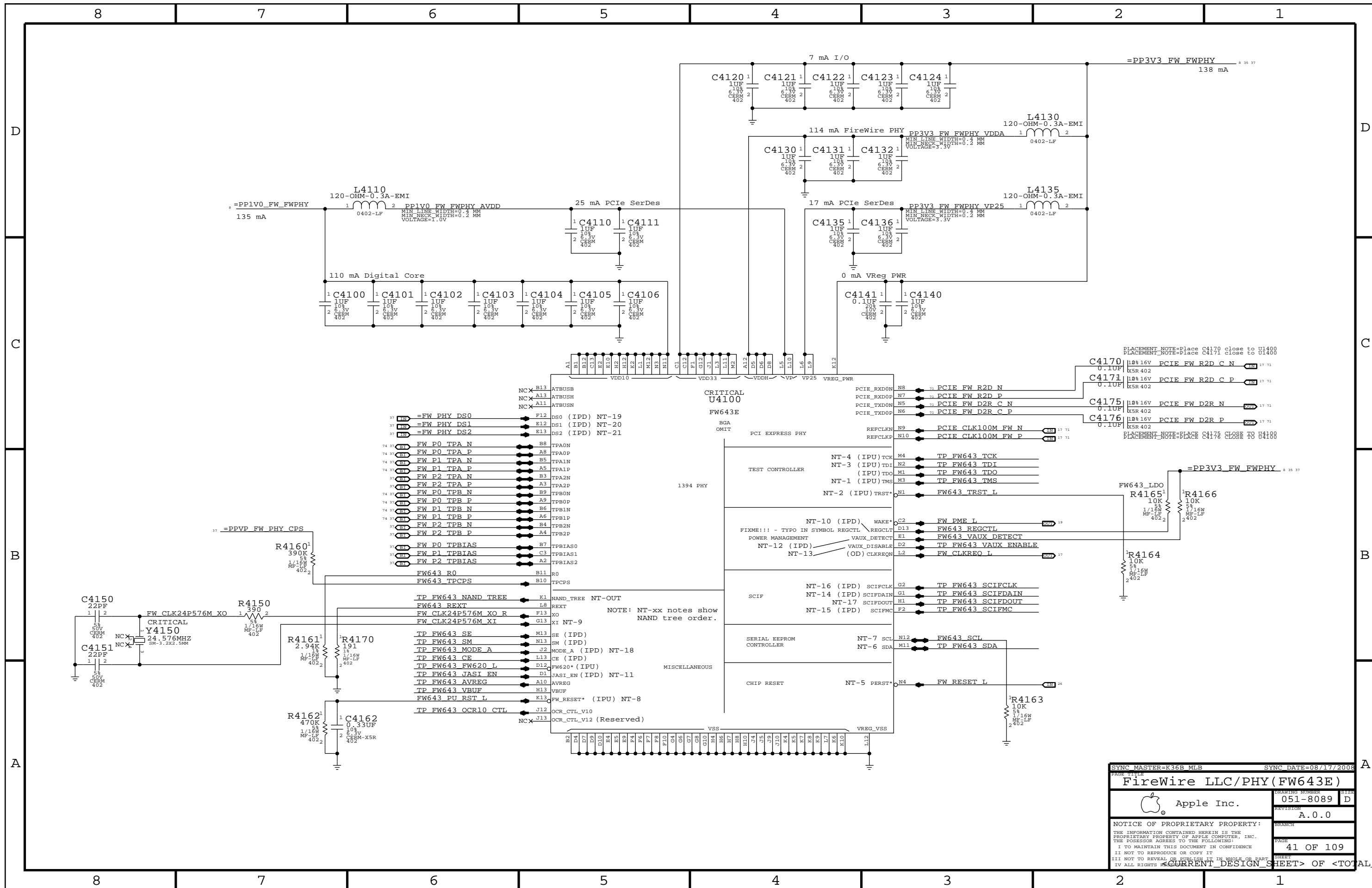
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC MASTER=SUMA		SYNC DATE=04/04/2008	
Ethernet & AirPort Support			
Apple Inc.		051-8089	D
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ETHERNET CONNECTOR			
Apple Inc.		DRAWING NUMBER	051-8089 D
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SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE			
FireWire LLC/PHY (FW643E)			
Apple Inc.		DRAWING NUMBER	051-8089 D
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SHEET		PAGE	
41 OF 109		41 OF 109	

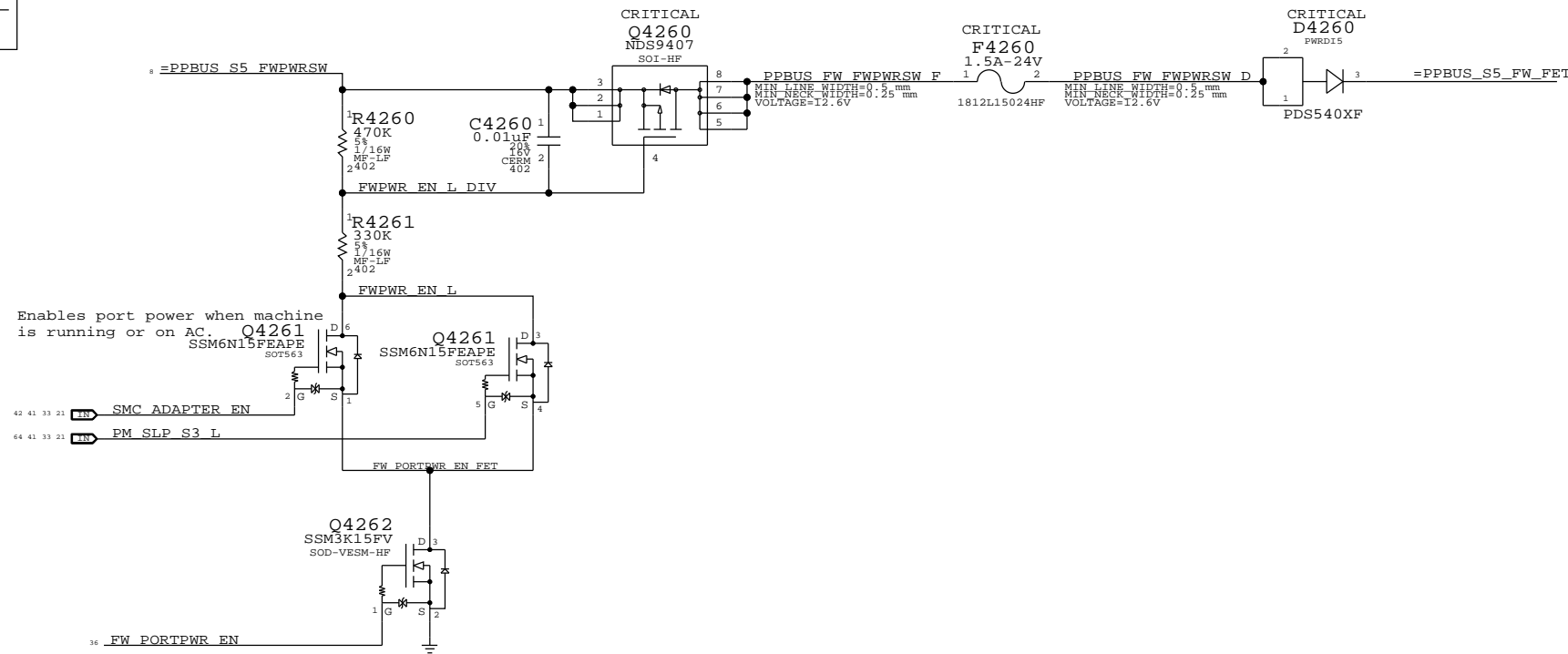
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

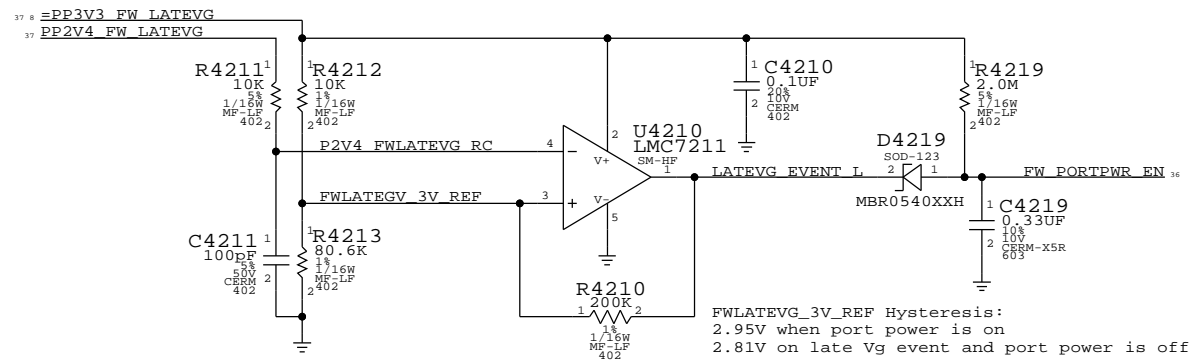
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE FireWire Port Power			
DRAWING NUMBER 051-8089		REV D	
REVISION A.0.0		BRANCH	
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CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS			

Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

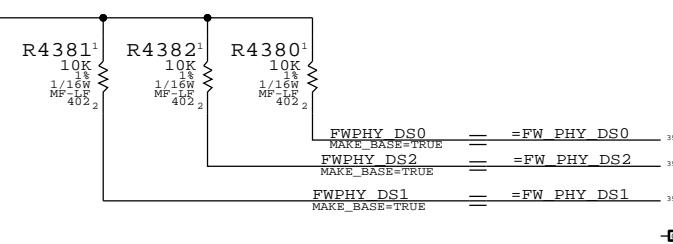
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

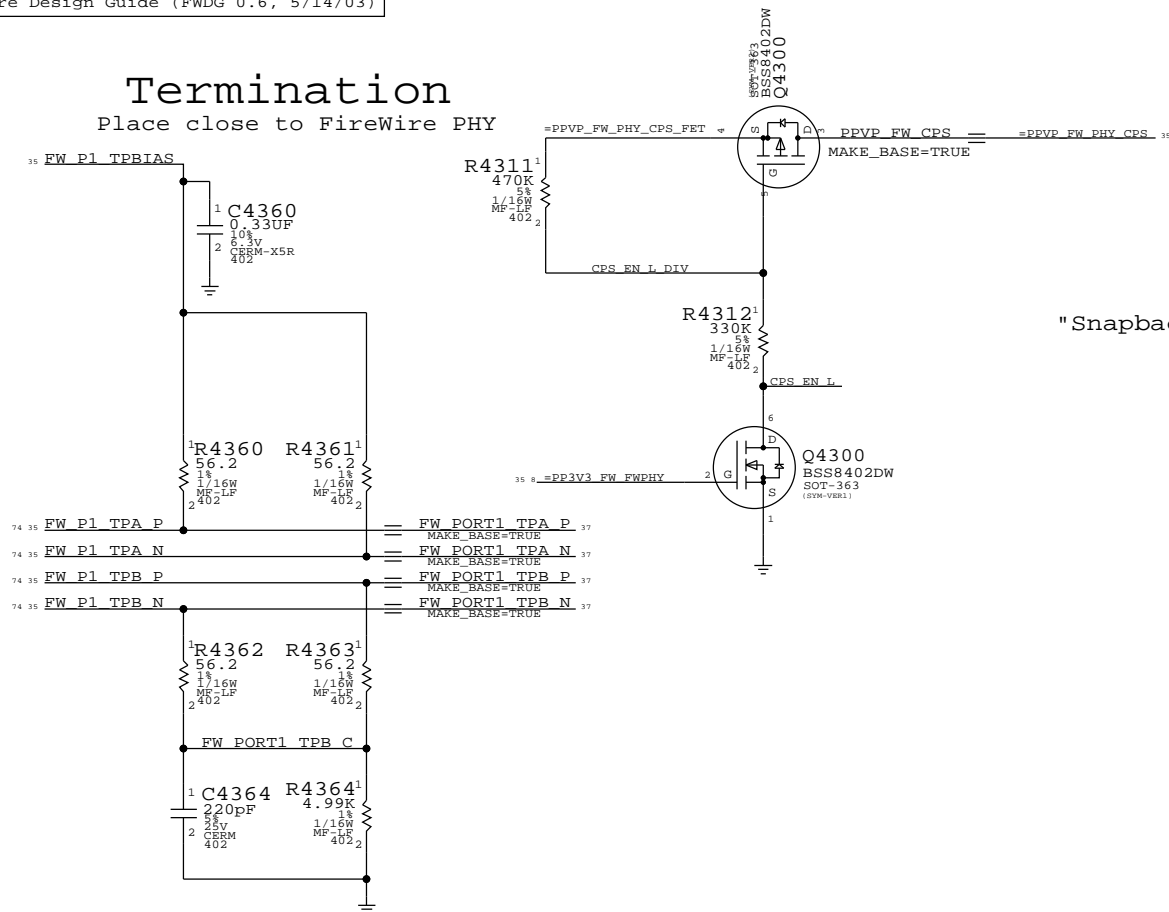
Configures PHY for:
 - 1-port Portable Power Class (0)



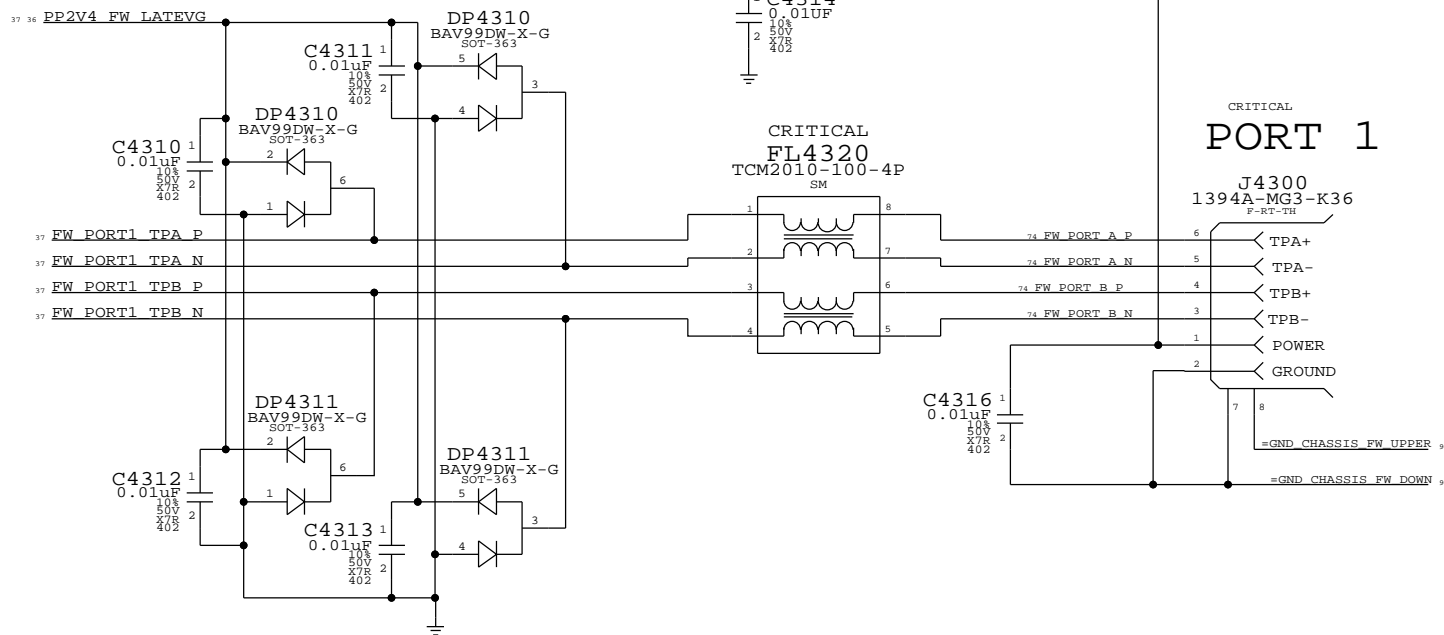
35	FW_P0_TPB_IAS	=	NC_FW0_TPB_IAS	MAKE_BASE=TRUE
35	FW_P2_TPB_IAS	=	NC_FW2_TPB_IAS	MAKE_BASE=TRUE
74	FW_P0_TPA_N	=	NC_FW0_TPA_N	MAKE_BASE=TRUE
74	FW_P2_TPA_N	=	NC_FW2_TPA_N	MAKE_BASE=TRUE
35	FW_P2_TPA_P	=	NC_FW2_TPA_P	MAKE_BASE=TRUE
74	FW_P0_TPB_N	=	NC_FW0_TPB_N	MAKE_BASE=TRUE
74	FW_P0_TPB_P	=	NC_FW0_TPB_P	MAKE_BASE=TRUE
35	FW_P2_TPB_N	=	NC_FW2_TPB_N	MAKE_BASE=TRUE
35	FW_P2_TPB_P	=	NC_FW2_TPB_P	MAKE_BASE=TRUE

Termination

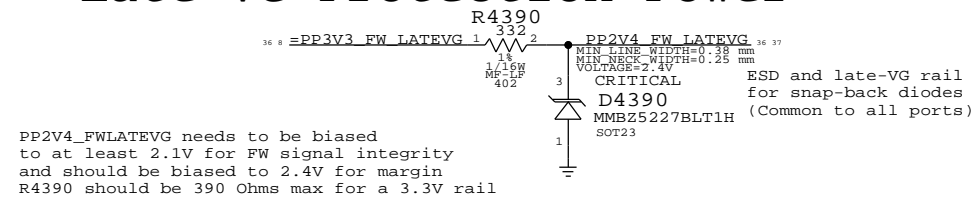
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



Late-VG Protection Power



PAGE TITLE		SYNC DATE=(MASTER)	
FireWire Ports			
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Apple Logo		051-8089	D
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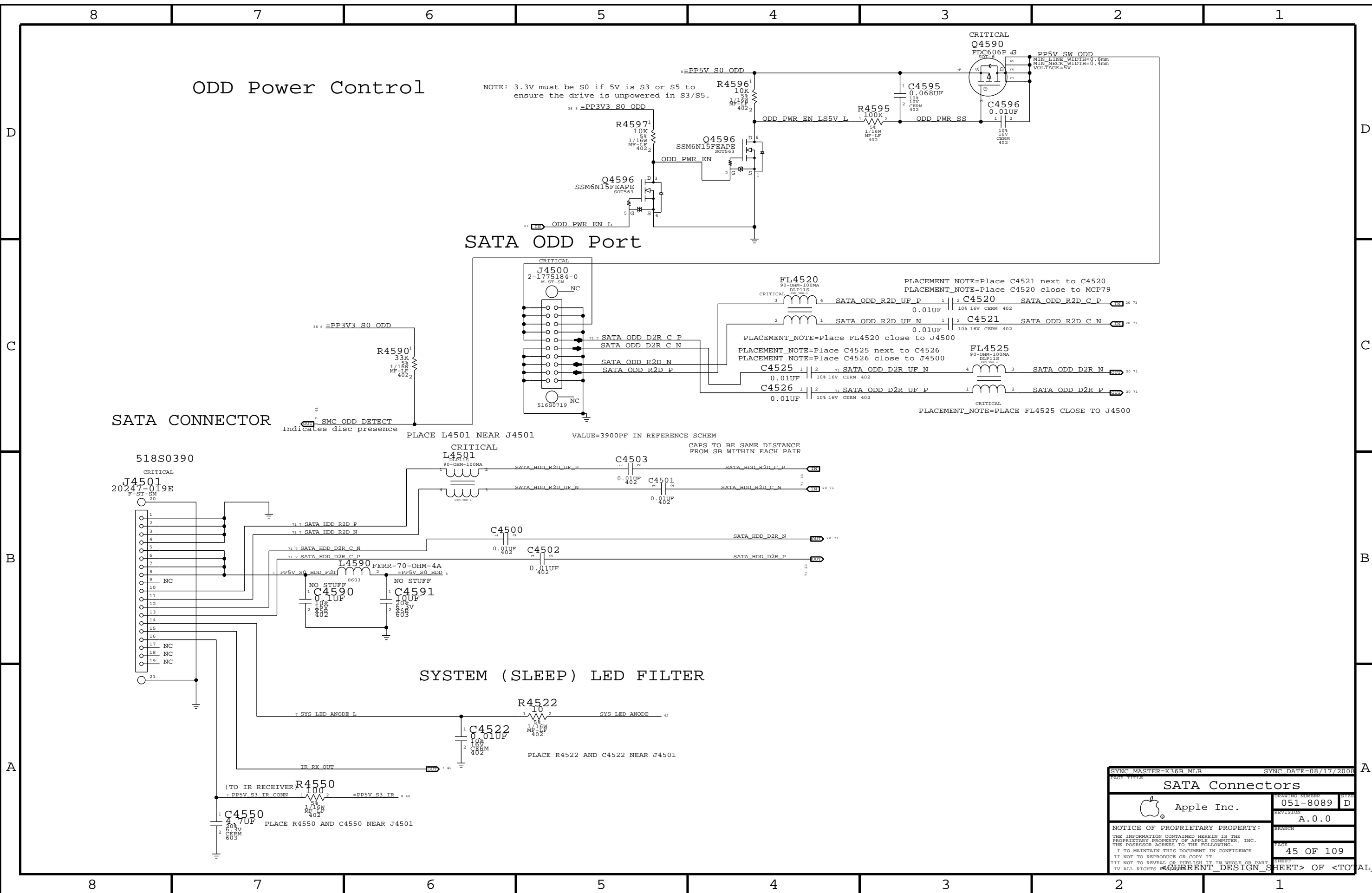
ODD Power Control

NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

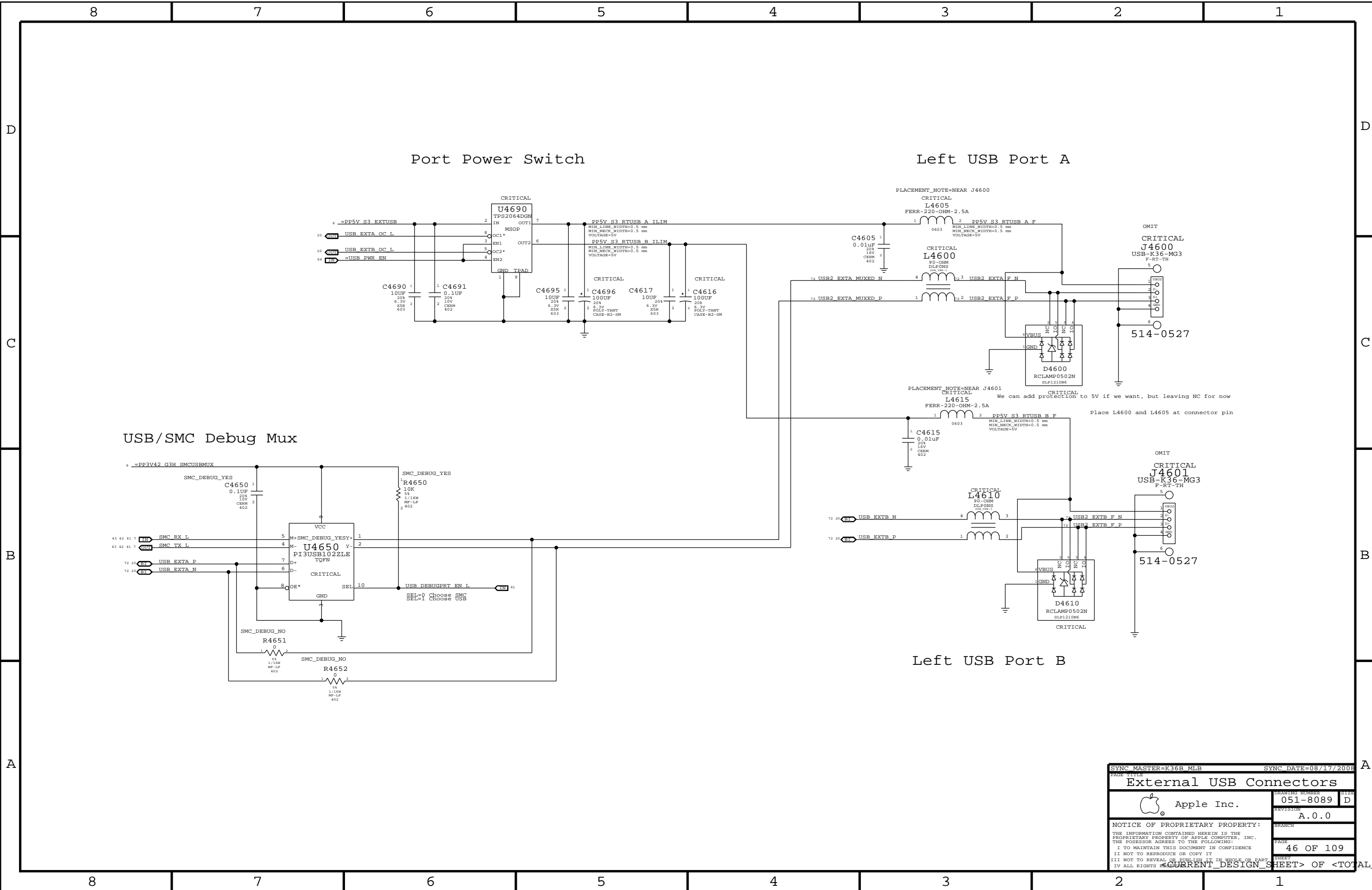
SATA ODD Port

SATA CONNECTOR

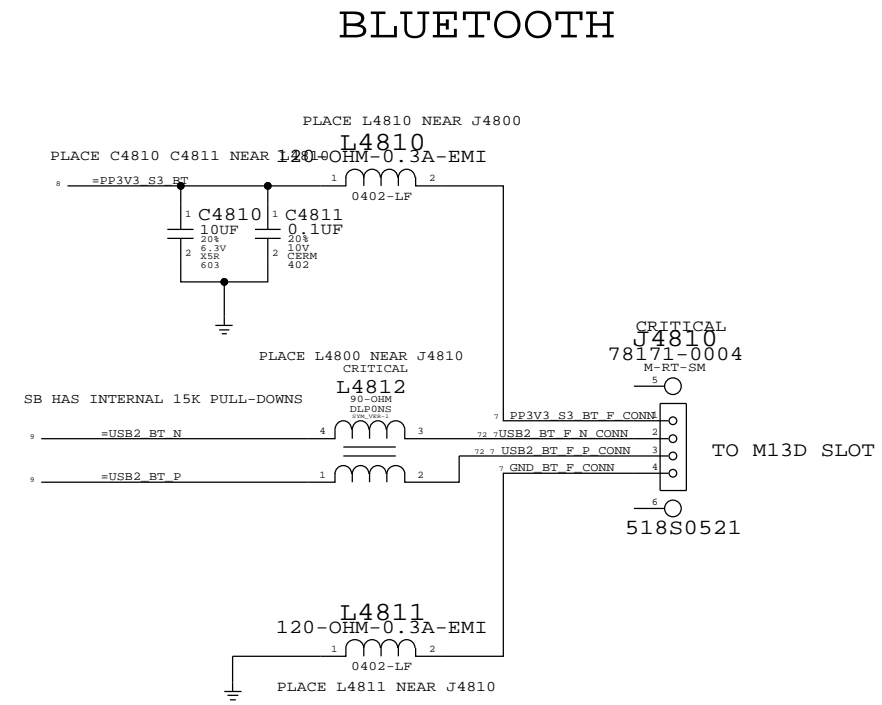
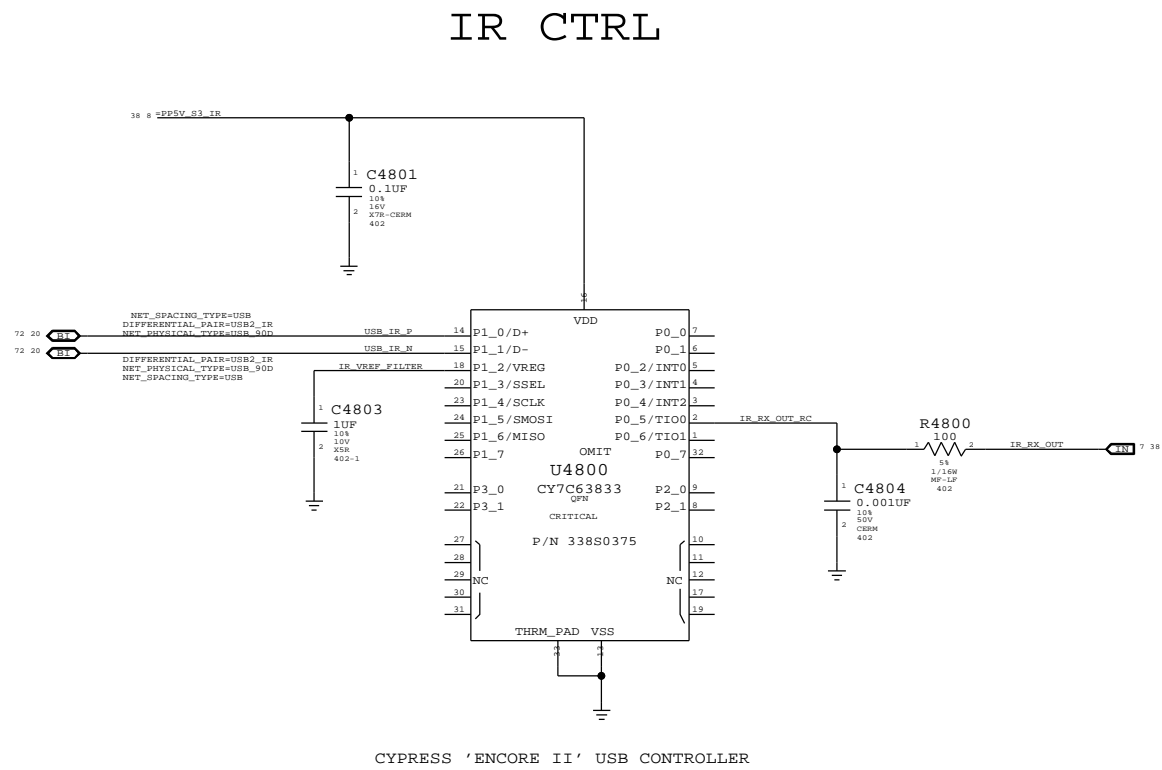
SYSTEM (SLEEP) LED FILTER



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
SATA Connectors			
Apple Inc.		DESIGN NUMBER	051-8089 D
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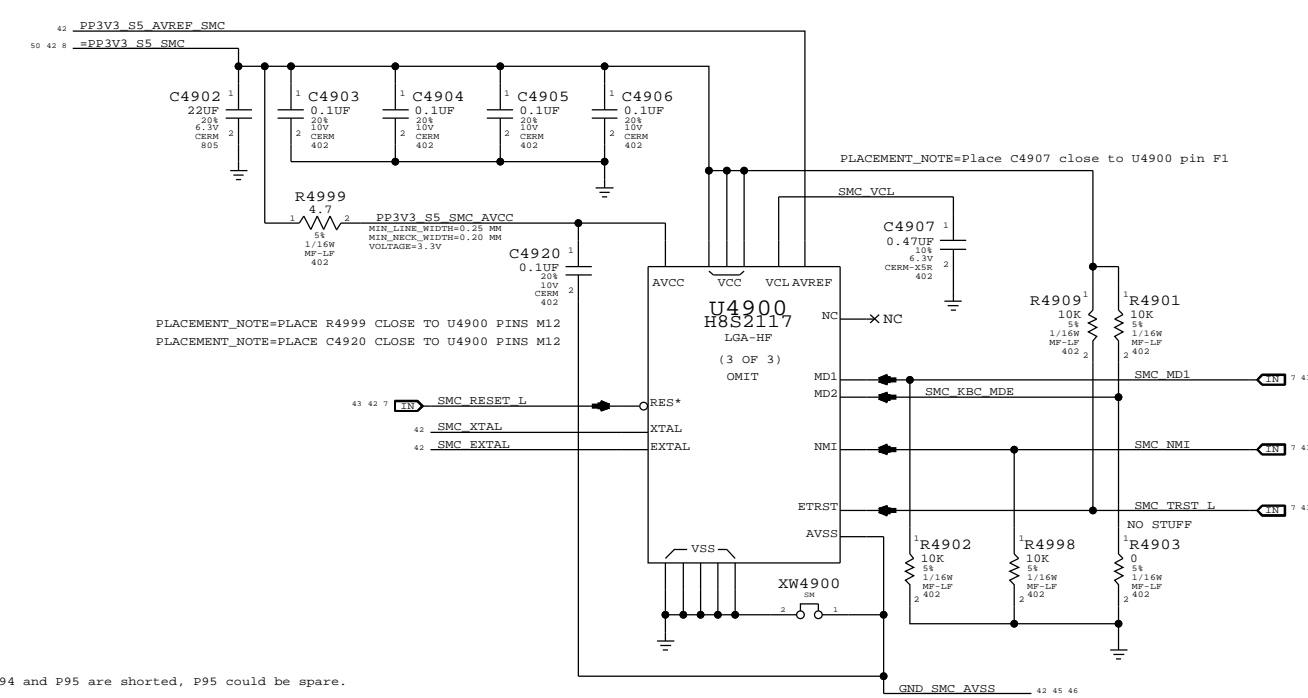
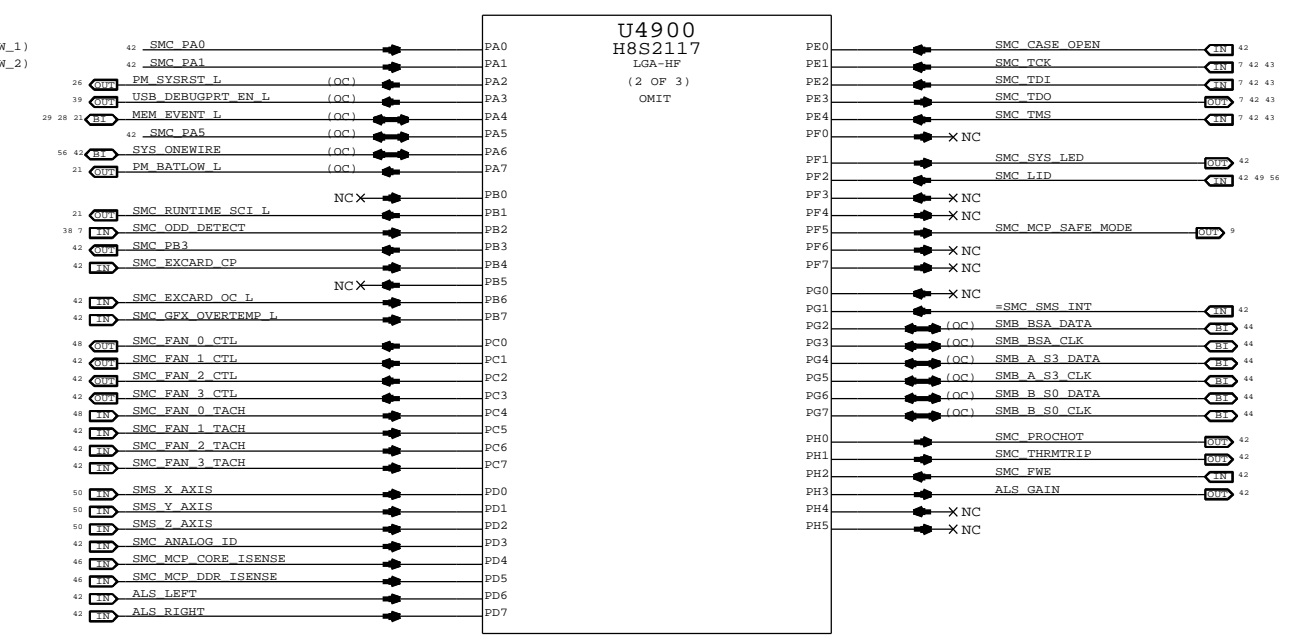
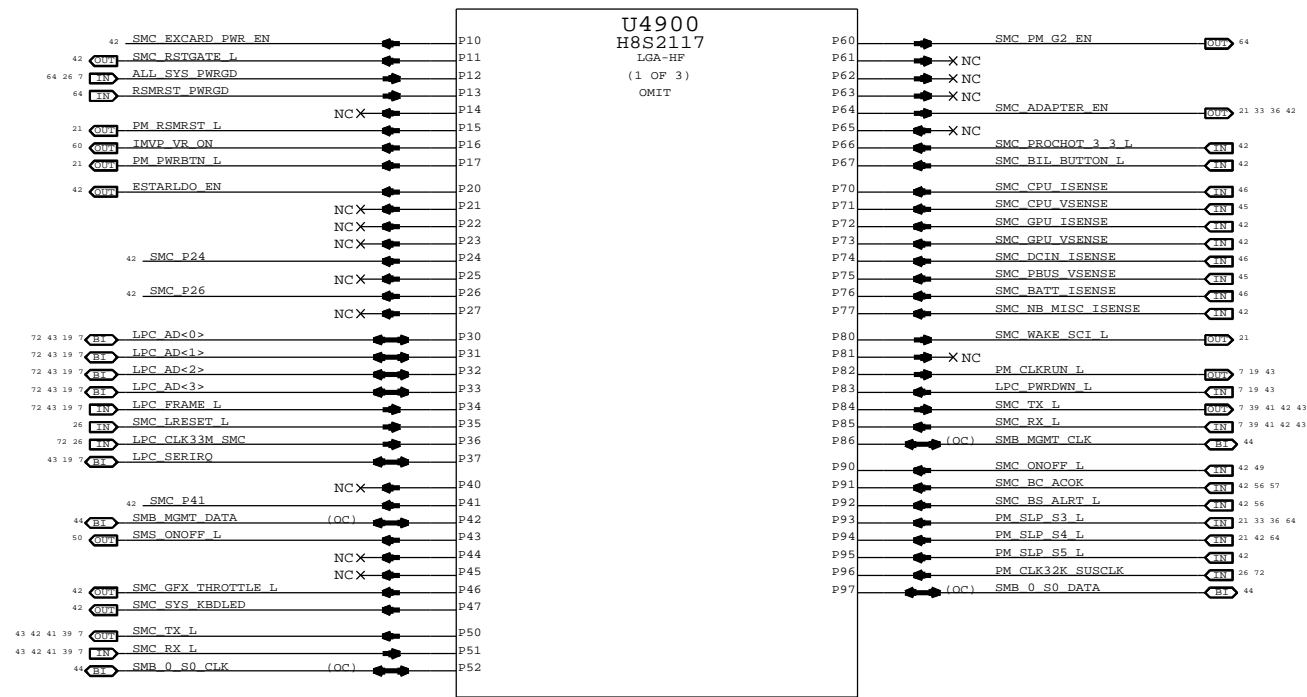


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External USB Connectors			
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Front Flex Support			
Apple Inc.		DRAWING NUMBER 051-8089	SIZE D
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		BRANCH 48 OF 109	SHEET 48 OF 109

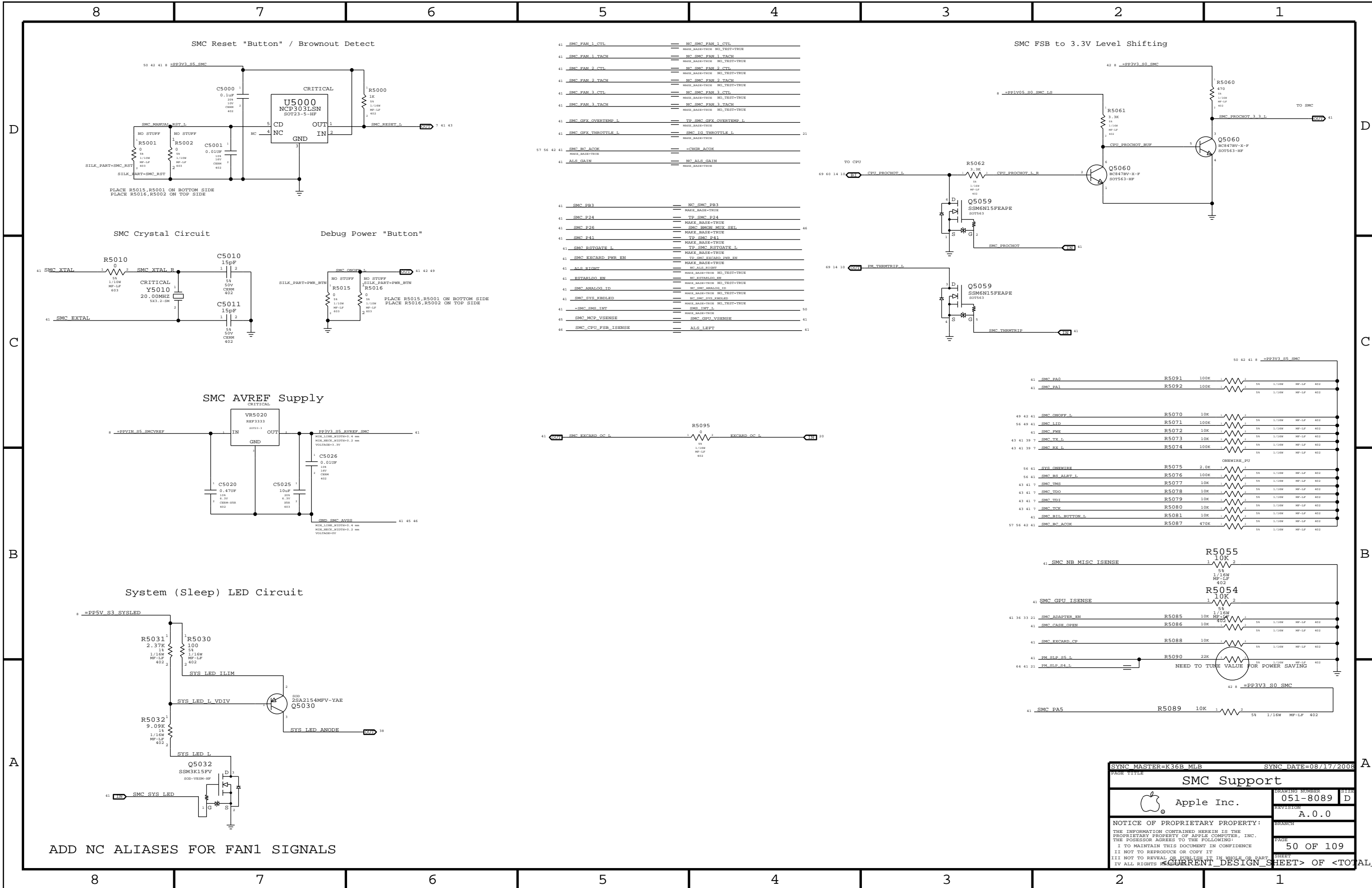
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

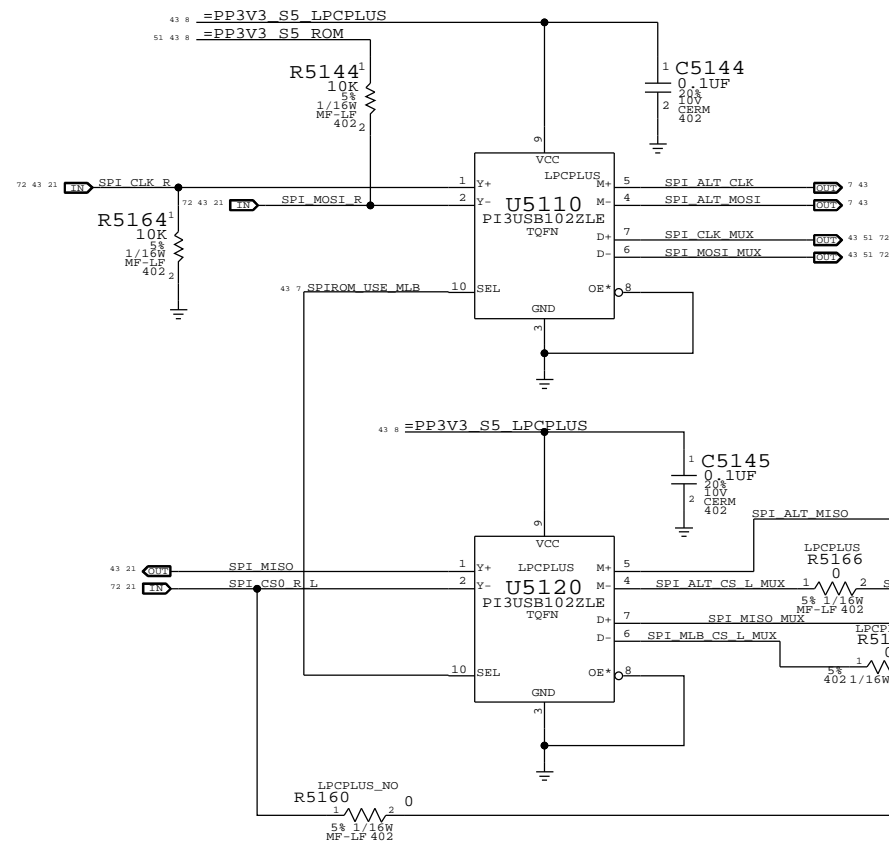
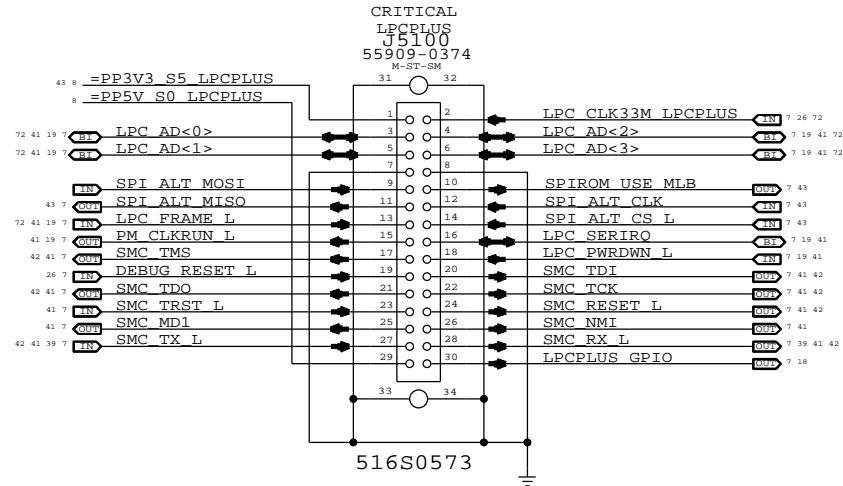
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SMC			
Apple Inc.		DRAWING NUMBER	051-8089
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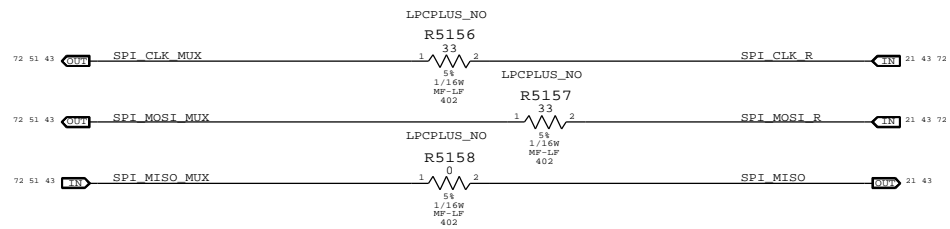
SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
SMC Support			
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		SHEET	

LPC+SPI Connector

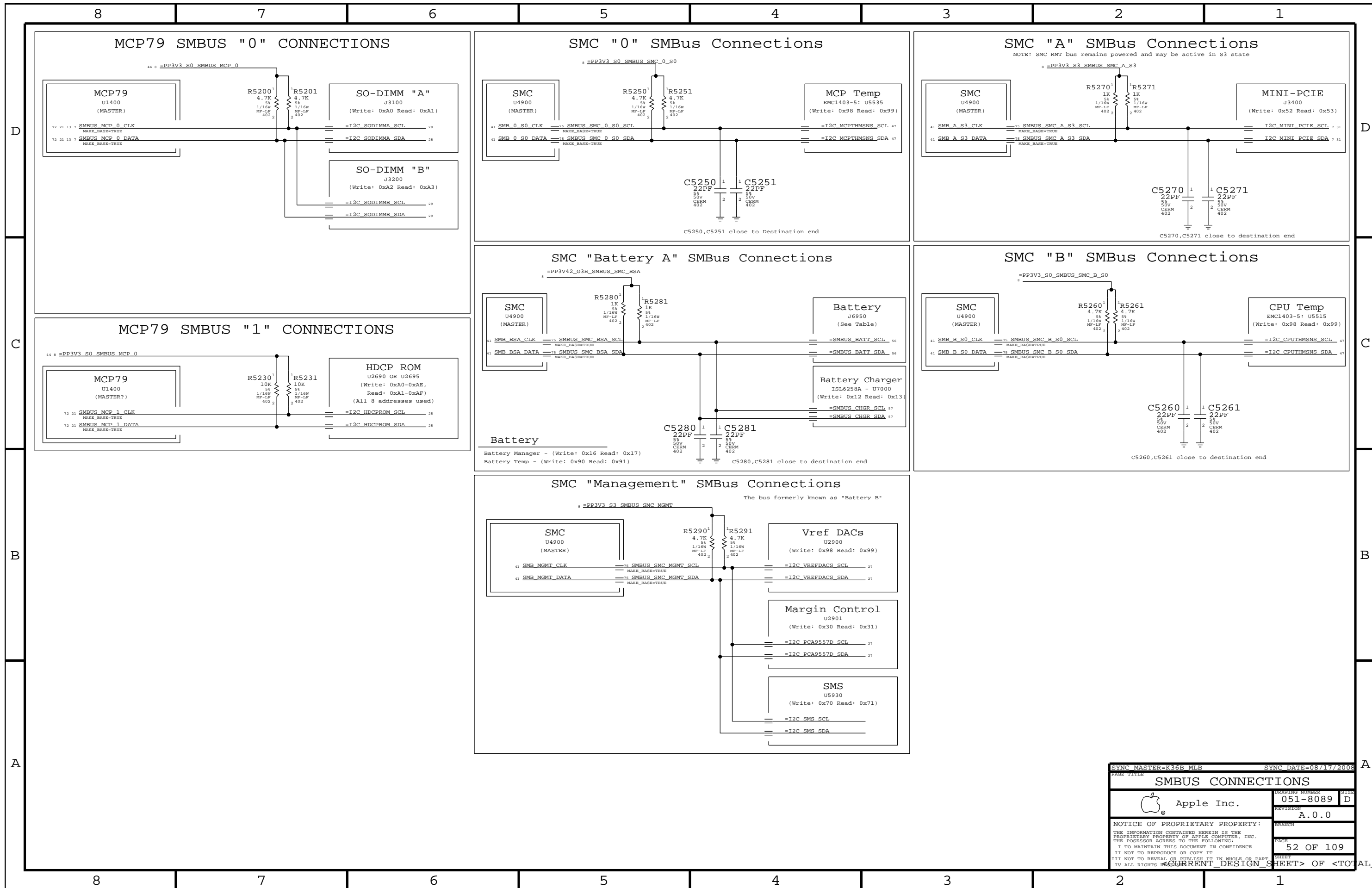
Alternate SPI ROM Support



SPI Bus Series Resistance Option

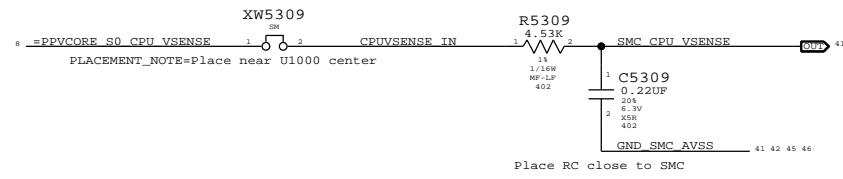


SYNC MASTER=K36B_MLB		SYNC DATE=08/17/2008	
LPC+SPI Debug Connector			
Apple Inc.		051-8089	D
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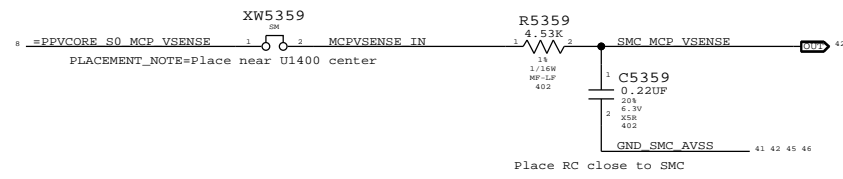


SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
SMBUS CONNECTIONS			
Apple Inc.		DRAWING NUMBER	051-8089
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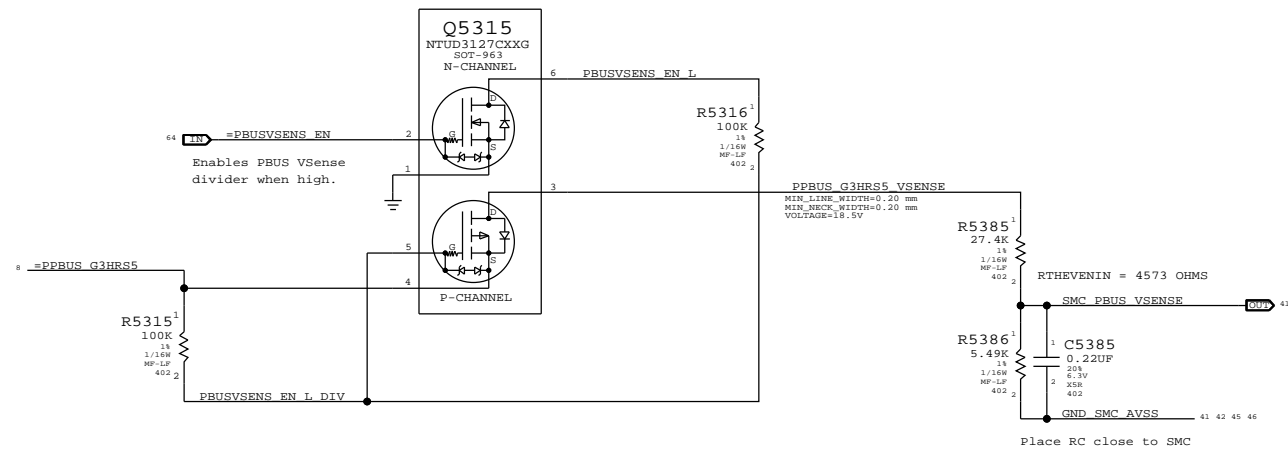
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE: VOLTAGE SENSING			
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8

7

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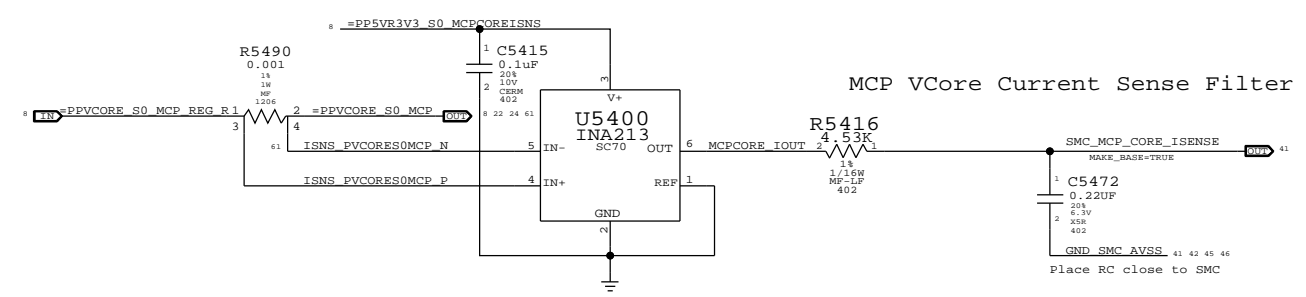
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3

2

1

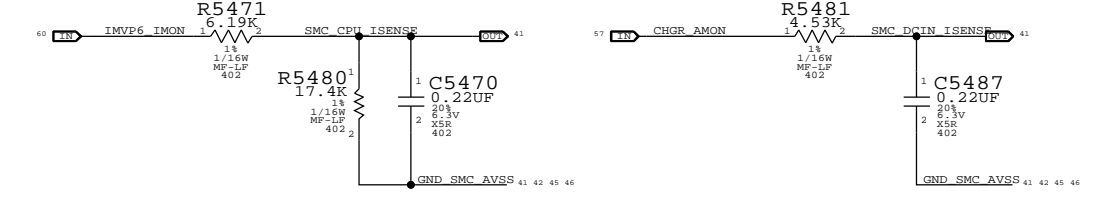
MCP VCore Current Sense



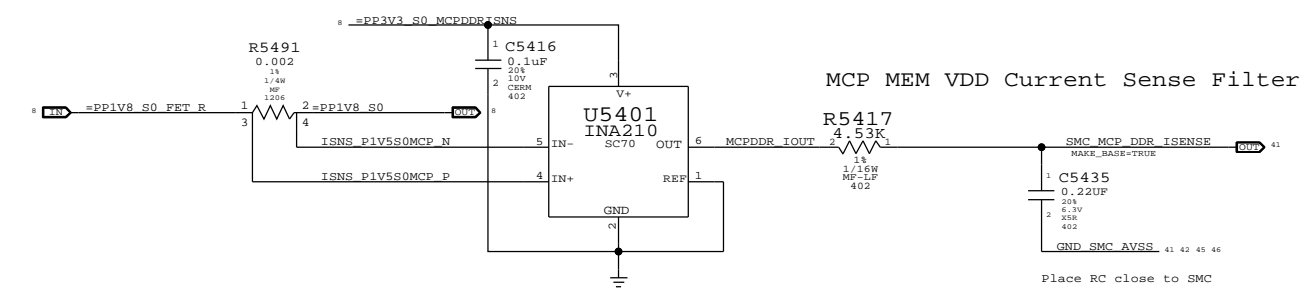
MCP VCore Current Sense Filter

CPU VCore Load Side Current Sensor / Filter

DC-IN (AMON) CURRENT SENSE

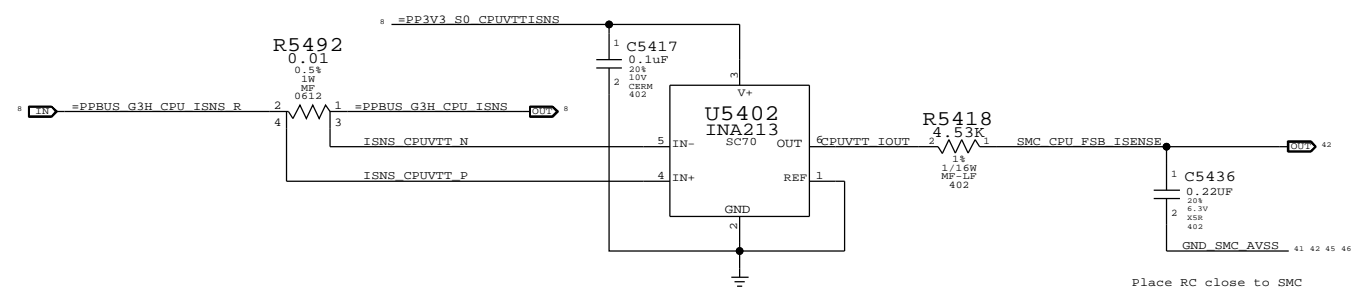


MCP MEM VDD Current Sense

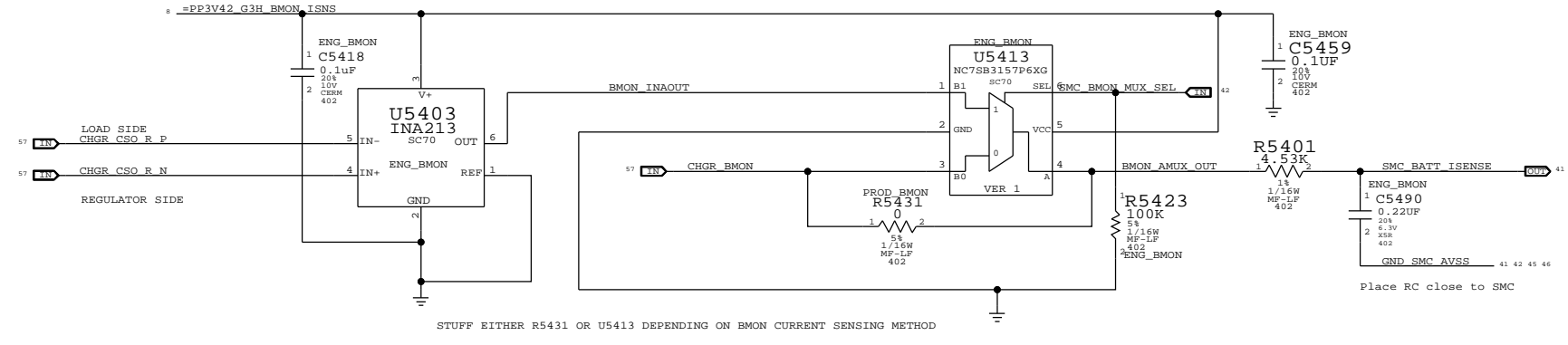


MCP MEM VDD Current Sense Filter

CPU 1.05V CURRENT SENSE



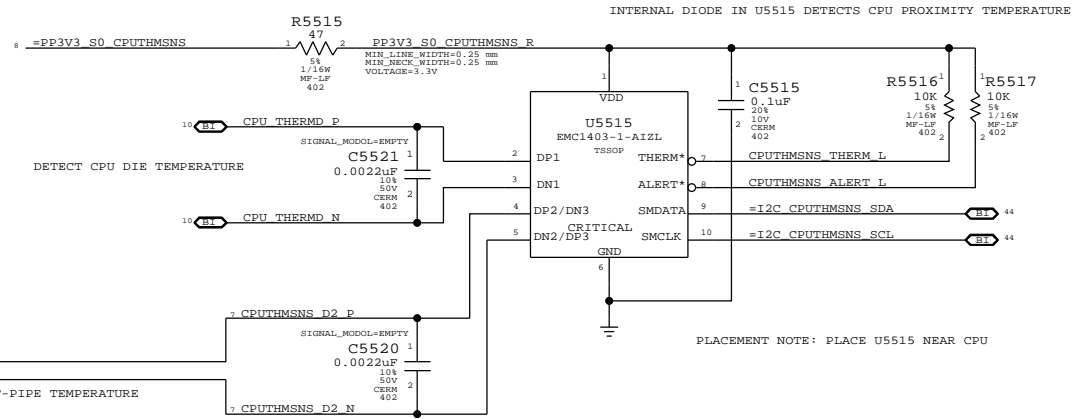
CHARGER BMON CURRENT SENSE



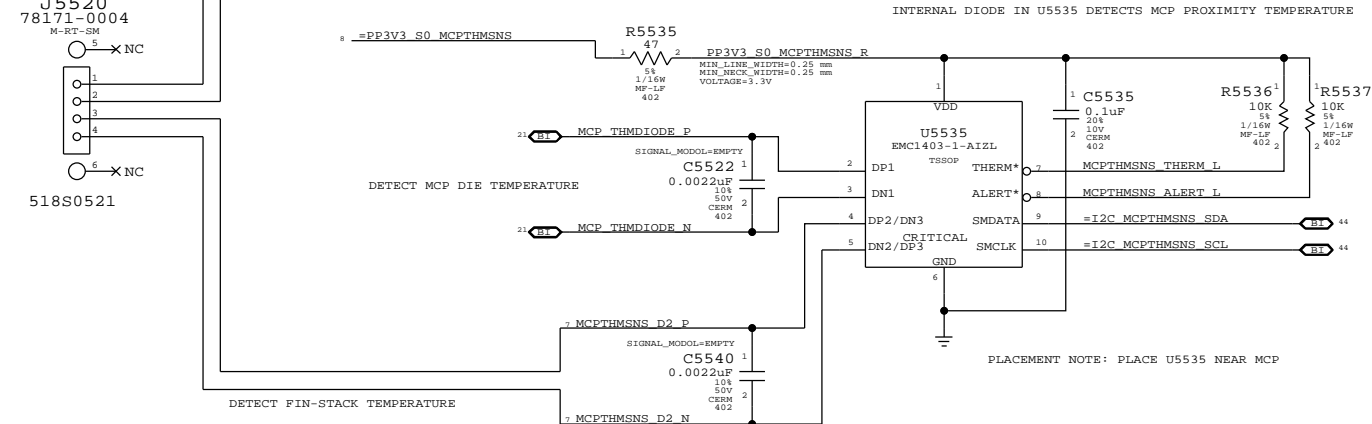
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PAGE TITLE		Current Sensing	
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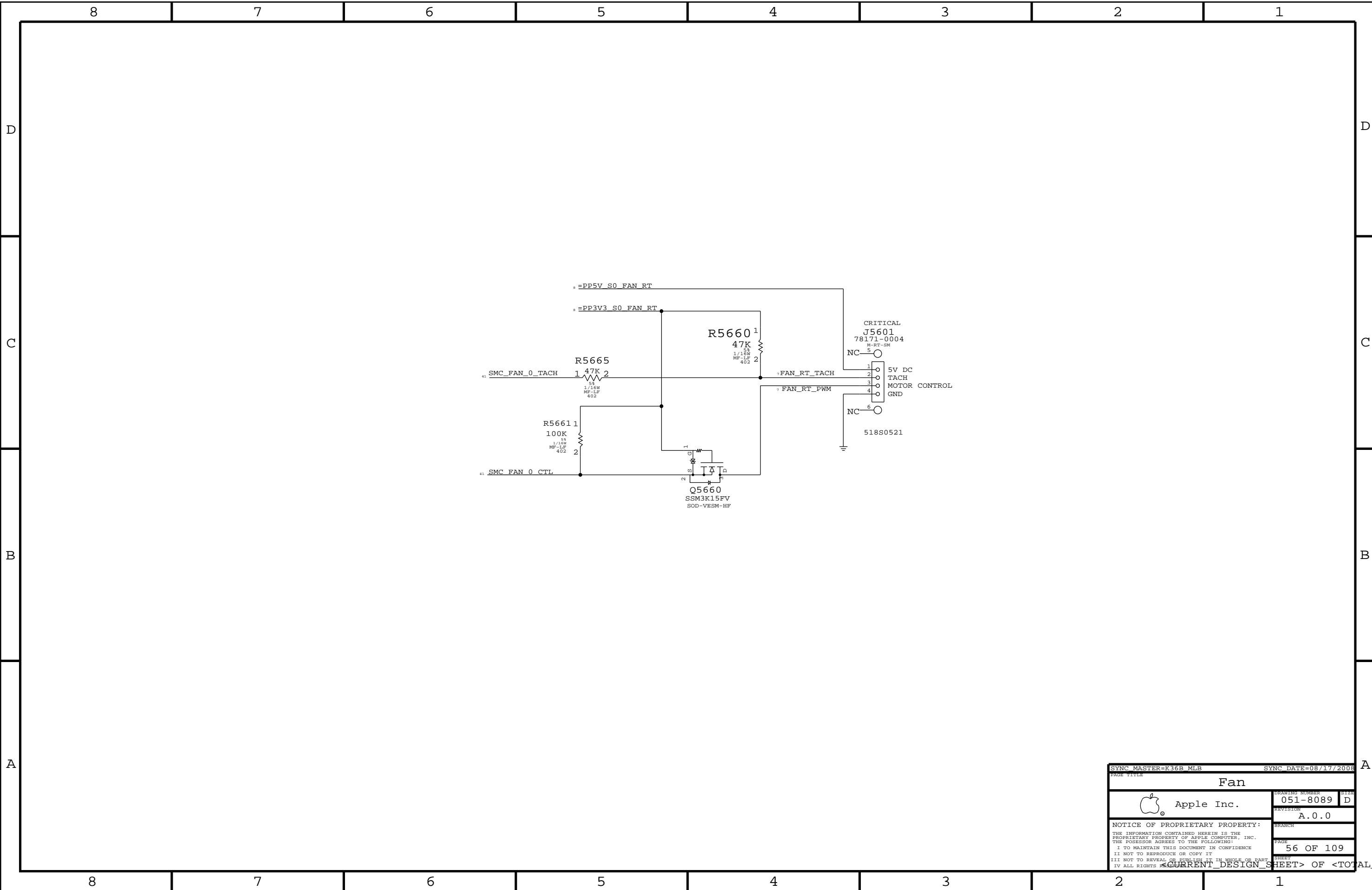
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	051-8089 D
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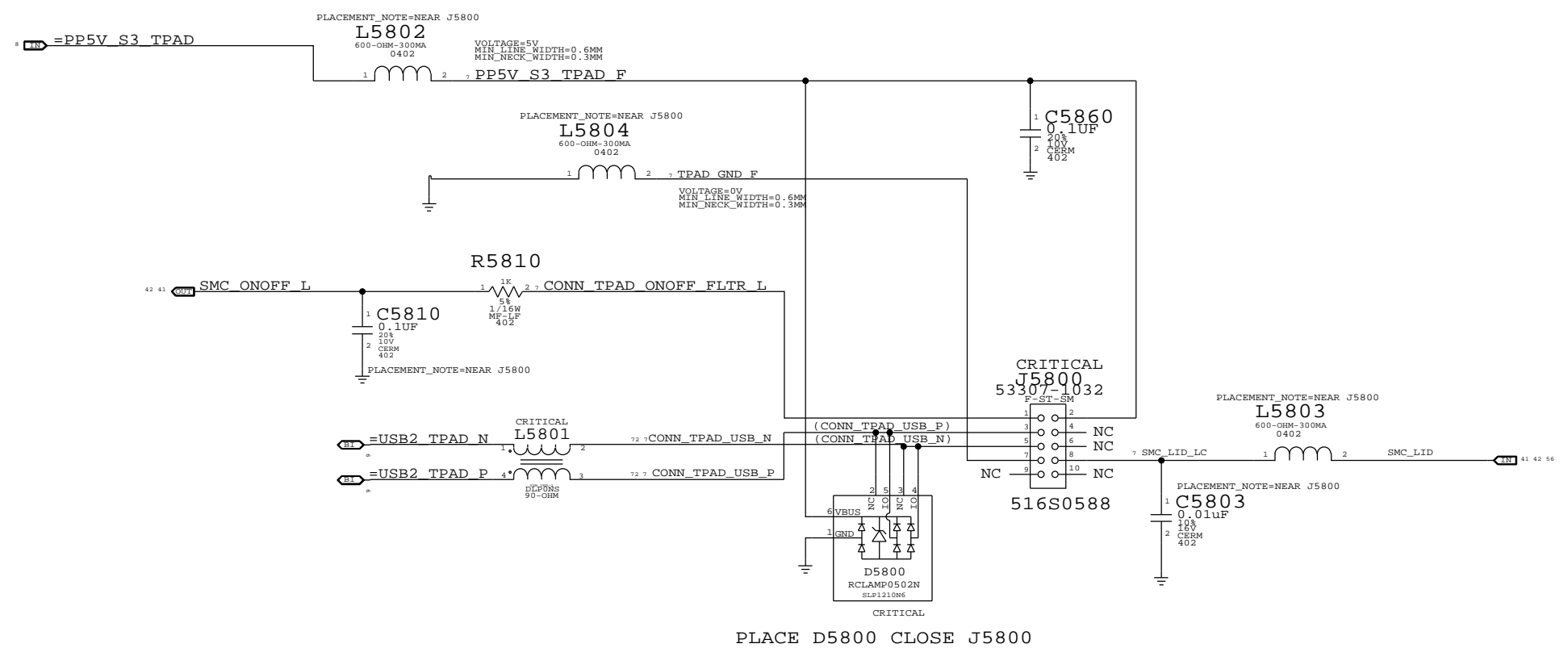
SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
Fan			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8089	D
		REVISION	
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		56 OF 109	
		SHEET	
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- SYNC WITH T18
 - COPY THIS PAGE FROM T18 CSA.58

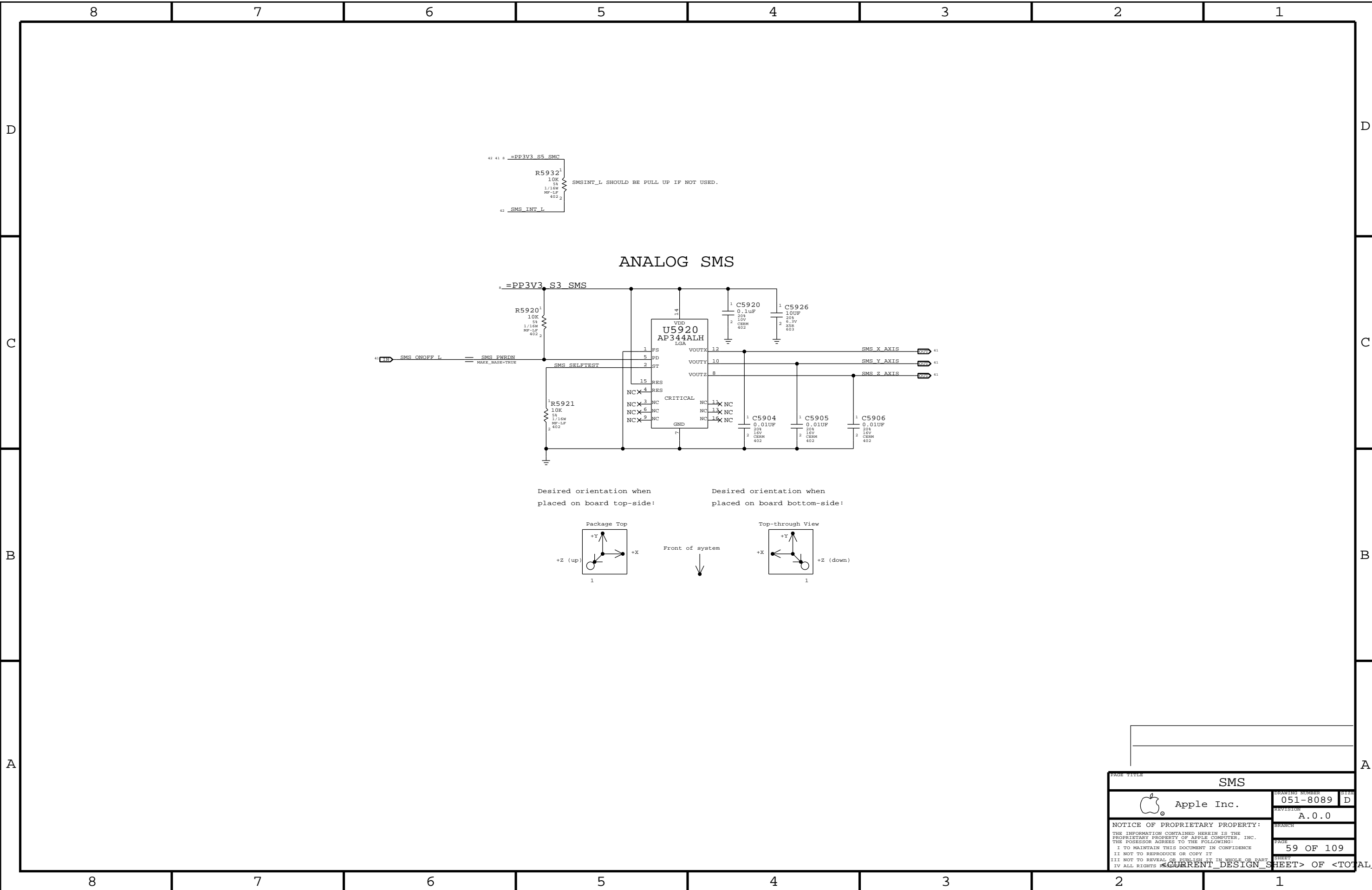
PLACEMENT NOTE

PLACE L5800,L5801,L5803 NEAR J5800
 PLACE C5800,C5810,C5803 NEAR J5800
 PLACE D5800 NEAR J5800

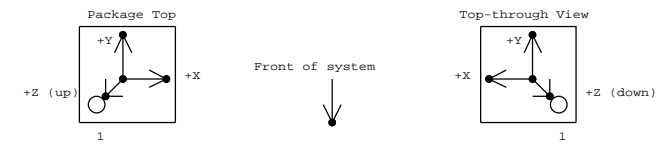
GEYSER



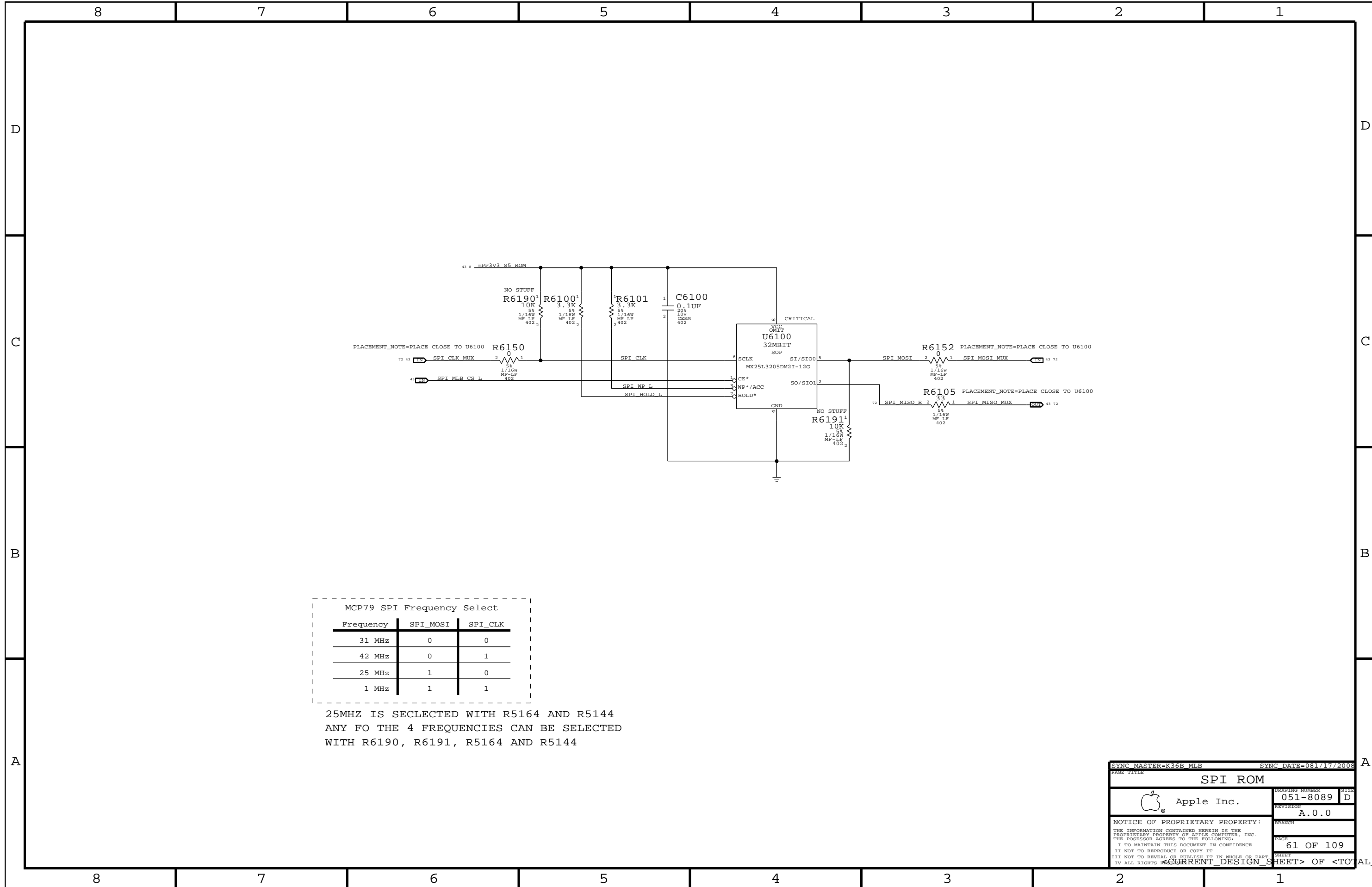
SYNC MASTER=K36B_MLB		SYNC DATE=08/17/2008	
GEYSER			
Apple Inc.		DRAWING NUMBER	SIZE
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		58 OF 109	
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Desired orientation when placed on board top-side: Desired orientation when placed on board bottom-side:



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MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHZ IS SELECTED WITH R5164 AND R5144
 ANY FO THE 4 FREQUENCIES CAN BE SELECTED
 WITH R6190, R6191, R5164 AND R5144

SYNC MASTER=K36B MLB SYNC DATE=081/17/2008

SPI ROM

Apple Inc. DRAWING NUMBER 051-8089 D

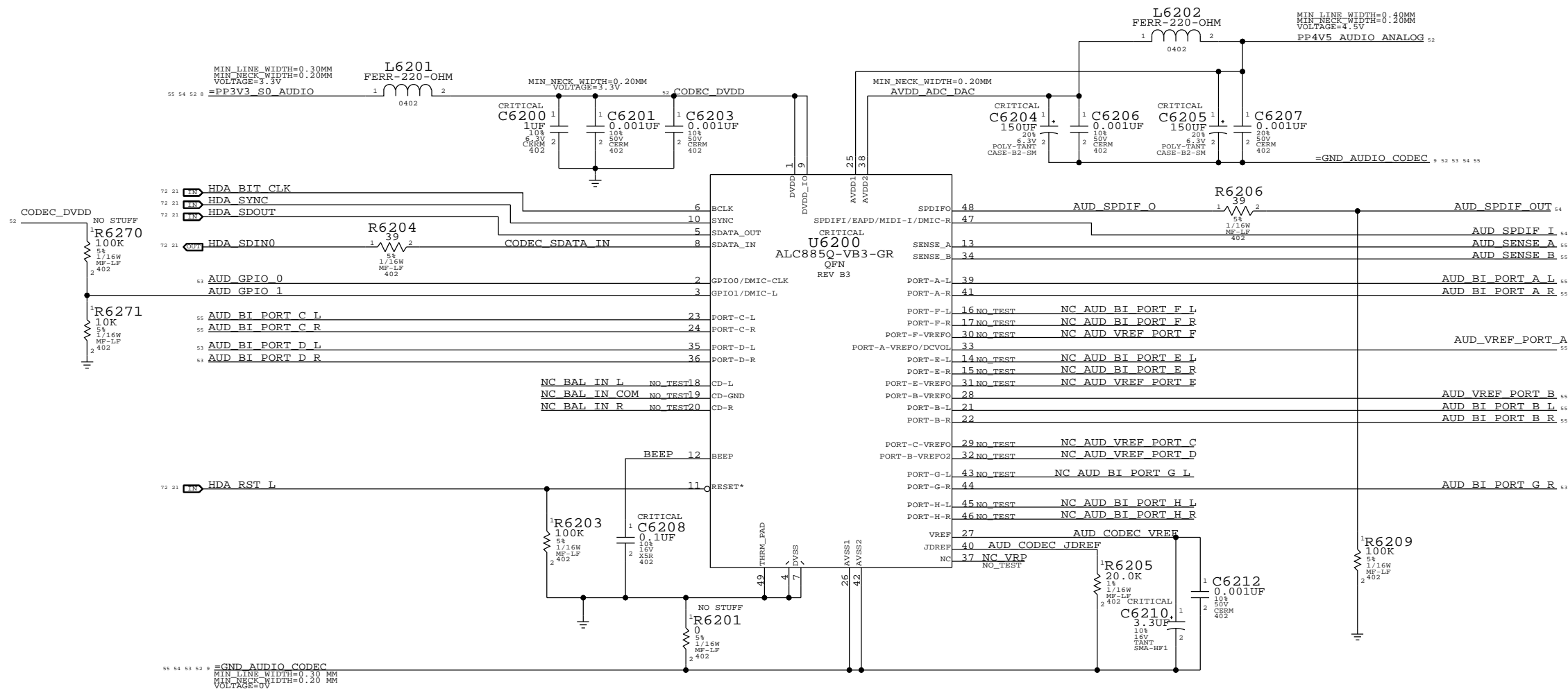
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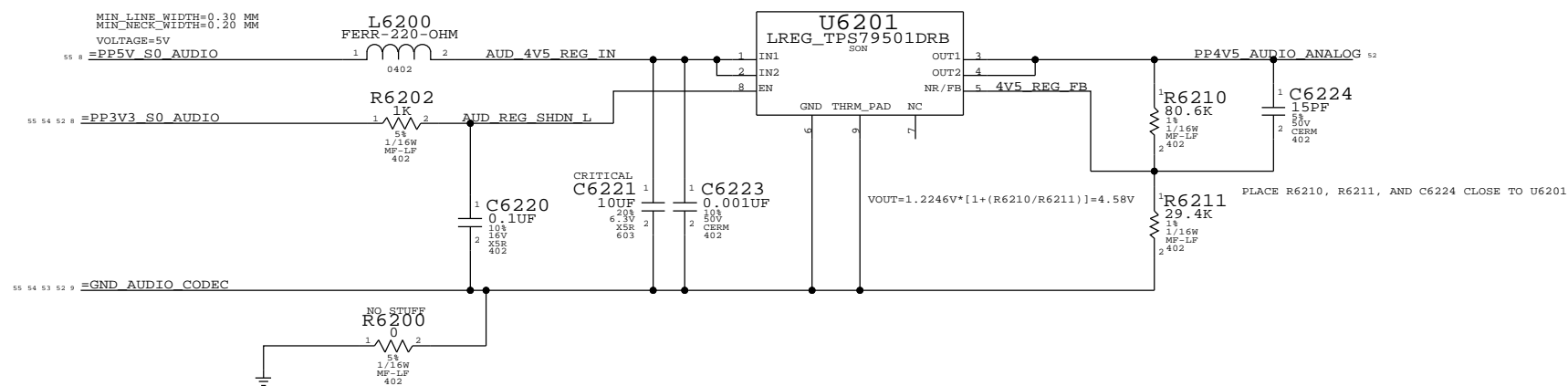
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<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

AUDIO CODEC
APPLE P/N 353S1538



AUDIO 4.5V REGULATOR
APPLE P/N 353S1576



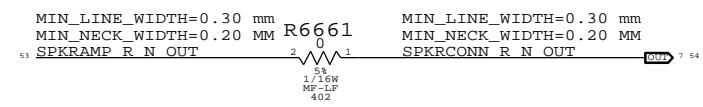
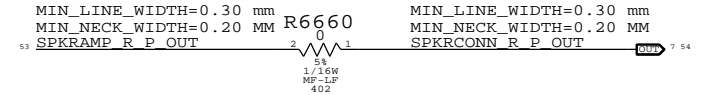
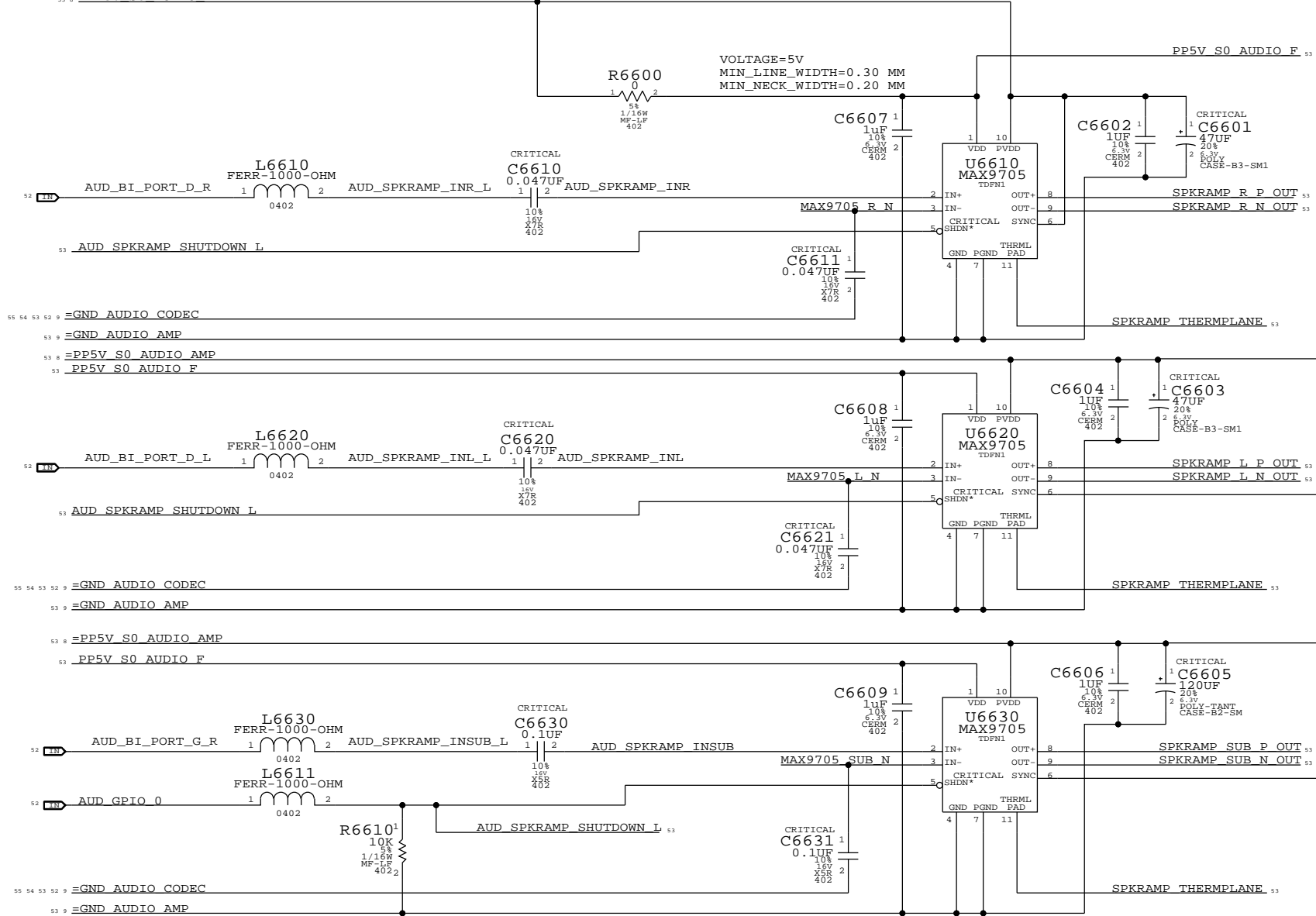
SYNC MASTER=K36A MLB SYNC DATE=08/29/2008

PAGE TITLE		AUDIO: CODEC	
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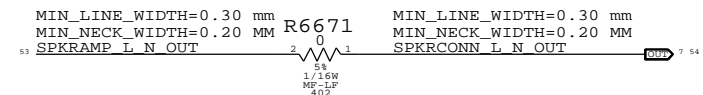
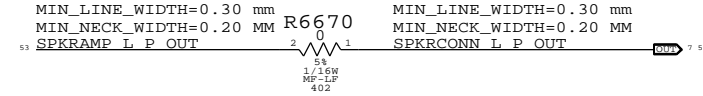
SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 12DB

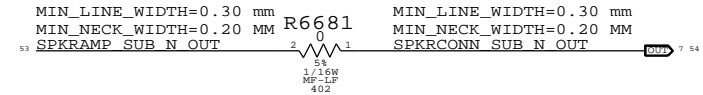
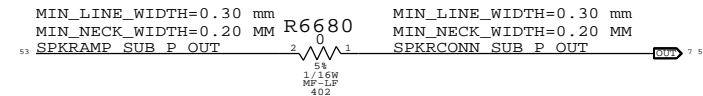
VOLTAGE=5V
 MIN_LINE_WIDTH=0.60 MM
 MIN_NECK_WIDTH=0.20 MM
 PP5V_S0_AUDIO_AMP



RIGHT SATELLITE



LEFT SATELLITE



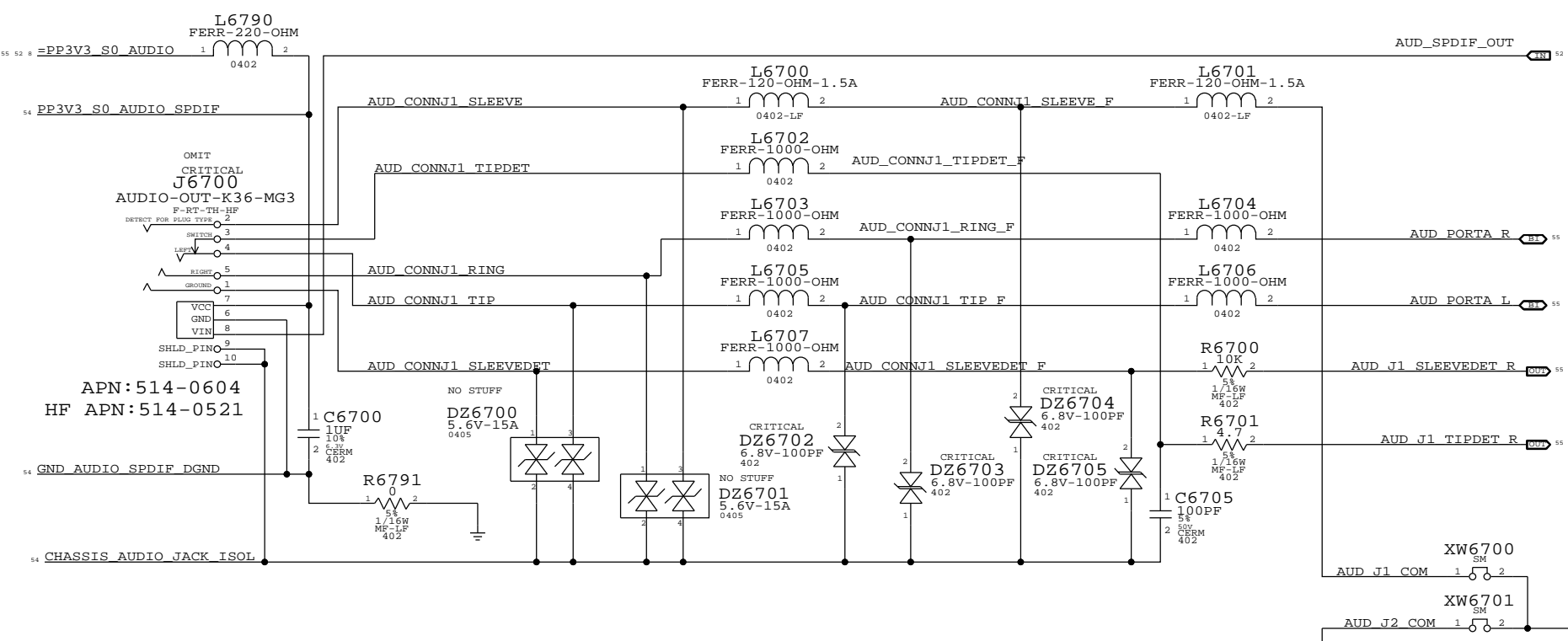
SUB-TWEETER

MIN_LINE_WIDTH=0.60 MM
 MIN_NECK_WIDTH=0.20 MM
 PP5V_S0_AUDIO_AMP SPKRAMP_THERMPLANE

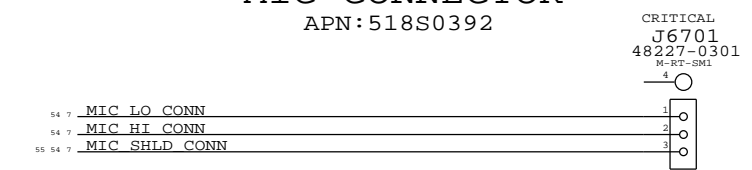
SYNC MASTER=K36A MLB SYNC DATE=08/29/2008

AUDIO: SPEAKER AMP	
Apple Inc.	051-8089 D
REVISION	A.0.0
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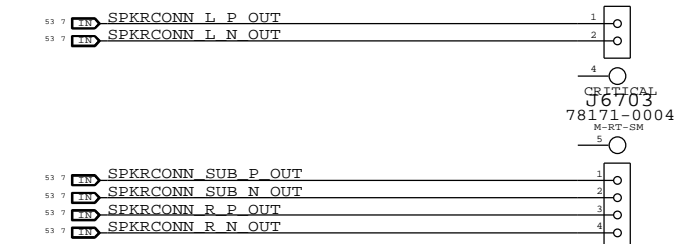
AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX



MIC CONNECTOR
APN:518S0392



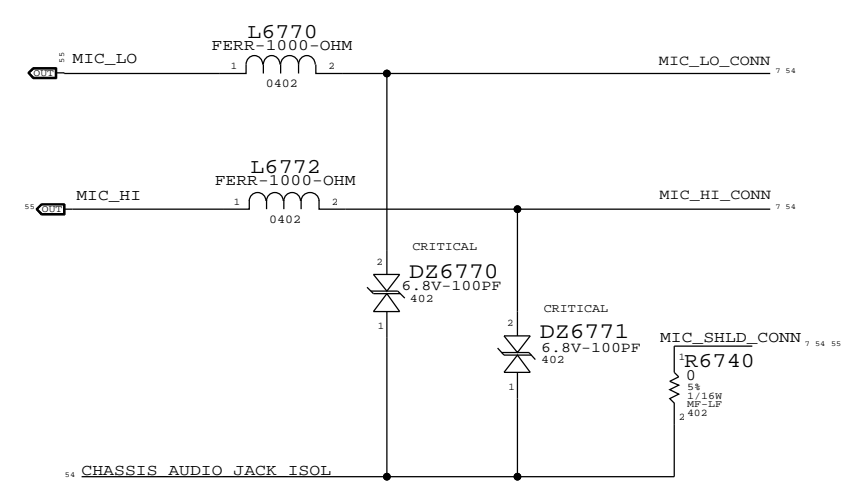
SPEAKER CONNECTOR
APN:518S0519



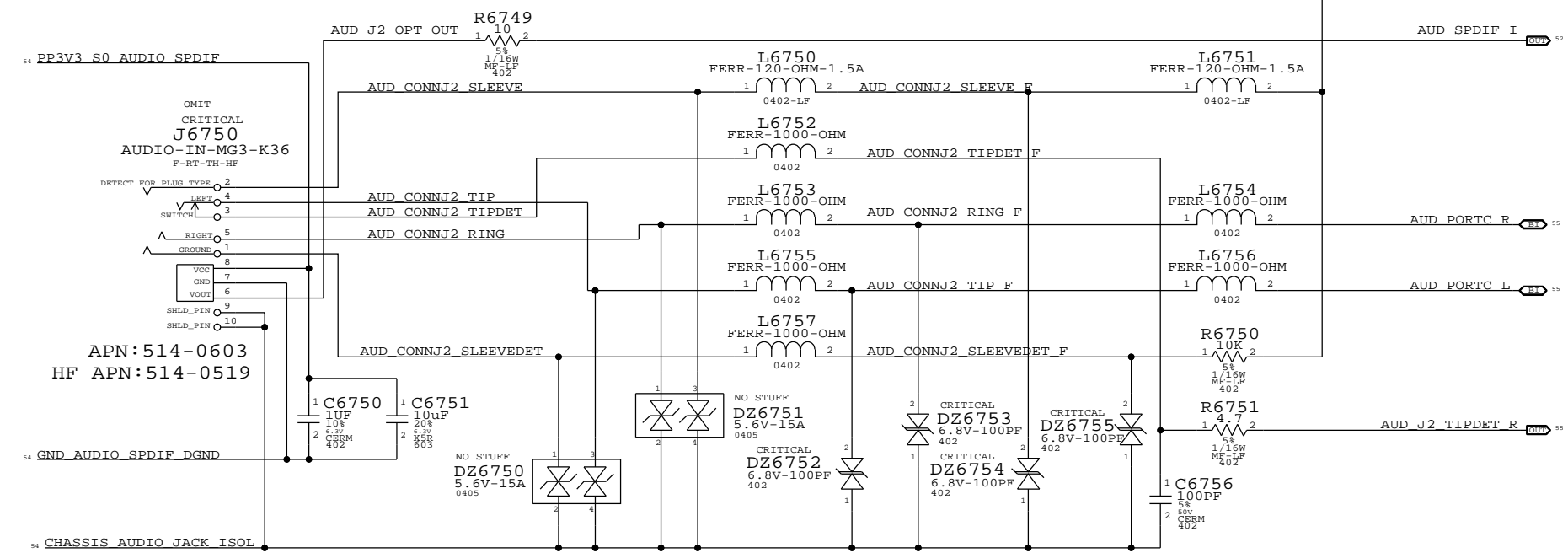
APN:518S0521

XW6705

MIC EMI FILTER



AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



SYNC MASTER=K36A MLB SYNC DATE=08/29/2008

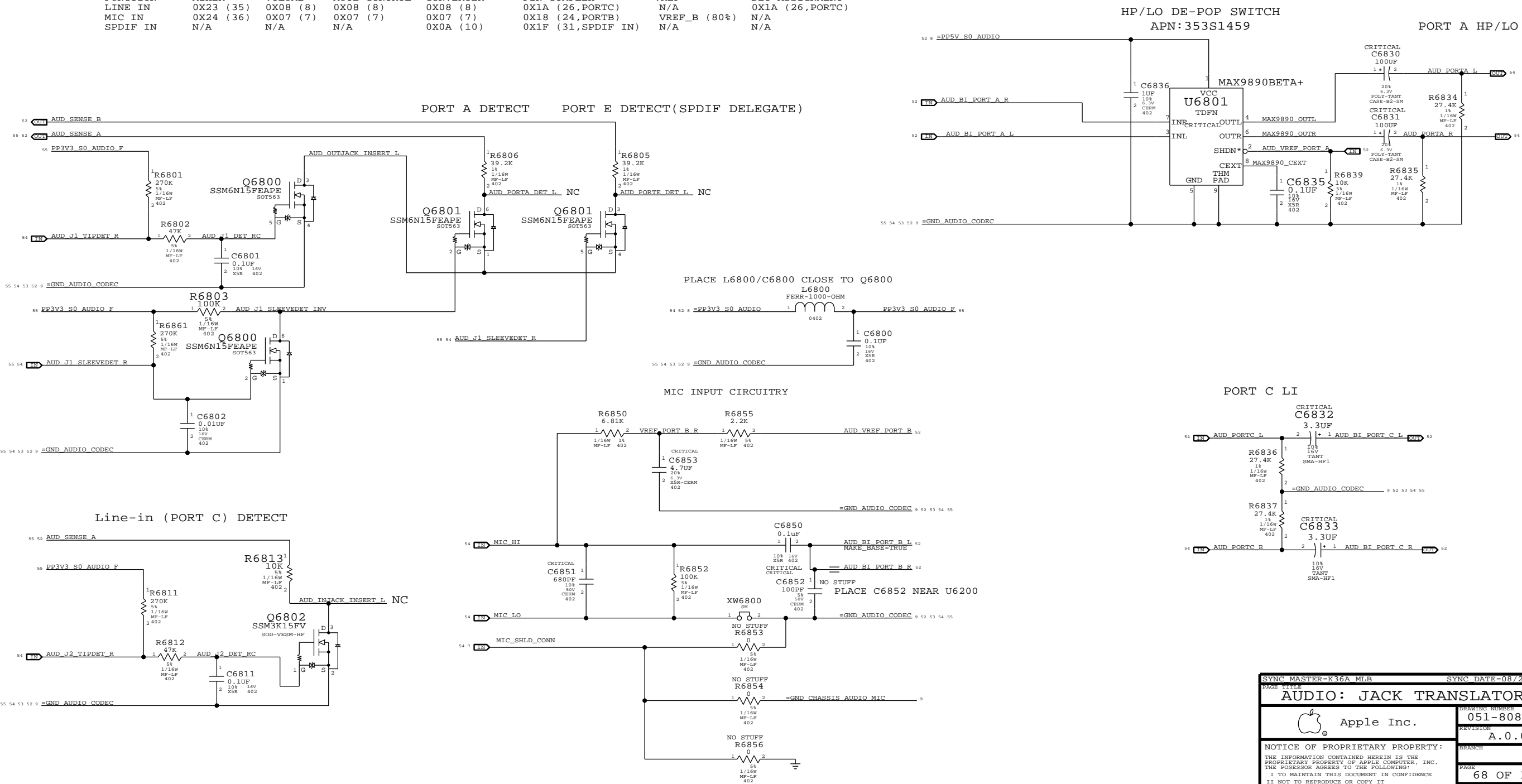
PAGE TITLE		AUDIO: JACK	
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A



SYNC MASTER=K36A MLB SYNC DATE=08/29/2008

AUDIO: JACK TRANSLATORS

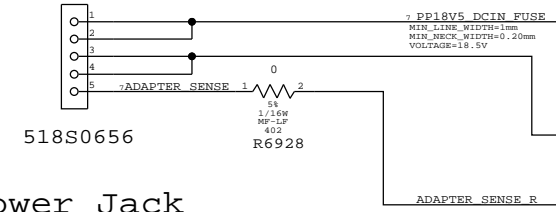
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PAGE	68 OF 109
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- COPY THIS PAGE FROM T18 CSA.69
- DO WE NEED TO CHANGE BATTERY CONNECTOR?

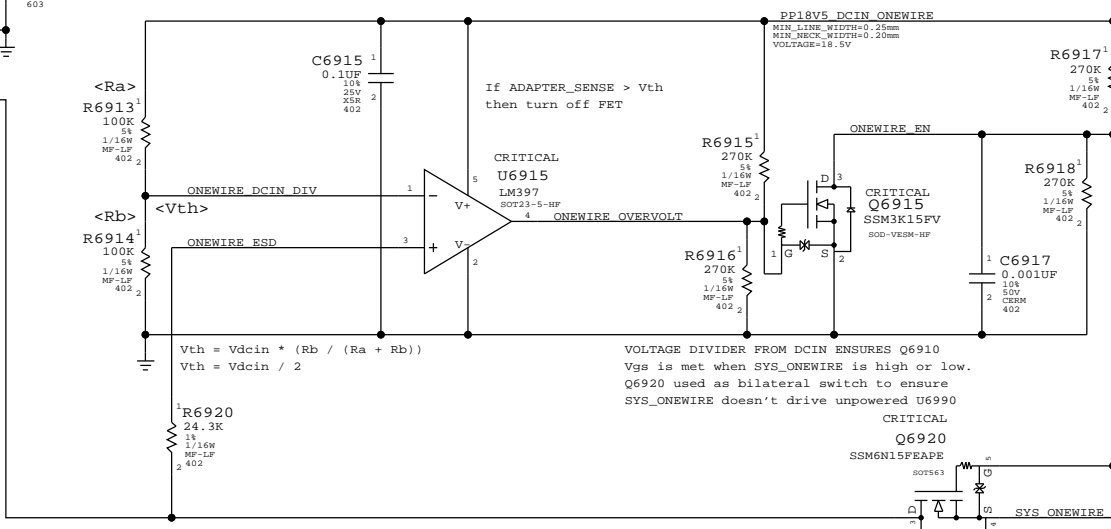
MagSafe DC Power Jack

CRITICAL
J6900
78048-0573
4-PT-SM



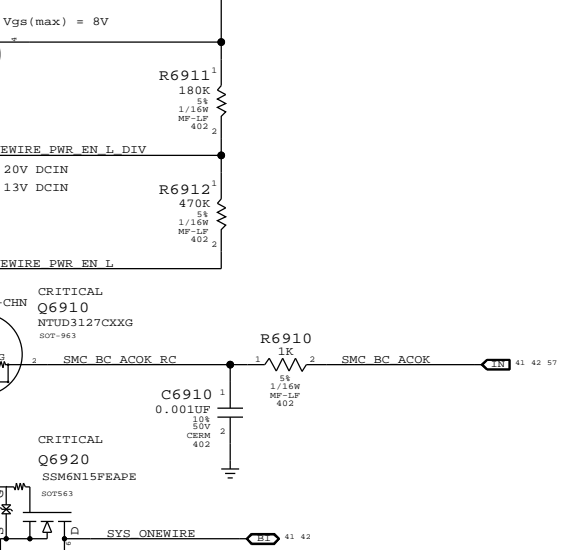
CRITICAL
F6905
6AMP-24V
1206

1-Wire OverVoltage Protection



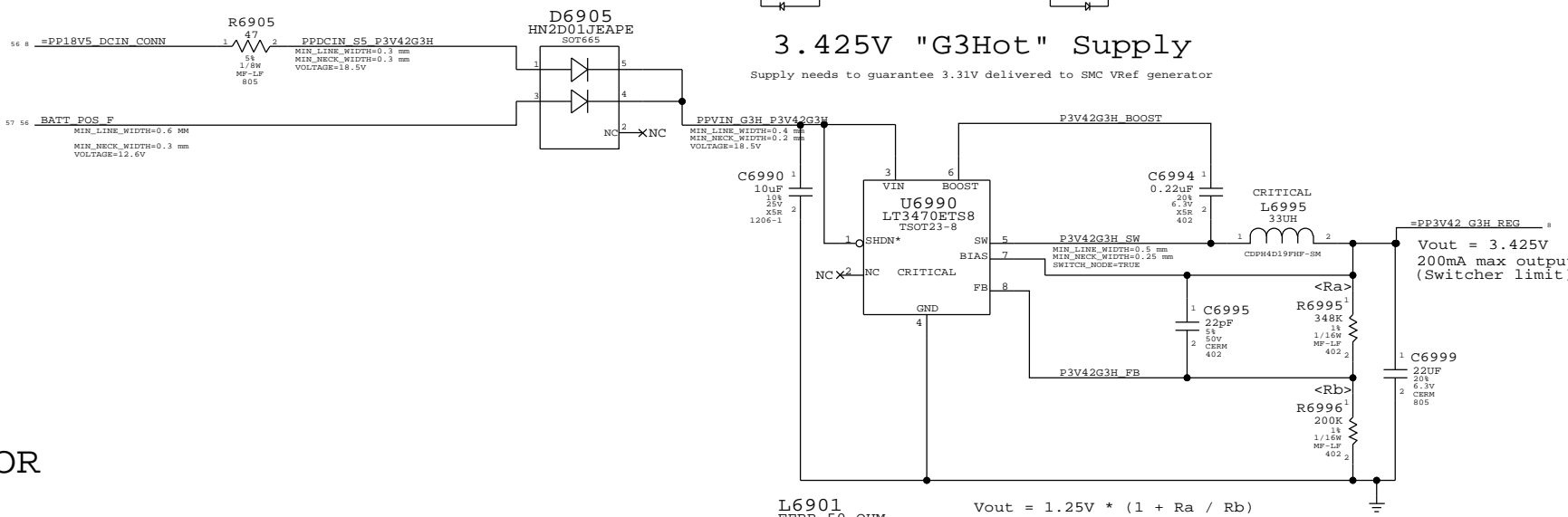
Q6910 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

CRITICAL
Q6910
NTUD3127CXXG
SOT-963

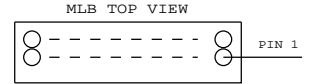


3.425V "G3Hot" Supply

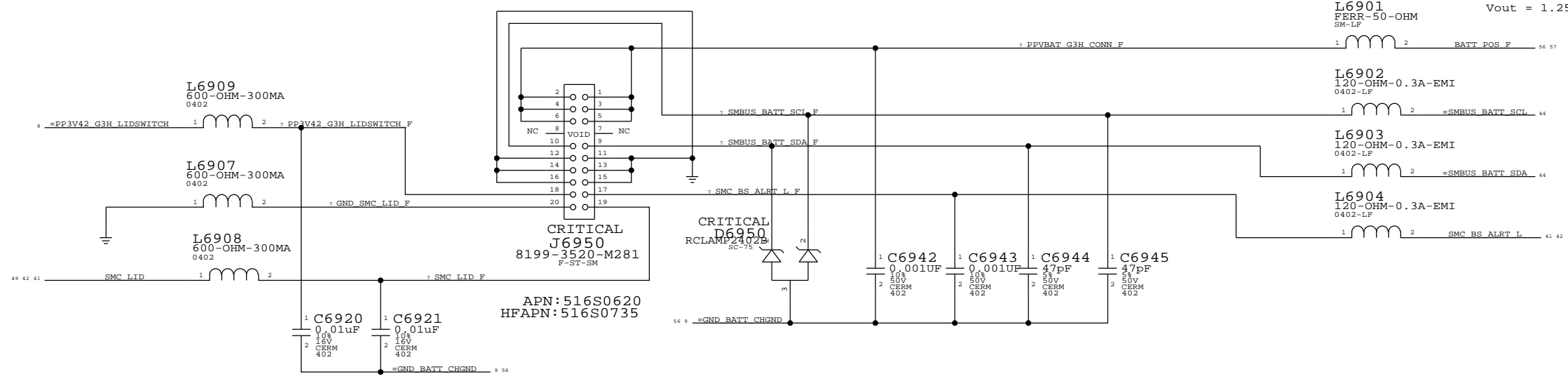
Supply needs to guarantee 3.31V delivered to SMC Vref generator



LID HALL EFFECT SENSOR

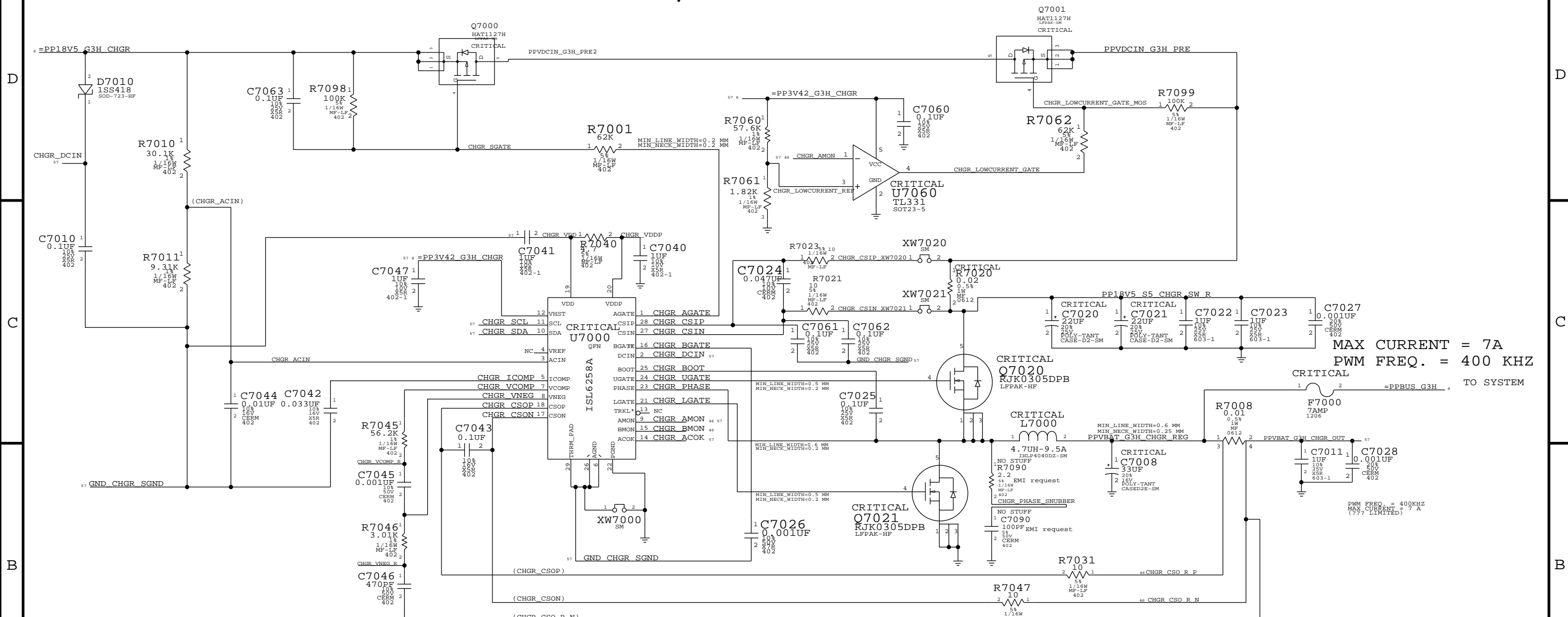


BATTERY/LID CONNECTOR



PAGE TITLE		SYNC DATE=08/17/2008	
DC-In & Battery Connectors			
Apple Inc.		DRAWING NUMBER	1122
		051-8089	D
		REVISION	A.0.0
		BRANCH	
		PAGE	69 OF 109
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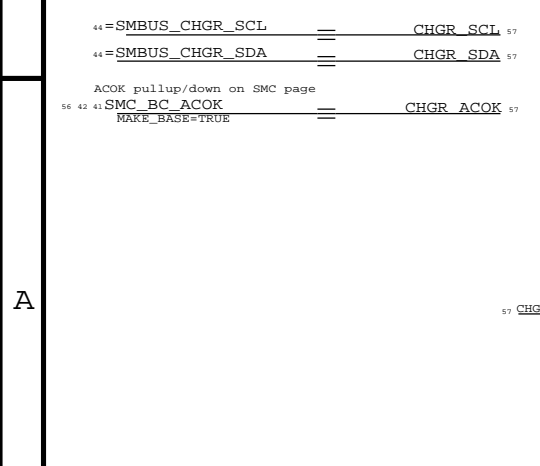
PBUS SUPPLY / BATTERY CHARGER



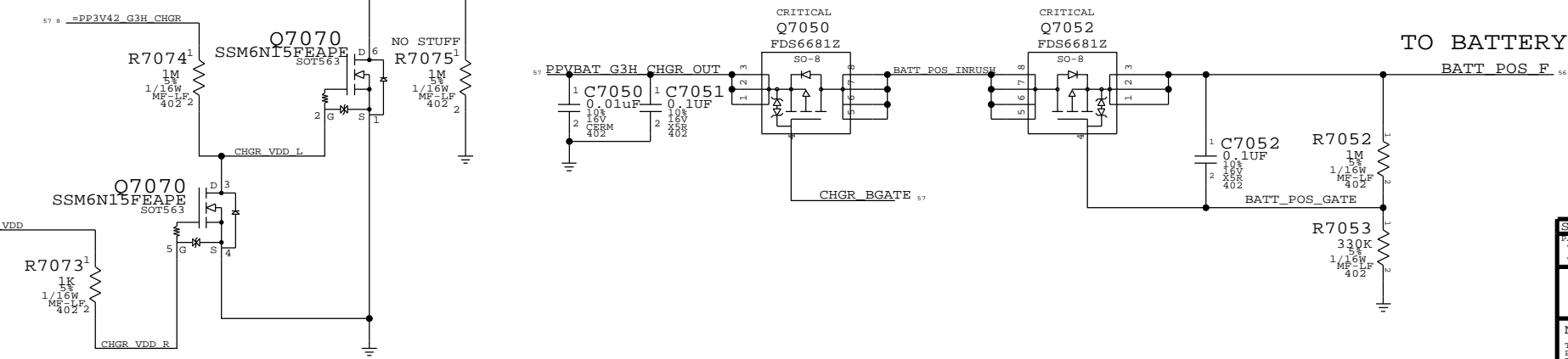
MAX CURRENT = 7A
PWM FREQ. = 400 KHZ

TO SYSTEM

AMON PULLDOWN LOGIC



BATTERY CHARGING



SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

PAGE TITLE: PBUS Supply/Battery Charger

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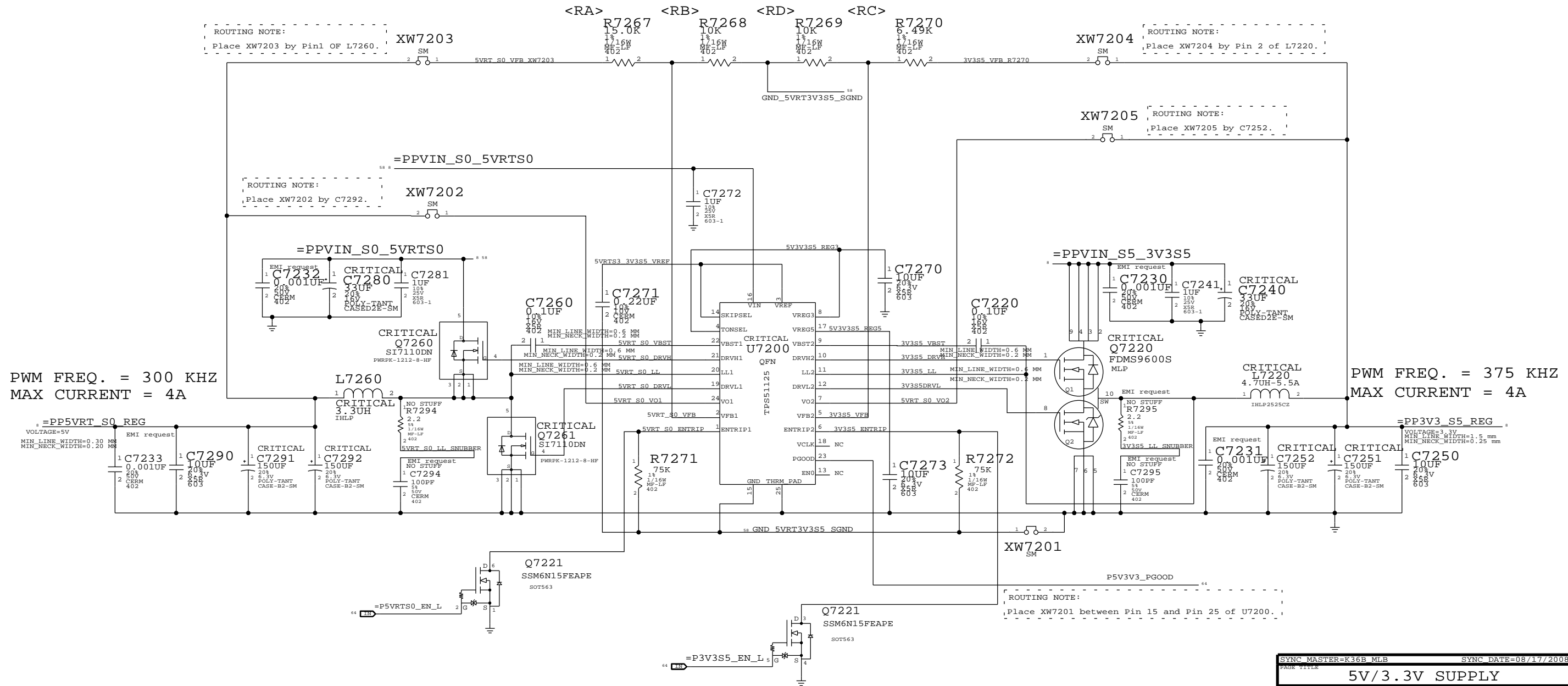
70 OF 109 SHEET

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5V_RT/3.3V POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

5V/3.3V SUPPLY

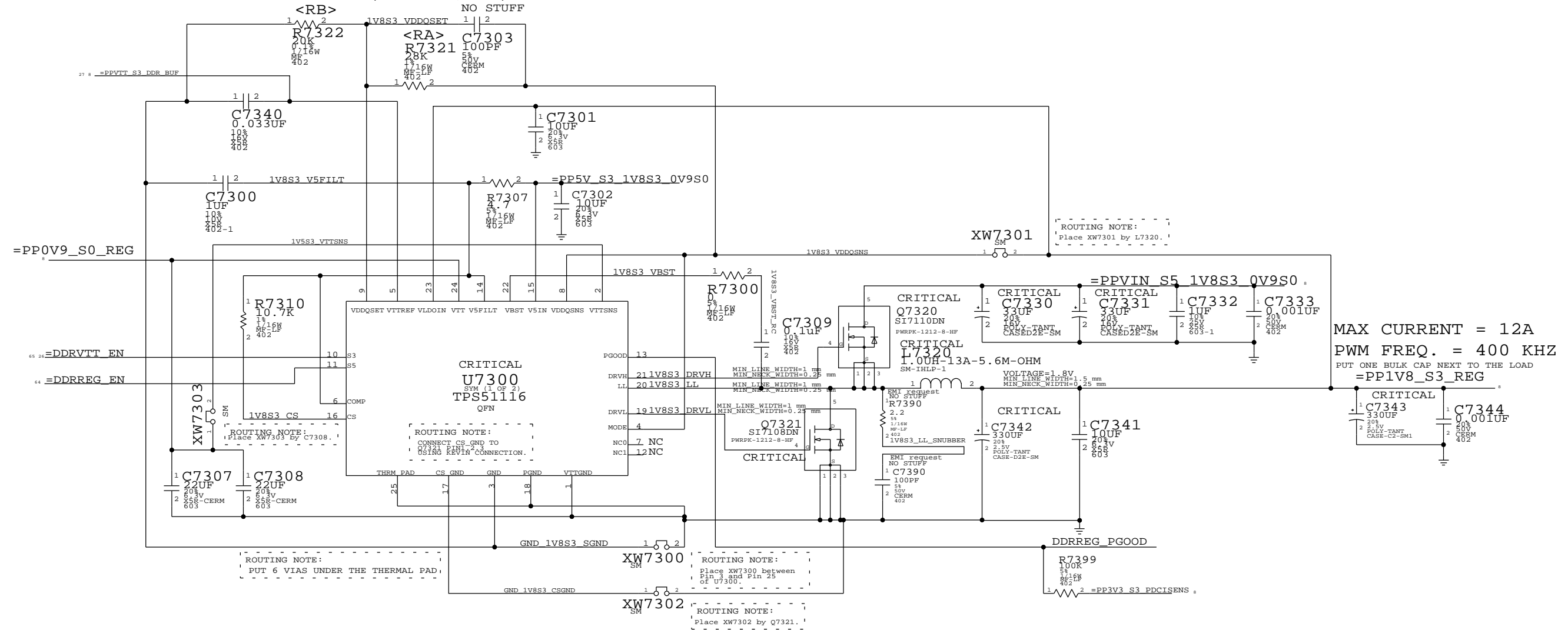
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1.8V/0.9V (DDR2) POWER SUPPLY

$$V_{OUT} = 0.75V * (1 + R_A / R_B)$$



MAX CURRENT = 12A
 PWM FREQ. = 400 KHZ
 PUT ONE BULK CAP NEXT TO THE LOAD
 =PP1V8_S3_REG

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

1.8V/0.9V DDR2 SUPPLY

Apple Inc.

051-8089 D

REVISION A.0.0

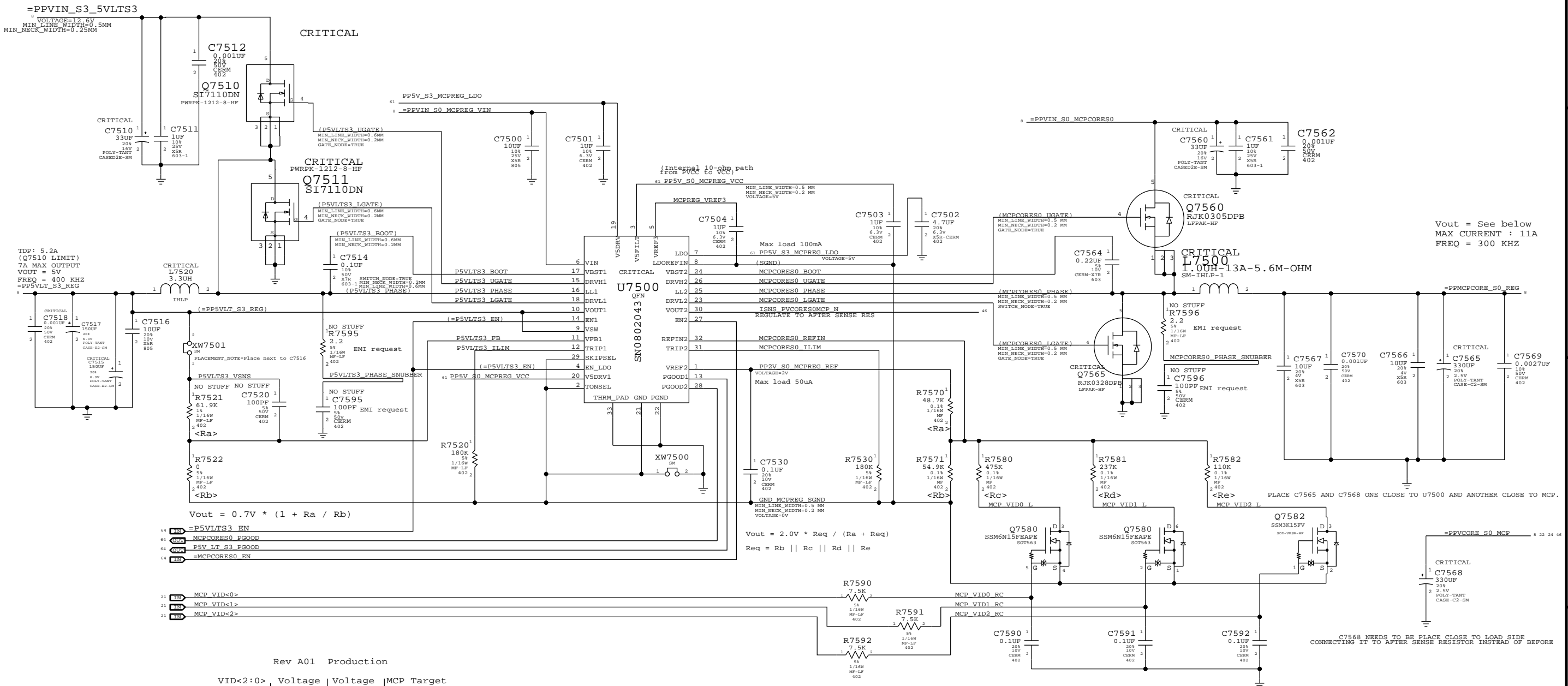
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MCP VCORE / 5V_S3 LEFT REGULATOR

- SYNC WITH T18
- COPY THIS PAGE FROM T18 CSA.75



Rev A01 Production

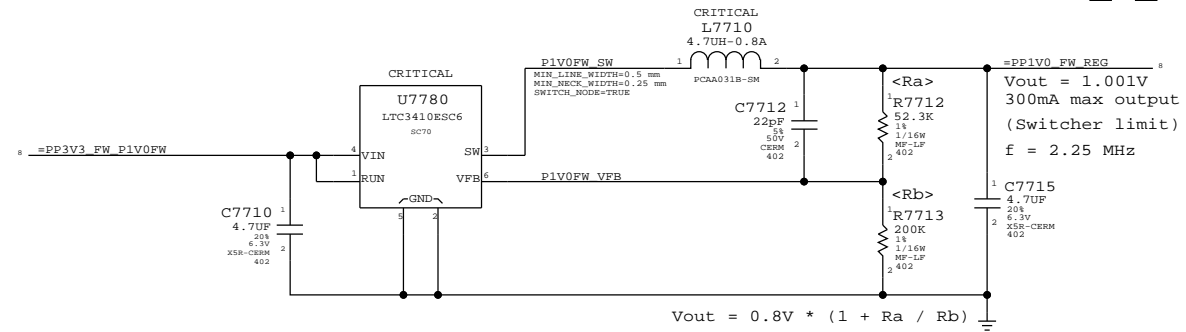
VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:
 Added C7568 bulk cap on output.
 Tied TON to REF.
 Changed Q7510 to 376S0674.
 C7500 changed to 138S0638.
 L7560 changed from T18 MLB inductor to 152S0782.
 Changed Q7565 to 376S0637.
 Changed R7514 to 280K, R7564 to 180K.

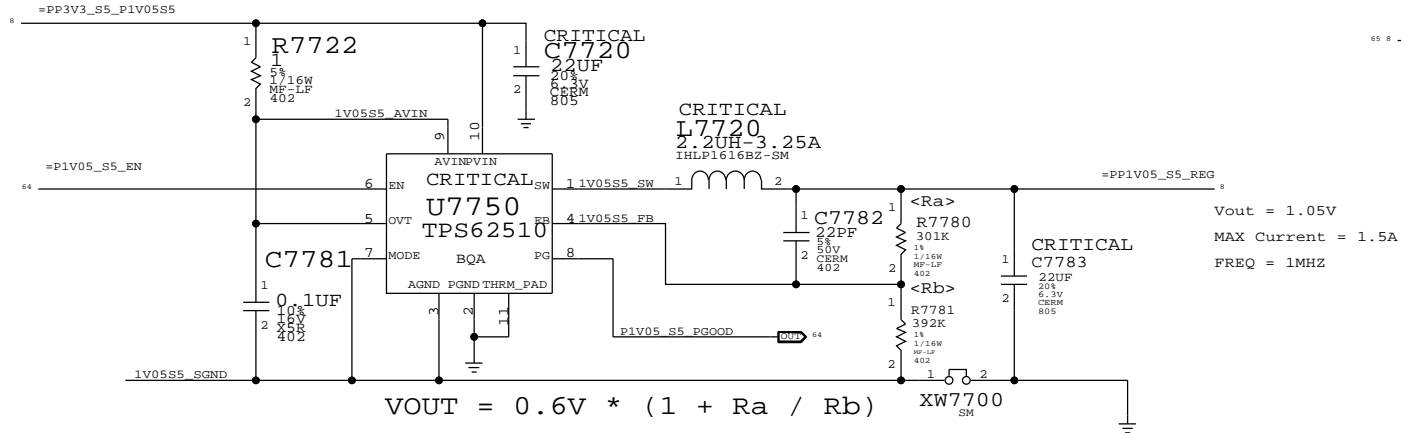
SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

MCP VCORE REGULATOR	
Apple Inc.	051-8089 D
REVISION	A.0.0
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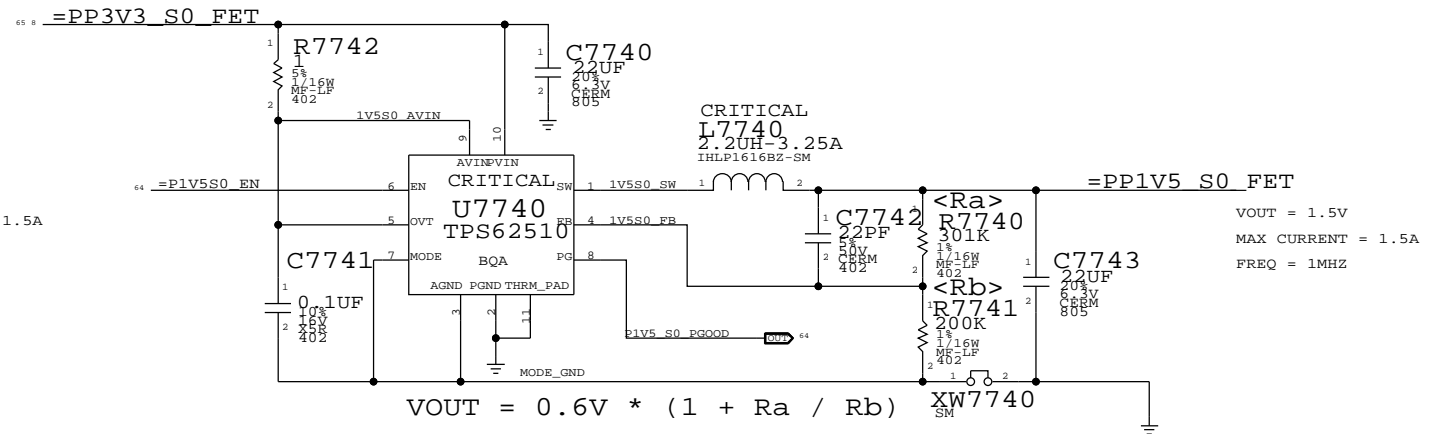
FireWire 1.0V (Core) Supply



MCP 1.05V_S5 AUXC SUPPLY



1.5V S0 SWITCH



SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
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MISC POWER SUPPLIES			
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D

C

B

A

D

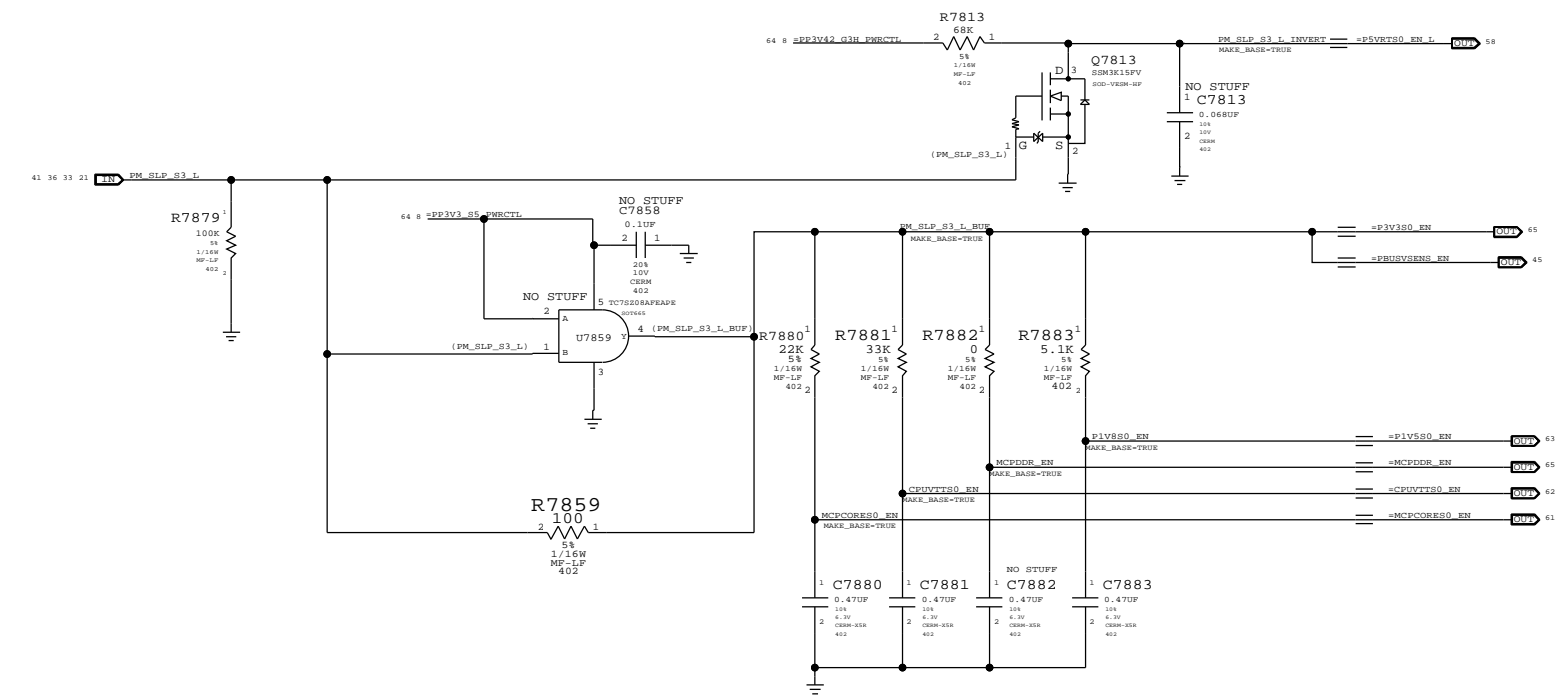
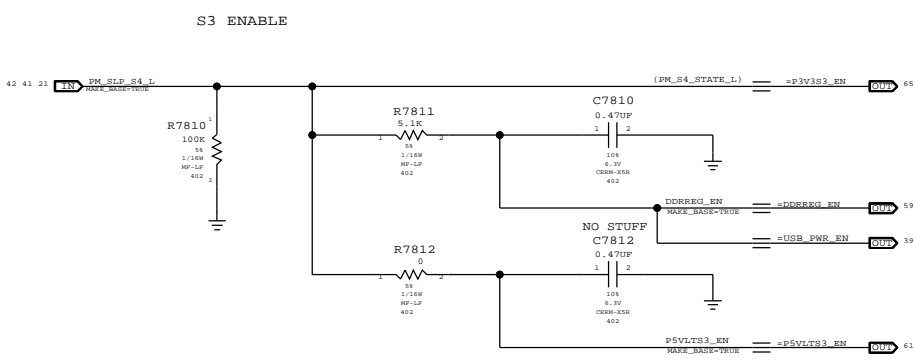
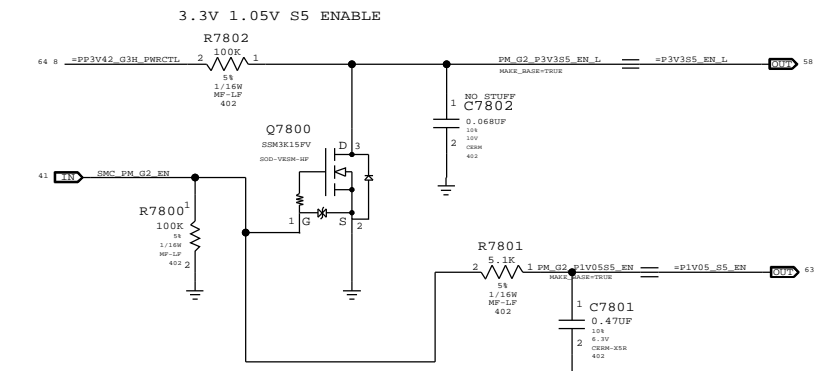
C

B

A

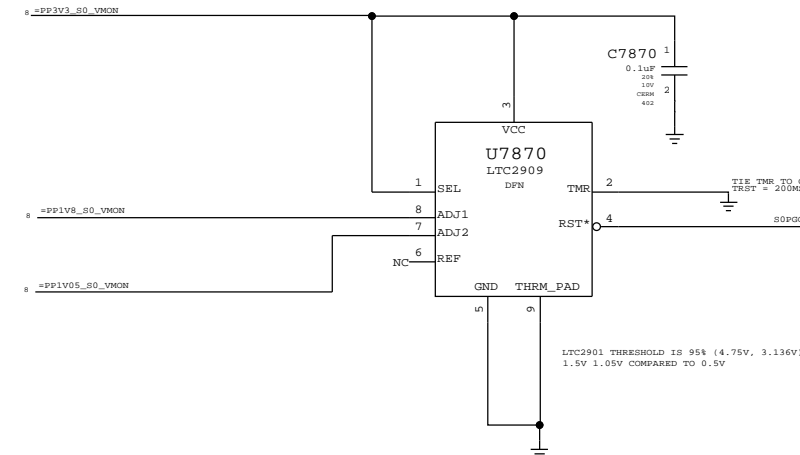
Power Control Signals

SVLT_S0, 3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT, MCPCORES0 ENABLE
1.5V_S0 AND 1.05V_S0 ENABLE

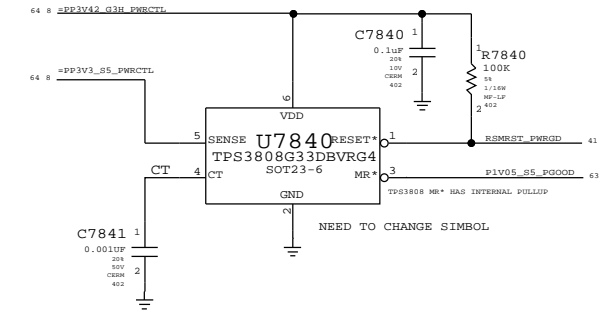
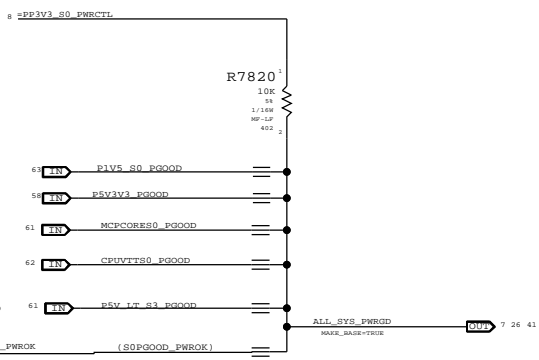


5.0V (RIGHT AND LEFT), 3.3V AND 1.5V S0 RAILS MONITOR CIRCUIT

LAYOUT_NOTE: ADD XW IF NEEDS TO SAVE SPACE FOR PIN2,10,1,9



OTHER S0 RAILS PGOOD



Unused PGOOD signal

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

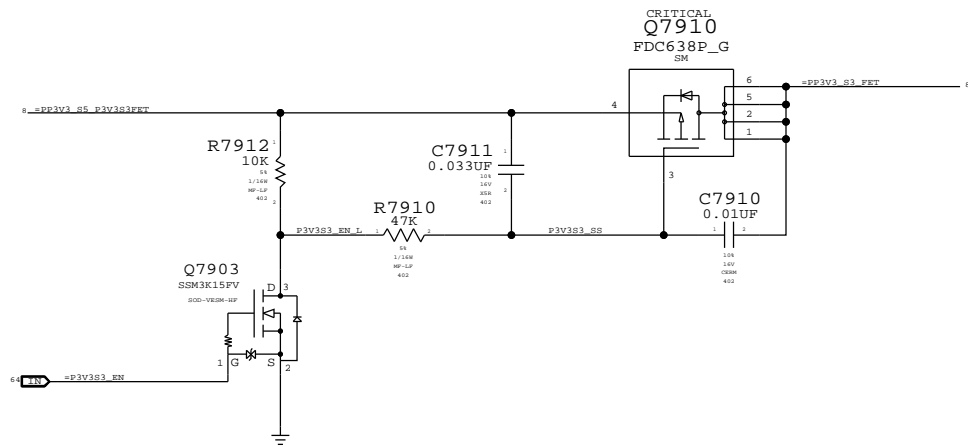
POWER SEQUENCING

Apple Inc.		DESIGN NUMBER	051-8089
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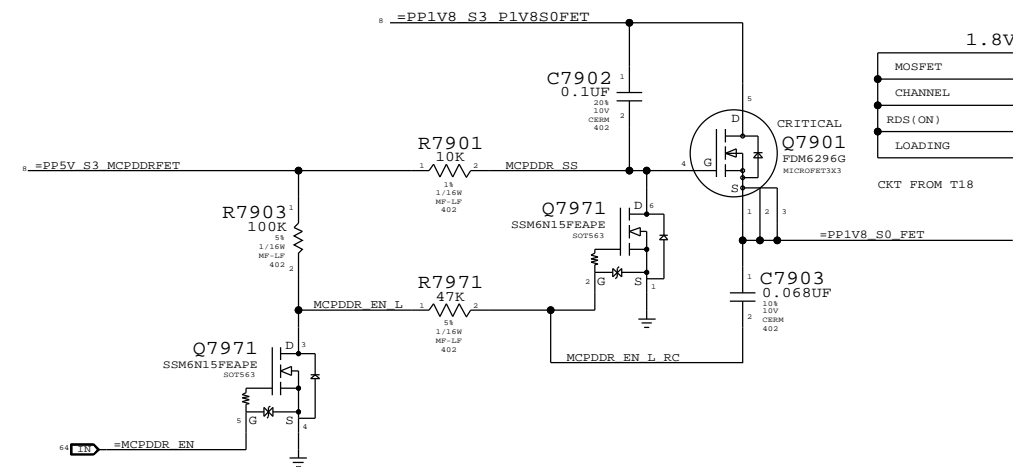
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3.3V S3 FET



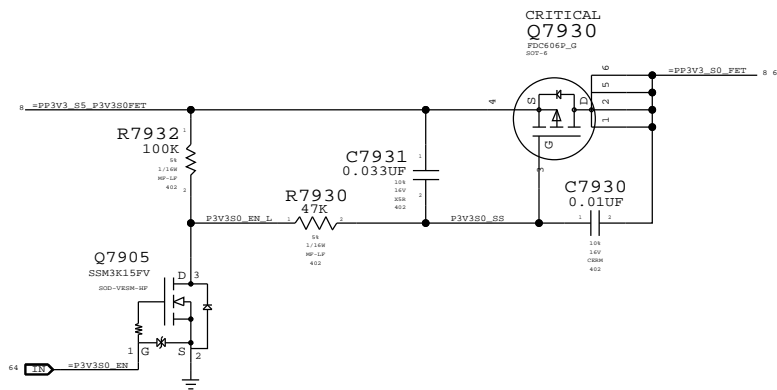
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

1.8V S0 FET
(1.8V S0 FET FOR DDR2 MEM)



MOSFET	FDM6296G
CHANNEL	N-TYPE
RDS(ON)	15 MOHM @4.5V VGS
LOADING	5A (EDP)

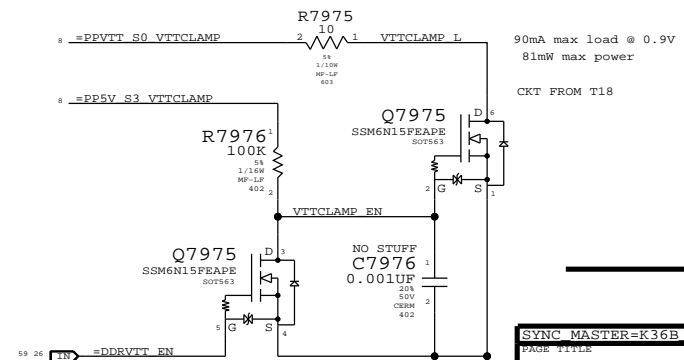
3.3V S0 FET



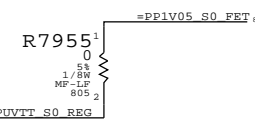
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

MCP79 DDRVTT FET

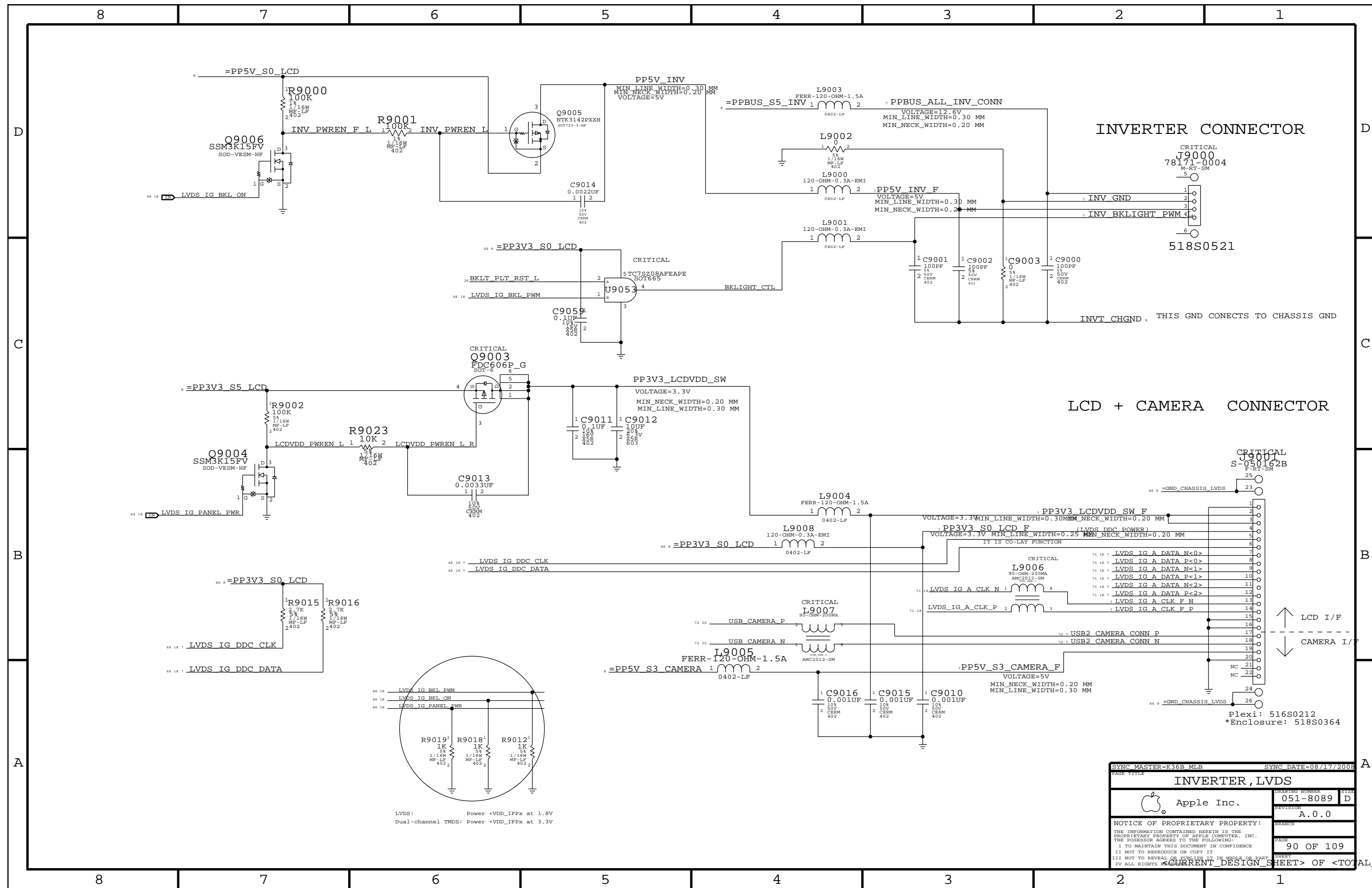
MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



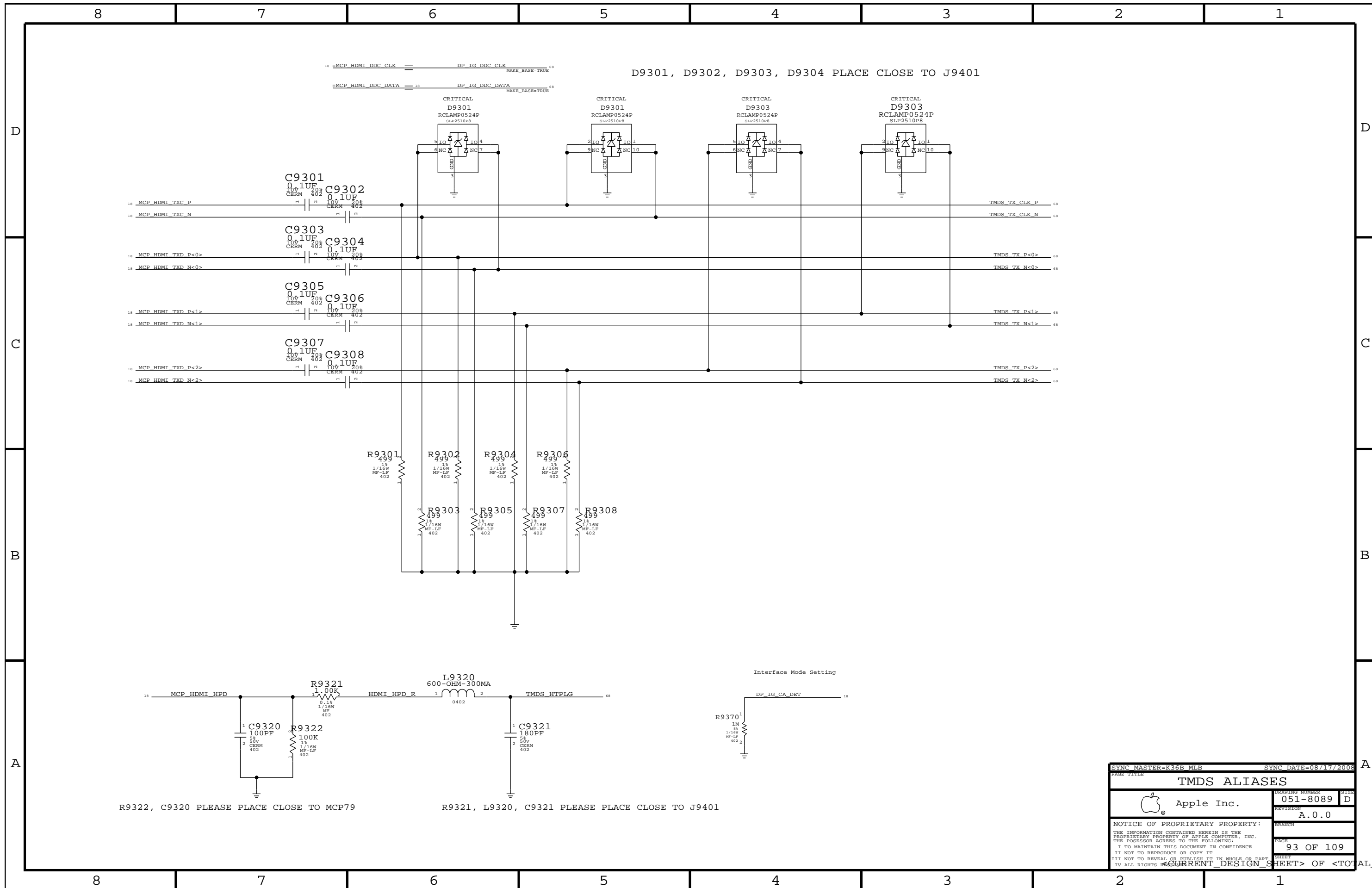
90mA max load @ 0.9V
81mW max power
CKT FROM T18



PAGE TITLE		SYNC DATE=08/17/2008	
POWER FETS		051-8089	D
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SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
INVERTER, LVDS			
Apple Inc.		DRAWING NUMBER	SIZE
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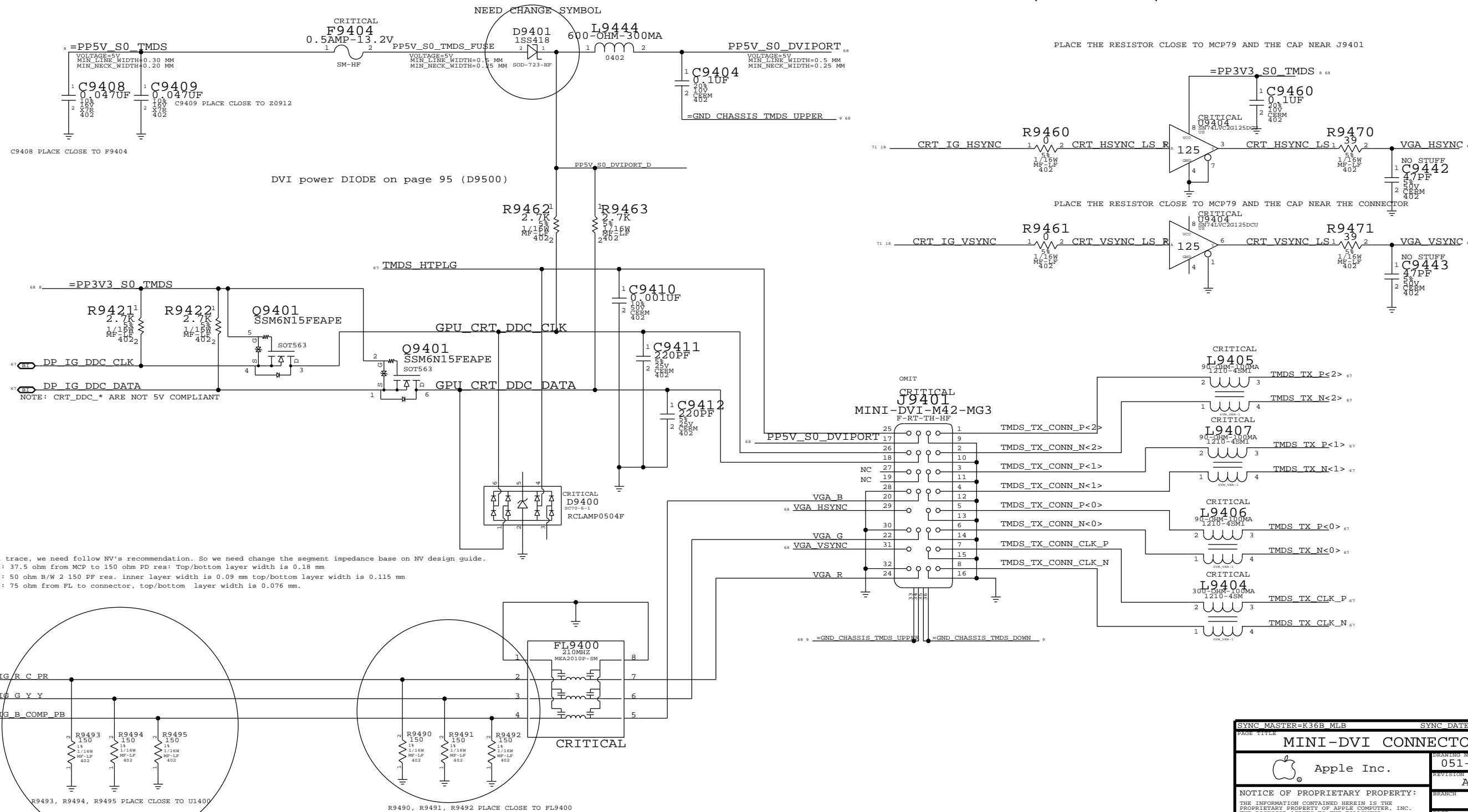
PAGE TITLE		SYNC DATE=08/17/2008	
TMD5 ALIASES			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8089	D
		REVISION	
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		PAGE	
		93 OF 109	
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Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

TMDS (MINI DVI) INTERFACE



for VG signal trace, we need follow NV's recommendation. So we need change the segment impedance base on NV design guide.
 for A segment: 37.5 ohm from MCP to 150 ohm PD res; Top/bottom layer width is 0.18 mm
 for B segment: 50 ohm B/W 2 150 PF res; inner layer width is 0.09 mm top/bottom layer width is 0.115 mm
 for C segment: 75 ohm from FL to connector, top/bottom layer width is 0.076 mm.

SYNC MASTER=K36B MLB		SYNC DATE=08/17/2008	
PAGE TITLE			
MINI-DVI CONNECTOR			
Apple Inc.		CREATION NUMBER	051-8089 D
		REVISION	A.0.0
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFPPAIR	=1:1_DIFPPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2k_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4k_DIELECTRIC	?
FSB_DSTB	*	=3k_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5k_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3k_DIELECTRIC	?
FSB_ADSTB	*	=2k_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4k_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3k_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
 Signals within each 4x group should be matched within 5 ps of strobe.
 DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
 Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
 DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
 Signals within each 2x group should be matched within 20 ps. ADTSTB#s should be matched +/- 300 ps.
 Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSTB#.

FSB 1X signals shown in signal table on right.
 Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
 Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
 SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2k_DIELECTRIC	?
CPU_BMIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
 Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
 SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3k_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4k_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10 14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	10 14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	10 14
FSB_BREQ0	FSB_50S	FSB_1X	FSB BREQ0 L	10 14
FSB_BREQ1	FSB_50S	FSB_1X	FSB BREQ1 L	14
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	10 14
FSB_CPURST	FSB_50S	FSB_1X	FSB CPURST L	10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10 14
CPU_ASYM	CPU_50S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR	CPU_50S	CPU_BMIL	CPU FERR L	10 14
CPU_ASYM	CPU_50S	CPU_AGTL	CPU IGNE L	10 14
CPU_INIT	CPU_50S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYM	CPU_50S	CPU_AGTL	CPU INTR	10 14
CPU_ASYM	CPU_50S	CPU_AGTL	CPU NMI	10 14
CPU_PROCHOT	CPU_50S	CPU_AGTL	CPU PROCHOT L	10 14 42 60
CPU_PERR0	CPU_50S	CPU_AGTL	CPU PWRGD	10 13 14
CPU_ASYM	CPU_50S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYM	CPU_50S	CPU_AGTL	CPU STPCLK L	10 14
PM_THRMTRIP	CPU_50S	CPU_BMIL	PM THRMTRIP L	10 14 42
FSB_CPUSLP	CPU_50S	CPU_AGTL	FSB CPUSLP L	10 14
CPU_FERR	CPU_50S	CPU_AGTL	CPU DESLP L	10 14
CPU_DPRSTP	CPU_50S	CPU_AGTL	CPU DPRSTP L	10 14 60
CPU_ASYM	CPU_50S	CPU_AGTL	FSB DPNR L	10 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	7 13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	7 13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR	CPU_50S		CPU IERR L	10
PM DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	21 60
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	60
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 27
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_50S	CPU_STP	XDP TDI	6 7 10 13
XDP_TDO	CPU_50S	CPU_STP	XDP TDO	6 10
XDP_TMS	CPU_50S	CPU_STP	XDP TMS	6 7 10 13
XDP_TCK	CPU_50S	CPU_STP	XDP TCK	6 7 10 13
XDP_TRST	CPU_50S	CPU_STP	XDP TRST L	6 7 10 13
XDP_BPM	CPU_50S	CPU_STP	XDP BPM L<4..0>	7 10 13
XDP_BPM	CPU_50S	CPU_STP	XDP BPM L<5>	7 10 13
(FSB_CPURST L)	CPU_50S	CPU_STP	XDP CPURST L	7 13
	CPU_50S	CPU_BMIL	CPU VID<6..0>	11 60
	CPU_50S	CPU_BMIL	IMVP6 VID<6..0>	11 60
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 60
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 60
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SR	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SR	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DATA	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER

Need to support MEM*-style wildcards!

DDR2:
 DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_TYPE	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK N<5..0>	15 28
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28 30
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM_A_CS L<3..0>	15 28 30
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A A<14..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A BA<2..0>	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A RAS L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A CAS L	15 28 30
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A WE L	15 28 30
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<7..0>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<15..8>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<23..16>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<31..24>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<39..32>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<47..40>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<55..48>	15 28
MEM_A_DQ	MEM_40S	MEM_DATA	MEM_A DQ<63..56>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<0>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<1>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<2>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<3>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<4>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<5>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<6>	15 28
MEM_A_DM	MEM_40S	MEM_DATA	MEM_A DM<7>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<0>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<0>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<1>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<1>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<2>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<2>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<3>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<3>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<4>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<4>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<5>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<5>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<6>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<6>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS P<7>	15 28
MEM_A_DQS	MEM_70D	MEM_DQS	MEM_A DQS N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK N<5..0>	15 29
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29 30
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM_B_CS L<3..0>	15 29 30
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B A<14..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B BA<2..0>	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B RAS L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B CAS L	15 29 30
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B WE L	15 29 30
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<7..0>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<15..8>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<23..16>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<31..24>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<39..32>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<47..40>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<55..48>	15 29
MEM_B_DQ	MEM_40S	MEM_DATA	MEM_B DQ<63..56>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<0>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<1>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<2>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<3>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<4>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<5>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<6>	15 29
MEM_B_DM	MEM_40S	MEM_DATA	MEM_B DM<7>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<0>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<0>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<1>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<1>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<2>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<2>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<3>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<3>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<4>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<4>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<5>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<5>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<6>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<6>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS P<7>	15 29
MEM_B_DQS	MEM_70D	MEM_DQS	MEM_B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_GND	16

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

Memory Constraints	
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A.0.0	
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	*	=3X_DIELECTRIC	?	PCI_E	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCI_E	*	20 MIL	?				
MCP_PEX_COMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	*	=4:1_SPACING	?	CRT	CRT	*	CRT_2CRT
CRT_2CRT	*	=STANDARD	?				
CRT_2CLK	*	50 MIL	?				
CRT_2SWITCHER	*	250 MIL	?				
CRT_SYNC	*	16 MIL	?				
MCP_DAC_COMP	*	=2:1_SPACING	?				

CRT signal single-ended impedance varies by location:
 - 37.5-ohm from MCP to first termination resistor.
 - 50-ohm from first to second termination resistor.
 - 75-ohm from output of three-pole filter to connector (if possible).
 R/G/B signals should be matched as close as possible and < 10 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?	SATA	TOP,BOTTOM	=3X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCI_E_90D	PCI_E	PEG R2D P<15..0>
	PCI_E_90D	PCI_E	PEG R2D N<15..0>
	PCI_E_90D	PCI_E	PEG R2D C P<15..0>
	PCI_E_90D	PCI_E	PEG R2D C N<15..0>
	PCI_E_90D	PCI_E	PEG D2R P<15..0>
	PCI_E_90D	PCI_E	PEG D2R N<15..0>
	PCI_E_90D	PCI_E	PEG D2R C P<15..0>
	PCI_E_90D	PCI_E	PEG D2R C N<15..0>
	PCI_E_90D	PCI_E	PCI_E MINI R2D P
	PCI_E_90D	PCI_E	PCI_E MINI R2D N
	PCI_E_90D	PCI_E	PCI_E MINI R2D C P
	PCI_E_90D	PCI_E	PCI_E MINI R2D C N
	PCI_E_90D	PCI_E	PCI_E MINI D2R P
	PCI_E_90D	PCI_E	PCI_E MINI D2R N
	PCI_E_90D	PCI_E	PCI_E FW R2D P
	PCI_E_90D	PCI_E	PCI_E FW R2D N
	PCI_E_90D	PCI_E	PCI_E FW R2D C P
	PCI_E_90D	PCI_E	PCI_E FW R2D C N
	PCI_E_90D	PCI_E	PCI_E FW D2R P
	PCI_E_90D	PCI_E	PCI_E FW D2R N
	PCI_E_90D	PCI_E	PCI_E FW D2R C P
	PCI_E_90D	PCI_E	PCI_E FW D2R C N
	PCI_E_90D	PCI_E	PCI_E EXCARD R2D P
	PCI_E_90D	PCI_E	PCI_E EXCARD R2D N
	PCI_E_90D	PCI_E	PCI_E EXCARD R2D C P
	PCI_E_90D	PCI_E	PCI_E EXCARD R2D C N
	PCI_E_90D	PCI_E	PCI_E EXCARD D2R P
	PCI_E_90D	PCI_E	PCI_E EXCARD D2R N
	CLK_PCI_E_100D	CLK_PCI_E	PEG CLK100M P
	CLK_PCI_E_100D	CLK_PCI_E	PEG CLK100M N
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI P
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI N
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M FW P
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M FW N
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M EXCARD P
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M EXCARD N
	MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP PEX CLK COMP
	CRT_RED	CRT_MCP_E	CRT IG R C PR
	CRT_GREEN	CRT_MCP_E	CRT IG G Y Y
	CRT_BLUE	CRT_MCP_E	CRT IG B COMP PB
	CRT_SYNC	CRT_50S	CRT IG HSYNC
	CRT_SYNC	CRT_50S	CRT IG VSYNC
	MCP_DAC_RSET	MCP_DAC_COMP	MCP TV DAC RSET
	MCP_DAC_VREF	MCP_DAC_COMP	MCP TV DAC VREF
	TMDS_IG_TXC	DISPLAYPORT	TMDS IG TXC P
	TMDS_IG_TXC	DISPLAYPORT	TMDS IG TXC N
	TMDS_IG_TXD	DISPLAYPORT	TMDS IG TXD P<2..0>
	TMDS_IG_TXD	DISPLAYPORT	TMDS IG TXD N<2..0>
	DP_ML	DISPLAYPORT	DP IG ML P<3..0>
	DP_ML	DISPLAYPORT	DP IG ML N<3..0>
	DP_AUX_CH	DISPLAYPORT	TP DP IG AUX CH P
	DP_AUX_CH	DISPLAYPORT	TP DP IG AUX CH N
	MCP_HDMI_RSET	MCP_DV_COMP	MCP HDMI RSET
	MCP_HDMI_VPROBE	MCP_DV_COMP	MCP HDMI VPROBE
	LVDS_IG_A_CLK	LVDS_100D	LVDS IG A CLK P
	LVDS_IG_A_CLK	LVDS_100D	LVDS IG A CLK N
	LVDS_IG_A_DATA	LVDS_100D	LVDS IG A DATA P<2..0>
	LVDS_IG_A_DATA	LVDS_100D	LVDS IG A DATA N<2..0>
	LVDS_IG_A_DATA1	LVDS_100D	LVDS IG A DATA P<3>
	LVDS_IG_A_DATA1	LVDS_100D	LVDS IG A DATA N<3>
	LVDS_IG_B_CLK	LVDS_100D	LVDS IG B CLK P
	LVDS_IG_B_CLK	LVDS_100D	LVDS IG B CLK N
	LVDS_IG_B_DATA	LVDS_100D	LVDS IG B DATA P<2..0>
	LVDS_IG_B_DATA	LVDS_100D	LVDS IG B DATA N<2..0>
	LVDS_IG_B_DATA1	LVDS_100D	LVDS IG B DATA P<3>
	LVDS_IG_B_DATA1	LVDS_100D	LVDS IG B DATA N<3>
	MCP_IFPAB_RSET	MCP_DV_COMP	MCP IFPAB RSET
	MCP_IFPAB_VPROBE	MCP_DV_COMP	MCP IFPAB VPROBE
	SATA_HDD_R2D	SATA_100D_HDD	SATA HDD R2D C P
	SATA_HDD_R2D	SATA_100D_HDD	SATA HDD R2D C N
	SATA_HDD_R2D	SATA_100D_HDD	SATA HDD R2D P
	SATA_HDD_R2D	SATA_100D_HDD	SATA HDD R2D N
	SATA_HDD_R2D	SATA_100D_HDD	SATA HDD R2D UF P
	SATA_HDD_R2D	SATA_100D_HDD	SATA HDD R2D UF N
	SATA_HDD_D2R	SATA_100D_HDD	SATA HDD D2R P
	SATA_HDD_D2R	SATA_100D_HDD	SATA HDD D2R N
	SATA_HDD_D2R	SATA_100D_HDD	SATA HDD D2R C P
	SATA_HDD_D2R	SATA_100D_HDD	SATA HDD D2R C N
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D C P
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D C N
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D P
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D N
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D UF P
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D UF N
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R P
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R N
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R C P
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R C N
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R UF P
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R UF N
	MCP_SATA_TERM	SATA_TERM	MCP SATA TERM

SYNC MASTER=K36B MLB SYNC DATE=08/17/2008

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	7 13 19
PCI_AD	PCI_55S	PCI	PCI AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI AD<24>	
PCI_AD	PCI_55S	PCI	PCI AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	
PCI_CBE_L	PCI_55S	PCI	PCI IRDY L	
PCI_CBE_L	PCI_55S	PCI	PCI DEVSEL L	
PCI_CBE_L	PCI_55S	PCI	PCI PERR L	
PCI_CBE_L	PCI_55S	PCI	PCI SERR L	
PCI_CBE_L	PCI_55S	PCI	PCI STOP L	
PCI_CBE_L	PCI_55S	PCI	PCI TRDY L	
PCI_CBE_L	PCI_55S	PCI	PCI FRAME L	
PCI_REQ0_L	PCI_55S	PCI	PCI REQ0 L	19
PCI_REQ0_L	PCI_55S	PCI	PCI GNT0 L	
PCI_REQ0_L	PCI_55S	PCI	PCI REQ1 L	19
PCI_REQ1_L	PCI_55S	PCI	PCI GNT1 L	
PCI_INTW_L	PCI_55S	PCI	PCI INTW L	
PCI_INTW_L	PCI_55S	PCI	PCI INTX L	
PCI_INTX_L	PCI_55S	PCI	PCI INTY L	
PCI_INTY_L	PCI_55S	PCI	PCI INTZ L	
MCP_PCI_CLK2	CLK PCI_55S	CLK PCI	PCI CLK33M MCP R	19
MCP_PCI_CLK2	CLK PCI_55S	CLK PCI	PCI CLK33M MCP	19
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 41 43
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 41 43
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 26
MCP_LPC_CLK	CLK LPC_55S	CLK LPC	LPC CLK33M SMC R	19 26
MCP_LPC_CLK	CLK LPC_55S	CLK LPC	LPC CLK33M SMC	26 41
MCP_LPC_CLK	CLK LPC_55S	CLK LPC	LPC CLK33M LCPPLUS	7 26 43
USB_EXTN	USB_90D	USB	USB EXTN P	20 39
USB_EXTN	USB_90D	USB	USB EXTN N	20 39
USB_EXTN	USB_90D	USB	USB2_EXTN_MUXED_P	39
USB_EXTN	USB_90D	USB	USB2_EXTN_MUXED_N	39
USB_EXTN	USB_90D	USB	USB2_EXTN_F_P	39
USB_EXTN	USB_90D	USB	USB2_EXTN_F_N	39
USB_MINI	USB_90D	USB	USB MINI P	9 20
USB_MINI	USB_90D	USB	USB MINI N	9 20
USB_MINI	USB_90D	USB	USB2_AIRPORT_P	7 31
USB_MINI	USB_90D	USB	USB2_AIRPORT_N	7 31
USB_EXTD	USB_90D	USB	USB EXT D P	9 20
USB_EXTD	USB_90D	USB	USB EXT D N	9 20
USB_CAMERA	USB_90D	USB	USB CAMERA P	20 66
USB_CAMERA	USB_90D	USB	USB CAMERA N	20 66
USB_CAMERA	USB_90D	USB	USB2_CAMERA_CONN_P	7 66
USB_CAMERA	USB_90D	USB	USB2_CAMERA_CONN_N	7 66
USB_IR	USB_90D	USB	USB IR P	20 60
USB_IR	USB_90D	USB	USB IR N	20 60
USB_TPAD	USB_90D	USB	USB TPAD P	9 20
USB_TPAD	USB_90D	USB	USB TPAD N	9 20
USB_TPAD	USB_90D	USB	CONN_TPAD_USB_P	7 49
USB_TPAD	USB_90D	USB	CONN_TPAD_USB_N	7 49
USB_BT	USB_90D	USB	USB BT P	9 20
USB_BT	USB_90D	USB	USB BT N	9 20
USB_BT	USB_90D	USB	USB2_BT_F_P_CONN	7 40
USB_BT	USB_90D	USB	USB2_BT_F_N_CONN	7 40
USB_EXTB	USB_90D	USB	USB EXT B P	20 39
USB_EXTB	USB_90D	USB	USB EXT B N	20 39
USB_EXTB	USB_90D	USB	USB2_EXTB_F_P	39
USB_EXTB	USB_90D	USB	USB2_EXTB_F_N	39
USB_EXCARD	USB_90D	USB	USB EXCARD P	9 20
USB_EXCARD	USB_90D	USB	USB EXCARD N	9 20
USB_EXTC	USB_90D	USB	USB EXTC P	9 20
USB_EXTC	USB_90D	USB	USB EXTC N	9 20
MCP_USB_RBIA	MCP_USB_RBIA		MCP_USB_RBIA GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS MCP 1 CLK	21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS MCP 1 DATA	21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	21 52
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK R	21
HDA_SYNC	HDA_55S	HDA	HDA SYNC	21 52
HDA_SYNC	HDA_55S	HDA	HDA SYNC R	21
HDA_RST_L	HDA_55S	HDA	HDA RST L	21
HDA_RST_L	HDA_55S	HDA	HDA RST L	21 52
HDA_SDIN	HDA_55S	HDA	HDA SDIN	21 52
HDA_SDIN	HDA_55S	HDA	HDA SDIN CODEC	21 52
HDA_SDOIT	HDA_55S	HDA	HDA SDOIT	21 52
HDA_SDOIT	HDA_55S	HDA	HDA SDOIT R	21
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP_HDA_PULLDN_COMP	21
MCP_SIO_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK R	21 26
MCP_SIO_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 41
SPI_CLK	SPI_55S	SPI	SPI_CLK R	21 43
SPI_CLK	SPI_55S	SPI	SPI_CLK_MUX	43 51
SPI_MOSI	SPI_55S	SPI	SPI_MOSI R	21 43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_MUX	43 51
SPI_MISO	SPI_55S	SPI	SPI_MISO_MUX	43 51
SPI_MISO	SPI_55S	SPI	SPI_MISO R	43 51
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 43
SPI_CS0	SPI_55S	SPI	SPI_CS0 L	

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SR	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0	18 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	18 32
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWDOWN_L	ENET_MII_55S	ENET_MII	ENET_PWDOWN_L	18 32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RX_CTRL	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RX_CTRL	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
ENET_RESET_L	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	12 34
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	12 34

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Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_P	37
FW_P1_TPA	FW_110D	FW_TP	FW_PORT_A_N	37
FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_P	37
FW_P1_TPB	FW_110D	FW_TP	FW_PORT_B_N	37

Port 2 Not Used

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FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SMBUS SMC A S3 SCL	SMR 550	5MM	SMBUS SMC A S3 SCL
SMBUS SMC A S3 SDA	SMR 550	5MM	SMBUS SMC A S3 SDA
SMBUS SMC B S0 SCL	SMR 550	5MM	SMBUS SMC B S0 SCL
SMBUS SMC B S0 SDA	SMR 550	5MM	SMBUS SMC B S0 SDA
SMBUS SMC O S0 SCL	SMR 550	5MM	SMBUS SMC O S0 SCL
SMBUS SMC O S0 SDA	SMR 550	5MM	SMBUS SMC O S0 SDA
SMBUS SMC BSA SCL	SMR 550	5MM	SMBUS SMC BSA SCL
SMBUS SMC BSA SDA	SMR 550	5MM	SMBUS SMC BSA SDA
SMBUS SMC MGMT SCL	SMR 550	5MM	SMBUS SMC MGMT SCL
SMBUS SMC MGMT SDA	SMR 550	5MM	SMBUS SMC MGMT SDA

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
CHGR CSI	1TO1 DIFFPAIR		CHGR CSI P
	1TO1 DIFFPAIR		CHGR CSI N
CHGR CSO	1TO1 DIFFPAIR		CHGR CSO P
	1TO1 DIFFPAIR		CHGR CSO N

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SMC Constraints

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K36B BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA_P1MM				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	*	Y	0.145 MM	0.145 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
27F4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27F4_OHM_SE	*	Y	0.275 MM	0.275 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.175 MM	0.175 MM	0.200 MM	0.200 MM	0.200 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.109 MM	0.109 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.089 MM	0.089 MM		0.230 MM	0.230 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM	0.400 MM	0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM	0.330 MM	0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
1:1_DIFPPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.152 MM	?
3X_DIELECTRIC	*	0.228 MM	?
4X_DIELECTRIC	*	0.304 MM	?
5X_DIELECTRIC	*	0.380 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

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K36B RULE DEFINITIONS

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