1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
14.5			2009-06-12

K84 MLB SCHEMATIC

PVT 06/12/2009

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7982	1	SCHEM,MLB,K84	SCH	CRITICAL	
820-2567	1	PCBF,MLB,K84	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K84

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: 14.5.0

BRANCH:

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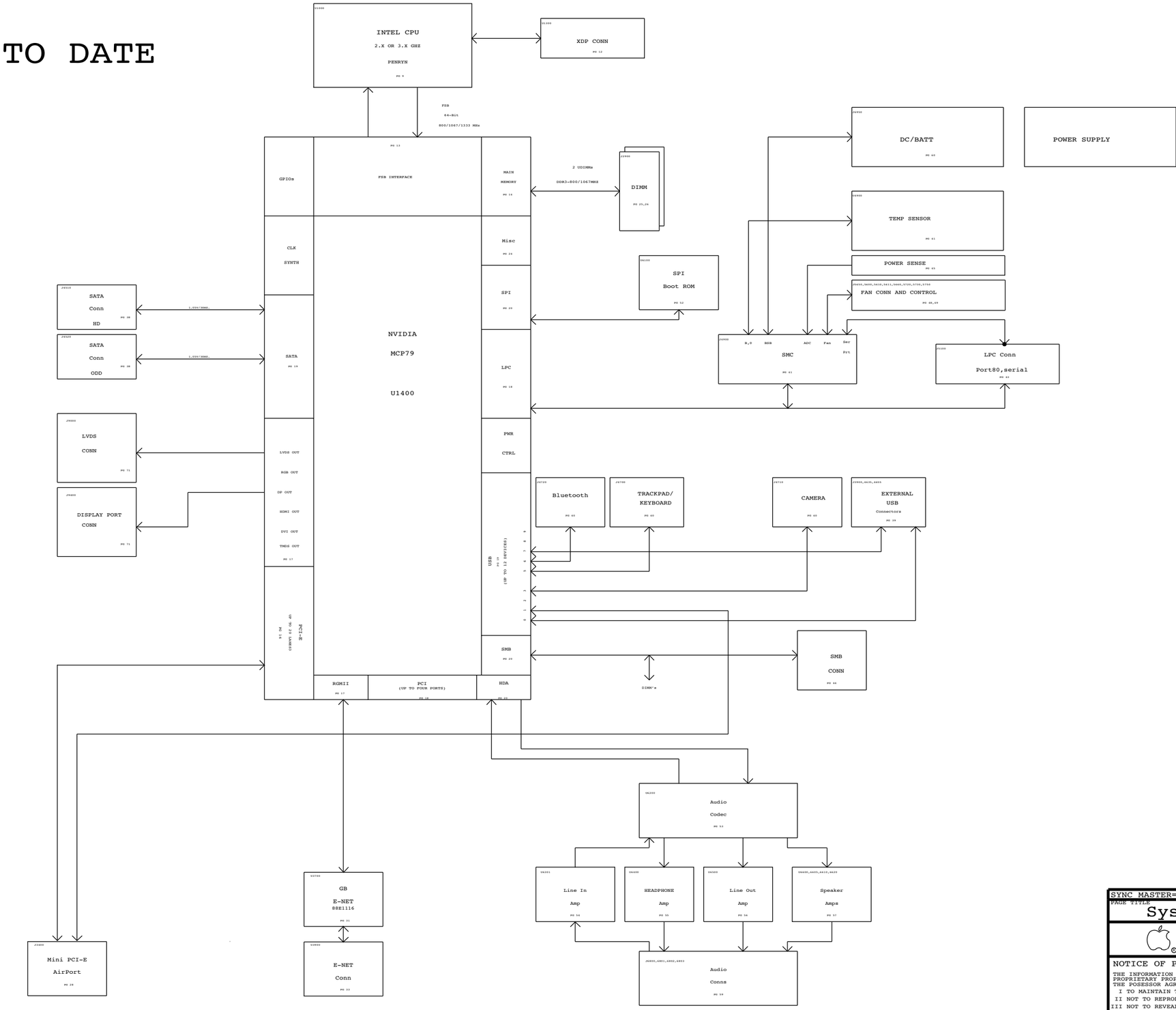
NOT UP TO DATE



SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

PAGE TITLE
System Block Diagram

Apple Inc.

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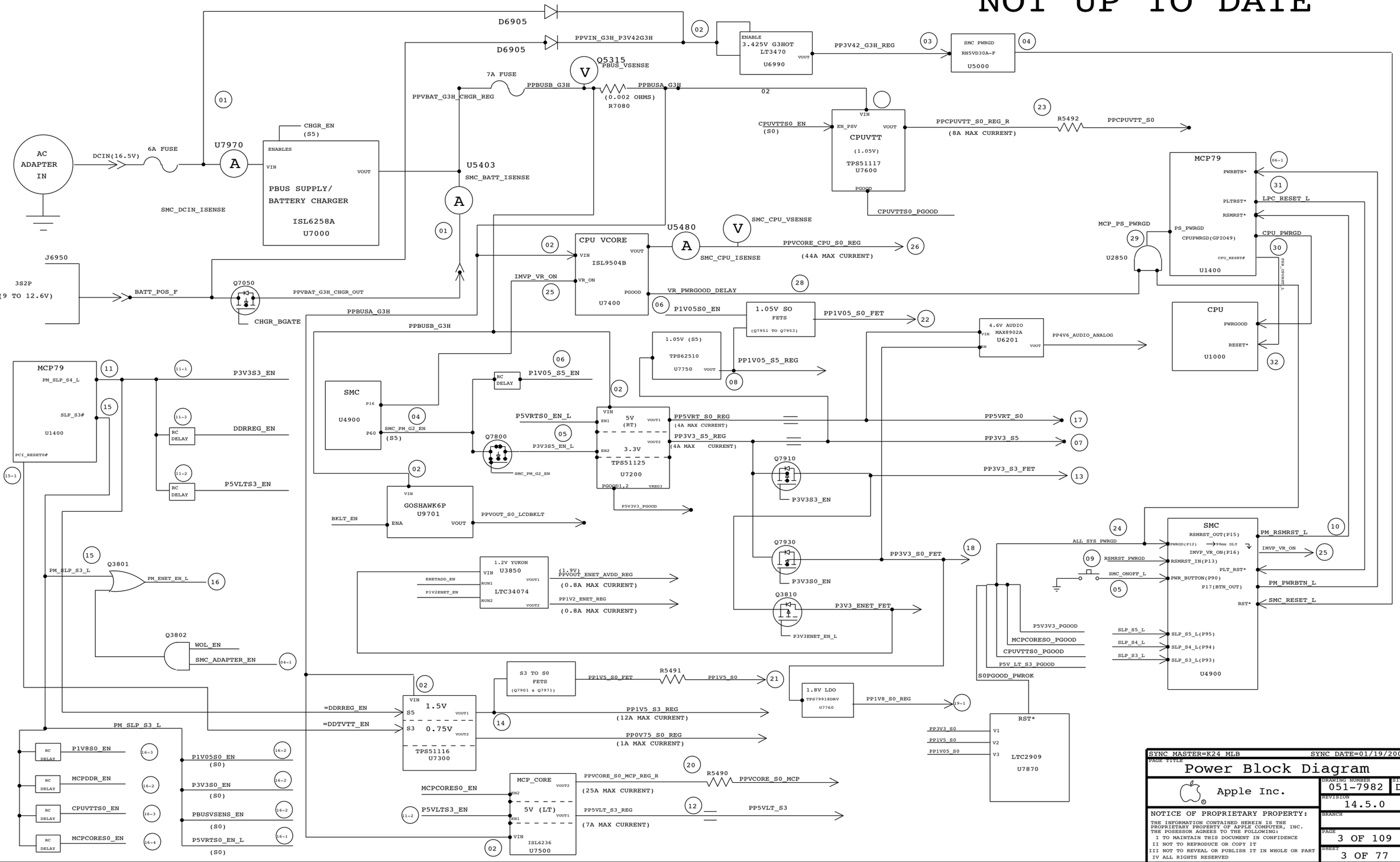
K84 POWER SYSTEM ARCHITECTURE

NOT UP TO DATE



SYNC MASTER=K24_MLB SYNC DATE=01/19/2009

PAGE TITLE

Power Block Diagram

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0035	PCBA,MLB,FOX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,FOX_DDR_CONN,EEE_8CG
639-0254	PCBA,MLB,MLX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,MLX_DDR_CONN,EEE_A36
085-0748	K84 MLB DEVELOPMENT BOM	K84_DEVEL_ENG

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	{EEE:8CG}	CRITICAL	EEE_8CG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	{EEE:A36}	CRITICAL	EEE_A36

BOM Groups

BOM GROUP	BOM OPTIONS
K84_COMMON	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_ENG,K84_PROGPARTS
K84_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K84_MISC	ONEWIRE_PU,DP_ESD,MIKEY,LDO_NO,MIKEY_LOAD_DET,MEM_SENSE,1P05_HIGH_SIDE_SENSE,MCP_T_DIODE_SENSOR,MCPSMC_DIGITEMP_YES
K84_PROGPARTS	BOOTROM_PROG,SMC_PROG,WELLSPRING_PROG
K84_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K84_DEBUG_PVT	DEVEL_BOM,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K84_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K84_DEVEL_ENG	DEBUG_ADC,XDP_CONN,LPCPLUS,VREFMRGN
K84_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33783704	1	PDC,8LGE2,PRQ,2.26,25W,1066,80,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
33880710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03
51680706	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3200	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SODIMM,P=0.60MM	J3100	CRITICAL	FOX_DDR_CONN
51680790	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,NON/SC	J3200	CRITICAL	MLX_DDR_CONN
516-0213	1	CONN,204P,SODIMM,P=0.6MM,HF	J3100	CRITICAL	MLX_DDR_CONN
452-1708	4	SCR,M1.6X0.35X6.0,D4,NO.3,BLK,N97	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0748	1	K84 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

Programmable Parts

33880563	1	IC,SMC,RS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
34182485	1	IC,SMC,K84	U4900	CRITICAL	SMC_PROG
33580610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
34182487	1	IC,PRGRM,SPI BOOTROM,UNLOCK,K84	U6100	CRITICAL	BOOTROM_PROG
33782983	1	IC,PSOC+ W/ USB,56 PIN,MLP,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
34182491	1	IC,WELLSPRING CONTROLLER,K84	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 34182488

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15280693	15280778		ALL	DALE/VISHAY, MAGLAYERS AS ALTERNATE
15280796	15280685		ALL	CYNTEC AS ALTERNATE
15780058	15780055		ALL	DELTA AS ALTERNATE
13880603	13880602		ALL	MURATA AS ALTERNATE
12880093	12880218		ALL	KEMET AS ALTERNATE
15280874	15280516		ALL	MAGLAYERS AS ALTERNATE
15280847	15280586		ALL	MAGLAYERS AS ALTERNATE
10480018	10480023		ALL	DALE/VISHAY AS ALTERNATE
514-0690	514-0691		ALL	PLASTIC PART AS ALTERNATE
514-0688	514-0689		ALL	PLASTIC PART AS ALTERNATE
35382718	35382310		ALL	NEW INTERSIL PART AS ALTERNATE
13880661	13880540		ALL	LOW NOISE MURRATA AS ALTERNATE

514-0690 IS PLASTIC VERSION OF 514-0691 METAL PART FOR MINI DP CONNECTOR
514-0688 IS PLASTIC VERSION OF 514-0689 METAL PART FOR USB CONNECTORS

K84 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

1/19/2009:INITIAL RELEASE 0.0.1-
- ALL PAGES SYNC'ED FROM K24
- REPLACED K24 REFERENCES WITH K84
- UPDATED SCHEMATIC AND PCB PART NUMBER INFO

1/21/2009: RELEASE 0.0.2-
- DELETED PAGES 41,42,43,48,97,98,105 [FIREWIRE, IR CONTROLLER, BACKLIGHT CKT]
- UPDATED BOM CONFIGURATIONS
- DELETED IR SPECIFIC NETS ON SATA CONNECTOR

1/21/2009: RELEASE 0.0.3-
- CORRECTD BOM CONFIG TABLES

1/21/2009: RELEASE 0.0.4-
- CORRECTED BOM CONFIG TABLE (ADDED BACK BKLT_ENG)
- ADDED BACK PAGES 97-98 (LCD BACKLIGHT DRIVER AND SUPPORT CKT)
- DELETED KB BACKLIGHT DRIVER/DETECTION CKT

1/23/2009: RELEASE 0.0.5-
- UPDATED PAGES 72-73 : 5V/3.3V & DDR3 POWER SUPPLIES AS PER FLO'S RECOMMENDATIONS
- SET SOURCE SYNC OF AUDIO PAGES (62-63, 65-68) FROM LENG'S AUDIO PAGES

1/27/2009: TMLB FIRST RELEASE 0.0.1-
- NAME CHANGED TO TMLB. SO CALLING IT RELEASE 0.0.1
- UPDATED SCHEM AND PCBF PART NUMBER INFO
- UPDATED BOM OPTION TABLE TO REFLECT K84_DEBUG_PROD AND BLANK PROGRAMMED PARTS. ALSO, DELETED BMON_ENG BOM OPTION
- PAGE 54: REMOVED BMON CURRENT SENSE CIRCUIT
- REMOVED ALS SPECIFIC NETS (PAGE 34 & 52)

2/5/2009: RELEASE 0.0.2 -
- COPIED TMLB OVER TO MLB AS K84 WILL BE PENRYN SKU WHILE K83 WILL BE ATOM SKU
- UPDATED THE SCHEMATICS, PCBF AND PCBA PART NUMBER INFO
- REPLACED TEXT TMLB WITH MLB THROUGH OUT THE SCHEMATICS
- PAGE 4: UPDATED BOM OPTION TABLE TO REFLECT K84_DEBUG_ENG FOR K84_COMMON BOM GROUP
- PAGE 4: UPDATED EEE NUMBER - 8CG
- PAGE 4: ADDED 085 DEVELOPMENT BOM VARIANT & K84_DEVEL_ENG, K84_DEVEL_PVT BOM GROUPS
- PAGE 7: DELETED IR_RX_OUT, PP5V_S3_IR_R, KBDLED_ANODE, SMC_KBDLED_PRESENT_L
- PAGE 8: DELETED FIREWIRE, IR AND BMON SPECIFIC NETS
- PAGE 9: DELETED R0950 PCIE_FW_PRSNT_L 'S PD RESISTOR
- PAGE 9: ADDED UNUSED FIREWIRE LANE NETS AS TEST POINTS
- PAGE 9: CHANGED ALIAS OF FW_PME_L TO TP_FW_PME_L
- PAGE 9: ADDED SMC_SYS_KBDLED TP ALIAS
- PAGE 55: REPLACED CPU/MCP THERMAL SENSORS U5515 ANDB U5535 WITH THE CHEAPER VERSION APNB 353S2573
- PAGE 72: REPLACE 16V INPUT SIDE CAPS C7280 & C7240 WITH 39UF APN 128S0248 AS PER DAYU'S RECOMMENDATIONS
- PAGE 72: REPLACE Q7220 WITH SIZ700DT
- PAGE 73: REPLACE 16V INPUT SIDE CAPS C7331 WITH 39UF APN 128S0248 AS PER DAYU'S RECOMMENDATIONS
- PAGE 76: REPLACE Q7620 WITH SIZ700DT

2/6/2009: MAJOR RELEASE 0.1.0 -
- NO CHANGES SINCE LAST MINOR RELEASE 0.0.2

2/6/2009: WEEKLY RFA BOM RELEASE 1.0.0-
- NO CHANGES SINCE LAST MAJOR RELEASE 0.1.0

2/15/2009: RELEASE 2.0.0 (WEEKLY RFA)-
1. PAGE 3: POWER BLOCK DIAGRAM - ADDED TWO ALIASES OF PPBUS (PPBUSA_G3H & PPBUSB_G3H). PPBUSA_G3H FEEDS CORE REGULATORS: CPUVTT, MCP VCORE, CPU VCORE & DDR. ALSO, ADDED SENSE RESISTOR ON PPBUS
2. PAGE 8: ADDED TWO ALIASES OF PPBUS (PPBUSA_G3H & PPBUSB_G3H). PPBUSA_G3H FEEDS CORE REGULATORS: CPUVTT, MCP VCORE, CPU VCORE & DDR, WHILE PPBUSB FEEDS 5V/3.3 V SUPPLY, LCD BKLT & PPBUS VOLTAGE SENS
3. PAGES 31, 32: REPLACED 0.1UF 0204 TYPE DDR3 DECOUPLING CAPS WITH 0402 TYPE CAPS (APPLE P/N : 132S1059)
4. PAGE 34: REPLACED AIRPORT CONNECTOR WITH PN 516S0580 AND UPDATED CONNECTIONS ACCORDINGLY
5. PAGE 34: REPLACED SCHMITT'S TRIGGER WITH PN 311S0449
6. PAGE 45: REPLACED SATA HDD CONNECTOR WITH APPLE PN 516S0350 AND UPDATED CONNECTIONS ACCORDINGLY
7. PAGE 45: ADDED 2 PIN CONNECTOR (APPLE PN 518S0519) FOR SIL
8. PAGE 46: REPLACED ESD DIODES WITH CHEAPER PN 377S0066
9. PAGE 54: ADDED BOM OPTION- DEBUG_SENSE- TO CPU 1.05V/CPU VCORE HIGH SIDE CURRENT SENSE AND MCP MEM VDD CURRENT SENSE CIRCUITS FOR DEVELOPMENT BOM
10. PAGE 4: ADDED DEBUG_SENSE BOM OPTION TO THE K84_DEVEL_ENG BOM GROUP
11. ... J5800. RENAMED PP18V5_S3, PP3V3_S3_LDO_R, PP3V3_S3_LDO TO PP18V5_S3_LDO, PP3V3_S3_IPD_R AND PP3V3_S3_IPD RESPECTIVELY TO MATCH WITH NEW ADDED PAGE 60 NET NAMES.
12. ADDED PAGE 60 AND COPIED OVER ZEPHYR2 SCHEMATICS PAGE FROM M97 IPD FLEX WELLSPRING. DELETED THE IPD BOARD CONNECTOR. CALLING IT WELLSPRING 3
13. PAGE 69: REPLACED BATTERY CONNECTER WITH PN 518S0540 AND BIL CONNECTOR WITH PN 518S0588. UPDATED CONNECTIONS ACCORDINGLY
14. ... PPBUS INTO TWO BRANCHES - PPBUSA & PPBUSB. ADDED SENSE RESISTOR R7080 (2 MOHMS) ON PPBUSA. ALSO ADDED INA210 AMPLIFIER CKT ACROSS SENSE LINES. ADDED PP3V42_G3H_PPBUSAISNS (IN210
15. PAGE 97: REPLACED BKLT DRIVER CKT WITH THAT OF FREESCALE PART, SIMILAR TO K19I
16. PAGE 69: MOVED THE DECAP C6908 TO CORRECT PART U6901.5 (SIMILAR TO K24)
17. PAGE 4: REMOVED BKLT_ENG BOM OPTION

PAGES SYNC'ED FROM LENG OOI'S AUDIO_MLB SINCE LAST RELEASE 1.0.0
1. REPLACED MIKEY CD3272 WITH CD3282
2. ADAPT JACK INSERT DETECT CIRCUIT TO CD3282 JACK INSERT DETECT FUNCTION.
3. REMOVED JACK EXTRACT CIRCUITRY, FUNCTION IS TAKEN OVER BY CD3282
4. REMOVE FM ANTENNA NET.

PAGES SYNC'ED FROM K24 SINCE LAST RELEASE 1.0.0
1. PAGE 75: MCP VCORE INDUCTOR CHECK FOR PD: CHANGED L7560 TO 152S0966 AND THEN TO 152S0867. BUT NOW IT IS BACK TO 13A PART FOR NOW
2. ADDED DIDT TO ALL THE GATE AND PHASE NETS

2/25/09: WEEKLY RFA RELEASE (3.0.0)
- ADDED DIDT ATTRIBUTE
- PAGE 4: REMOVED SUPERCAP NO BOM OPTION. ADDED DEBUG_ADC BOM OPTION UNDER K84_DEVEL_ENG (THIS IS FOR NEW SENSOR PAGE 60)
- PAGE 4: CORRECTED APN FOR PROGRAMMED PARTS - SMC, BOOT ROM, WELLSPRING
- PAGE 4: REMOVED LDO_YES BOM OPTION
- PAGE 8: DIVIDED PP5V_S0_FET INTO TWO BRANCHES - PP5VRT_S0_FET & PP5VLT_S0_FET (FOR ROUTING PURPOSE, 5V_S3 IS DIVIDED INTO RT AND LT POWER SUPPLY AND WILL HAVE CORRESPONDING S0 FETS)
- PAGE 8: DIVIDED PP5V_S3_REG INTO TWO BRANCHES - PP5VRT_S3_REG & PP5VLT_S3_REG
- PAGE 8: ADDED PP5V_S3_DEBUG_ADC_AVDD/DVDD & PP5V_S3_DEBUG_ISNS ALIASES FOR NEW SENSOR PAGE 60
- PAGE 8: ADDED PP3V3_S3_BT ALIAS FOR BLUETOOTH ON RIGHT CLUTCH CONNECTOR PAGE
- PAGE 8: ADDED ALIAS PPVIN_S3_5VLTS3 UNDER PPBUSB
- PAGE 8: ADDED ALIAS PP5VLT_S3_V5IN UNDER PP5VRT_S3_REG
- PAGE 28: REMOVED RTC POWER SOURCES CIRCUIT AND SUPERCAP NO BOM OPTION FROM R2820
- PAGE 34: SINCE X16 AIRPORT CARD SOLUTION IS BEING USED, PP5V_S3_WLAN IS REPLACED BY PP3V3_S3_WLAN (GOING TO Q3450). ALSO, REPLACED PP5V_WLAN WITH PP3V3_WLAN ON PAGE 6 (FUNCTIONAL TEST POINTS)
- PAGE 34: R3453 IS MODIFIED TO 110K RESISTOR, R3454 IS NOSTUFF AND R3453 IS PULLED UP TO PP3V3_WLAN_F. THIS IS TO ENSURE 3.3V LEVEL AT THE INPUT OF U3402 AND MAINTAIN 100MS DELAY SPEC BETWEEN 3.3V POWER TO THE CARD GETTING STABLE AND AIRPORT GETTING OUT OF RESET
- PAGE 34: DISCONNECTED PP5V_S3_BTCAMERA_F POWER RAIL FROM THE CONNECTOR AND REPLACED IT WITH PP3V3_S3_BT (SIMILAR TO M96). CAMERA SIGNALS ARE ROUTED VIA LVDS CONNECTOR. MOVED PP5V_S3_BTCAMERA POWER CIRCUIT ALONG WITH THE USB CAMERA SIGNALS TO LVDS PAGE. ALSO, RENAMED THIS POWER RAIL TO PP5V_S3_CAMERA ON LVDS PAGE
- PAGE 34: ADDED SENSE RESISTOR R3452 ON PP3V3_WLAN SIGNAL
- PAGE 34: ADDED CHOKES ON PCIE TX/RX SIGNALS. UPDATED PAGE 6 (FUNCTIONAL TEST POINTS) ACCORDINGLY
- PAGE 34: REPLACED L3404 WLAN INDUCTOR WITH LOW DCR 0603 PART - APN 155S0367
- PAGE 39: REPLACED ETHERNET CONNECTOR WITH APN 514-0668 (SIMILAR TO K36B)

- PAGE 45: CHANGED SATA HDD CONNECTOR TO APN 516S0616
- PAGE 45: ADDED SENSE RESISTORS R4598 AND R4599 ON 5V ODD AND 5V HDD RAILS RESPECTIVELY
- PAGE 50: UNSTUFFED R5055 AND USED SMC_NB_MISC_ISENSE SIGNAL PORT (SMC) FOR CONNECTING PPBUSA ISENSE SIGNAL. ADDED ALIAS ON THIS PAGE
- PAGE 51: REPLACED TWO DEMUX SOLUTION WITH A SINGLE DEMUX 1X2 SOLUTION. APN USED - 353S2220 [ONLY CHIP SELECT IS BEING DEMUXED]
- PAGE 51: R5156, R5157 AND R5158 ARE NOW 0 OHM ISOLATION RESISTORS PLACED ON SPI BUS NEXT TO THE LOCATION WHERE IT BRANCHES INTO TWO - ONE GOING TO MLB SPI ROM AND THE OTHER GOING TO LPC CONNECTOR. THESE RESISTORS ARE PLACED ON THE LPC CONNECTOR BRANCH. THIS IS TO AVOID STUBS IN PRODUCTION
- PAGE 52: ADDED SENSOR ADC CONNECTION BLOCK UNDER 'SMC 0 SMBUS CONNECTIONS' SECTION
- PAGE 54: MOVED PBUS INA210 CIRCUIT TO THIS CURRENT SENSOR PAGE. RENAMED REF DES AS PER THIS PAGE 54
- PAGE 55: DELETED J5590 CONNECTOR (CONNECTED TO HEAT-PIPE TEMPERATURE DETECTION RAILS)
- PAGE 55: REPLACED U5515 & U5535 WITH CHEAPER APN 353S2571
- PAGE 60: REMOVED WELLSPRING 3 PAGE (GOING BACK TO K24 SOLUTION) AND REPLACED IT WITH K19I DEBUG SENSOR PAGE (SCHUTIL SYNC)
- PAGE 61: RENAMED SPI SIGNALS TO MATCH WITH CHANGES ON PAGE 51
- PAGE 69: ADDED BOM OPTION NOSTUFF TO D6950 FOR NOW
- PAGE 69: ADDED D6951 ESD DIODE ON BIL SMBUS SIGNALS (NOSTUFF FOR NOW)
- PAGE 69: REPLACED BATTERY CONNECTOR J6950 WITH APN 518S0540 (M96) CONNECTOR
- PAGE 70: ADDED BYPASS 0 OHM RESISTOR R7050 (NOSTUFF FOR NOW) OPTION FOR NEW CHIP WHICH WON'T REQUIRE U7060 SOLUTION
- PAGE 71: ADDED NEW PAGE FOR PP5V_LT_REG POWER SUPPLY. UPDATED ALL THE REF DES AS PER THE PAGE NUMBER
- PAGE 72: REPLACE 16V INPUT SIDE CAPS C7280 WITH 68UF OSCON CAP (APN 128S0275) & C7240 WITH 39UF (APN 128S0248)
- PAGE 71: CHANGED C7160 TO 39UF OSCON CAP (APN 128S0248)
- PAGE 72: REPLACE Q7220 WITH SIZ700DT AND L7260 WITH SMALLER 10A PART (APN 152S0778)
- PAGE 73: ADDED SENSE RESISTOR R7350 ON 1.5V DDR3 SUPPLY RAIL
- PAGE 77: REMOVED 1.05V S0 PLL LDO CIRCUIT. AND, REMOVED LDO_NO BOM OPTION FROM R7745
- PAGE 75: CHANGED C7571 & C7560 TO 68UF OSCON CAPS (APN 128S0275)
- PAGE 78: RENAMED P5VS3_EN_L TO P5VRTS3_EN_L (RT POWER SUPPLY ENABLE) AND ADDED R7814, C7814 S3 ENABLE CIRCUIT FOR GENERATING P5VLTS3_EN ENABLE SIGNAL FOR LT POWER SUPPLY
- PAGE 78: ADDED P5V_LTS3_PGOOD POWER GOOD SIGNAL (WIRED AND WITH OTHER S0 RAILS PGOOD) CORRESPONDING TO 5V LT POWER SUPPLY
- PAGE 78: ADDED 0 OHM ISOLATION RESISTORS ON POWER GOOD SIGNALS (BEFORE WIRED AND)
- PAGE 79: ADDED 5V LT S0 FET AND UPDATED NET NAMES FOR BOTH RT AND LT S0 FET CIRCUITS ACCORDINGLY
- PAGE 90: UPDATED LVDS CONNECTOR CONNECTIONS AS PER STEVE'S RECOMMENDATION. ADDED CAMERA SIGNALS
- PAGE 97: ADDED BOM OPTION - NOSTUFF- TO R9702 AS PER K19I
- PAGE 8: DELETED PP5V_S0_BKL, RENAMED PP1V05_S0_MCP_PLL_UF_R TO PP1V05_S0_MCP_PLL_UF
- PAGE 8: DELETED PP1V5_S0_MCP_PLL_VLDO, PP3V3_S0_BKL_VDDIO, PP3V3_S0_MCP_PLL_VLDO
- PAGE 8: RENAMED PPVIN_S5_1V5S3_0V75S0 TO PPVIN_S5_1V5S30V75S0
- PAGE 28: DELETED FW_RESET_L SIGNAL
- PAGE 58: DELETED KB BKLT CIRCUIT
- PAGE 60: UPDATED WLAN DIVIDER CIRCUIT WITH 3V3 POWER RAIL INSTEAD OF 5V
- PAGE 73: UPDATED 1.5V/0.75V POWER SUPPLY WITH CORRECT NET NAMES REFLECTING 1.5V/0.75V INSTEAD OF 1.8V/0.9V AND IN SYNC WITH PAGE 8 ALIASES
- PAGE 4: REMOVED 152S0778 ALTERNATE PART ENTRY FROM THE ALTERNATE PARTS TABLE SINCE L7260 AS HAS BEEN REPLACED WITH THIS PART
- PAGE 4: REMOVED 104S0018 ALTERNATE PART ENTRY FROM THE ALTERNATE PARTS TABLE

PAGES SYNCED FROM K24 SINCE LAST RELEASE 2.0.0

- PG 50: SWAPPED THE PART NUMBER AND THE ALTERNATE PART NUMBER FOR VR5020. MADE ISL60002 THE ALTERNATE PART

PAGES SYNCED FROM LENG OOI'S AUDIO_MLB SINCE LAST RELEASE 2.0.0
- CHANGED SPEAKER AMPS TO LM48310, PLACEHOLDERS FOR LM48311. LM48311 IS THE CSP VERSION OF THE LM48310.
- CHANGED LDO TO B LP5900.
- REMOVED OPTIONAL STUFFING RESISTORS AROUND THE RE-TASKING JACK ANALOG SWITCH.

2/26/2009: RELEASE 4.0.0 (RFA RELEASE):
- PAGE 4: ADDED LDO_NO BOM OPTION
- PAGE 8: RENAMED PP1V05_S0_MCP_PLL_UF BACK TO PP1V05_S0_MCP_PLL_UF_R
- PAGE 8: ADDED BACK - PP1V5_S0_MCP_PLL_VLDO, PP3V3_S0_MCP_PLL_VLDO
- PAGE 13: REPLACED XDP CONNECTOR WITH MINI XDP CONNECTOR APN 516S0625
- PAGE 34: ADDED NOTE WITH REGARD TO SMBUS CONNECTIONS TO THE AIRPORT CONNECTOR
- PAGE 34: ADDED NOTE WITH REGARD TO 100 MS DELAY REQUIREMENT BETWEEN 3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET
- PAGE 54: REMOVED NOTE ON AMON AND BMON
- PAGE 57: REPLACED KEYBOARD CONNECTOR WITH APN 518S0738
- PAGE 77: ADDED BACK - 1.05 PLL LDO CIRCUIT
- PAGE 90: REFRESHED THE SYMBOL OF U9000, PART NUMBER CHANGED TO 353S2603

3/4/2009: RELEASE 5.0.0 (RFA)-
- PAGE 34: ADDED A TEXT NOTE THAT J3401 (AIRPORT CONNECTOR) COULD CHANGE TO 1.8MM HEIGHT APN 516S0582
- PAGE 57: REPLACED KEYBOARD CONNECTOR WITH THAT OF K24 (APN 518S0637) - SYNC'ED FROM K24
- PAGE 69: REPLACED BATTERY CONNECTOR WITH THAT OF K24 (APN 518-0359)
- PAGE 69: DELETED NOTE REGARDING INDUCTOR FILTER REQUIREMENT ON BATT_POS_F (AS PER JOHN SCHEN)
- PAGE 70: CHANGED Q7050 TO 376S0761 AS PER DAYU & K24 DESIGN
- PAGE 70: CHANGED Q7000 AND Q7001 CHEAPER TO 376S0667 (HAT1128) AS PER DAYU'S RECOMMENDATION
- PAGE 71: DISCONNECTING EN_PSV (PIN 34) FROM P5VLTS3_EN SIGNAL AND CONNECTING IT TO PP5VLT_S3_V5IN (5VRT PS)
- PAGE 72: L7220 CHANGED TO 152S0778 FOR COST SAVING AS PER DAYU
- PAGE 73: ADDED ONE MORE OSCON 39UF CAP ON INPUT SIDE
- PAGE 73: MOVED THE SENSE RESISTOR NEXT TO INDUCTOR
- PAGE 74: REMOVED UNUSED NETWORK ON U7400 PIN 5 AND PIN 6 AS PER DAYU [R7406, C7410, R7427, R7426]
- PAGE 74: STUFF R7413 AS PER DAYU
- PAGE 74: CHANGED Q7400 AND Q7402 TO 376S0772 AS PER DAYU
- PAGE 74: CHANGED Q7401 AND Q7403 TO 376S0771 AS PER DAYU
- PAGE 75: CHANGED R7525 TO 107S0132 FOR COST SAVING AS PER DAYU
- PAGE 78: DELETING P5VLTS3_EN RC CIRCUIT AS IT IS NO LONGER NEEDED (SEE ABOVE). ALSO UPDATED ASSOCIATED TEXT NOTE
- PAGE 97: FIXED CONNECTION POINT (DOT) FOR LCDBKLT_VIN
- PAGE 97: ADDED 0 OHMS SERIES RESISTOR ON LCD_BKLT_PWM FOR DEBUGGING PURPOSES
- PAGE 97: RENAMED LCD_BKLT_PWM TO LVDS_IG_BKL_PWM
- PAGE 97: CHANGED VOVP VALUE TO 6.9V AS PER FREESCALE FEEDBACK
- PAGE 97: ADDED R9726 (22K) AND SWAPPED C9705 AND R9705 LOCATIONS FOR NOISE REDUCTION AS PER FREESCALE RECOMMENDATION
- PAGE 97: DELETED C9712 AS IT IS REDUNDANT
- PAGE 97: ADDED PLACEMENT NOTE ATTRIBUTE TO C9713 AND C9710 FOR PLACING THOSE NEAR L9710

3/20/2009: RELEASE 7.1.0 (MAJOR)-

- PAGE 31 & 32: PIN SWAPS ON THE DDR3 CONNECTOR PAGES FOR ROUTING PURPOSES (REFER TO RON'S EMAIL)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 7.0.0

-PG. 67, DELETED R6726
-PG. 66, CHANGED C6610/11/30/31 TO 0.015UF
-PG. 68, ADDED MIKEY MIC LOAD COMPARATOR CKT
-PG. 68, ADDED R6873
-PG. 68, CORRECTED CODEC OUTPUT SIGNALS TABLE COMMENTS

3/24/2009: RELEASE 7.2.0 (MAJOR)-

- PAGE 4: CHANGE THE CPU TO NEW APNB 337S3704
- PAGE 7: DELETED PPBUS_R_G3H AS NO NEED OF TWO PPBUS BRANCHES
- PAGE 8: COMBINED TWO SEPARATE PPBUSA/B BRANCHES INTO ONE =PPBUS_G3H
- PAGE 9: ADDED LVDS HOLE APN 998-1521
- PAGE 34: CHANGED J3401 ROUTING CONNECTIONS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 45: MIRROR'ED J4500 AND RECONNECTED PINS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 45: CHANGED J4501 ROUTING CONNECTIONS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 50: DELETED SMC_PPBUSA_ISENSE ALIAS AND STUFFED R5055
- PAGE 54: DELETED U5470 INA210 CIRCUIT AS THERE IS NO NEED
- PAGE 70: REMOVED R7080 SENSE RESISTOR AND RENAMED =PPBUSB_G3H TO =PPBUS_G3H AS NO NEED TO HAVE TWO PPBUS BRANCHES
- PAGE 70: DELETED R7050 CONNECTION BETWEEN CHGR_AGATE AND CHGR_LOWCURRENT_GATE AS PER DAYU
- PAGE 70: ADDED R7050 (6259_YES) CONNECTION FROM PIN 4 (VREF) TO PM_SLP_S3_L AS PER DAYU
- PAGE 70: AS PER DAYU, ADDED:
  R7051 (6259_YES) CONNECTION BETWEEN CHGR_PIN26 AND CHGR_LOWCURRENT_GATE;
  R7052 (6259_NO) CONNECTION BETWEEN CHGR_PIN26 AND GND_CHGR_SGND;
  R7053 (6259_YES) CONNECTION BETWEEN CHGR_PIN6 AND PIN 12 (VHST);
  R7054 (6259_NO) CONNECTION BETWEEN CHGR_PIN6 AND GND_CHGR_SGND
- PAGE 73: RENAMED TEXT NOTE FOR =PP1V5_S3_REG NET TO VOLTAGE=1.5V
- PAGE 97: STUFF R9716 AS PER KIRAN'S FEEDBACK

3/6/2009: RELEASE 6.0.0 (RFA:)-

- PAGE 4: ADDED 152S0693 AS ALT FOR 152S0778 FOR SUPPLY REDUNDANCY
- PAGE 4: ADDED 138S0603 AS ALT FOR 138S0602B FOR SUPPLY REDUNDANCY
- PAGE 4: ADDED CYNTEC ALTERNATES FOR 107S0074 --> 107S0138 [R7020] AND 107S0075 [R7008] --> 107S0139
- PAGE 4: ADDED DALE/VISHAY ALTERNATES FOR 104S0023 --> 104S0018
- PAGE 4: ADDED BOM OPTION 6259_NO TO THE TABLE UNDER K84_MISC BOM GROUP
- PAGE 7: DELETED SMC_BIL_BUTTON_L NET FROM BATT SIGNAL CONN GROUP AS BIL IS NO LONGER A POR
- PAGE 8: DELETED =PP3V42_G3H_AUDIO AS IT IS NO LONGER USED
- PAGE 8: DELETED =PP3V3_S0_TPAD AS THERE IS NO KEYBOARD BACKLIGHT DRIVER
- PAGE 8: DELETED =PP3V42_G3H_5V3V3_EN AS IT IS NO LONGER USED
- PAGE 9: ADDED 3 ADDITIONAL TALL POGO PINS AS PER NEW MCO AND DELETED ZS0909 SHORT POGO AS IT WAS EXTRA
- PAGE 9: ADDED TP ALIASES TO IMVP6_VR_TT AND IMVP6_NTC
- PAGE 34: ADDED LC FILTER (L3406 AND C3432) ON PP3V3_S3_BT POWER RAIL AS PER JOHN SCHEN'S FEEDBACK
- PAGE 34: REPLACED THE AIRPORT CONNECTOR WITH 1.8 MM HEIGHT CONNECTOR APN 516S0582
- PAGE 39: REPLACED ETHERNET CONNECTOR WITH THAT OF M97A/K24 PART APN 514-0636 (SYNC'ED WITH K24)
- PAGE 45: RENAMED =PP5V_S0_HDD_R TO PP5V_S0_HDD_R (AS PER UNALIASED.LST REPORT)
- PAGE 50: ADDED UNUSED NET ALIAS FOR SMC_BIL_BUTTON_L (NC_SMC_BIL_BUTTON_L)
- PAGE 52: DELETED TERM BIL FROM SMC BATTERY & BIL CONNECTIONS
- PAGE 57: ADDED PLACEMENT NOTES TO C5702 AND C5704 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 59: REPLACED SMS PART WITH THE NEW BOSCH BMA141 ANALOG PART. ADDED R5923 10K PU RESISTOR ON SEL1 SIGNAL AND REMOVED 10K PD ON ST PIN. REPLACED C5926 WITH 0.01UF CAP AS PER DATA SHEET. AND, REPLACED C5923-C5925 CAPS WITH 0.033 UF VALUES FOR CUT-OFF FREQUENCY OF ~146HZ
- PAGE 60: CORRECTED PLACEMENT NOTE ASSOCIATED TO XW6080 TO REFLECT D9710 INSTEAD OF D9701
- PAGE 69: CHANGED L6995 TOB APN 152S1017 FOR COT SAVING AND EFFICIENCY
- PAGE 69: REMOVED BIL CIRCUIT AS IT NO LONGER A POR [R6960, C6954, D6951, C6953, C6952, J6955, C6951]
- PAGE 70: MOVED C7028 TO PPVBAT_G3H_CHGR_REG AS PER JOHN SCHEN'S FEEDBACK
- PAGE 70: ADDED PLACEMENT NOTE TO C7027 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 70: REPLACED R7080 WITH APN 107S0142 WHICH IS TRUE 4-TERMINAL SENSE RESISTOR WITH SMALLER PACKAGE (DAYU'S RECOMMENDATION)
- PAGE 70: ADDED BOM OPTION 6259_YES TO R7050 AND 6259_NO TO U7060 AND AMON PULLDOWN LOGIC CIRCUIT COMPONENTS. TURNED ON 6259_NO, FOR NOW, ON PAGE 4 TABLE
- PAGE 72: CONNECTED SMC_PM_G2_EN SIGNAL TO EN0 PIN 13 OF U7200 VIA A 100K RESISTOR FOR KEEPING THE POWER SUPPLY OFF IN CASE IF SMC TURNS OFF
- PAGE 72: ADDED PLACEMENT NOTE TO C7230 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 72: REMOVED NOSTUFF'ED C7251 AS PER DAYU
- PAGE 73: REPLACED C7307,C7308 WITH APN 138S0654 (ADDS ADDITIONAL AVL FOR SUPPLY REDUNDANCY)
- PAGE 73: ADDED PLACEMENT NOTE TO C7333 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 73: DELETED NOTES AT THE BOTTOM RIGHT AFTER CONSULTING WITH DAYU
- PAGE 73: MOVED C7344 NEXT TO R7350 AND ADDED PLACEMENT NOTE (JOHN SCHEN WANTED IT TO BE NEXT TO L7320 DAYU PERFERRED IT TO BE AFTER THE SENSE RESISTOR
- PAGE 74: ADDED PLACEMENT NOTES TO C7419,C7422 AND C7423 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 74: STUFFED C7432 AS PER DAYU
- PAGE 74: REMOVED C7400, C7402, R7451 AND R7452 AS PER DAYU
- PAGE 75: ADDED PLACEMENT NOTE TO C7563 AS PER JOHN SCHEN'S FEEDBACK
- PAGE 74: CHANGE L7400 AND L7401 TO 152S1019 AS PER DAYU FOR COST SAVING. ALSO, UPDATED ASSOCIATED TEXTS
- PAGE 75: MOVED C7569 TO PPMCPCORE_S0_R AS PER JOHN SCHEN'S FEEDBACK
- PAGE 90: ADDED EMI CAPS (C9017-C9025) ON I2C, LED_RETURNS AND LCD_BKLT POWER RAILS GOING TO LVDS. ADDED PLACEMENT NOTES TOO
- PAGE 94: REPLACED C9486 WITH APN 138S0654 (ADDS ADDITIONAL AVL FOR SUPPLY REDUNDANCY)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 5.0.0
-PG. 67, CHANGED U6700 CB INPUT TO BE CONTROLLED BY CS4206 GPIO0.
-PG. 62, CHANGED TP_AUD_GPIO_0 TO AUD_GPIO_0.
-PG.66, REPLACED THE LM48310'S (U6610/20/30) WITH LM48311'S
-PG. 67, CONNECTED HP OUTPUTS TO NC OF U6700 AND LINE INPUTS TO NO OF U6700.
-PG. 68, CHANGED AUD_PORTB_DET_L TO AUD_PORTA_DET_L.
-PG. 68, CHANGED AUD_PORTG_DET_L TO AUD_PORTB_DET_L.
-PG. 67, SET MIN. LINE AND NECK WIDTHS FOR AUD_CONN_L AND AUD_CONN_R

PAGES SYNCED FROM K24 SINCE LAST RELEASE 5.0.0
- PAGE 25: CHANGED C2500,C2501,C2502,C2503,C2515,C2520,C2528,C2540,C2580,C2582,C2584,C2586,C2588, C2595 TO 138S0653
- PAGE 26: CHANGED C2615,C6210 TO 138S0653
- PAGE 77: CHANGED U7740 TO 500MA 1.05V LDO

3/17/2009: RELEASE 7.0.0 (RFA)-
- ADDED PLACEMENT NOTES (ATTRIBUTE) TO ALL XW SHORTS
- PAGE 4: DELETING ENTRIES FOR 107S0138 AND 107S0139 FROM ALTERNATES PARTS TABLE AS THEY WOULD BE REPLACING THE 107S0074/75 PARTS
- PAGE 7: RENAMED PP5V_S3_BTCAMERA_F WITH PP3V3_S3_BT_F
- PAGE 7: DELETED PP5V_S0, PP5V_S3 AND ADDED PP5VRT_S0,PP5VLT_S0, PP5VRT_S3, PP5VLT_S3 DEBUG VOLTAGE TEST POINTS
- PAGE 7: ADDED PPBUS_R_G3H DEBUG VOLTAGE TEST POINT
- PAGE 8: DELETED ALIAS =PP1V05_S0_SMC_LS AS IT IS NO LONGER NEEDED
- PAGE 9: REMOVING 2 EXTRA TALL POGO PINS (ZS0911, ZS0912) AS PER NEW MCO
- PAGE 9: REPLACED 5 SHORT POGO PINS WITH MEDIUM ONES AND ADDED THREE EXTRA MEDIUM ONES (TOTAL MEDIUM POGO PINS = 8) AS PER NEW MCO
- PAGE 34: REPLACE Q3450 WITH TPCP8102 APN 376S0778 PART, SIMILAR TO K24
- PAGE 45: REPLACE Q4590 WITH TPCP8102 APN 376S0778 PART, SIMILAR TO K24
- PAGE 52: DELETE J6955 REFERENCE AS THERE IS NO BIL CONNECTOR
- PAGE 52: REMOVED REFERENCES TO THE LED BACKLIGHT AS FREESCALE PART DOESN'T HAVE I2C BUS ACCESS
- PAGE 54: REPLACING R5492 WITH APN 107S0139 PART FOR COST SAVING
- PAGE 59: REMOVING R5923 AND ONLY 1 PU ON SEL LINES IS ENOUGH
- PAGE 70: REPLACING R7020 WITH APN 107S0138 PART FOR COST SAVING
- PAGE 70: REPLACING R7008 WITH APN 107S0139 PART FOR COST SAVING
- PAGE 70: R7080 PIN SWAP (MIRRORED HORIZONTALLY) AS PER LAYOUT ENGINEER
- PAGE 73: R7350 PIN SWAP (MIRRORED HORIZONTALLY) AS PER LAYOUT ENGINEER
- PAGE 79: REPLACE Q7940 AND Q7948 WITH TPCP8102 APN 376S0778 PART, SIMILAR TO K24
- PAGE 90: REMOVED EMI CAPS [C9017-C9025] ON LED RETURN, I2C AND LCD BKLT POWER NETS
- PAGE 90: UPDATED LVDS CONNECTOR PINOUT CONNECTIONS AS PER STEVE'S NEW SPREADSHEET
- PAGE 97: ADDED DIDIT=TRUE ATTRIBUTE TO THE SWITCHING NODE PINS 3 & 4
- PAGE 97: CHANGED C9711 FROM 0.1UF TO 1.0UF 0603 TYPE CAP AS PER FREESCALE FEEDBACK
- PAGE 97: CHANGED C9715 AND C9716 TO 50V CAPS FOR COST SAVING AND AS PER FREESCALE FEEDBACK
- PAGE 97: CHANGED R9717 - R9722 FROM 0.1% TO 1% PARTS FOR COST SAVINGS AND AS PER FREESCALE FEEDBACK
- PAGE 97: NO STUFF'ED C9721 - C9726 AS PER FREESCALE FEEDBACK
- PAGE 97: FOR 25KHZ OPERATION, CHANGE R9726 TO NO STUFF, INTERCHANGE R9705(6.8K) WITH C9705 AS IN K19I
- PAGE 97: CHANGED R9710 TO 6.65K APN 114S0298 AND R9716 TO 226K APN 114S0445 PARTS AS PER FREESCALE FEEDBACK
- PAGE 107: ADDED CONSTRAINTS FOR FOLLOWING SENSOR NETS: ISNS_HDD_P/ISNS_HDD_N; ISNS_ODD_P/ISNS_ODD_N; ISNS_AIRPORT_P/ISNS_AIRPORT_N; ISNS_1V5_S3_P/ISNS_1V5_S3_N; ISNS_LCDBKLT_P/ ISNS_LCDBKLT_N
- PAGE 107: REMOVED FOLLOWING SENSOR NETS CONSTRAINTS: ISNS_P1V5S0MCP_P/ISNS_P1V5S0MCP_N; ISNS_PVCORES0MCP_P/ISNS_PVCORES0MCP_N
- PAGE 74: ADDED XW7401-XW7404 SHORTS ACROSS L7400 AND L7401

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 6.0.0
-PG. 67, DELETED R6725 AND NET =PP3V42G3H_AUDIO
-PG. 66, ADDED R6613/14/15/16/17
-PG. 66, ADDED C6612/13
-PG. 66, ADDED R6631/2/3/4/5
-PG. 66, ADDED C6634/5
-PG. 66, CHANGED C6610/11 TO 0.022UF
-PG. 66, CHANGED C6630/31 TO 0.022UF
-PG. 65, DELETED R6521
-PG. 65, ADDED R6523/4
-PG. 62, ADDED PLACEMENT COMMENT ATTR. TO XW6200/1
-PG. 67, ADDED PLACEMENT COMMENT ATTR. TO XW6700/1/10/11
-PG. 68, ADDED PLACEMENT COMMENT ATTR. TO XW6851/80
-PG. 66, REPLACED U6610/30 WITH LM48556 CKTS
-PG. 67, DELETED C6760/1/2/3.
-PG. 67, CHANGEED J6703 TO TWO PIN CONN.
-PG. 67, ADDED J6704
-PG. 62, REPLACED C6225 WITH APN: 128S0216

3/25/2009: RELEASE 7.3.0 (MAJOR)-

- DELETED PAGE 71 (5V S3 LT POWER SUPPLY) AS THERE IS NO NEED OF A SEPARATE 5V S3/S0 SUPPLY
- PAGE 7: DELETED PP5VLT_S3 NETS
- PAGE 7: RENAMED PP5VRT_S3 TO PP5V_S3 ["LT" & "RT" NOMENCLATURE CLEAN-UP]
- PAGE 8: COMBINED 5V S3 LT AND RT ALIASES INTO ONE =PP5V_S3_REG AND RENAMED NETS (LT & RT NOMENCLATURE CLEAN-UP)
- PAGE 8: DELETED =PPVIN_S3_5VLTS3, =PP5VLT_S3_V5IN NETS
- PAGE 9: ADDED ALIAS MCP_GPIO_4 FOR MIKEY MIC LOAD DETECT CIRCUIT
- PAGE 21: UNSTUFFED R2143 PU ON MCP_GPIO_4 AS THERE IS ALREADY A 100K PU ON AUDIO PAGE
- PAGE 45: ADDED APN TEXT NOTE FOR SIL CONNECTOR
- PAGE 55: ADDED BC846BM NPN TRANSISTOR (APN 372S0129) TO MCP T-DIODE SENSOR CIRCUIT SIMILAR TO THAT IN CPU T-DIODE SENSOR AND STUFFED C5540
- PAGE 72: RENAMED NETS AND NOTES TO REMOVE REFERENCES TO RT POWER SUPPLY
- PAGE 72: REPLACED L7260 WITH APN 152S0959 AS PER DAYU
- PAGE 72: ADDED C7282 APN 128S0218 IN PARALLEL WITH C7280 AS PER DAYU
- PAGE 73: REPLACED Q7320 AND Q7321 WITH CSD58858 APN 376S0790 MOSFETS AS PER DAYU
- PAGE 74: REPLACED C7433 AND C7431 WITH 0.001UF CAPS APN 132S1035
- PAGE 75: REPLACED C7576 WITH 0.022UF APN 132S0102 CAP TO INCREASE THE SLEW RATE
- PAGE 75: ADDED A NOTE OCP=14.5A TO R7575
- PAGE 75: REPLACED Q7560 AND Q7565 WITH CSD58858 APN 376S0790 MOSFETS AS PER DAYU
- PAGE 76: CORRECTED MAX OUTPUT NOTE TO REFLECT 7.2A INSTEAD OF 8A
- PAGE 76: REPLACED Q7620 WITH 2 CSD58858 APN 376S0790 MOSFETS AS PER DAYU
- PAGE 77: ADDED P1V05S0_LDO_PGOOD POWER GOOD SIGNAL VIA A 0 OHM RESISTOR TO PIN 3 (PG) OF THE LDO
- PAGE 78: DELETED P5V_LTS3_PGOOD AS THERE IS NO 5V LT POWER SUPPLY ANYMORE
- PAGE 78: RENAMED =P5VRTS3_EN_L TO =P5VS3_EN_L
- PAGE 78: ROUTED P1V05S0_LDO_PGOOD POWER GOOD SIGNAL TO THE WIRED AND CIRCUIT

3/26/2009: RELEASE 7.4.0 (MAJOR)-

- PAGE 60: REPLACED DUAL PACKAGE OPA330 OPAMPS WITH SINGLE PACKAGE ONES - APN 353S2179 [U6030, U6031, U6040, U6041]. ALSO, ADDED C6031 & C6041
- PAGE 9: DELETED EXTRA MEDIUM POGO PIN ZS0912 AND SCREW HOLES Z0908, Z0909

3/26/2009: RELEASE 7.5.0 (MAJOR)-

- PAGE 73: ADDED SHORT XW7304 FROM PIN 1 OF C7300 TO POWER GND (PIN 18)
- PAGE 72: REPLACED C7282 WITH OSCON APN 128S0248 IN PARALLEL WITH C7280 AS PER DAYU

3/26/2009: RELEASE 7.6.0 (MAJOR)-

- ADDED PLACEMENT NOTES TO XW SHORTS AS PER DAYU
- ADDED OMIT BOM OPTION TO ALL THE XW SHORTS
- ADDED DIDT=TRUE ATTRIBUTE TO BOOT/VBST SIGNALS OF ALL THE SWITCHING SUPPLIES
- PAGE 8: DELETED =PP3V42_G3H_BATT AS THERE IS NO BIL CONNECTOR
- PAGE 8: ADDED =PP3V42_G3H_HALL FOR THE HALL EFFECT CONNECTOR
- PAGE 8: ADDED =PP3V3_S3_AUDIO ALIAS NET FOR CASEY'S NEW CHANGES BELOW
- PAGE 8: DELETED =PP3V42_G3H_PPBUSAISNS AS PPBUS SENSE CIRCUIT HAS BEEN REMOVED
- PAGE 8: RENAMED ALIAS =PP5V_S3_P5VS0FET TO =PP5V_S3_P5VLTS0FET AS THIS GOES TO 5V LT S0 FET CIRCUIT
- PAGE 8: ADDED =PP5V_S3_P5VRTS0FET ALIAS, GOING TO 5V RT S0 FET CIRCUIT
- PAGE 8: ADDED PLACEMENT NOTE TO Q5502
- PAGE 9: ADDED OMIT ATTRIBUTE TO THE LVDS HOLE
- PAGE 69: ADDED HALL EFFECT CONNECTOR CIRCUIT J6955 APN 516S0787
- PAGE 79: RENAMED INPUT VOLTAGE NETS OF 5V S0 FET CIRCUITS TO REFLECT RT AND LT (MATCHES UPDATED ALIASES ON PAGE 8)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 7.5.0
-PG. 67, ADDED R6725
-PG. 67 ADDED =PP3V3_S3_AUDIO NET
-PG. 67, DELETED L6706
-PG. 67, ADDED XW6702
-PG. 66, UPDATED 5V S3 ALIAS NOTES
-PG. 67, NO STUFFED R6724

3/29/2009: RELEASE 8.0.0 (RFA)-

- PAGE 7: SCRUBBED THROUGH THE FUNCTIONAL TEST POINTS AGAINST TOM'S SPREADSHEET
- PAGE 7: RENAMED RIGHT CLUTCH CONNECTOR TO X16 WIRELESS CONNECTOR
- PAGE 7: DELETED BATT SIGNAL CONN AND ADDED HALL EFFECT CONNECTOR TEST POINTS
- PAGE 7: DELETED THERMAL FUNC TEST SECTION
- PAGE 9: ADDED TP_ ALIASES FOR - CARDREADER_RESET, USB_CARDREADER_N/P, AND USB_IR_N/P
- PAGE 9: FIXED BAD TP NC NETS - TP_RTL8211_CLK125, TP_PP3V3_ENET_PHY_VDDREG
- PAGE 9: DELETED Z0912 MLB MOUNTING HOLE AS NO LONGER NEEDED
- PAGE 34: RENAMED TITLE: RIGHT CLUTCH CONNECTOR TO X16 WIRELESS CONNECTOR
- PAGE 50: REPLACED R5030 WITH APN: 114S0114,(IT'S A 1% TOL, 1/16W, 0402, 84.5OHM RESISTOR)
- PAGE 66: FIXED UNNAMED NETS CONNECTED TO - R6632
- PAGE 74: FIXED UNNAMED NETS CONNECTED TO - XW7401, XW7402, XW7403 AND XW7404
- PAGE 78: FIXED BAD TP NC NETS - TP_DDRREG_PGOOD
- PAGE 76: REPLACED L7620 WITH ITS REPLACEMENT - APN 152S0518
- PAGE 69: CHANGE PIN OUTS OF J6955 AS PER CHINMAY

3/31/2009: RELEASE 9.0.0 (RFA)-

- PAGE 4: DELETED DEBUG_SENSE BOM OPTION AND ADDED MEM_SENSE AND 1P05_HIGH_SIDE_SENSE OPTIONS UNDER K84_COMMON BOM GROUP
- PAGE 4: ADDED MCP_T_DIODE_SENSOR, MCPSMC_DIGITEMP_NO BOM OPTIONS UNDER K84_COMMON BOM GROUP
- PAGE 4: ADDED SHORT POGO PIN 870-1699 AS ALTERNATE FOR THE MEDIUM ONES
- PAGE 4: UPDATED DESCRIPTION FOR THE CPU
- PAGE 7: UPDATED TPS AS PER NEW UPDATE FROM TOM (SPREADSHEET ATTACHED TO THE RADAR)
- PAGE 12: REPLACED C1260 WITH APN 128S0267 AS PER DAYU
- PAGE 34: DELETED TEXT NOTE ASSOCIATED WITH J3401
- PAGE 45: ADDED VOLTAGE, MIN LINE AND NECK WIDTH FOR PP5V_S0_HDD_FLT
- PAGE 52: ADDED 0 OHMS STUFFING OPTION TO CONNECT MIKEY SMBUS CONNECTIONS TO MCP SMBUS 0. ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 52: ADDED 0 OHMS STUFFING OPTION BETWEEN MIKEY AND MCP SMBUS 1 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_NO WITH THESE 0 OHMS
- PAGE 52: ADDED 0 OHMS STUFFING OPTION BETWEEN SMC_B SMBUS AND MCP SMBUS 1 CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 52: ADDED BOM OPTION MCPSMC_DIGITEMP_NO TO R5230 AND R5231
- PAGE 54: REPLACED DEBUG_SENSE BOM OPTION WITH MEM_SENSE FOR MCP MEMORY VDD CURRENT SENSE CIRCUIT AND WITH 1P05_HIGH_SIDE_SENSE FOR CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE CIRCUIT
- PAGE 55: ADDED MCP_T_DIODE_SENSOR BOM OPTION TO THE MCP T-DIODE THERMAL SENSOR CIRCUIT
- PAGE 59: DELETED R5923 FROM THE TEXT NOTE
- PAGE 60: MANUALLY UPDATED RESISTORS VALUES (VOLTAGE DIVIDERS,AMPLIFIER GAINS, RC) TO MATCH WITH K19I UPDATES, EXCEPT VOLTAGE DIVIDER FOR PP3V3_WLAN [K19I USES 5V RAIL]. FOR PP3V3_WLAN, R6010 HAS BEEN CHANGED TO 634K TO GET VDIVIDER = ~2V
- PAGE 75: ADDED C7590 (2.2UF) APN 138S0579 IN PARALLEL WITH C7563 AS PER DAYU
- PAGE 102: ADDED CONN_PCIE_MINI_R2D_P/N AND CONN_PCIE_MINI_D2R_P/N NETS IN THE CONSTRAINT SET
- PAGE 70: ADDED TP TO PIN 13
- PAGE 4: ADDED MIKEY_LOAD_DET BOM OPTION UNDER K84_MISC BOM GROUP

PAGES SYNCED FROM DAVID'S AUDIO_MLB SINCE LAST RELEASE 8.0.0
- CHANGED R6211 & R6212 FROM 39 OHMS TO 22 OHMS
- DELETED NOTE ABOVE U6500
- ADDED BOMOPTION = MIKEY_LOAD_DET ATTRIBUTE TO R6870, R6871, C6870,
- UPDATED SIGNAL PATH CHART TO INCLUDE MCP79 GPIO ASSIGNMENTS
- ADDED BOMOPTION = MIKEY ATTRIBUTE TO R6860, C6860, Q6802, R6864, R6865, & R6861 C6871, U6870, C6872, R6872, & R6873
- REMOVED NOTE RE: ROUTING TO MCP79 GPIO ABOVE U6870
- REMOVED BOMOPTION = NOSTUFF ATTRIBUTE FROM R6724
- ADDED BOMOPTION = NOSTUFF ATTRIBUTE TO R6725

4/1/2009: RELEASE 9.1.0 (MAJOR)-

- PAGE 4: CHANGED MCP P/N TO 338S0702 AS PER CHALLEE
- PAGE 52: FIXED SENSOR ADC SMBUS CONNECTIONS (BOTH SCL AND SDA WERE WRONGLY CONNECTED TO SMB_0_S0_DATA NETS
- PAGE 69: REFRESHED HALL EFFECT SENSOR WITH THE NEW SYMBOL
- PAGE 90:RE-ROUTED LED RETURN SIGNALS FOR LAYOUT FEASIBILITY(CHIP WAS MOVED TO TOP SIDE)
- PAGE 90: ADDED C9017 (1000PF) CAP AS PER JOHN SCHEN
- PAGE 97: FIXED THE LCDBKLT_VIN SIGNAL NAME ASSOCIATION TO THE CORRECT NET INSTEAD OF R9730 PIN
- PAGE 97: DISCONNECTED PGND (OF CAPS) FROM XW9700 AND ADDED A SEPARATE XW9701 SHORT TO ISOLATE NOISY PGND FROM THE SYSTEM GND. NAMED IT GND_LCDBKLT_PGND AND ASSIGNED MIN LINE/NECK WIDTH ATTRIBUTES
- PAGE 97: RENAMED GND_LCDBKLT TO GND_LCDBKLT_SGND
- PAGE 97:DISCONNECTED PINS 2 AND 5 FROM GND PINS(13,19,21)AND CONNECTED SEPARATELY TO SYSTEM GND
- PAGE 97: REPLACED D9710 WITH 40V PART- APN 371S0580 AS PER DEREK
- PAGE 97: STUFFED R9726 AND SWAPPED C9705 AND R9705 AS PER FREESCALE FOR COMPENSATION ALSO, CHANGED R9705 TO 10K 1% VALUE - APN 114S0315

4/2/2009: RELEASE 9.2.0 (MAJOR):
- PAGE 7: SCRUBBED TPS AS PER UPDATE FROM TOM
- PAGE 49: FIXED PLACEMENT NOTE ASSOCIATED WITH C4907 (SHOULD BE: PLACE NEAR PIN E1)
- PAGE 49:FIXED PLACEMENT NOTES ASSOCIATED WITH R4999,C4920(SHOULD BE:PLACE NEAR PIN M12)
- PAGE 51: FIXED PLACEMENT NOTE ASSOCIATED WITH R5146 - PLACE NEAR U5110 INSTEAD OF SMC
- PAGE 52: FIXED DUPLICATION OF MAKE_BASE=TRUE ASSOCIATED WITH SMBUS_SMC_B_S0_SCL/SDA
- PAGE 97: RENAMED SINGLE PIN NET GND_LCDBKLT TO GND_LCDBKLT_PGND

SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

PAGE TITLE
Revision History

Apple Inc.

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

4/2/2009: RELEASE 9.3.0 (MAJOR):
- PAGE 4:B ADDED 5.98MM SANYO PART 128S0288 AS ALTERNATE TO 128S0271
- PAGE 4:B ADDED 5.95MM SANYO PART 128S0286 AS ALTERNATE TO 128S0248
- PAGE 4: DELETED 152S0694 ALTERNATE ENTRY FOR 152S0138 AS IT IS NOT USED
- PAGE 50: REPLACED DUAL Q5032 FET WITH TWO SINGLE Q5032 & Q5033 (APN 376S0612)
- N-CH FETS FOR ROUTING PURPOSES (TIL AMODE SIGNAL)
- PAGE 54:B CHANGED R5412 TO 118OHM (111S0071)
- PAGE 97: ADDED MIN_LINE/NECK_WIDTH ATTRIBUTES TO 5V_S3_DRVL, 3V3S5_VBST, 3V3S5_DRVL (LINKED THE NET NAME). ADDED UNDERSCORE TO THE SMBUS
- PAGE 75: CHANGED L7560 TO APN 152S0526 - 0.68UH, 3.5MOHM,16A - AS PER DAYU
- PAGE 75: CHANGED R7569 TO 11.3K APN 114S0319 FOR SETTING THE CORRECT OCSET AS PER DAYU
- PAGE 97: CHANGED MIN_NECK_WIDTH ASSOCIATED WITH PPVOUT_S0_LCDBKLT TO 0.24MM AS THAT'S THE PIN WIDTH
- PAGE 97: CHANGED MIN_LINE/NECK_WIDTH ASSOCIATED WITH GND_LCDBKLT_SGND TO 0.6/0.24MM

PAGES SYNCED FROM DAVID'S AUDIO MLB SINCE LAST RELEASE 9.2.0
- REMOVED R6725 AND =PP3V3_S3_AUDIO CONNECTION TO MAX14504 ANALOG SWITCH

4/2/2009: RELEASE: 9.4.0 (MAJOR):
- PAGE 97: ADDED A 1000PF CAP (C9727) ON LCDBKLT_VIN NEAR PIN 1
- PAGE 97: REPLACED C9717 WITH 1000PF CAP APN 13ZS0147 AND ADDED PLACEMENT NOTE AS PER JOHN SCHEN

4/2/2009: RELEASE: 9.5.0 (MAJOR):
- PAGE 9: REPLACED Z0906,Z0907,Z0910 AND Z0911 MLB MOUNTING HOLES WITH 2.7 MM DIAMETER PLATED HOLES - APN 998-1584

4/3/2009: RELEASE: 9.6.0 (MAJOR):
- PAGE 4: UNDER K84_PROGPARTS BOM GROUP, REPLACED BLANK P/N WITH PROGRAMMED P/N
- PAGE 9: ADDED GLOBAL DIGITAL GROUND NET WITH MIN_LINE/NECK_WIDTH AND VOLTAGE ATTRIBUTES
- PAGE 9: REPLACED Z0905 AND Z0913 MLB MOUNTING HOLES WITH 2.7 MM DIAMETER PLATED HOLES - APN 998-1584
- PAGE 9: DELETED GND MIN_LINE/NECK_WIDTH AND VOLTAGE ATTRIBUTES FROM FAN STANDOFF

PAGES SYNCED FROM LENG'S AUDIO MLB SINCE LAST RELEASE 9.5.0*
- REMOVED OPTIONAL STUFF-AROUND RESISTORS FOR ANALOG SWITCH
- CONNECT AUDIO JACK SHIELD TO DIGITAL GROUND.

4/3/2009: RELEASE: 10.0.0 (RFA):
- PAGE 9: ADDED 7 EXTRA TALL POGO PINS FOR EMI - 4 STUFFED AT THE BOTTOM, 3 UNSTUFFED ON THE TOP
- PAGE 28: DELETED MAKE_BASE=TRUE ASSOCIATED WITH PCIE_RESET_L
- PAGE 52: FIXED DUPLICATION OF MAKE_BASE=TRUE ASSOCIATED WITH I2C_MIKEY_SCL/SDA_R
- PAGE 69: REFRESHED J6955 SYMBOL - APN 516S0787
- PAGE 78: DELETED MAKE_BASE=TRUE ASSOCIATED WITH ALL_SYS_PWRGD
- PAGE 78: DELETED SYNONYMS AS THEY ARE NOT NEEDED ANYMORE (DUE TO 0 OHMS)

PAGES SYNCED FROM LENG'S AUDIO MLB SINCE LAST RELEASE 9.6.0*
- ADDED 100PF EMC CAP ON THREE SPEAKER CONNECTORS.
- CHANGED MIN_WIDTH OF CODEC HP OUT NETS.

4/5/2009: RELEASE 10.1.0 (MAJOR):

- PAGE 4: ADDED CHGR_6258 BOM OPTION UNDER MODULE PARTS TABLE AND TO K84 MISC BOM GROUP. THIS IS TO STUFF ISL6258 PART
- PAGE 9: ADDED ONE MORE TALL POGO PIN ON BOTTOM SIDE
- PAGE 51: FIXED THE NOTE ON THE XDP PAGE- REPLACING 920-0620 ADAPTER BOARD WITH 922-0782 ADAPTER FLEX
- PAGE 34: RENAMED P3VWLAN_SS NET TO P3V3WLAN_SS
- PAGE 46: DELETED TEXT NOTE RELATED TO R4691 & R4690 AS IT IS NA TO K84
- PAGE 52: MOVED THE R5251 CONNECTION TO SENSOR ADC TO THE RIGHT SIDE TO SHOW A SEPARATE CONNECTION FOR CLARITY
- PAGE 52: DELETED TEXT NOTE ON BATTERY LED DRIVER AS IT IS NA TO K84
- PAGE 69: PUT R6961 BEFORE C6955 TO GET RC FILTER. ALSO, FOR NOW, REPLACED R6961 WITH A 0 OHM RESISTOR AND NOSTUFF'ED C6955
- PAGE 70: ADDED OMIT BOM OPTION TO U7000 AS THIS PART WILL GET STUFFED WITH EITHER ISL6258 OR ISL6259 DEPENDING UPON PAGE 4 BOM TABLE
- PAGE 70: FIXED Q7001 DRAIN-SOURCE ORIENTATION

4/6/2009 - RELEASE 10.1.1 (MINOR):

SCHEMATIC AND BOM CLEAN-UP
- PAGE 4: DELETED CHGR_6258 AND RENAMED 6259_NO TO CHGR_6259_NO. REPLACED CHGR_6258 WITH CHGR_6259_NO IN MODULE_PARTS_TABLE
- PAGE 4: DELETED ENTRIES IN THE ALTERNATE BOM TABLE FOR THE FOLLOWING APN: 516-0213 AND 516S0709
- PAGE 8: DELETED =PP3V3_S3_AUDIO ALIAS AS IT IS NO LONGER APPLICABLE
- PAGE 57: DELETED NO_TEST = TRUE ATTRIBUTE FROM J2_SCLK AND J2_MOSI AS THEY CONFLICT WITH FUNC_TEST ATTRIBUTE ON PAGE 7
- PAGE 69: RENAMED 6259_NO/YES TO CHGR_6259_NO/YES

4/6/2009 - RELEASE 11.0.0 (OK2FAB):

- NO CHANGE SINCE LAST MINOR RELEASE 10.1.1

4/7/2009 - RELEASE 12.0.0 OK2FAB (RFA):
- NO CHANGE SINCE LAST RFA RELEASE 11.0.0
THIS IS A RESUBMIT AS PREVIOUS RFA DIDNT GO THROUGH

4/23/2009 - RELEASE 12.1.0 (MAJOR):
- PAGE 4: ADDED METAL PART ALTERNATES FOR USB AND MINI DP CONNECTORS. ALSO ADDED CORRESPONDING NOTES-
  514-0691 ALTERNATE FOR 514-0690;
  514-0689 ALTERNATE FOR 514-0688
- PAGE 13: REPLACED J1300 XDP CONNECTOR WITH MORE ROBUST CONNECTOR APN 998-2515
- PAGE 39: REPLACED J3900 ETHERNET CONNECTOR WITH POR PLASTIC CONNECTOR APN 514-0692
- PAGE 46: REPLACED J4600 & J4610 USB CONNECTORS WITH POR PLASTIC CONNECTOR APN 514-0688
- PAGE 75: CHANGE Q7560 AND Q7565 TO SIS426 APN 376S0749 PER RDAR://6812904
- PAGE 75: CHANGE R7565 TO 10HM APN 113S0023 PER RDAR://6812904
- PAGE 76: CHANGED THE CPU VTT OVER CURRENT TRIP POINT PER RDAR://6792329 BY CHANGING R7604 FROM 8.97KR1 TO 6.04KR1
- PAGE 94: REPLACED J9400 DP CONNECTOR WITH POR PLASTIC CONNECTOR APN 514-0690
- PAGE 75: CHANGED C7565 AND C7568 TO CASE_B4_SM PACKAGE FROM CASE_B2_SM DUE TO PACKAGING ERROR (SAME APN)

4/24/2009 - RELEASE 12.2.0 (MAJOR):

PAGES SYNCED FROM CASEY'S AUDIO MLB SINCE LAST RELEASE 12.1.0*
- REPLACED J6700 WITH APN# 514-0694
- ADDED DZ 6702 AND L6706
- CONNECTED R6860 TO AUD_IP_PERPH_DET

4/27/2009 - RELEASE 12.3.0 (MAJOR & WEEKLY ECO):
- PAGE 4: ADDED NEW BOM ENTRY 639-0254 FOR MOLEX DDR3 CONNECTOR CONFIG. ALSO, EDITED 639-0035 BOM NAME TO REFLECT FOXCONN DDR3 CONNECTOR. ADDED TWO ENTRIES (J3200 AND J3100) FOR FOXCONN AND TWO FOR MOLEX UNDER MODULE PARTS TABLE .
- PAGE 74: CHANGED C7432 TO 0.001UF AS PER RDAR://6792327
- PAGE 74: UNSTUFFED C7434 AS PER RDAR://6792327
- PAGE 74: CHANGED C7428 TO 0.47UF AS PER RDAR//6792327
- PAGE 74: CHANGED R7415 TO 10.5K AS PER RDAR://6792327
- PAGE 97: CHANGED R9716 FROM 226K TO 243K TO CHANGE THE OVP POINT TO 35.3V AS PER KIRAN

4/28/2009: RELEASE 12.4.0 (MAJOR):

- PAGE 67: ADDED 0603_FERRITE_PLACEHOLDERS APN 155S0367 ON RIGHT PIEZO SPEAKER FOR EMI PURPOSES - L6707 & L6708

4/28/2009: RELEASE 12.5.0 (MAJOR):
- PAGE 67: MOVED L6707 & L6708 TO J6703 (FULL RANGE SPEAKER CONNECTOR) BETWEEN CAPS AND CONNECTOR

4/29/2009: RELEASE 12.6.0 (MAJOR & WEEKLY ECO):

- PAGE 67: ADDED 0603_FERRITE_PLACEHOLDERS APN 155S0367 ON RIGHT PIEZO SPEAKER J6704 FOR EMI PURPOSES - L6709 & L6710
- PAGE 971: CHANGED L9710 TO A BIOGER 2525 PACKAGE (LOW DCR) APN 152S0585 FOR BETTER EFFICIENCY

4/29/2009: RELEASE 12.7.0 (MAJOR & WEEKLY ECO):
- PAGE 97: CHANGED L9710 BACK TO THE ORIGINAL APN 152S0826 AS 2525 PACKAGE CAN'T FIT IN

5/01/2009: RELEASE 12.8.0 (MAJOR):
- PAGE 4: ADDED A36 BEE NUMBER FOR NEW BOM CONFIGURATION 639-0254
- PAGE 60: ADDED 0 OHMS SERIES RESISTORS R6003 AND R6004 ON AVDD AND DVDD SUPPLY RAILS TO ADC CHIP
- PAGE 60: CHANGED R6001 & R6002 TO 33 OHMS RESISTORS TO FIX UNDERSHOOT ON I2C BUS

05/01/2009: RELEASE 12.9.0 (MAJOR):

- PAGE 4: UPDATED PLASTIC PART ALTERNATES FOR USB AND MINI DP CONNECTORS. ALSO ADDED CORRESPONDING NOTES-
  514-0690 PLASTIC ALTERNATE FOR 514-0691 METAL;
  514-0688 PLASTIC ALTERNATE FOR 514-0689 METAL
- PAGE 46: REPLACED PLASTIC USB CONNECTORS WITH METAL APN 514-0689 PARTS
- PAGE 94: REPLACED PLASTIC MINI DP CONNECTOR WITH METAL APN 514-0691 PART

05/04/2009: RELEASE 12.10.0 (MAJOR):
- PAGE 4: REMOVED SHORT POGO PIN ALTERNATE
- PAGE 21: REVERTING MCP TO EARLIER USE APN 338S0710
- PAGE 60: CHANGED U6050 INA 211 PART TO 200X GAIN INA 210 APN 353S2073

05/05/2009: RELEASE 12.11.0 (MAJOR & WEEKLY ECO):
- PAGE 4: ADDED 4 QUANTITIES OF DIMM CONNECTOR SCREWS APN 452-1708
- PAGE 46: ADDED NOTE ABOUT USING METAL PART'S SCHEMATIC AND CAD SYMBOLS THOUGH POR IS PLASTIC USB CONNECTOR PART
- PAGE 94: ADDED NOTE ABOUT USING METAL PART'S SCHEMATIC AND CAD SYMBOLS THOUGH POR IS PLASTIC MINI DP CONNECTOR PART

05/08/2009: RELEASE 12.12.0 (MAJOR & WEEKLY ECO):

- PAGE 4: DELETED SANYO 6.00MM OSCON CAPS 128S0248 & 128S0271 FROM THE ALTERNATE TABLE (MAKING ALTERNATES AS PRIMARY)
- PAGE 4: TURNING ON BOM OPTION MCPSMC DIGITIMES YES AS POR IS TO CONNECT MIKEY TO MCP70 SMBUS 1 INSTEAD OF SMBUS 1 AND TO CONNECT SMC'S SMBUS TO SMBUS 2
- PAGE 4: ADDED A TEXT NOTE STATING THAT ADC CAN ONLY WORK IN S0 STATE AS IT HAS I2C BUS PU TO S0 POWER RAIL
- PAGE 37: CHANGED C3714 AND C3715 TO 2.2UF APN 138S0642 TO FIX ETHERNET JITTER ISSUE
- PAGE 50: CHANGED R5030 TO 63.4 OHMS APN 114S0102 TO INCREASE THE SIL CURRENT PER RDAR://PROBLEM/6752822
- PAGE 50: CHANGED R5712 TO 0 OHM APN 116S0004 PER RDAR://PROBLEM/6752822
- PAGE 52: CHANGED R5200, R5201, R5260 & R5261 TO 2K APN 116S0073
- PAGE 72: REPLACED C7252, C7291 & C7292 WITH 5.95MM SANYO APN 128S0288
- PAGE 73: REPLACED C7240 & C7282 WITH 5.95MM SANYO APN 128S0286
- PAGE 73: REPLACED C7331 & C7345 WITH 5.95MM SANYO APN 128S0286
- PAGE 77: CHANGED C7771 TO 47UF APN 138S0659 TO FIX ETHERNET JITTER ISSUE

05/10/2009: RELEASE 12.13.0 (MAJOR & WEEKLY ECO - THRU' EMAIL):
- PAGE 60: CHANGED R6003 AND R6004 TO 10 OHMS 5% RESISTOR VALUES RDAR://PROBLEM/6834630

05/11/2009: RELEASE 12.14.0 (MAJOR & WEEKLY ECO - THRU' EMAIL):

- PAGE 57 : CHANGED R5714 TO 165 OHMS APN 114S0141 AS PER RDAR://PROBLEM/6872938
- PAGE 72 : CHANGED C7252, C7291 & C7292 BACK TO ORIGINAL APN 128S0271

05/20/2009: AGILE RELEASE PROTO 2 OK2FAB 13.0.0 (FAB):

- FINAL PROTO 2 OK2FAB RELEASE
- UPDATED PAGE BORDERS TO NEW E4 DSIZE STANDARDS

05/22/2009: AGILE RELEASE PROTO 2 OK2FAB 14.0.0 (FAB)-

RETRY
- FINAL PROTO 2 OK2FAB RELEASE
- UPDATED PAGE BORDERS TO NEW E4 DSIZE STANDARDS

06/09/2009: RELEASE 14.1.0 (MAJOR)-
- PAGE 4: REMOVING CHGR_6259_NO BOM OPTION AS ISL 6259 IS NOT POR
- PAGE 4: ADDED NEW ISL PART APN 353S2718 AS AN ALTERNATE TO FIX B4 DONGLE ISSUE
- PAGE 9: REPLACED ALL MEDIUM POGO PINS WITH APN 870-1794 (2 MM) AND Z0916-2S0918 WITH THINNC APN 870-1820 (2 MM) ONES
- PAGE 59: ADDED 5922 10 OHMS SERIES R ON VDD SUPPLY TO FIX SMS NOISE ISSUE
- PAGE 67: CHANGED J6704 TO A THREE PIN CONNECTOR 518S0520
- PAGE 69: REFRESHED J6955 SYMBOL (HALL EFFECT CONNECTOR)
- PAGE 70: REMOVED CHGR_6259_YES/NO BOM ATTRIBUTES AS ISL 6259 IS NOT POR
- PAGE 70: DELETED R7057 & R7053 CHGR_6259_YES BOM OPTIONS COMPONENTS
- PAGE 70: REPLACING R7052 & R7054 CHGR_6259_NO BOM OPTION COMPONENTS WITH XW SHORTS- XW7052 & XW7054
- PAGE 70: REMOVED R7058 CHGR_6259 YES COMPONENT AS IT IS NOT NEEDED WITH 6258 (PH_SUB_S3_R DIRECTLY CONNECTS TO Q7058 PIN)
- PAGE 94: STUFFED C9485 AND CHANGED IT TO 22UF (APN 138S0654). CHANGED C9400 & C9481 TO 4.7UF (APN 138S0618) & CHANGED C9480 TO 220F (APN 138S0654): TO FIX B4 DONGLE ISSUE

PAGES SYNCED FROM CASEY HARDY'S AUDIO MLB SINCE LAST RELEASE 14.0.0
- ADDED R6862 PULL-UP RESISTOR TO PERPH_DETECT CKT.

06/10/2009: RELEASE 14.2.0 (MAJOR)-

- PAGE 4: ADDED APN 138S0661 LOW_NOISE MURATA CAPS AS ALTERNATE FOR C9715 & C9716 TO FIX LCD BKLT AUDIBLE NOISE ISSUE
- PAGE 49: ADDED 0.1UF CAPS ON SMS_X_AXIS, SMS_Y_AXIS & SMS_Z_AXIS NETS TO FIX NOISE ISSUE
- PAGE 77: CHANGED R7780 TO 25.5K APN 114S0354 & R7781 TO 80.6K APN 114S0402 AS PER DAYU

06/11/2009: RELEASE 14.3.0 (MAJOR)-
- PAGE 77: ADDED 0 OHMS BOM OPTIONS R7782 BETWEEN PIN 4 OF U7750 (SKIP PIN) AND POWER RAIL AND R7783 BETWEEN PIN 4 AND GND. R7782 WILL BE NOSTUFF FOR NOW. THIS IS AS PER DAYU TO FIX ETHERNET JITTER ISSUE

06/11/2009: RELEASE 14.4.0 (MAJOR)-
- PAGE 49: REPLACED C4950-C4952 WITH 1UF APN 138S0640 CAPS
- PAGE 78: DISCONNECTED P1V05_S5_PGOOD FROM PIN 3 OF U7840 AND CONNECTED IT TO PIN 1 (RSMRST_PWRGD) TO FIX LEAKAGE ISSUE

06/12/2009: RELEASE 14.5.0 (MAJOR)-
- PAGE 9: ADDED ONE MORE EXTRA TALL POGO PIN AS PER EMC RECOMMENDATION : 2S0920
- PAGE 78: ADDED 0 OHM BOM OPTION R7895 BETWEEN 1V05_S5_PGOOD AND RSMRST_PWRGD FOR DEBUG PURPOSES

SYNC MASTER=K24_MLB SYNC DATE=01/19/2009

PAGE TITLE: Revision History

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D
REVISION: 14.5.0
BRANCH:
PAGE: 6 OF 109
SHEET: 6 OF 77

Functional Test Points

FAN CONNECTORS FUNC_TEST

P1V	TRUE	PP5VRT_S0	7 8
P1W	TRUE	FAN_RT_PWM	43
P1Y	TRUE	FAN_RT_TACH	43

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

P2G	TRUE	BI_MIC_LO	53 54
P2H	TRUE	BI_MIC_HI	53 54
P2J	TRUE	BI_MIC_SHIELD	53 54

SPEAKER FUNC_TEST

P2K	TRUE	SPKRAMP_L_N_OUT	52 53
P2L	TRUE	SPKRAMP_L_P_OUT	52 53
P2M	TRUE	SPKRAMP_R_N_OUT	52 53
P2N	TRUE	SPKRAMP_R_P_OUT	52 53
P2P	TRUE	SPKRAMP_SUB_N_OUT	52 53
P2R	TRUE	SPKRAMP_SUB_P_OUT	52 53

LVDS FUNC_TEST

P2A	TRUE	PP3V3_LCDVDD_SW_F	7 65 (NEED 2 TP)
P2B	TRUE	PP3V3_S0_LCD_F	65
P2C	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68 (NEED 2 TP)
P2D	TRUE	LVDS_IG_DDC_CLK	18 65
P2E	TRUE	LVDS_IG_DDC_DATA	18 65
P2F	TRUE	LVDS_IG_A_DATA_N<0>	18 65 72
P2G	TRUE	LVDS_IG_A_DATA_P<0>	18 65 72
P2H	TRUE	LVDS_IG_A_DATA_N<1>	18 65 72
P2J	TRUE	LVDS_IG_A_DATA_P<1>	18 65 72
P2K	TRUE	LVDS_IG_A_DATA_N<2>	18 65 72
P2L	TRUE	LVDS_IG_A_DATA_P<2>	18 65 72
P2M	TRUE	LVDS_IG_A_CLK_F_N	65 72
P2N	TRUE	LVDS_IG_A_CLK_F_P	65 72
P2P	TRUE	LED_RETURN_1	65 68
P2R	TRUE	LED_RETURN_2	65 68
P2T	TRUE	LED_RETURN_3	65 68
P2V	TRUE	LED_RETURN_4	65 68
P2W	TRUE	LED_RETURN_5	65 68
P2Y	TRUE	LED_RETURN_6	65 68
P3A	TRUE	PP5V_S3_CAMERA_F	7 65
P3G	TRUE	USB_CAMERA_CONN_P	65 73
P3H	TRUE	USB_CAMERA_CONN_N	65 73

(NEED TO ADD 5 GND TP)

SATA ODD CONN FUNC_TEST

P2AG	TRUE	PP5V_SW_ODD	(NEED 2 TP) 7 34 47
P2AH	TRUE	SMC_ODD_DETECT	34 36
P2AJ	TRUE	SATA_ODD_D2R_C_P	34 72
P2AK	TRUE	SATA_ODD_D2R_C_N	34 72
P2AL	TRUE	SATA_ODD_R2D_P	34 72
P2AM	TRUE	SATA_ODD_R2D_N	34 72

(NEED TO ADD 2 GND TP)

SATA HDD/SIL FUNC_TEST

P3J	TRUE	PP5V_S0_HDD_FLT	(NEED 2 TP) 7 34
P3K	TRUE	SATA_HDD_R2D_P	34 72
P3L	TRUE	SATA_HDD_R2D_N	34 72
P3M	TRUE	SATA_HDD_D2R_C_P	34 72
P3N	TRUE	SATA_HDD_D2R_C_N	34 72
P3P	TRUE	SYS_LED_ANODE_R	34

(NEED TO ADD 3 GND TP)

BATT POWER CONN FUNC_TEST

P3Y	TRUE	SMBUS_SMC_BSA_SCL	39 75
P3Z	TRUE	SMBUS_SMC_BSA_SDA	39 75
P4A	TRUE	SYS_DETECT_L	55
P4B	TRUE	BATT_POS_F	55 56 (NEED 2 TP)

(NEED TO ADD 2 GND TP)

HALL EFFECT CONNECTOR FUNC_TEST

P4G	TRUE	PP3V42_G3H	7 8
P4H	TRUE	SMC_LID_R	55

X16 WIRELESS CONN FUNC_TEST

P3D	TRUE	PP3V3_S3_BT_F	30
P3E	TRUE	CONN_PCIE_MINI_D2R_P	30 72
P3F	TRUE	CONN_PCIE_MINI_D2R_N	30 72
P3G	TRUE	CONN_PCIE_MINI_R2D_P	30 72
P3H	TRUE	CONN_PCIE_MINI_R2D_N	30 72
P3J	TRUE	PCIE_CLK100M_MINI_CONN_P	30 72
P3K	TRUE	PCIE_CLK100M_MINI_CONN_N	30 72
P3L	TRUE	PP3V3_WLAN	7 30 (NEED 2 TP)
P3M	TRUE	PCIE_WAKE_L	17 30
P3N	TRUE	CONN_USB2_BT_P	30 73
P3P	TRUE	CONN_USB2_BT_N	30 73
P3R	TRUE	MINI_CLKREQ_Q_L	30
P3T	TRUE	MINI_RESET_CONN_L	30

(NEED TO ADD 2 GND TP)

IPD_FLEX_CONN FUNC_TEST

P3U	TRUE	PP3V3_S3_LDO	7 45
P3V	TRUE	PP18V5_S3	7 45
P3W	TRUE	Z2_CS_L	44 45
P3X	TRUE	Z2_DEBUG3	44 45
P3Y	TRUE	Z2_MOSI	44 45
P3Z	TRUE	Z2_MISO	44 45
P4A	TRUE	Z2_SCLK	44 45
P4B	TRUE	Z2_BOOST_EN	45
P4C	TRUE	Z2_HOST_INTN	44 45
P4D	TRUE	Z2_CLKIN	44 45
P4E	TRUE	Z2_KEY_ACT_L	44 45
P4F	TRUE	Z2_RESET	44 45
P4G	TRUE	PSOC_MISO	44 45
P4H	TRUE	PSOC_MOSI	44 45
P4J	TRUE	PSOC_SCLK	44 45
P4K	TRUE	SMBUS_SMC_A_S3_SDA	39 75
P4L	TRUE	SMBUS_SMC_A_S3_SCL	39 75
P4M	TRUE	PSOC_F_CS_L	44 45
P4N	TRUE	PICKB_L	44 45

(NEED TO ADD 2 GND TP)

KEYBOARD CONN FUNC_TEST

P4P	TRUE	PP3V3_S3	7 8
P4R	TRUE	PP3V42_G3H	7 8
P4T	TRUE	WS_KBD1	44
P4U	TRUE	WS_KBD2	44
P4V	TRUE	WS_KBD3	44
P4W	TRUE	WS_KBD4	44
P4Y	TRUE	WS_KBD5	44
P5A	TRUE	WS_KBD6	44
P5B	TRUE	WS_KBD7	44
P5C	TRUE	WS_KBD8	44
P5D	TRUE	WS_KBD9	44
P5E	TRUE	WS_KBD10	44
P5F	TRUE	WS_KBD11	44
P5G	TRUE	WS_KBD12	44
P5H	TRUE	WS_KBD13	44
P5J	TRUE	WS_KBD14	44
P5K	TRUE	WS_KBD15_CAP	44
P5L	TRUE	WS_KBD16_NUM	44
P5M	TRUE	WS_KBD17	44
P5N	TRUE	WS_KBD18	44
P5P	TRUE	WS_KBD19	44
P5R	TRUE	WS_KBD20	44
P5T	TRUE	WS_KBD21	44
P5U	TRUE	WS_KBD22	44
P5V	TRUE	WS_KBD23	44
P5W	TRUE	WS_KBD_ONOFF_L	44
P5Y	TRUE	WS_LEFT_SHIFT_KBD	44
P6A	TRUE	WS_LEFT_OPTION_KBD	44
P6B	TRUE	WS_CONTROL_KBD	44

(NEED TO ADD 1 GND TP)

POWER NETS FUNC_TEST

P2T	TRUE	PPVCORE_S0_CPU	8
P2U	TRUE	PPVCORE_S0_MCP	8
P2V	TRUE	PP0V75_S0	8
P2W	TRUE	PP1V05_S0	8
P2Y	TRUE	PP1V5_S0	8
P3A	TRUE	PP1V8_S0	8
P3B	TRUE	PP5VLT_S0	8
P3C	TRUE	PP5VRT_S0	7 8
P3D	TRUE	PP3V3_S0	8
P3E	TRUE	PP1V5_S3	8
P3F	TRUE	PP3V3_S3	7 8
P3G	TRUE	PP5V_S3	8
P3H	TRUE	PP1V1R1V05_S5	8
P3J	TRUE	PP3V3_S5	8
P3K	TRUE	PP3V42_G3H	7 8
P3L	TRUE	PPBUS_G3H	8
P3M	TRUE	PP3V3_ENET_PHY	8
P3N	TRUE	PP1V2R1V05_ENET	8
P3P	TRUE	PP3V3_G3_RTC	21 22 25
P3R	TRUE	PP3V3_WLAN	7 30
P3T	TRUE	PP5V_SW_ODD	7 34 47
P3U	TRUE	PP5V_S0_HDD_FLT	7 34
P3V	TRUE	PP3V3_S5_AVREF_SMC	36 37
P3W	TRUE	PP18V5_S3	7 45
P3Y	TRUE	PP3V3_S3_LDO	7 45
P4A	TRUE	PP3V3_LCDVDD_SW_F	7 65
P4B	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68
P4C	TRUE	PP4V5_AUDIO_ANALOG	49
P4D	TRUE	SMC_PM_G2_EN	36 57 63
P4E	TRUE	PM_SLP_S4_L	21 36 37 63
P4F	TRUE	PM_SLP_S3_L	21 32 36 56 63 67
P4G	TRUE	PP5V_S3_CAMERA_F	7 65

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC_TEST

P4K	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	55
P4L	TRUE	ADAPTER_SENSE	55

(NEED TO ADD 2 GND TP)

SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

PAGE TITLE: FUNC TEST

Apple Inc.

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"S0,S0M" RAILS

59 =PPVCORE_S0_CPU_REG (CPU VCORE PWR) — PPVCORE_S0_CPU 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 11 12
=PPVCORE_S0_CPU_VSENSE 40

61 =PPCPUVTT_S0_REG — PP1V05_S0 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 10 11 12 13
=PP1V05_S0_MCP_FSB 14 22 23
=PP1V05_S0_MCP_PEX_DVDD 8 23
=PP1V05_S0_MCP_AVDD_UF 23
=PP1V05_S0_MCP_SATA_DVDD 8 23
=PP1V05_S0_MCP_HDMI_VDD 18 24
=PP1V05_S0_VMON 63
=PP1V05_S0_MCP_PLL_UF_R 62

60 =PPMCPCORE_S0_REG (MCP VCORE AFTER SENSE RES) — PPVCORE_S0_MCP 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 22 23
=PPVCORE_S0_MCP_VSENSE 40

58 =PP0V75_S0_REG — PP0V75_S0 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP 64
=PP0V75_S0_MEM_VTT_A 27
=PP0V75_S0_MEM_VTT_B 28

64 =PP1V5_S0_FET — PP1V5_S0 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 11 12
=PP1V5_S0_VMON 63
=PP1V8R1V5_S0_MCP_MEM 16 23
=PP1V5_S0_MEM_MCP 28
=PP1V5_S0_MCP_PLL_VLDO 62

62 =PP1V8_S0_REG — PP1V8_S0 7
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD 18 24
=PP1V8_S0_AUDIO 49

62 23 =PP1V05_S0_MCP_PLL_UF — PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

64 =PP5VRT_S0_FET — PP5VRT_S0 7
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_CPUVTTS0 61
=PP5V_S0_LPCPLUS 38
=PP5V_S0_FAN_RT 43
=PP5V_S0_CPU_IMVP 59

64 =PP5VLT_S0_FET — PP5VLT_S0 7
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_DP_AUX_MUX 66
=PP5V_S0_HDD 34
=PP5V_S0_MCPREG 60
=PP5V_S0_VMON 63

64 =PP3V3_S0_FET — PP3V3_S0 7
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP 13
=PP3V3_S0_MCP 21 22 23
=PP3V3_S0_MCP_DAC_UF 24
=PP3V3_S0_MCP_VPLL_UF 24
=PP3V3_S0_ODD 34
=PP3V3_S0_SMBUS_SMC_0_S0 39
=PP3V3_S0_SMBUS_SMC_B_S0 39
=PP3V3_S0_SMBUS_MCP_0 39
=PP3V3_S0_FAN_RT 43
=PP3V3_S0_AUDIO 49 53 54
=PP3V3_S0_IMVP 59
=PP3V3_S0_LCD 65
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3R1V5_S0_MCP_HDA 21 23
=PP3V3_S0_SMC 37
=PP3V3_S0_MCPTHMSNS 42
=PP3V3_S0_CPUTHMSNS 42
=PP3V3_S0_DPCONN 67
=PPSPD_S0_MEM_A 27
=PPSPD_S0_MEM_B 28
=PP3V3_S0_PWRCTL 63
=PP3V3_S0_VMON 63
=PP3V3_S0_CPUVTTISNS 41
=PP3V3_S0_SMBUS_MCP_1 39
=PP3V3_S0_P1V8S0 62
=PP3V3_S0_MCP_PLL_VLDO 62
=PP3V3_S0_MCPDDRISNS 41

"ENET" RAILS

32 =PP3V3_ENET_FET — PP3V3_ENET_PHY 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 18 23
=PP3V3_ENET_PHY 31

32 =PP1V05_ENET_FET — PP1V2R1V05_ENET 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC 23
=PP1V05_ENET_MCP_RMGT 18 23
=PP1V05_ENET_PHY 31

PEX & SATA AVDD/DVDD aliases

23 =PP1V05_S0_MCP_PEX_AVDD MAKE_BASE=TRUE
206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0 17
=PP1V05_S0_MCP_PEX_AVDD1 17
206 mA (A01)

23 8 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 17
=PP1V05_S0_MCP_PEX_DVDD1 17
57 mA (A01)

23 =PP1V05_S0_MCP_SATA_AVDD MAKE_BASE=TRUE
127 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0 20
=PP1V05_S0_MCP_SATA_AVDD1 20
127 mA (A01)

23 8 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0 20
=PP1V05_S0_MCP_SATA_DVDD1 20
43 mA (A01)

"S3" RAILS

58 =PP1V5_S3_REG — PP1V5_S3 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_P1V5S0FET 64
=PP1V5_S3_MEM_A 27
=PP1V5_S3_MEM_B 28
=PP1V5_S3_MEMRESET 29

64 =PP3V3_S3_FET — PP3V3_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 39
=PP3V3_S3_PDCISENS 58
=PP3V3_S3_SMBUS_SMC_MGMT 39
=PP3V3_S3_VREFMRGN 26
=PP3V3_S3_WLAN 30
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_TPAD 44
=PP3V3_S3_SMS 46
=PP3V3_S3_BT 30

57 =PP5V_S3_REG — PP5V_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB 35
=PP5V_S3_CAMERA 65
=PP5V_S3_AUDIO_AMP 52
=PP5V_S3_MCPDDRFET 64
=PP5V_S3_1V5S30V75S0 58
=PP5V_S3_AUDIO 49 51 53
=PP5V_S3_P5VLTS0FET 64
=PP5V_S3_VTTCLAMP 64
=PP5V_S3_DEBUG_ISNS 47
=PP5V_S3_SYSLED 37
=PP5V_S3_TPAD 45
=PP5V_S3_ODD 34
=PP5V_S3_DEBUG_ADC_AVDD 47
=PP5V_S3_DEBUG_ADC_DVDD 47
=PP5V_S3_P5VRTS0FET 64

58 26 =PPVTT_S3_DDR_BUF — PPVTT_S3_DDR_BUF
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

"S5" RAILS

62 =PP1V05_S5_REG — PP1V1R1V05_S5 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC 22 23
=PP1V05_S5_ENET_P1V05ENETFET 32

57 =PP3V3_S5_REG — PP3V3_S5 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_S5_ROM 38 48
=PP3V3_S5_LCD 65
=PP3V3_S5_MCP 22 23
=PP3V3_S5_MCPPWRGD 25
=PP3V3_S5_PWRCTL 63
=PP3V3_S5_P1V05ENETFET 32
=PP3V3_S5_P3V3S3FET 64
=PP3V3_S5_P3V3S0FET 64
=PP3V3_S5_P1V05S5 62
=PP3V3_S5_MEMRESET 29
=PP3V3_S5_P3V3ENETFET 32
=PP3V3_S5_DP_PORT_PWR 67

"G3H" RAILS

55 =PP3V42_G3H_REG — PP3V42_G3H 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF 37
=PP3V42_G3H_SMBUS_SMC_BSA 39
=PP3V42_G3H_PWRCTL 63
=PP3V42_G3H_CHGR 56
=PP3V42_G3H_SMCUSBMUX 35
=PP3V42_G3H_TPAD 44
=PP3V3_S5_SMC 36 37
=PP3V3_S5_LPCPLUS 38
=PP3V42_G3H_RTC_D 25
=PP3V42_G3H_ONEWIRE 55
=PP3V42_G3H_HALL 55

55 =PP18V5_DCIN_CONN — PP18V5_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PP18V5_G3H_CHGR 56

56 =PPBUS_G3H — PPBUS_G3H 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_MCPCORE 60
=PPVIN_S5_1V5S30V75S0 58
=PPCPUVCORE_VTT_ISNS_R 41
(BEFORE HIGH SIDE SENSING RES.)
=PPBUS_S0_LCDBKLT 69
=PPVIN_S5_3V3S5 57
=PPVIN_S3_5VS3 57
=PPBUS_G3HRS5 40

41 =PPCPUVCORE_VTT_ISNS (AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.) — PPBUS_G3H_CPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 61
=PPVIN_S5_CPU_IMVP 59

DIGITAL GROUND
GND
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

SYNC MASTER=K24_MLB SYNC DATE=02/04/2009
PAGE TITLE
Power Aliases

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HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.5OD.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

OMIT
Z0905
3P2R2P7

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT
Z0906
3P2R2P7

OMIT
Z0907
3P2R2P7

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT
Z0911
3P2R2P7

OMIT
Z0910
3P2R2P7

LVDS CONNECTOR HOLE

OMIT
Z0913
3P2R2P7

EMI IO MEDIUM POGO PINS (870-1794)

ZS0900
2.0DIA-MED-EMI-MLB-K84

ZS0901
2.0DIA-MED-EMI-MLB-K84

ZS0902
2.0DIA-MED-EMI-MLB-K84

ZS0903
2.0DIA-MED-EMI-MLB-K84

ZS0908
2.0DIA-MED-EMI-MLB-K84

ZS0909
2.0DIA-MED-EMI-MLB-K84

ZS0911
2.0DIA-MED-EMI-MLB-K84

EMI TALL POGO PINS (870-1698)

ZS0904
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0905
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0906
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0907
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0910
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0912
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0913
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0914
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0915
2.0DIA-TALL-EMI-MLB-M97-M98

ZS0919
2.0DIA-TALL-EMI-MLB-M97-M98

EMI THINBC POGO PINS (870-1820)

ZS0917
2.0DIA-MLB-THIN-BC-K84

ZS0918
2.0DIA-MLB-THIN-BC-K84

ZS0916
2.0DIA-MLB-THIN-BC-K84

ZS0920
2.0DIA-MLB-THIN-BC-K84

PCI-E ALIASES

UNUSED GPU LANES

17	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
17	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
17	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

17	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
17	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
17	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
17	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
17	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
17	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
17	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
17	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

UNUSED FIREWIRE LANE

72 17	PCIE_FW_D2R_P	TP_PCIE_FW_D2R_P	MAKE_BASE=TRUE
72 17	PCIE_FW_D2R_N	TP_PCIE_FW_D2R_N	MAKE_BASE=TRUE
72 17	PCIE_FW_R2D_C_P	TP_PCIE_FW_R2D_C_P	MAKE_BASE=TRUE
72 17	PCIE_FW_R2D_C_N	TP_PCIE_FW_R2D_C_N	MAKE_BASE=TRUE
17	PCIE_FW_PRSNT_L	TP_PCIE_FW_PRSNT_L	MAKE_BASE=TRUE
17	FW_CLKREQ_L	TP_FW_CLKREQ_L	MAKE_BASE=TRUE
17	PCIE_CLK100M_FW_P	TP_PCIE_CLK100M_FW_P	MAKE_BASE=TRUE
17	PCIE_CLK100M_FW_N	TP_PCIE_CLK100M_FW_N	MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

20	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
20	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
20	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
20	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
20	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
20	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE
20	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
20	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
73 20	USB_CARDREADER_P	TP_USB_CARDREADER_P	MAKE_BASE=TRUE
73 20	USB_CARDREADER_N	TP_USB_CARDREADER_N	MAKE_BASE=TRUE
73 20	USB_IR_N	TP_USB_IR_N	MAKE_BASE=TRUE
73 20	USB_IR_P	TP_USB_IR_P	MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

18	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE

LVDS ALIASES

18	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC MCP79 ALIASES

14	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
19	FW_PME_L	TP_FW_PME_L	MAKE_BASE=TRUE
17	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
17	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
19	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
19	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE
21	MCP_GPIO_4	MIKEY_MIC_LOAD_DET	MAKE_BASE=TRUE, 54
17	CARDREADER_RESET	TP_CARDREADER_RESET	MAKE_BASE=TRUE

LAN ALIASES

18	=MCP_MII_RXER	MCP_MII_PD	MAKE_BASE=TRUE
18	=MCP_MII_COL		
18	=MCP_MII_CRS		

R0930
47K
5%
1/16W
MF-LF
402

DP HOTPLUG PULL-DOWN

18	=DVI_HPD_GMUX_INT	HPLUG_DET2	MAKE_BASE=TRUE

R0940
20K
5%
1/16W
MF-LP
402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

27	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
28	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32	=P3V3ENET_EN	PM_SLP_RMGT_L 21	MAKE_BASE=TRUE
32	=P1V05ENET_EN		
31	=PP3V3_ENET_PHY_VDDREG	RTL8211_VDDREG	MAKE_BASE=TRUE
31	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31	=RTL8211_ENSWREG		
31	TP_RTL8211_CLK125	RTL8211_CLK125	MAKE_BASE=TRUE

R0931
22
5%
1/16W
MF-LP
402

CPU FSB FREQUENCY STRAPS

70 18 IN CPU_BSEL<0:2> MAKE_BASE=TRUE = =MCP_BSEL<0:2> OUT 14

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

SMC ALIASES

36	SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE

CPU VCORE ALIASES

59	IMVP6_VR_TT	TP_IMVP6_VR_TT	MAKE_BASE=TRUE
59	IMVP6_NTC	TP_IMVP6_NTC	MAKE_BASE=TRUE

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SIGNAL ALIAS

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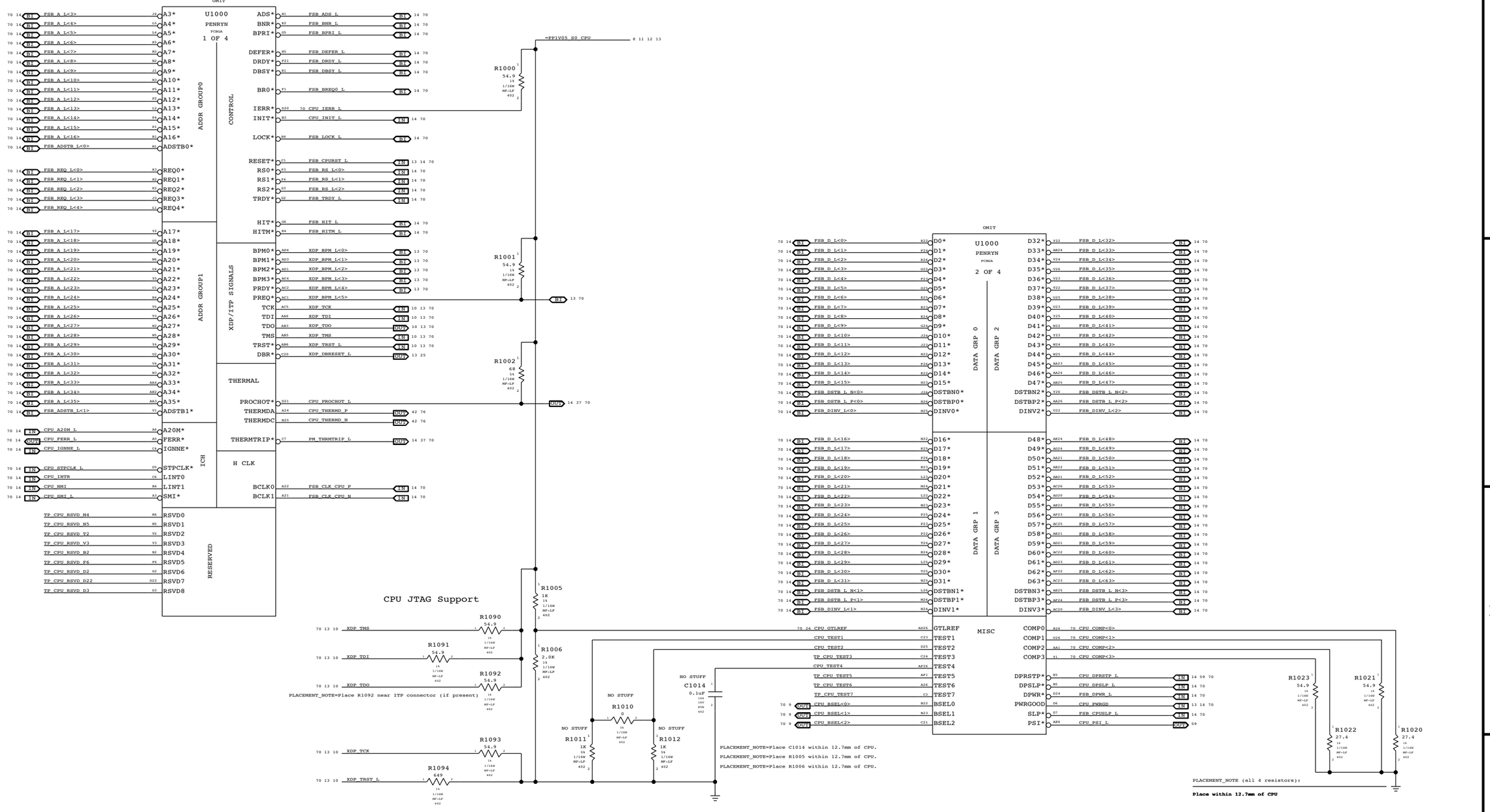

SYNC FROM T18

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

CPU FSB

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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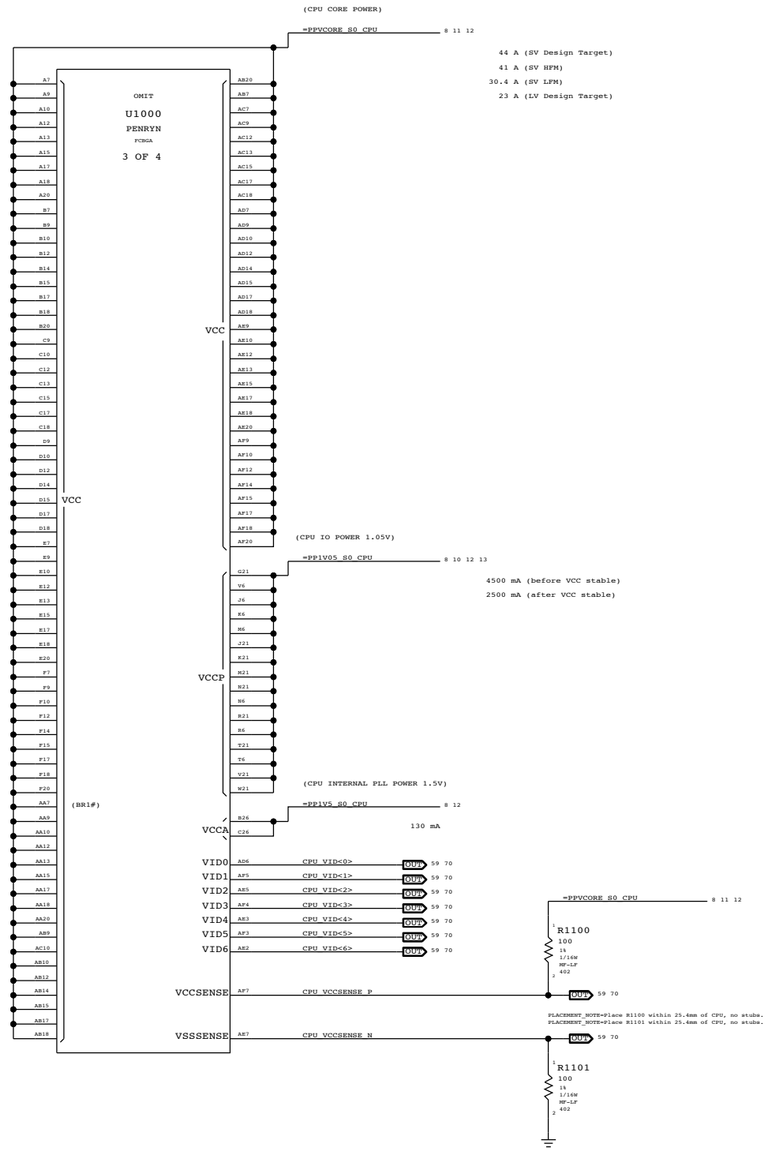

SYNC FROM T18

CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=K24_MLB SYNC DATE=04/06/2009

PAGE TITLE

CPU Power & Ground

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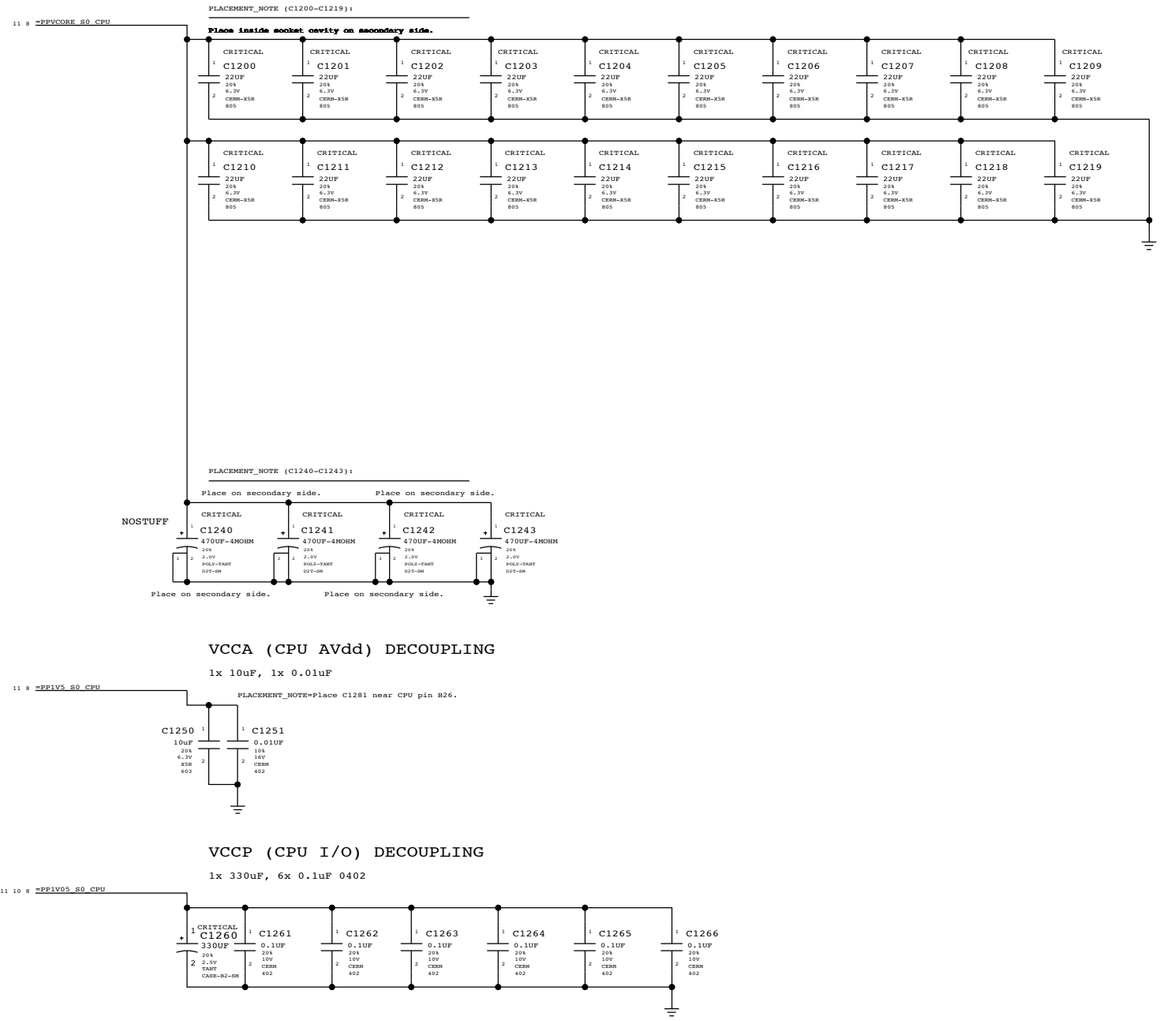
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC MASTER=K24 MLB SYNC DATE=03/30/2009

PAGE TITLE: CPU Decoupling

Apple Inc.

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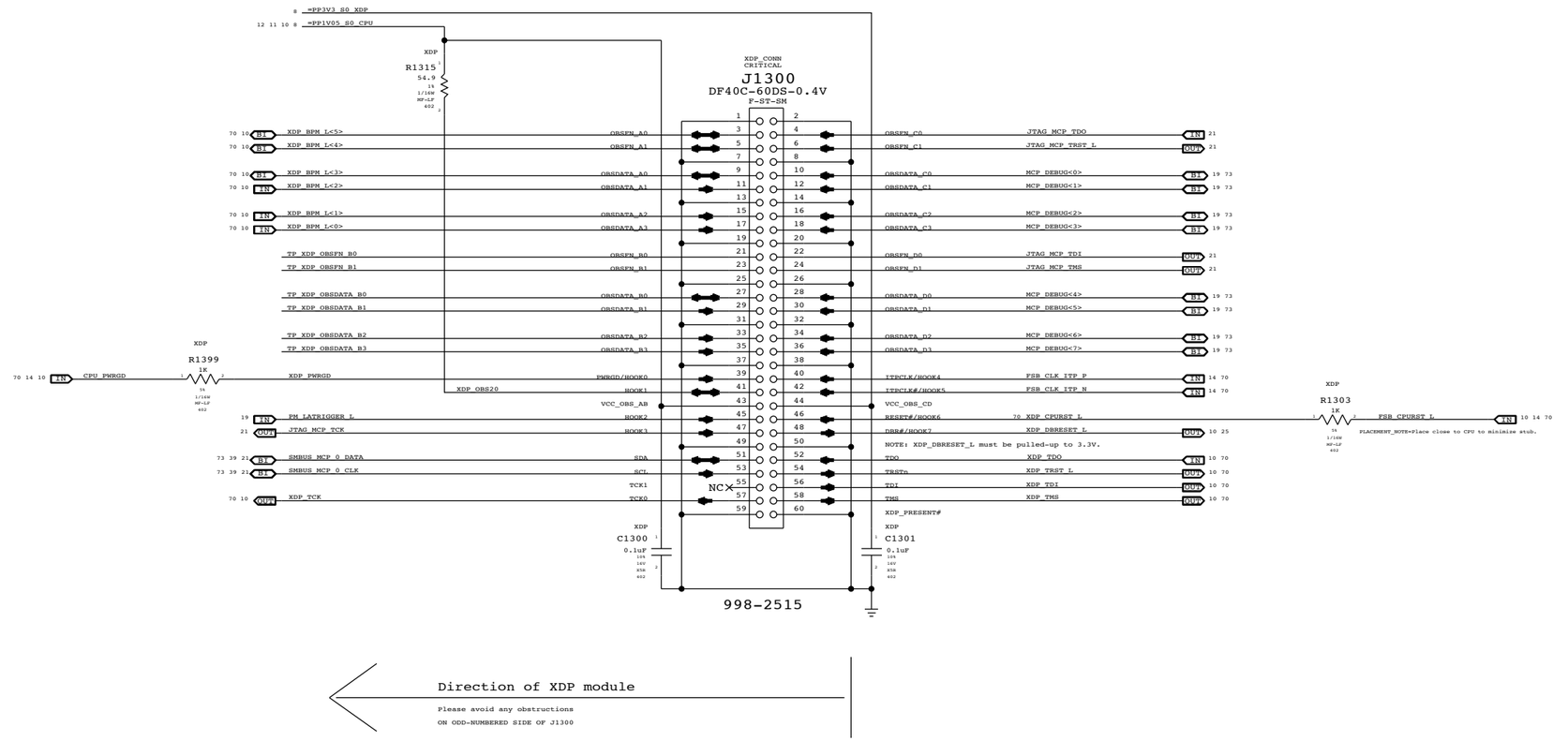
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP79-specific pinout



SYNC MASTER=K24 MLB SYNC DATE=02/25/2009

PAGE TITLE

eXtended Debug Port(MiniXDP)

Apple Inc.

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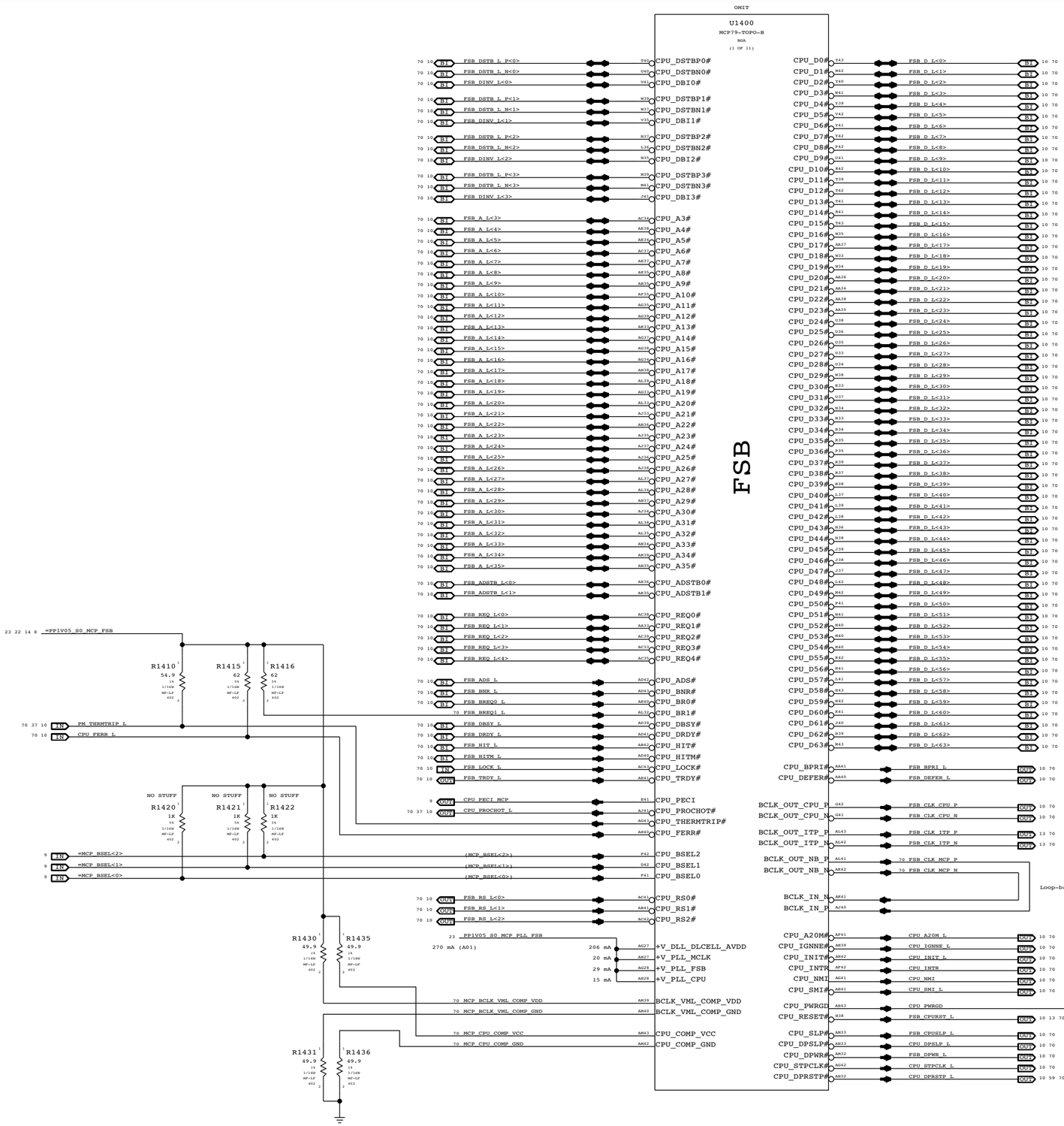

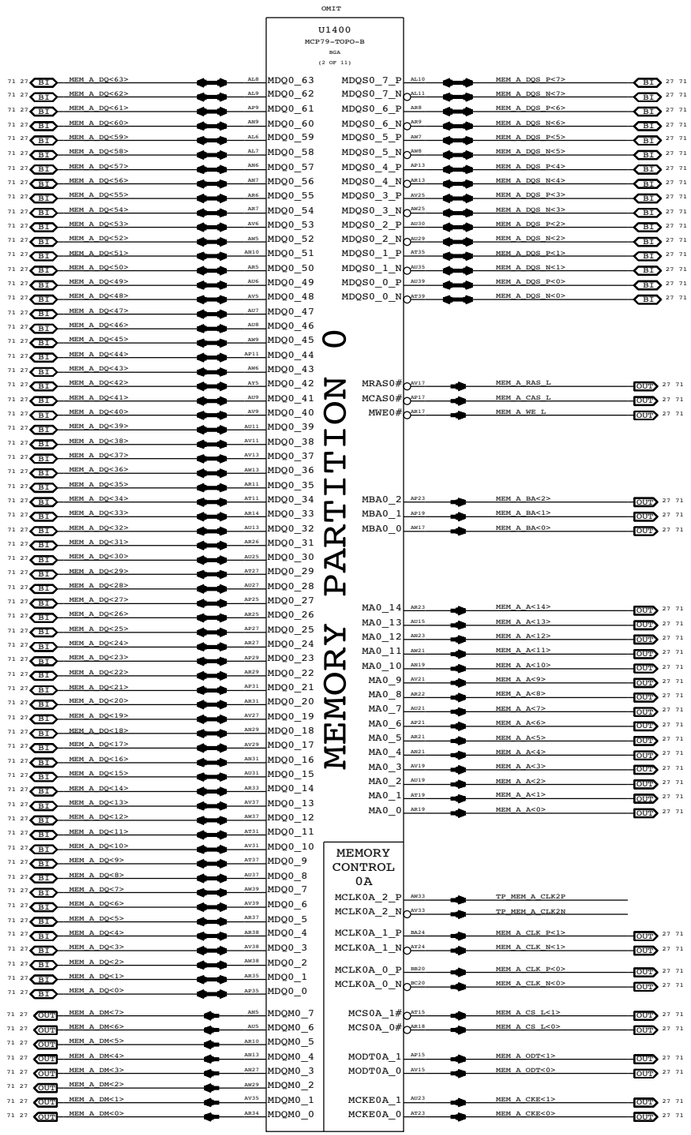

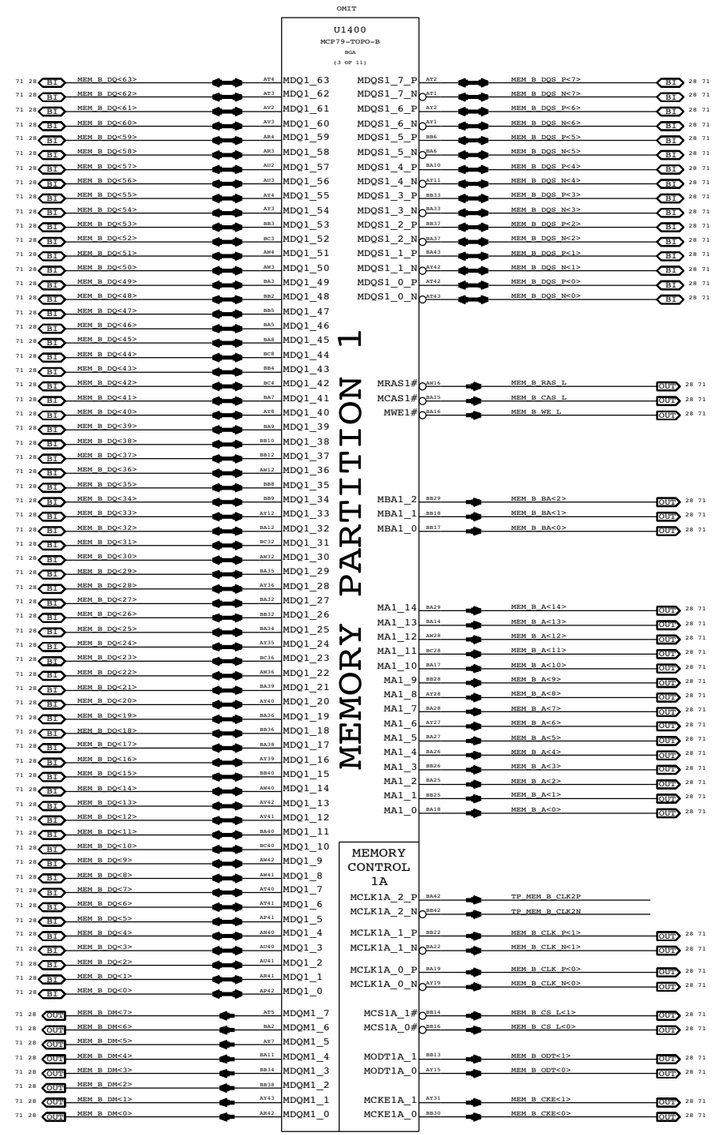

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Memory Interface

Apple Inc.

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U1400
MCP79-TOPO-B
BGA
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MEMORY CONTROL 0B

TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
TP_MEM_A_CLK5N	AU32	MCLK0B_2_N	
TP_MEM_A_CLK4P	BB24	MCLK0B_1_P	
TP_MEM_A_CLK4N	BC23	MCLK0B_1_N	
TP_MEM_A_CLK3P	BA21	MCLK0B_0_P	
TP_MEM_A_CLK3N	BB21	MCLK0B_0_N	
TP_MEM_A_CS_L<2>	AU16	MCS0B_0#	
TP_MEM_A_CS_L<3>	AR16	MCS0B_1#	
TP_MEM_A_ODT<2>	AR17	MODT0B_0	
TP_MEM_A_ODT<3>	AR15	MODT0B_1	
TP_MEM_A_CKE<2>	AV23	MCKE0B_0	
TP_MEM_A_CKE<3>	AM25	MCKE0B_1	

MEMORY CONTROL 1B

		MCLK1B_2_P	BA41
		MCLK1B_2_N	BB41
		MCLK1B_1_P	AY23
		MCLK1B_1_N	BA23
		MCLK1B_0_P	BA20
		MCLK1B_0_N	AY20
		MCS1B_0#	BC16
		MCS1B_1#	BA13
		MODT1B_0	AY16
		MODT1B_1	BC13
		MCKE1B_0	BA30
		MCKE1B_1	BA31

TP_MEM_B_CLK5P
TP_MEM_B_CLK5N
TP_MEM_B_CLK4P
TP_MEM_B_CLK4N
TP_MEM_B_CLK3P
TP_MEM_B_CLK3N
TP_MEM_B_CS_L<2>
TP_MEM_B_CS_L<3>
TP_MEM_B_ODT<2>
TP_MEM_B_ODT<3>
TP_MEM_B_CKE<2>
TP_MEM_B_CKE<3>

23 16 8 =PP1V8R1V5_S0_MCP_MEM

R1610 1 40.2 1% 1/16W MF-LF 402 2

R1611 1 40.2 1% 1/16W MF-LF 402 2

23 _PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS
12 mA	U28	+V_PLL_DP
19 mA	U27	+V_PLL_CORE
39 mA	T28	+V_VPLL

MRESET0# AY32 → MCP_MEM_RESET_L → DDR 29

TP or NC for DDR2.

71 MCP_MEM_COMP_VDD → AM41 MEM_COMP_VDD
71 MCP_MEM_COMP_GND → AM41 MEM_COMP_GND

=PP1V8R1V5_S0_MCP_MEM 8 16 23
4771 mA (A01, DDR3)

		+VDD_MEM1	AM17
		+VDD_MEM2	AM19
		+VDD_MEM3	AM21
		+VDD_MEM4	AM23
		+VDD_MEM5	AM25
		+VDD_MEM6	AM27
		+VDD_MEM7	AM29
		+VDD_MEM8	AM16
		+VDD_MEM9	BC29
		+VDD_MEM10	AM20
		+VDD_MEM11	AM24
		+VDD_MEM12	AT17
		+VDD_MEM13	AP16
		+VDD_MEM14	AM22
		+VDD_MEM15	AP20
		+VDD_MEM16	AP24
		+VDD_MEM17	AV16
		+VDD_MEM18	AR16
		+VDD_MEM19	AR20
		+VDD_MEM20	AR24
		+VDD_MEM21	AM15
		+VDD_MEM22	AP22
		+VDD_MEM23	AP18
		+VDD_MEM24	AG16
		+VDD_MEM25	AN19
		+VDD_MEM26	AG24
		+VDD_MEM27	AY21
		+VDD_MEM28	AY29
		+VDD_MEM29	AV24
		+VDD_MEM30	AG20
		+VDD_MEM31	AG22
		+VDD_MEM32	AW27
		+VDD_MEM33	BC17
		+VDD_MEM34	AV20
		+VDD_MEM35	AY17
		+VDD_MEM36	AY18
		+VDD_MEM37	AM15
		+VDD_MEM38	AG18
		+VDD_MEM39	AY25
		+VDD_MEM40	AY26
		+VDD_MEM41	AW19
		+VDD_MEM42	AW24
		+VDD_MEM43	BC25
		+VDD_MEM44	AL30
		+VDD_MEM45	AW31

AA22	GND1		
AP12	GND2		
G30	GND3		
P10	GND4		
T10	GND5		
T6	GND6		
V10	GND7		
V34	GND8		
W5	GND9		
AA34	GND10		
AB22	GND11		
AB7	GND12		
AD22	GND13		
AE20	GND14		
AF24	GND15		
AG24	GND16		
AH35	GND17		
AK7	GND18		
AM28	GND19		
AT25	GND20		
AP30	GND21		
AR34	GND22		
AU10	GND23		
F28	GND24		
BC21	GND25		
AY9	GND26		
BC9	GND27		
D34	GND28		
F24	GND29		
G32	GND30		
H31	GND31		
K7	GND32		
M38	GND33		
M5	GND34		
M6	GND35		
M1	GND36		
M9	GND37		
N39	GND38		
N8	GND39		
P33	GND40		
P34	GND41		
P37	GND42		
P4	GND43		
P40	GND44		
P7	GND45		
R36	GND46		
R40	GND47		
R41	GND48		
R5	GND49		
T18	GND50		
T20	GND51		
AK11	GND52		
T24	GND53		
T26	GND54		
		GND55	T33
		GND56	T34
		GND57	T35
		GND58	T37
		GND59	T38
		GND60	T7
		GND61	T9
		GND62	U18
		GND63	U20
		GND64	U22

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Memory Misc

Apple Inc.

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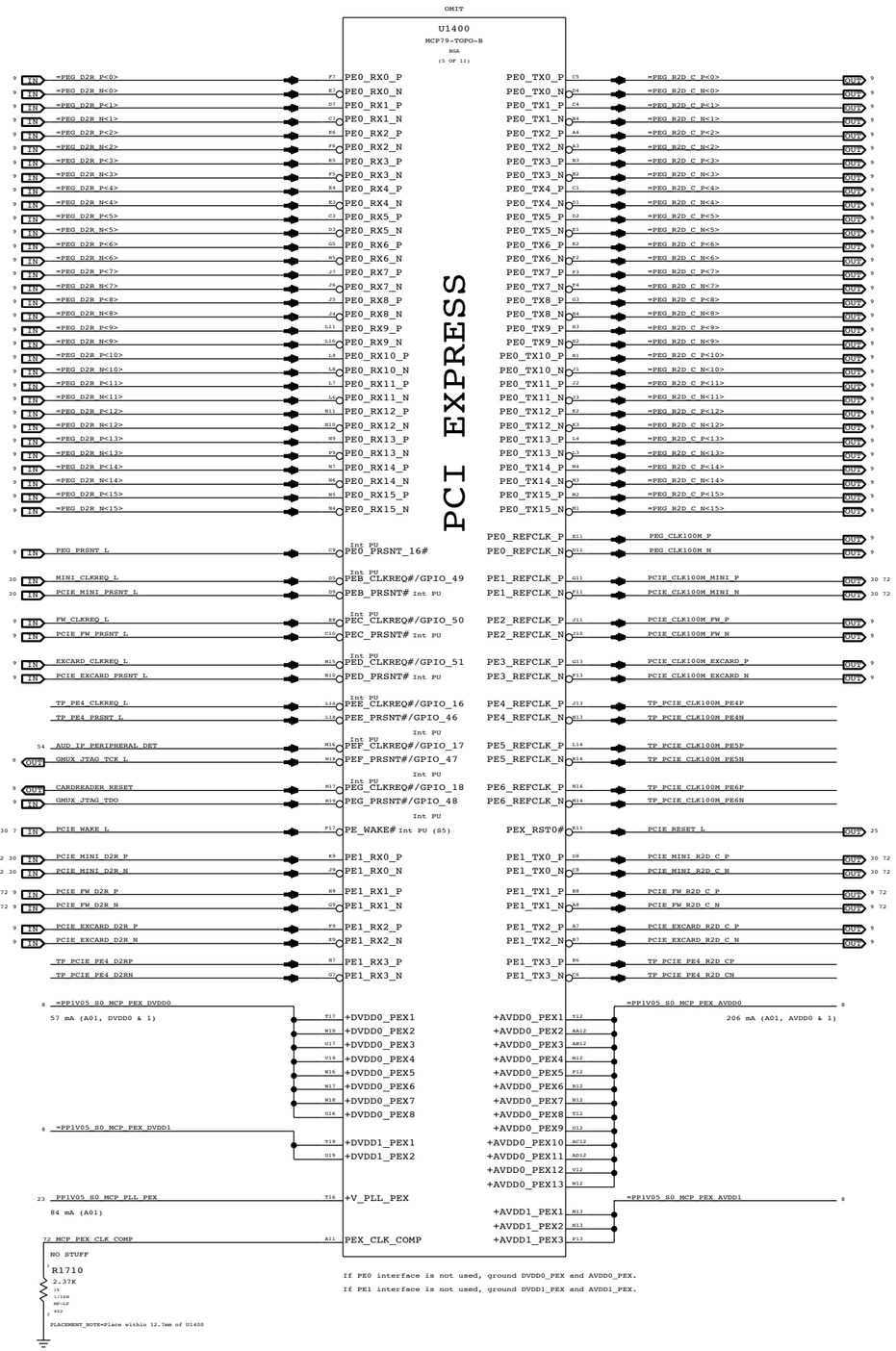

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
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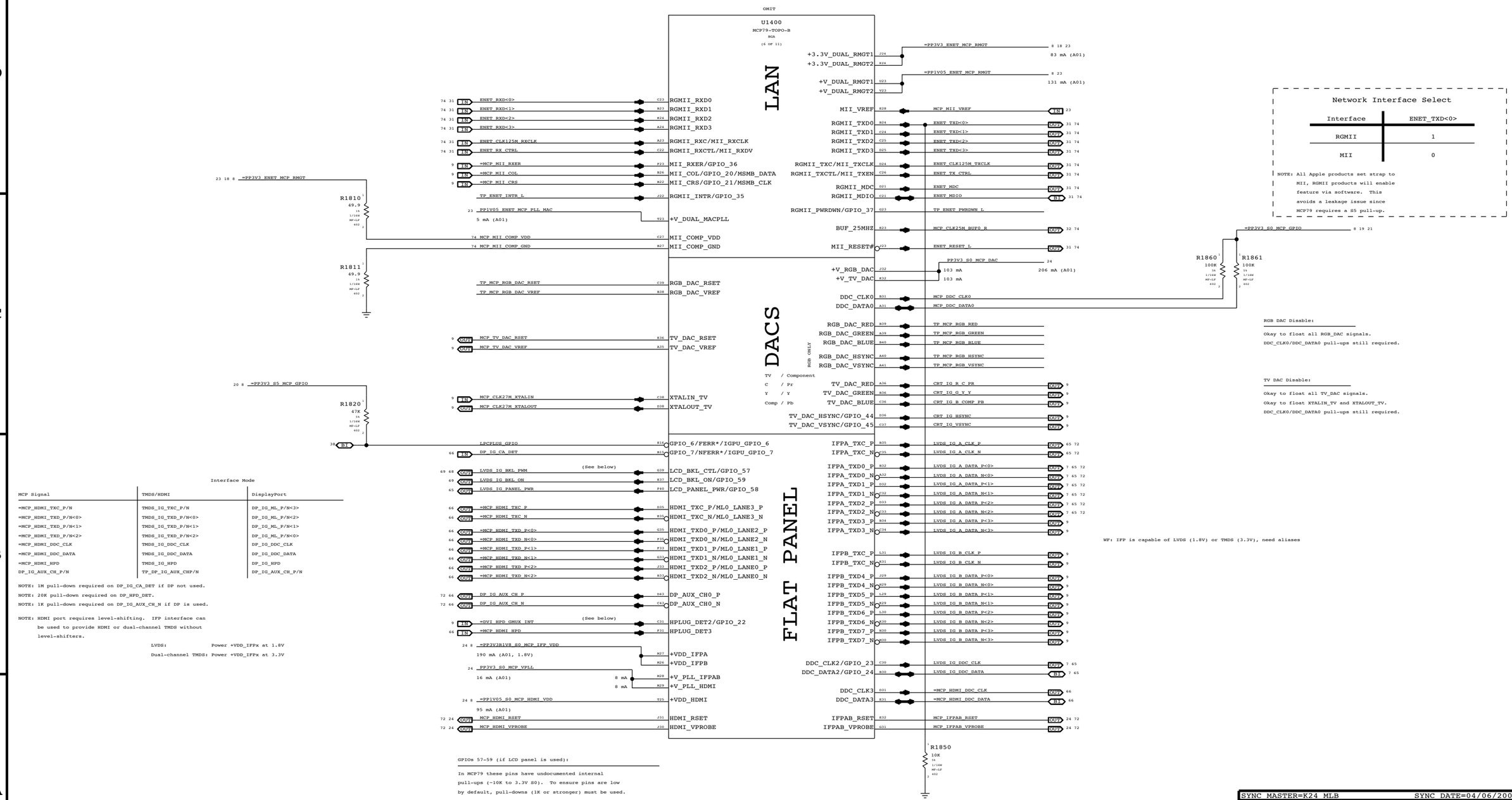

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

73 19	PCI_REQ0_L	T2	PCI_REQ0#
73 19	PCI_REQ1_L	V3	PCI_REQ1#/FANRPM2
19	OUT FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#
54	OUT AUD_IPHS_SWITCH_EN	U3	PCI_REQ3#/GPIO_38/RS232_CTS#
19	IN MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#
73 13	BI MCP_DEBUG<0>	AC3	PCI_AD0
73 13	BI MCP_DEBUG<1>	AB10	PCI_AD1
73 13	BI MCP_DEBUG<2>	AC4	PCI_AD2
73 13	BI MCP_DEBUG<3>	AB11	PCI_AD3
73 13	BI MCP_DEBUG<4>	AB3	PCI_AD4
73 13	BI MCP_DEBUG<5>	AC6	PCI_AD5
73 13	BI MCP_DEBUG<6>	AB2	PCI_AD6
73 13	BI MCP_DEBUG<7>	AC7	PCI_AD7
	TP_PCI_AD<8>	AC8	PCI_AD8
	TP_PCI_AD<9>	AA2	PCI_AD9
	TP_PCI_AD<10>	AC9	PCI_AD10
	TP_PCI_AD<11>	AC10	PCI_AD11
	TP_PCI_AD<12>	AC11	PCI_AD12
	TP_PCI_AD<13>	AA1	PCI_AD13
	TP_PCI_AD<14>	AA5	PCI_AD14
	TP_PCI_AD<15>	Y5	PCI_AD15
	TP_PCI_AD<16>	W3	PCI_AD16
	TP_PCI_AD<17>	W6	PCI_AD17
	TP_PCI_AD<18>	W4	PCI_AD18
	TP_PCI_AD<19>	W7	PCI_AD19
	TP_PCI_AD<20>	V3	PCI_AD20
	TP_PCI_AD<21>	W8	PCI_AD21
	TP_PCI_AD<22>	V2	PCI_AD22
	TP_PCI_AD<23>	W9	PCI_AD23
	TP_PCI_AD<24>	U3	PCI_AD24
	TP_PCI_AD<25>	W11	PCI_AD25
	TP_PCI_AD<26>	U2	PCI_AD26
	TP_PCI_AD<27>	U5	PCI_AD27
	TP_PCI_AD<28>	U1	PCI_AD28
	TP_PCI_AD<29>	U6	PCI_AD29
	TP_PCI_AD<30>	T5	PCI_AD30
	TP_PCI_AD<31>	U7	PCI_AD31
	TP_PCI_INTW_L	P2	PCI_INT#W
	TP_PCI_INTX_L	R3	PCI_INTX#
	TP_PCI_INTY_L	N2	PCI_INTY#
	TP_PCI_INTZ_L	N1	PCI_INTZ#
	TP_PCI_TRDY_L	Y3	PCI_TRDY#
38 36	IN PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42
9	IN FW_PME_L	AE2	PCI_DRQ1#/GPIO_19 Int PU
	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU
38 36	BI LPC_SERIRQ	AE6	LPC_SERIRQ Int PU
	PCI_GNT0#	AJ3	TP_PCI_GNT0_L
	PCI_GNT1#/FANCTL2	AD10	TP_PCI_GNT1_L
	PCI_GNT2#/GPIO_41/RS232_DTR#	AJ4	GMUX_JTAG_TMS OUT 9
	PCI_GNT3#/GPIO_39/RS232_RTS#	AD11	GMUX_JTAG_TDI OUT 9
	PCI_GNT4#/GPIO_53/RS232_SOUT#	AJ1	MCP_RS232_SOUT_L OUT 19
	PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>
	PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>
	PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>
	PCI_CBE3#	AA10	TP_PCI_C_BE_L<3>
	PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L
	PCI_FRAME#	Y4	TP_PCI_FRAME_L
	PCI_IRDY#	AA10	TP_PCI_IRDY_L
	PCI_PAR	Y1	TP_PCI_PAR
	PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L
	PCI_SERR#	AA7	TP_PCI_SERR_L
	PCI_STOP#	Y2	TP_PCI_STOP_L
	PCI_PME#/GPIO_30	Y1	PM_LATRIGGER_L OUT 13
	Int PU (S5)		
	PCI_RESET0#	AJ10	MEM_VTT_EN_R OUT 25
	PCI_RESET1#	AJ11	TP_PCI_RESET1_L
	PCI_CLK0	R6	TP_PCI_CLK0
	PCI_CLK1	R7	TP_PCI_CLK1
	PCI_CLK2	R8	73 PCI_CLK33M_MCP_R
	PCI_CLKIN	R9	73 PCI_CLK33M_MCP

R1910 22 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

	LPC_FRAME#	AD4	LPC_FRAME_R_L — R1960 22 5% 1/16W MF-LF 402 — LPC_FRAME_L OUT 36 38 73
	LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L OUT 36 38
	LPC_RESET0#	AB5	LPC_RESET_L OUT 25 73
	LPC_AD0	AD3	LPC_AD_R<0> — R1950 22 5% 1/16W MF-LF 402 — LPC_AD<0> BI 36 38 73
	LPC_AD1	AD2	LPC_AD_R<1> — R1951 22 5% 1/16W MF-LF 402 — LPC_AD<1> BI 36 38 73
	LPC_AD2	AD1	LPC_AD_R<2> — R1952 22 5% 1/16W MF-LF 402 — LPC_AD<2> BI 36 38 73
	LPC_AD3	AD5	LPC_AD_R<3> — R1953 22 5% 1/16W MF-LF 402 — LPC_AD<3> BI 36 38 73
	LPC_CLK0	AB9	LPC_CLK33M_SMC_R OUT 25 73

R1961 10K 5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	Y26	GND98
U26	GND66	Y27	GND99
U39	GND67	AB18	GND100
U4	GND68	B34	GND101
U8	GND69	AB20	GND102
V16	GND70	AB21	GND103
V17	GND71	AB23	GND104
V18	GND72	AB24	GND105
V20	GND73	AB25	GND106
V22	GND74	AB26	GND107
V24	GND75	AB27	GND108
V26	GND76	AB28	GND109
V27	GND77	AB34	GND110
V28	GND78	AB37	GND111
V33	GND79	AB4	GND112
V37	GND80	AB40	GND113
V4	GND81	AC22	GND114
V40	GND82	AC36	GND115
V7	GND83	AC40	GND116
W20	GND84	AB33	GND117
W22	GND85	AC5	GND118
W24	GND86	AD16	GND119
W36	GND87	AD17	GND120
W40	GND88	AD18	GND121
W43	GND89	AD19	GND122
Y16	GND90	AD20	GND123
Y17	GND91	AD24	GND124
Y18	GND92	AD25	GND125
Y19	GND93	AD26	GND126
Y20	GND94	AD27	GND127
Y22	GND95	AD28	GND128
Y24	GND96	AD33	GND129
Y25	GND97	AD34	GND130

21 18 8 +PP3V3_S0_MCP_GPIO

19	MCP_RS232_SOUT_L	R1989	8.2K 5% 1/16W MF-LF 402
73 19	PCI_REQ0_L	R1990	8.2K 5% 1/16W MF-LF 402
73 19	PCI_REQ1_L	R1991	8.2K 5% 1/16W MF-LF 402
19	FW_PWR_EN	R1992	8.2K 5% 1/16W MF-LF 402
19	MCP_RS232_SIN_L	R1994	8.2K 5% 1/16W MF-LF 402

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009
PAGE TITLE: MCP PCI & LPC

Apple Inc.

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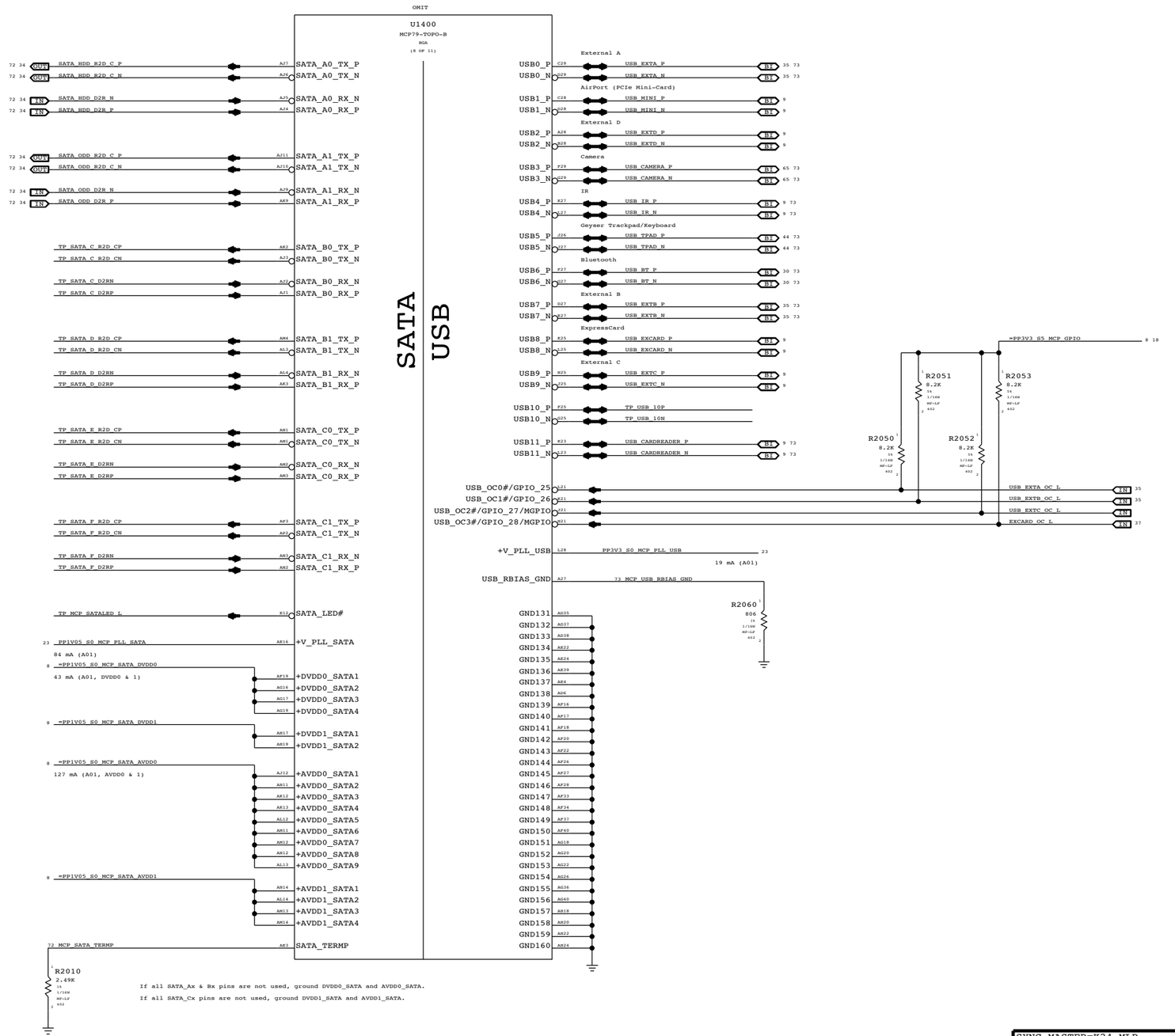

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SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

MCP SATA & USB

Apple Inc.

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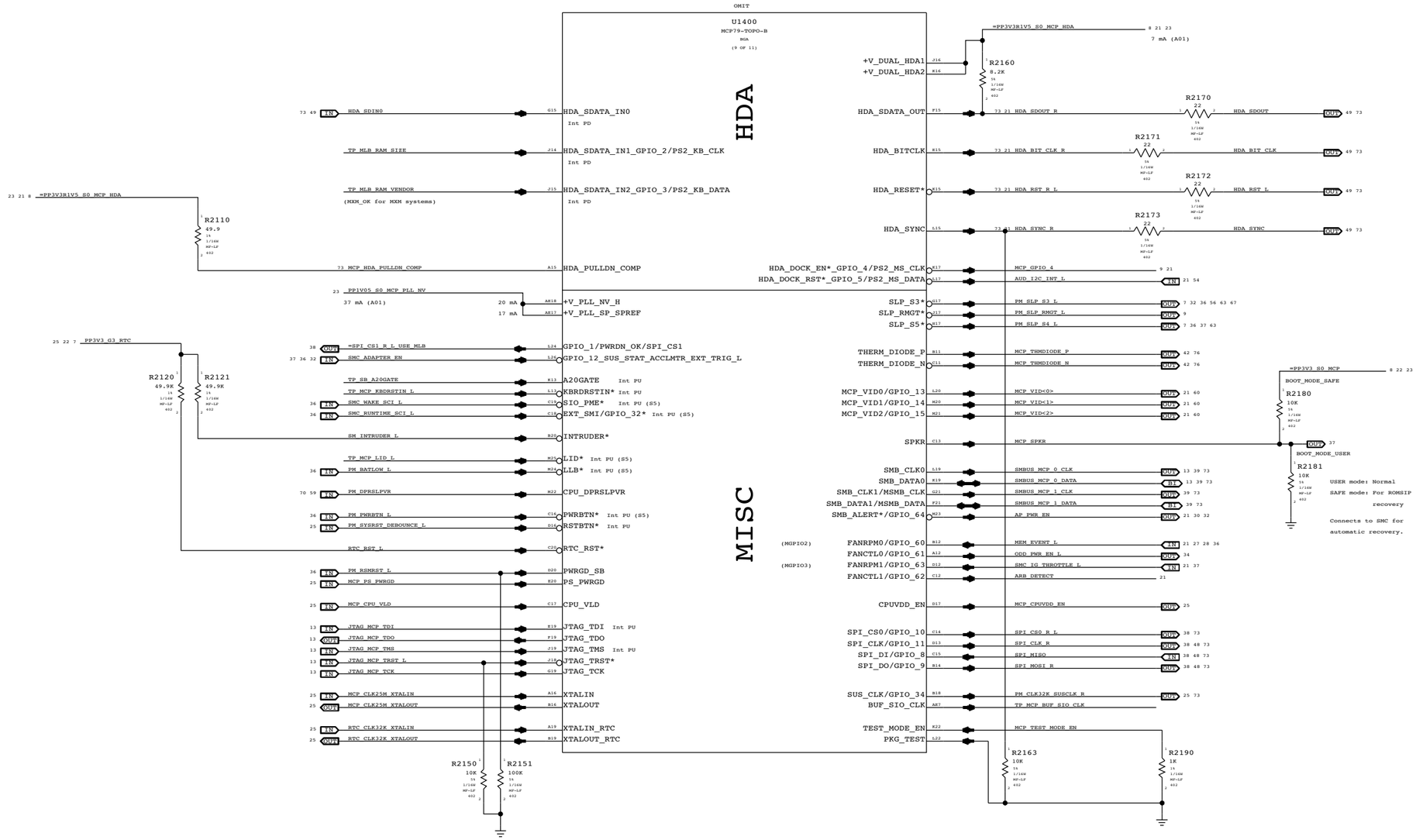

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K24 MLB SYNC DATE=03/24/2009

PAGE TITLE: MCP HDA & MISC

Apple Inc.

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U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

A26	GND161	GND253	AV40
A33	GND162	GND254	BA1
A34	GND163	GND255	BA4
A37	GND164	GND256	AM31
A38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AM20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AM35
AP7	GND210	GND302	H23
AN23	GND211	GND303	A88
AN28	GND212	GND304	G40
AN32	GND213	GND305	J12
AN40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	A07
AW11	GND241	GND333	M11
G20	GND242	GND334	A64
AW43	GND243	GND335	AB19
AW43	GND244	GND336	AU13
AY10	GND245	GND337	F11
AY12	GND246	GND338	F6
AY30	GND247	GND339	Y11
AY33	GND248	GND340	Y11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AB16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

23 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	R40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AK32
AC16	+VDD_CORE13	+VTT_CPU13	AM32
AC17	+VDD_CORE14	+VTT_CPU14	AJ32
AC18	+VDD_CORE15	+VTT_CPU15	AK31
AC19	+VDD_CORE16	+VTT_CPU16	AK32
AC20	+VDD_CORE17	+VTT_CPU17	AD32
AC21	+VDD_CORE18	+VTT_CPU18	AL31
AA17	+VDD_CORE19	+VTT_CPU19	AB32
AC24	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AB19	+VDD_CORE30	+VTT_CPU30	F37
AB21	+VDD_CORE31	+VTT_CPU31	F38
AB23	+VDD_CORE32	+VTT_CPU32	F39
AB25	+VDD_CORE33	+VTT_CPU33	G36
AB26	+VDD_CORE34	+VTT_CPU34	G37
AB27	+VDD_CORE35	+VTT_CPU35	G38
AB28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CORE40	+VTT_CPU40	K33
AF21	+VDD_CORE41	+VTT_CPU41	K34
AF23	+VDD_CORE42	+VTT_CPU42	K35
AF25	+VDD_CORE43	+VTT_CPU43	L32
AF3	+VDD_CORE44	+VTT_CPU44	L33
AF4	+VDD_CORE45	+VTT_CPU45	L34
AF7	+VDD_CORE46	+VTT_CPU46	M31
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	M31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58		
AG7	+VDD_CORE59	+3.3V_1	AD10
AG8	+VDD_CORE60	+3.3V_2	AE8
AG9	+VDD_CORE61	+3.3V_3	AB10
AH1	+VDD_CORE62	+3.3V_4	AG9
AH10	+VDD_CORE63	+3.3V_5	Y10
AH11	+VDD_CORE64	+3.3V_6	AH11
W26	+VDD_CORE65	+3.3V_7	AA8
AH2	+VDD_CORE66	+3.3V_8	Y9
AA23	+VDD_CORE67		
W28	+VDD_CORE68		
AB25	+VDD_CORE69		
AB21	+VDD_CORE70	+3.3V_DUAL1	G18
AB3	+VDD_CORE71	+3.3V_DUAL2	H19
AB4	+VDD_CORE72	+3.3V_DUAL3	J20
AB5	+VDD_CORE73	+3.3V_DUAL4	K20
AB6	+VDD_CORE74		
AB7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AB9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
		+VDD_AUXC1	V21
		+VDD_AUXC2	U21
A20	+VBAT	+VDD_AUXC3	V21

=PP1V05_S0_MCP_FSB 8 14 23
1139 mA 1182 mA (A01)

43 mA

=PP3V3_S0_MCP 8 21 23
450 mA (A01)

=PP3V3_S5_MCP 8 23
16 mA 266 mA (A01)

250 mA

=PP1V05_S5_MCP_VDD_AUXC 8 23
105 mA (A01)

25 21 7 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
BRANCH
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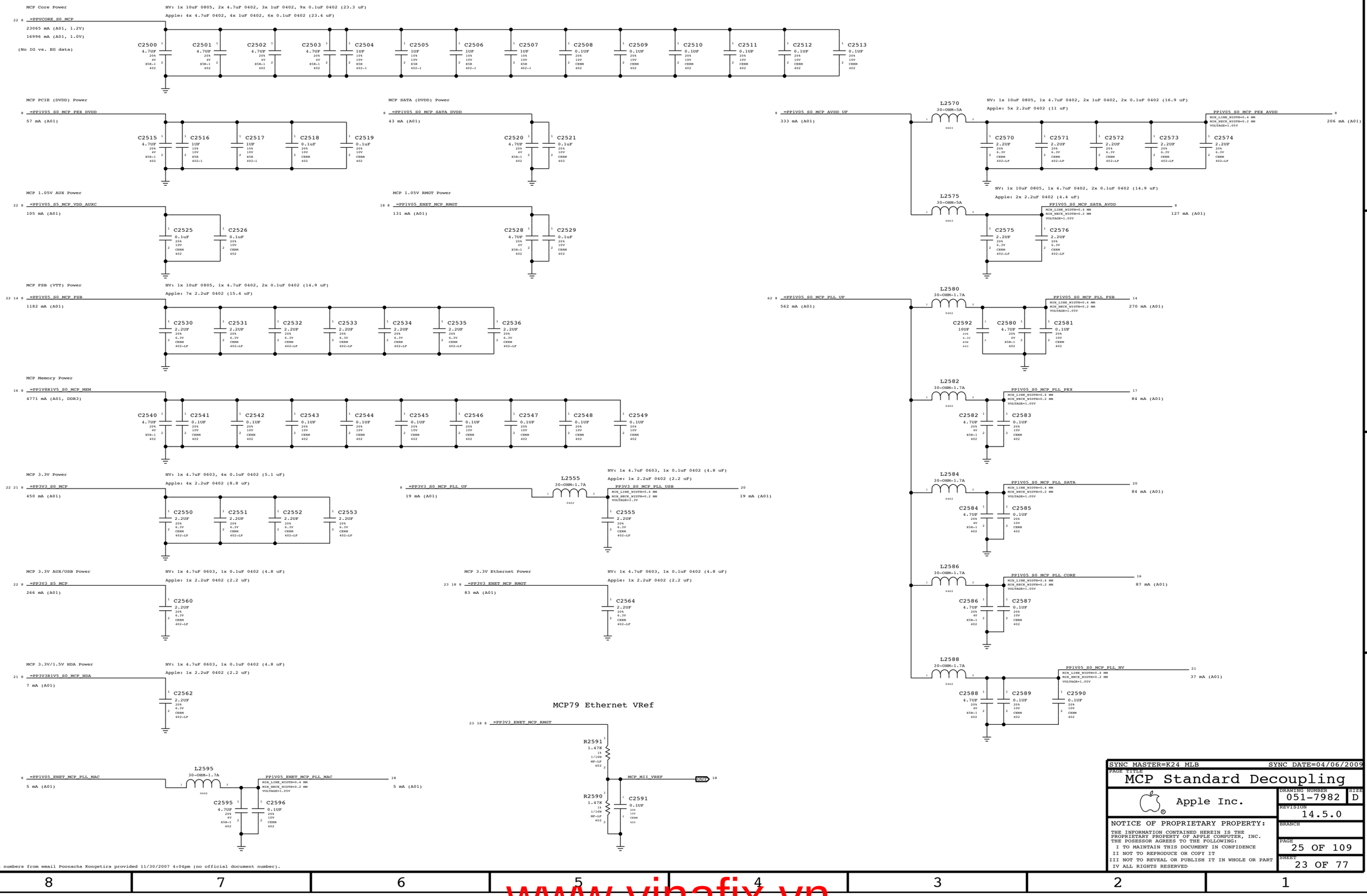
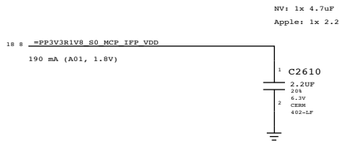
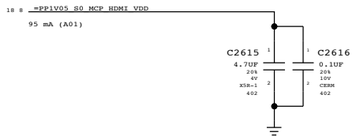
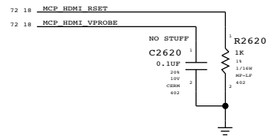


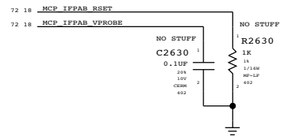
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



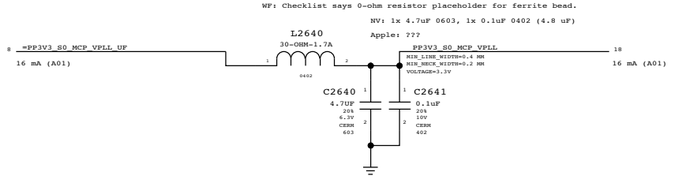




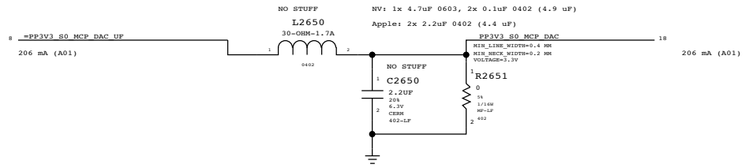


WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
MCP Graphics Support

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
BRANCH
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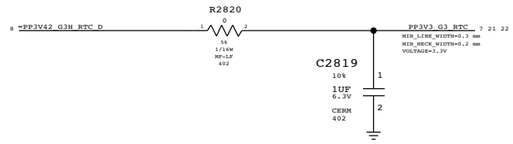
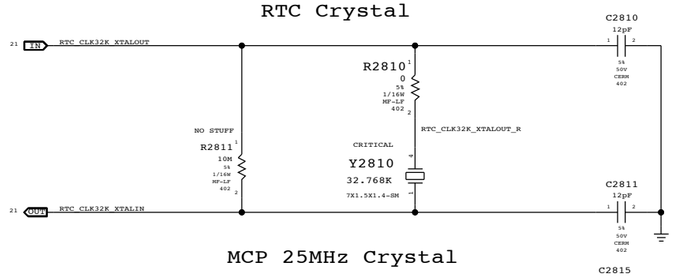


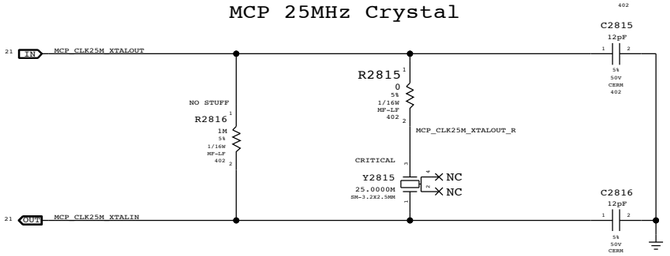
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79

PLACE C2819 CLOSE TO MCP79

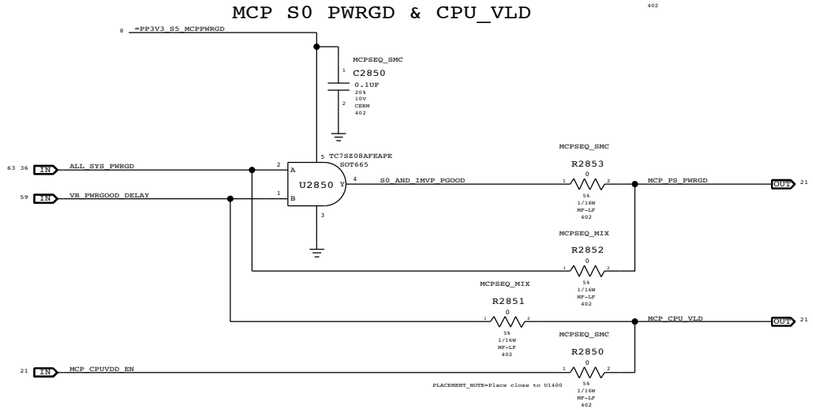
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections,
but results in MCP79 ROMSIP sequence happening after CPU powers up.

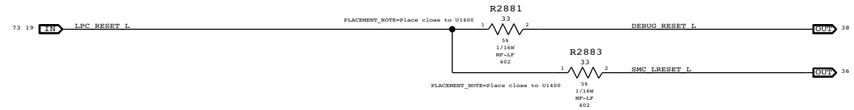
MCPSEQ_MIX is cross between MLB and internal power sequencing, which
results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for
VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before
CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

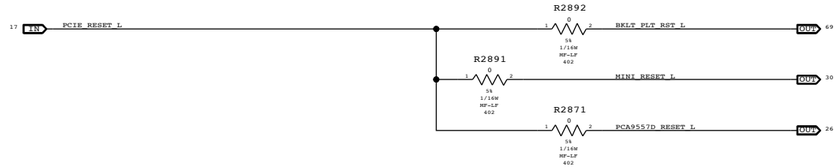
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

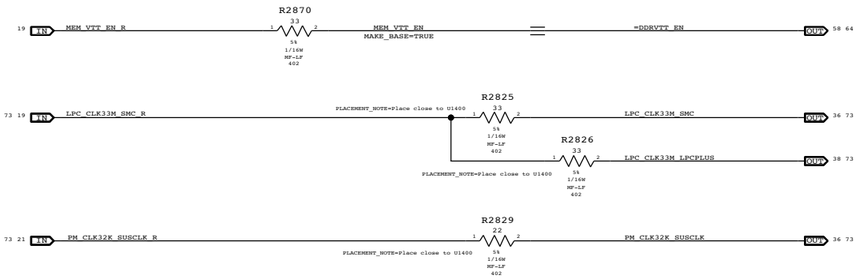
Platform Reset Connections

LPC Reset (Unbuffered)

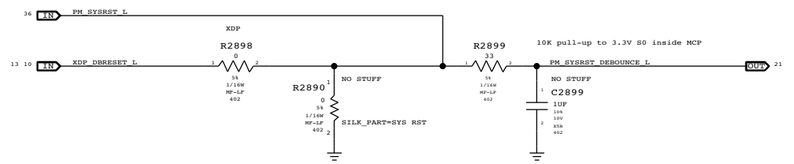


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC_MASTER=K24_MLB	SYNC_DATE=02/15/2009
PAGE TITLE: SB Misc	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: 14.5.0
	BRANCH:
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Page Notes

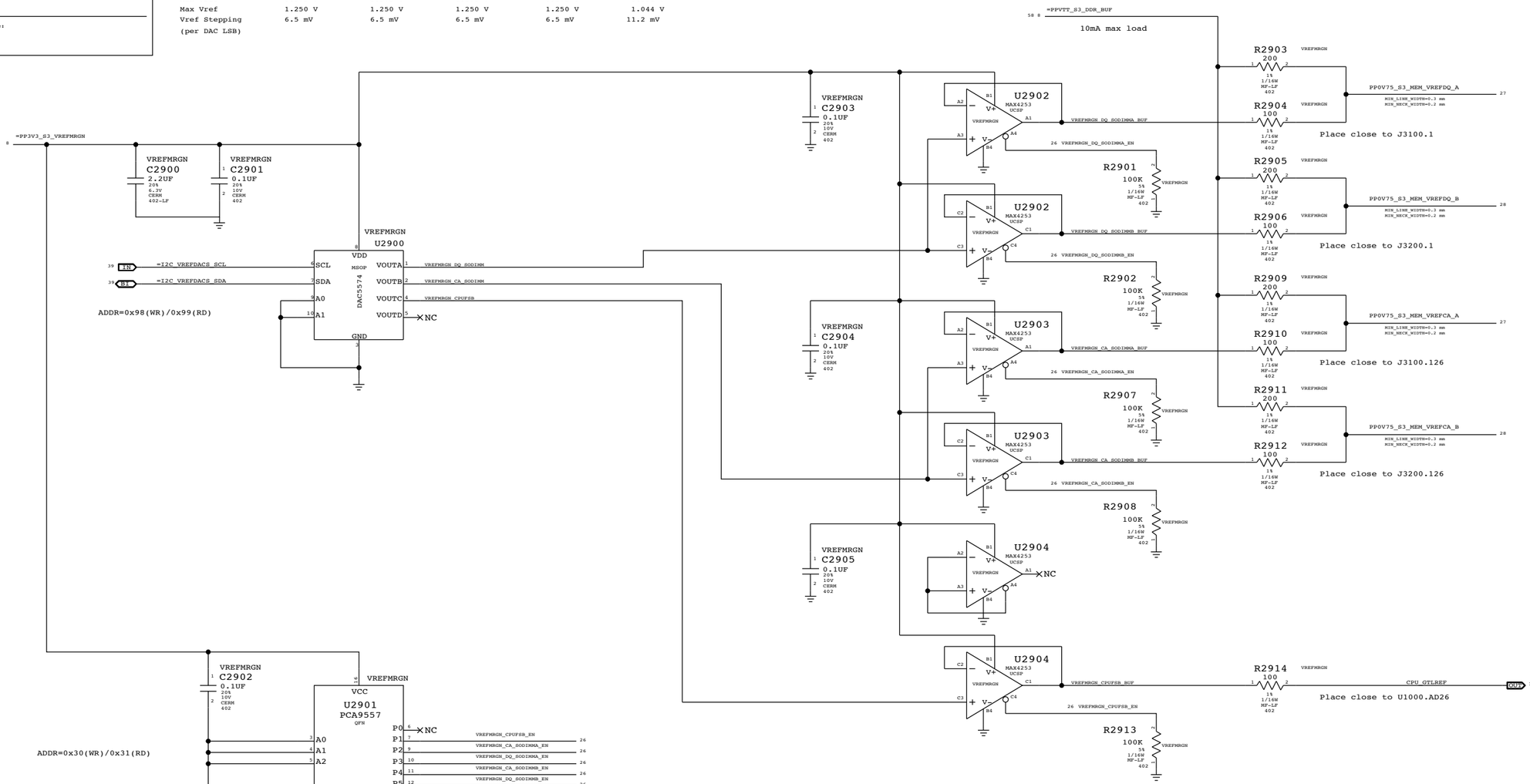
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE: FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D
REVISION: 14.5.0
BRANCH:
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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 (SYMBOL 2 OF 2)

DDR3-SODIMM-DUAL-M97-3
F-RT-THB
KEY

71 15	IN	MEM_A_CKE<0>	73 CKE0	74 CKE1	MEM_A_CKE<1>	IN 15 71
		NC	75 VDD	76 VDD		
			77 NC	78 A15	MEM_A_A<15>	IN 9
71 15	IN	MEM_A_BA<2>	79 BA2	80 A14	MEM_A_A<14>	IN 15 71
			81 VDD	82 VDD		
71 15	IN	MEM_A_A<12>	83 A12/BC*	84 A11	MEM_A_A<11>	IN 15 71
71 15	IN	MEM_A_A<9>	85 A9	86 A7	MEM_A_A<7>	IN 15 71
			87 VDD	88 VDD		
71 15	IN	MEM_A_A<8>	89 A8	90 A6	MEM_A_A<6>	IN 15 71
71 15	IN	MEM_A_A<5>	91 A5	92 A4	MEM_A_A<4>	IN 15 71
			93 VDD	94 VDD		
71 15	IN	MEM_A_A<3>	95 A3	96 A2	MEM_A_A<2>	IN 15 71
71 15	IN	MEM_A_A<1>	97 A1	98 A0	MEM_A_A<0>	IN 15 71
			99 VDD	100 VDD		
71 15	IN	MEM_A_CLK_P<0>	101 CK0	102 CK1	MEM_A_CLK_P<1>	IN 15 71
71 15	IN	MEM_A_CLK_N<0>	103 CK0*	104 CK1*	MEM_A_CLK_N<1>	IN 15 71
			105 VDD	106 VDD		
71 15	IN	MEM_A_A<10>	107 A10/AP	108 BA1	MEM_A_BA<1>	IN 15 71
71 15	IN	MEM_A_BA<0>	109 BA0	110 RAS*	MEM_A_RAS_L	IN 15 71
			111 VDD	112 VDD		
71 15	IN	MEM_A_WE_L	113 WE*	114 S0*	MEM_A_CS_L<0>	IN 15 71
71 15	IN	MEM_A_CAS_L	115 CAS*	116 ODT0	MEM_A_ODT<0>	IN 15 71
			117 VDD	118 VDD		
71 15	IN	MEM_A_A<13>	119 A13	120 ODT1	MEM_A_ODT<1>	IN 15 71
71 15	IN	MEM_A_CS_L<1>	121 S1*	122 NC	NC	
			123 VDD	124 VDD		
NC			125 TEST	126 VREFCA		
			127 VSS	128 VSS		
71 15	BI	MEM_A_DQ<34>	129 DQ32	130 DQ36	MEM_A_DQ<37>	BI 15 71
71 15	BI	MEM_A_DQ<35>	131 DQ33	132 DQ37	MEM_A_DQ<36>	BI 15 71
			133 VSS	134 VSS		
71 15	BI	MEM_A_DQS_N<4>	135 DQS4*	136 DM4	MEM_A_DM<4>	IN 15 71
71 15	BI	MEM_A_DQS_P<4>	137 DQS4	138 VSS		
			139 VSS	140 DQ38	MEM_A_DQ<38>	BI 15 71
71 15	BI	MEM_A_DQ<32>	141 DQ34	142 DQ39	MEM_A_DQ<39>	BI 15 71
71 15	BI	MEM_A_DQ<33>	143 DQ35	144 VSS		
			145 VSS	146 DQ44	MEM_A_DQ<41>	BI 15 71
71 15	BI	MEM_A_DQ<44>	147 DQ40	148 DQ45	MEM_A_DQ<40>	BI 15 71
71 15	BI	MEM_A_DQ<45>	149 DQ41	150 VSS		
			151 VSS	152 DQS5*	MEM_A_DQS_N<5>	BI 15 71
71 15	IN	MEM_A_DM<5>	153 DM5	154 DQS5	MEM_A_DQS_P<5>	BI 15 71
			155 VSS	156 VSS		
71 15	BI	MEM_A_DQ<47>	157 DQ42	158 DQ46	MEM_A_DQ<43>	BI 15 71
71 15	BI	MEM_A_DQ<46>	159 DQ43	160 DQ47	MEM_A_DQ<42>	BI 15 71
			161 VSS	162 VSS		
71 15	BI	MEM_A_DQ<49>	163 DQ48	164 DQ52	MEM_A_DQ<53>	BI 15 71
71 15	BI	MEM_A_DQ<52>	165 DQ49	166 DQ53	MEM_A_DQ<48>	BI 15 71
			167 VSS	168 VSS		
71 15	BI	MEM_A_DQS_N<6>	169 DQS6*	170 DM6	MEM_A_DM<6>	IN 15 71
71 15	BI	MEM_A_DQS_P<6>	171 DQS6	172 VSS		
			173 VSS	174 DQ54	MEM_A_DQ<55>	BI 15 71
71 15	BI	MEM_A_DQ<54>	175 DQ50	176 DQ55	MEM_A_DQ<50>	BI 15 71
71 15	BI	MEM_A_DQ<51>	177 DQ51	178 VSS		
			179 VSS	180 DQ60	MEM_A_DQ<57>	BI 15 71
71 15	BI	MEM_A_DQ<61>	181 DQ56	182 DQ61	MEM_A_DQ<56>	BI 15 71
71 15	BI	MEM_A_DQ<60>	183 DQ57	184 VSS		
			185 VSS	186 DQS7*	MEM_A_DQS_N<7>	BI 15 71
71 15	IN	MEM_A_DM<7>	187 DM7	188 DQS7	MEM_A_DQS_P<7>	BI 15 71
			189 VSS	190 VSS		
71 15	BI	MEM_A_DQ<58>	191 DQ58	192 DQ62	MEM_A_DQ<62>	BI 15 71
71 15	BI	MEM_A_DQ<59>	193 DQ59	194 DQ63	MEM_A_DQ<63>	BI 15 71
			195 VSS	196 VSS		
		MEM_A_SA<0>	197 SA0	198 EVENT*	MEM_EVENT_L	OD 21 28 36
			199 VDDSPD	200 SDA	=I2C_SODIMMA_SDA	BI 39
		MEM_A_SA<1>	201 SA1	202 SCL	=I2C_SODIMMA_SCL	IN 39
			203 VTT	204 VTT	=PP0V75_S0_MEM_VTT_A	8

516-0201

SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 (SYMBOL 1 OF 2)

DDR3-SODIMM-DUAL-M97-3
F-RT-THB
OMIT
CRITICAL
KEY

			1 VREFDQ	2 VSS	
71 15	BI	MEM_A_DQ<0>	3 VSS	4 DQ4	MEM_A_DQ<4> BI 15 71
71 15	BI	MEM_A_DQ<1>	5 DQ0	6 DQ5	MEM_A_DQ<5> BI 15 71
			7 DQ1	8 VSS	
71 15	IN	MEM_A_DM<0>	9 VSS	10 DQS0*	MEM_A_DQS_N<0> BI 15 71
			11 DM0	12 DQS0	MEM_A_DQS_P<0> BI 15 71
71 15	BI	MEM_A_DQ<6>	13 VSS	14 VSS	
71 15	BI	MEM_A_DQ<7>	15 DQ2	16 DQ6	MEM_A_DQ<3> BI 15 71
			17 DQ3	18 DQ7	MEM_A_DQ<2> BI 15 71
71 15	BI	MEM_A_DQ<14>	19 VSS	20 VSS	
71 15	BI	MEM_A_DQ<11>	21 DQ8	22 DQ12	MEM_A_DQ<9> BI 15 71
			23 DQ9	24 DQ13	MEM_A_DQ<8> BI 15 71
71 15	BI	MEM_A_DQS_N<1>	25 VSS	26 VSS	
71 15	BI	MEM_A_DQS_P<1>	27 DQS1*	28 DM1	MEM_A_DM<1> IN 15 71
			29 DQS1	30 RESET*	MEM_RESET_L IN 28 29
71 15	BI	MEM_A_DQ<13>	31 VSS	32 VSS	
71 15	BI	MEM_A_DQ<12>	33 DQ10	34 DQ14	MEM_A_DQ<15> BI 15 71
			35 DQ11	36 DQ15	MEM_A_DQ<10> BI 15 71
71 15	BI	MEM_A_DQ<25>	37 VSS	38 VSS	
71 15	BI	MEM_A_DQ<29>	39 DQ16	40 DQ20	MEM_A_DQ<24> BI 15 71
			41 DQ17	42 DQ21	MEM_A_DQ<28> BI 15 71
71 15	BI	MEM_A_DQS_N<3>	43 VSS	44 VSS	
71 15	BI	MEM_A_DQS_P<3>	45 DQS2*	46 DM2	MEM_A_DM<3> IN 15 71
			47 DQS2	48 VSS	
71 15	BI	MEM_A_DQ<26>	49 VSS	50 DQ22	MEM_A_DQ<27> BI 15 71
71 15	BI	MEM_A_DQ<30>	51 DQ18	52 DQ23	MEM_A_DQ<31> BI 15 71
			53 DQ19	54 VSS	
71 15	BI	MEM_A_DQ<20>	55 VSS	56 DQ28	MEM_A_DQ<18> BI 15 71
71 15	BI	MEM_A_DQ<21>	57 DQ24	58 DQ29	MEM_A_DQ<17> BI 15 71
			59 DQ25	60 VSS	
71 15	IN	MEM_A_DM<2>	61 VSS	62 DQS3*	MEM_A_DQS_N<2> BI 15 71
			63 DM3	64 DQS3	MEM_A_DQS_P<2> BI 15 71
71 15	BI	MEM_A_DQ<23>	65 VSS	66 VSS	
71 15	BI	MEM_A_DQ<16>	67 DQ26	68 DQ30	MEM_A_DQ<22> BI 15 71
			69 DQ27	70 DQ31	MEM_A_DQ<19> BI 15 71
			71 VSS	72 VSS	

516-0201

PP0V75_S3_MEM_VREFCA_A 26

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

8 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402
C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

"Factory" (top) slot

SYNC MASTER=K24_MLB	SYNC DATE=02/05/2009
PAGE TITLE: DDR3 SO-DIMM Connector A	
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
	REVISION 14.5.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE 31 OF 109
	SHEET 27 OF 77

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

ROM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

8 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

DDR3-SODIMM (2 OF 2) — J3200 F-RT-BGA3 (OMIT)

KEY

71 15 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15 71
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_BA<15>	IN 9
71 15 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15 71
		81	VDD	VDD	82		
71 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15 71
71 15 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15 71
		87	VDD	VDD	88		
71 15 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15 71
71 15 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15 71
		93	VDD	VDD	94		
71 15 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15 71
71 15 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15 71
		99	VDD	VDD	100		
71 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15 71
71 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15 71
		105	VDD	VDD	106		
71 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15 71
71 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15 71
		111	VDD	VDD	112		
71 15 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15 71
71 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15 71
		117	VDD	VDD	118		
71 15 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15 71
71 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
71 15 BI	MEM_B_DQ<33>	129	DQ32	DQ36	130	MEM_B_DQ<37>	BI 15 71
71 15 BI	MEM_B_DQ<36>	131	DQ33	DQ37	132	MEM_B_DQ<32>	BI 15 71
		133	VSS	VSS	134		
71 15 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	BI 15 71
71 15 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<39>	BI 15 71
71 15 BI	MEM_B_DQ<35>	141	DQ34	DQ39	142	MEM_B_DQ<34>	BI 15 71
71 15 BI	MEM_B_DQ<38>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<40>	BI 15 71
71 15 BI	MEM_B_DQ<45>	147	DQ40	DQ45	148	MEM_B_DQ<44>	BI 15 71
71 15 BI	MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 15 71
71 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 15 71
		155	VSS	VSS	156		
71 15 BI	MEM_B_DQ<46>	157	DQ42	DQ46	158	MEM_B_DQ<42>	BI 15 71
71 15 BI	MEM_B_DQ<47>	159	DQ43	DQ47	160	MEM_B_DQ<43>	BI 15 71
		161	VSS	VSS	162		
71 15 BI	MEM_B_DQ<52>	163	DQ48	DQ52	164	MEM_B_DQ<53>	BI 15 71
71 15 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<48>	BI 15 71
		167	VSS	VSS	168		
71 15 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15 71
71 15 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<51>	BI 15 71
71 15 BI	MEM_B_DQ<55>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 15 71
71 15 BI	MEM_B_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<63>	BI 15 71
71 15 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<59>	BI 15 71
71 15 BI	MEM_B_DQ<58>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 15 71
71 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15 71
		189	VSS	VSS	190		
71 15 BI	MEM_B_DQ<61>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 15 71
71 15 BI	MEM_B_DQ<60>	193	DQ59	DQ63	194	MEM_B_DQ<57>	BI 15 71
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	MUX 21 27 36
8 =PPSPD_S0_MEM_B		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 39
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 39
		203	VTT	VTT	204		=PP0V75_S0_MEM_VTT_B 8
	MTG PINS	205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

DDR3-SODIMM (1 OF 2) — J3200 F-RT-BGA3 (CRITICAL)

KEY

		1	VREFDQ	VSS	2
71 15 BI	MEM_B_DQ<1>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15 71
71 15 BI	MEM_B_DQ<0>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15 71
		7	DQ1	VSS	8		
71 15 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15 71
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15 71
		13	VSS	VSS	14		
71 15 BI	MEM_B_DQ<7>	15	DQ2	DQ6	16	MEM_B_DQ<3>	BI 15 71
71 15 BI	MEM_B_DQ<6>	17	DQ3	DQ7	18	MEM_B_DQ<2>	BI 15 71
		19	VSS	VSS	20		
71 15 BI	MEM_B_DQ<13>	21	DQ8	DQ12	22	MEM_B_DQ<12>	BI 15 71
71 15 BI	MEM_B_DQ<14>	23	DQ9	DQ13	24	MEM_B_DQ<9>	BI 15 71
		25	VSS	VSS	26		
71 15 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28	MEM_B_DM<1>	IN 15 71
71 15 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 27 29
		31	VSS	VSS	32		
71 15 BI	MEM_B_DQ<15>	33	DQ10	DQ14	34	MEM_B_DQ<8>	BI 15 71
71 15 BI	MEM_B_DQ<10>	35	DQ11	DQ15	36	MEM_B_DQ<11>	BI 15 71
		37	VSS	VSS	38		
71 15 BI	MEM_B_DQ<20>	39	DQ16	DQ20	40	MEM_B_DQ<22>	BI 15 71
71 15 BI	MEM_B_DQ<17>	41	DQ17	DQ21	42	MEM_B_DQ<16>	BI 15 71
		43	VSS	VSS	44		
71 15 BI	MEM_B_DQS_N<2>	45	DQS2*	DM2	46	MEM_B_DM<2>	IN 15 71
71 15 BI	MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<21>	BI 15 71
71 15 BI	MEM_B_DQ<18>	51	DQ18	DQ23	52	MEM_B_DQ<23>	BI 15 71
71 15 BI	MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<29>	BI 15 71
71 15 BI	MEM_B_DQ<24>	57	DQ24	DQ29	58	MEM_B_DQ<25>	BI 15 71
71 15 BI	MEM_B_DQ<28>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<3>	BI 15 71
71 15 IN	MEM_B_DM<3>	63	DM3	DQS3	64	MEM_B_DQS_P<3>	BI 15 71
		65	VSS	VSS	66		
71 15 BI	MEM_B_DQ<30>	67	DQ26	DQ30	68	MEM_B_DQ<26>	BI 15 71
71 15 BI	MEM_B_DQ<27>	69	DQ27	DQ31	70	MEM_B_DQ<31>	BI 15 71
		71	VSS	VSS	72		

516S0706

PP0V75_S3_MEM_VREFCA_B 26

DDR3 GROUND RETURN CAPS (MCP SIDE)

8 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402
C3224 0.1UF 20% 10V CERM 402
C3225 0.1UF 20% 10V CERM 402
C3226 0.1UF 20% 10V CERM 402
C3227 0.1UF 20% 10V CERM 402
C3228 0.1UF 20% 10V CERM 402
C3229 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

SYNC MASTER=K24_MLB SYNC DATE=02/05/2009
PAGE TITLE
DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
BRANCH
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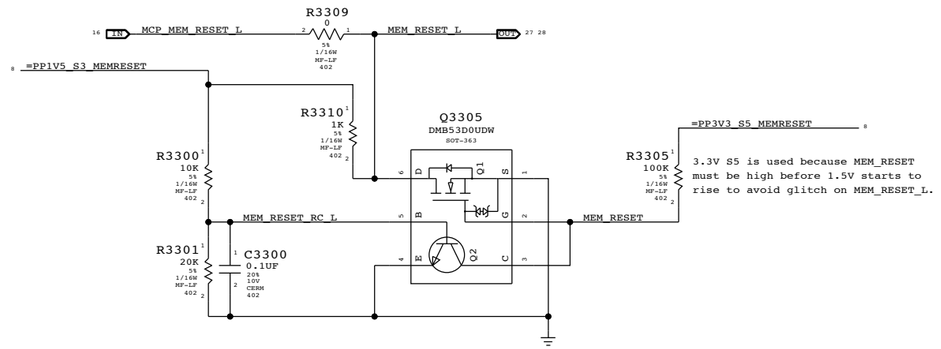
DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE: DDR3 Support

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: 14.5.0

BRANCH:

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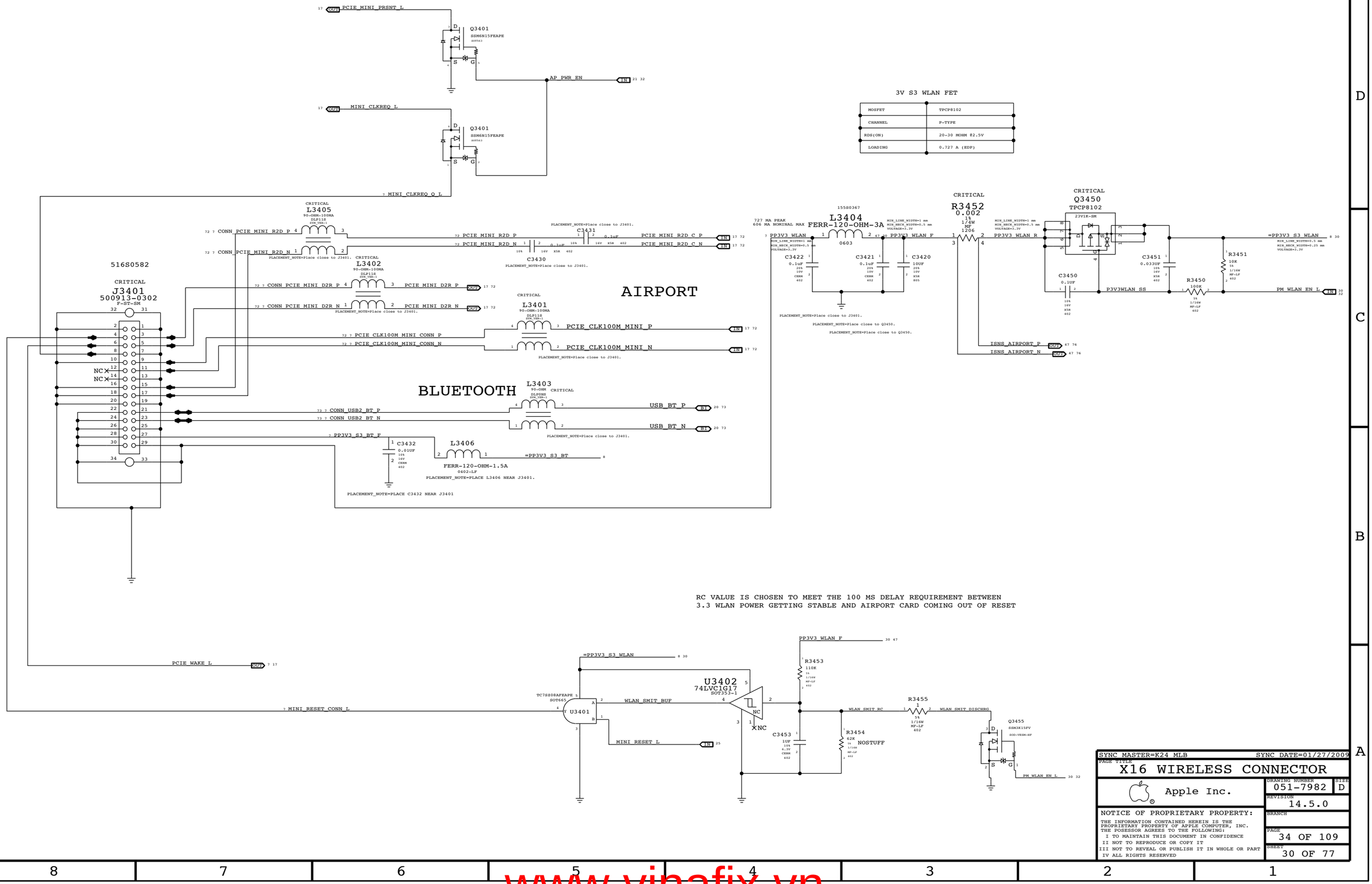

SYNC MASTER=K24 MLB SYNC DATE=01/27/2009

PAGE TITLE
X16 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
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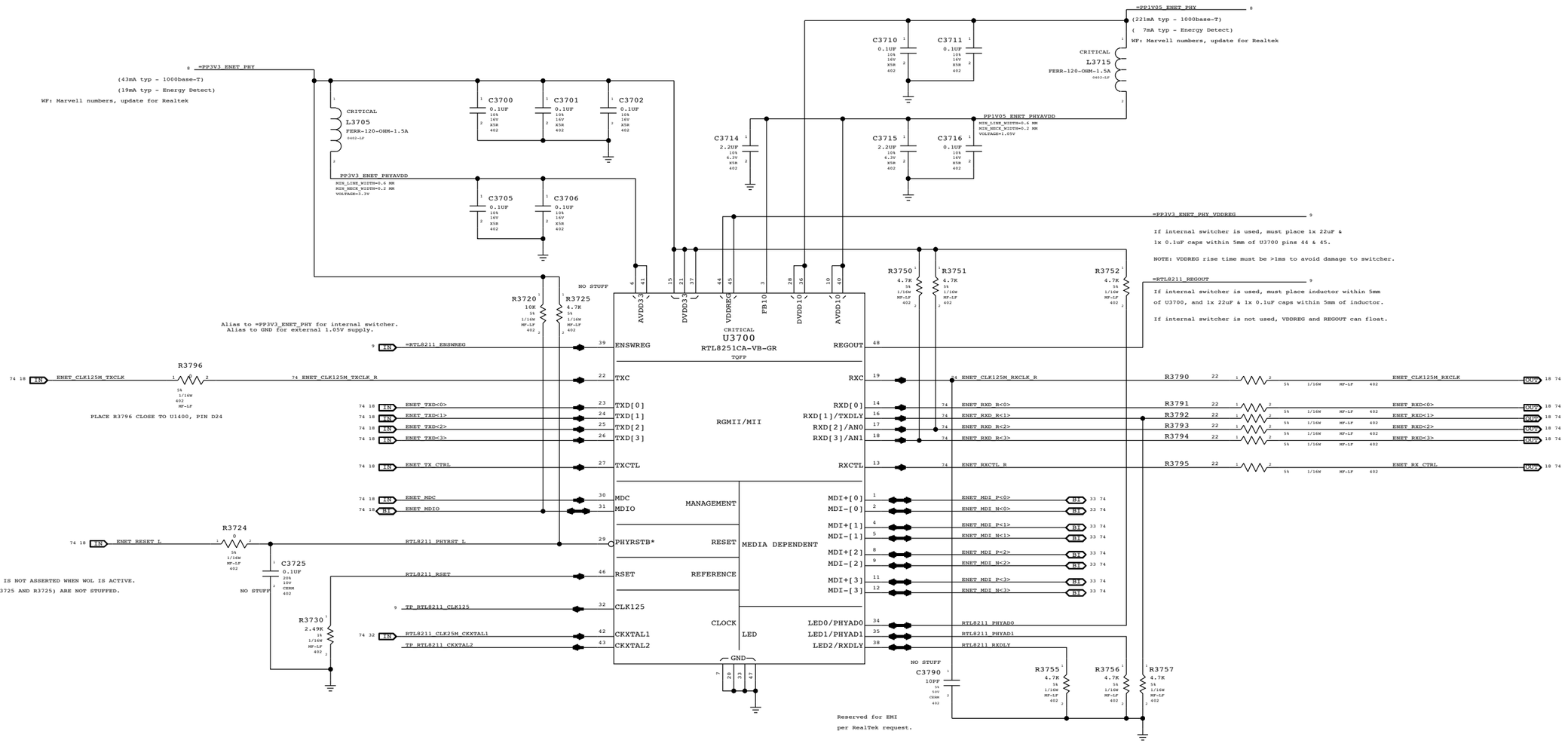

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
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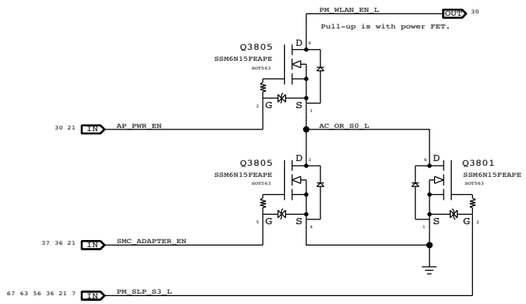
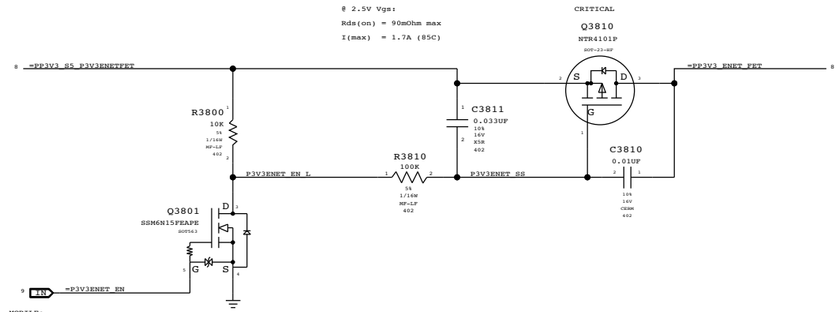
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



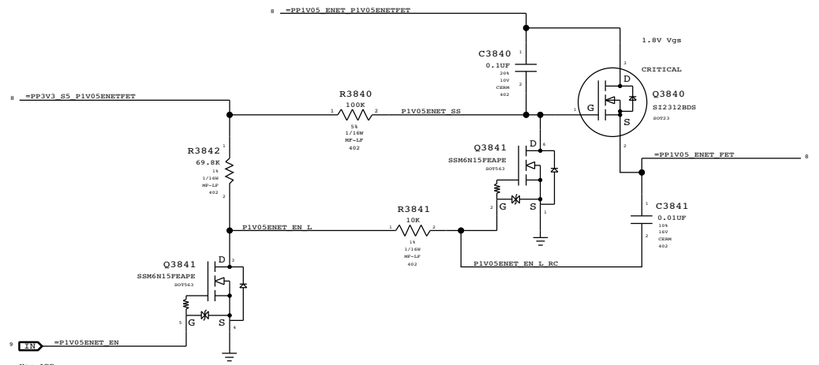
3.3V ENET FET



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

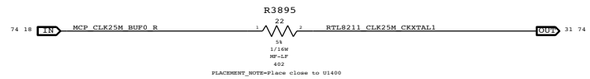


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE: Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: 14.5.0

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- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901 SM
TX
TLA-6T213HF
RX

CRITICAL
T3902 SM
TX
TLA-6T213HF
RX

R3903 75 1% 1/16W MF-LF 402
R3902 75 1% 1/16W MF-LF 402
R3901 75 1% 1/16W MF-LF 402
R3900 75 1% 1/16W MF-LF 402

74 31 B1 ENET_MDI_P<1>
74 31 B1 ENET_MDI_N<1>
74 31 B1 ENET_MDI_P<3>
74 31 B1 ENET_MDI_N<3>
74 31 B1 ENET_MDI_N<2>
74 31 B1 ENET_MDI_P<2>
74 31 B1 ENET_MDI_N<0>
74 31 B1 ENET_MDI_P<0>

ENET_CENTER_TAP<1>
ENET_CENTER_TAP<3>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<0>

74 ENET_MDI_TRAN_P<1>
74 ENET_MDI_TRAN_N<1>
74 ENET_MDI_TRAN_P<3>
74 ENET_MDI_TRAN_N<3>
74 ENET_MDI_TRAN_N<2>
74 ENET_MDI_TRAN_P<2>
74 ENET_MDI_TRAN_N<0>
74 ENET_MDI_TRAN_P<0>

C3911 10PF 5% 50V CERM 402-1 CRITICAL
C3912 10PF 5% 50V CERM 402-1 CRITICAL
C3913 10PF 5% 50V CERM 402-1 CRITICAL
C3914 10PF 5% 50V CERM 402-1 CRITICAL
C3915 10PF 5% 50V CERM 402-1 CRITICAL
C3916 10PF 5% 50V CERM 402-1 CRITICAL
C3917 10PF 5% 50V CERM 402-1 CRITICAL
C3918 10PF 5% 50V CERM 402-1 CRITICAL

PLACEMENT_NOTE=PLACE C3911-C3918 ON MDI LINES WITHOUT ANY STUBS

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-10/100TX-K83
F-R-TH

1 ENET_MDI TRAN_P0
2 TRAN_N0
3 TRAN_P1
4 TRAN_P2
5 TRAN_N2
6 TRAN_N1
7 TRAN_P3
8 TRAN_N3
9 10 11 12 SHIELD PINS

514-0692

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE: ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D
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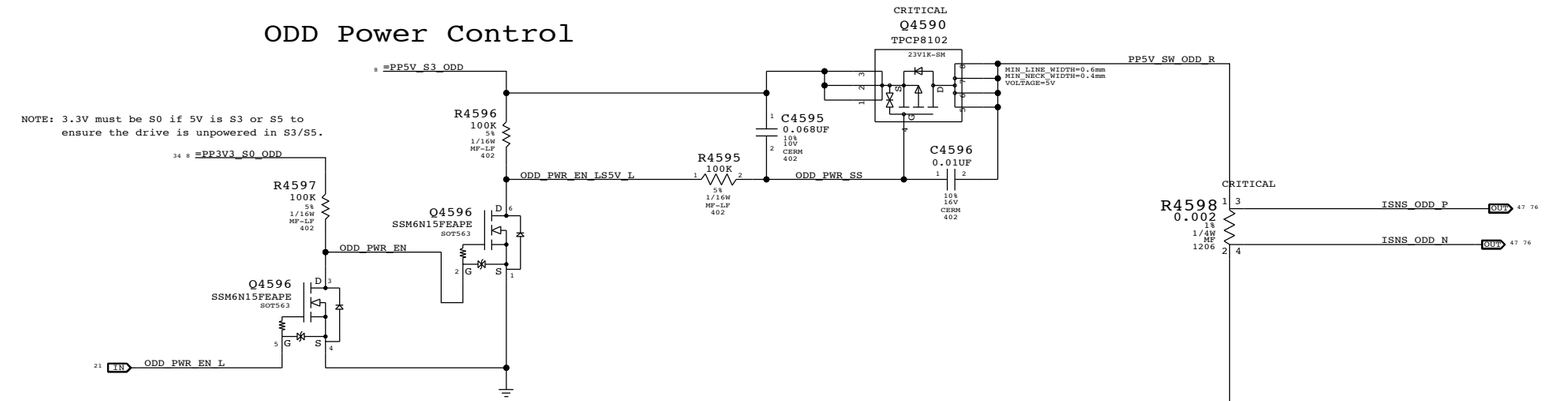
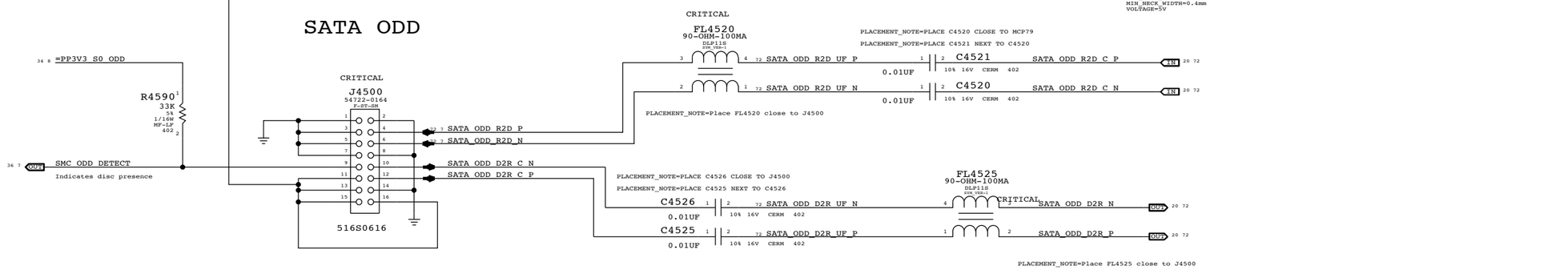
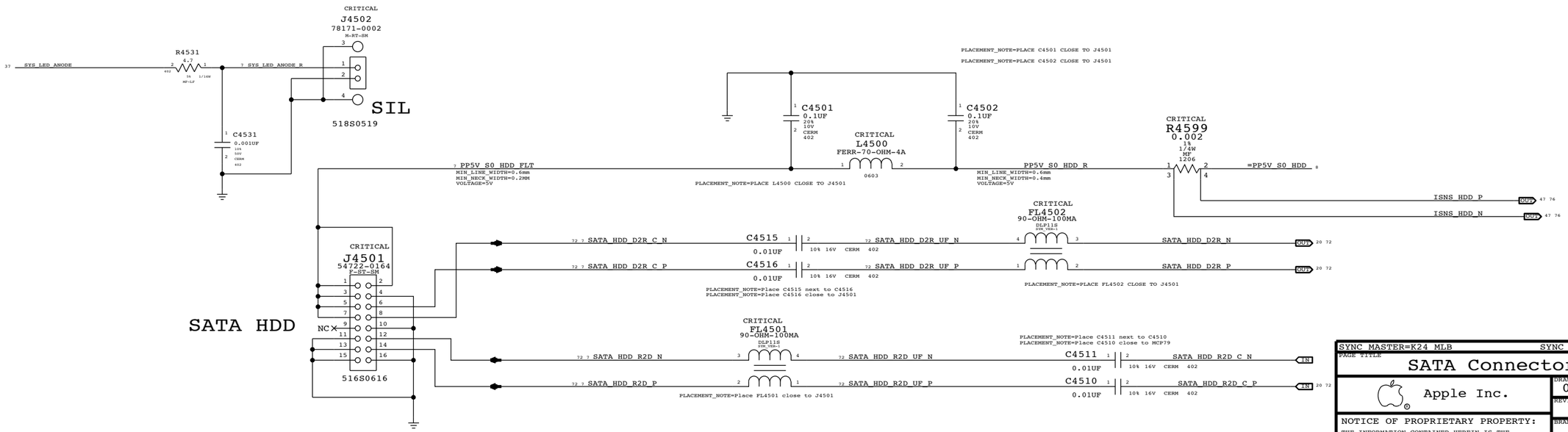
ODD Power Control



SATA ODD



SATA HDD



SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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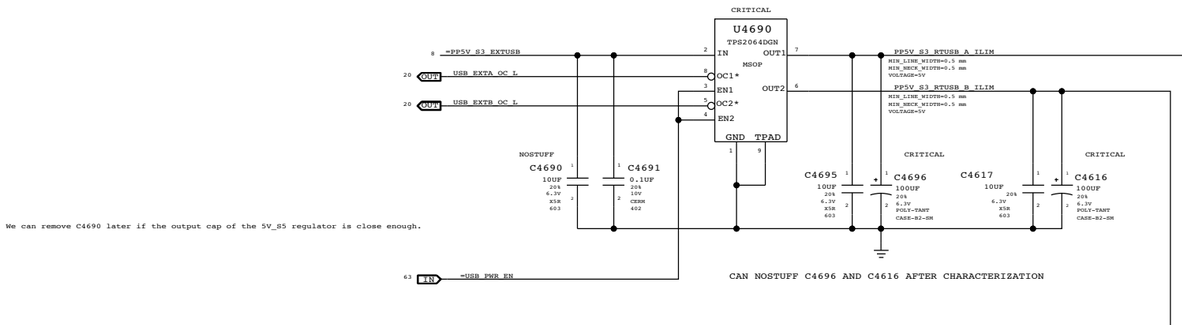
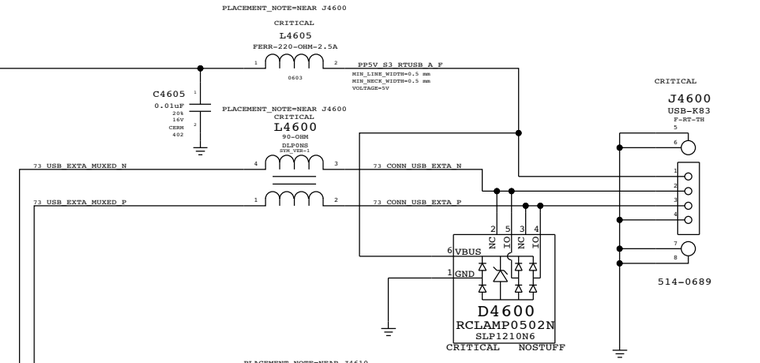
POR IS PLASTIC USB CONNECTOR PARTS BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS
HAVE BEEN USED AS ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch

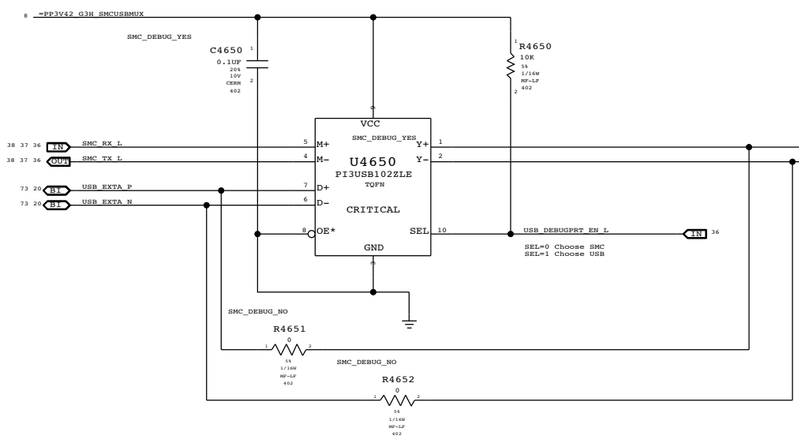


We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

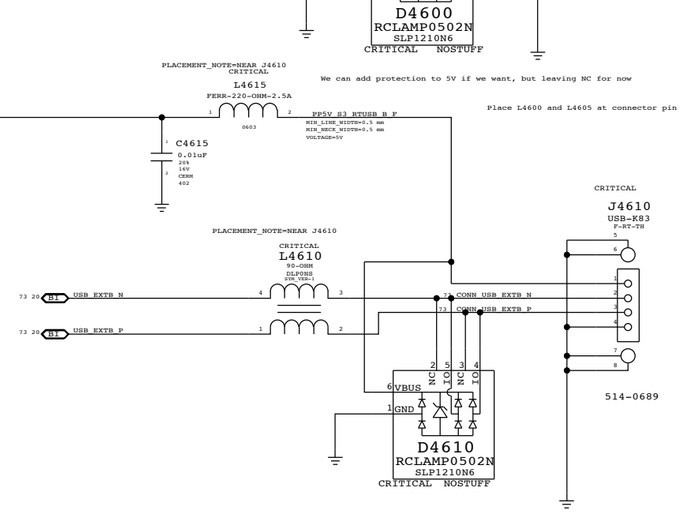
USB PORT A (FRONT PORT)



USB/SMC Debug Mux



USB PORT B (BACK PORT)



SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

PAGE TITLE
External USB Connectors

Apple Inc.

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REVISION 14.5.0
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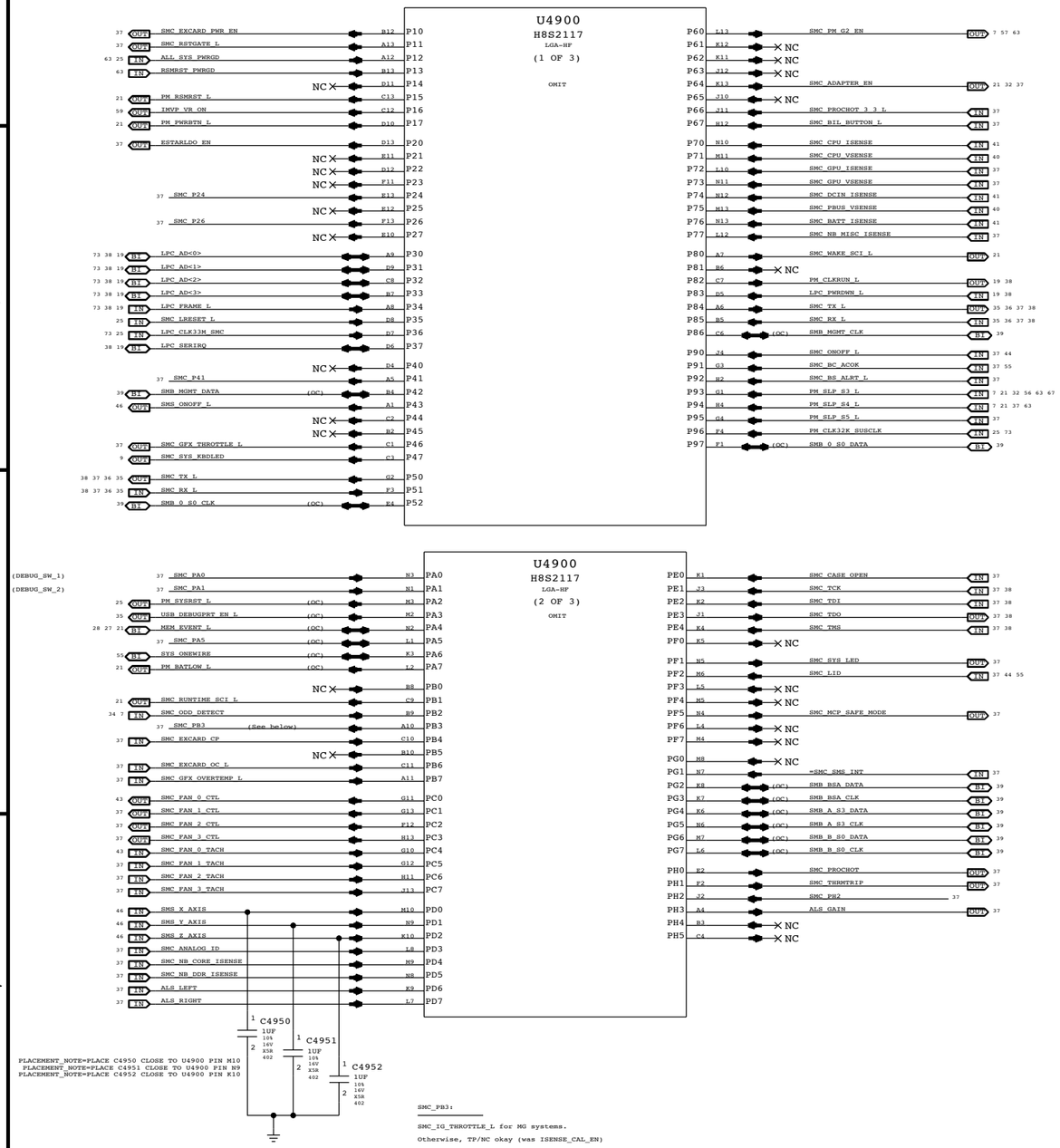
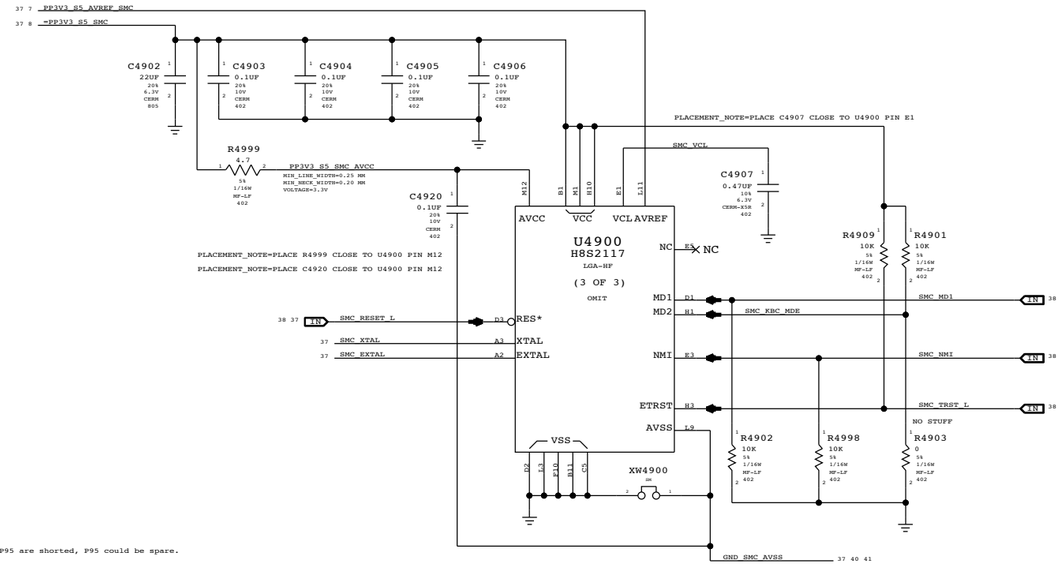
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC MASTER=K24 MLB						SYNC DATE=04/02/2009	
PAGE TITLE: SMC							
Apple Inc.						DRAWING NUMBER 051-7982	SIZE D
						REVISION 14.5.0	
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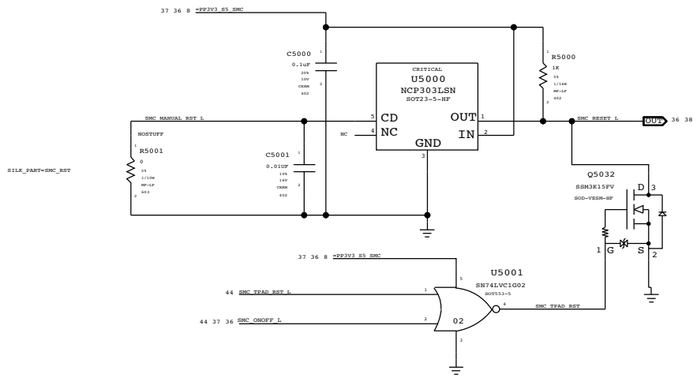
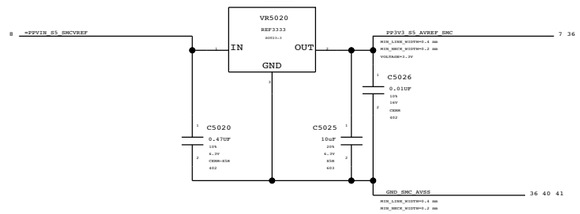
						PAGE 49 OF 109	
						SHEET 36 OF 77	

SMC Reset "Button" / Brownout Detect

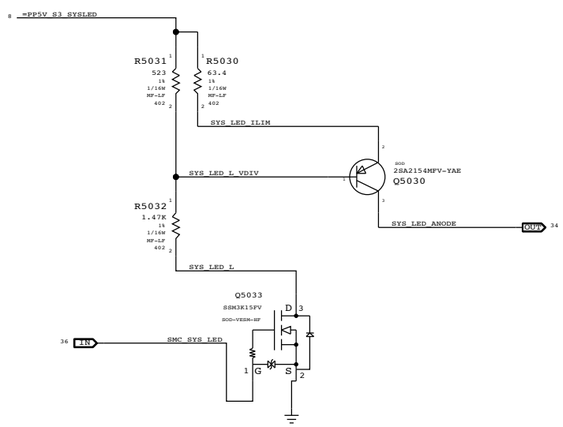


SMC AVREF Supply

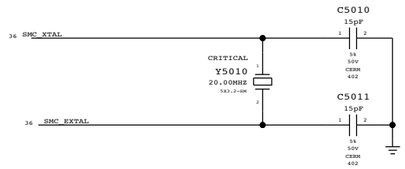


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL6000Z-33, INTERSIL

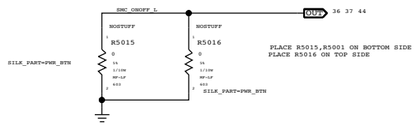
System (Sleep) LED Circuit



SMC Crystal Circuit

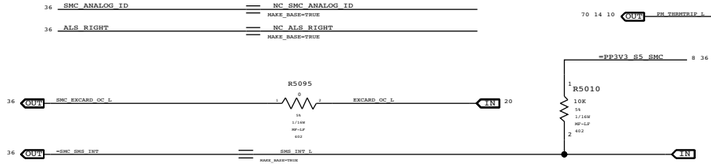


Debug Power "Button"

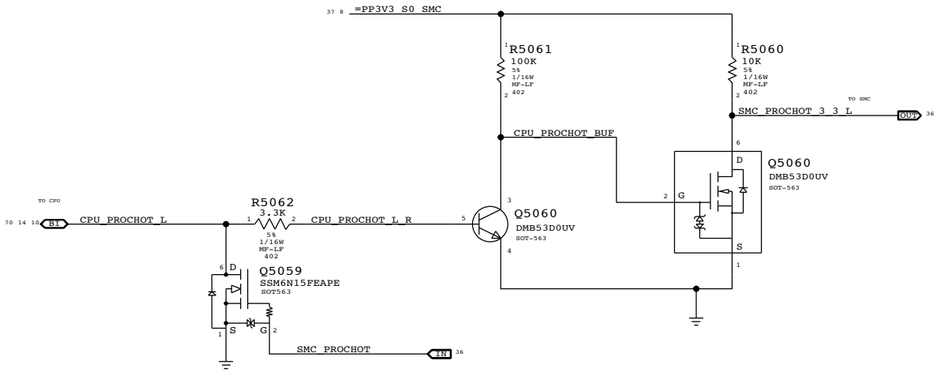


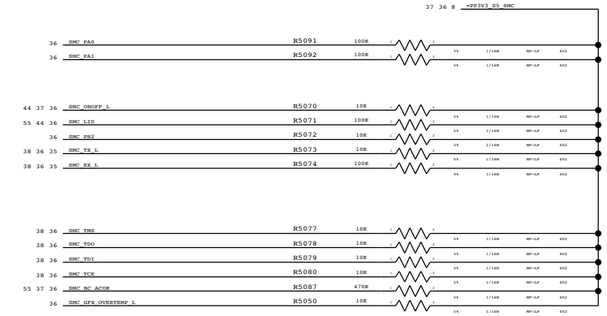
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

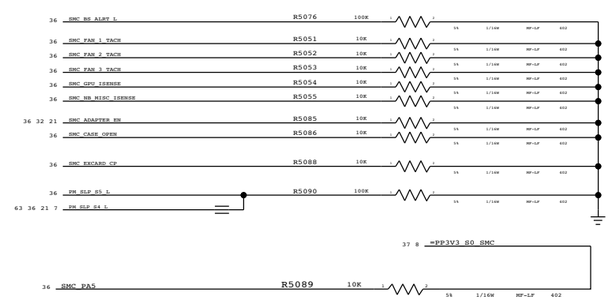
RADAR 5925345



SMC FSB to 3.3V Level Shifting







SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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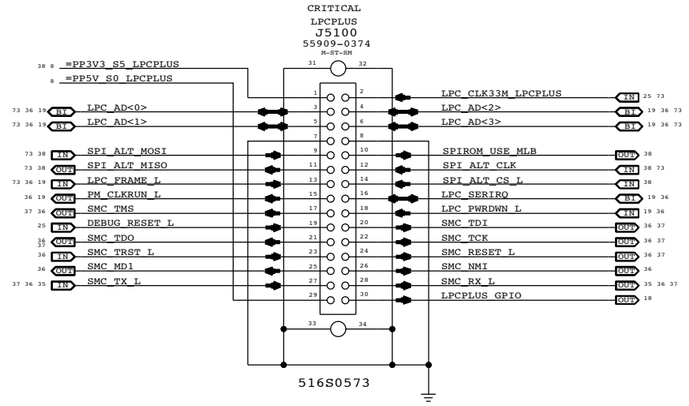
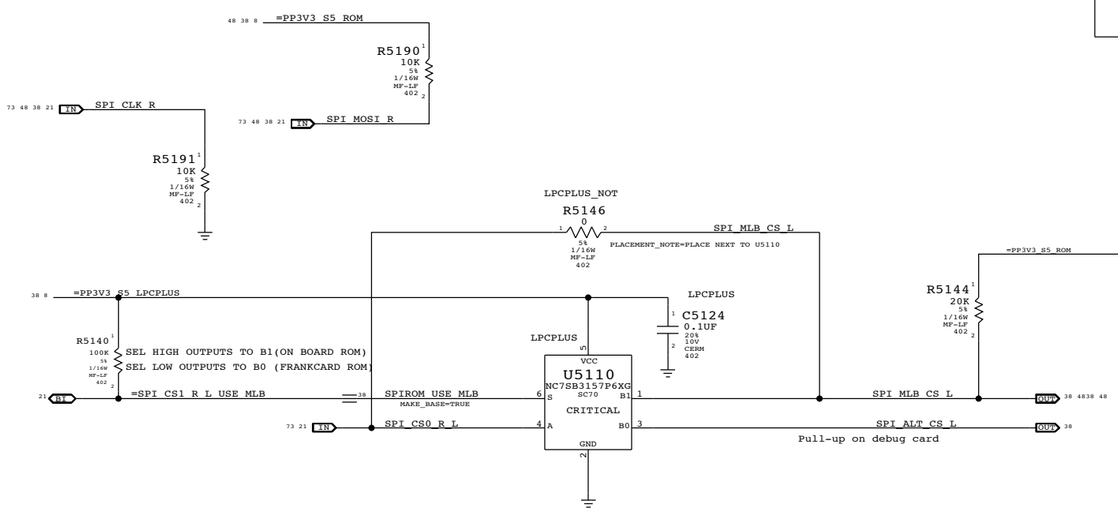
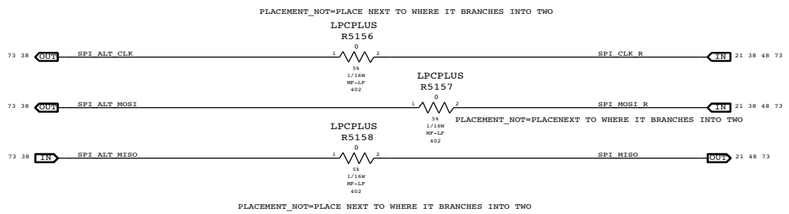
LPC+SPI Connector

CRITICAL
LPCPLUS
J5100
55909-0374
M-ST-SM



Alternate SPI ROM Support





SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION 14.5.0
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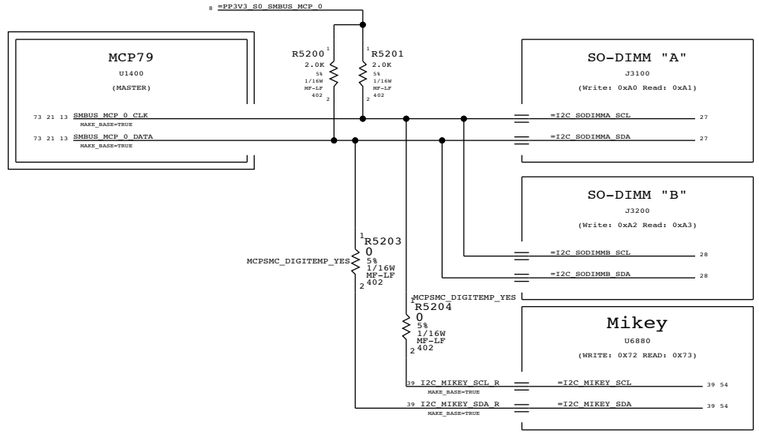
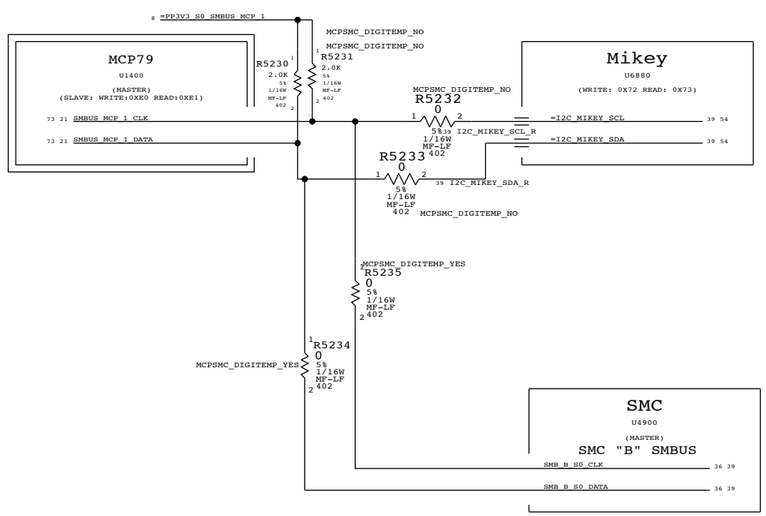
MCP79 SMBUS "0" CONNECTIONS

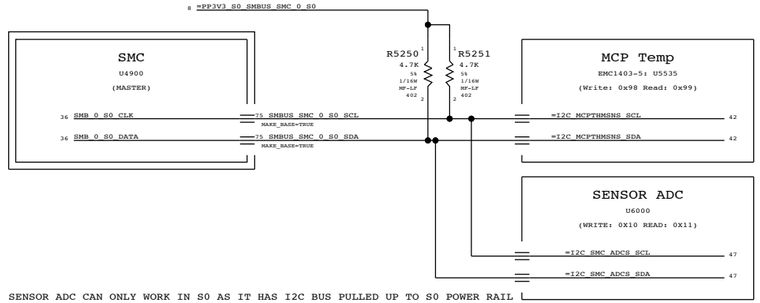


MCP79 SMBUS "1" CONNECTIONS



MCP SMBUS1 ACTS AS SLAVE DEVICE FOR MCPSMC_DIGITEMP_YES STUFFED

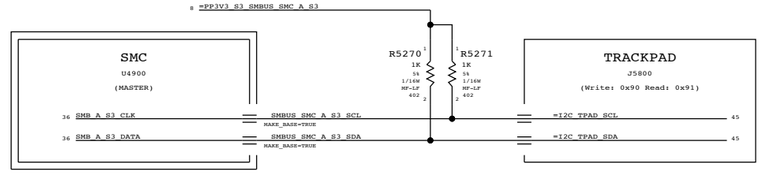
SMC "0" SMBus Connections



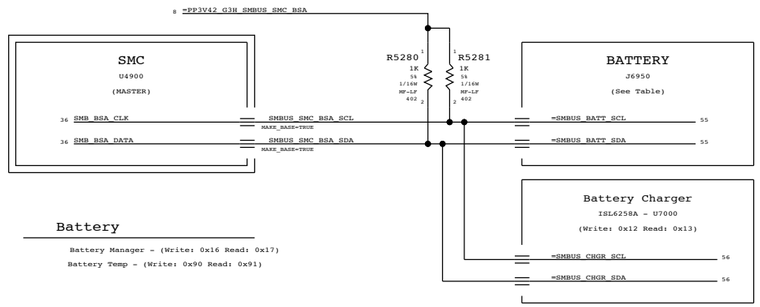
SENSOR ADC CAN ONLY WORK IN S0 AS IT HAS I2C BUS PULLED UP TO S0 POWER RAIL

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections

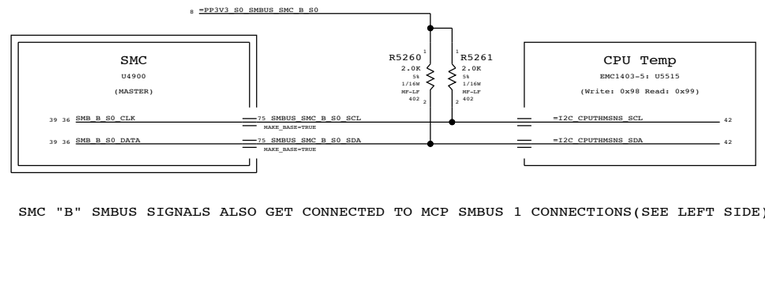


Battery

Battery Manager - (Write: 0x16 Read: 0x17)

Battery Temp - (Write: 0x90 Read: 0x91)

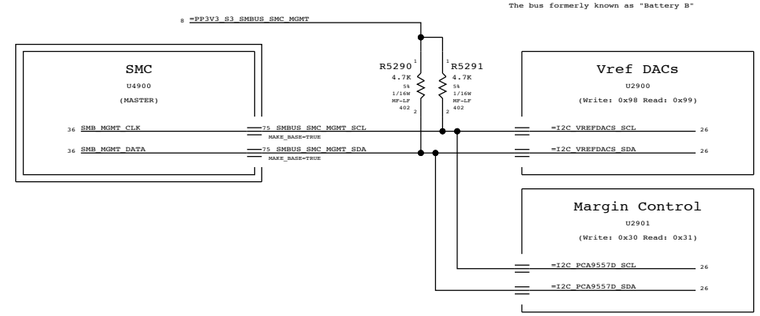
SMC "B" SMBus Connections



SMC "B" SMBUS SIGNALS ALSO GET CONNECTED TO MCP SMBUS 1 CONNECTIONS(SEE LEFT SIDE)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

PAGE TITLE

K84 SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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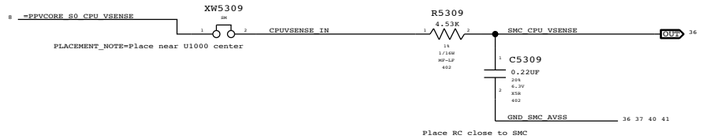
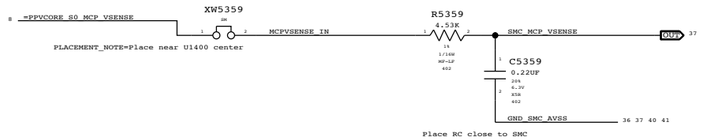
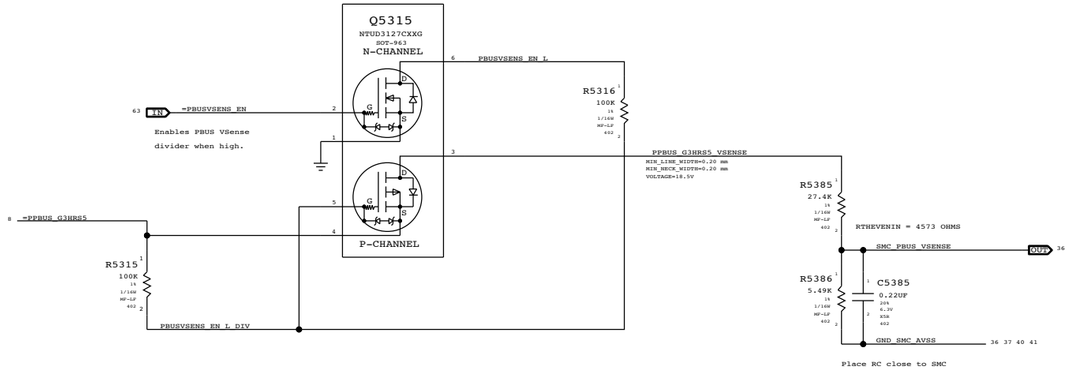
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

VOLTAGE SENSING

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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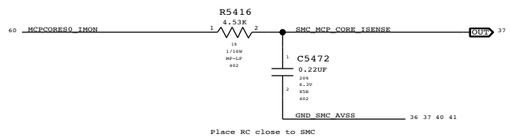
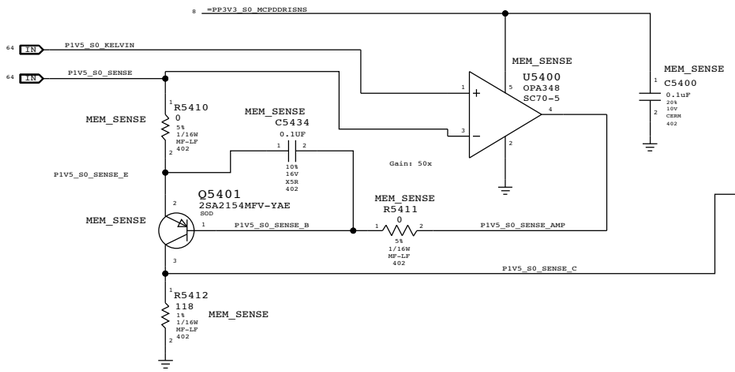
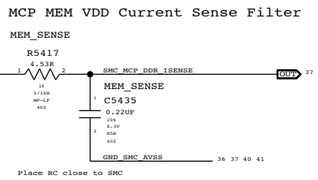
MCP VCore Current Sense Filter



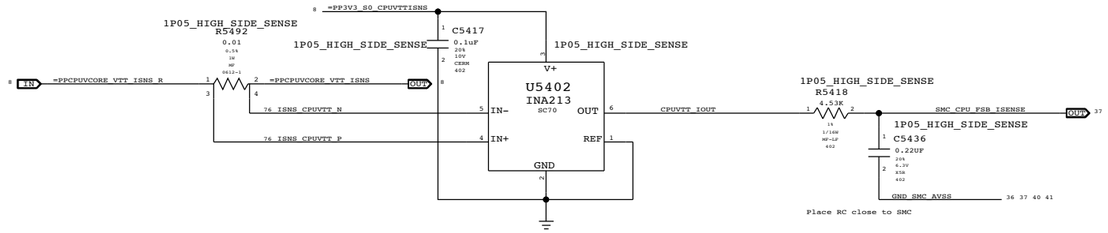
MCP MEM VDD Current Sense



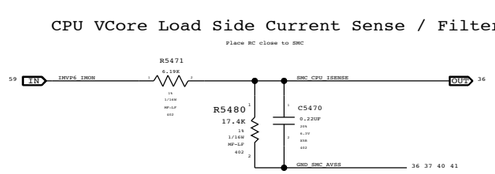
MCP MEM VDD Current Sense Filter



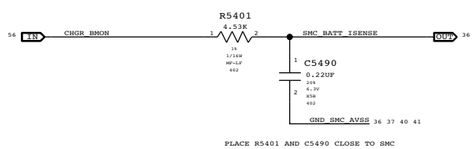
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



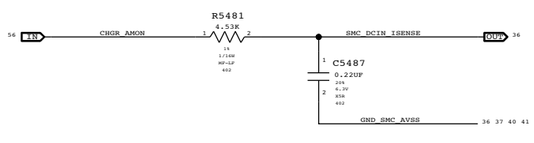
CPU VCore Load Side Current Sense / Filter



DC-IN (BMON) CURRENT SENSE



DC-IN (AMON) CURRENT SENSE



SYNC_MASTER=K24_MLB SYNC_DATE=01/27/2009

PAGE TITLE

Current Sensing

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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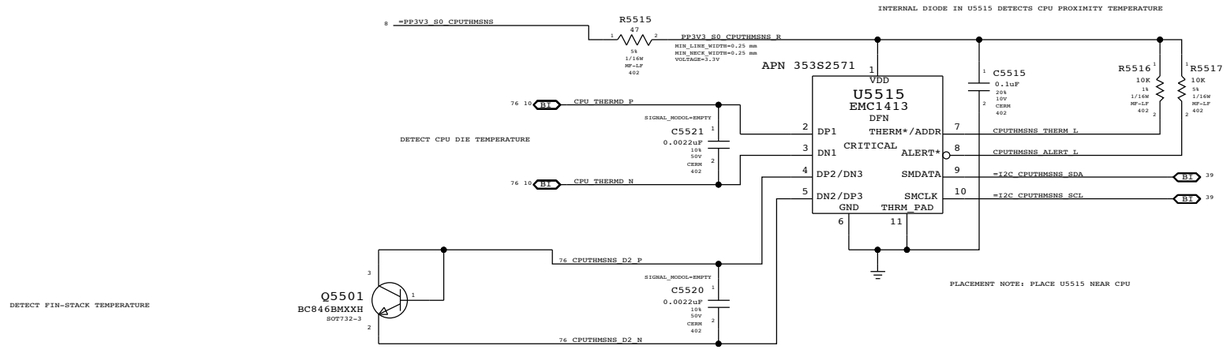
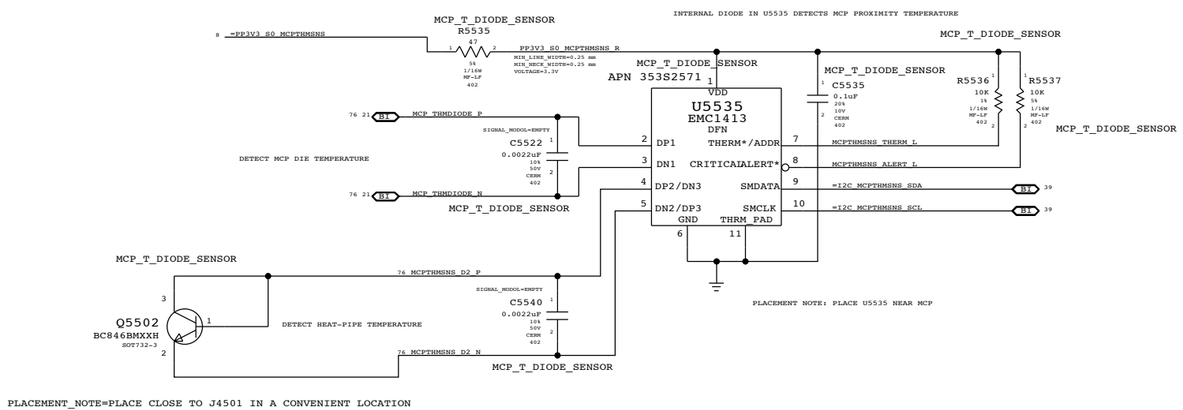
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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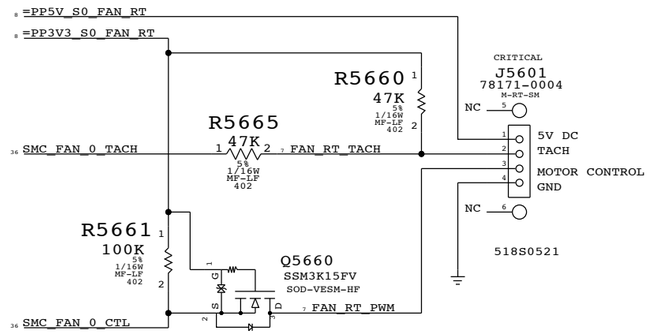

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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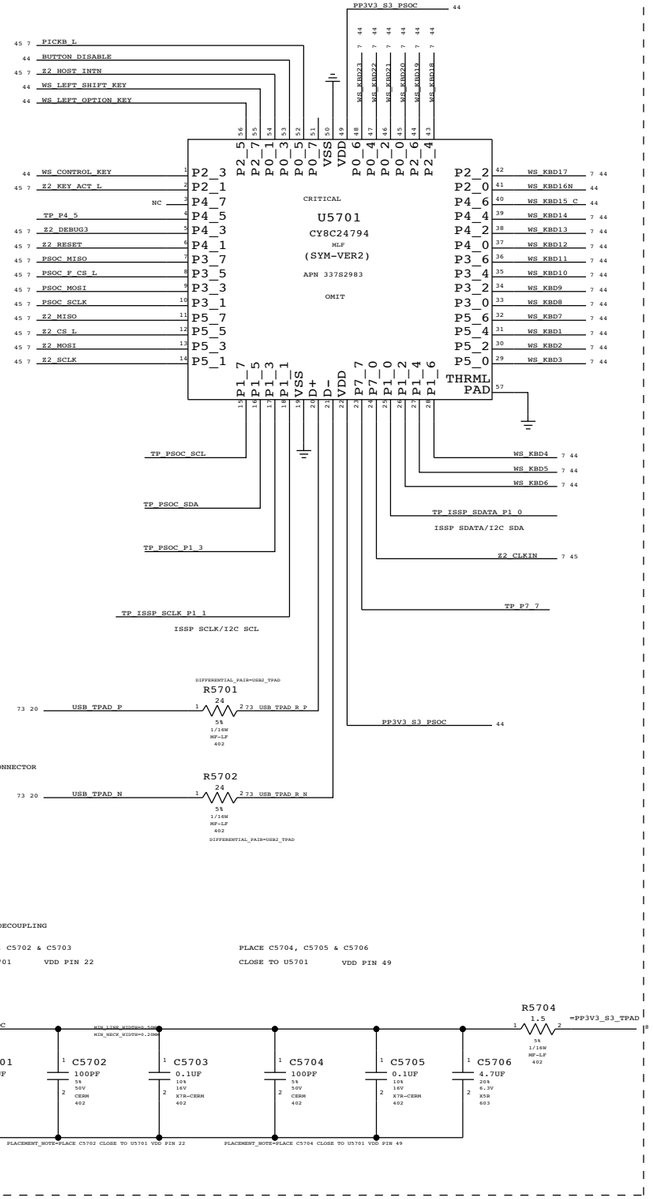
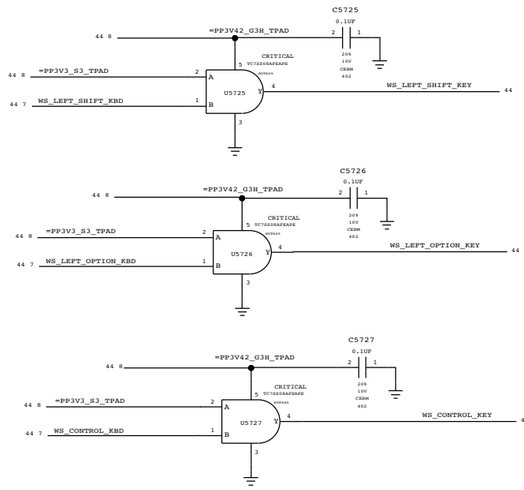
PSOC USB CONTROLLER

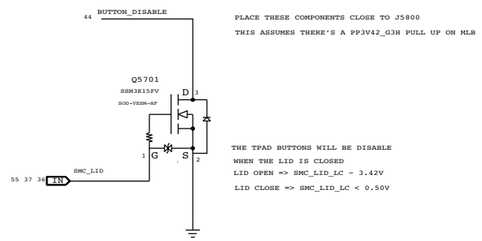


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

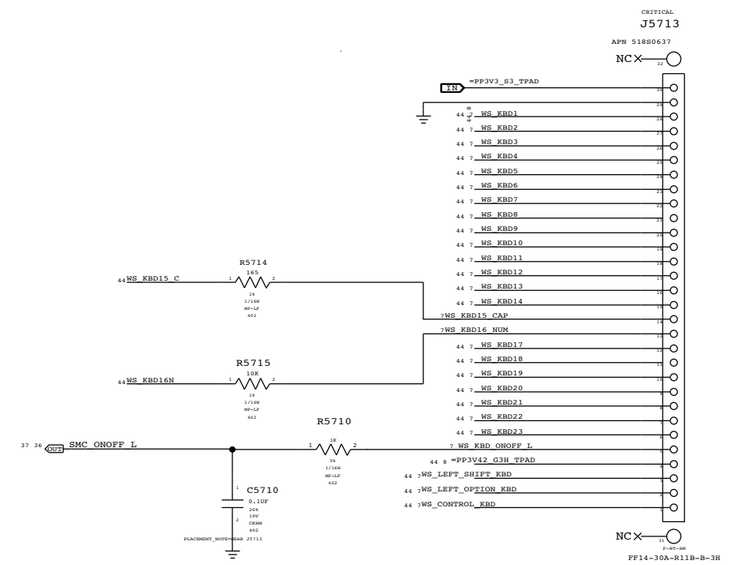
ISOLATION CIRCUIT



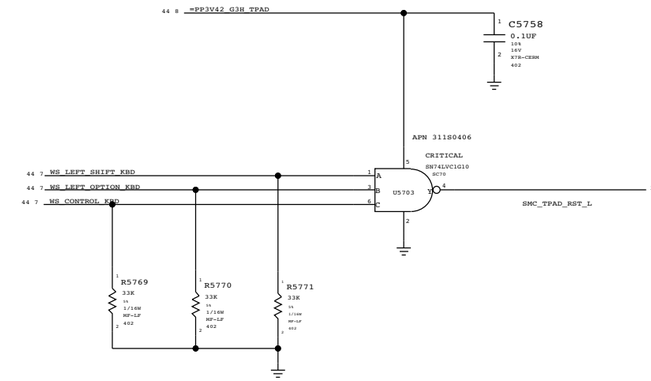
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180406	31180447		ALL	REP PART AS ALTERNATE

SYNC MASTER=K24 MLB SYNC DATE=03/04/2009

PAGE TITLE

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Apple Inc.

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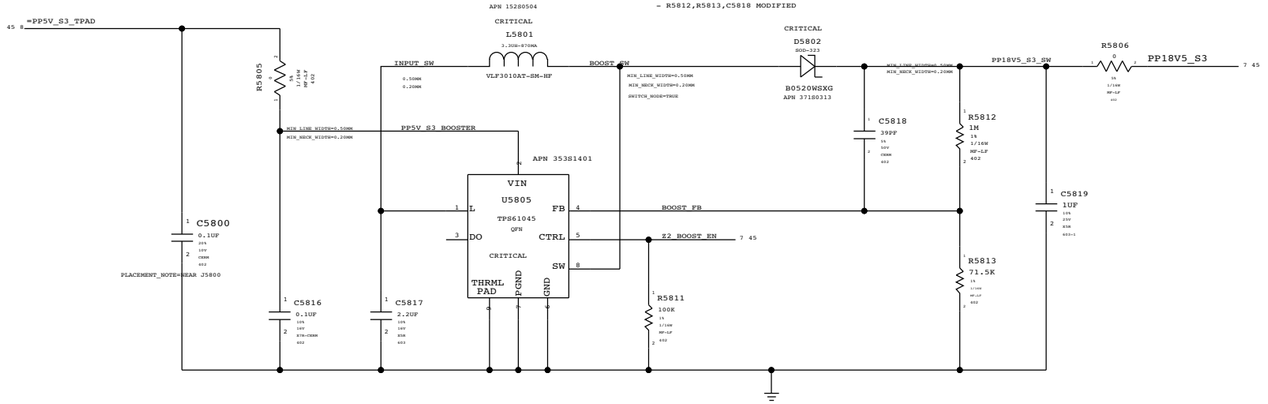
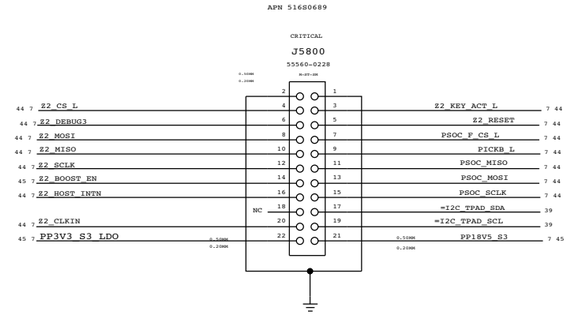
BOOSTER +18.5VDC FOR SENSORS

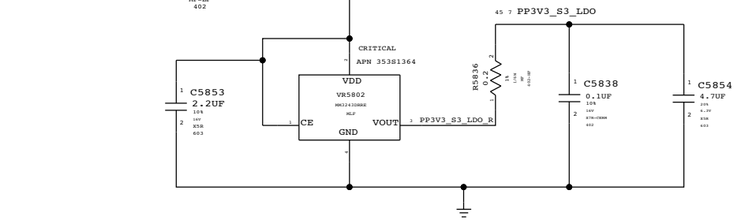
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



SYNC MASTER=K24 MLB SYNC DATE=02/25/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

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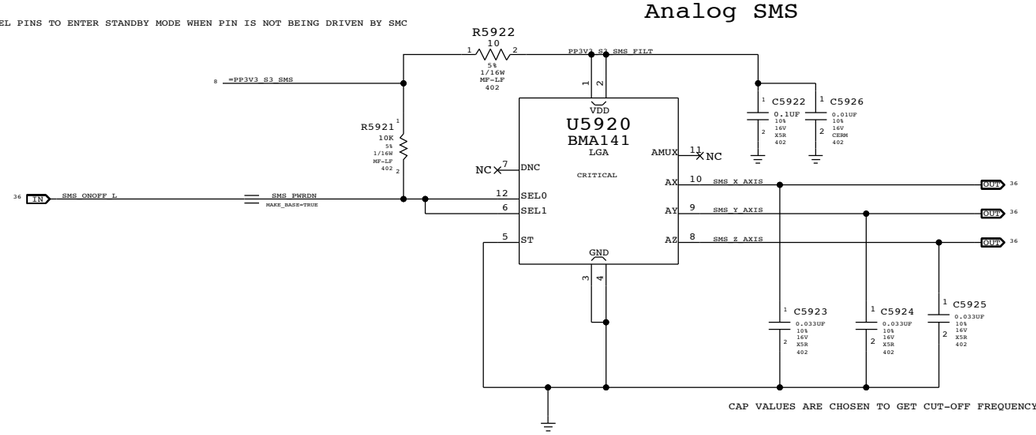
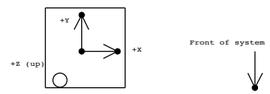
Analog SMS

R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

CAP VALUES ARE CHOSEN TO GET CUT-OFF FREQUENCY OF ~146HZ

PAGE TITLE: SMS

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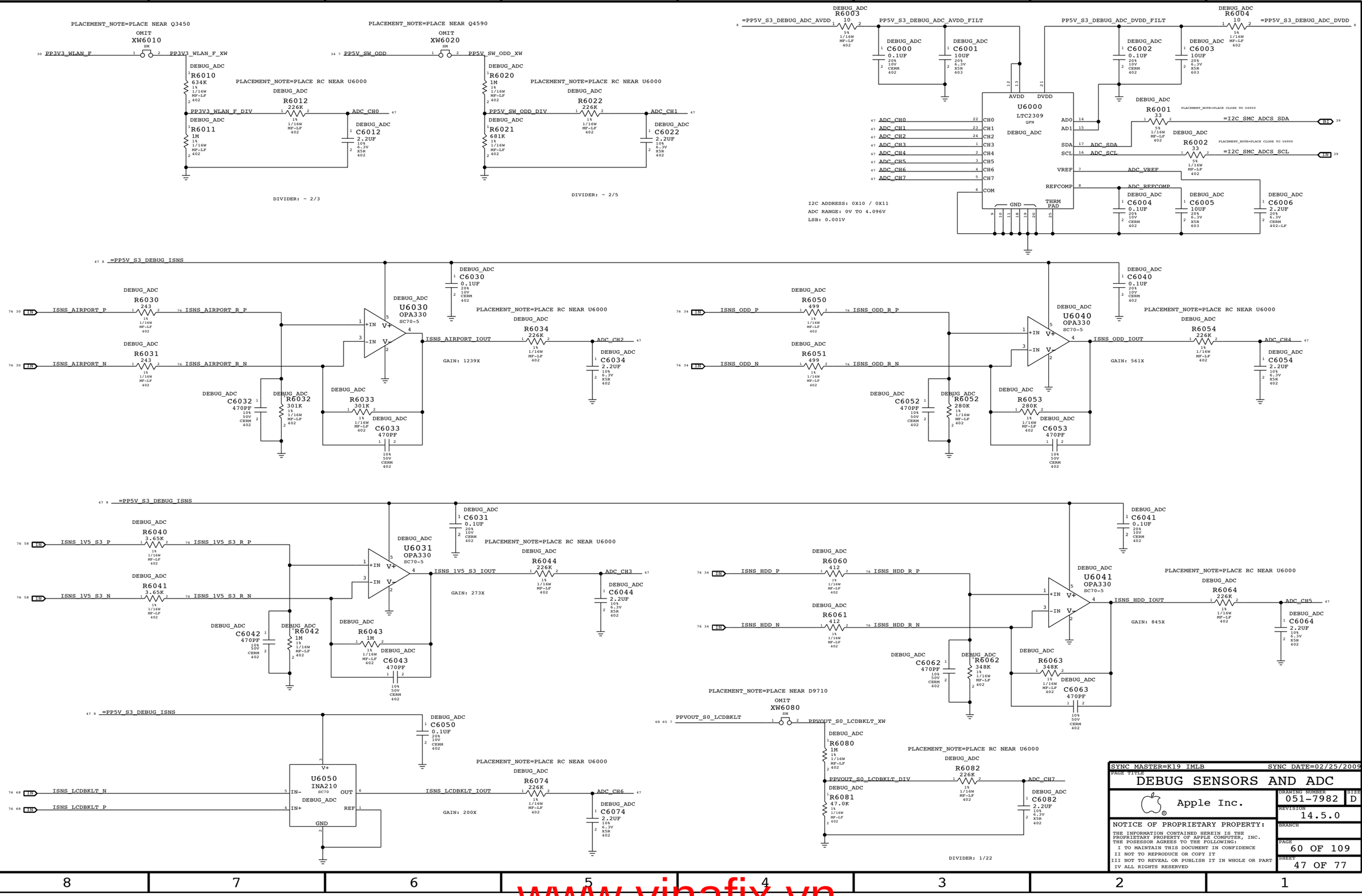

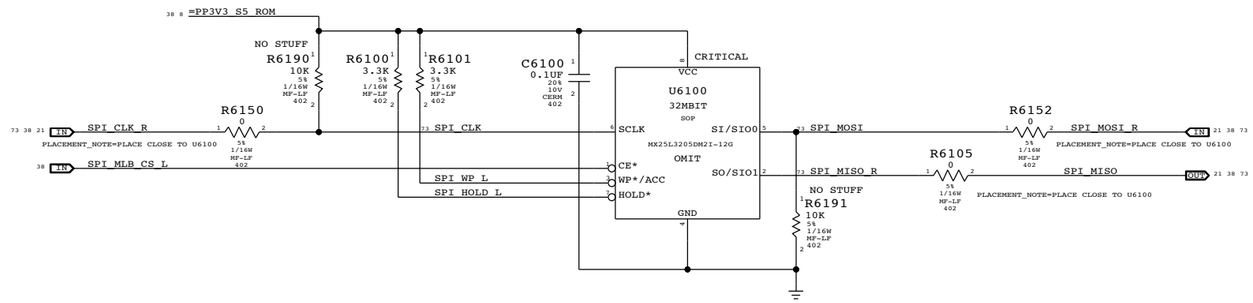

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
SPI ROM

Apple Inc.

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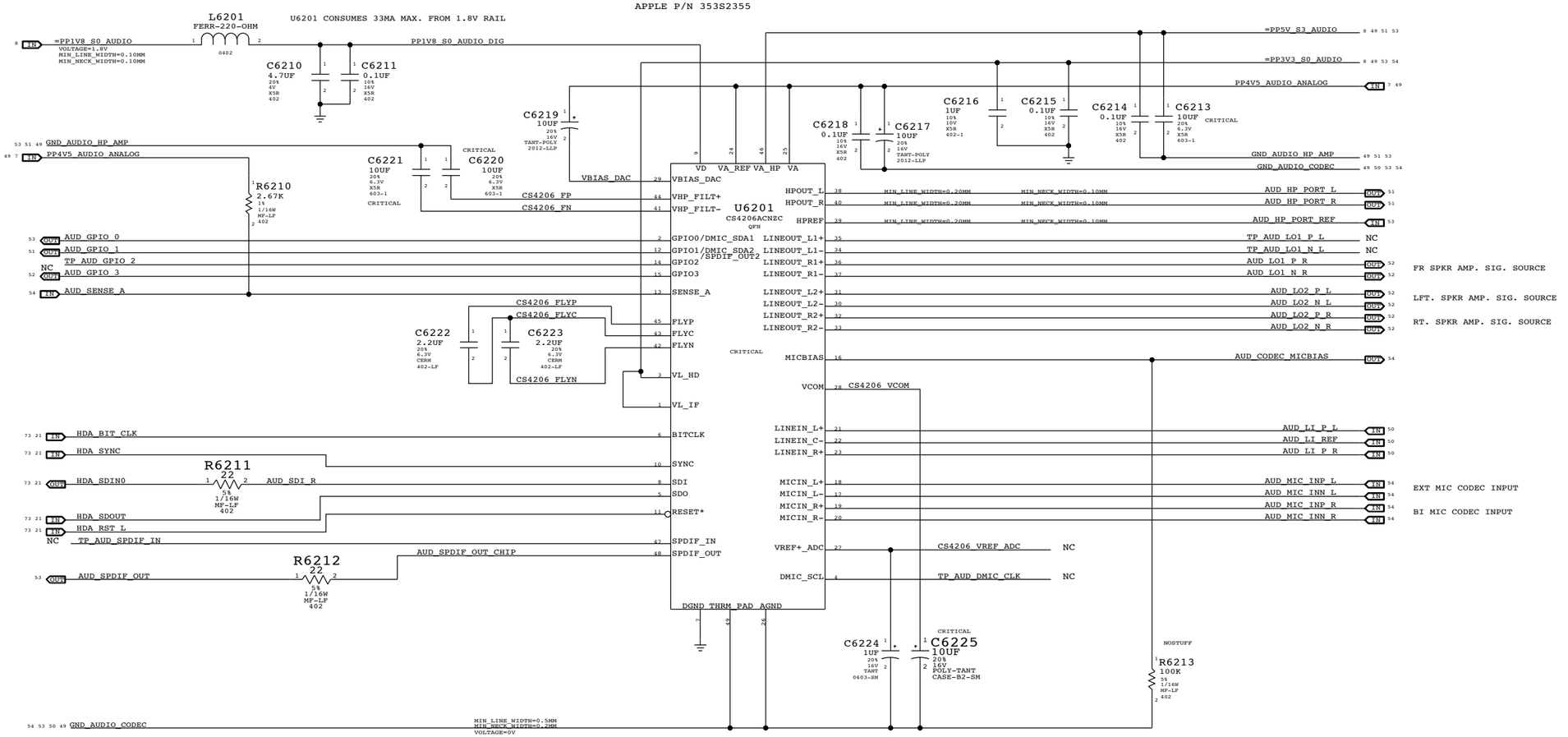
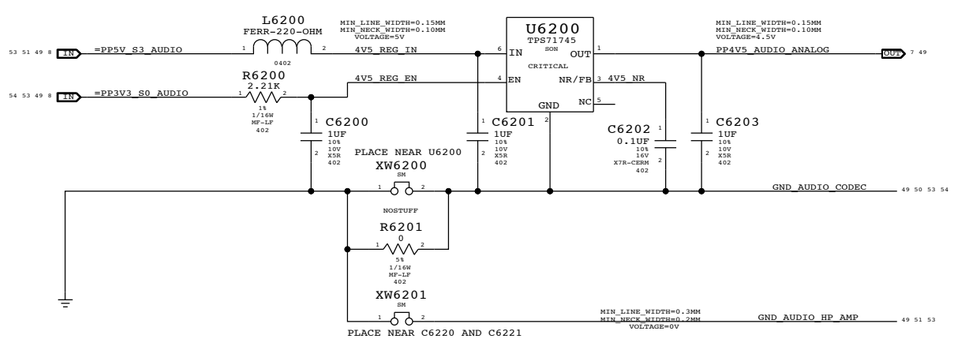
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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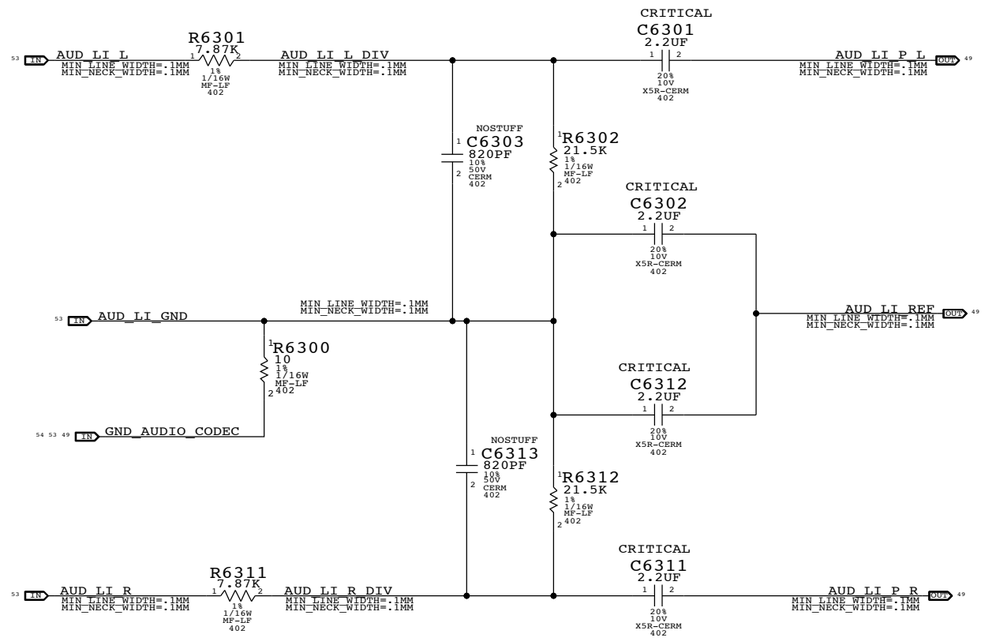
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

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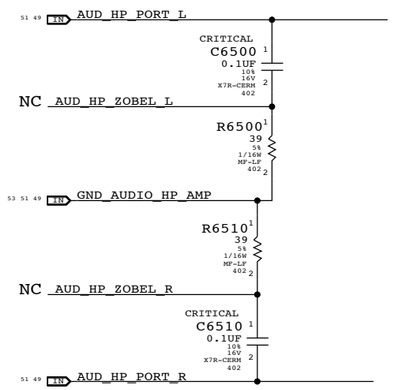
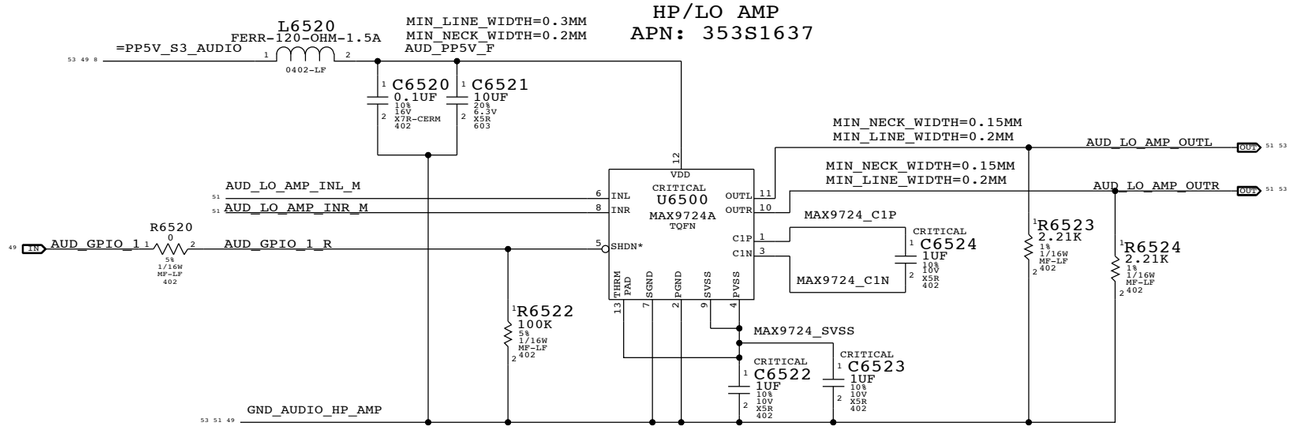
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

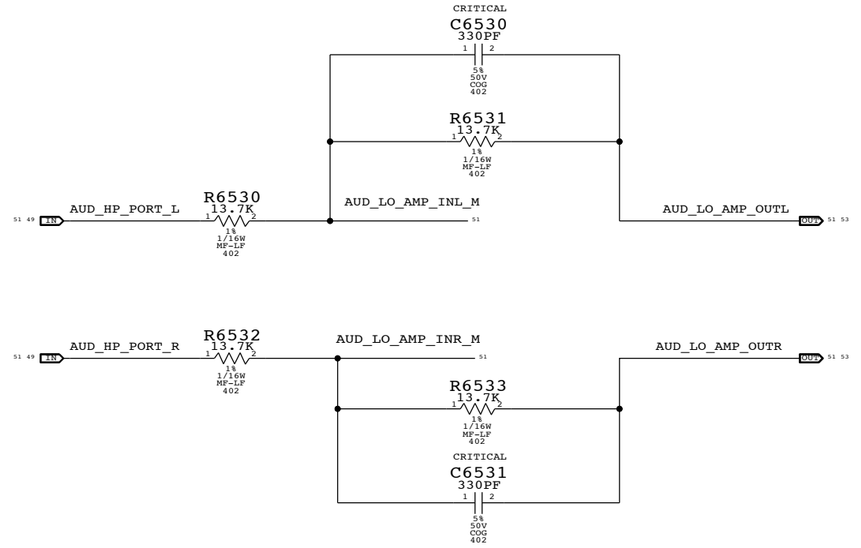


HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

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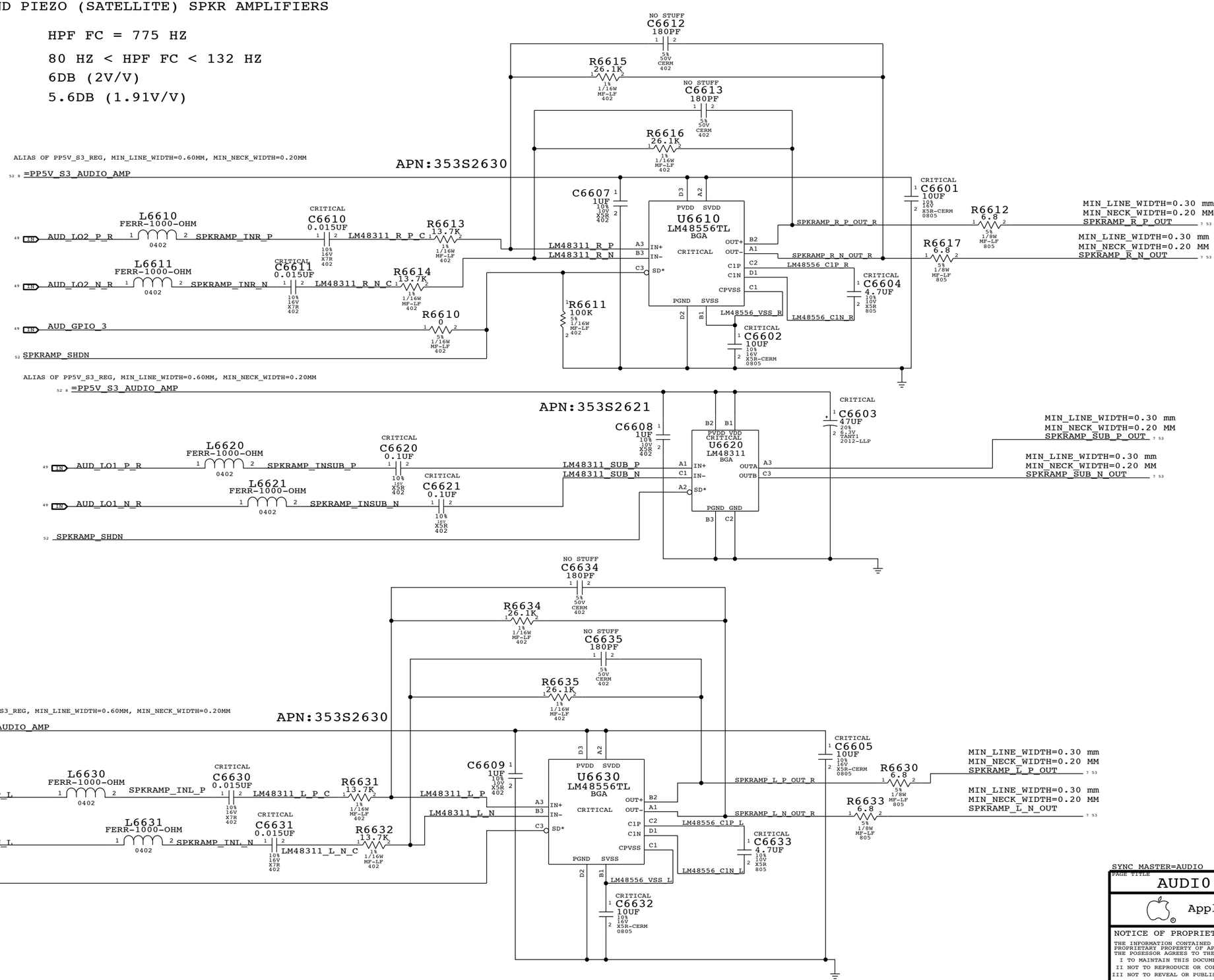
DYNAMIC (SUB) AND PIEZO (SATELLITE) SPKR AMPLIFIERS

SATELLITE	HPF FC = 775 HZ
SUB	80 HZ < HPF FC < 132 HZ
SUB GAIN	6DB (2V/V)
SAT GAIN	5.6DB (1.91V/V)



SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

54 49 8 =PP3V3_S0_AUDIO

APN:514-0694

J6700
AUDIO-JACK-TRANS-K83
F-RT-TH
CRITICAL

AUDIO
PHS_DETECT
GND
HP DETECT

A - VIN
B - VCC
C - GND

OPERATING VOLTAGE 3.3
POF

SHELL
SHIELD PINS

C6700 1UF 10% 6.3V CERM 402

AUD_SPDIF_OUT → OUT 49

L6701 FERR-1000-OHM 0402 → HS_MIC_HI OUT 54

L6702 FERR-1000-OHM 0402 → HS_MIC_LO OUT 54

AUD_CONNJ1_MIC

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE

CRITICAL
L6703 FERR-120-OHM-1.5A 0402-LF
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONN_GND

CRITICAL
L6704 FERR-220-OHM 0402 → AUD_CONN_L BI 53

CRITICAL
L6705 FERR-220-OHM 0402 → AUD_CONN_R BI 53

AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_IP_PERPH_DET_JACK
AUD_CONNJ1_TIPDET

L6706 FERR-1000-OHM 0402 → AUD_IP_PERPH_DET OUT 54

R6700 10K 5% 1/16W MF-LF 402 → AUD_J1_SLEEVEDET_R OUT 54

R6701 4.7 5% 1/16W MF-LF 402 → AUD_J1_TIPDET_R OUT 54

CRITICAL DZ6705 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402

C6701 100PF 5% 50V CERM 402

PLACE NEAR J6700
XW6702 EM
AUD_HP_PORT_REF OUT 49

PLACE NEAR J6700
XW6700 EM
GND_AUDIO_HP_AMP 49 51

PLACE NEAR J6700
XW6701 EM
AUD_LI_GND 50
AUD_CONN_GND 5353

MIC CONNECTOR

APN:518S0520

CRITICAL
J6701
78171-0003
M-RT-SM

54 7 BI_MIC_LO
54 7 BI_MIC_SHIELD
54 7 BI_MIC_HI

SPEAKER CONNECTORS

APN:518S0519

CRITICAL
J6702
78171-0002
M-RT-SM

52 7 IN SPKRAMP_L_P_OUT
52 7 IN SPKRAMP_L_N_OUT

LEFT PIEZO

C6703 100PF 5% 50V CERM 402
C6702 100PF 5% 50V CERM 402

CRITICAL
J6703
78171-0002
M-RT-SM

CRITICAL L6707 FERR-120-OHM-3A 0603
SPKRAMP_SUB_P_OUT_CONN

52 7 IN SPKRAMP_SUB_P_OUT
52 7 IN SPKRAMP_SUB_N_OUT

C6705 100PF 5% 50V CERM 402
C6704 100PF 5% 50V CERM 402

CRITICAL L6708 FERR-120-OHM-3A 0603
SPKRAMP_SUB_N_OUT_CONN

DYN. FULL RANGE

CRITICAL
J6704
78171-0003
M-RT-SM

CRITICAL L6709 FERR-120-OHM-3A 0603
SPKRAMP_R_P_OUT_CONN

52 7 IN SPKRAMP_R_P_OUT
52 7 IN SPKRAMP_R_N_OUT

C6707 100PF 5% 50V CERM 402
C6706 100PF 5% 50V CERM 402

CRITICAL L6710 FERR-120-OHM-3A 0603
SPKRAMP_R_N_OUT_CONN

RT. PIEZO

ANALOG AUDIO IO SWITCH

APN: 353S2536

51 49 8 =PP5V_S3_AUDIO
R6724 0 5% 1/16W MF-LF 402
PP_MAX14504_VCC
C6710 1UF 10% 10V X5R 402

51 OUT AUD_LO_AMP_OUTL → R6716 0 → AUD_LO_AMP_OUTL_SWITCH
51 OUT AUD_LO_AMP_OUTR → R6717 0 → AUD_LO_AMP_OUTR_SWITCH
50 IN AUD_LI_L → R6718 0 → AUD_LI_L_SWITCH
50 IN AUD_LI_R → R6719 0 → AUD_LI_R_SWITCH
49 IN AUD_GPIO_0 → R6720 0 → AUD_SWITCH_CTRL

U6700
MAX14504
WLP
CRITICAL

VCC
NC1
NC2
NO1
NO2
CB
NEG
COM1
COM2
EN*
GND
SWITCH_CP

C6711 0.0033UF 10% 50V CERM 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_CONN_L
R6712 24K 5% 1/16W MF-LF 402
AUD_CONN_L BI 53

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_CONN_R
R6713 24K 5% 1/16W MF-LF 402
AUD_CONN_R BI 53

R6721 100K 5% 1/16W MF-LF 402

53 AUD_CONN_GND → R6715 0 → AUD_SWITCH_GND

GND STUFFING OPTIONS FOR CMOS SWITCH

54 50 49 GND_AUDIO_CODEC → R6714 0

NOSTUFF
R6727 0

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

SYNC_MASTER=AUDIO
SYNC_DATE=06/09/2009

PAGE TITLE
AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

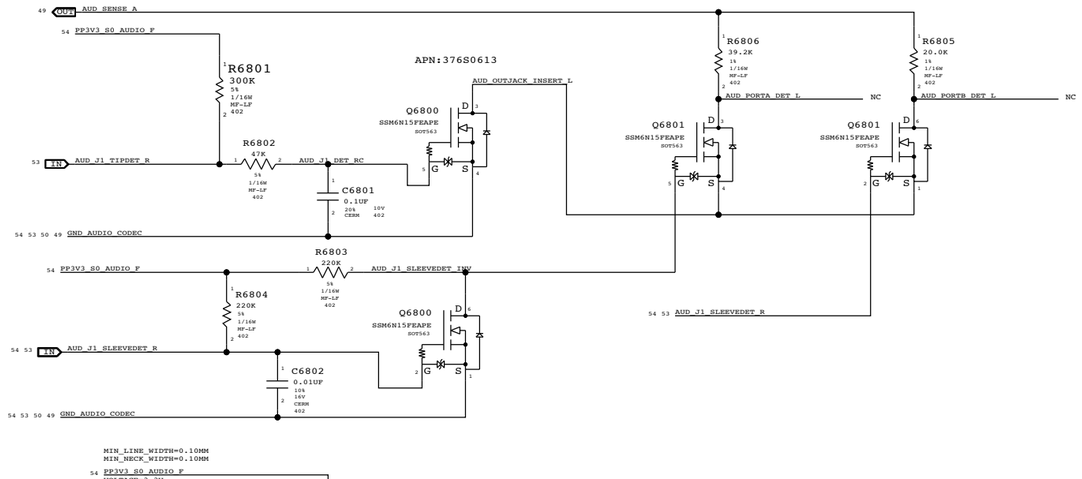
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

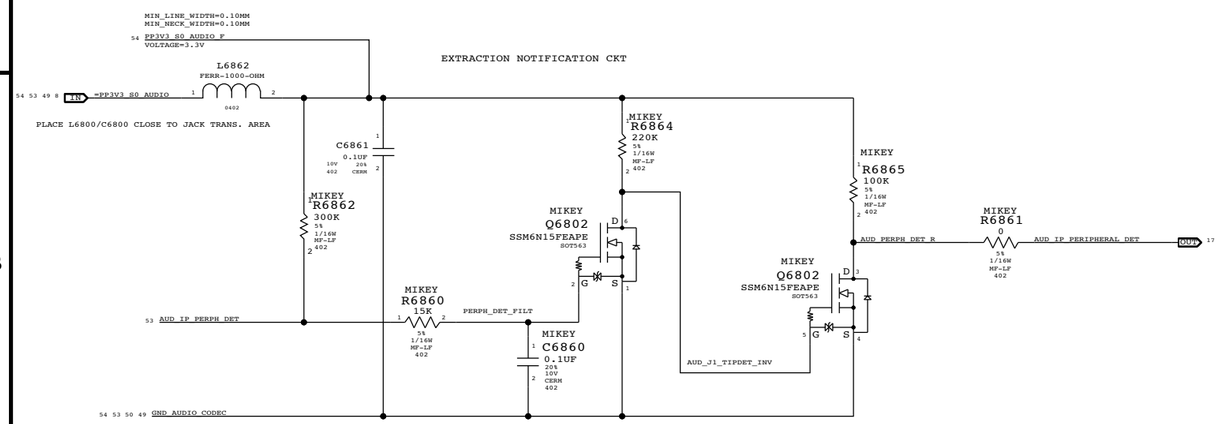
FUNCTION	CONVERTER	PIN COMPLEX	VREF/ENABLE	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MCP79 GPIO_38	MCP79 GPIO_17 (PERIPH DETECT) MCP79 GPIO_4 (LOAD DETECT)

PORT A DETECT (HEADPHONES)

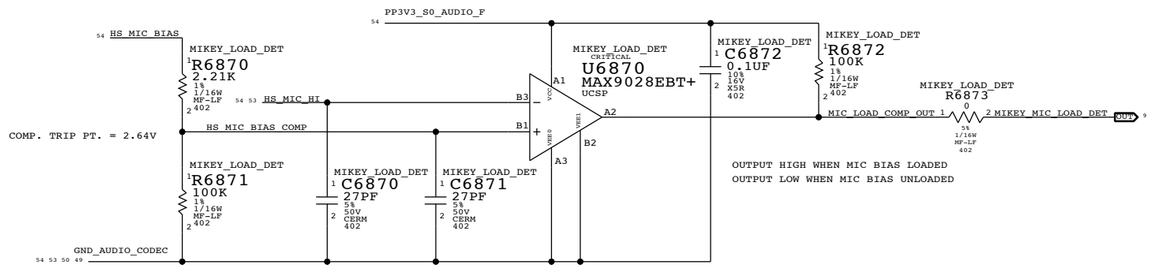
PORT B DETECT(SPDIF DELEGATE)



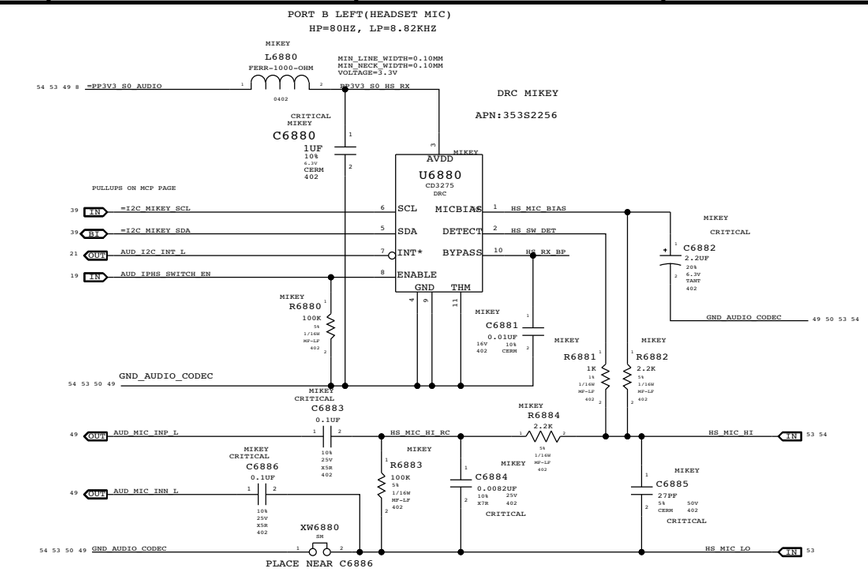
EXTRACTION NOTIFICATION CKT



MIKEY MIC LOAD DET CKT



PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)

SYNC MASTER=AUDIO	SYNC DATE=06/09/2009
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Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
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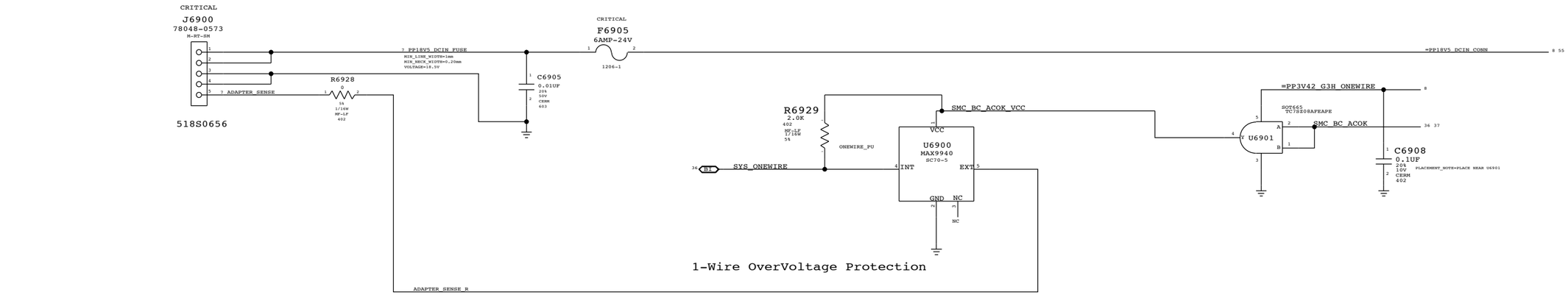
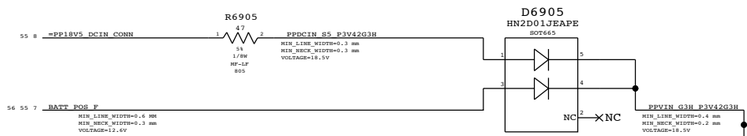
MagSafe DC Power Jack

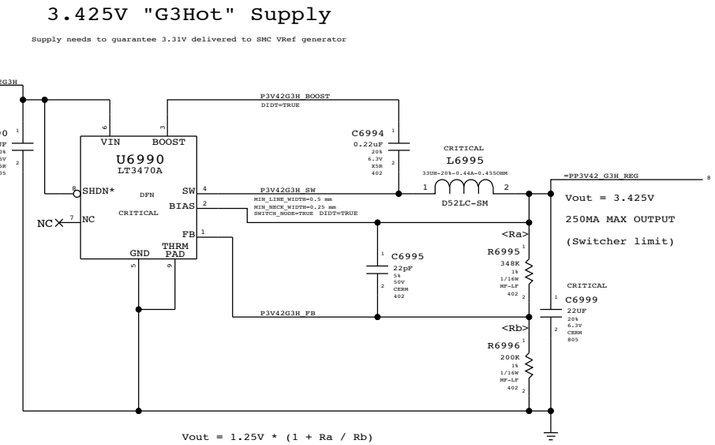


1-Wire OverVoltage Protection



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

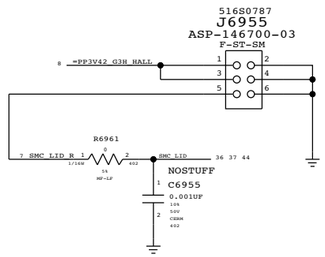


Vout = 1.25V * (1 + Ra / Rb)

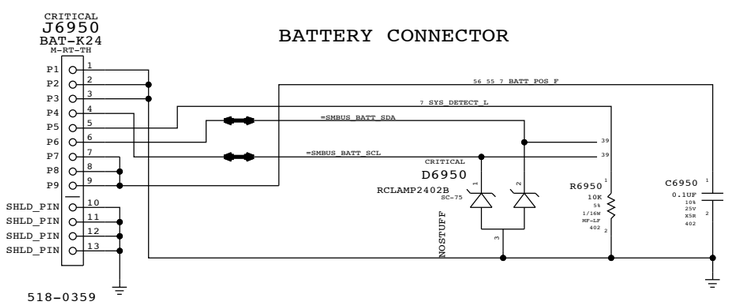
Vout = 3.425V

250MA MAX OUTPUT

(Switcher limit)



HALL EFFECT CONNECTOR



BATTERY CONNECTOR

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

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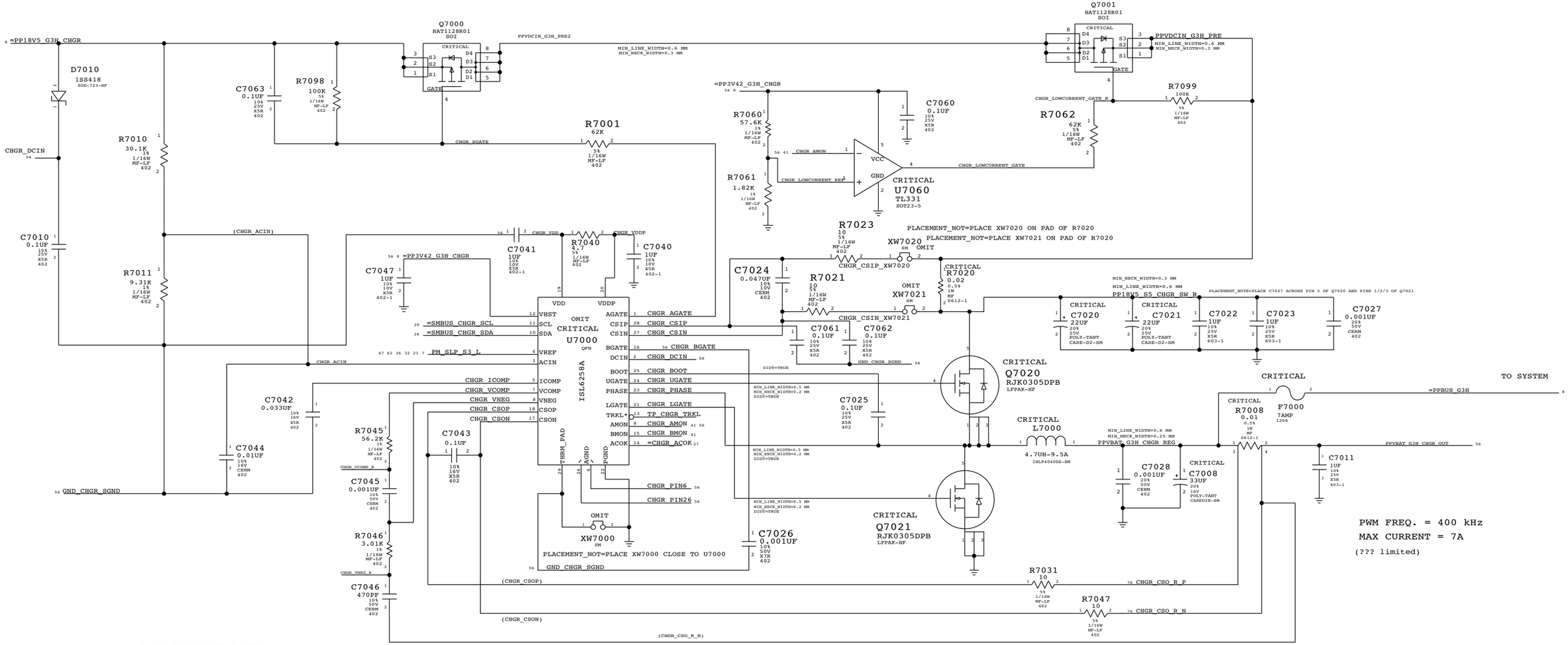
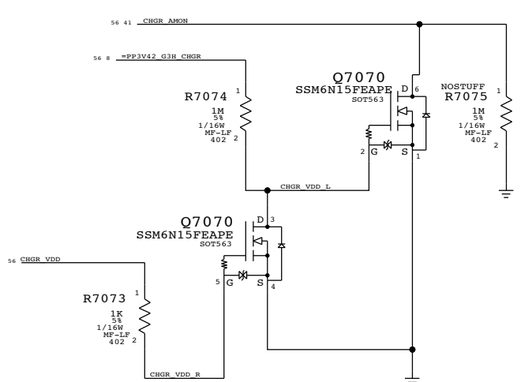
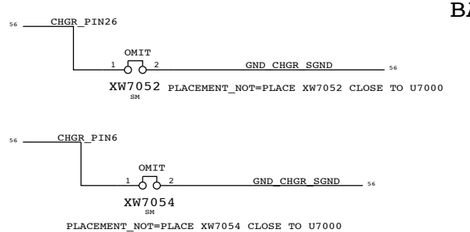
PBUS SUPPLY / BATTERY CHARGER

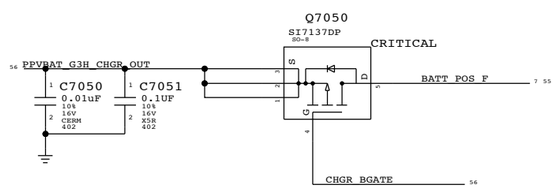


AMON PULLDOWN LOGIC





BATTERY CHARGE LIMITING FETS



SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

PAGE TITLE
PBUS Supply/Battery Charger

Apple Inc.

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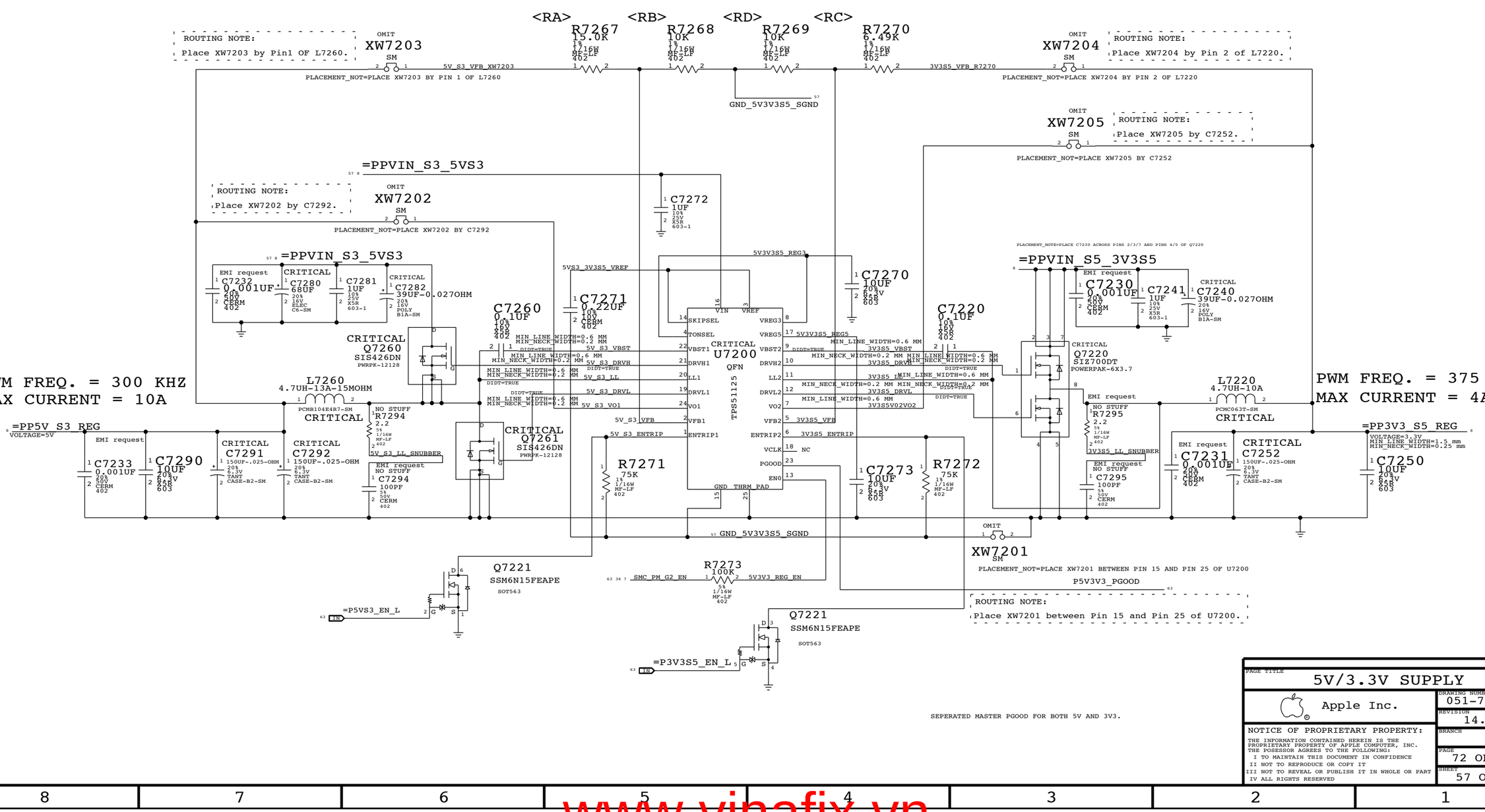
- COPY THIS PAGE FROM K36 CSA.76

5V S3/3.3V S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



PAGE TITLE	5V/3.3V SUPPLY
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1.5V/0.75V(DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

<RB> R7322 20K 0.1% 1/16W MF 402

<RA> R7321 20.0K 1% 1/16W MF-LF 402

NO STUFF C7303 100PF 5% 50V CERM 402

=PPVTT_S3_DDR_BUF

C7340 0.033UF 10% 16V X5R 402

C7301 10UF 20% 6.3V X5R 603

PLACEMENT_NOTE=PLACE XW7304 BY C7300

XW7304 OMIT SM

1V5S3_V5FILT_XW

C7300 1UF 10% 10V X5R 402-1

1V5S3_V5FILT

R7307 4.7 5% 1/16W MF-LF 402

=PP5V_S3_1V5S30V75S0

C7302 10UF 20% 6.3V X5R 603

=PP0V75_S0_REG

1V5S3_VTTSNS

1V5S3_VBST DIDT=TRUE

R7300 0 5% 1/16W MF-LF 402

C7309 0.1UF 16V 10% X5R 402

1V5S3_VBST_DC

PLACEMENT_NOTE=PLACE XW7301 BY L7320

XW7301 OMIT SM

ROUTING NOTE: Place XW7301 by L7320.

1V5S3_VDDQSNS

=PPVIN_S5_1V5S30V75S0

CRITICAL C7331 39UF-0.027OHM 20% 16V POLY B1A-SM

C7332 1UF 10% 6.3V X5R 603-1 CRITICAL

CRITICAL C7345 39UF-0.027OHM 20% 16V POLY B1A-SM

C7333 0.001UF 20% 50V CERM 402

PLACEMENT_NOTE=PLACE C7333 ACROSS Q7320 PWR AND Q7321 GND

ISNS_1V5_S3_P

ISNS_1V5_S3_N

R7310 10.7K 1% 1/16W MF-LF 402

=DDRVTT_EN

=DDRREG_EN

PLACEMENT_NOT=PLACE XW7303 BY C7308

XW7303 OMIT SM

1V5S3_CS

ROUTING NOTE: Place XW7303 by C7308.

VDDQSET VTTREF VLDOIN VTT V5FILT VBST V5IN VDDQSNS VTTSNS

PGOOD 13

DRVH 21 1V5S3_DRVH

LL 20 1V5S3_LL

DRVL 19 1V5S3_DRVL

MODE 4

NC0 7 NC

NC1 12 NC

COMP 6

CS 16

CRITICAL U7300 SYM (1 OF 2) TPS51116 QFN

ROUTING NOTE: CONNECT CS_GND TO Q7321 PIN1,2,3 USING KELVIN CONNECTION.

THRM_PAD CS_GND GND PGND VTTGND

25 17 3 18 1

MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm DIDT=TRUE

CRITICAL Q7320 CSD58858Q3 3.3X3.3-QFN

CRITICAL L7320 1.0UH-13A-5.6M-OHM SM-IHLP-1

CRITICAL Q7321 CSD58858Q3 3.3X3.3-QFN

NO STUFF R7390 2.2 EMI request 5% 1/16W MF-LF 402 1V5S3_LL_SNUBBER

NO STUFF C7390 100PF 5% 50V CERM 402 EMI request

PP1V5_S3_REG_R

R7350 0.001 1% 1W MF-1 0612

PLACE NEXT TO L7320

VOLTAGE=1.5V

=PP1V5_S3_REG

MIN_LINE_WIDTH=1.5 mm MIN_NECK_WIDTH=0.25 mm

CRITICAL C7343 330UF 20% 2.5V TANT CASE-B2-SM

C7344 0.001UF 20% 50V CERM 402

C7342 330UF 20% 2.5V TANT CASE-B2-SM CRITICAL

C7341 10UF 20% 6.3V X5R 603

PLACE CLOSE TO L7320

MAX CURRENT = 13A
PWM FREQ. = 400 KHZ

C7307 22UF 20% 6.3V X5R-CERM-1 603

C7308 22UF 20% 6.3V X5R-CERM-1 603

GND_1V5S3_SGND

GND_1V5S3_CSGND

XW7300 OMIT SM

ROUTING NOTE: Place XW7300 between Pin 3 and Pin 25 of U7300.

XW7302 OMIT SM

ROUTING NOTE: Place XW7302 by Q7321.

ROUTING NOTE: PUT 6 VIAS UNDER THE THERMAL PAD

PLACEMENT_NOT=PLACE XW7300 BETWEEN PIN 3 AND PIN 25 OF U7300

PLACEMENT_NOT=PLACE XW7302 BY Q7321

DDRREG_PGOOD

R7399 100K 5% 1/16W MF-LF 402

=PP3V3_S3_PDCISENS

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: 14.5.0

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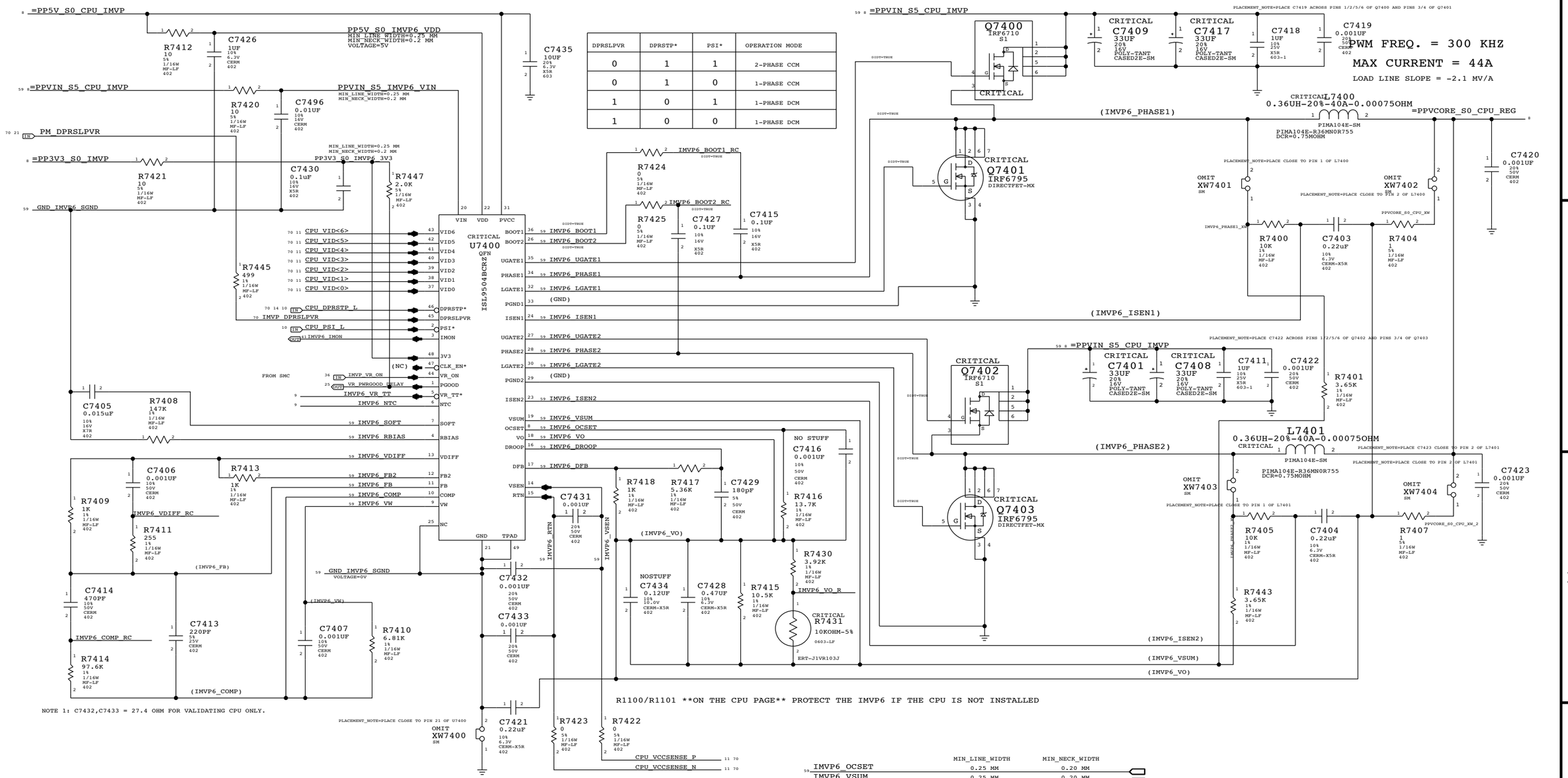

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC_MASTER=K24_MLB SYNC_DATE=03/03/2009

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

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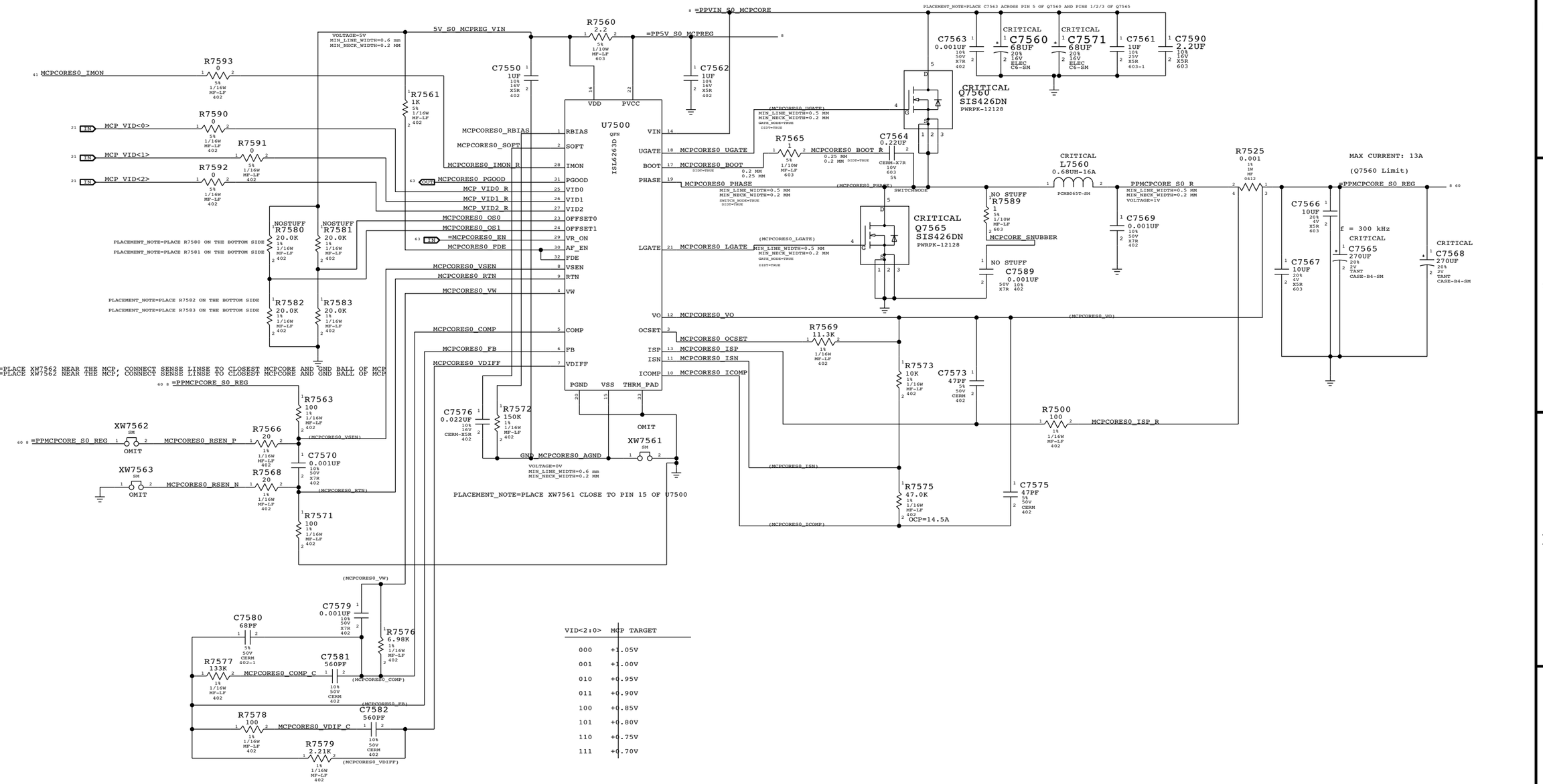

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE: MCP CORE REGULATOR

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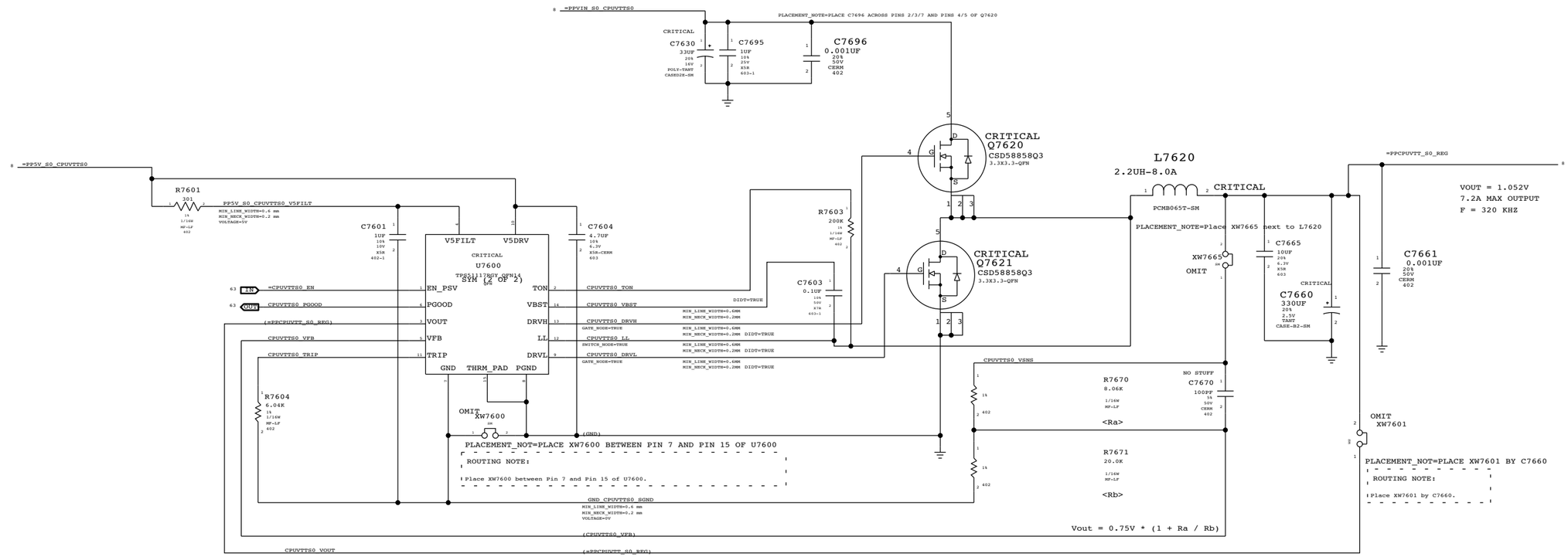
CPUVTT POWER SUPPLY



SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

PAGE TITLE

CPU VTT(1.05V) SUPPLY

Apple Inc.

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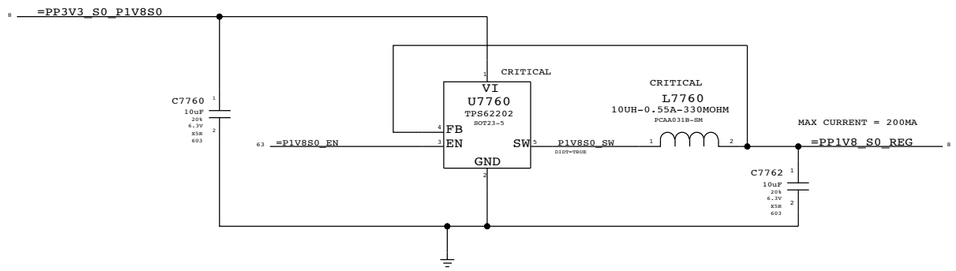
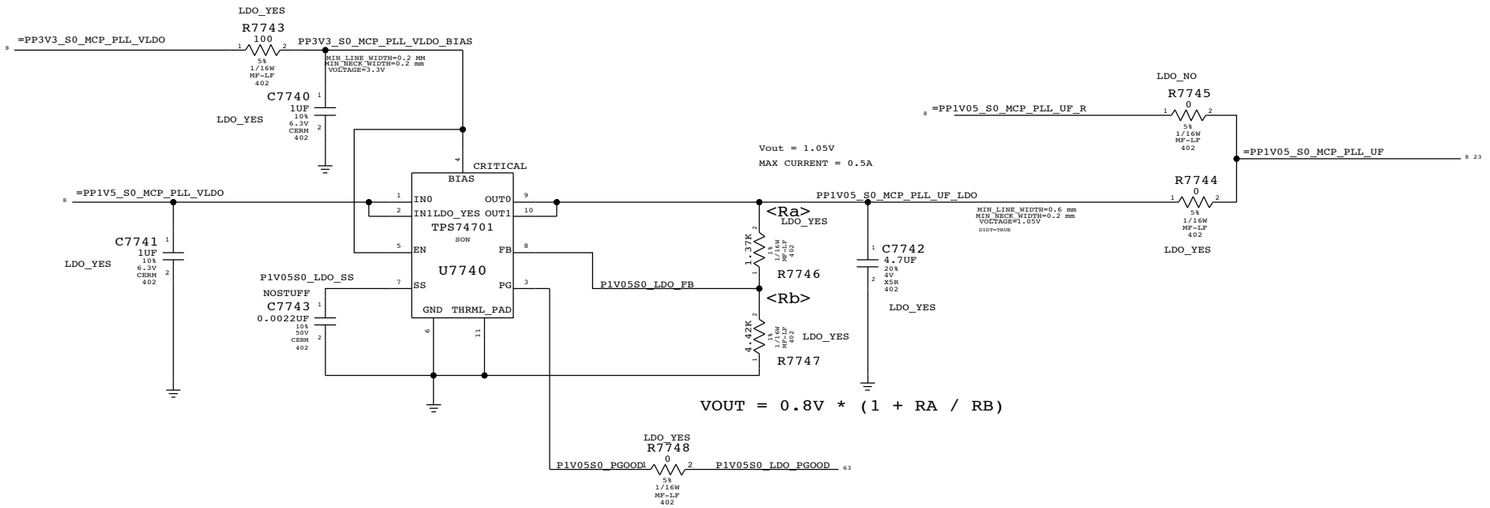
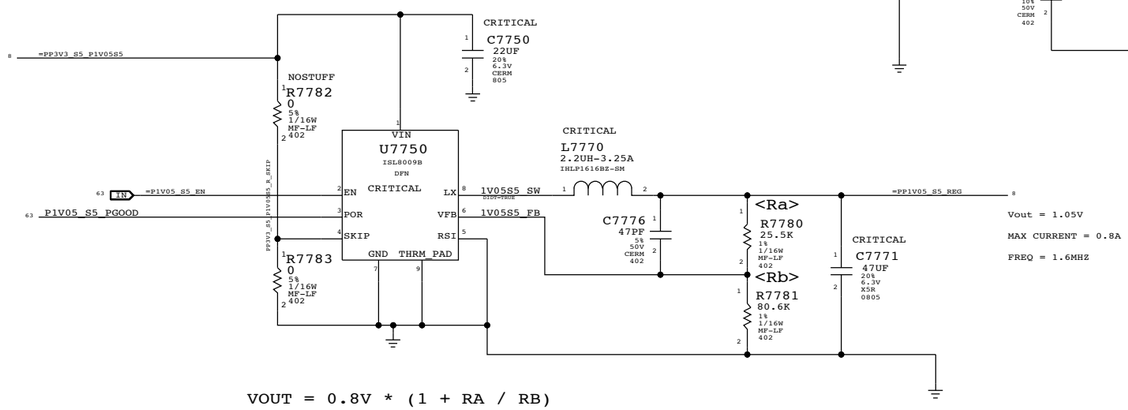
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



SYNC_MASTER=K24_MLB SYNC_DATE=03/24/2009

PAGE TITLE

MISC POWER SUPPLIES

Apple Inc.

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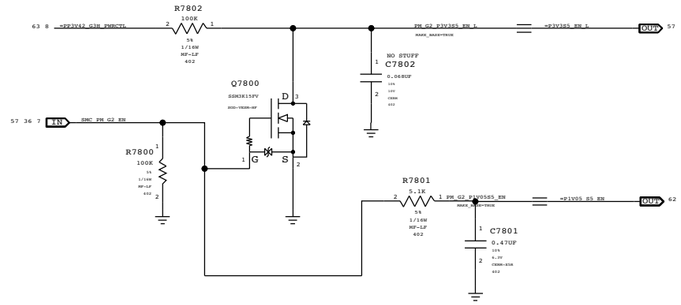
3.3V 1.05V S5 ENABLE



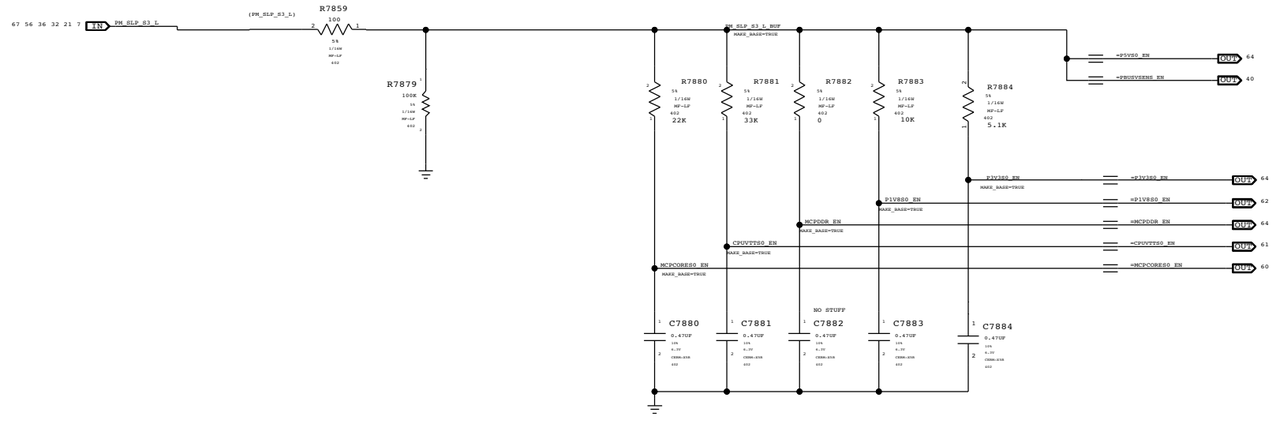
Power Control Signals

State	SNC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

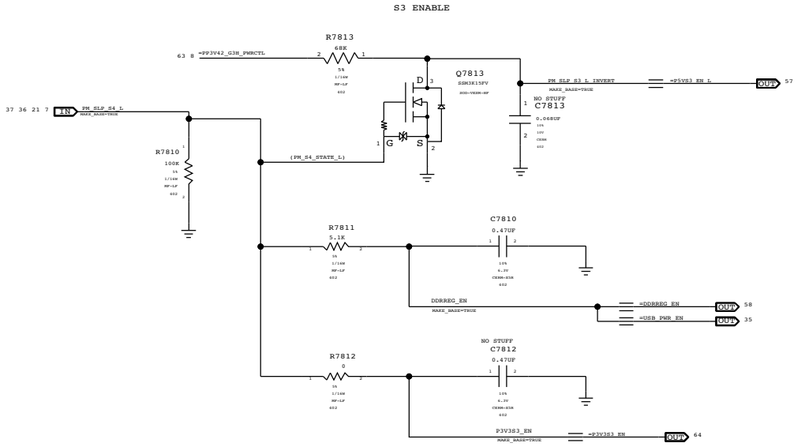
3.3V_S0, 1.8V_S0 ENABLE

MCPDDR, CPUVTT,MCPCORES0 ENABLE

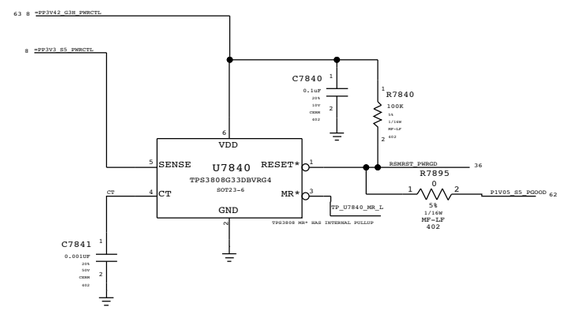
1.5V S0 AND 1.05V S0 ENABLE



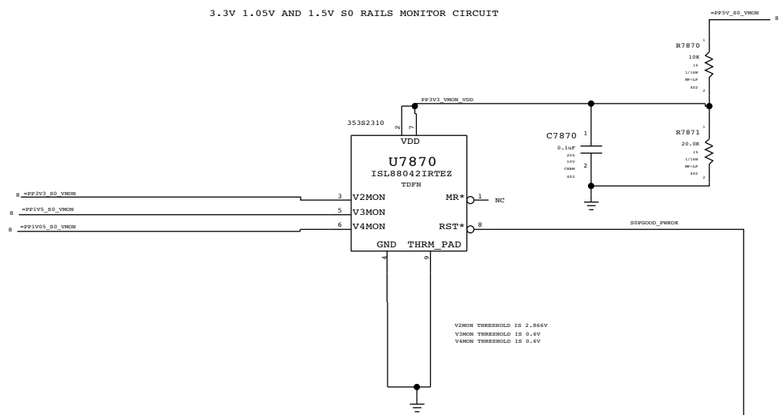
S3 ENABLE



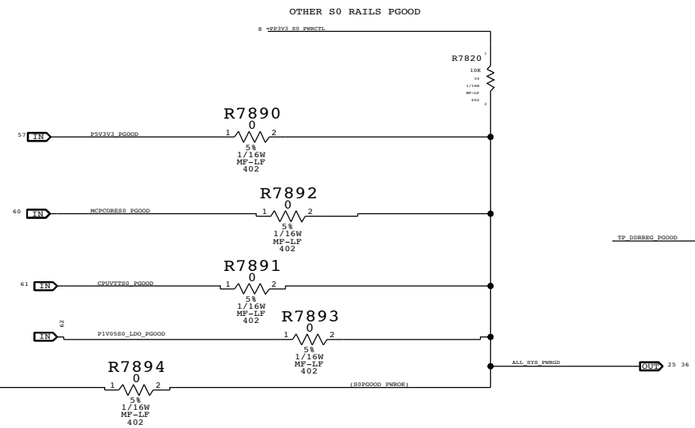
VOLTAGE MONITOR



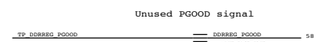
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal



PAGE TITLE	POWER SEQUENCING
	Apple Inc.
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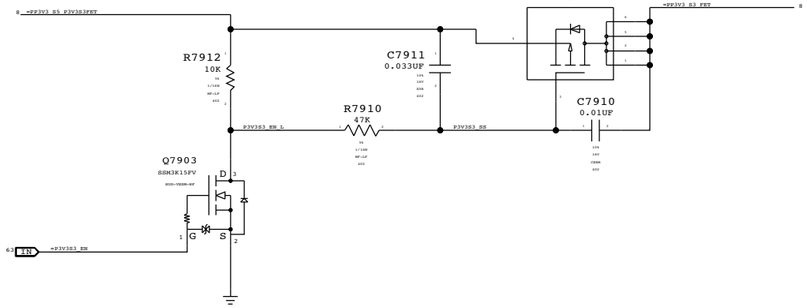
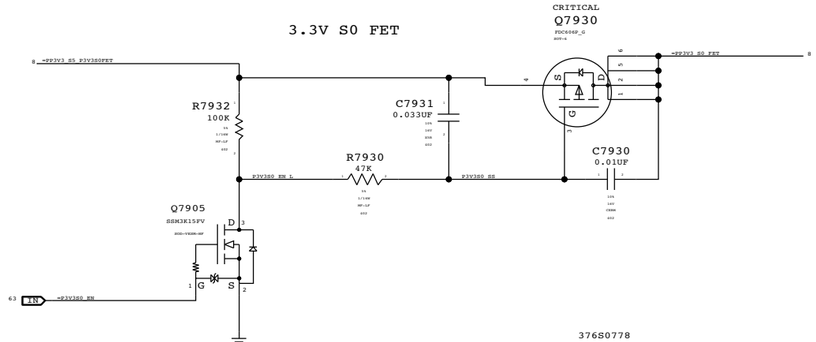
3.3V S3 FET



3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

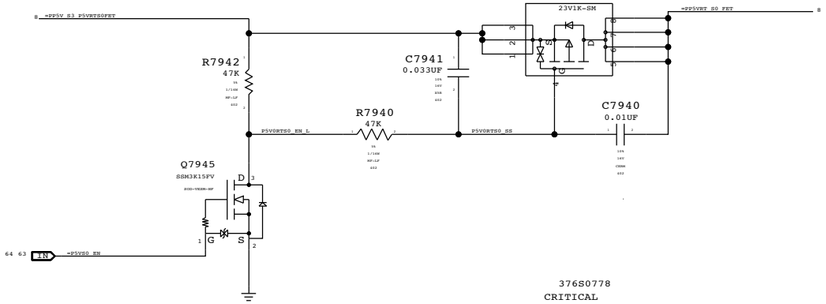
3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

376S0778

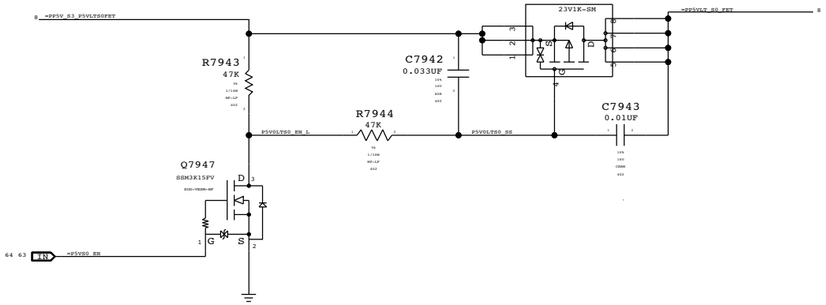
5.0V RT S0 FET



5.0V RT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	0.48 A (EDP)

376S0778

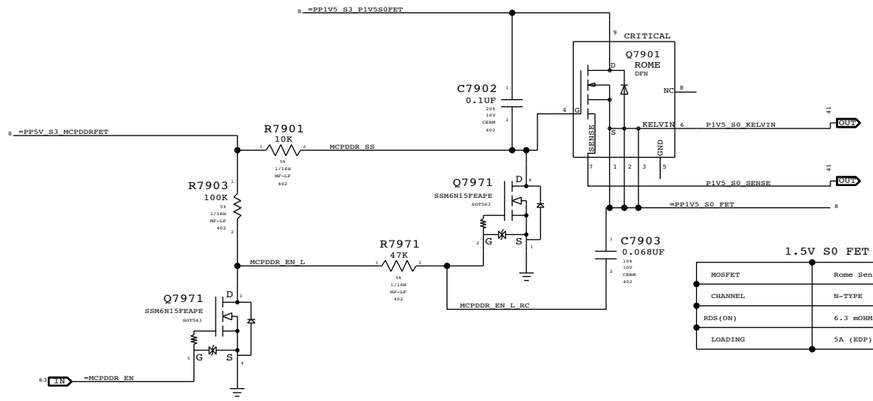
5.0V LT S0 FET



5.0V LT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.302 A (EDP)

1.5V S0 FET

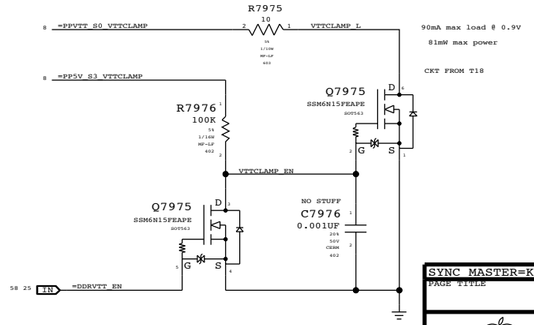
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC_MASTER=K24_MLB SYNC_DATE=02/15/2009

PAGE TITLE

POWER FETS

Apple Inc.

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CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

18 LVDS_IG_PANEL_PWR

R9014 1K 5% 1/16W MF-LF 402

8 =PP3V3_S5_LCD

CRITICAL
U9000
FPF1009
MFET-2X2

1 ON
2 VIN_1
3 VIN_2
VOUT_1 4
VOUT_2 5
GND 6
THRM PAD 7

C9009 0.1UF 10% 16V X5R 402

C9011 0.1UF 10% 16V X5R 402

C9012 10UF 20% 6.3V X5R 603

PP3V3_LCDVDD_SW
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

L9004
FERR-120-OHM-1.5A
0402-LF

L9008
120-OHM-0.3A-EMI
CRITICAL
0402-LF

C9015 0.001UF 10% 50V X7R 402

C9010 0.001UF 10% 50V X7R 402

MIN_NECK_WIDTH=0.20 MM

7 PP3V3_LCDVDD_SW_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM

7 PP3V3_S0_LCD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM

8 =PP3V3_S0_LCD

(LVDS DDC POWER)

R9008 100K 5% 1/16W MF-LF 402

R9009 100K 5% 1/16W MF-LF 402

18 7 LVDS_IG_DDC_CLK
18 7 LVDS_IG_DDC_DATA

LCD CONNECTOR
LVDS CONNECTOR:518S0650

CRITICAL
J9000
20474-030E-11
F-RT-SM

72 18 7 LVDS_IG_A_DATA_N<0>
72 18 7 LVDS_IG_A_DATA_P<0>
72 18 7 LVDS_IG_A_DATA_N<1>
72 18 7 LVDS_IG_A_DATA_P<1>
72 18 7 LVDS_IG_A_DATA_N<2>
72 18 7 LVDS_IG_A_DATA_P<2>
72 7 LVDS_IG_A_CLK_F_N
72 7 LVDS_IG_A_CLK_F_P

LVDS I/F

CRITICAL
L9080
90-OHM-200MA
AMC2012-SM
EMC_VSS-1

72 18 LVDS_IG_A_CLK_N
72 18 LVDS_IG_A_CLK_P

C9017 1000PF 5% 50V C0G-CERM 603

PLACEMENT_NOTE=PLACE CLOSE TO J9000

68 47 7 PPVOUT_S0_LCDBKLT

NCX
NCX

68 7 LED_RETURN_6
68 7 LED_RETURN_5
68 7 LED_RETURN_4
68 7 LED_RETURN_3
68 7 LED_RETURN_2
68 7 LED_RETURN_1

LED BKLT I/F

L9050
FERR-120-OHM-1.5A
0402-LF

8 =PP5V_S3_CAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

7 PP5V_S3_CAMERA_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9016 0.1uF 20% 10V CERM 402

CAMERA I/F

CAMERA

CRITICAL
L9060
90-OHM
DLP0NS
SYM_VER-1

73 20 OUT USB_CAMERA_P
73 20 OUT USB_CAMERA_N

73 7 USB_CAMERA_CONN_P
73 7 USB_CAMERA_CONN_N

PLACEMENT_NOTE=PLACE CLOSE TO J9000.

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

PAGE TITLE
LVDS CONNECTOR

Apple Inc.

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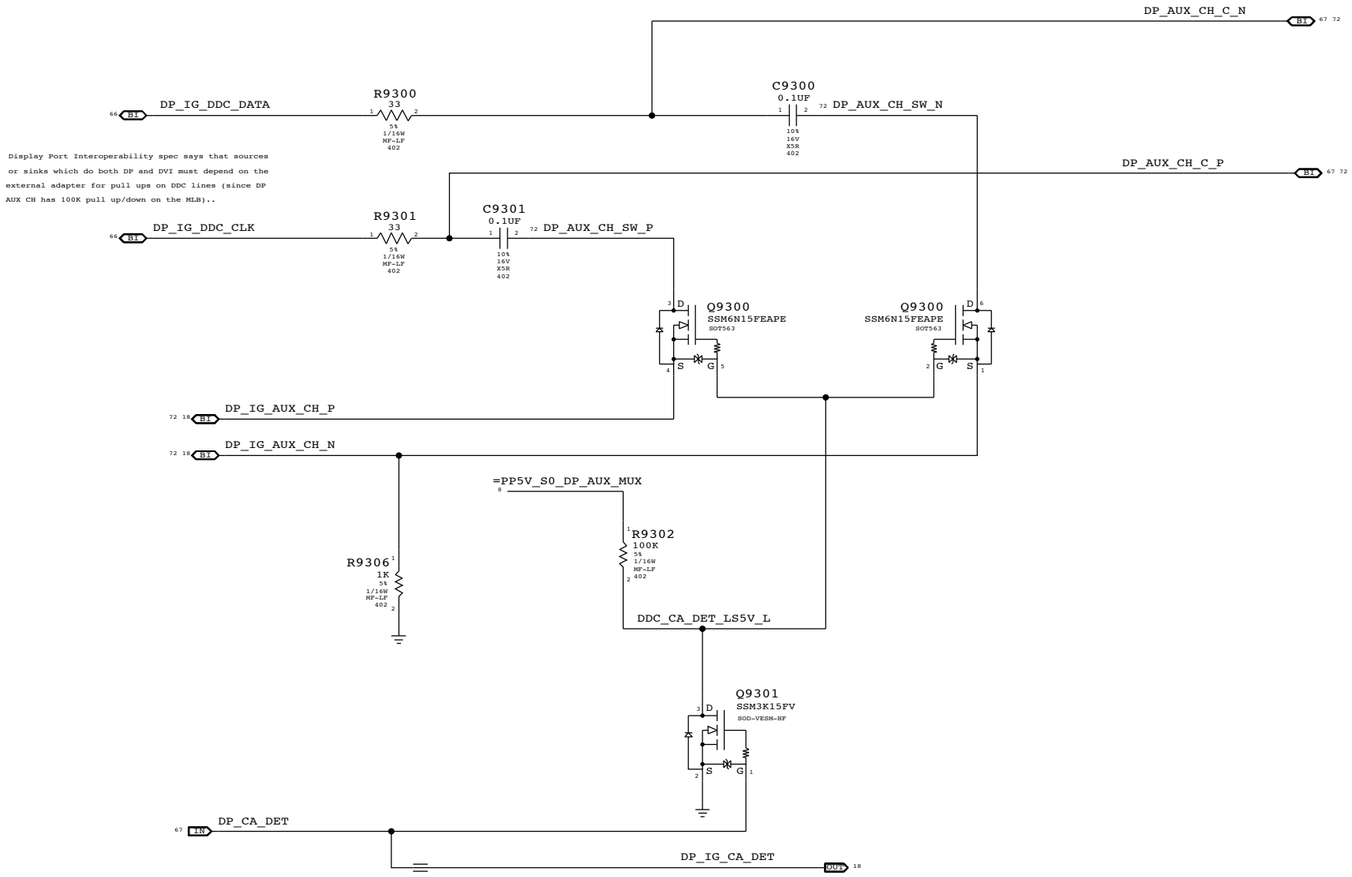
18 =MCP_HDMI_TXC_P — DP_ML_P<3> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXC_N — DP_ML_N<3> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_P<0> — DP_ML_P<2> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_N<0> — DP_ML_N<2> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_P<1> — DP_ML_P<1> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_N<1> — DP_ML_N<1> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_P<2> — DP_ML_P<0> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_N<2> — DP_ML_N<0> — 67 72 — MAKE_BASE=TRUE
18 =MCP_HDMI_HPD — DP_HPD — 67 — MAKE_BASE=TRUE
18 =MCP_HDMI_DDC_CLK — DP_IG_DDC_CLK — 66 — MAKE_BASE=TRUE
18 =MCP_HDMI_DDC_DATA — DP_IG_DDC_DATA — 66 — MAKE_BASE=TRUE



SYNC_MASTER=K24_MLB — SYNC_DATE=04/06/2009

PAGE TITLE: DISPLAYPORT SUPPORT

Apple Inc.

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POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SUMBOLS
HAVE BEEN USED BEACUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch

U9480 TPS2051B SOT23
L9400 FERR-120-OHM-3A
C9400 4.7UF
C9480 22UF
C9481 4.7UF
C9485 22UF
C9486 22UF
R9420 100K
R9421 100K
R9422 1M
R9423 100K
R9425 1M
R9443 100K
R9442 100K
R9445 10K
R9444 10K
R9446 100K
Q9440 2N7002DW-X-G
Q9441 2N7002DW-X-G
D9400 RCLAMP0504F
D9410 RCLAMP0524P
D9411 RCLAMP0524P
J9400 MINIDSPLYPRT-K83
FL9400 12-OHM-100MA TCM1210-48M
FL9401 12-OHM-100MA TCM1210-48M
FL9402 12-OHM-100MA TCM1210-48M
FL9403 12-OHM-100MA TCM1210-48M
C9410 0.1uF
C9411 0.1uF
C9412 0.1uF
C9413 0.1uF
C9414 0.1uF
C9415 0.1uF
C9416 0.1uF
C9417 0.1uF

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

MCP79 requires pull down HPD input with 100K if DP_HPD is used.

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

514-0691

SYNC MASTER=K24 MLB	SYNC DATE=04/06/2009
PAGE TITLE: DisplayPort Connector	
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
	REVISION 14.5.0
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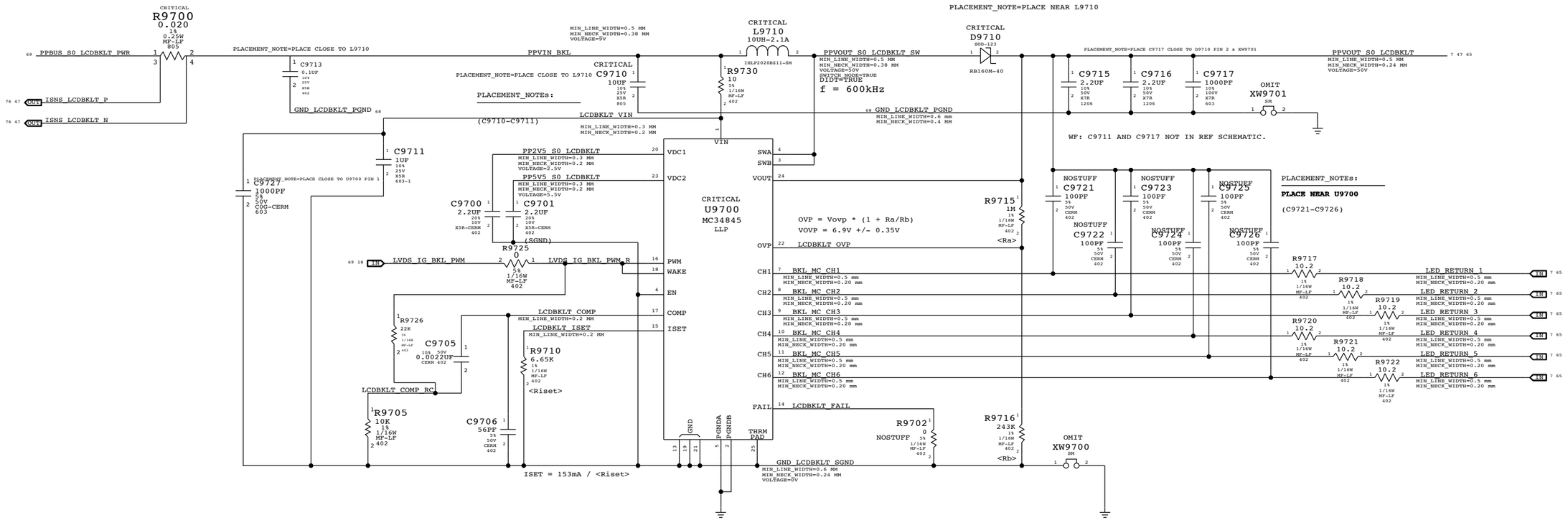

13.3 Inch Panel (9 LEDs per string)

Target: ISET = 23mA, OVP = 35V

ACTUAL: ISET = 23MA, OVP = 35.2V

SYNC_MASTER=VEMURI K19I SYNC_DATE=02/09/2009

PAGE TITLE

LCD Backlight Driver (MC34845)

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION 14.5.0

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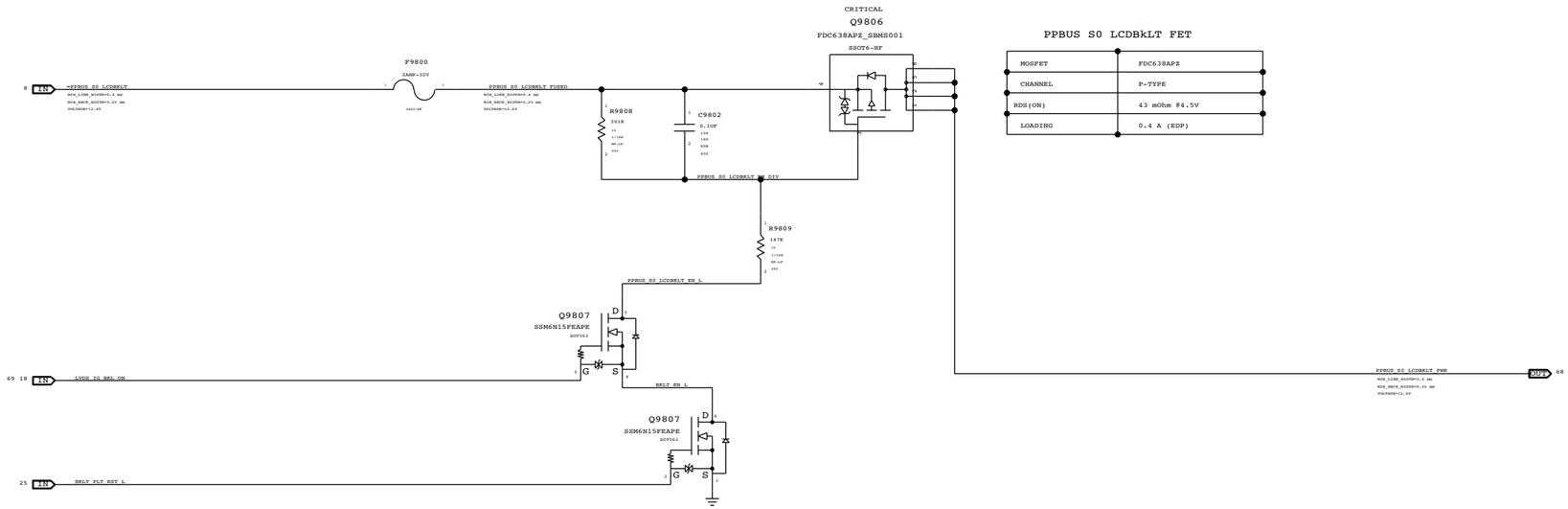

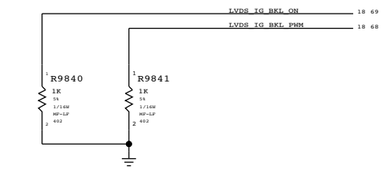

MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION 14.5.0

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_SMIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<15..0>	10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_SMIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_H	CPU_50S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_H	CPU_50S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 37
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_SMIL	PM_THRMTRIP_L	10 14 37
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_PROC_SEL	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	10 14 59
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 59
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	59
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_SMIL	CPU_VID<6..0>	11 59
		CPU_50S	CPU_SMIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 59
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 59
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE: CPU/FSB Constraints

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DRAWING NUMBER: 051-7982 SIZE: D
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PCIE_MINI_R2D_P 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P 17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N 17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P
	PCIE_90D	PCIE	PCIE_FW_R2D_N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P 9 17
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N 9 17
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P 9 17
	PCIE_90D	PCIE	PCIE_FW_D2R_N 9 17
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P 17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N 17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P 7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N 7 30
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_P 7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_N 7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_P 7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_N 7 30
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP 17
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0> 66 67
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0> 67
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0> 66 67
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0> 67
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P 18 66
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N 18 66
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P 66
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N 66
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P 66 67
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N 66 67
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET 18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE 18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P 18 65
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P 7 65
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N 18 65
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N 7 65
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0> 7 18 65
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0> 7 18 65
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0> 67
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0> 67
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET 18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE 18 24
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P 20 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N 20 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P 7 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N 7 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N 34
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P 20 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N 20 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P 7 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N 7 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N 34
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P 20 34
	SATA_100D	SATA	SATA_ODD_R2D_C_N 20 34
	SATA_100D	SATA	SATA_ODD_R2D_P 7 34
	SATA_100D	SATA	SATA_ODD_R2D_N 7 34
	SATA_100D	SATA	SATA_ODD_R2D_UF_P 34
	SATA_100D	SATA	SATA_ODD_R2D_UF_N 34
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P 20 34
	SATA_100D	SATA	SATA_ODD_D2R_N 20 34
	SATA_100D	SATA	SATA_ODD_D2R_C_P 7 34
	SATA_100D	SATA	SATA_ODD_D2R_C_N 7 34
	SATA_100D	SATA	SATA_ODD_D2R_UF_P 34
	SATA_100D	SATA	SATA_ODD_D2R_UF_N 34
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP 20

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTM_L	PCI_55S	PCI	PCI_INTM_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 36 38
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 36 38
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 36
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	25 38
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 35
	USB_90D	USB	USB_EXTA_N	20 35
	USB_90D	USB	USB_EXTA_MUXED_P	35
	USB_90D	USB	USB_EXTA_MUXED_N	35
	USB_90D	USB	CONN_USB_EXTA_P	35
	USB_90D	USB	CONN_USB_EXTA_N	35
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 65
	USB_90D	USB	USB_CAMERA_N	20 65
	USB_90D	USB	USB_CAMERA_CONN_P	7 65
	USB_90D	USB	USB_CAMERA_CONN_N	7 65
USB_BT	USB_90D	USB	USB_BT_P	20 30
	USB_90D	USB	USB_BT_N	20 30
	USB_90D	USB	CONN_USB2_BT_P	7 30
	USB_90D	USB	CONN_USB2_BT_N	7 30
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 44
	USB_90D	USB	USB_TPAD_N	20 44
	USB_90D	USB	USB_TPAD_R_P	44
	USB_90D	USB	USB_TPAD_R_N	44
USB_IR	USB_90D	USB	USB_IR_P	9 20
	USB_90D	USB	USB_IR_N	9 20
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 35
	USB_90D	USB	USB_EXTB_N	20 35
	USB_90D	USB	CONN_USB_EXTB_P	35
	USB_90D	USB	CONN_USB_EXTB_N	35
USB_SD	USB_90D	USB	USB_CARDREADER_P	9 20
	USB_90D	USB	USB_CARDREADER_N	9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	13 21 39
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	13 21 39
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 39
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 39
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21 49
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 49
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 49
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 49
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 49
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 36
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 38 48
	SPI_55S	SPI	SPI_CLK	48
	SPI_55S	SPI	SPI_ALT_CLK	38
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 38 48
	SPI_55S	SPI	SPI_MOSI	48
	SPI_55S	SPI	SPI_ALT_MOSI	38
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 38 48
	SPI_55S	SPI	SPI_MISO_R	48
	SPI_55S	SPI	SPI_ALT_MISO	38
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 38
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 32
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31 32
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 31
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TGI_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5V5	SMB	SMBUS_SMC_A_S3_SCL	7 39
SMBUS_SMC_A_S3_SDA	SMB_5V5	SMB	SMBUS_SMC_A_S3_SDA	7 39
SMBUS_SMC_B_S0_SCL	SMB_5V5	SMB	SMBUS_SMC_B_S0_SCL	39
SMBUS_SMC_B_S0_SDA	SMB_5V5	SMB	SMBUS_SMC_B_S0_SDA	39
SMBUS_SMC_0_S0_SCL	SMB_5V5	SMB	SMBUS_SMC_0_S0_SCL	39
SMBUS_SMC_0_S0_SDA	SMB_5V5	SMB	SMBUS_SMC_0_S0_SDA	39
SMBUS_SMC_BSA_SCL	SMB_5V5	SMB	SMBUS_SMC_BSA_SCL	7 39
SMBUS_SMC_BSA_SDA	SMB_5V5	SMB	SMBUS_SMC_BSA_SDA	7 39
SMBUS_SMC_MGMT_SCL	SMB_5V5	SMB	SMBUS_SMC_MGMT_SCL	39
SMBUS_SMC_MGMT_SDA	SMB_5V5	SMB	SMBUS_SMC_MGMT_SDA	39

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TGI_DIFFPAIR		CHGR_CSI_P
	1TGI_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TGI_DIFFPAIR		CHGR_CSO_P
	1TGI_DIFFPAIR		CHGR_CSO_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K84 SENSOR NET PROPERTIES

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	DIFFPAIR		CHGR_CSO_R_P	56
	DIFFPAIR		CHGR_CSO_R_N	56
	DIFFPAIR		CPUTHMSNS_D2_P	42
	DIFFPAIR		CPUTHMSNS_D2_N	42
	DIFFPAIR		CPU_THERMD_P	10 42
	DIFFPAIR		CPU_THERMD_N	10 42
	DIFFPAIR		ISNS_CPUVTT_P	41
	DIFFPAIR		ISNS_CPUVTT_N	41
	DIFFPAIR		ISNS_HDD_P	34 47
	DIFFPAIR		ISNS_HDD_N	34 47
	DIFFPAIR		ISNS_HDD_R_P	47
	DIFFPAIR		ISNS_HDD_R_N	47
	DIFFPAIR		MCPTHMSNS_D2_P	42
	DIFFPAIR		MCPTHMSNS_D2_N	42
	DIFFPAIR		MCP_THMDIODE_P	21 42
	DIFFPAIR		MCP_THMDIODE_N	21 42
	DIFFPAIR		ISNS_ODD_P	34 47
	DIFFPAIR		ISNS_ODD_N	34 47
	DIFFPAIR		ISNS_ODD_R_P	47
	DIFFPAIR		ISNS_ODD_R_N	47
	DIFFPAIR		ISNS_AIRPORT_P	30 47
	DIFFPAIR		ISNS_AIRPORT_N	30 47
	DIFFPAIR		ISNS_AIRPORT_R_P	47
	DIFFPAIR		ISNS_AIRPORT_R_N	47
	DIFFPAIR		ISNS_1V5_S3_P	47 58
	DIFFPAIR		ISNS_1V5_S3_N	47 58
	DIFFPAIR		ISNS_1V5_S3_R_P	47
	DIFFPAIR		ISNS_1V5_S3_R_N	47
	DIFFPAIR		ISNS_LCDBKLT_P	47 68
	DIFFPAIR		ISNS_LCDBKLT_N	47 68

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K84 SPECIAL CONSTRAINTS

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K84 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

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