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</table>

3. All crystals & oscillator values are in hertz.

1. All resistance values are in ohms, 0.1 watt +/- 5%.

Schematic / PCB #s

<table>
<thead>
<tr>
<th>PART</th>
<th>NUM</th>
<th>QUANTITY</th>
<th>DESCRIPTION</th>
<th>REFERENCE (LEG)</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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K84 MLB SCHEMATIC

PVT 06/12/2009
NOT UP TO DATE

System Block Diagram
Apple Inc.
051-7982 E
14.5.0

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Apple Inc.

www.sp860.com  QQ:453100829
### BOM Configuration

**Apple Inc.**

**K84 MLB DEVELOPMENT BOM**

**Part Numbers and Notes**

#### Development BOM

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
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#### Programmable Parts

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#### Alternate Parts

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<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
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### Bar Code Labels / KEI F's

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<th>REFERENCE DES</th>
<th>CRITICAL</th>
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### K84 BOARD STACK-UP

#### Top

- **SIGNAL**
- **GROUND**
- **SIGNAL(High Speed)**
- **SIGNAL(High Speed)**
- **POWER**
- **POWER**
- **GROUND**
- **SIGNAL(High Speed)**
- **SIGNAL(High Speed)**
- **GROUND**

#### Bottom

- **SIGNAL**

---

Apple Inc.

514-0690 is plastic version of 514-0691 metal part for mini DP connector.

514-0688 is plastic version of 514-0689 metal part for USB connectors.
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CPU VCore HF and Bulk Decoupling

Sync from T18

Remove no stuff caps C1220 to C1231

Remove C1244 & C1245

Change C1240-C1243 and C1260 from 128uf 22uf to 12uf 22uf (Milli-Ohm)

0.1uf CERM

0.1uf CERM

10V 20%

10V 20%

22uf 20%

22uf 20%

22uf 20%

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22uf 20%
MCP79-specific pinout

NOTE: This is not the standard XDP pinout.

The mini-XDP adapter may be repositioned, see comments...

Direction of XDP module

This is not the standard XDP pinout.

Mini-XDP Connector

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Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

REMOVED DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672

CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

SYNC FROM T18

REMOVE MCP 27MHz CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT

NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V MIN_LINE_WIDTH=0.4 MM

=PP1V05_S0_MCP_HDMI_VDD
=PP3V3_S0_MCP_HDMI_RSET
=PP3V3_S0_MCP_IFP_VDD
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_MCP_VPLL
=PP3V3R1V8_S0_MCP_IFP_VDD

MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

MIN_LINE_WIDTH=0.4 MM
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for results in earlier ROMSIP and MCP FSB I/O interface initialization.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which but results in MCP79 ROMSIP sequence happening after CPU powers up.

SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO +3DVTT_EN
CHANGE V3.3 VPP TO U2850 TO SMALLER PARTS

PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
MCP 25MHz Crystal

RTC Crystal

MCP_SEQ_SMC

MCP_SEQ_MIX

Reset Button

Platform Reset Connections

LPC reset (unbuffered);

PCIE reset (unbuffered);

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

RESET BUTTON TO RESET PADS

SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO +3DVTT_EN
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PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
MCP 25MHz Crystal

RTC Crystal

MCP_SEQ_SMC

MCP_SEQ_MIX

Reset Button

Platform Reset Connections

LPC reset (unbuffered);

PCIE reset (unbuffered);

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)
Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

3.3V S5 is used because MEM_RESET must be high before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

DDR3 RESET Support

MCP_MEM_RESET_L = PP1V5_S3_MEMRESET
MEM_RESET_RC_L = PP3V3_S5_MEMRESET

R3305
100K
402
MF-LF
5%

R3310
1K
402
MF-LF
5%

R3309
5%
402
CERM
20%
0.1UF
10V

R3300
10K
402
MF-LF

WLAN Enable Generation

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

3.3V ENET FET

1.05V ENET FET

RTL8211 25MHz Clock

SYNC_DATE=04/06/2009
SYNC_MASTER=K24_MLB

Ethernet & AirPort Support

Apple Inc.

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**ODD Power Control**

**NOTE**: All pins on 00 to 03 or 03 to 06 to ensure the drive is unpowered in S3/S5.

**SYS_LED_ANODE**

Indicates disc presence

**R4531**

4.7K 5% 1/16W

**C4531**

402 CERM 50V 10%

**R4590**

SYS_LED_ANODE_R MF-LF 1/16W 33K 5%

**21 C4501**

16V 0.01UF

**C4502**

100K MF-LF 1/16W 1206 1% 20 72

**J4500**

47 76 OUT

**J4501**

54 72 OUT

**J4502**

518 71-0002

**516S0616**

54722-0164

**CRITICAL**

VOLTAGE=5V MIN_NECK_WIDTH=0.4mm MIN_LINE_WIDTH=0.6mm

**PP5V_S0_HDD_FLT**

=PP5V_S3_ODD

**PP5V_SW_ODD**

OUT

**SYNC_MASTER=K24_MLB**

SYNC_DATE=01/19/2009

Apple Inc. 051-7982 D 14.5.0

NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

**PLACEMENT_NOTE=Place FL4501 close to J4501**

**PLACEMENT_NOTE=PLACE C4525 NEXT TO C4526**

**PLACEMENT_NOTE=PLACE C4526 CLOSE TO J4500**

**PLACEMENT_NOTE=PLACE FL4520 close to J4500**

**PLACEMENT_NOTE=PLACE L4500 CLOSE TO J4501**

**PLACEMENT_NOTE=Place C4515 next to C4516**

**PLACEMENT_NOTE=Place C4516 close to J4501**

**SYM_VER-1**

**DLP11S**

**CRITICAL**

**90-OHM-100MA**

**VOLTAGE=5V**

**MIN_NECK_WIDTH=0.4mm**

**PP5V_S0_HDD_FLT**

OUT

**PP5V_SW_ODD**

OUT

**SYNC_MASTER=K24_MLB**

SYNC_DATE=01/19/2009
Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

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USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

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USB PORT B (BACK PORT)

USB/SMC Debug Mux

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USB PORT B (BACK PORT)

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USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux

Port Power Switch

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

USB/SMC Debug Mux
pins designed as outputs can be left floating.

NOTE: Unused pins have "SMC_Pxx" names.

PLACEMENT_NOTE=PLACE C4950 CLOSE TO U4900 PIN M10
PLACEMENT_NOTE=PLACE C4951 CLOSE TO U4900 PIN N9

If SMS interrupt is not used, pull up to SMC rail.

NOTE: P94 and P95 are shorted, P95 could be spare.
Alternate SPI ROM Support
BOOSTER +18.5VDC FOR SENSORS

3V3 LDO FOR IPD

IPD FLEX CONNECTOR

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Sync Date: 02/25/2009
Sync Master: K24_MLB

Wellspring 2

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Analog SMS

R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC

C5922
16V
10%
X5R
402
0.1UF

C5923
16V
10%
X5R
402
0.033UF

C5924
0.033UF
X5R
402
10%

C5925
402
16V
0.033UF

C5926
16V
0.01UF

R5921
10K
402
1/16W
5%

R5922
10M
402
5%

Cap Values are chosen to get cutoff frequency of ~146Hz

SMS
SMS_ONOFF_L
SMS_X_AXIS
SMS_Y_AXIS
SMS_Z_AXIS

MAKE_BASE=TRUE
SMS_PWRDN=PP3V3_S3_SMS
PP3V3_S3_SMS_FILT=36.0

SMS

www.sp860.com  QQ:453100829
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
PEAK RIN = 15.16K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC HP = 3.6 HZ
FC LP = 43KHZ

V IN = 2VRMS, CODEC VIN = 1.14 VRMS

Audio: Line Input Filter

R6301
R6302
R6311
R6312
C6301
C6302
C6311
C6312

FBG AUDIO_CODEC
AUD_LI_P_L
AUD_LI_P_R
AUD_LI_R
AUD_LI_R_DIV
AUD_LI_L
AUD_LI_L_DIV
AUD_LI_GND

MIN_LINE_WIDTH=.1MM
MIN_NECK_WIDTH=.1MM

 Vin = 2VRMS, Codec VIN = 1.14 VRMS
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

---

MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ

---

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WWW.SP860.COM QQ:453100829
5V S3/3.3V S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

PWM FREQ. = 300 KHZ
MAX CURRENT = 10A
VOLTAGE = 5V

PLACE XW7203 by Pin 1 OF L7260.

ROUTING NOTE:
- CRITICAL
- EMI request
- MF-LF 1/16W

PLACE XW7201 BETWEEN PIN 15 AND PIN 25 OF U7200

PLACE XW7205 BETWEEN PIN 12 OF Q7220 AND PIN 15 OF L7220

PLACE XW7204 BY PIN 2 OF L7220

PLACE XW7202 BY C7292.
1.5V/0.75V(DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

VOLTAGE = 1.5V = PP1V5_S3_REG

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=1 mm

CRITICAL
Q7321
3.3X3.3-QFN

PWM FREQ. = 400 KHZ
MAX CURRENT = 13A

STATE | PM_SLP_S4_L | PM_SLP_S3_L | PP1V5_S3 | PP0V75_S0
S0 | HIGH | HIGH | 1.5V | 0.75V
S3 | HIGH | LOW | 1.5V | 0.0V
S5/G3HOT | LOW | LOW | 0.0V | 0.0V

Apple Inc. 051-7982 D 14.5.0
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www.sp860.com  QQ:453100829
IMVP6 CPU VCORE REGULATOR

NOTE 1: C7432, C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.
### Power Control Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery Off (G3Hot)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft-Off (S5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep (S3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Run (S0)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Power Sequencing**

- 3.3V 1.05V S5 ENABLE
- 1.5V S0 AND 1.05V S0 ENABLE
- 3.3V_S0, 1.8V_S0 ENABLE
- Battery Off (G3Hot)
- Soft-Off (S5)
- Sleep (S3)
- Run (S0)
or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP Display Port Interoperability spec says that sources AUX CH has 100K pull up/down on the MLB).
Port Power Switch

POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS HAVE BEEN USED BECAUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES.

DisplayPort Connector

Apple Inc.

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FSB Clock Constraints

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<tr>
<th>NET</th>
<th>TYPE</th>
<th>TOP (X)</th>
<th>TOP (Y)</th>
<th>BOTTOM (X)</th>
<th>BOTTOM (Y)</th>
<th>PADS</th>
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<td>CK</td>
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<td>0</td>
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<tr>
<td>CK</td>
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</table>

Most CPU signals with impedance requirements are 55-ohm single-ended.
### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Bus</th>
<th>Name</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Min Clock</th>
<th>Max Clock</th>
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</thead>
<tbody>
<tr>
<td>DQ</td>
<td>DQ/A/BA/cmd</td>
<td>3x dielectric</td>
<td>3x dielectric</td>
<td>4x dielectric</td>
<td>4x dielectric</td>
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<tr>
<td>DQS/CLK</td>
<td>DQ/A/BA/cmd</td>
<td>3x dielectric</td>
<td>3x dielectric</td>
<td>4x dielectric</td>
<td>4x dielectric</td>
</tr>
</tbody>
</table>

- DDR3: DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.
- DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Group</th>
<th>Assignments</th>
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<tbody>
<tr>
<td>MEM_CTRL2CTRL</td>
<td>2:1_SPACING*</td>
</tr>
<tr>
<td>MCP_MEM_COMP</td>
<td>8 MIL*</td>
</tr>
<tr>
<td>MEM_CTRL2MEM</td>
<td>?=2.5:1_SPACING</td>
</tr>
<tr>
<td>MEM_40S</td>
<td>STANDARD* =STANDARD=40_OHM_SE =40_OHM_SE =40_OHM_SE =40_OHM_SE</td>
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### Memory Net Properties

<table>
<thead>
<tr>
<th>Mem Type</th>
<th>Net Type</th>
<th>Properties</th>
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<tr>
<td>MEM_B_CLK</td>
<td>MEM_CLK</td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK_P&lt;5..0&gt;</td>
<td>MEM_70D_VDD</td>
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<tr>
<td>MEM_B_WE_L</td>
<td>MEM_B_CMD</td>
<td></td>
</tr>
<tr>
<td>MEM_B_CAS_L</td>
<td>MEM_B_CMD</td>
<td></td>
</tr>
<tr>
<td>MEM_B_RAS_L</td>
<td>MEM_B_CMD</td>
<td></td>
</tr>
<tr>
<td>MEM_B_BA&lt;2..0&gt;</td>
<td>MEM_B_CMD</td>
<td></td>
</tr>
<tr>
<td>MEM_B_CNTL</td>
<td>MEM_B_ODT&lt;3..0&gt;</td>
<td></td>
</tr>
<tr>
<td>MEM_B_CS_L&lt;3..0&gt;</td>
<td>MEM_CTRL</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_P&lt;7&gt;</td>
<td>MEM_A_DQS7</td>
<td></td>
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<tr>
<td>MEM_A_DQS_N&lt;5&gt;</td>
<td>MEM_A_DQS5</td>
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<tr>
<td>MEM_A_DQS_P&lt;4&gt;</td>
<td>MEM_A_DQS4</td>
<td></td>
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<tr>
<td>MEM_A_DQS_N&lt;3&gt;</td>
<td>MEM_A_DQS3</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_P&lt;2&gt;</td>
<td>MEM_A_DQS2</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;0&gt;</td>
<td>MEM_A_DQS0</td>
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<tr>
<td>MEM_A_DQ_BYTE6</td>
<td>MEM_DATA</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ_BYTE1</td>
<td>MEM_DATA</td>
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<td>MEM_A_DQ&lt;63..56&gt;</td>
<td>MEM_A_DQ_BYTE7</td>
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<td>MEM_A_DQ_BYTE4</td>
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<tr>
<td>MEM_A_DQBYTE3</td>
<td>MEM_DATA</td>
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<td>MEM_A_DQ_BYTE5</td>
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<tr>
<td>MEM_A_DQ&lt;47..40&gt;</td>
<td>MEM_A_DQ_BYTE5</td>
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<td>MEM_A_DQ&lt;31..24&gt;</td>
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<td>MEM_CMD</td>
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<td>MEM_A_CMD</td>
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<tr>
<td>MEM_A_RAS_L</td>
<td>MEM_A_CMD</td>
<td></td>
</tr>
<tr>
<td>MEM_A_BA&lt;2..0&gt;</td>
<td>MEM_A_CMD</td>
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<tr>
<td>MEM_A_CNTL</td>
<td>MEM_A_CS_L&lt;3..0&gt;</td>
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### Memory Net Constraints

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<th>Min Length</th>
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<tbody>
<tr>
<td>MEM_DQS</td>
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<td>MEM_A_DQS6</td>
<td>MEM_70D</td>
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<tr>
<td>MEM_A_DQS_N&lt;6&gt;</td>
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<td>MEM_70D</td>
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<td>MEM_A_DQS_P&lt;4&gt;</td>
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<td>MEM_A_DQS_N&lt;4&gt;</td>
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<td>MEM_A_DQS2</td>
<td>MEM_70D</td>
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<td>MEM_A_DQS_P&lt;0&gt;</td>
<td>MEM_A_DQS0</td>
<td>MEM_70D</td>
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<tr>
<td>MEM_A_DQS_N&lt;0&gt;</td>
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### SPI Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

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### HD Audio Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

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### SMBus Interface Constraints

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### USB 2.0 Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

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<td>CLK</td>
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### PCI Bus Constraints

TABLE матч SPACING RULE ITEM

<table>
<thead>
<tr>
<th>ON LAYER?</th>
<th>LAYER MINIMUM NECK WIDTH (µm)</th>
<th>MAXIMUM NECK LENGTH (µm)</th>
<th>DIFFPAIR PRIMARY GAP (µm)</th>
<th>DIFFPAIR NECK GAP (µm)</th>
<th>PHYSICAL RULE_SET</th>
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<tbody>
<tr>
<td>1</td>
<td>55</td>
<td>55</td>
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</tr>
<tr>
<td>2</td>
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<td>STANDARD</td>
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</tr>
</tbody>
</table>

**Physical Rules**

- **ENET_MDI_100D**: 100 Ohm Differential
- **ENET_MII**: 55 Ohm Differential
- **ENET_RXD**: 55 Ohm Differential
- **ENET_CLOCK**: 55 Ohm Differential
- **ENET_RST**: 55 Ohm Differential
- **ENET_RXD**: 55 Ohm Differential
- **ENET_TXD**: 55 Ohm Differential
- **ENET_MDI**: 100 Ohm Differential
- **ENET_MII**: 100 Ohm Differential
- **ENET_MDC**: 100 Ohm Differential
- **ENET_PWRDWN_L**: 100 Ohm Differential
- **ENET_INTR_L**: 100 Ohm Differential
- **ENET_RESET_L**: 100 Ohm Differential

**Source:** MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

**Other Ethernet Constraints:**

- **ENET_MII_55S**: 55 Ohm Differential
- **ENET_RXD_R<3..0>**: 55 Ohm Differential
- **ENET_CLK125M_TXCLK**: 55 Ohm Differential
- **ENET_TXD**: 55 Ohm Differential
- **ENET_TXD0**: 55 Ohm Differential
- **ENET_TX_CTRLE**: 55 Ohm Differential
- **ENET_RESET**: 55 Ohm Differential
- **ENET_MDI**: 100 Ohm Differential
- **ENET_MDI_P<3..0>**: 100 Ohm Differential
- **ENET_MDI_100D**: 100 Ohm Differential

**Source:** MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4
<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>PHYSICAL SPACING</th>
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<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SDA</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SDA</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
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<td>SMBUS_SMC_MGMT_SDA</td>
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<td>CHGR_CSO_N1TO1_DIFFPAIR</td>
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APPLE INC.

106 OF 109

www.sp860.com  QQ:453100829
## BOARD SPECIFIC SPACING & PHYSICAL CONSTRAINTS

<table>
<thead>
<tr>
<th>BOARD LAYER</th>
<th>PHYSICAL_RULE_SET</th>
<th>AREA_TYPE</th>
<th>NET_PHYSICAL_TYPE</th>
<th>PHYSICAL_RULE_ASSIGNMENT</th>
<th>NAME</th>
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</table>

### 110_OHM_DIFF

- **YISL3, ISL4, ISL9, ISL10**
  - **0.330 MM**
  - **0.075 MM**

### 100_OHM_DIFF

- **TOP, BOTTOM**
  - **0.230 MM**
  - **0.091 MM**

### 50_OHM_SE

- **27P4_OHM_SE**
  - **TOP, BOTTOM**
  - **0.222 MM**
  - **0.076 MM**

### 90_OHM_DIFF

- **TOP, BOTTOM**
  - **0.234 MM**
  - **0.095 MM**

### 40_OHM_SE

- **TOP, BOTTOM**
  - **0.100 MM**
  - **0.126 MM**

### 70_OHM_DIFF

- **TOP, BOTTOM**
  - **0.224 MM**
  - **0.151 MM**

### 30 MM

- **TOP, BOTTOM**
  - **0.100 MM**
  - **0.090 MM**

### 4X_DIELECTRIC

- **TOP, BOTTOM**
  - **0.252 MM**

### 3X_DIELECTRIC

- **TOP, BOTTOM**
  - **0.210 MM**

### 2X_DIELECTRIC

- **TOP, BOTTOM**
  - **0.140 MM**

### 1.5:1_SPACING

- **TOP, BOTTOM**
  - **0.15 MM**

### 2:1_SPACING

- **TOP, BOTTOM**
  - **0.2 MM**

### 0.280 MM

- **TOP, BOTTOM**
  - **0.210 MM**

### 0.140 MM

- **TOP, BOTTOM**
  - **0.100 MM**

### 3:1_SPACING

- **TOP, BOTTOM**
  - **0.3 MM**

### BGA_P1MM

- **TOP, BOTTOM**
  - **0.090 MM**

### BGA_P2MM

- **TOP, BOTTOM**
  - **0.150 MM**

### BGA_PCIE

- **TOP, BOTTOM**
  - **0.100 MM**

### MEM_CLK

- **TOP, BOTTOM**
  - **0.090 MM**

### MEM_40S

- **TOP, BOTTOM**
  - **0.090 MM**

### MEM_40S_VDD

- **TOP, BOTTOM**
  - **0.090 MM**

### CLK_PCIE

- **TOP, BOTTOM**
  - **0.100 MM**

### CLK_PCI

- **TOP, BOTTOM**
  - **0.100 MM**

### CLK_FSB

- **TOP, BOTTOM**
  - **0.100 MM**

### FSBDSTB

- **TOP, BOTTOM**
  - **0.100 MM**

### BGA_P1MM

- **TOP, BOTTOM**
  - **0.100 MM**

### BGA_P2MM

- **TOP, BOTTOM**
  - **0.100 MM**

### BGA_P3MM

- **TOP, BOTTOM**
  - **0.100 MM**

### 1.5:1_SPACING

- **TOP, BOTTOM**
  - **0.15 MM**

### 2:1_SPACING

- **TOP, BOTTOM**
  - **0.2 MM**

### 0.280 MM

- **TOP, BOTTOM**
  - **0.210 MM**

### 0.140 MM

- **TOP, BOTTOM**
  - **0.100 MM**