2. All capacitance values are in microfarads.

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Schematic / PCB #s
### BOM Configuration

**K86/K87 Board Stack-Up**

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<td>Signal (High Speed)</td>
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<tr>
<td>11</td>
<td>Ground</td>
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</table>

**Bottom**

**Signal**

12 **Signal (High Speed)**

---

### Part Substitutions (differences with K6/K69)

- **MCP83M**
  - **K87 Specific**
  - **MCP89M:A02**

---

### Bar Code Labels / EEE #'s

- **826-4393**
  - **1**
  - **LBL, P/N Label, PCB, 28MM x 6MM [EEEE:DCV2]**
  - **Critical**

---

### Part Numbers

- **353S2811**
  - **NEW IMPROVED INTERSIL PART AS ALTERNATE**
- **138S0603**
  - **MURATA AS ALTERNATE**
- **152S0693, 152S0778, 152S0685, 152S0796**

---

### Module Parts

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<td>U1000 CRITICAL</td>
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---

### Development BOM

- **K86_K87_DEBUG**: PROD
- **VREFMRGN**: NO
- **BMON**: PROD
- **SENS_R**: PROD
- **PROJECT_PHASE**: DEVELOPMENT_BOM

---

### Bar Code Labels / EEE #'s

- **826-4393**
  - **1**
  - **LBL, P/N Label, PCB, 28MM x 6MM [EEEE:DCV3]**
  - **Critical**

---

### BOM Groups (always-present)

- **Module Parts**

---

### BOM Groups (project phase-dependent)

- **K86_K87_DEBUG**: PROD
- **VREFMRGN**: NO
- **BMON**: PROD
- **SENS_R**: PROD
- **PROJECT_PHASE**: DEVELOPMENT_BOM

---

### LED: K86_K87

- **R5714**
  - **RES, MTL FILM, 1/16W, 113 OHM, 1, 0402, SMD, LF**

---

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### Page Title

- **SYNC_MASTER=K87_MLB**

---

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- **A.0.0**
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---

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Revision History

2010-02-25: 2.19.0
2010-02-18: 2.16.0
2010-02-15: 2.10.0
2010-02-15: 2.9.0
2010-02-02: 2.8.0
2010-01-28: 2.7.0
2010-01-22: 2.6.0

*** Resynced Audio pages with the following changes:

- Added L4530, L4531 (APN 155S0137) to SIL connector pins
  - pg. 67, no stuffed R6712 and R6713
  - pg. 66, added C6602
- Added row to EEE table for E3T
- CSA 4: Per <rdar://problem/7571786> K86/K87: Add E3T EEE code for K86 to schematic
- Changed L3720 to 152S1182 (IND,PWR,SHD,4.7UH,20%,0.91A,31X31X12MM) for lower ESR
- CSA 37: Per <rdar://problem/7554342> K86/K87: Change L3720 to 152S1182

CSA 97: U9700 changed to APN 353S2965
CSA 12: For K86 only: C1272 = 330uF added.
CSA 70: R7015 changed to 56.2K, C7015 changed to 1000pF, C7042 changed to 0.068uF
CSA 75: R7572 changed to 147K

*** Started syncing with K6

Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD

Changed BOM group structure to match that in the radar (see PDF attached to radar)
Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes)
Cleaned up text notes for 1phase, 2phase, and edp #s per radar request.

CSA 74, CSA 79:
Keeping K86 and K87 pgs identical for CSA 74, modifying BOM table for IMVP1 phase on K87's schematic to reflect changes for K86.
Changed all instances of K87_DEVEL_xxxx to K87_DEVEL:xxxx

Changed J5100 BOMOPTION from LPCPLUS to LPCPLUS_CON to unstuff connector at DVT

CSA 4: Cosmetic: changed text sizes and alignment

Unchanged:

Removed:

BKLT:ENG        ==>     BKLT:PROD

Diff from the two changes above:

Changed 085-1093 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG
Per <rdar://problem/7540522> K86/K87: Production Debug Components

CSA 45: Per <rdar://problem/7524364> K86/K87: change SATA HDD D2R passive EQ values

CSA 70: Per <rdar://problem/7519048> K86/K87: Change U7000 to 353S2929
Need to resync with T27 once the change has been made there

Updated Q2355 and Q2356 with new schematic symbols

SMC_TMS
CSA 7: Per <rdar://problem/7517432> K86/K87 functional net property needed on signals in schematics

Changed BOMOPTION for R7872 from S0PGOOD_ISL to NOSTUFF

CSA 78: Per <rdar://problem/7495000> K87: Add NOSTUFF to R7872 to disconnect U7870 from ALL_SYS_PWRGD

- BOM: 639-0680

"Assembly APN: 339S0114
Added text note with part numbers for components of the assembly
Deleted OMIT BOMOPTION from J6955
Deleted BOM table for Hall effect assembly
Created SMC:PROG_K86 pointing to 341T0250 (SUBASSY, IC, SMC, K86)
Removed table entry that says 376S0868 is an alternate for 376S0624
Added LED:K86_K87 BOMOPTION to the K87_MISC BOM group
BOMOPTION is "MCP83M"
This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86

Updated DLY text note for U3440 to match T27

CSA 4: Added BOM table to substitute in parts that have BOMOPTION xxx:K6_K69 (to allow sync with T27)

*** Other changes

CSA 25: T27: Removed R2575 & R2580 per DG v1.3 (pg. 25). per <radar:7459260 > Design Guide v1.3 updates
R5714 has BOMOPTION LED:K6_K69, and we need to substitute a different part on csa 4

CSA 57: Began syncing from T27 per <radar:7304029 > T27 schematic bom option for R5714 & R5030 to keep K87 in sync
T27: Changed RC balance on BATT_ISENSE, same time constant (pg. 54).
T27: Added gain note for U5402 and SMC_BATT_ISENSE (pg. 54).

CSA 54: Began syncing from T27 per <radar:7432091 > BATT_ISENSE filter change to address lower max sink current on ISL6259 BMON pin (K17 auto-shutdown issue)
CSA 29,31: Began syncing from T27 per <radar:7424246 > BOM: K87 needs omit on J3100 and J2900 from T27

CSA 4: Deleted entry in Module Parts table for R6612, R6617, R6630, R6633 since they were removed when we switched from piezo to dynamic speakers

Cosmetic cleanup

Changed C7428 from 0.47uF => 0.33uF (132S0101) per Intersil

CSA 74: Changed C7434 from NOSTUFF to IMVP6:2PHASE per Intersil

CSA 34: Deleted net properties for =PP3V3_S3_WLAN
=PPSPD_S0_MEM_B'
=PP5V_S0_HDD'

STILL NEED TO UPDATE VALUE OF C7428!

C7414 = 1000pF  10% (132S0045)
C7428 = 0.22uF  10% (132S0102)

Added BOM table to insert the following APNs for IMVP6:1PHASE:

Added IMVP6:2PHASE to the following components:

Implemeted different stuffing options for 1-phase vs 2-phase:

2010-01-18: 2.4.0
2010-01-06: 1.11.0
2009-12-07: 1.2.0
10/1/2009:

Revision History

Apple Inc. 051-8407

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP89-SPECIFIC PINOUT

Direction of XDP module

Direction of XDP module

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PE0 ports are Gen2-capable. 4 RCs: 4x, x3, x2, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[0:3] and PE1[0:1] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND
If PE0[4:5] and PE1[0:1] are not used, +VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND
If PE0[3:0] are not used,

+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND
If PE0[4:5] and PE1[0:1] are not used,

+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND
If PE0[0:3] and PE1[0:1] are not used,

NOTE: Only pull-ups are necessary.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_P.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_N.

NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_P.

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NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN1_N.

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NOTE: 100K pull-downs required if DP_AUX_CHAN1 is used for DP_IG_AUX_CHAN0_P.
All other pins can be left TP or NC.
Connect RGMII_MDIO to 10K pull-down.
Connect RGMII_VREF to 10K pull-down.
RGMII_COMP_VDD/_GND must remain connected as shown.
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
Connect RGMII_RXCTL to 10K pull-down.
Internal MAC Disable:
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
Connect RGMII_RXD0 to 10K pull-down.
Connect RGMII_RXD3 to 10K pull-down.
All other pins can be left TP or NC.
NOTE: "SM" rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.

NOTE: VDD_COREA_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators. The VDD_COREA_SENSE point as close to COREF питания as possible.
Q2300 helps reduce input rail droop during Q2300 turn-on.

**DIMM CKE Clamps**

CKE must be held low to keep memory in self-refresh. Clamps enable after MCP89 MEMVDD is up and CKEs are driven by MCP89. Clamps prevent noise on CKE signals. Use a 4.7K ohm resistor on each CKE signal on DIMM.

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.
Approx. Ramp Time (EN to 1V, uS): \(43.9 + 0.6943 \times C_1\) (pF)

- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1300 uS (10% to 90%)
- PTE Rise = 2.5 milliseconds

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW
RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

System Reset Circuit

Platform Reset Connections
LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

DO NOT SYNC WITH T27, REMOVED PCIE RESET SIGNALS +CAESAR XTAL

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REVISION

DRAWING NUMBER SIZE

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Apple Inc.

051-8407 G

A.0.0

SYNC_DATE=02/26/2010SYNC_MASTER=K87_MLB

www.vinafix.vn
Configuration Settings:

- ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.
- designs must ensure PHY in powered absence ENET rails are, or use separate crystal.
- DO NOT SYNC, EXTERNAL 1.05V REGULATOR OPTION
NOTE: 3.3V must be 3.3V if 3.3V or 5V to ensure the drive is unpowered in S3/S5.

Resistors should be on inside, with SATA passing straight through.

Use 0-ohm resistors and M0.01UF caps if not using Passive de-emphasis filter.

The drive is unpowered in S3/S5.

Ensure the drive is unpowered in S3/S5.

Passive de-emphasis filter should not be used. Use 0-ohm resistors and M0.01UF caps if not using Passive de-emphasis filter.

The drive should not be powered in S3/S5.

Ensure the drive is unpowered in S3/S5.

Passive de-emphasis filter should not be used. Use 0-ohm resistors and M0.01UF caps if not using Passive de-emphasis filter.
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
NOTE: Internal pull-ups are to VIN, not V+.

MR1* and MR2* must both be low to cause manual reset. Use no resistors to support SMC reset via keyboard.

SMC Pull-ups

SMC Pull-downs

SMC Crystal Circuit

Debug Power "Buttons"

System (Sleep) LED Circuit
**CPU Voltage Sense / Filter**

- **XW535**
  - Place RC close to SMC

**MCP Voltage Sense / Filter**

- **XW535**
  - Place RC close to SMC

**PBUS Voltage Sense Enable & Filter**

- **R5315**
  - Place RC close to SMC divider when high.

- **R5316**
  - Place RC close to SMC

- **R5315**
  - Place RC close to SMC

- **R5316**
  - Place RC close to SMC

- **R5385**
  - Place RC close to SMC

- **R5386**
  - Place RC close to SMC

**Voltage Sensing**

- **PPBUS_G3H**
  - **PPBUS_G3H_VSENSE**
  - **PPVCORE_S0_MCP**
  - **MCPVSENSE_IN**
  - **CPUVSENSE_IN**

- **SMC_MCP_VSENSE**
  - **GND_SMC_AVSS**
  - **SMC_CPU_VSENSE**

- **SMC_PBUS_VSENSE**
  - **GND_SMC_AVSS**

---

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801-8407 02 09.0

SYNC_DATE=02/26/2010

SYNC_MASTER=K87_MLB

- www.vinafix.vn
DETECT HDD TEMPERATURE

DETECT CPU DIE TEMPERATURE

DETECT FIN-STACK TEMPERATURE

PLACEMENT NOTE: PLACE CLOSE TO J4501 IN A CONVENIENT LOCATION

PLACEMENT NOTE: PLACE CLOSE TO HEADER CPU

PLACEMENT NOTE: PLACE CLOSE TO HEADER MCP
PSOC USB CONTROLLER

- SSN TO Z2
- TRACKPAD STROBE
- KEYBOARD SCANNER

---

**Keyboard Connector**

---

**SMC Manual Reset & Isolation**

Left shift, option & control keys combined with power button cause SMC reset assertion. Keys added with PSOC power to isolate when PSOC is not powered.

---

DEVICE NAME: SMC

---

**TPAD Buttons Disable**

- BUTTON DISABLE
-(strcmp
- (("SMC")
- SMAPM2(K6)
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BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROP LINE REGULATION
- RIPPLE TO MEET ERS
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

BOOSTER +18.5VDC FOR SENSORS

- POWER CONSUMPTION
- DROP LINE REGULATION
- RIPPLE TO MEET ERS
- STARTUP TIME LESS THAN 2MS

R5812,R5813,C5818 MODIFIED

CRITICAL

C5816

10%
X7R-CERM
402
0.1UF
16V
C5817

16V
2.2UF
603
X5R
10%
C5818

18.5V
402
MF-LF
1/16W
1%
1M
R5812

71.5K
1%
1/16W
MF-LF
402
R5813

5K
1%
1/16W
MF-LF
402

IPD Flex Connector

DO NOT SYNC FROM T27. REMOVED KEYBOARD BACKLIGHT CIRCUIT

CRITICAL

M-ST-SM
55560-0228
J5800
B0520WSXG
SOD-323
CRITICAL

D5802
25V
1UF
603-1
X5R
10%
C5819

10%
X7R-CERM
402
0.1UF
16V
C5816
16V
2.2UF
603
X5R
10%
C5817

18.5V
402
MF-LF
1/16W
1%
1M
R5812

71.5K
1%
1/16W
MF-LF
402
R5813

402

58 OF 109
051-8407
44 OF 76

www.vinafix.vn
Analog SMS

C5923: 0.033μF 16V 10% 402X5R
C5924: 0.033μF 16V 10% 402X5R
C5925: 0.033μF 16V 10% 402X5R

R5921: PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

C5923-5925 CAP VALUES WILL BE USED TO GET CUTOFF FREQUENCY OF ~146HZ

PLACE NEARS:
PLACE_NEAR=U4900.M10:2.54MM 0.033UF C5923
PLACE_NEAR=U4900.N9:2.54MM 0.033UF C5924
PLACE_NEAR=U4900.K10:2.54MM 0.033UF C5925

DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923, C5924, C5925. ADDED PLACE NEARS

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SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010 SMS
SMS_Z_AXIS SMS_Y_AXIS SMS_X_AXIS
SMS_ONOFF_L SMS_PWRDN
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
PP3V3_S3_SMS_FILT
PP3V3_S3_SMS

www.vinafix.vn
NOTE: If HOLD* is asserted ROM will ignore SPI cycles.

NOTE: 42 & 62 MHz use FAST_READ command.

MCP89 SPI Frequency Select:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>MOSI</th>
<th>CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>25.0 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>31.2 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>41.7 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>62.5 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

* NOTE: 42 & 62 MHz use FAST_READ command.
4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2281

NOTES ON CODEC I/O
DIFF INPUT: 2.0Vpp CLR: 0.5Vpp DIFF: 500kHz-5MHz
SE INPUT: 1.22Vpp CLR: 1Vpp SE: 500kHz-5MHz
DAC/2FS OUTPUTS: 1.34VRMS
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.20K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC HP = 3.6 HZ
FC LP = 43KHZ
VIN = 2V RMS, CODEC VIN = 1.14 VRMS

CODEC RIN = 20K OHMS
NET RIN = 10.20K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC HP = 3.6 HZ
FC LP = 43KHZ
VIN = 2V RMS, CODEC VIN = 1.14 VRMS
SATELLITE 796Hz < HPF FC < 936Hz
SUB 80 Hz < HPF FC < 94 Hz
GAIN 6DB (2V/V)
SPRK AMP. INPUT REFERRED CLIP POINT = ~6dBFS
PWM FREQ. = 300 KHZ

PLACE_NEAR=L7260.1:1.5 MM

C7280 39UF-0.027OHM

C7282 0.001UF 20%

C7281 1UF 10%

C7270 10UF 6.3V X5R 20%

C7283 0.001UF 20%

C7290 10UF 6.3V X5R 20%

C7291 220UF D1A-SM 6.3V 20%

PWM FREQ. = 375 KHZ

PLACE_NEAR=U7200.6:1 MM

C7220 0.1UF CERM 50V 20%

C7271 1UF X5R 25V 10%

C7272 1UF X5R 25V 10%

C7273 10UF 6.3V X5R 20%

C7251 150UF 20%

C7252 1UF X5R 25V 10%

C7253 402 50V 20%

C7242 402

C7240 39UF-0.027OHM CRITICAL

B1A-SM 16V POLY 20%

R7266 10K 1% MF-LF 1/16W

R7267 62 IN 1/16W 86.6K

R7268 10K 1% MF-LF 1/16W

R7269 10K 1% MF-LF 1/16W

R7270 10K 1% MF-LF 1/16W

R7271 10K 1% MF-LF 1/16W

R7272 56 IN 402

R7273 10K 1% MF-LF 1/16W

R7220 100K 5% 1/16W

RJK0384DPA WPAK

PCMC063T-SM

L7220

PCMC104E4R7-SM

5V/3.3V SUPPLY

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.

NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

THE POSSESSOR AGREES TO THE FOLLOWING:

SPC: 051-8407

051-8407-A.0.0

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www.vinafix.vn
1.5V/0.75 DDR3 POWER SUPPLY

NOTE: DONT SYNC THIS PAGE FROM K6 REMOVED R7380
NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS

62
8
157
DDRREG_PGOOD
CRITICAL
X5R-CERM
6.3V20%
1
8
X5R-CERM
Vout = VDDQSNS/2
10mA max load
805
10%
0.033UF
C7305
MF-LF
1/16W
10%
5%
402-1
X5R
VOLTAGE=0V
MIN_NECK_WIDTH=0.17 mm
MIN_LINE_WIDTH=0.6 mm
PP5V_S3_DDRREG_V5FILT
PLACE_NEAR=U7300.3:1 mm
12
24
13
10
7
5
S5
S3
1.5V/0.75 DDR3 POWER SUPPLY
VDDQ PGOOD
=PPVIN_S0_DDRREG_LDO
25
22
4
8
6
0
29
DIDT=TRUE
GATE_NODE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
SWITCH_NODE=TRUE
DDRREG_LL
39UF-0.027OHM
20%
MF-LF
402
1%
C7355
603
PLACE_NEAR=U7300.25:1 mm
VLDOINV5FILTV5IN
VDDQSET
VDDQSNSCOMP
23
DIDT=TRUE
MIN_NECK_WIDTH=0.17 mm
BEGIN_SCAN
PLACE_NEAR=Q7335.1:1 mm
2
1
PLACE_NEAR=Q7330.5:1.5 MM
C7332
1UF
603-1
10%
XW7335
1 2
1 2
X5R
10%
2
C7333
10%
D
321
CRITICAL
Q7330
SIS424DN
PWRPK-1212-8-SM
SIS426DN
PWRPK-12128
CRITICAL
L7330
CASE-B2-SM
2.5V
330UF
2.5V
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
THE POSSESSION AGREES TO THE FOLLOWING:
PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
FOUR GROUND VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY.
13.3 Inch, K84 Panel (9 LEDs per string)

TARGET: ISET = 20mA, OVP = 35V
ACTUAL: ISET = 153mA / \langle\text{Riset}\rangle

MIN_LINE_WIDTH = 0.2 mm
MIN_NECK_WIDTH = 0.2 mm

10.2 ohm resistors for current measurement on LED strings.

DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

DO NOT REPRODUCE OR COPY IT
FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Layer</th>
<th>Routing Type</th>
<th>Route Height</th>
<th>Route Width</th>
<th>Route Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CPURST_L</td>
<td>1</td>
<td>2:1_DIFFPAIR</td>
<td>2</td>
<td>2</td>
<td>2:1_DIFFPAIR</td>
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</table>

CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Pin 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CPURST_L</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>

FSB Clock Constraints

<table>
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<th>Layer</th>
<th>Routing Type</th>
<th>Route Height</th>
<th>Route Width</th>
<th>Route Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_MCP</td>
<td>1</td>
<td>2:1_DIFFPAIR</td>
<td>2</td>
<td>2</td>
<td>2:1_DIFFPAIR</td>
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</tbody>
</table>

MCP FSB COMP Signal Constraints

<table>
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<tr>
<th>Signal Name</th>
<th>Layer</th>
<th>Routing Type</th>
<th>Route Height</th>
<th>Route Width</th>
<th>Route Weight</th>
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</thead>
<tbody>
<tr>
<td>MCP_CPU_COMP</td>
<td>1</td>
<td>2:1_DIFFPAIR</td>
<td>2</td>
<td>2</td>
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</tbody>
</table>

CPU Signal Constraints

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<th>Route Width</th>
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<tr>
<td>CPU_VCCSENSE</td>
<td>1</td>
<td>2:1_DIFFPAIR</td>
<td>2</td>
<td>2</td>
<td>2:1_DIFFPAIR</td>
</tr>
</tbody>
</table>

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.
**NEED PCIe Gen1/Gen2 notes!**

### Analog Video Signal Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>Min Width</th>
<th>Min Trace</th>
<th>Max Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSYNC</td>
<td>0.25</td>
<td>0.25</td>
<td>0.4</td>
</tr>
<tr>
<td>HSYNC</td>
<td>0.25</td>
<td>0.25</td>
<td>0.4</td>
</tr>
</tbody>
</table>

**Digital Video Signal Constraints**

<table>
<thead>
<tr>
<th>Port</th>
<th>Min Width</th>
<th>Min Trace</th>
<th>Max Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMDS_IG_TXD_P&lt;5..0&gt;</td>
<td>0.25</td>
<td>0.25</td>
<td>0.4</td>
</tr>
</tbody>
</table>

**SATA Interface Constraints**

<table>
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<tr>
<th>Port</th>
<th>Max Width</th>
<th>Min Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data_Tx</td>
<td>0.6</td>
<td>0.3</td>
</tr>
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</table>

### MCP89 Net Properties

<table>
<thead>
<tr>
<th>Port</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>3.3V</td>
</tr>
<tr>
<td>GND</td>
<td>0V</td>
</tr>
</tbody>
</table>

**PCI-Express**

<table>
<thead>
<tr>
<th>Port</th>
<th>Min Width</th>
<th>Min Trace</th>
<th>Max Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIE_90D</td>
<td>0.25</td>
<td>0.25</td>
<td>0.4</td>
</tr>
</tbody>
</table>

**DisplayPort/TMDS intra-pair matching should be 5 ps.**

**Inter-pair matching should be within 100 ps.**

**DisplayPort AUX CH intra-pair matching should be 5 ps.**

**No relationship to other signals.**

**LVDS intra-pair matching should be 5 mils.**

**Pairs should be matched within 100 mils.**

**Source:** MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

**PCI-Express**

<table>
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<tr>
<th>Port</th>
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<tbody>
<tr>
<td>PCIE_90D</td>
<td>3.3V</td>
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</table>

**LVDS_IG_A_DATA3 LVDS_100D LVDS_IG_B_CLK_P LVDS_IG_B_CLK_N LVDS_IG_A_CLK_P LVDS_IG_A_CLK_N**

**Source:** MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6
### K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

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